TEXAS INSTRUMENTS
INA301-Q1
JAJSNR9B – APRIL 2016 – REVISED APRIL 2022

INA301-Q1、36V、車載用、高速、ゼロドリフト、電圧出力、高速、過電流保護コンパレータ搭載電流シャント・モニタ

1 特長

- 車載アプリケーション認定済み
- 下記内容で AEC-Q100 認定済み:
  - デバイス温度グレード 1:–40℃～+125℃の動作時周囲温度範囲
  - デバイス HBM ESD 分類レベル 2
  - デバイス CDM ESD 分類レベル C6
- 機能安全対応
  - 機能安全システムの設計に役立つ資料を利用可能
- 広い同相入力範囲:0V～36V
- デュアル出力:アンプ / コンパレータ出力
- 高精度アンプ:
  - オフセット電圧:35µV (最大値)
  - オフセット電圧ドリフト:0.5µV/℃以下
  - ゲイン誤差:0.1% (最大値)
  - ゲインの温度特性:10ppm/℃
- アンプ・ゲインを選択可能:
  - INA301A1-Q1:20V/V
  - INA301A2-Q1:50V/V
  - INA301A3-Q1:100V/V
- 1 つの抵抗で設定するプログラマブルなアラート・スレッショルド
- アラート応答時間の合計:1µs
- 透過モードとラッチ・モードの両方のオープン・ドレイン出力
- パッケージ:VSSOP-8

2 アプリケーション

- ソレノイド制御
- ローサイド・モーター監視
- 電動パワー・ステアリング
- パワー・シート
- パワー・ウィンドウ
- 車体制御モジュール
- 電子制御ユニット
- 過電流保護
- eFuse

3 概要

INA301-Q1 には、大きい同相電圧の、電流センシング・アンプと、高速コンパレータの両方が搭載されています。コンパレータは、電流センシングまたは電流シャント抵抗の両端に発生する電圧を測定し、その電圧と、コンパレータの基準ピンにより設定される定義済みのスレッショルド制限とを比較して、過電流保護を実現するよう構成されています。このデバイスは、外付けの制限設定抵抗 1 つで、スレッショルド範囲を設定できます。この電流シャント・モニタは、電源電圧にかかわらず、0V から 36V まで変動する同相電圧上で差動電圧信号を測定できます。

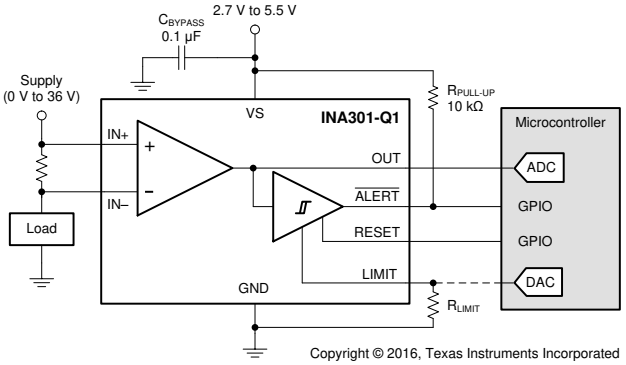
オープン・ドレインのアラート出力があり、透過モード (出力ステータスが入力状態に従う) またはラッチ・モード (ラッチがリセットされたときにアラート出力がクリアされる) で動作するよう構成できます。デバイスのアラートの応答時間は 1µs 未満で、過電流イベントを迅速に検出できます。

このデバイスは 2.7V～5.5V の単一電源で動作し、最大消費電流は 700µA です。このデバイスは、拡張動作温度範囲の -40℃～+125℃で動作が規定されており、8 ピンの VSSOP パッケージで供給されます。

製品情報(1)

部品番号	パッケージ	本体サイズ (公称)
INA301-Q1	VSSOP (8)	3.00mm × 3.00mm

(1) 利用可能なパッケージについては、データシートの末尾にあるパッケージ・オプションについての付録を参照してください。



代表的なアプリケーション

英語版の TI 製品についての情報を翻訳したこの資料は、製品の概要を確認する目的で便宜的に提供しているものです。該当する正式な英語版の最新情報は、www.ti.com で閲覧でき、その内容が常に優先されます。TI では翻訳の正確性および妥当性につきましては一切保証いたしません。実際の設計などの前には、必ず最新版の英語版をご参照くださいますようお願いいたします。

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4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision A (June 2016) to Revision B (April 2022)	Page
• 機能安全の情報を追加	1
• Changed the *Power Supply Recommendations* section	25

Changes from Revision * (April 2016) to Revision A (June 2016)	Page
• 「製品プレビュー」から「量産データ」に変更	1

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5 Pin Configuration and Functions

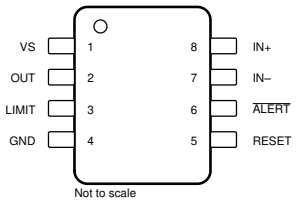


図 5-1. DGK Package 8-Pin VSSOP Top View

表 5-1. Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
1	VS	Analog	Power supply, 2.7 V to 5.5 V
2	OUT	Analog output	Output voltage
3	LIMIT	Analog input	Alert threshold limit input; see the *セクション 7.3.2* section for details on setting the limit threshold.
4	GND	Analog	Ground
5	RESET	Digital input	Transparent or latch mode selection input
6	$\overline{\text{ALERT}}$	Digital output	Overlimit alert, active-low, open-drain output
7	IN–	Analog input	Negative voltage input. Connect to load side of the shunt resistor.
8	IN+	Analog input	Positive voltage input. Connect to supply side of the shunt resistor.

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Supply voltage, V_S			6	V
Analog inputs (IN+, IN–)	Differential (V_{IN+}) – ($V_{IN–}$)(2)	–40	40	V
	Common-mode(3)	GND – 0.3	40	
Analog input	LIMIT pin	GND – 0.3	(V_S) + 0.3	V
Analog output	OUT pin	GND – 0.3	(V_S) + 0.3	V
Digital input	RESET pin	GND – 0.3	(V_S) + 0.3	V
Digital output	$\overline{\text{ALERT}}$ pin	GND – 0.3	6	V
Operating temperature, T_A		–55	150	°C
Junction temperature, T_J			150	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) V_{IN+} and $V_{IN–}$ are the voltages at the IN+ and IN– pins, respectively.
(3) Input voltage can exceed the voltage shown without causing damage to the device if the current at that pin is limited to 5 mA.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{CM}	Common-mode input voltage		12		V
V_S	Operating supply voltage	2.7	5	5.5	V
T_A	Operating free-air temperature	–40		125	°C

6.4 Thermal Information

THERMAL METRIC(1)		INA301-Q1 DGK (VSSOP) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	161.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	62.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	81.4	°C/W
ψ_{JT}	Junction-to-top characterization parameter	6.8	°C/W
ψ_{JB}	Junction-to-board characterization parameter	80	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

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6.5 Electrical Characteristics

at T_A = 25°C, V_{SENSE} = V_{IN+} – $V_{IN–}$ = 10 mV, V_S = 5 V, V_{IN+} = 12 V, and V_{LIMIT} = 2 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT						
V_{CM}	Common-mode input voltage range		0		36	V
V_{IN}	Differential input voltage range	V_{IN} = V_{IN+} – $V_{IN–}$, INA301A1-Q1	0		250	mV
		V_{IN} = V_{IN+} – $V_{IN–}$, INA301A2-Q1	0		100	
		V_{IN} = V_{IN+} – $V_{IN–}$, INA301A3-Q1	0		50	
CMR	Common-mode rejection	INA301A1-Q1, V_{IN+} = 0 V to 36 V, T_A = –40°C to +125°C	100	110		dB
		INA301A2-Q1, V_{IN+} = 0 V to 36 V, T_A = –40°C to +125°C	106	118		
		INA301A3-Q1, V_{IN+} = 0 V to 36 V, T_A = –40°C to +125°C	110	120		
V_{OS}	Offset voltage, RTI(1)	INA301A1-Q1		±25	±125	µV
		INA301A2-Q1		±15	±50	
		INA301A3-Q1		±10	±35	
dV_{OS}/dT	Offset voltage drift, RTI(1)	T_A= –40°C to +125°C		0.1	0.5	µV/°C
PSRR	Power-supply rejection ratio	V_S = 2.7 V to 5.5 V, V_{IN+} = 12 V, T_A = –40°C to +125°C		±0.1	±10	µV/V
I_B	Input bias current	I_{B+}, $I_{B–}$		120		µA
I_{OS}	Input offset current	V_{SENSE} = 0 mV		±0.1		µA
OUTPUT						
G	Gain	INA301A1-Q1		20		V/V
		INA301A2-Q1		50		
		INA301A3-Q1		100		
	Gain error	INA301A1-Q1, V_{OUT} = 0.5 V to V_S – 0.5 V		±0.03%	±0.1%	
		INA301A2-Q1, V_{OUT} = 0.5 V to V_S – 0.5 V		±0.05%	±0.15%	
		INA301A3-Q1, V_{OUT} = 0.5 V to V_S – 0.5 V		±0.11%	±0.2%	
		T_A= –40°C to 125°C		3	10	ppm/°C
	Nonlinearity error	V_{OUT} = 0.5 V to V_S – 0.5 V		±0.01%		
	Maximum capacitive load	No sustained oscillation		500		pF
VOLTAGE OUTPUT						
	Swing to V_S power-supply rail	R_L = 10 kΩ to GND, T_A = –40°C to +125°C		V_S – 0.05	V_S – 0.1	V
	Swing to GND	R_L = 10 kΩ to GND, T_A = –40°C to +125°C		V_{GND} + 20	V_{GND} + 30	mV
FREQUENCY RESPONSE						
BW	Bandwidth	INA301A1-Q1		550		kHz
		INA301A2-Q1		500		
		INA301A3-Q1		450		
SR	Slew rate			4		V/µs
NOISE, RTI(1)						
	Voltage noise density			30		nV/√Hz

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at T_A = 25°C, V_{SENSE} = V_{IN+} – $V_{IN–}$ = 10 mV, V_S = 5 V, V_{IN+} = 12 V, and V_{LIMIT} = 2 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
COMPARATOR						
t_p	Total alert propagation delay	Input overdrive = 1 mV		0.75	1	µs
	Slew-rate-limited t_p	V_{OUT} step = 0.5 V to 4.5 V, V_{LIMIT} = 4 V		1	1.5	
I_{LIMIT}	Limit threshold output current	T_A = 25°C	79.7	80	80.3	µA
		T_A = –40°C to +125°C	79.2		80.8	
V_{OS}	Comparator offset voltage	INA301A1-Q1		1	3.5	mV
		INA301A2-Q1		1	4	
		INA301A3-Q1		1.5	4.5	
V_{HYS}	Hysteresis	INA301A1-Q1		20		mV
		INA301A2-Q1		50		
		INA301A3-Q1		100		
V_{IH}	High-level input voltage		1.4		6	V
V_{IL}	Low-level input voltage		0		0.4	V
V_{OL}	Alert low-level output voltage	I_{OL} = 3 mA		70	300	mV
	$\overline{\text{ALERT}}$ pin leakage input current	V_{OH} = 3.3 V		0.1	1	µA
	Digital leakage input current	0 ≤ V_{IN} ≤ V_S		1		µA
POWER SUPPLY						
I_Q	Quiescent current	V_{SENSE} = 0 mV, T_A = 25°C		500	650	µA
		T_A = –40°C to +125°C			700	

(1) RTI = referred-to-input.

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6.6 Typical Characteristics

at T_A = 25°C, V_S = 5 V, V_{IN+} = 12 V, and alert pullup resistor = 10 kΩ (unless otherwise noted)

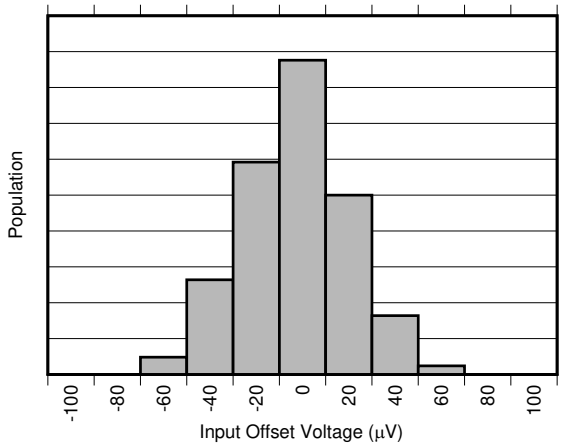


図 6-1. Input Offset Voltage Distribution (INA301A1-Q1)

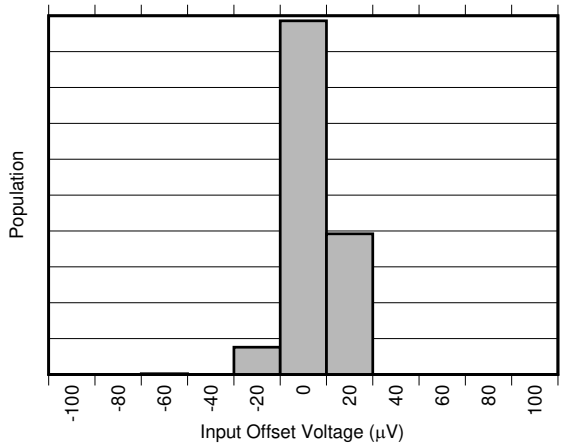


図 6-2. Input Offset Voltage Distribution (INA301A2-Q1)

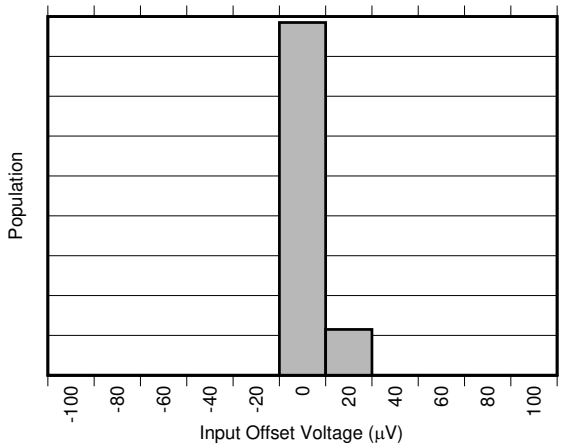


図 6-3. Input Offset Voltage Distribution (INA301A3-Q1)

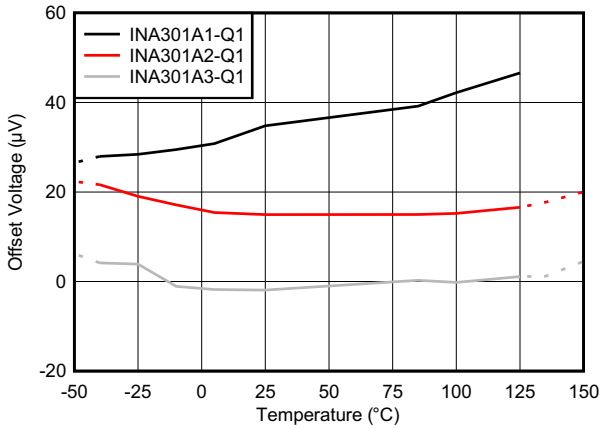


図 6-4. Input Offset Voltage vs. Temperature

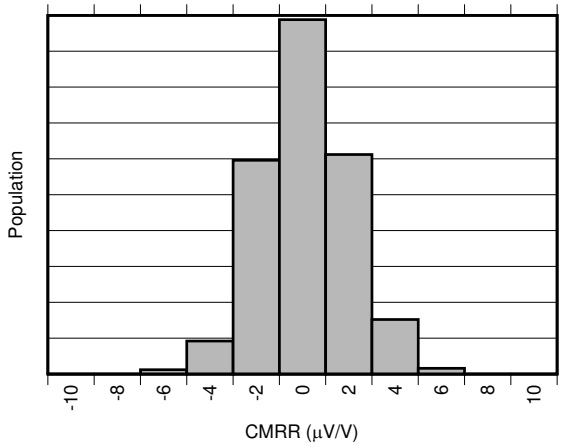


図 6-5. Common-Mode Rejection Ratio Distribution (INA301A1-Q1)

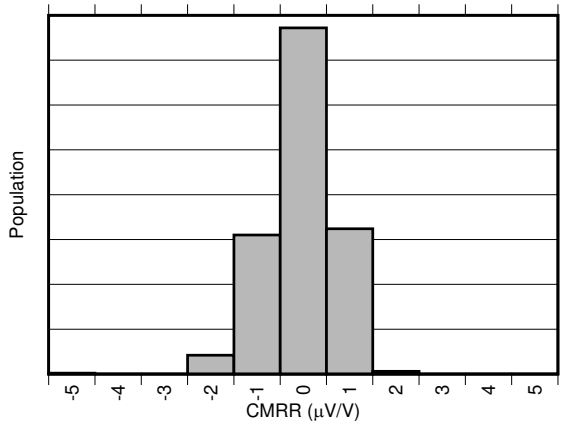


図 6-6. Common-Mode Rejection Ratio Distribution (INA301A2-Q1)

6.6 Typical Characteristics (continued)

at T_A = 25°C, V_S = 5 V, V_{IN+} = 12 V, and alert pullup resistor = 10 kΩ (unless otherwise noted)

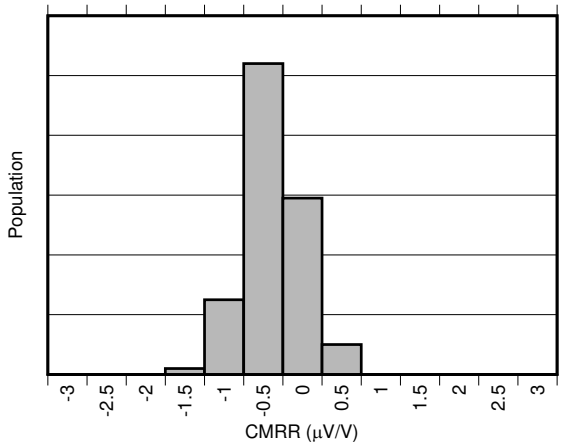


図 6-7. Common-Mode Rejection Ratio Distribution (INA301A3-Q1)

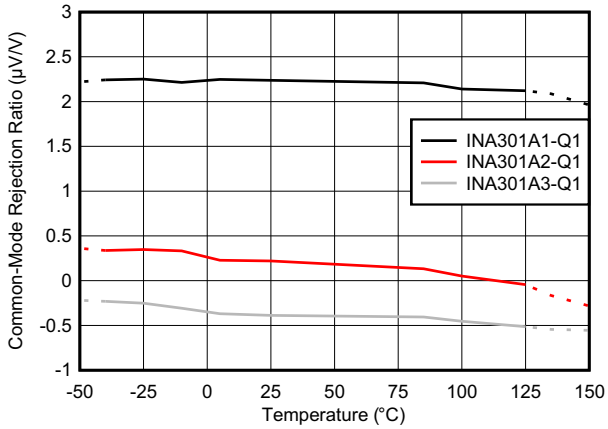


図 6-8. Common-Mode Rejection Ratio vs. Temperature

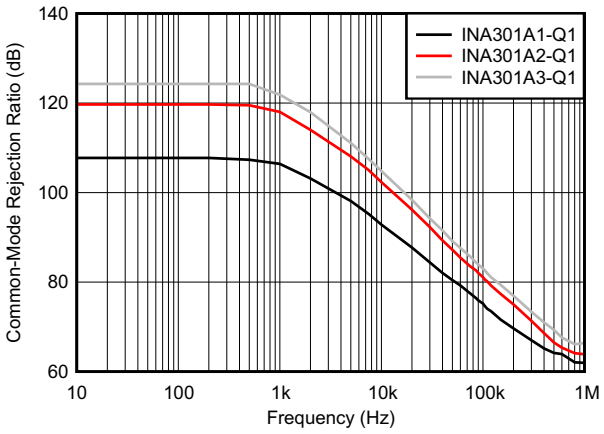


図 6-9. Common-Mode Rejection Ratio vs. Frequency

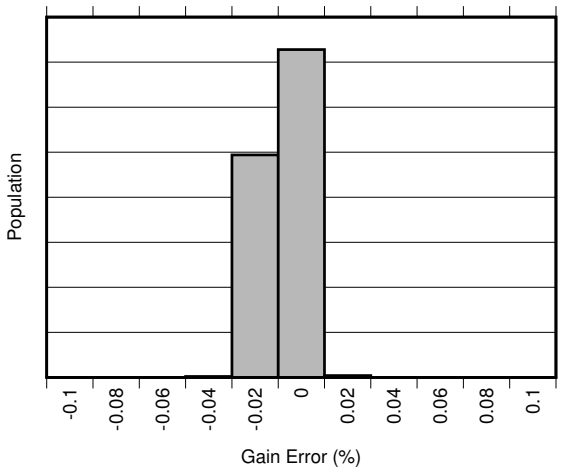


図 6-10. Gain Error Distribution (INA301A1-Q1)

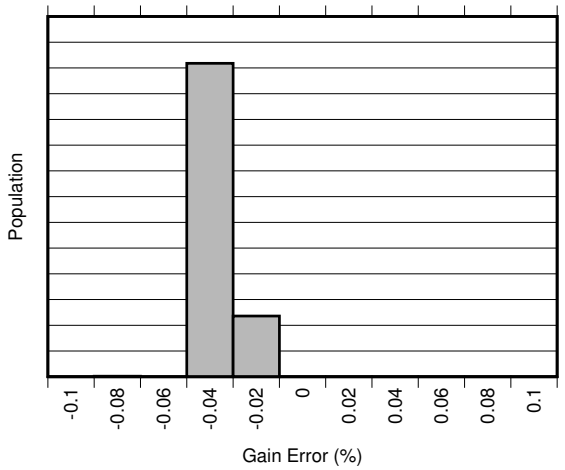


図 6-11. Gain Error Distribution (INA301A2-Q1)

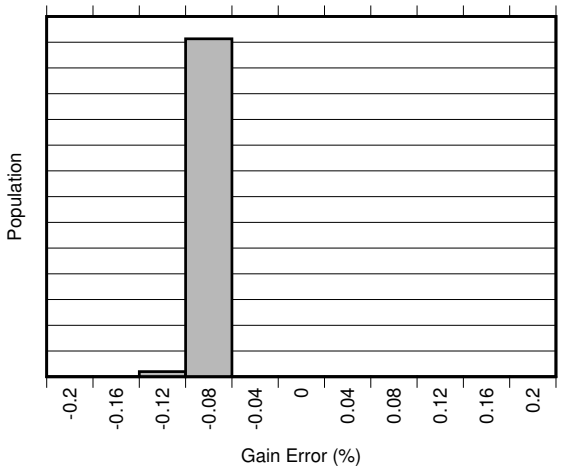


図 6-12. Gain Error Distribution (INA301A3-Q1)

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6.6 Typical Characteristics (continued)

at T_A = 25°C, V_S = 5 V, V_{IN+} = 12 V, and alert pullup resistor = 10 kΩ (unless otherwise noted)

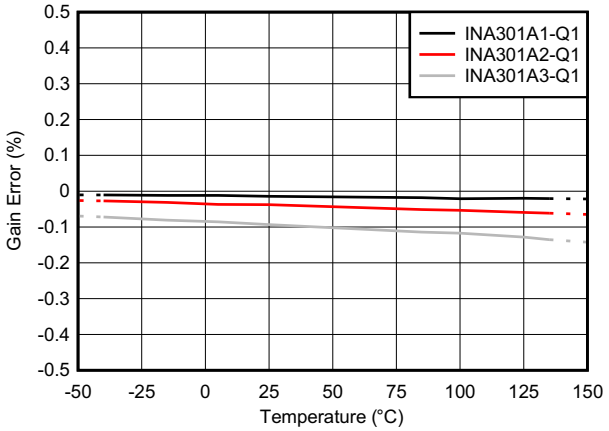


図 6-13. Gain Error vs. Temperature

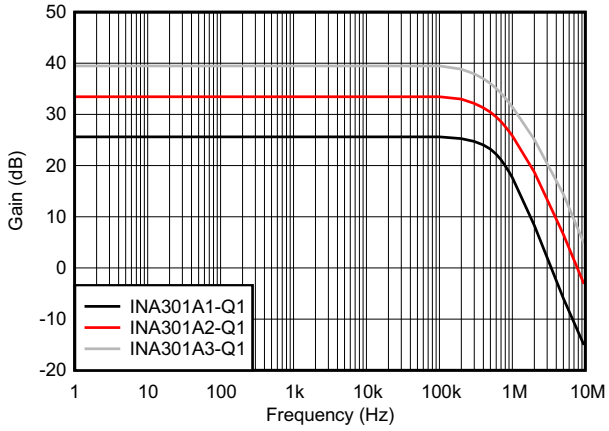


図 6-14. Gain vs. Frequency

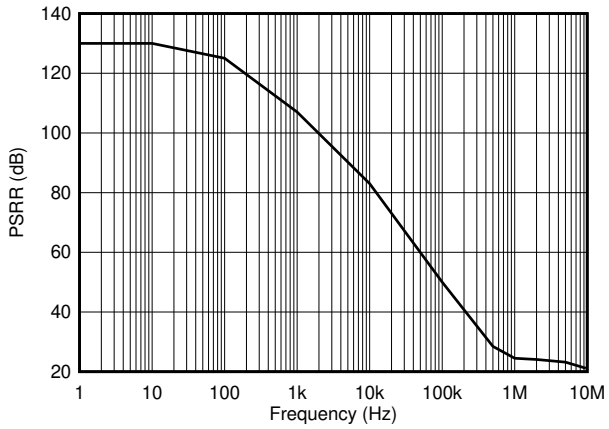


図 6-15. Power-Supply Rejection Ratio vs. Frequency

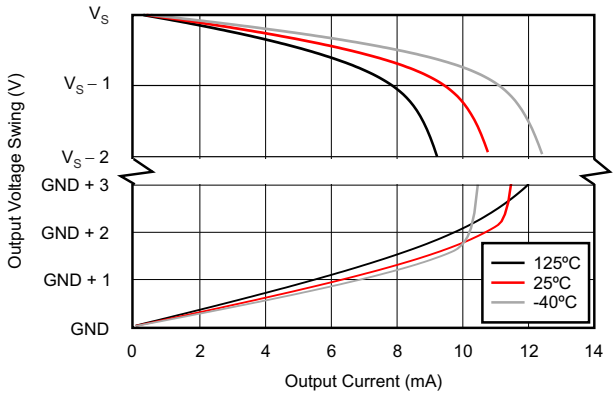


図 6-16. Output Voltage Swing vs. Output Current

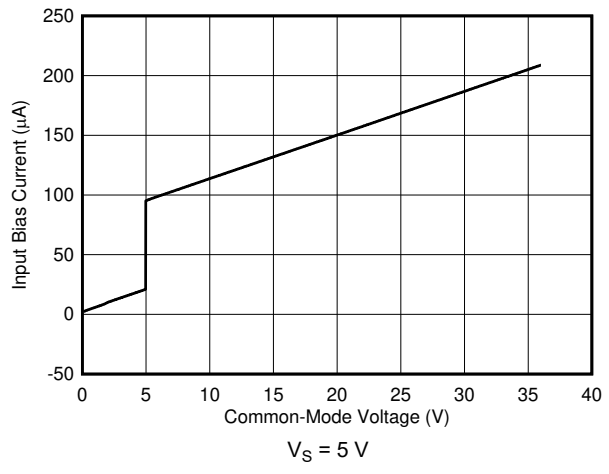


図 6-17. Input Bias Current vs. Common-Mode Voltage

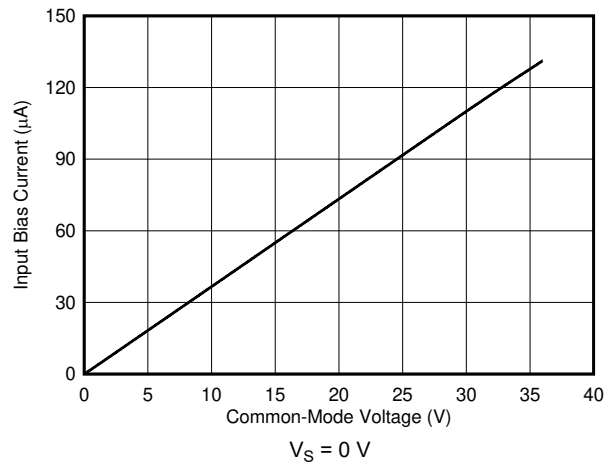


図 6-18. Input Bias Current vs. Common-Mode Voltage

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6.6 Typical Characteristics (continued)

at T_A = 25°C, V_S = 5 V, V_{IN+} = 12 V, and alert pullup resistor = 10 kΩ (unless otherwise noted)

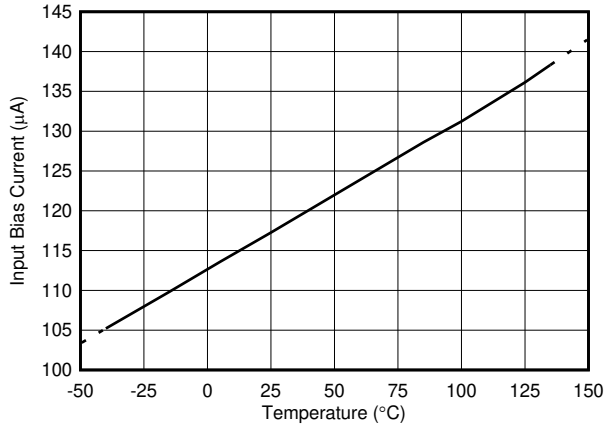


図 6-19. Input Bias Current vs. Temperature

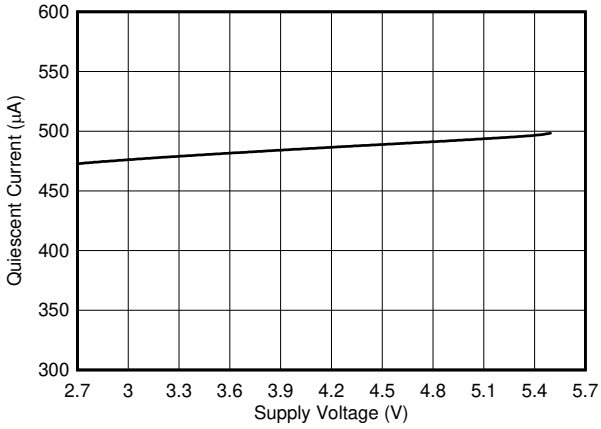


図 6-20. Quiescent Current vs. Supply Voltage

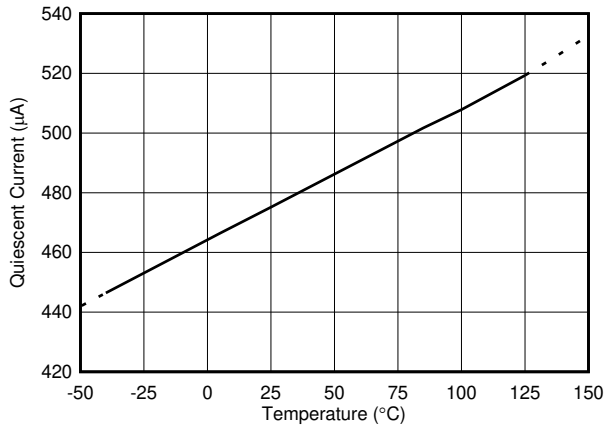


図 6-21. Quiescent Current vs. Temperature

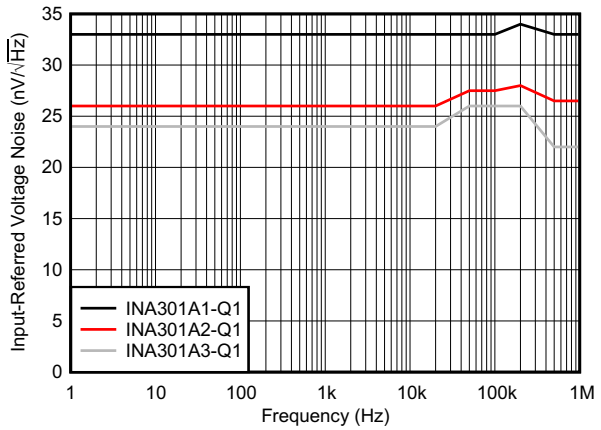


図 6-22. Input-Referred Voltage Noise vs. Frequency

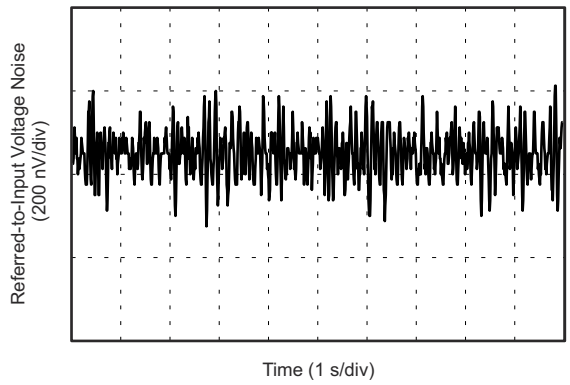
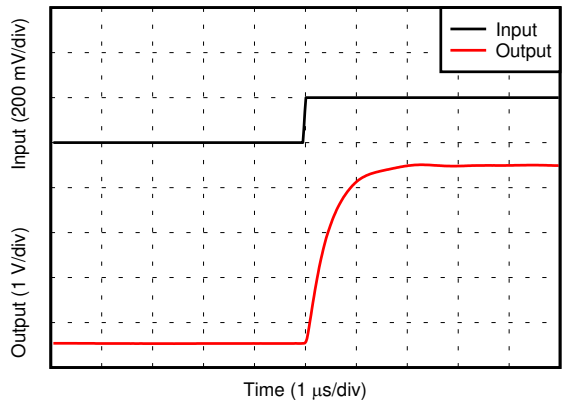


図 6-23. 0.1-Hz to 10-Hz Referred-to-Input Voltage Noise



4-V_{PP} output step

図 6-24. Voltage Output Rising Step Response

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6.6 Typical Characteristics (continued)

at T_A = 25°C, V_S = 5 V, V_{IN+} = 12 V, and alert pullup resistor = 10 kΩ (unless otherwise noted)

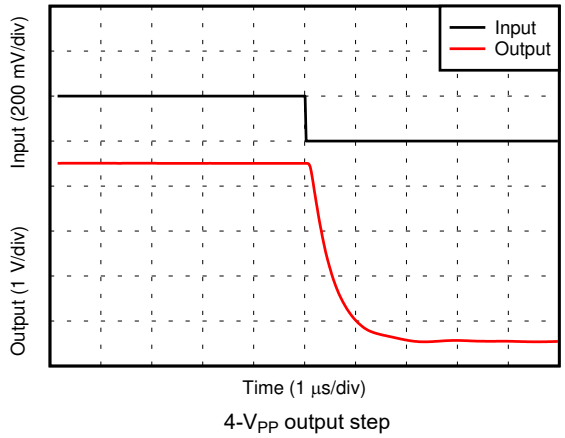


図 6-25. Voltage Output Falling Step Response

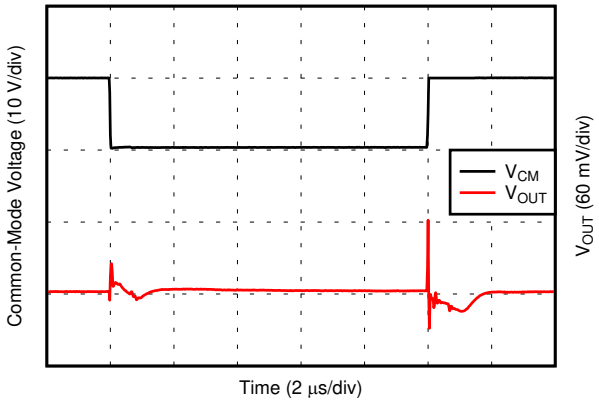


図 6-26. Common-Mode Voltage Transient Response

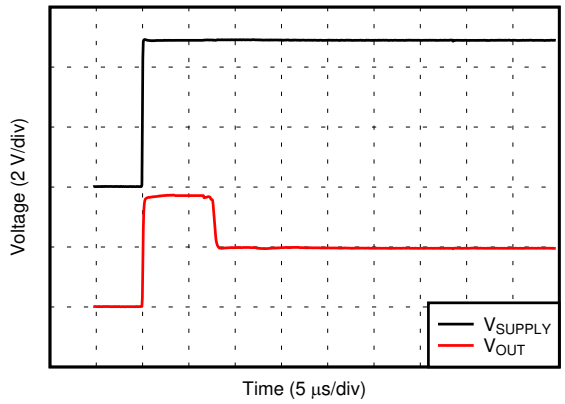


図 6-27. Start-Up Response

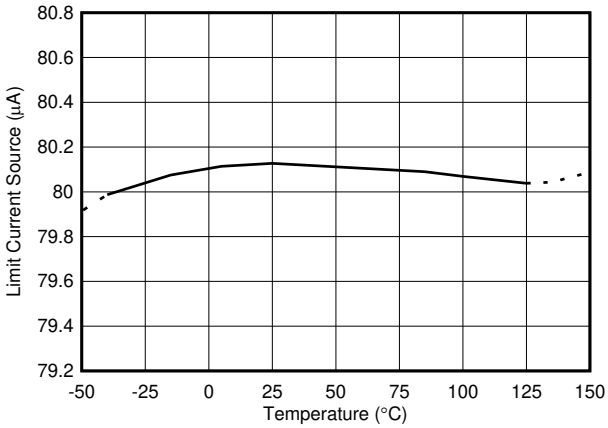


図 6-28. Limit Current Source vs. Temperature

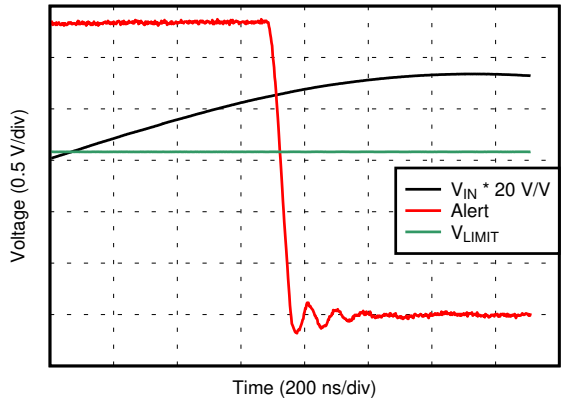


図 6-29. Total Propagation Delay (INA301A1-Q1)

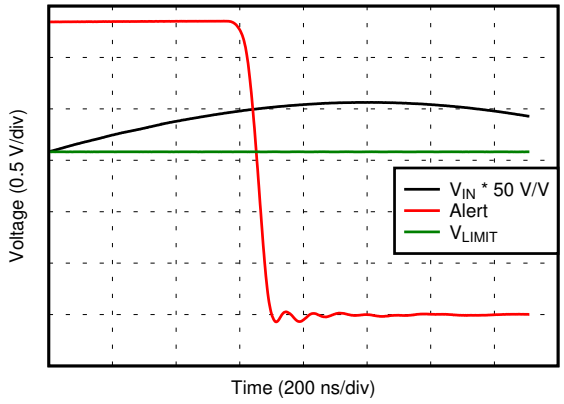


図 6-30. Total Propagation Delay (INA301A2-Q1)

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6.6 Typical Characteristics (continued)

at T_A = 25°C, V_S = 5 V, V_{IN+} = 12 V, and alert pullup resistor = 10 kΩ (unless otherwise noted)

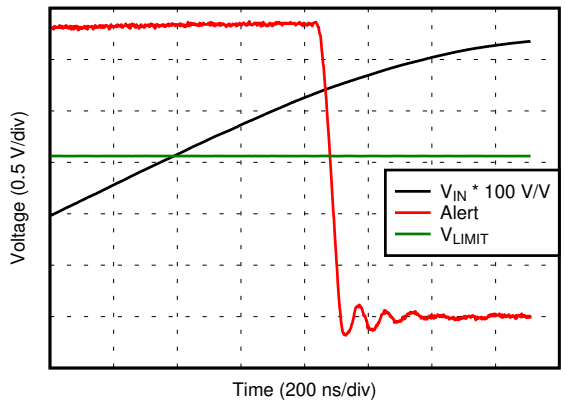


図 6-31. Total Propagation Delay (INA301A3-Q1)

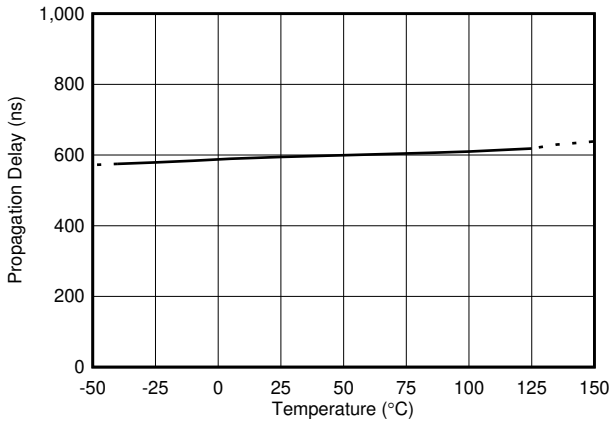


図 6-32. Comparator Propagation Delay vs. Temperature

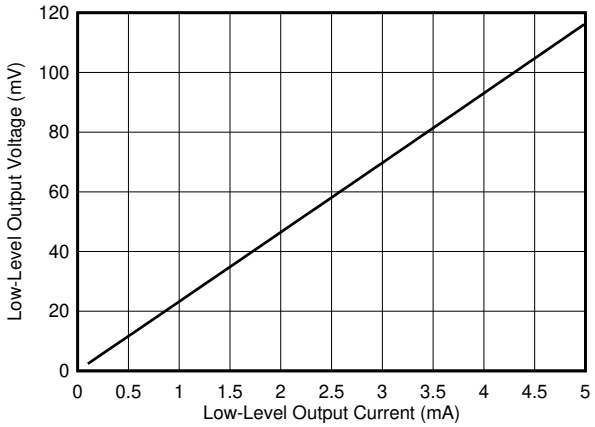


図 6-33. Comparator Alert V_{OL} vs. I_{OL}

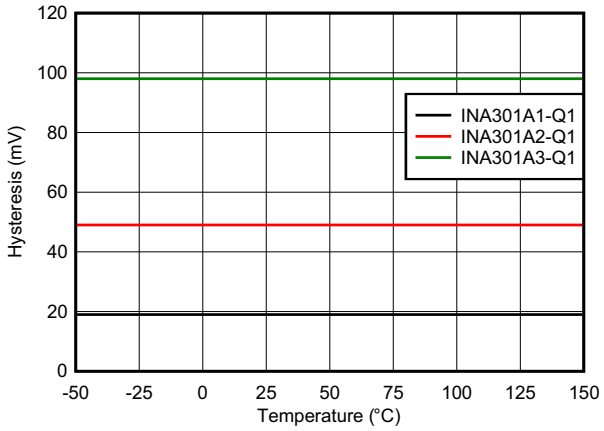


図 6-34. Hysteresis vs. Temperature

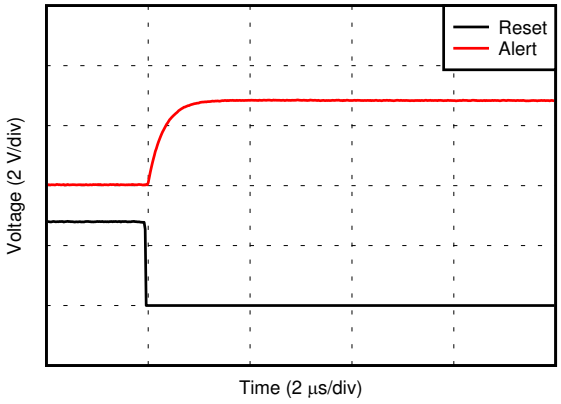


図 6-35. Comparator Reset Response

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7 Detailed Description

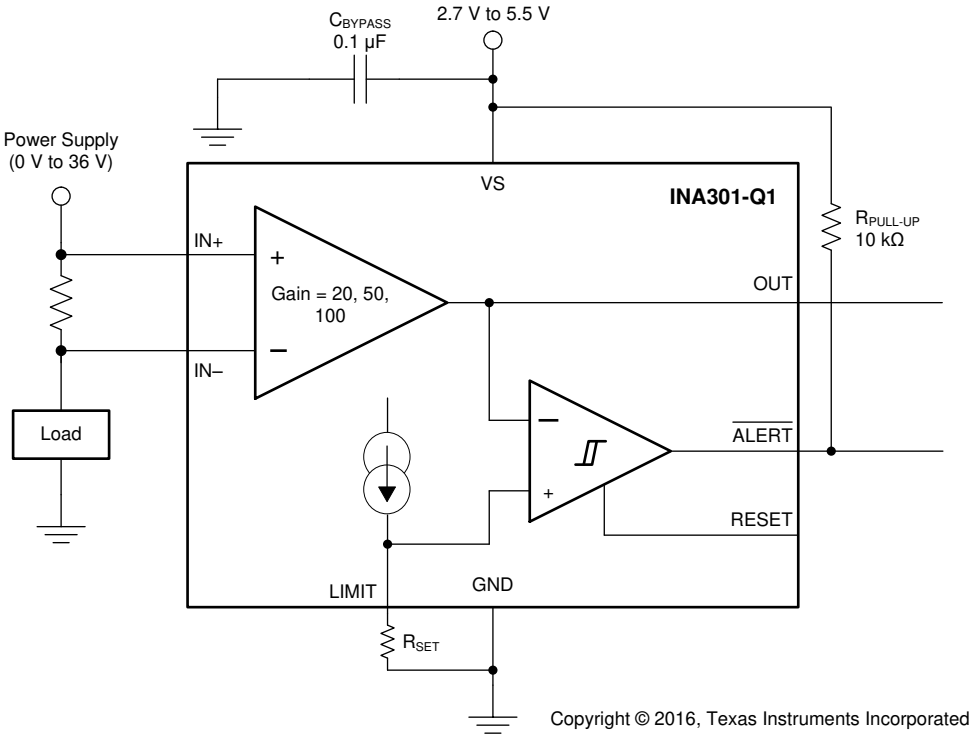
7.1 Overview

The INA301-Q1 is a 36-V common-mode, zero-drift topology, current-sensing amplifier that can be used in both low-side and high-side configurations. These specially-designed, current-sensing amplifiers are able to accurately measure voltages developed across current-sensing resistors (also known as current-shunt resistors) on common-mode voltages that far exceed the supply voltage powering the device. Current can be measured on input voltage rails as high as 36 V, and the device can be powered from supply voltages as low as 2.7 V. The device can also withstand the full 36-V common-mode voltage at the input pins when the supply voltage is removed without causing damage.

The zero-drift topology enables high-precision measurements with maximum input offset voltages as low as 35 µV with a temperature contribution of only 0.5 µV/°C over the full temperature range of –40°C to +125°C. The low total offset voltage of the INA301-Q1 enables smaller current-sense resistor values to be used, and allows for a more efficient system operation without sacrificing measurement accuracy resulting from the smaller input signal.

The INA301-Q1 uses a single external resistor to allow for a simple method of setting the corresponding current threshold level for the device to use for out-of-range comparison. Combining the precision measurement of the current-sense amplifier and the onboard comparator enables an all-in-one overcurrent detection device. This combination creates a highly-accurate solution that is capable of fast detection of out-of-range conditions, and allows the system to take corrective actions to prevent potential component or system-wide damage.

7.2 Functional Block Diagram



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7.3 Feature Description

7.3.1 Alert Output ($\overline{\text{ALERT}}$ Pin)

The device $\overline{\text{ALERT}}$ pin is an active-low, open-drain output that is designed to be pulled low when the input conditions are detected to be out-of-range. Add a 10-kΩ pullup resistor from $\overline{\text{ALERT}}$ pin to the supply voltage. This open-drain pin can be pulled up to a voltage beyond the V_S supply voltage, but must not exceed 5.5 V.

図 7-1 shows the alert output response of the internal comparator. When the output voltage of the amplifier is less than the voltage developed at the LIMIT pin, the comparator output is in the default high state. When the amplifier output voltage exceeds the threshold voltage set at the LIMIT pin, the comparator output becomes active and pulls low. This active low output indicates that the measured signal at the amplifier input has exceeded the programmed threshold level, indicating an overcurrent or out-of-range condition has occurred.

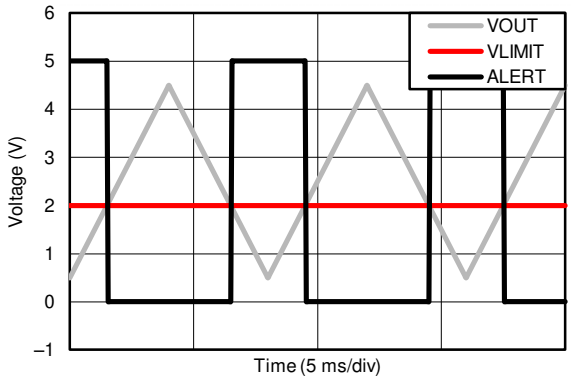


図 7-1. Overcurrent Alert Response

7.3.2 Current-Limit Threshold

The INA301-Q1 determines if an overcurrent event is present by comparing the amplified measured voltage developed across the current-sensing resistor to the corresponding signal developed at the LIMIT pin. The threshold voltage for the LIMIT pin is set using a single external resistor, or by connecting an external voltage source to the LIMIT pin.

7.3.2.1 Resistor-Controlled Current Limit

The typical method for setting the limit threshold voltage is to connect a resistor from the LIMIT pin to ground. The value of this resistor, R_{LIMIT}, is chosen in order to create a corresponding voltage at the LIMIT pin equivalent to the output voltage, V_{OUT}, when the maximum desired load current is flowing through the current-sensing resistor. An internal 80-µA current source is connected to the LIMIT pin to create a corresponding voltage used to compare to the amplifier output voltage, depending on the value of the R_{LIMIT} resistor.

In the equations from 表 7-1, V_{TRIP} represents the overcurrent threshold that the device is programmed to monitor, and V_{LIMIT} is the programmed signal set to detect the V_{TRIP} level.

表 7-1. Calculating the Threshold-Limit-Setting Resistor, R_{LIMIT}

PARAMETER		EQUATION
V_{TRIP}	V_{OUT} at the desired-current trip value	I_{LOAD} × R_{SENSE} x Gain
V_{LIMIT}	Threshold limit voltage	$V_{LIMIT} = V_{TRIP}$
		I_{LIMIT} × R_{LIMIT}
R_{LIMIT}	Threshold limit-setting resistor value	V_{LIMIT} / I_{LIMIT}
		V_{LIMIT} / 80 µA

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7.3.2.1.1 Resistor-Controlled, Current-Limit Example

If the current level indicating an out-of-range condition is present is 20 A, and the current-sense resistor value is 10 mΩ, then the input threshold signal is 200 mV. The INA301A1-Q1 has a gain of 20, therefore, the resulting output voltage at the 20-A input condition is 4 V. The value for R_{LIMIT} is selected to allow the device to detect to this 20-A threshold, indicating an overcurrent event occurred. When the INA301-Q1 detects this out-of-range condition, the $\overline{ALERT}$ pin asserts and pulls low. For this example, 表 7-2 lists the calculated value of R_{LIMIT} required to detect a 4-V level as 50 kΩ.

表 7-2. Example of Calculating the Limit Threshold Setting Resistor, R_{LIMIT}

PARAMETER		EQUATION
V_{TRIP}	V_{OUT} at the desired current trip value	$I_{LOAD} \times R_{SENSE}$ x Gain ↓ 20 A x 10 mΩ x 20 V/V = 4 V
V_{LIMIT}	Threshold limit voltage	$V_{LIMIT} = V_{TRIP}$
		$I_{LIMIT} \times R_{LIMIT}$
R_{LIMIT}	Threshold limit-setting resistor value	V_{LIMIT} / I_{LIMIT} ↓ 4 V / 80 µA = 50 kΩ

7.3.2.2 Voltage-Source-Controlled Current Limit

Another method for setting the limit voltage is to connect the LIMIT pin to a programmable digital-to-analog converter (DAC) or other external voltage source. The benefit of this method is the ability to adjust the current-limit threshold to account for different threshold voltages that are used for different system operating conditions. For example, this method can be used in a system that has one current-limit threshold level that must be monitored during a power-up sequence, but different threshold levels that must be monitored during other system operating modes.

In 表 7-3, V_{TRIP} represents the overcurrent threshold that the device is programmed to monitor, and V_{SOURCE} is the programmed signal set to detect the V_{TRIP} level.

表 7-3. Calculating the Limit Threshold Voltage Source, V_{SOURCE}

PARAMETER		EQUATION
V_{TRIP}	V_{OUT} at the desired current trip value	$I_{LOAD} \times R_{SENSE} \times$ Gain
V_{SOURCE}	Threshold limit voltage	$V_{SOURCE} = V_{TRIP}$

7.3.3 Hysteresis

The onboard comparator in the INA301-Q1 reduces the possibility of oscillations in the alert output when the measured signal level is near the overlimit threshold level because of noise. When the output voltage (V_{OUT}) exceeds the voltage developed at the LIMIT pin, the $\overline{ALERT}$ pin is asserted and pulls low. The output voltage must drop below the LIMIT pin threshold voltage by the gain-dependent hysteresis level for the $\overline{ALERT}$ pin to deassert and return to the nominal high state (see 図 7-2).

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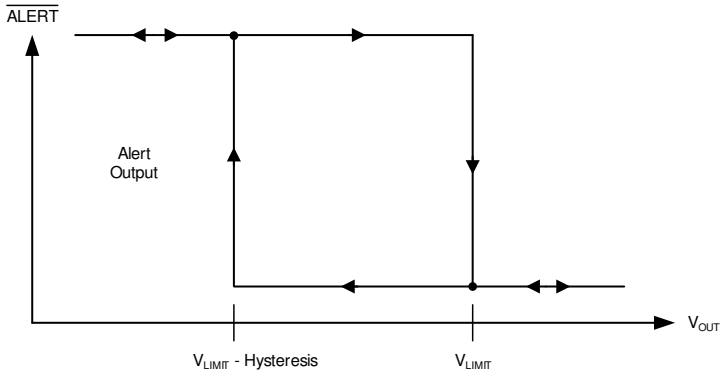


図 7-2. Typical Comparator Hysteresis

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7.4 Device Functional Modes

7.4.1 Alert Mode

The device has two output operating modes, transparent and latched, that are selected based on the RESET pin setting. These modes change how the $\overline{\text{ALERT}}$ pin responds following an alert when the overcurrent condition is removed.

7.4.1.1 Transparent Output Mode

The device is set to transparent mode when the RESET pin is pulled low, thus allowing the output alert state to change and follow the input signal with respect to the programmed alert threshold. For example, when the differential input signal rises above the alert threshold, the $\overline{\text{ALERT}}$ output pin is pulled low. As soon as the differential input signal drops below the alert threshold, the output returns to the default high-output state. A common implementation using the device in transparent mode is to connect the $\overline{\text{ALERT}}$ pin to a hardware interrupt input on a microcontroller. As soon as an overcurrent condition is detected and the $\overline{\text{ALERT}}$ pin is pulled low, the hardware interrupt input detects the output-state change, and the microcontroller can begin to make changes to the system operation required to address the overcurrent condition. Under this configuration, the $\overline{\text{ALERT}}$ pin transition from high to low is captured by the microcontroller so that the output can return to the default high state when the overcurrent event is removed.

7.4.1.2 Latch Output Mode

Some applications do not have the functionality available to continuously monitor the state of the output $\overline{\text{ALERT}}$ pin to detect an overcurrent condition as described in the *Transparent Output Mode* section. A typical example of this application is a system that is only able to poll the $\overline{\text{ALERT}}$ pin state periodically to determine if the system is functioning correctly. If the device is set to transparent mode in this type of application, the state change of the $\overline{\text{ALERT}}$ pin might be missed when $\overline{\text{ALERT}}$ is pulled low to indicate an out-of-range event, if the out-of-range condition does not appear during one of these periodic polling events. Latch mode is specifically intended to accommodate these applications.

The INA301-Q1 is placed into the corresponding output modes based on the signal connected to RESET (see 表 7-4). The difference between latch mode and transparent mode is how the $\overline{\text{ALERT}}$ pin responds when an overcurrent event ends. In transparent mode (RESET = low), when the differential input signal drops below the limit threshold level after the $\overline{\text{ALERT}}$ pin asserts because of an overcurrent event, the $\overline{\text{ALERT}}$ pin state returns to the default high setting to indicate that the overcurrent event has ended.

表 7-4. Output Mode Settings

OUTPUT MODE	RESET PIN SETTING
Transparent mode	RESET = low
Latch mode	RESET = high

In latch mode (RESET = high), when an overlimit condition is detected and the $\overline{\text{ALERT}}$ pin is pulled low, the $\overline{\text{ALERT}}$ pin does not return to the default high state when the differential input signal drops below the alert threshold level. In order to clear the alert, pull the RESET pin low for at least 100 ns. Pulling the RESET pin low allows the $\overline{\text{ALERT}}$ pin to return to the default high level, provided that the differential input signal has dropped below the alert threshold. If the input signal is still greater than the threshold limit when the RESET pin is pulled low, the $\overline{\text{ALERT}}$ pin remains low. When the alert condition is detected by the system controller, the RESET pin can be set back to high in order to place the device back in latch mode.

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The latch and transparent modes represented in 図 7-3 show that when V_{IN} drops back below the V_{LIMIT} threshold for the first time, the RESET pin is pulled high. With the RESET pin is pulled high, the device is set to latch mode, so that the $\overline{ALERT}$ pin output state does not return high when the input signal drops below the V_{LIMIT} threshold. Only when the RESET pin is pulled low does the $\overline{ALERT}$ pin return to the default high level, thus indicating that the input signal is below the limit threshold. When the input signal drops below the limit threshold for the second time, the RESET pin is already pulled low. The device is set to transparent mode at this point and the $\overline{ALERT}$ pin is pulled back high as soon as the input signal drops below the alert threshold.

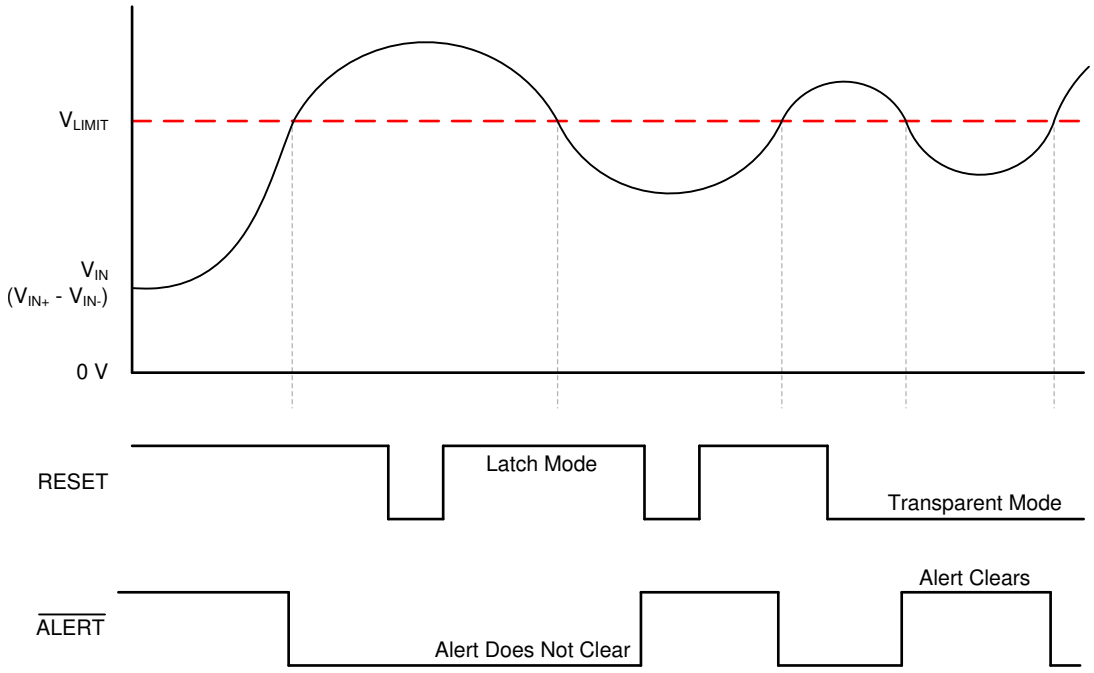


図 7-3. Transparent Mode vs. Latch Mode

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8 Applications and Implementation

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8.1 Application Information

The INA301-Q1 enables easy configuration to detect overcurrent conditions in an application. This device is individually targeted towards unidirectional overcurrent detection of a single threshold. However, this device can also be paired with additional INA301-Q1 devices and circuitry to create more complex monitoring functional blocks.

8.1.1 Selecting a Current-Sensing Resistor

The INA301-Q1 measures the differential voltage developed across a resistor when current flows through the component in order to determine if the current being monitored exceeds a defined limit. This resistor is commonly referred to as a *current-sensing resistor* or a *current-shunt resistor*, with each term commonly used interchangeably. The flexible design of this device allows for measuring a wide differential input signal range across the current-sensing resistor.

Selecting the value of this current-sensing resistor is primarily based on two factors: the required accuracy of the current measurement, and the allowable power dissipation across the current-sensing resistor. Larger voltages developed across this resistor allow for more accurate measurements to be made. Amplifiers have fixed internal errors that are largely dominated by the inherent input offset voltage. When the input signal decreases, these fixed internal amplifier errors become a larger portion of the measurement and increase the uncertainty in the measurement accuracy. When the input signal increases, the measurement uncertainty is reduced because the fixed errors are a smaller percentage of the signal being measured. Therefore, the use of larger-value, current-sensing resistors inherently improves measurement accuracy.

However, a system design trade-off must be evaluated through the use of larger input signals that improve measurement accuracy. Increasing the current sense resistor value results in an increase in power dissipation across the current-sensing resistor, and also increases the differential voltage developed across the resistor when current passes through the component. This increase in voltage across the resistor increases the power that the resistor must be able to dissipate. Decreasing the value of the current-shunt resistor reduces the power dissipation requirements of the resistor, but increases the measurement errors resulting from the decreased input signal. Selecting the optimal value for the shunt resistor requires factoring both the accuracy requirement for the specific application, and the allowable power dissipation of this component.

Low-ohmic-value resistors enable large currents to be accurately monitored with the INA301-Q1. An increasing number of very low-ohmic-value resistors are becoming more widely available, with values of 200 µΩ and less, and power dissipations of up to 5 W.

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8.1.1.1 Selecting a Current-Sensing Resistor Example

In this example, the trade-offs involved in selecting a current-sensing resistor are described. This example requires 2.5% accuracy for detecting a 10-A overcurrent event, with only 250 mW of allowable power dissipation across the current-sensing resistor at the full-scale current level. Although the maximum power dissipation is defined as 250 mW, a lower dissipation is preferred in order to improve system efficiency. Some initial assumptions are made that are used in this example:

- the limit-setting resistor (R_{LIMIT}) is a 1% component
- the maximum tolerance specification for the internal threshold setting current source (0.5%) is used

Given the total error budget of 2.5%, up to 1% of error is available to be attributed to the measurement error of the device under these conditions.

As shown in 表 8-1, the maximum value calculated for the current-sensing resistor with these requirements is 2.5 mΩ. Although this value satisfies the maximum power dissipation requirement of 250 mW, headroom is available from the 2.5% maximum total overcurrent detection error in order to reduce the value of the current-sensing resistor, and reduce the power dissipation further. Selecting a 1.5-mΩ, current-sensing resistor value offers a good tradeoff for reducing the power dissipation in this scenario by approximately 40% while still remaining within the accuracy region.

表 8-1. Calculating the Current-Sensing Resistor, R_{SENSE}

PARAMETER		EQUATION	VALUE	UNIT
I_{MAX}	Maximum current		10	A
P_{D_MAX}	Maximum allowable power dissipation		250	mW
R_{SENSE_MAX}	Maximum allowable R_{SENSE}	P_{D_MAX} / I_{MAX}^2	2.5	mΩ
V_{OS}	Offset voltage		150	µV
V_{OS_ERROR}	Initial offset voltage error	$(V_{OS} / (R_{SENSE_MAX} \times I_{MAX}) \times 100$	0.6%	
E_G	Gain error		0.25%	
$ERROR_{TOTAL}$	Total measurement error	$\sqrt{(V_{OS_ERROR}^2 + E_G^2)}$	0.65%	
	Allowable current threshold accuracy		2.5%	
$ERROR_{INITIAL}$	Initial threshold error	I_{LIMIT} Tolerance + R_{LIMIT} Tolerance	1.5%	
$ERROR_{AVAILABLE}$	Maximum allowable measurement error	Maximum Error – $ERROR_{INITIAL}$	1%	
$V_{OS_ERROR_MAX}$	Maximum allowable offset error	$\sqrt{(ERROR_{AVAILABLE}^2 - E_G^2)}$	0.97%	
V_{DIFF_MIN}	Minimum differential voltage	$V_{OS} / V_{OS_ERROR_MAX\ (1\%)}$	15	mV
R_{SENSE_MIN}	Minimum sense resistor value	V_{DIFF_MIN} / I_{MAX}	1.5	mΩ
P_{D_MIN}	Minimum power dissipation	$R_{SENSE_MIN} \times I_{MAX}^2$	150	mW

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8.1.2 Input Filtering

External system noise can significantly affect the ability of a comparator to accurately measure and detect whether input signals exceed the reference threshold levels and reliably indicate overrange conditions. The most obvious effect that external noise has on the operation of a comparator is to cause a false-alert condition. If a comparator detects a large noise transient coupled into the signal, the device can easily interpret this transient as an overrange condition.

External filtering helps reduce the amount of noise that reaches the comparator, and thus reduce the likelihood of a false alert from occurring. The tradeoff to adding this noise filter is that the alert response time is increased because of the input signal being filtered along with the noise. 図 8-1 shows the implementation of an input filter for the device.

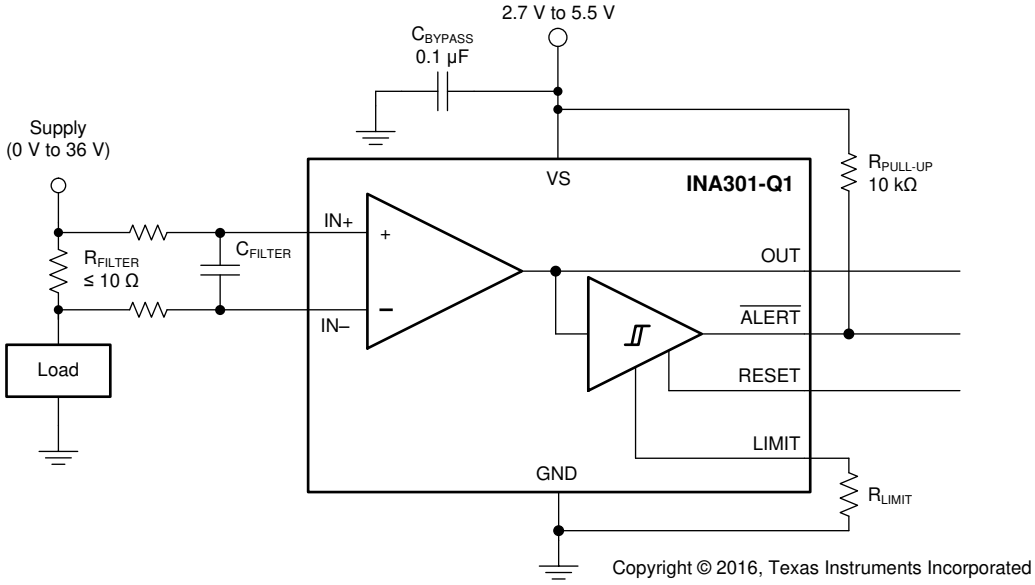


図 8-1. Input Filter

Limiting the input resistance this filter is important because this resistance can have a significant affect on the input signal that reaches the device input pins because of the device input bias currents. A typical system implementation involves placing the current-sensing resistor very near the device so that the traces are very short and the trace impedance is very small. This layout helps reduce the ability of coupling additional noise into the measurement. Under these conditions, the characteristics of the input bias currents have minimal affect on device performance.

As illustrated in 図 8-2, the input bias currents increase in opposite directions when the differential input voltage increases. This increase results from a device design that allows common-mode input voltages to far exceed the device supply voltage range. With input filter resistors now placed in series with these unequal input bias currents, there are unequal voltage drops developed across these input resistors. The difference between these two voltage drops appears as an added signal that, in this case, subtracts from the voltage developed across the current-sensing resistor, thus reducing the signal that reaches the device input pins. Smaller-value input resistors reduce this effect of signal attenuation to allow for a more accurate measurement.

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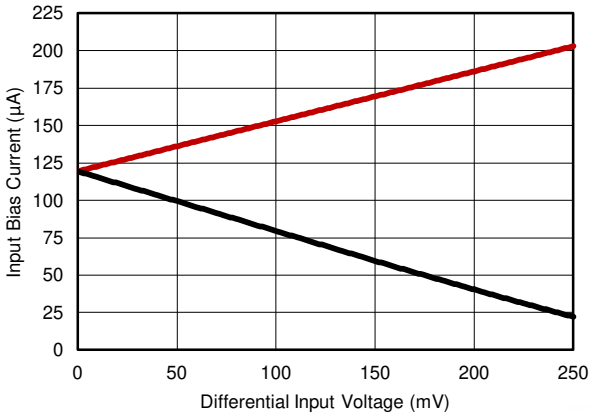


図 8-2. Input Bias Current vs. Differential Input Voltage

For example, with a differential voltage of 10 mV developed across a current-sensing resistor and using 20-Ω resistors, the differential signal that actually reaches the device is 9.85 mV. A measurement error of 1.5% is created as a result of these external input filter resistors. Use 10-Ω input filter resistors instead of the 20-Ω resistors to reduce this added error from 1.5% down to 0.75%.

8.1.3 INA301-Q1 Operation With Common-Mode Voltage Transients Greater Than 36 V

With a small amount of additional circuitry, the INA301-Q1 can be used in circuits subject to transients greater than 36 V. Use only Zener diodes or Zener-type transient absorbers (sometimes referred to as *transzorbs*). Any other type of transient absorber has an unacceptable time delay. Start by adding a pair of resistors as a working impedance for the Zener diode, as shown in 図 8-3. Keep these resistors as small as possible; preferably, 10 Ω or less. Larger values can be used, but with an additional induced error resulting from less signal reaching the device input pins. Because this circuit limits only short-term transients, many applications are satisfied with a 10-Ω resistor along with conventional Zener diodes of the lowest power rating available. This combination uses the least amount of board space. These diodes can be found in packages as small as SOT-523 or SOD-523.

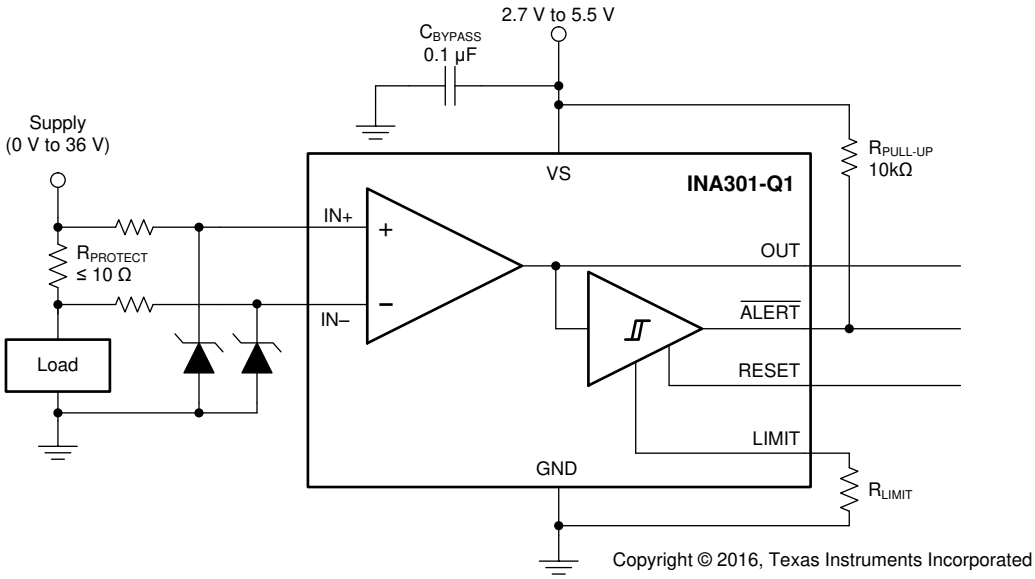


図 8-3. Transient Protection

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8.2 Typical Application

Although this device is only able to measure current through a current-sensing resistor flowing in one direction, a second INA301-Q1 can be used to create a bidirectional monitor (see 図 8-4).

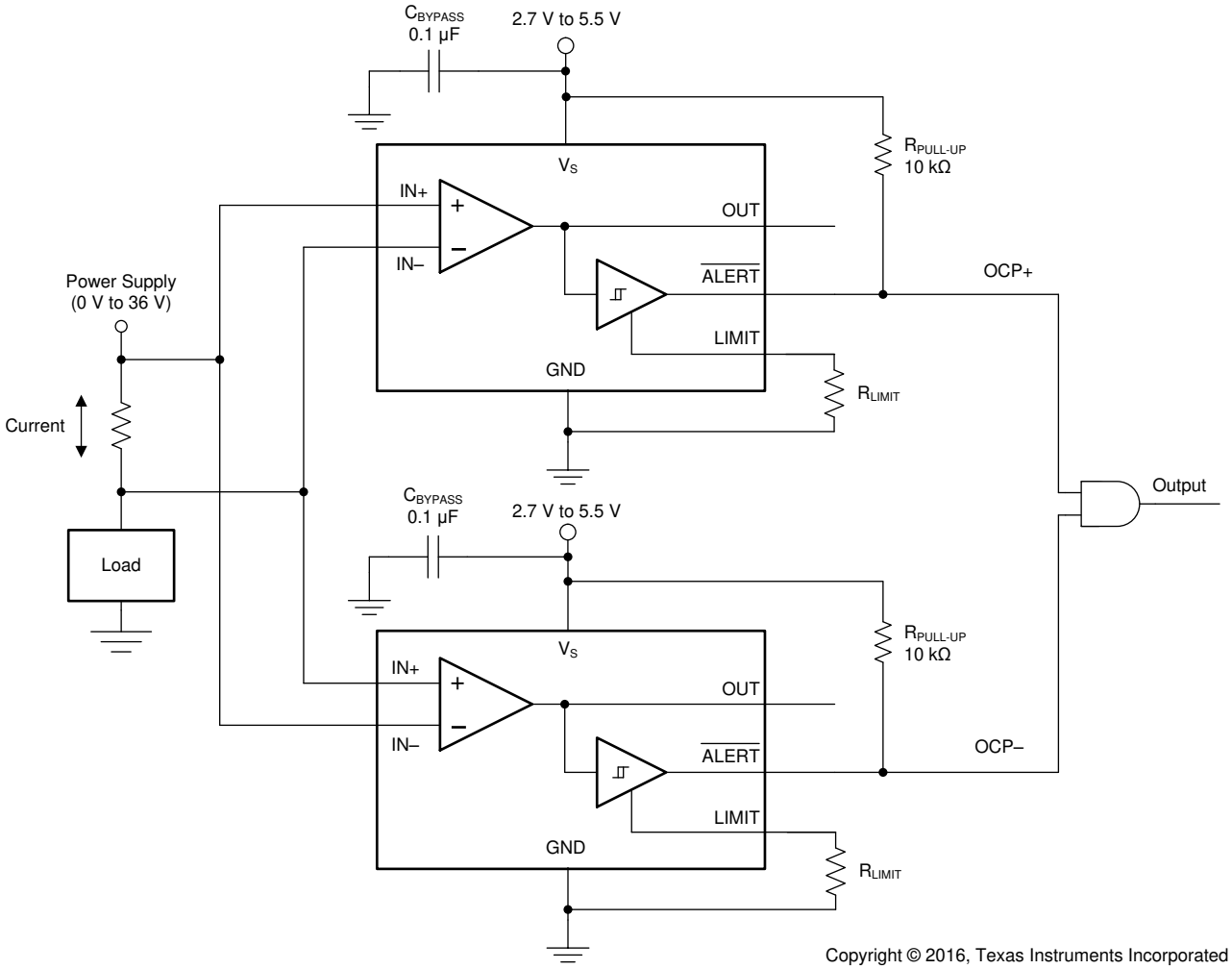


図 8-4. Bidirectional Application

8.2.1 Design Requirements

For this design example, use the parameters listed in 表 8-2 as the input parameters.

表 8-2. Design Parameters

DESIGN PARAMETERS	EXAMPLE VALUE
Supply voltage	3.3 V
Common-mode voltage	12 V
Voltage gain	100 V/V
Sense resistance	5 mΩ
Source-current swing	–2 A to +2 A
Voltage trip points	–1 A and +1 A

8.2.2 Detailed Design Procedure

First, reverse the input pins of the second INA301-Q1 across the current-sensing resistor. The second device is now able to detect current flowing in the other direction relative to the first device.

Then, select limit resistors to set the voltage trip points by using the equations in 表 7-1. For this application example, these equations give a value of 6.25 kΩ for both limit resistors.

Connect the outputs of each device to an AND gate in order to detect if either of the limit threshold levels are exceeded. 表 8-3shows that the output of the AND gate is high if neither overcurrent limit thresholds are exceeded. A low output state of the AND gate indicates that either the positive overcurrent limit or the negative overcurrent limit are surpassed.

表 8-3. Bidirectional Overcurrent Output Status

OCP STATUS	OUTPUT
OCP+	0
OCP–	0
No OCP	1

8.2.3 Application Curve

図 8-5 shows two INA301-Q1 devices being used in a bidirectional configuration and an output control circuit to detect if one of the two alerts is exceeded.

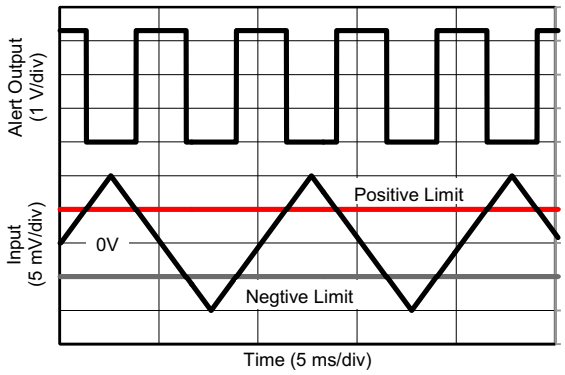


図 8-5. Bidirectional Application Curve

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9 Power Supply Recommendations

The device input circuitry accurately measures signals on common-mode voltages beyond the power-supply voltage, V_S. For example, the voltage applied to the VS power-supply pin can be 5 V, whereas the load power-supply voltage being monitored (V_{CM}) can be as high as 36 V. At power up, for applications where the common-mode voltage (V_{CM}) slew rate is greater than 6 V/µs with a final common-mode voltage greater than 20 V, TI recommends that the V_S supply be present before V_{CM}. If the use case requires V_{CM} to be present before V_S with V_{CM} under these same slewing conditions, then a 331-Ω resistor must be added between the V_S supply and the V_S pin bypass capacitor.

Power-supply bypass capacitors are required for stability and must be placed as close as possible to the supply and ground pins of the device. A typical value for this supply bypass capacitor is 0.1 µF. Applications with noisy or high-impedance power supplies may require additional decoupling capacitors to reject power-supply noise.

During slow power-up events, current flow through the sense resistor or voltage applied to the REF pin can result in the output voltage momentarily exceeding the voltage at the LIMITx pins, resulting in an erroneous indication of an out-of-range event on the $\overline{\text{ALERT}}$x output. When powering the device with a slow ramping power rail where an input signal is already present, all alert indications should be disregarded until the supply voltage has reached the final value.

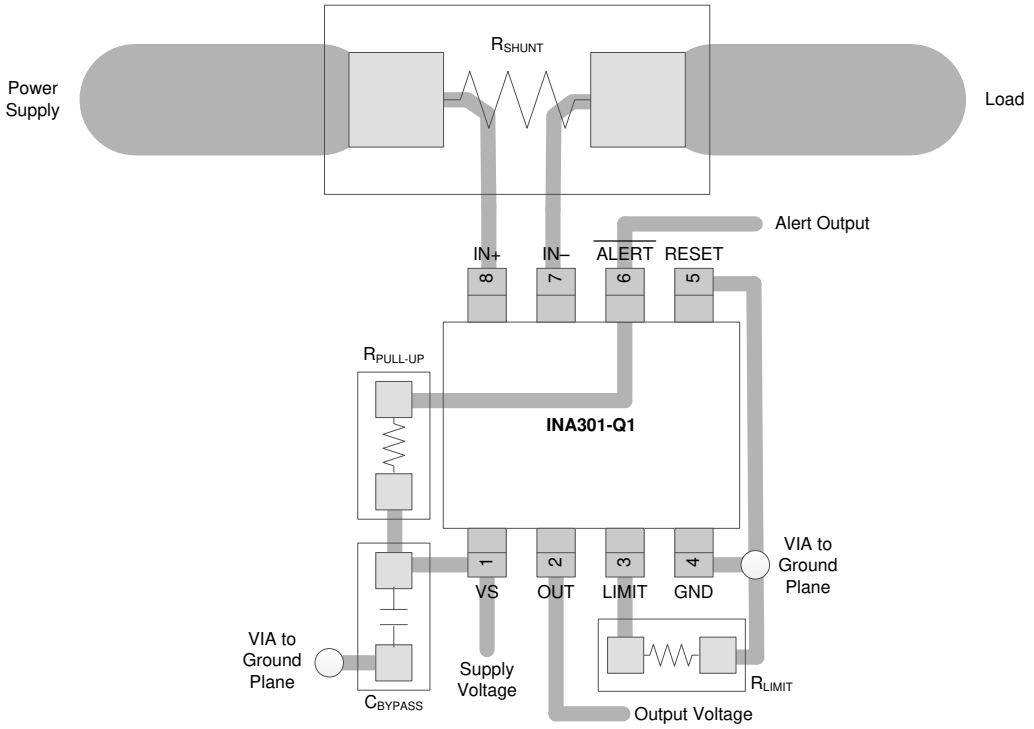
10 Layout

10.1 Layout Guidelines

- Place the power-supply bypass capacitor as close as possible to the supply and ground pins. The recommended value of this bypass capacitor is 0.1 µF. Add more decoupling capacitance to compensate for noisy or high-impedance power supplies.
- Connect R_{LIMIT} to the ground pin as directly as possible to limit additional capacitance on this node. If possible, route this connection to the same plane in order to avoid vias to internal planes. If the connection cannot be routed on the same plane and must pass through vias, make sure that a path is routed from R_{LIMIT} back to the ground pin, and that R_{LIMIT} is not simply connected directly to a ground plane.
- Pull up the open-drain output pin to the supply voltage rail through a 10-kΩ pullup resistor.

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10.2 Layout Example



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Connect the limit resistor directly to the GND pin.

図 10-1. Recommended Layout

11 Device and Documentation Support

11.1 Documentation Support

11.1.1 Related Documentation

INA301EVM User Guide (SBOU154)

11.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.3 サポート・リソース

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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
INA301A1QDGKRQ1	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	ZGG6
INA301A1QDGKRQ1.B	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	ZGG6
INA301A1QDGKTQ1	Active	Production	VSSOP (DGK) | 8	250 | SMALL T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	ZGG6
INA301A1QDGKTQ1.B	Active	Production	VSSOP (DGK) | 8	250 | SMALL T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	ZGG6
INA301A2QDGKRQ1	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	ZGK6
INA301A2QDGKRQ1.B	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	ZGK6
INA301A2QDGKTQ1	Active	Production	VSSOP (DGK) | 8	250 | SMALL T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	ZGK6
INA301A2QDGKTQ1.B	Active	Production	VSSOP (DGK) | 8	250 | SMALL T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	ZGK6
INA301A3QDGKRQ1	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	ZGJ6
INA301A3QDGKRQ1.B	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	ZGJ6
INA301A3QDGKTQ1	Active	Production	VSSOP (DGK) | 8	250 | SMALL T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	ZGJ6
INA301A3QDGKTQ1.B	Active	Production	VSSOP (DGK) | 8	250 | SMALL T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	ZGJ6

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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OTHER QUALIFIED VERSIONS OF INA301-Q1 :

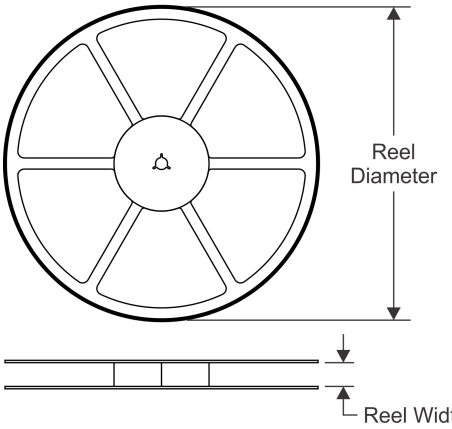
- Catalog : INA301

NOTE: Qualified Version Definitions:

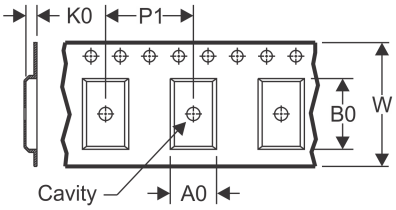
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

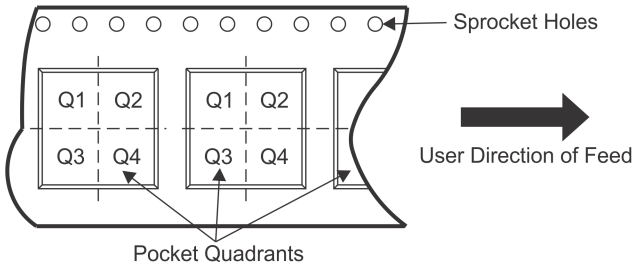


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

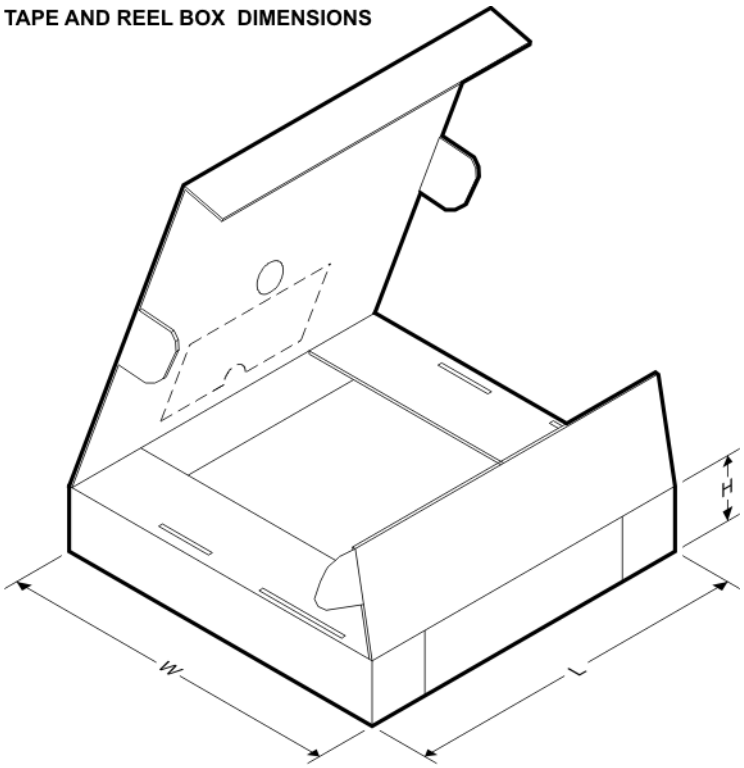
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
INA301A1QDGKRQ1	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
INA301A1QDGKTQ1	VSSOP	DGK	8	250	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
INA301A2QDGKRQ1	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
INA301A2QDGKTQ1	VSSOP	DGK	8	250	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
INA301A3QDGKRQ1	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
INA301A3QDGKTQ1	VSSOP	DGK	8	250	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

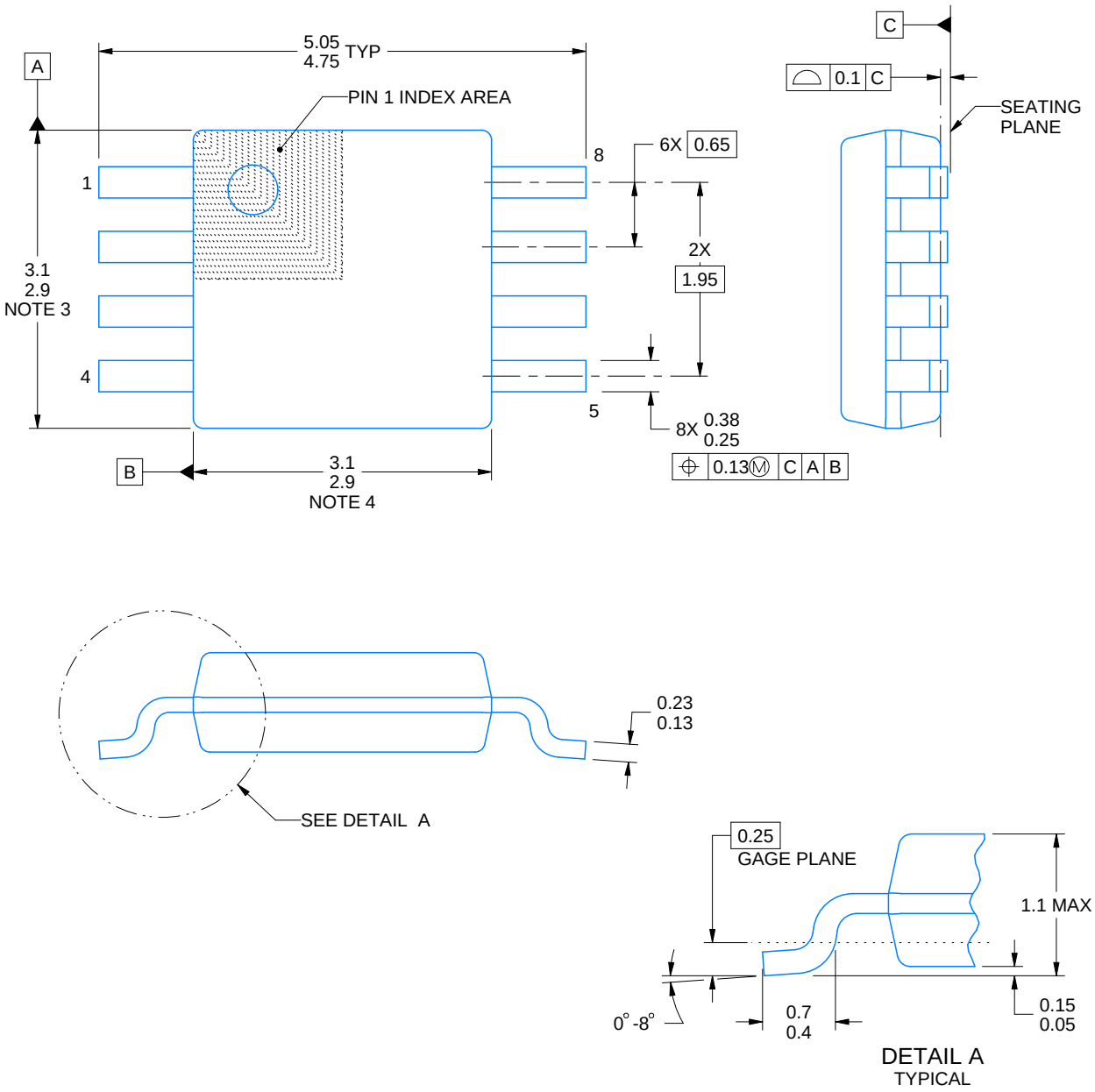
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
INA301A1QDGKRQ1	VSSOP	DGK	8	2500	366.0	364.0	50.0
INA301A1QDGKTQ1	VSSOP	DGK	8	250	366.0	364.0	50.0
INA301A2QDGKRQ1	VSSOP	DGK	8	2500	366.0	364.0	50.0
INA301A2QDGKTQ1	VSSOP	DGK	8	250	366.0	364.0	50.0
INA301A3QDGKRQ1	VSSOP	DGK	8	2500	366.0	364.0	50.0
INA301A3QDGKTQ1	VSSOP	DGK	8	250	366.0	364.0	50.0

PACKAGE OUTLINE

DGK0008A

VSSOP - 1.1 mm max height

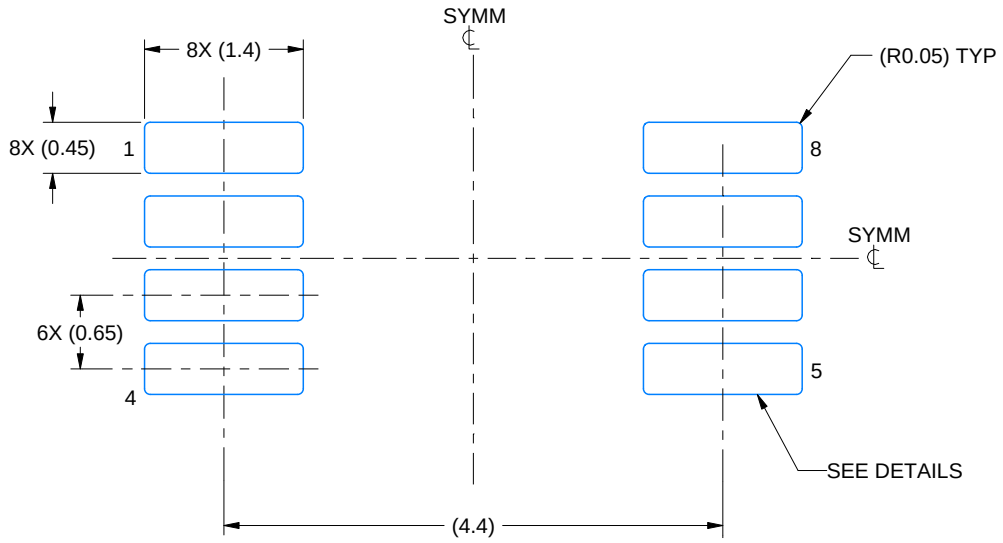
SMALL OUTLINE PACKAGE



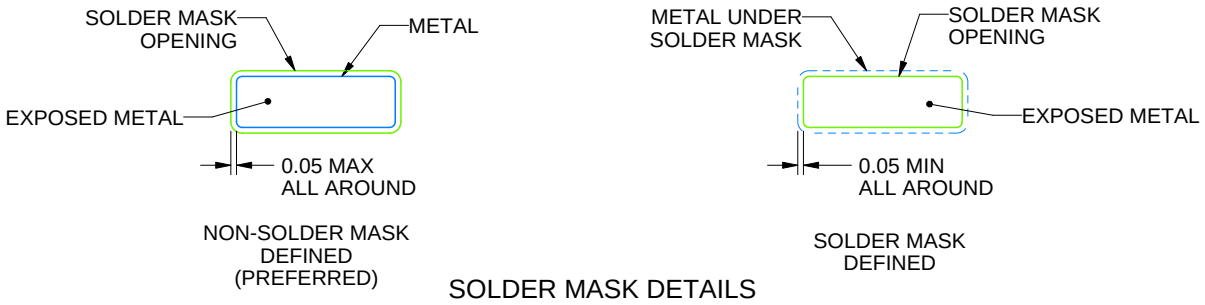
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X

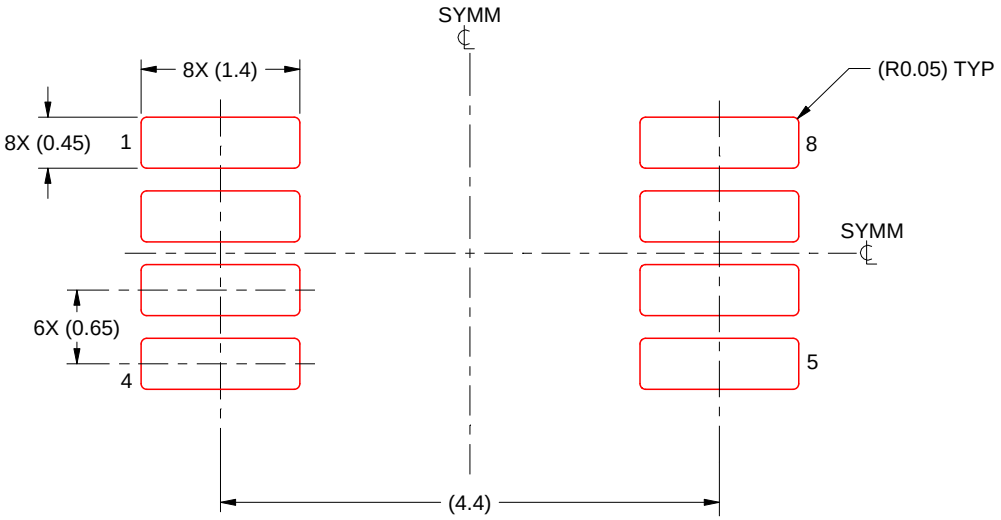


SOLDER MASK DETAILS

4214862/A 04/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
SCALE: 15X

4214862/A 04/2023

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

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