INA317 マイクロパワー(50µA)、ゼロドリフト、レール・ツー・レール出力計測アンプ

1 特長

- 低オフセット電圧: 75µV (最大値)、G≧100
- 低ドリフト: 0.3µV/℃、G≧100
- 低ノイズ: 50nV/√Hz、G≧100
- 高CMRR: 100dB (最大値)、G≧10
- 低い入力バイアス電流: 200pA (最大値)
- 電源電圧範囲: 1.8V～5.5V
- 入力電圧: (V－) 0.1V～(V＋)－0.1V
- 出力範囲: (V－) 0.05V～(V＋)－0.05V
- 低い静止電流: 50µA
- 動作温度範囲: －40℃～＋125℃
- RFIフィルタ付きの入力
- 8ピンのVSSOPパッケージ

2 アプリケーション

- ブリッジ・アンプ
- ECGアンプ
- 圧力センサ
- 医療用計測機器
- ポータブル機器
- 重量計
- 熱電対アンプ
- RTDセンサ・アンプ
- データ収集

3 概要

INA317は、優れた精度を提供する、低消費電力・高精度の計測アンプです。多用途な3オペアンプ構成、コンパクトなサイズ、低消費電力であるため、幅広い携帯型アプリケーションに最適です。

業界標準のゲイン式: G＝1＋(100kΩ/R_G)を使用し、1個の外付け抵抗により1～1000の範囲で任意のゲインを設定できます。

この計測アンプは、低いオフセット電圧(75µV、G≧100)と優れたオフセット電圧ドリフト(0.3µV/℃、G≧100)、高い同相除去(100dB、G≧10)を特長としています。最小1.8V(±0.9V)の電源で動作し、静止電流は50µAであるため、バッテリ駆動システムに最適です。自動較正機能により、拡張工業用温度範囲全体にわたって優れた精度を確保し、DCまでのノイズ密度も低く抑えることができます(50nV/√Hz)。

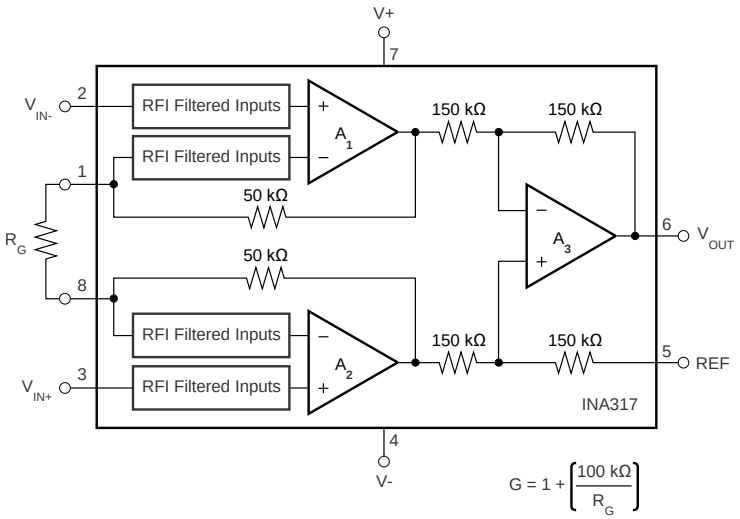
INA317は8ピンVSSOP表面実装パッケージで供給され、T_A＝－40℃～＋125℃の温度範囲で仕様が規定されています。

製品情報(1)

型番	パッケージ	本体サイズ(公称)
INA317	VSSOP (8)	3.00mm×3.00mm

(1) 提供されているすべてのパッケージについては、データシートの末尾にある注文情報を参照してください。

概略回路図



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4 改訂履歴

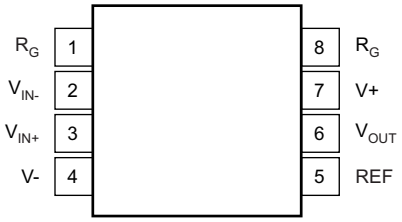
資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

日付	改訂内容	注
2017年11月	*	初版

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5 Pin Configuration and Functions

DGK Package
8-Pin VSSOP
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
REF	5	I	Reference input. This pin must be driven by low impedance or connected to ground.
R_G	1, 8	—	Gain setting pins. For gains greater than 1, place a gain resistor between pins 1 and 8.
V_+	7	—	Positive supply
$V_–$	4	—	Negative supply
V_{IN+}	3	I	Positive input
$V_{IN–}$	2	I	Negative input
V_{OUT}	6	O	Output

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

	MIN	MAX	UNIT
Supply voltage	7		V
Analog input voltage (2)	(V–) – 0.3	(V+) + 0.3	V
Output short-circuit (3)	Continuous		
Operating temperature, T_A	–40	150	°C
Junction temperature, T_J		150	°C
Storage temperature, T_{stg}	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Input pins are diode-clamped to the power-supply rails. Input signals that can swing more than 0.3 V beyond the supply rails must be current limited to 10 mA or less.
(3) Short-circuit to ground.

6.2 ESD Ratings

		VALUE	UNIT
$V_{(ESD)}$ Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±4000	V
	Charged-device model (CDM), per JEDEC specification JESD22-C101 (2)	±1000	
	Machine model (MM)	±200	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
VS	Supply voltage	1.8	5.5	V
	Specified temperature	–40	125	°C

6.4 Thermal Information

THERMAL METRIC (1)		INA317 DGK (VSSOP) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	169.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	62.7	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	90.3	°C/W
ψ_{JT}	Junction-to-top characterization parameter	7.6	°C/W
ψ_{JB}	Junction-to-board characterization parameter	88.7	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	—	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

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6.5 Electrical Characteristics

for V_S = 1.8 V to 5.5 V at T_A = 25°C, R_L = 10 kΩ, V_{REF} = V_S / 2, and G = 1 (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT(1)						
V_{OSI}	Offset voltage, RTI(2)			±10 ±25 / G	±75 ±75 / G	µV
PSR		vs temperature, T_A = –40°C to 125°C			±0.3 ±0.5 / G	µV/°C
		vs power supply,1.8 V ≤ V_S ≤ 5.5 V		±1 ±5 / G	±5 ±15 / G	µV/V
		Long-term stability		See (3)		
	Turnon time to specified V_{OSI}	T_A = –40°C to 125°C		See *Typical Characteristics*		
	Impedance					
Z_{IN}	Differential			100 || 3		GΩ || pF
Z_{IN}	Common-mode			100 || 3		GΩ || pF
V_{CM}	Common-mode voltage range	V_O = 0 V	(V–) + 0.1		(V+) – 0.1	V
CMR	Common-mode rejection	DC to 60 Hz				
		V_{CM} = (V–) + 0.1 V to (V+) – 0.1 V, G = 1	80	90		dB
		V_{CM} = (V–) + 0.1 V to (V+) – 0.1 V, G = 10	100	110		dB
		V_{CM} = (V–) + 0.1 V to (V+) – 0.1 V, G = 100,	100	115		dB
		V_{CM} = (V–) + 0.1 V to (V+) – 0.1 V, G = 1000	100	115		dB
INPUT BIAS CURRENT						
I_B	Input bias current			±70	±200	pA
	vs temperature	T_A = –40°C to 125°C		See 図 26		pA/°C
I_{OS}	Input offset current			±50	±200	pA
	vs temperature	T_A = –40°C to 125°C		See 図 28		pA/°C
INPUT VOLTAGE NOISE						
e_{NI}	Input voltage noise	G = 100, R_S = 0 Ω, f = 10 Hz		50		nV/√Hz
		G = 100, R_S = 0 Ω, f = 100 Hz		50		nV/√Hz
		G = 100, R_S = 0 Ω, f = 1 kHz		50		nV/√Hz
		G = 100, R_S = 0 Ω, f = 0.1 Hz to 10 Hz		1		$µV_{PP}$
i_N	Input current noise	f = 10 Hz		100		fA/√Hz
		f = 0.1 Hz to 10 Hz		2		pA_{PP}
GAIN						
G	Gain equation			1 + (100 kΩ / R_G)		V/V
	Range of gain		1		1000	V/V
	Gain error	V_S = 5.5 V, (V–) + 100 mV ≤ V_O ≤ (V+) – 100 mV				
		G = 1		±0.01%	±0.1%	
		G = 10		±0.05%	±0.25%	
		G = 100		±0.07%	±0.25%	
		G = 1000		±0.25%	±0.5%	
	Gain vs temperature, G = 1	T_A = –40°C to 125°C		±1	±5	ppm/°C
	Gain vs temperature, G > 1(4)	T_A = –40°C to 125°C		±15	±50	ppm/°C
	Gain nonlinearity	V_S = 5.5 V, (V–) + 100 mV ≤ V_O ≤ (V+) – 100 mV				
	Gain nonlinearity, G = 1 to 1000	R_L = 10 kΩ		10		ppm
OUTPUT						
	Output voltage swing from rail	V_S = 5.5 V, R_L = 10 kΩ		See 図 29	50	mV
	Capacitive load drive			500		pF

(1) Total V_{OS}, referred-to-input = (V_{OSI}) + (V_{OSO} / G)
(2) RTI = Referred-to-input
(3) 300-hour life test at 150°C demonstrated randomly distributed variation of approximately 1 µV
(4) Does not include effects of external resistor R_G

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Electrical Characteristics (continued)

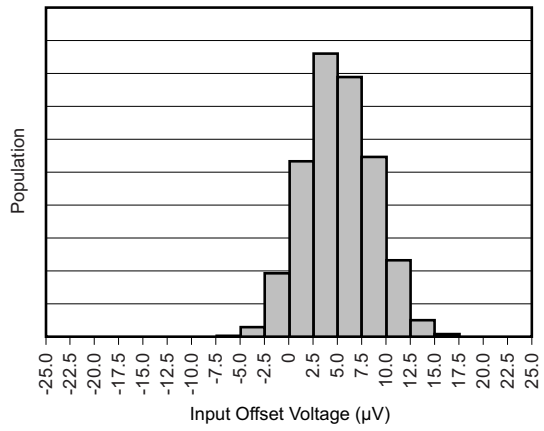
for V_S = 1.8 V to 5.5 V at T_A = 25°C, R_L = 10 kΩ, V_{REF} = V_S / 2, and G = 1 (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{SC}	Short-circuit current	Continuous to common		–40, 5		mA
FREQUENCY RESPONSE						
	Bandwidth, –3 dB	G = 1		150		kHz
		G = 10		35		kHz
		G = 100		3.5		kHz
		G = 1000		350		Hz
SR	Slew rate	V_S = 5 V, V_O = 4-V step, G = 1		0.16		V/µs
		V_S = 5 V, V_O = 4-V step, G = 100		0.05		V/µs
t_S	Settling time to 0.01%	V_{STEP} = 4 V, G = 1		50		µs
		V_{STEP} = 4 V, G = 100		400		µs
t_S	Settling time to 0.001%	V_{STEP} = 4 V, G = 1		60		µs
		V_{STEP} = 4 V, G = 100		500		µs
	Overload recovery	50% overdrive		75		µs
REFERENCE INPUT						
	R_{IN}			300		kΩ
	Voltage range		V–		V+	V
POWER SUPPLY						
	Voltage range	Single voltage range	1.8		5.5	V
		Dual voltage range	±0.9		±2.75	V
I_Q	Quiescent current vs temperature	V_{IN} = V_S / 2		50	75	µA
		T_A = –40°C to 125°C			80	µA
TEMPERATURE RANGE						
	Specified temperature range		–40		125	°C
	Operating temperature range		–40		150	°C

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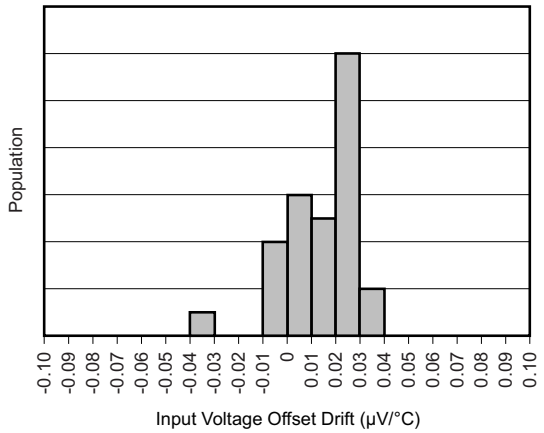
6.6 Typical Characteristics

at T_A = 25°C, V_S = 5 V, R_L = 10 kΩ, V_{REF} = midsupply, and G = 1, (unless otherwise noted)



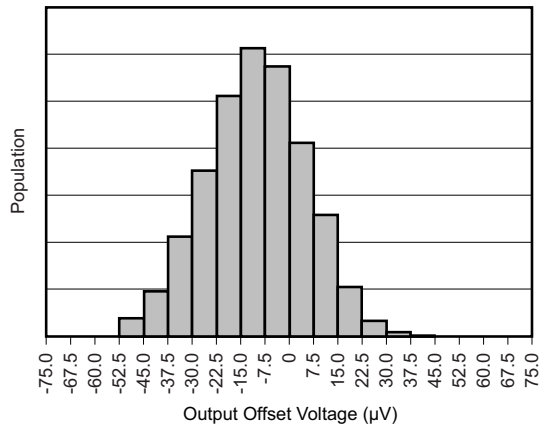
V_S = 5.5 V

図 1. Input Offset Voltage



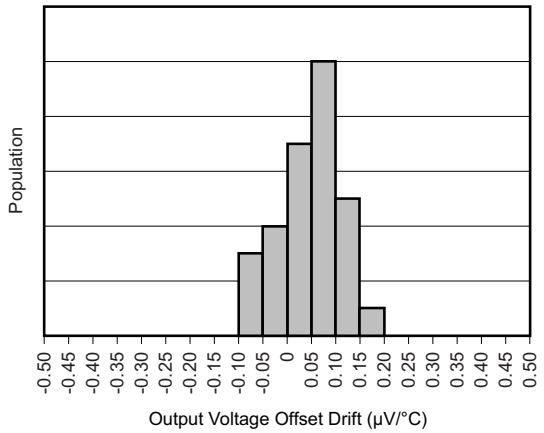
V_S = 5.5 V T_A = –40°C to +125°C

図 2. Input Voltage Offset Drift



V_S = 5.5 V

図 3. Output Offset Voltage



V_S = 5.5 V T_A = –40°C to +125°C

図 4. Output Voltage Offset Drift

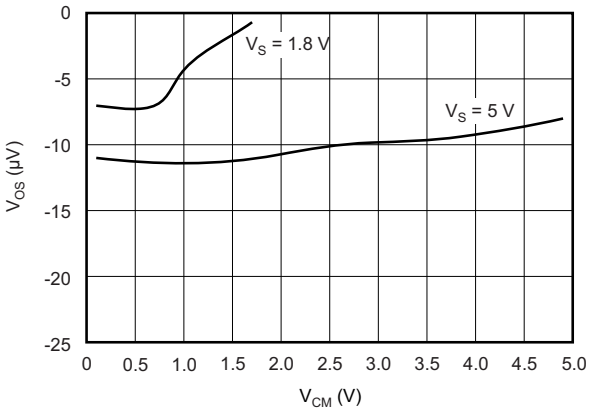
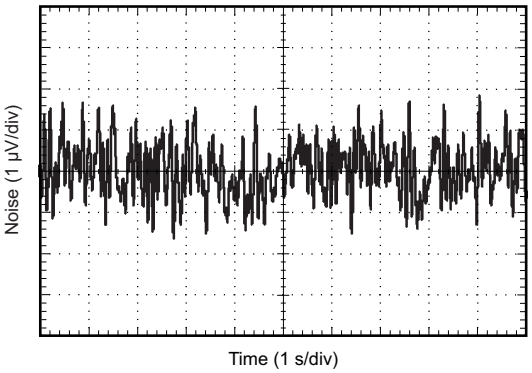


図 5. Offset Voltage vs Common-Mode Voltage



Gain = 1

図 6. 0.1-Hz to 10-Hz Noise

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Typical Characteristics (continued)

at T_A = 25°C, V_S = 5 V, R_L = 10 kΩ, V_{REF} = midsupply, and G = 1, (unless otherwise noted)

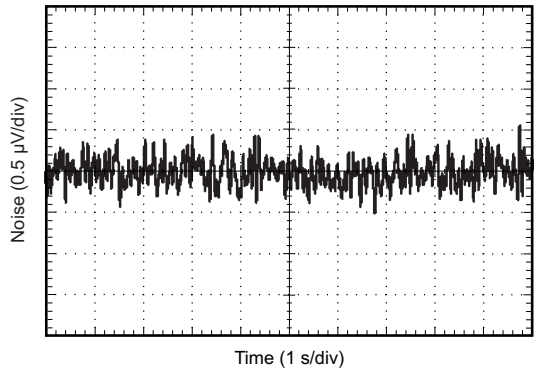


図 7. 0.1-Hz to 10-Hz Noise

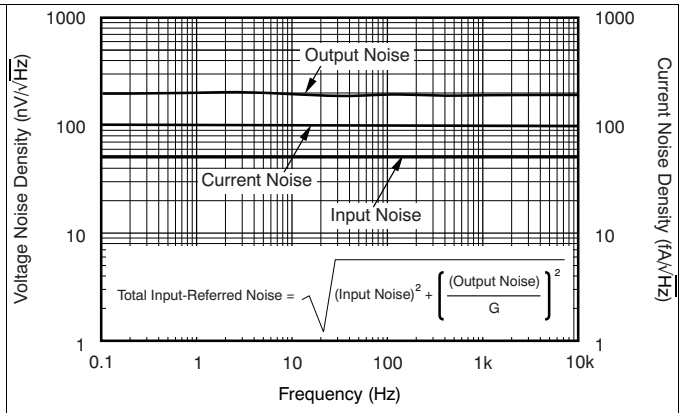


図 8. Spectral Noise Density

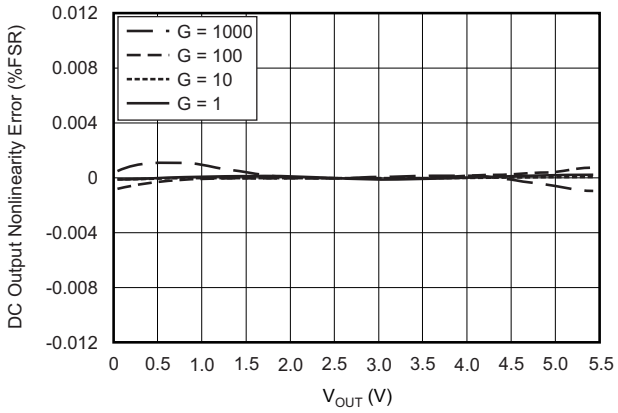


図 9. Nonlinearity Error

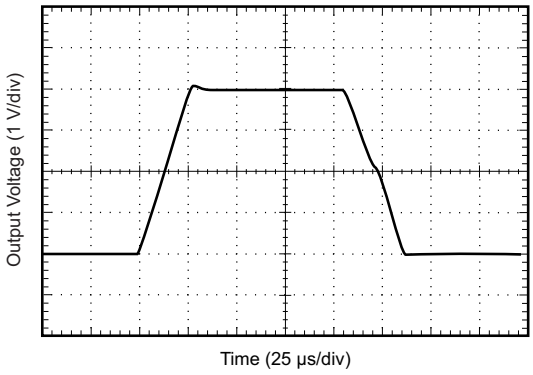


図 10. Large Signal Response

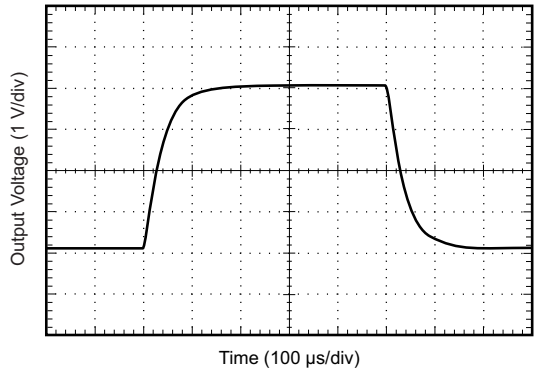


図 11. Large-Signal Step Response

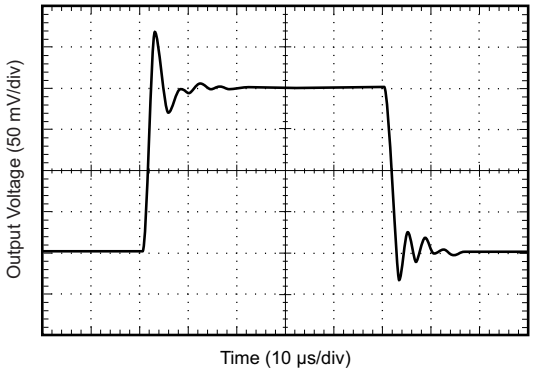


図 12. Small-Signal Step Response

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Typical Characteristics (continued)

at T_A = 25°C, V_S = 5 V, R_L = 10 kΩ, V_{REF} = midsupply, and G = 1, (unless otherwise noted)

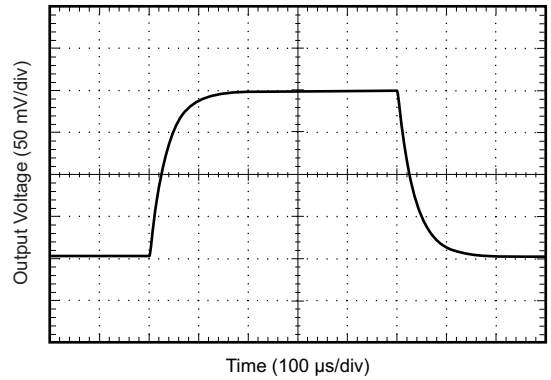


図 13. Small-Signal Step Response

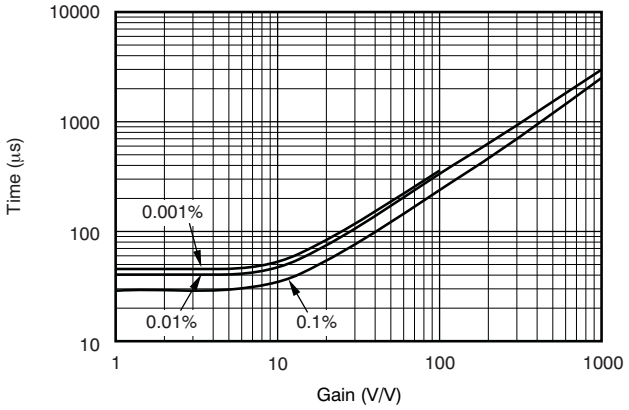


図 14. Settling Time vs Gain

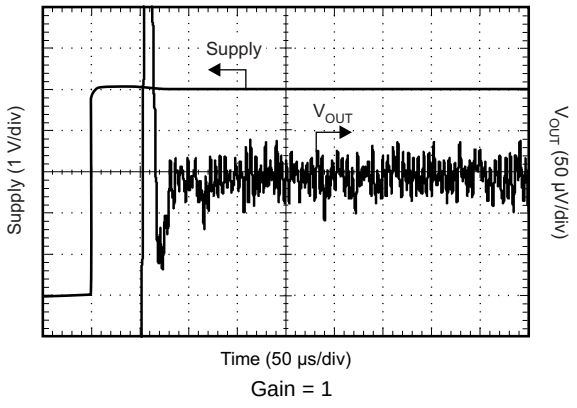


図 15. Start-Up Settling Time

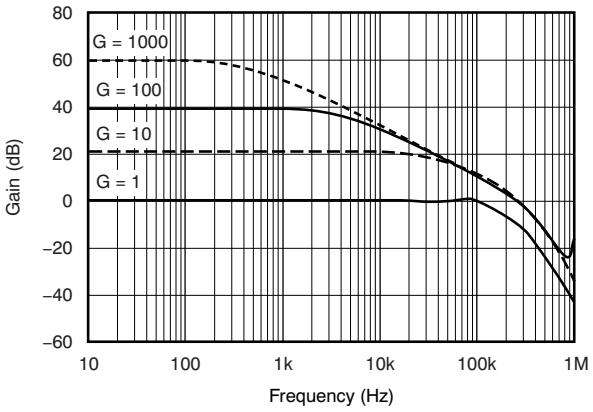


図 16. Gain vs Frequency

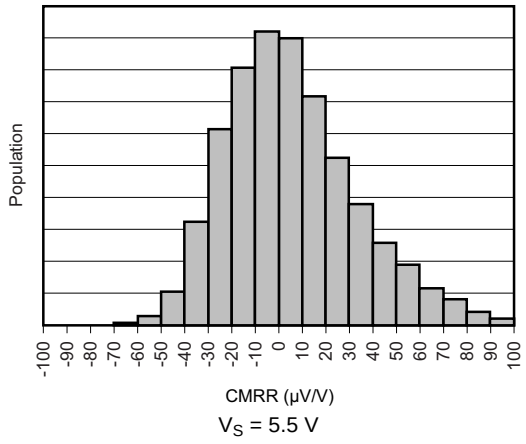


図 17. Common-Mode Rejection Ratio

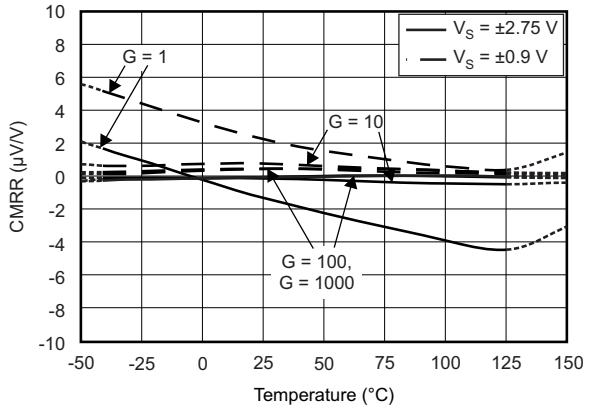


図 18. Common-Mode Rejection Ratio vs Temperature

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Typical Characteristics (continued)

at T_A = 25°C, V_S = 5 V, R_L = 10 kΩ, V_{REF} = midsupply, and G = 1, (unless otherwise noted)

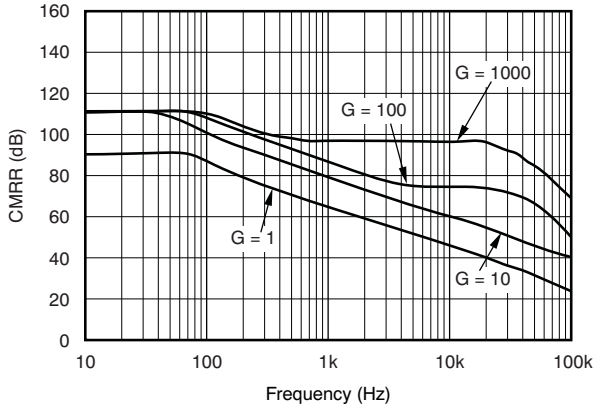
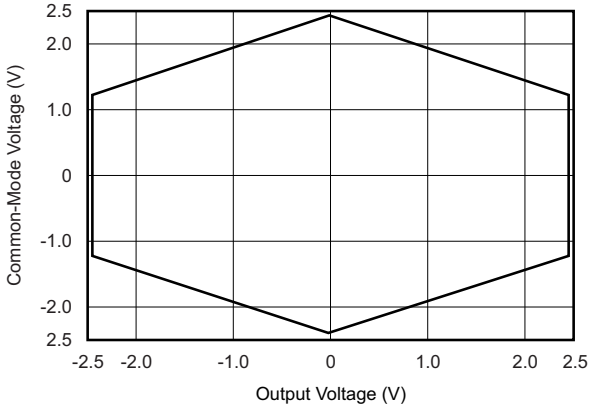
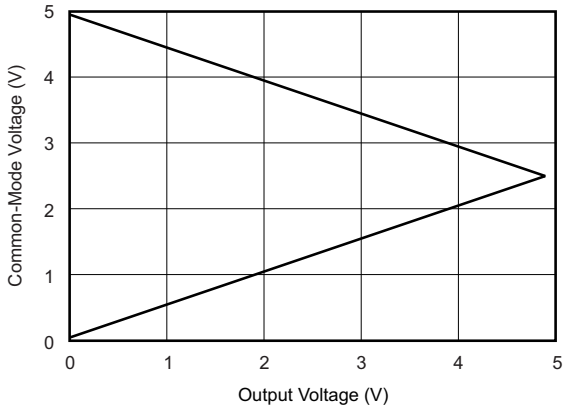


図 19. Common-Mode Rejection Ratio vs Frequency



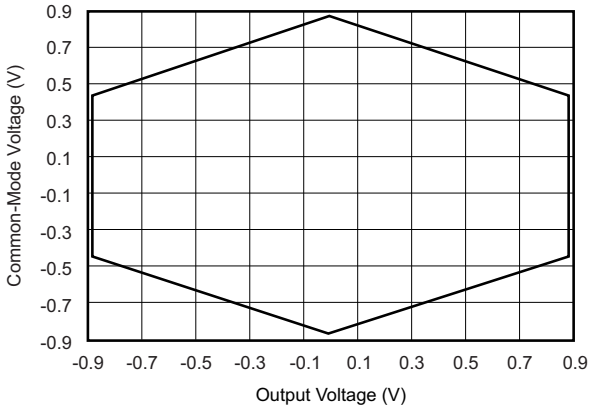
V_S = ±2.5 V V_{REF} = 0 All gains

図 20. Typical Common-Mode Range vs Output Voltage



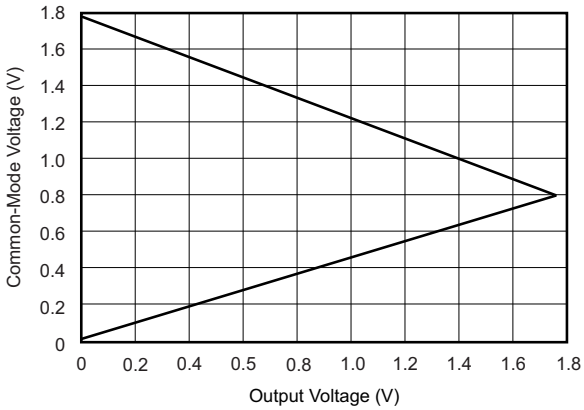
V_S = 5 V V_{REF} = 0 All gains

図 21. Typical Common-Mode Range vs Output Voltage



V_S = ±0.9 V V_{REF} = 0 All gains

図 22. Typical Common-Mode Range vs Output Voltage



V_S = 1.8 V V_{REF} = 0

図 23. Typical Common-Mode Range vs Output Voltage

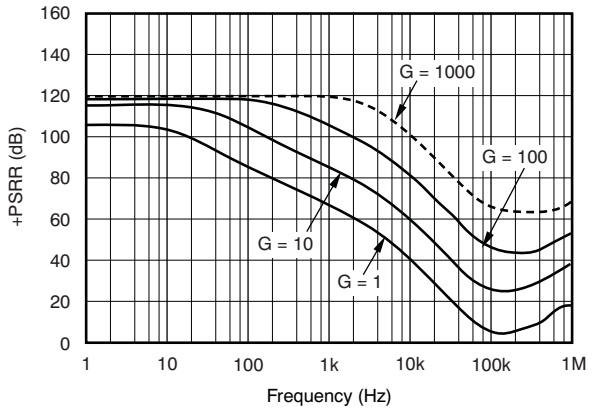


図 24. Positive Power-Supply Rejection Ratio

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Typical Characteristics (continued)

at T_A = 25°C, V_S = 5 V, R_L = 10 kΩ, V_{REF} = midsupply, and G = 1, (unless otherwise noted)

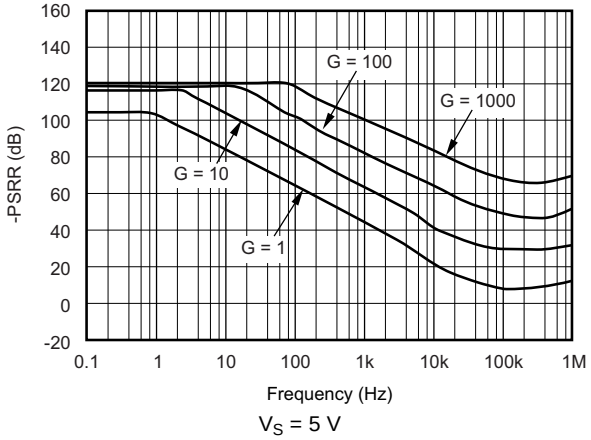


図 25. Negative Power-Supply Rejection Ratio

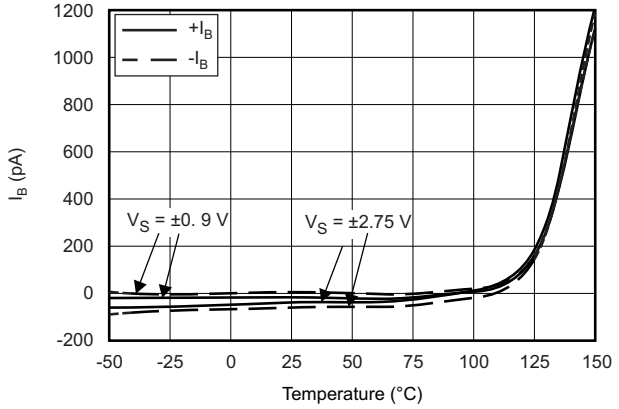


図 26. Input Bias Current vs Temperature

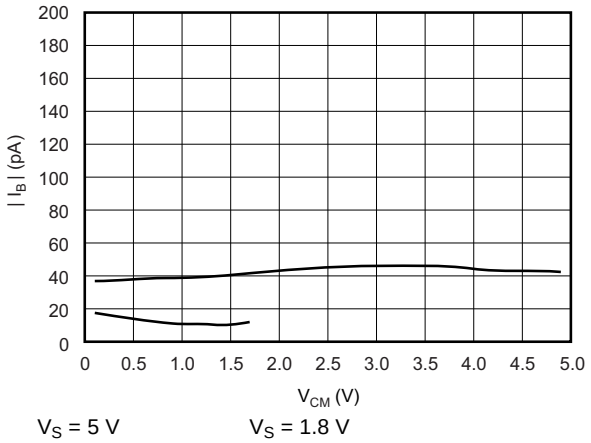


図 27. Input Bias Current vs Common-Mode Voltage

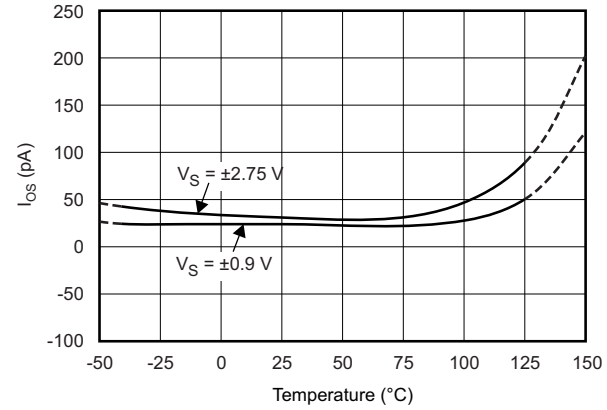


図 28. Input Offset Current vs Temperature

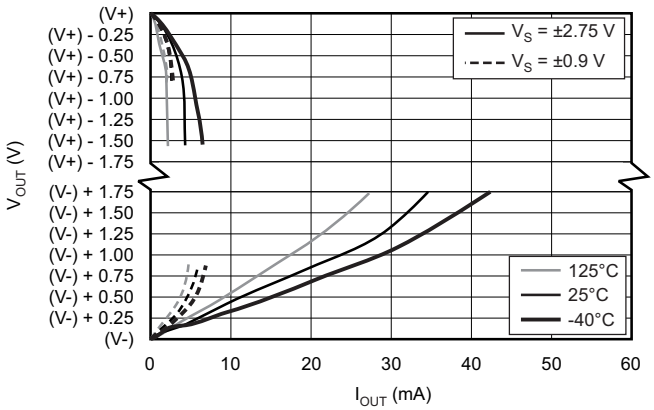


図 29. Output Voltage Swing vs Output Current

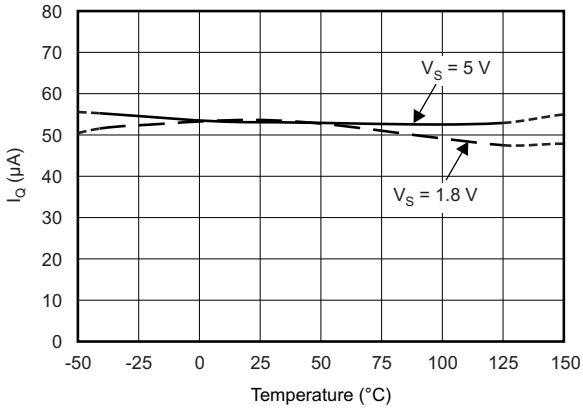


図 30. Quiescent Current vs Temperature

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Typical Characteristics (continued)

at T_A = 25°C, V_S = 5 V, R_L = 10 kΩ, V_{REF} = midsupply, and G = 1, (unless otherwise noted)

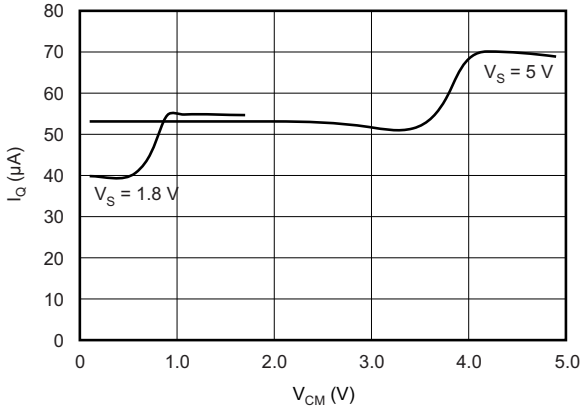


図 31. Quiescent Current vs Common-Mode Voltage

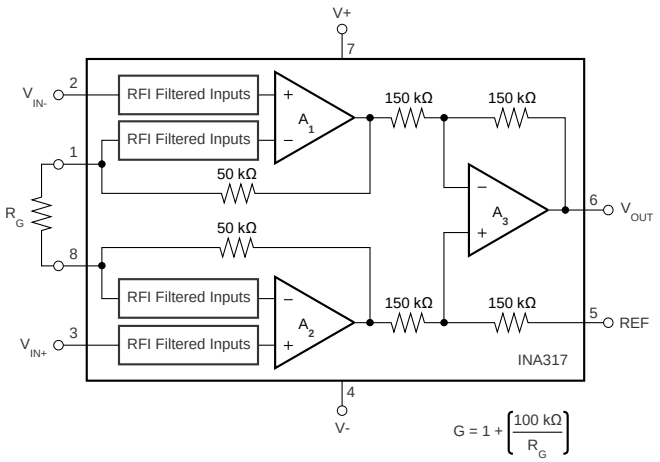
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7 Detailed Description

7.1 Overview

The INA317 is a monolithic instrumentation amplifier (INA) based on the precision zero-drift OPA333 (operational amplifier) core. The INA317 integrates laser-trimmed resistors to ensure excellent common-mode rejection and low gain error. The combination of the zero-drift amplifier core and the precision resistors allows this device to achieve outstanding DC precision and is designed for 3.3-V and 5-V industrial applications.

7.2 Functional Block Diagram



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7.3 Feature Description

The INA317 is a low-power, zero-drift instrumentation amplifier that offers accuracy. The versatile three-operational-amplifier design and small size makes the amplifier designed for a wide range of applications. Zero-drift chopper circuitry provides DC specifications. A single external resistor sets any gain from 1 to 10,000. The INA317 is laser trimmed for high common-mode rejection (100 dB at G ≥ 100). Typically, the INA317 operates with power supplies as low as 1.8 V and quiescent current of 50 µA.

7.4 Device Functional Modes

7.4.1 Internal Offset Correction

INA317 internal operational amplifiers use an autocalibration technique with a time-continuous 350-kHz operational amplifier in the signal path. The amplifier is zero-corrected every 8 µs using a proprietary technique. Upon power up, the amplifier requires approximately 100 µs to achieve specified VOS accuracy. This design has no aliasing or flicker noise.

7.4.2 Input Common-Mode Range

The linear input voltage range of the input circuitry of the INA317 is from approximately 0.1 V below the positive supply voltage to 0.1 V above the negative supply. However, as a differential input voltage causes the output voltage to increase, the output voltage swing of amplifiers A1 and A2 limits the linear input range. As a result, the linear common-mode input range is related to the output voltage of the complete amplifier. This behavior depends on supply voltage; see 図 20.

Input overload conditions can produce an output voltage that appears normal. For example, if an input overload condition drives the input amplifiers to the respective positive output swing limit, the difference voltage measured by the output amplifier is approximately zero. The output of the INA317 is approximately 0 V even though the inputs are overloaded.

8 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

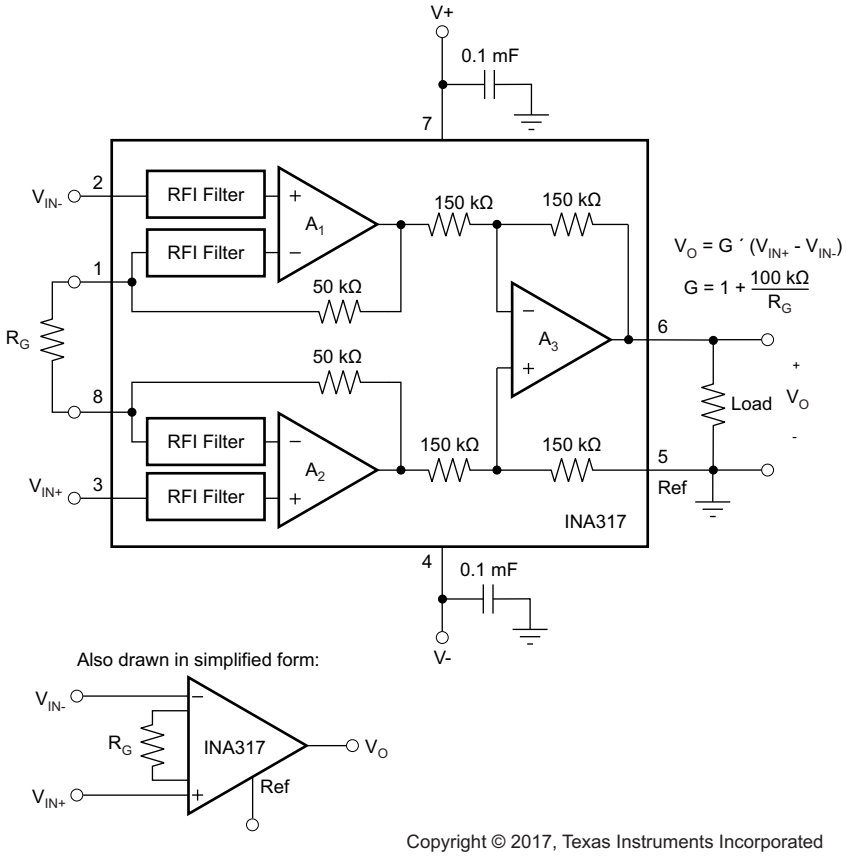
8.1 Application Information

The INA317 measures small differential voltage with high common-mode voltage that develops between the noninverting and inverting input. The high input impedance makes the INA317 designed for a wide range of applications. The ability to set the reference pin to adjust the functionality of the output signal offers additional flexibility that is practical for multiple configurations.

8.2 Typical Application

図 32 shows the basic connections required for operation of the INA317 device. Good layout practice mandates the use of bypass capacitors placed close to the device pins as shown.

The output of the INA317 device is referred to the output reference (REF) pin, which is normally grounded. This connection must be low-impedance to ensure good common-mode rejection. Although 15 Ω or less of stray resistance is tolerated while maintaining specified CMRR, small stray resistances of tens of ohms in series with the REF pin causes noticeable degradation in CMRR.



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図 32. Basic Connections

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Typical Application (continued)

8.2.1 Design Requirements

The device is configured to monitor the input differential voltage when the gain of the external resistor R_G sets the input signal. The output signal references to the REF pin. The most common application is where the output is referenced to ground when no input signal is present by connecting the REF pin to ground. When the input signal increases, the output voltage at the OUT pin increases.

8.2.2 Detailed Design Procedure

8.2.2.1 Setting the Gain

A single external resistor (R_G) that is connected between pins 1 and 8 sets the gain of the INA317. The value of R_G is selected according to 式 1:

$$G = 1 + (100\ k\Omega / R_G) \quad (1)$$

表 1 lists several commonly-used gains and resistor values. The 100 kΩ in 式 1 is a result of the sum of the two internal feedback resistors (A_1 and A_2.) These on-chip resistors are laser trimmed to accurate absolute values. The accuracy and temperature coefficient of these resistors are included in the gain accuracy and drift specifications of the INA317 device.

The stability and temperature drift of the external gain setting resistor (R_G) also affects gain. The contribution of R_G to gain accuracy and drift is inferred from the gain in式 1. Low resistor values required for high gain make wiring resistance important. Sockets add to the wiring resistance and contribute additional gain error (possibly an unstable gain error) in gains of approximately 100 or greater. To ensure stability, avoid parasitic capacitance of more than a few picofarads at the R_G connections. Careful matching of any parasitics on R_G pins maintains optimal CMRR over frequency.

表 1. Commonly-Used Gains and Resistor Values

DESIRED GAIN	R_G (Ω)	NEAREST 1% R_G (Ω)
1	NC(1)	NC
2	100 k	100 k
5	25 k	24.9 k
10	11.1 k	11 k
20	5.26 k	5.23 k
50	2.04 k	2.05
100	1.01 k	1 k
200	502.5	499
500	200.4	200
1000	100.1	100

(1) NC denotes no connection. When using the SPICE model, the simulation does not converge unless a resistor is connected to the R_G pins; use a large resistor value.

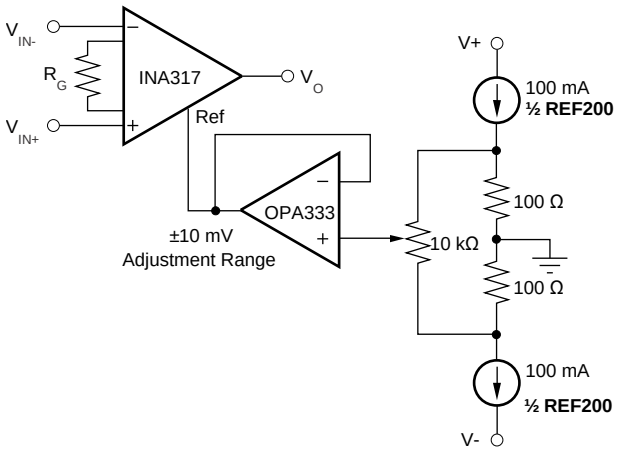
8.2.2.2 Internal Offset Correction

The INA317 device internal operational amplifiers use an autocalibration technique with a time-continuous 350-kHz operational amplifier in the signal path. The amplifier is zero-corrected every 8 µs using a proprietary technique. At power-up, the amplifier requires approximately 100 µs to achieve specified V_{OS} accuracy. This design has no aliasing or flicker noise.

8.2.2.3 Offset Trimming

Most applications require no external offset adjustment. However, apply a voltage to the REF pin to make adjustments if necessary. 図 33 shows an optional circuit for trimming the output offset voltage. The voltage applied to REF pin is added at the output. The operational amplifier buffer provides low impedance at the REF pin to preserve good common-mode rejection.

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図 33. Optional Trimming of Output Offset Voltage

8.2.2.4 Noise Performance

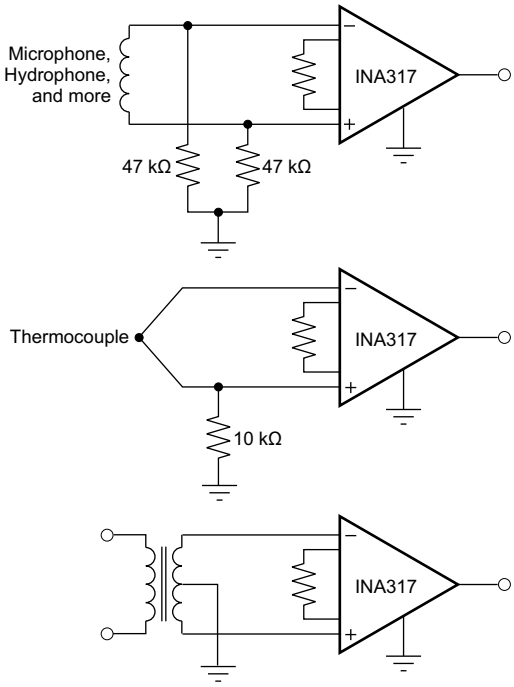
The autocalibration technique used by the INA317 device results in reduced low-frequency noise, typically only 50 nV/√Hz (G = 100). The spectral noise density is shown in 図 8. Low-frequency noise of the INA317 device is approximately 1 μV_{PP} measured from 0.1 Hz to 10 Hz (G = 100).

8.2.2.5 Input Bias Current Return Path

The input impedance of the INA317 device is extremely high(approximately 100 GΩ.) However, a path must be provided for the input bias current of the inputs. This input bias current is typically ±70 pA. High-input impedance means that this input bias current changes very little with varying input voltage.

For proper operation, input circuitry must provide a path for the input bias current. 図 34 shows various provisions for an input bias current path. Without a bias current path, the inputs float to a potential that exceeds the common-mode range of the INA317 device, and the input amplifiers saturate. If the differential source resistance is low, the bias current return path connects to one input (see the thermocouple example in 図 34). With higher source impedance, using two equal resistors provides a balanced input with possible advantages of lower input offset voltage as a result of bias current and better high-frequency common-mode rejection.

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図 34. Providing an Input Common-Mode Current Path

8.2.2.6 Input Common-Mode Range

The linear input voltage range of the input circuitry of the INA317 device is from approximately 0.1 V below the positive supply voltage to 0.1 V above the negative supply. As a differential input voltage causes the output voltage to increase, however, the linear input range is limited by the output voltage swing of amplifiers A_1 and A_2. The linear common-mode input range is related to the output voltage of the complete amplifier. This behavior depends on supply voltage(see 図 20 to 図 23 in the *Typical Characteristics* section.)

Input overload conditions can produce an output voltage that appears normal. For example, if an input overload condition drives both input amplifiers to the respective positive output swing limit, the difference voltage measured by the output amplifier is near zero. The output of the INA317 is near 0 V even though both inputs are overloaded.

8.2.2.7 Operating Voltage

The INA317 operates over a power-supply range of 1.8 V to 5.5 V (±0.9 V to ±2.75 V). Supply voltages higher than 7 V (absolute maximum) can permanently damage the device. Parameters that vary over supply voltage or temperature are shown in the *Typical Characteristics* section of this data sheet.

8.2.2.8 Low Voltage Operation

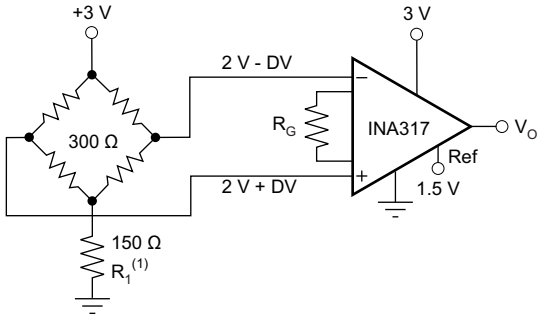
The INA317 device operates on power supplies as low as ±0.9 V. Most parameters vary only slightly throughout this supply voltage range; see the *Typical Characteristics* section. Operation at very low supply voltage requires careful attention to ensure that the input voltages remain within the linear range. Voltage swing requirements of internal nodes limit the input common-mode range with low power supply voltage. 図 20 to 図 23 show the range of linear operation for various supply voltages and gains.

8.2.2.9 Single-Supply Operation

The INA317 device can be used on single power supplies of 1.8 V to 5.5 V. 図 35 shows a basic single-supply circuit. The output REF pin is connected to midsupply. Zero differential input voltage demands an output voltage of midsupply. Actual output voltage swing is limited to approximately 50 mV more than ground when the load is referred to ground as shown. 図 29 shows how the output voltage swing varies with output current.

With single-supply operation, V_{IN+} and $V_{IN–}$ must be 0.1 V more than ground for linear operation. For instance, the inverting input cannot connect to ground to measure a voltage that is connected to the noninverting input.

To show the issues affecting low voltage operation, see 図 35. 図 35 shows the INA317 device operating from a single 3-V supply. A resistor in series with the low side of the bridge ensures that the bridge output voltage is within the common-mode range of the amplifier inputs.



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(1) R_1 creates proper common-mode voltage only for low-voltage operation; see *Single-Supply Operation*.

図 35. Single-Supply Bridge Amplifier

8.2.2.10 Input Protection

The input pins of the INA317 device are protected with internal diodes that are connected to the power-supply rails. These diodes clamp the applied signal to prevent the signal from damaging the input circuitry. If the input signal voltage exceeds the power supplies by more than 0.3 V, the input signal current must be limited to less than 10 mA to protect the internal clamp diodes. Limit the current with a series input resistor. Some signal sources are inherently current limited and do not require limiting resistors.

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8.2.3 Application Curves

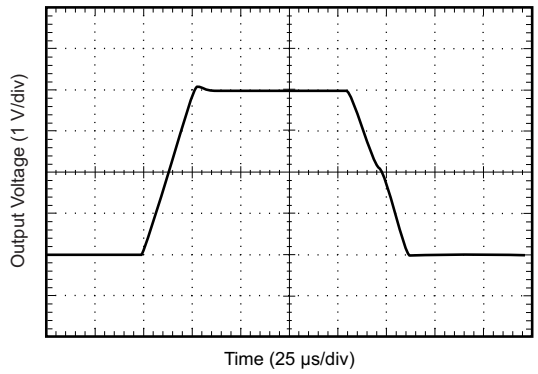


図 36. Large Signal Response

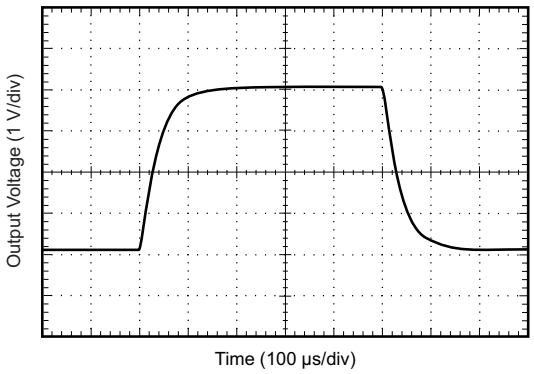


図 37. Large-Signal Step Response

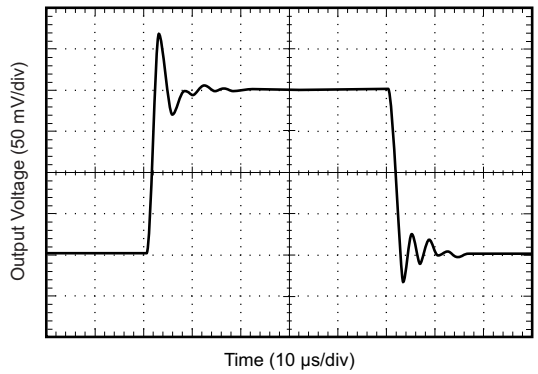


図 38. Small-Signal Step Response

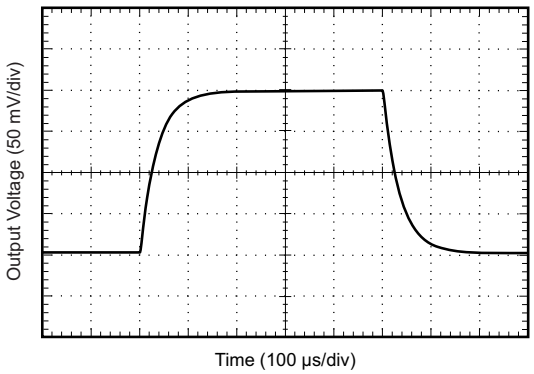


図 39. Small-Signal Step Response

9 Power Supply Recommendations

The minimum power supply voltage for INA317 is 1.8 V and the maximum power supply voltage is 5.5 V. For optimum performance, 3.3 V to 5 V is recommended. TI recommends adding a bypass capacitor at the input to compensate for the layout and power supply source impedance.

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10 Layout

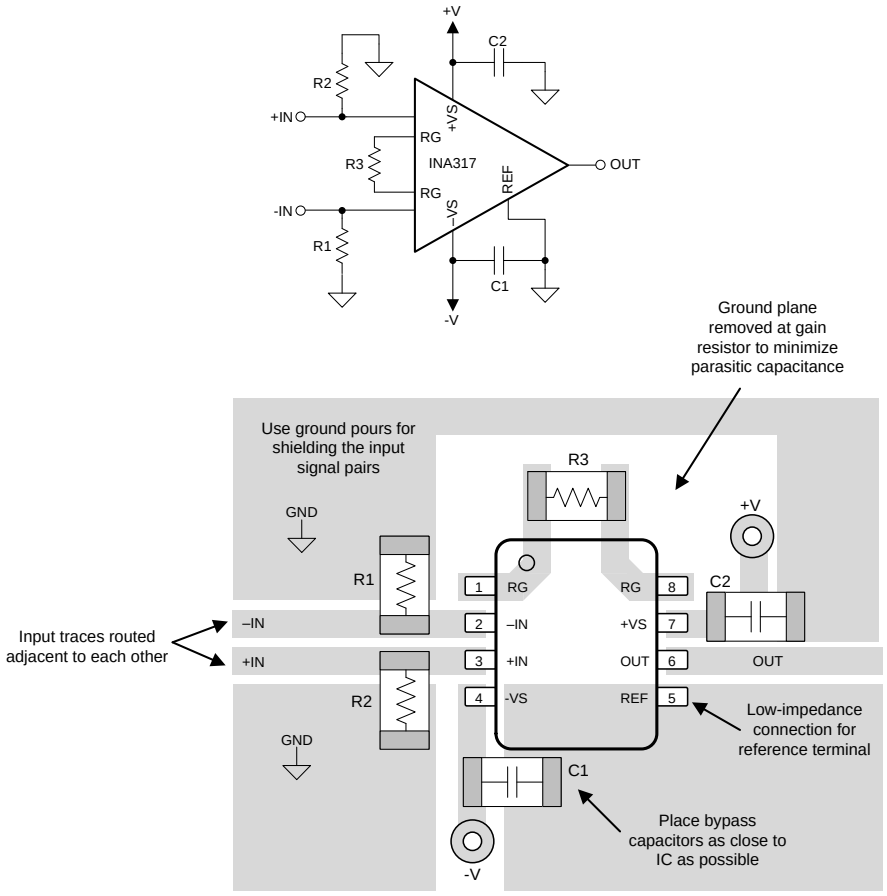
10.1 Layout Guidelines

TI recommends paying attention to good layout practices. Keep traces short and use a printed-circuit-board (PCB) ground plane with surface-mount components placed as close to the device pins as possible. Place a 0.1-µF bypass capacitor as close as possible the supply pins. Apply these guidelines throughout the analog circuit to improve performance and reduce electromagnetic interference (EMI) susceptibility.

Instrumentation amplifiers vary in the susceptibility to radio-frequency interference (RFI). RFI is identified as a variation in offset voltage or DC signal levels with changes in the interfering RF signal. The INA317 device is designed to minimize susceptibility to RFI by incorporating passive RC filters with an 8-MHz corner frequency at the V_{IN+} and $V_{IN–}$ inputs. As a result, the INA317 device demonstrates low sensitivity compared to previous generation devices. However, strong RF fields can cause varied offset levels and may require additional shielding.

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10.2 Layout Example



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図 40. INA317 Layout

11 デバイスおよびドキュメントのサポート

11.1 デバイス・サポート

11.1.1 開発サポート

11.1.1.1 TINA-TI (無料のダウンロード・ソフトウェア)

TINA-TI SPICEベースのアナログ・シミュレーション・プログラムを**INA317**で使用する

TINAは、SPICEエンジンをベースにした単純かつ強力な、使いやすい回路シミュレーション・プログラムです。TINA-TIはTINAソフトウェアの無料バージョンで、完全な機能を持ち、パッシブとアクティブ両方のモデルに加えて、マクロ・モデルのライブラリがプリロードされています。TINA-TIには、SPICEの標準的なDC解析、過渡解析、周波数ドメイン解析などの全機能に加え、追加の設計機能が搭載されています。

TINA-TIはAnalog eLab Design Centerから無料でダウンロードでき、ユーザーが結果をさまざまな方法でフォーマットできる、広範な後処理機能を備えています。

仮想計測器により、入力波形を選択し、回路ノード、電圧、および波形をプローブして、動的なクイック・スタート・ツールを作成できます。

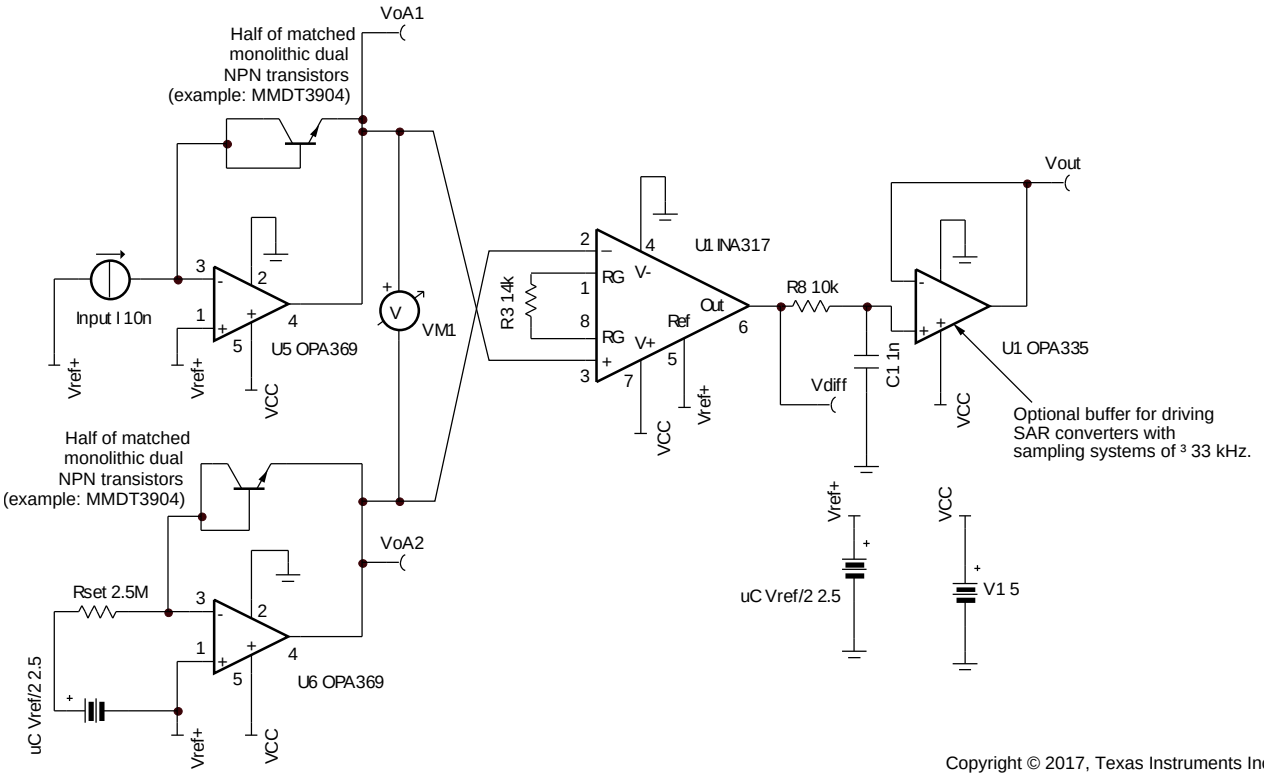
INA317用のTINA-TI回路の例を、図 41および図 42に示します。これによって、特定のアプリケーション用の回路設計を開発、変更、および評価できます。これらのシミュレーション・ファイルのダウンロード用リンクを以下に示します。

注

これらのファイルを使用するには、TINAソフトウェア(DesignSoftから入手できます)またはTINA-TIソフトウェアがインストールされている必要があります。TINA-TIフォルダから、無料のTINA-TIソフトウェアをダウンロードしてください。

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デバイス・サポート (continued)



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(1) 次のリンクからTIの対数アンプのWebページを開くことができます: 対数アンプ製品のホームページ

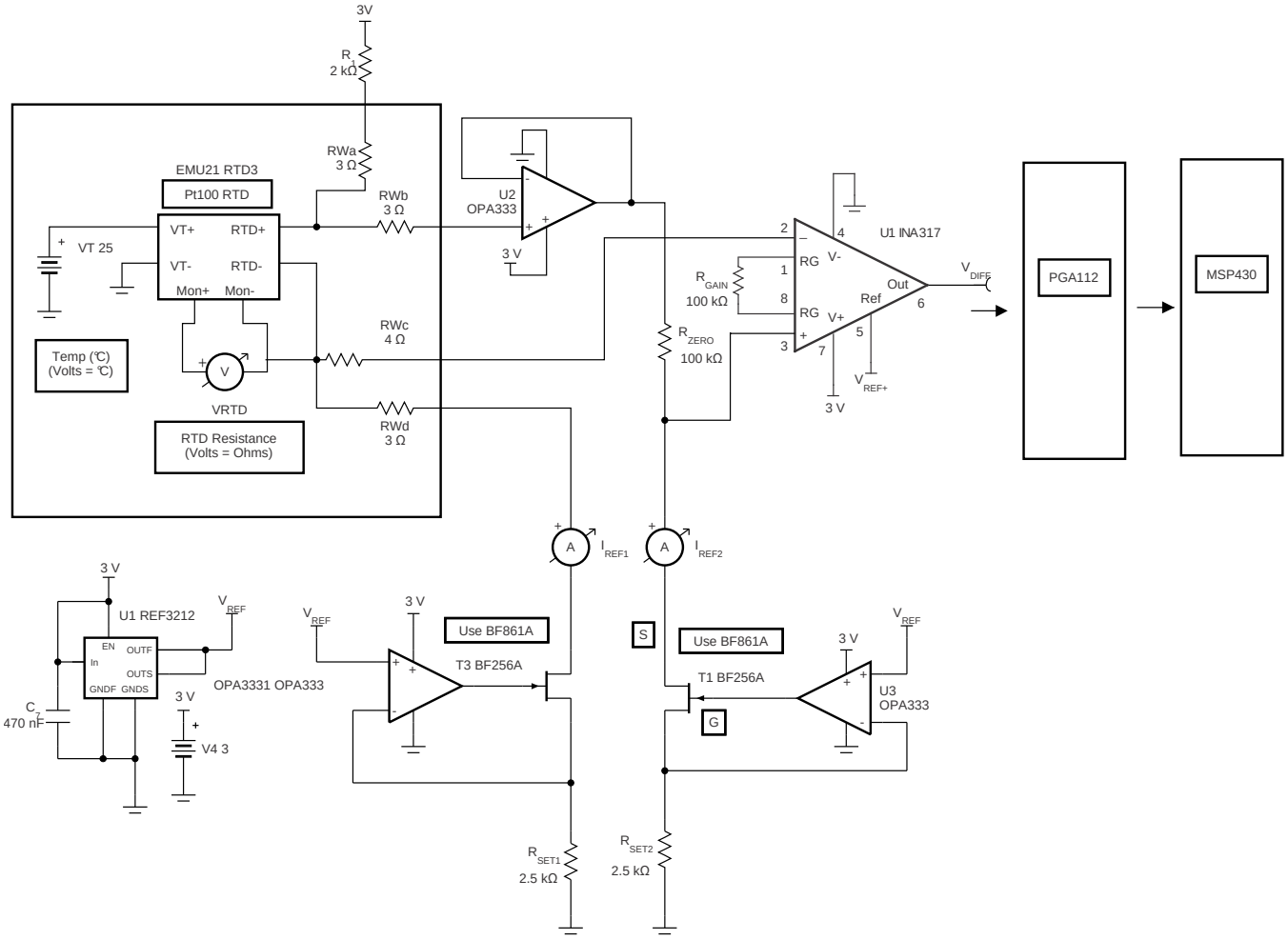
(2) ログ・トランジスタの温度補償は示されていません。

(3) モノリシック対数アンプ(LOG112、LOG114など)については、脚注1のリンクを参照してください。

図 41. 携帯型バッテリ駆動システム用低消費電力ログ機能回路 (例: 血糖計)

この回路用のTINA-TIシミュレーション・ファイルを収めた圧縮ファイルをダウンロードするには、次のリンクをクリックしてください: ログ回路

デバイス・サポート (continued)



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RWa、RWb、RWc、RWdは配線抵抗をシミュレートします。これらの抵抗は、ラインの不整合に対する4線式センス手法の耐性を示すために含まれています。この方法では、4線式RTDの使用を仮定しています。

図 42. プログラマブル·ゲイン·アクイジション·システムを備えたPT100 RTD用4線式3Vコンディショナー

この回路用のTINA-TIシミュレーション・ファイルを収めた圧縮ファイルをダウンロードするには、次のリンクをクリックしてください: PT100 RTD

11.2 ドキュメントのサポート

11.2.1 関連資料

関連資料については、以下を参照してください。

- *『高精度、低ノイズ、レール・ツー・レール出力、36V、ゼロドリフト・オペアンプ』*
- *『50μV VOS、0.25μV/℃、35μA CMOSオペアンプ・ゼロドリフト・シリーズ』*
- *『4ppm/℃、100μA、SOT23-6シリーズ基準電圧』*
- *『基板のレイアウト技法』*

11.3 商標

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11.4 静電気放電に関する注意事項



これらのデバイスは、限定的なESD（静電破壊）保護機能を内 蔵しています。保存時または取り扱い時は、MOSゲートに対す る静電破壊を防止するために、リード線同士をショートさせて おくか、デバイスを導電フォームに入れる必要があります。

11.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

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12 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。この情報は、そのデバイスについて利用可能な最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
INA317IDGKR	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAU | SN | NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	I317
INA317IDGKR.A	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	I317
INA317IDGKT	Active	Production	VSSOP (DGK) | 8	250 | SMALL T&R	Yes	NIPDAU | SN | NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	I317
INA317IDGKT.A	Active	Production	VSSOP (DGK) | 8	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	I317

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

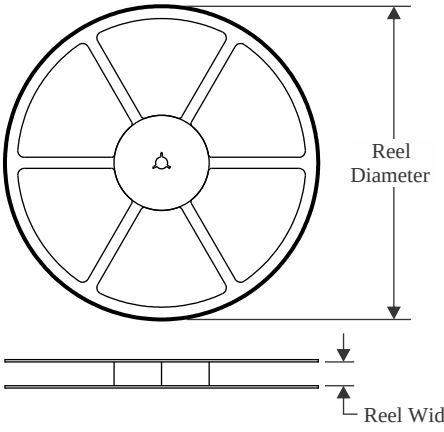
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

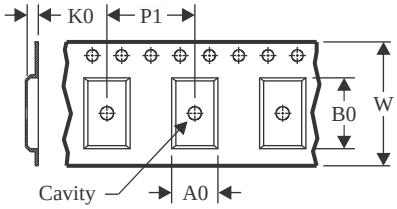
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

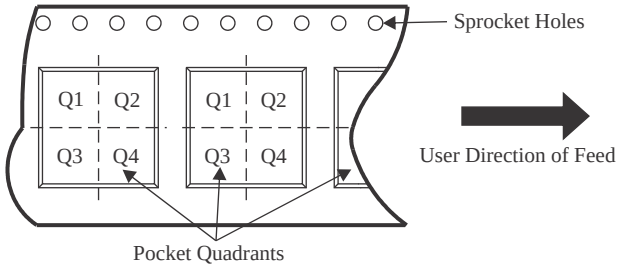


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

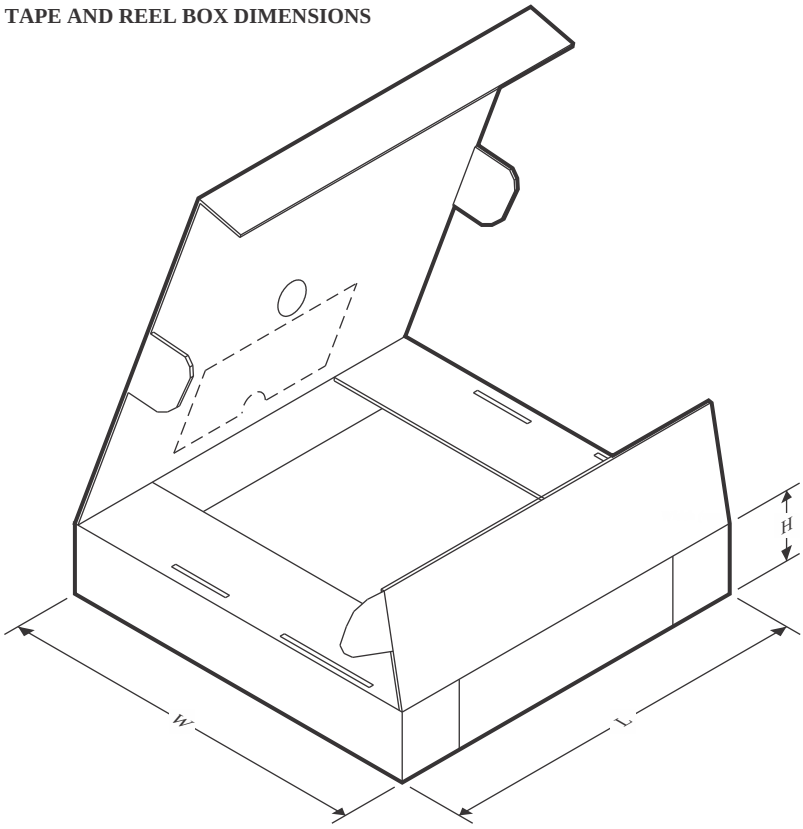
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
INA317IDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.25	3.35	1.25	8.0	12.0	Q1
INA317IDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
INA317IDGKT	VSSOP	DGK	8	250	330.0	12.4	5.25	3.35	1.25	8.0	12.0	Q1
INA317IDGKT	VSSOP	DGK	8	250	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

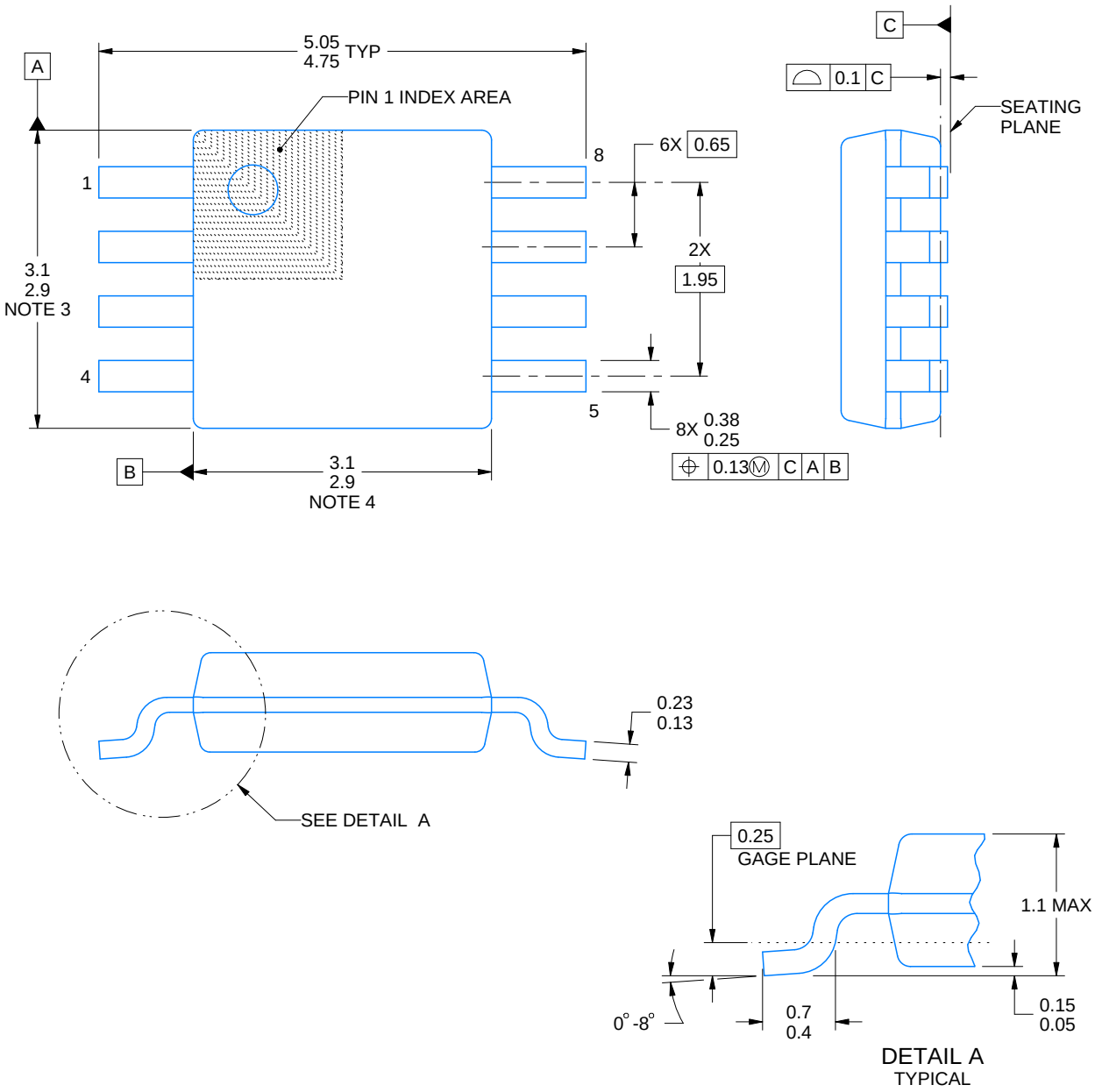
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
INA317IDGKR	VSSOP	DGK	8	2500	366.0	364.0	50.0
INA317IDGKR	VSSOP	DGK	8	2500	366.0	364.0	50.0
INA317IDGKT	VSSOP	DGK	8	250	366.0	364.0	50.0
INA317IDGKT	VSSOP	DGK	8	250	353.0	353.0	32.0

PACKAGE OUTLINE

DGK0008A

VSSOP - 1.1 mm max height

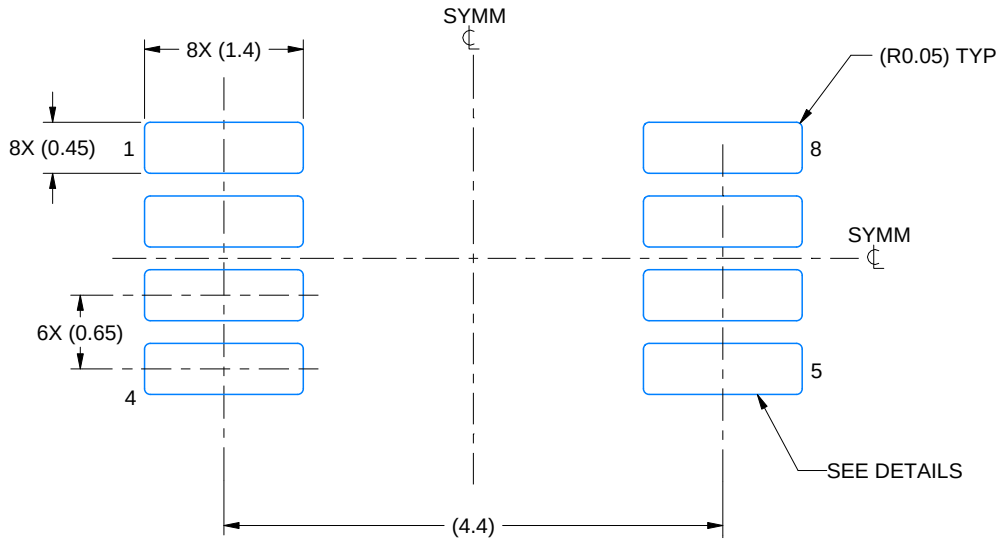
SMALL OUTLINE PACKAGE



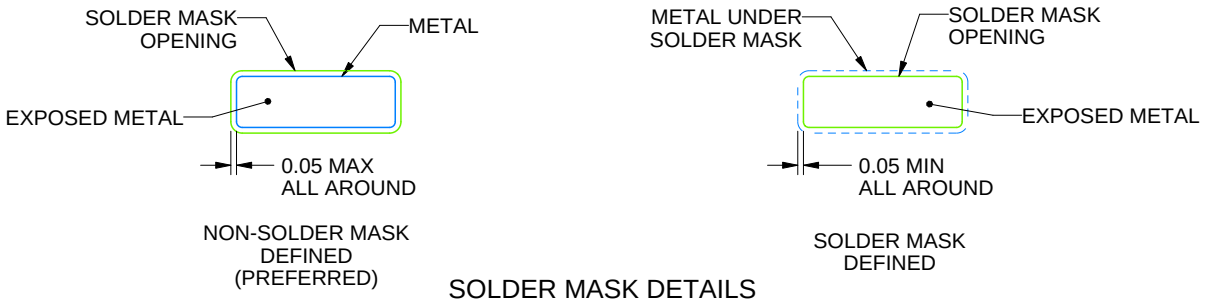
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X

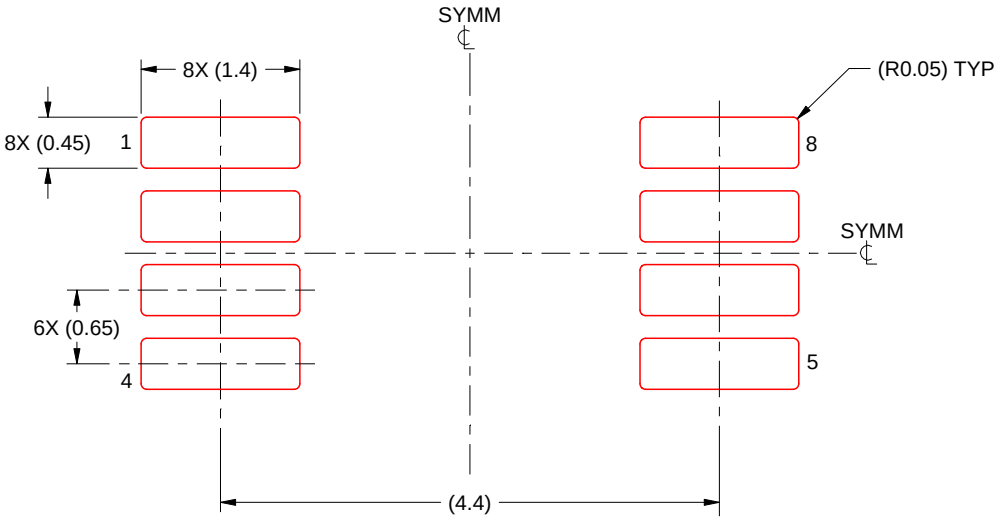


SOLDER MASK DETAILS

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NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
SCALE: 15X

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NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

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