INA381 26V、高速、コンパレータ内蔵の電流検出アンプ

1 特長

- 同相入力範囲：-0.2V～+26V
- 高精度アンプ
  - T_A = 25℃でのオフセット電圧
    - V_{CM} = 12V で 500µV (最大値)
    - V_{CM} = 0V で 150µV (最大値)
  - オフセット電圧ドリフト:1µV/℃ (最大値)
  - ゲイン誤差:25℃で 1% (最大値)
  - ゲイン誤差ドリフト:20ppm/℃ (最大値)
- アンプ・ゲインを選択可能
  - INA381A1: 20V/V
  - INA381A2: 50V/V
  - INA381A3: 100V/V
  - INA381A4: 200V/V
- オープン・ドレインのコンパレータ
  - ヒステリシス:50mV
  - 伝播遅延:400ns (標準値)
  - 外部の基準電圧によってアラートのスレッショルドを設定
  - 透過モードとラッチ・モードをサポート
- パッケージ：VSSOP-10 および WSON-8

2 アプリケーション

- 商用ネットワークとサーバーの PSU (電源)
- 商用 DC/DC
- DC 入力 BLDC モーター・ドライブ
- コードレス電動工具
- ヘッドセット、ヘッドフォン、イヤフォン

3 概要

INA381 は、26V 同相電流センシング・アンプと高速コンパレータを内蔵しています。このデバイスは、電流シャント抵抗の両端に生じた電圧を測定し、コンパレータ基準ピンで設定されたユーザー定義のスレッショルド制限値とその電圧を比較することで過電流状態を検出します。この電流シャント・モニタは、電源電圧にかかわらず、-0.2V から 26V まで変化する同相電圧上で差動電圧信号を測定できます。

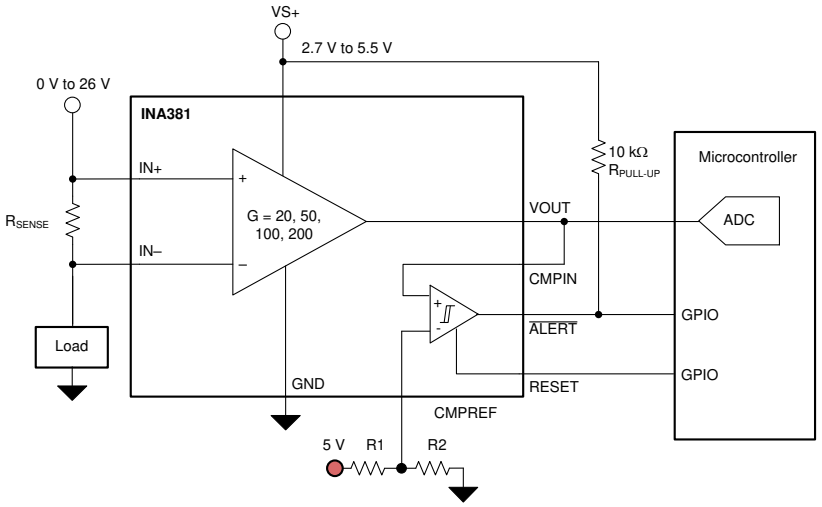
オープン・ドレインのアラート出力は、2 つのモード (透過、ラッチ) で動作するように構成できます。透過モードでは、出力状態は入力状態に従います。ラッチ・モードでは、ラッチがリセットされた場合のみアラート出力がクリアされます。スタンドアロン・コンパレータの大信号アラートの応答時間は 2µs 未満であるため、過電流を迅速に検出できます。INA381 を使うと、システムの過電流保護の総応答時間を 10µs 未満にできます。

製品情報(1)

型番	パッケージ	本体サイズ(公称)
INA381	VSSOP (10)	3.00mm×3.00mm
	WSON (8)	2.00mm×2.00mm

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にあるパッケージ・オプションについての付録を参照してください。

代表的なアプリケーション



英語版のTI製品についての情報を翻訳したこの資料は、製品の概要を確認する目的で便宜的に提供しているものです。該当する正式な英語版の最新情報は、www.ti.comで閲覧でき、その内容が常に優先されます。TIでは翻訳の正確性および妥当性につきましては一切保証いたしません。実際の設計などの前には、必ず最新版の英語版をご参照くださいますようお願いいたします。

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4 改訂履歴

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Revision A (April 2018) から **Revision B** に変更 **Page**

- DGS (VSSOP-8) パッケージおよび関連コンテンツをデータシートに 追加 ... 1
- 「特長」のオフセット誤差およびゲイン誤差についての箇条書き項目に規定温度を 追加 ... 1
- 「特長」の箇条書き項目で、応答時間 500ns を伝播遅延 400ns に 変更 ... 1
- 「アプリケーション」の箇条書きを新しい項目に 変更 ... 1
- Added plus-minus symbol to TYP and MAX values of comparator offset voltage ... 6
- 変更 Figure 54 to remove reset connection to supply ... 31

2017年12月発行のものから更新 **Page**

- 量産にリリース ... 1

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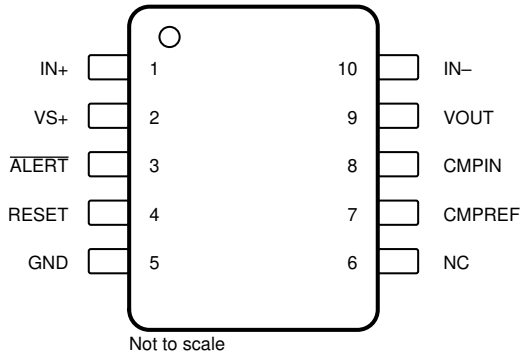
5 概要（続き）

このデバイスは 2.7V～5.5V の単一電源で動作し、最大消費電流は 350µA です。このデバイスは -40℃～+125℃の温度範囲で動作が規定されており、8 ピン WSON および 10 ピン VSSOP パッケージで供給されます。

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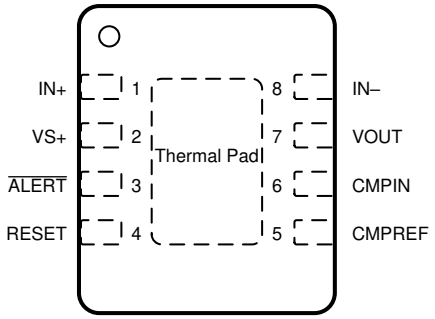
6 Pin Configuration and Functions

DGS Package
10-Pin VSSOP
Top View



Not to scale

DSG Package
8-Pin WSON
Top View



Not to scale

Pin Functions

PIN			TYPE	DESCRIPTION
NAME	DGS	DSG		
$\overline{\text{ALERT}}$	3	3	Digital output	Overlimit alert, active low, open-drain output
CMPIN	8	6	Analog input	Signal input to the comparator
CMPREF	7	5	Analog input	Input reference to the comparator
GND	5	—	Ground	Device ground. Connect the thermal pad to the system ground. See the layout example in 図 54.
IN–	10	8	Analog input	Connect this pin to the load side of the shunt resistor
IN+	1	1	Analog input	Connect this pin to the supply side of the shunt resistor
NC	6	—	—	Not internal connection to device. This pin can be left floating, grounded, or connected to the supply.
RESET	4	4	Digital input	Transparent or latch mode selection input. See the *Alert Modes* section for a detailed description on pin connections.
VOUT	9	7	Analog output	Current-sense amplifier output voltage
VS+	2	2	Supply	Power supply: 2.7 V to 5.5 V
Thermal Pad	—	Thermal Pad	—	Ground reference for the device that is also the thermal pad used to conduct heat from the device. Tie this pad externally to ground.

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7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_S	Supply voltage			6	V
V_{IN+},$V_{IN–}$	Analog inputs (IN+, IN–)	Differential (V_{IN+}) – ($V_{IN–}$)(2)	–26	26	V
		Common-mode (3)	GND – 0.3	26	
V_I	Analog input	CMPIN	GND – 0.3	(V_S) + 0.3	V
		CMPREF	GND – 0.3	(V_S) + 0.3	
V_O	Analog output	OUT	GND – 0.3	(V_S) + 0.3	V
	Digital input	RESET	GND – 0.3	(V_S) + 0.3	V
	Digital output	$\overline{\text{ALERT}}$	GND – 0.3	6	V
T_J	Junction temperature			150	°C
T_{stg}	Storage temperature		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) V_{IN+} and $V_{IN–}$ are the voltages at the IN+ and IN– pins, respectively.
(3) Input voltage may exceed the voltage shown without causing damage to the device if the current at that terminal is limited to 5 mA.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±3000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{CM}	Common-mode input voltage	–0.2	12	26	V
V_S	Operating supply voltage	2.7	5	5.5	V
T_A	Operating free-air temperature	–40		125	°C

7.4 Thermal Information

THERMAL METRIC(1)		INA381		UNIT
		DGS (VSSOP)	DSG (WSON)	
		10 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	188.6	77	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	78.1	96.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	111.0	43.4	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	17.5	5.4	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	109.2	43.6	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	18.8	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

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7.5 Electrical Characteristics

at T_A = 25°C, V_{SENSE} = V_{IN+} – $V_{IN–}$ = 10 mV, V_S = 5 V, V_{IN+} = 12 V, and CMPREF = 2 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT						
CMRR	Common-mode rejection ratio, RTI(1)	V_{IN+} = 0 V to 26 V, T_A= –40ºC to +125ºC	84	100		dB
V_{OS}	Offset voltage, RTI(1)	V_{IN+} = 12 V, $V_{IN–}$ = 12 V		±100	±500	µV
		V_{IN+} = 0 V, $V_{IN–}$ = 0 V		±25	±150	
dV_{OS}/dT	Offset voltage drift, RTI(1)	T_A= –40ºC to +125ºC		0.1	1	µV/°C
PSRR	Power-supply rejection ratio	V_S = 2.7 V to 5.5 V, T_A= –40ºC to +125ºC		±8	±40	µV/V
I_B	Input bias current	V_{SENSE} = 0 mV, I_{B+}, $I_{B–}$		80		µA
I_{OS}	Input offset current	V_{SENSE} = 0 mV		±0.05		µA
OUTPUT						
G	Gain	INA381A1		20		V/V
		INA381A2		50		
		INA381A3		100		
		INA381A4		200		
E_G	Gain error	VOUT = 0.5 V to V_S – 0.5 V		±0.1%	±1%	
	Gain error drift	T_A= –40ºC to +125ºC		1.5	20	ppm/°C
	Nonlinearity error	V_{OUT}= 0.5 V to V_S – 0.5 V		±0.01%		
	Maximum capacitive load	No sustained oscillation		1		nF
VOLTAGE OUTPUT						
	Swing to V_S power-supply rail	R_L = 10 kΩ to GND, T_A= –40ºC to +125ºC		V_S – 0.02	V_S – 0.05	V
	Swing to GND(2)	R_L = 10 kΩ to GND, T_A= –40ºC to +125ºC		V_{GND} + 0.0005	V_{GND} + 0.005	V
FREQUENCY RESPONSE						
BW	Bandwidth	INA381A1		350		kHz
		INA381A2		210		
		INA381A3		150		
		INA381A4		105		
SR	Slew rate			2		V/µs
NOISE						
	Voltage noise density			40		nV/√Hz
COMPARATOR						
t_p	Propagation delay time, comparator only	CMPIN Input overdrive = 20 mV		0.4	1	µs
	Large-signal propagation delay, comparator only	CMPIN step = 0.5 V to 4.5, V_{CMPREF} = 4 V		0.4	2	
	Small-signal total alert propogation delay, comparator and amplifier	Input overdrive = 1 mV		2	5	
	Slew rate limited total alert propagation delay, comparator and amplifier	V_{OUT} = 0.5 V to 4.5, V_{CMPREF} = 4 V		3	10	
V_{OS}	Comparator offset voltage			±1	±5	mV
HYS	Hysteresis			50		mV
V_{IH}	High-level input voltage		1.4		6	V
V_{IL}	Low-level input voltage		0		0.4	V
V_{OL}	Alert low-level output voltage	I_{OL} = 3 mA		70	300	mV
	$\overline{ALERT}$ pin leakage input current	V_{OH} = 3.3 V		0.1	1	µA
	Digital leakage input current	0 ≤ V_{IN} ≤ V_S		1		µA
POWER SUPPLY						
I_Q	Quiescent current	V_{SENSE} = 10 mV, T_A = +25ºC		250	350	µA
		T_A = –40ºC to +125ºC			450	

(1) RTI = referred-to-input.
(2) Swing specifications are tested with an overdriven input condition.

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7.6 Typical Characteristics

at T_A = 25°C, V_S = 5 V, V_{IN+} = 12 V, and alert pullup resistor = 10 kΩ (unless otherwise noted)

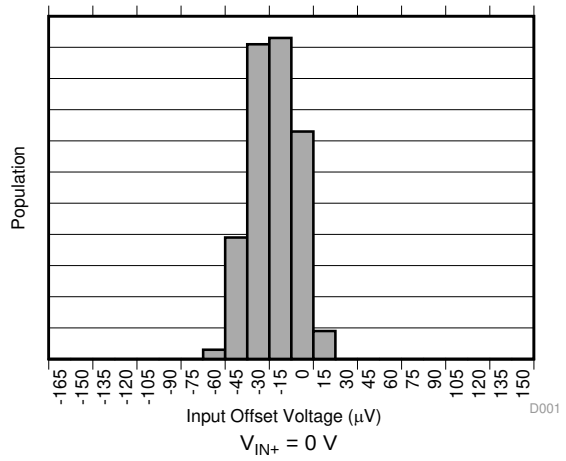


図 1. Input Offset Voltage Production Distribution (INA381A1)

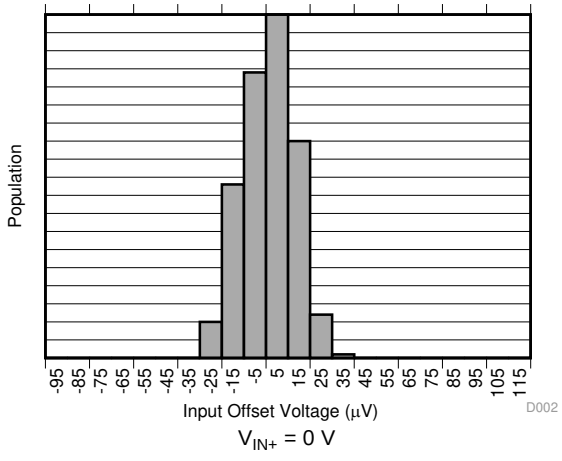


図 2. Input Offset Voltage Production Distribution (INA381A2)

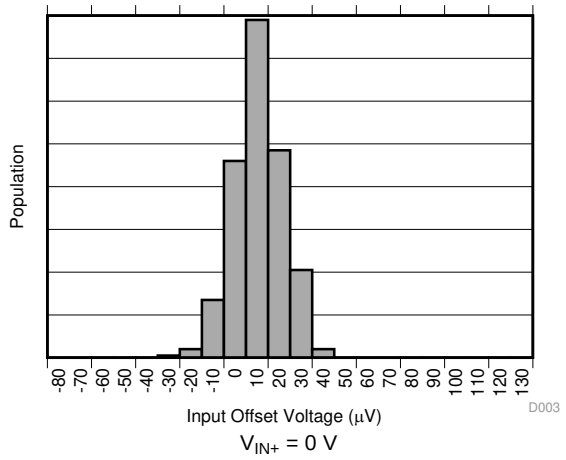


図 3. Input Offset Voltage Production Distribution (INA381A3)

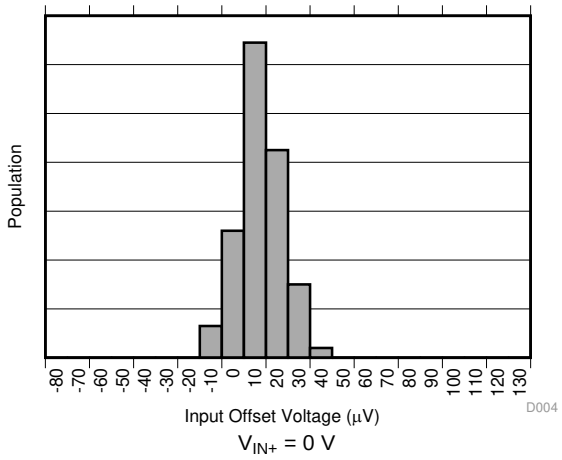


図 4. Input Offset Voltage Production Distribution (INA381A4)

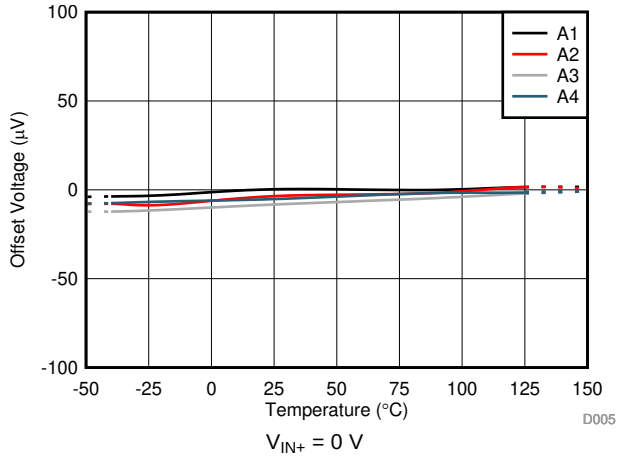


図 5. Offset Voltage vs Temperature

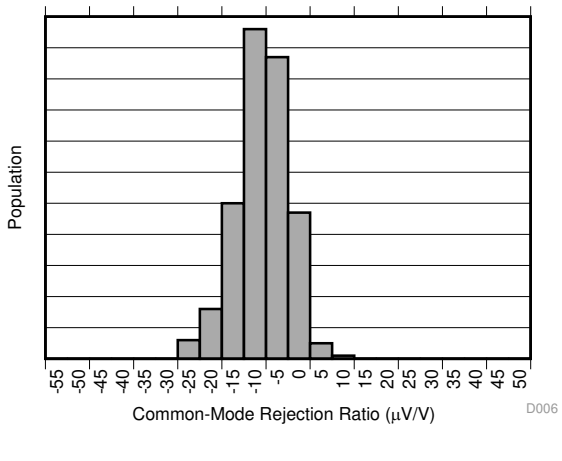


図 6. Common-Mode Rejection Production Distribution (INA381A1)

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Typical Characteristics (continued)

at T_A = 25°C, V_S = 5 V, V_{IN+} = 12 V, and alert pullup resistor = 10 kΩ (unless otherwise noted)

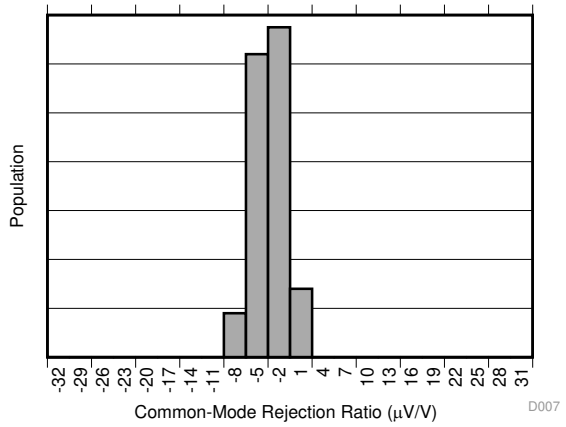


図 7. Common-Mode Rejection Production Distribution (INA381A2)

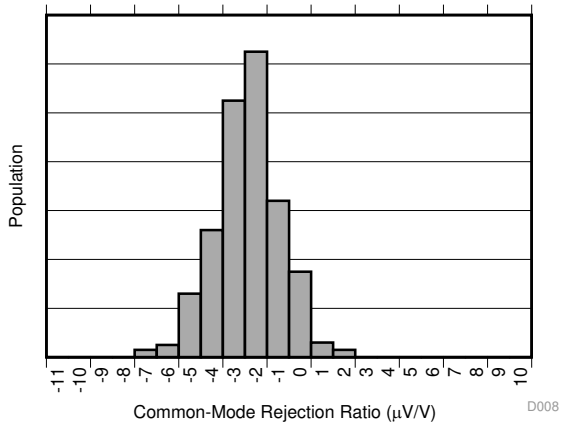


図 8. Common-Mode Rejection Production Distribution (INA381A3)

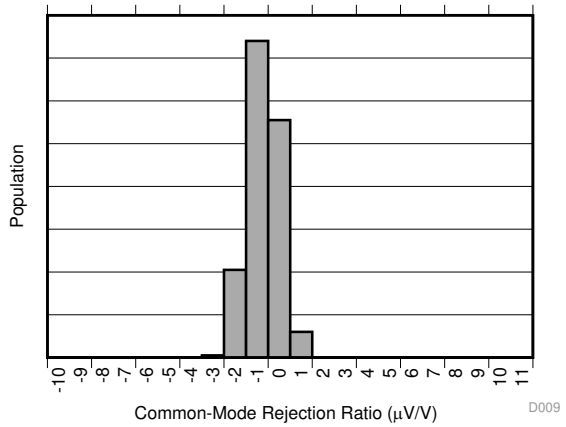


図 9. Common-Mode Rejection Production Distribution (INA381A4)

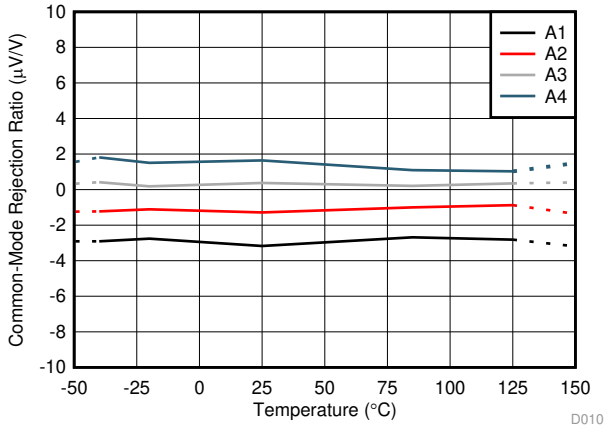


図 10. Common-Mode Rejection Ratio vs Temperature

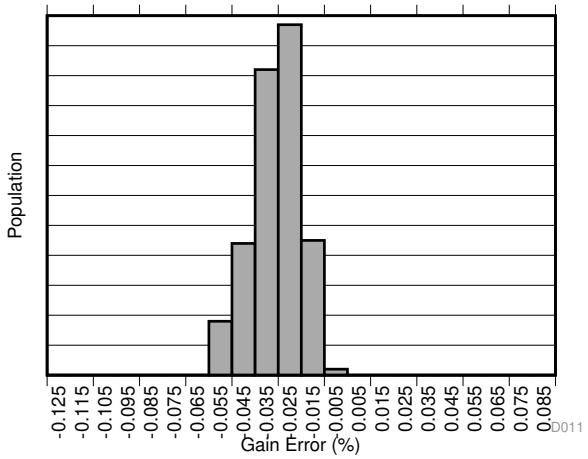


図 11. Gain Error Production Distribution (INA381A1)

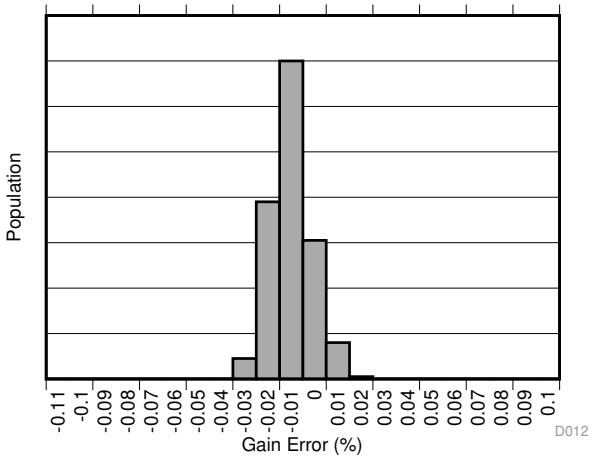


図 12. Gain Error Production Distribution (INA381A2)

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Typical Characteristics (continued)

at T_A = 25°C, V_S = 5 V, V_{IN+} = 12 V, and alert pullup resistor = 10 kΩ (unless otherwise noted)

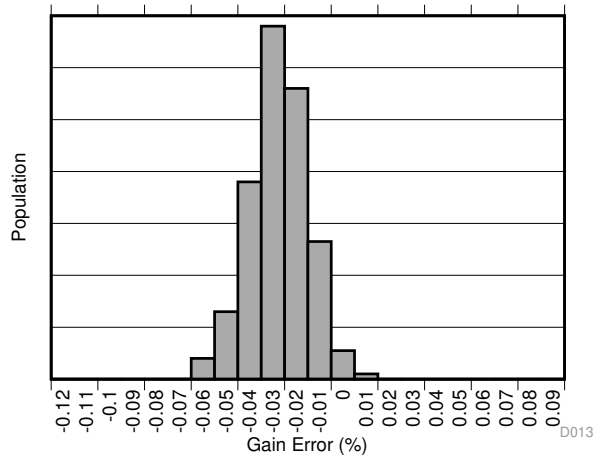


図 13. Gain Error Production Distribution (INA381A3)

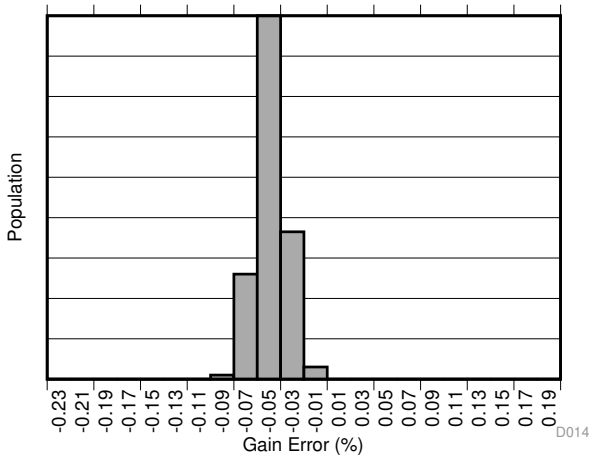


図 14. Gain Error Production Distribution (INA381A4)

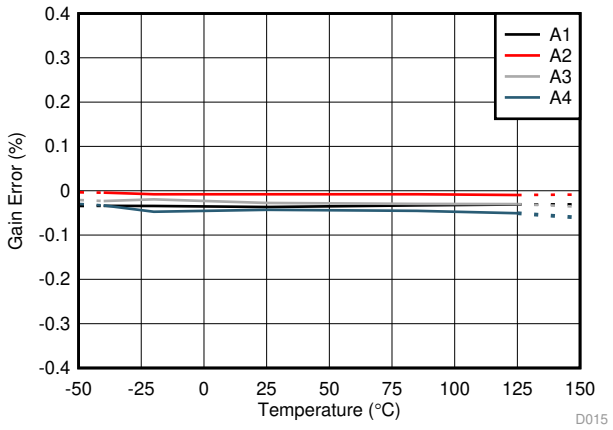


図 15. Gain Error vs Temperature

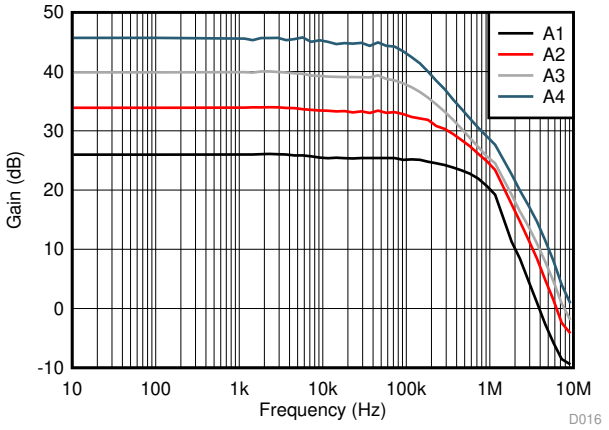


図 16. Gain vs Frequency

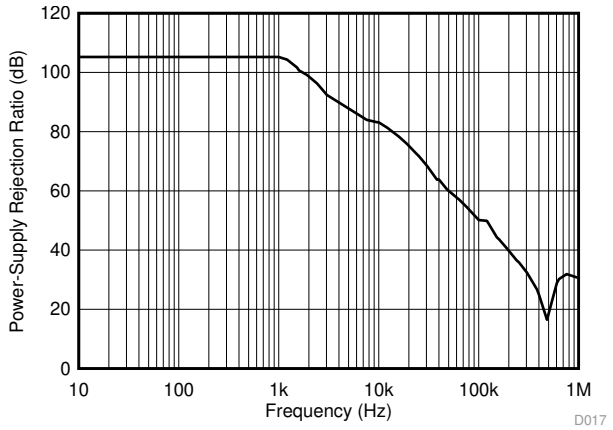


図 17. Power-Supply Rejection Ratio vs Frequency

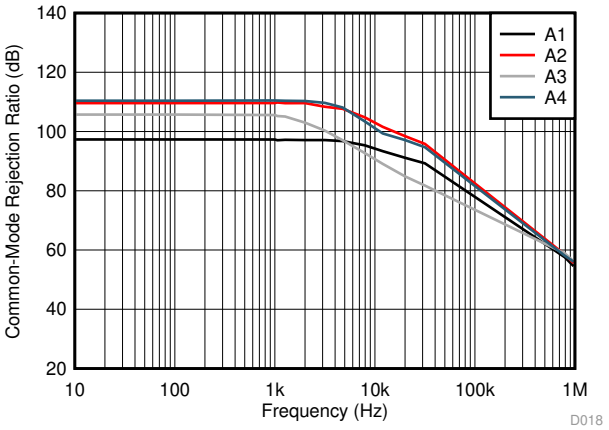


図 18. Common-Mode Rejection Ratio vs Frequency

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Typical Characteristics (continued)

at T_A = 25°C, V_S = 5 V, V_{IN+} = 12 V, and alert pullup resistor = 10 kΩ (unless otherwise noted)

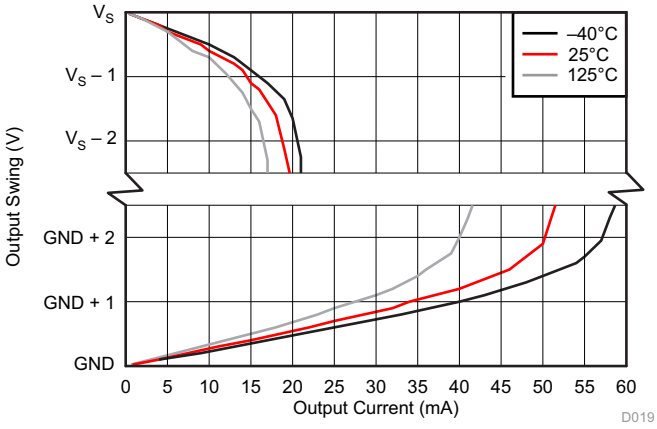


図 19. Output Voltage Swing vs Output Current

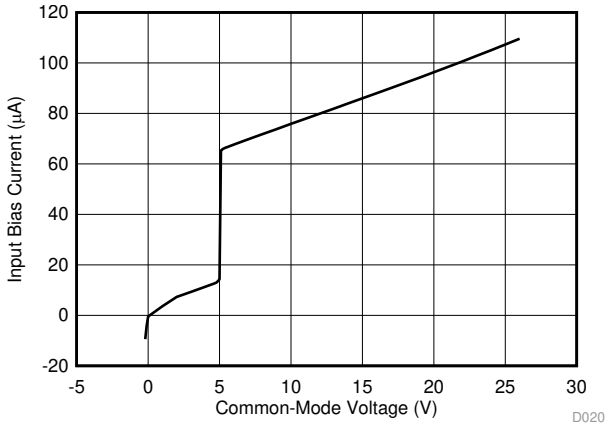


図 20. Input Bias Current vs Common-Mode Voltage

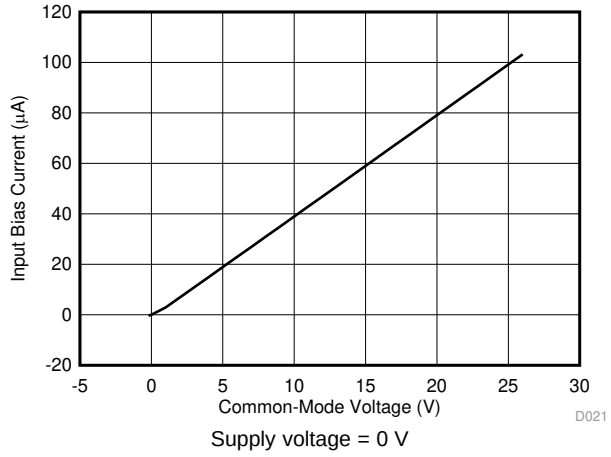


図 21. Input Bias Current vs Common-Mode Voltage (Both Inputs, Shutdown)

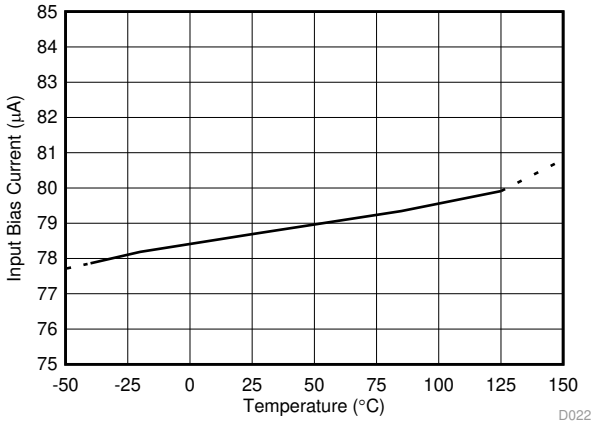


図 22. Input Bias Current vs Temperature

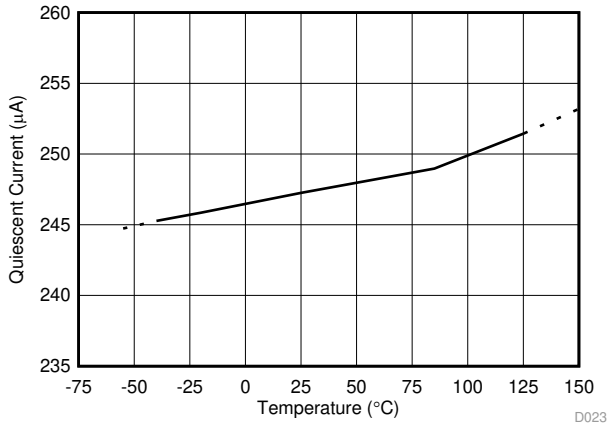


図 23. Quiescent Current vs Temperature

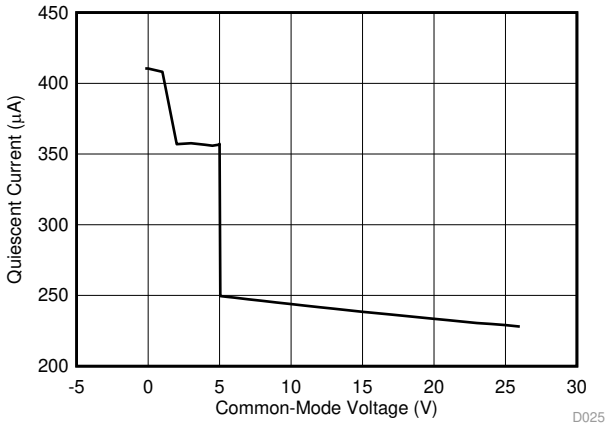


図 24. Quiescent Current vs Common-Mode Voltage

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Typical Characteristics (continued)

at T_A = 25°C, V_S = 5 V, V_{IN+} = 12 V, and alert pullup resistor = 10 kΩ (unless otherwise noted)

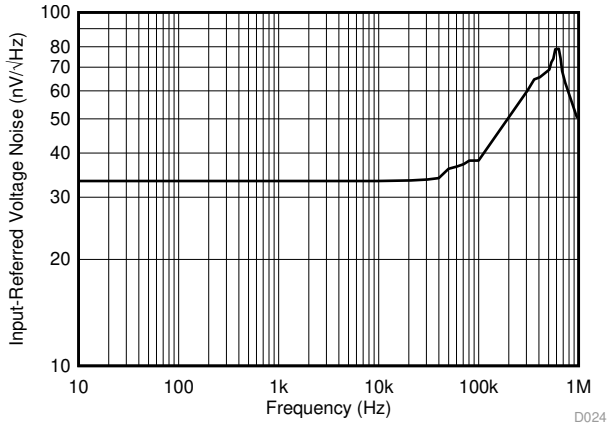


図 25. Input-Referred Voltage Noise vs Frequency (INA381A3 Devices)

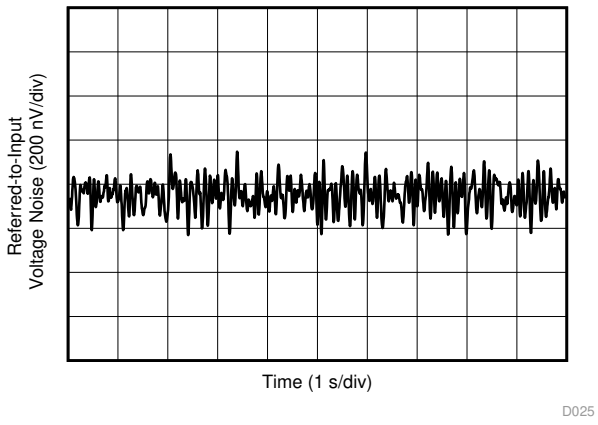
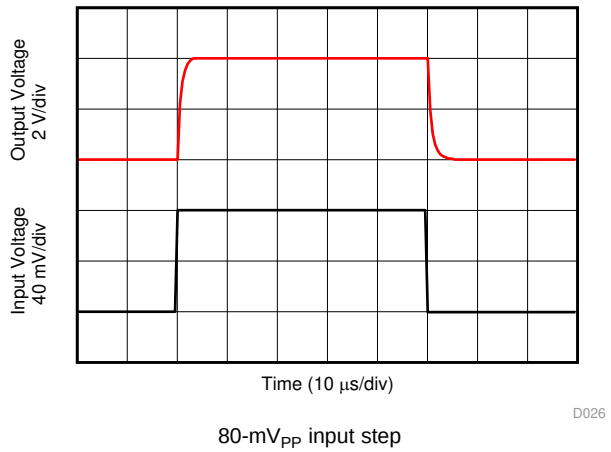


図 26. 0.1-Hz to 10-Hz Voltage Noise (Referred-to-Input)



80-mV_{PP} input step

図 27. Step Response

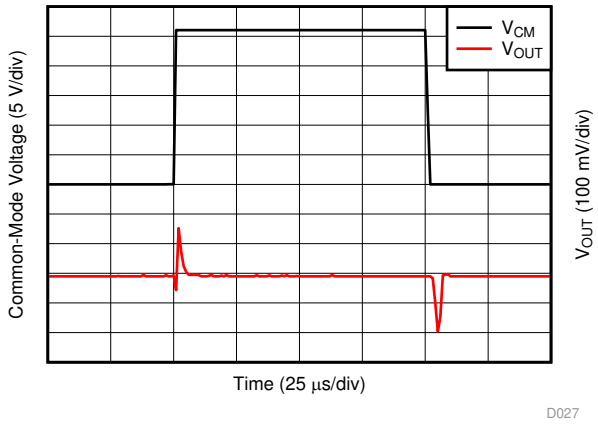


図 28. Common-Mode Voltage Transient Response

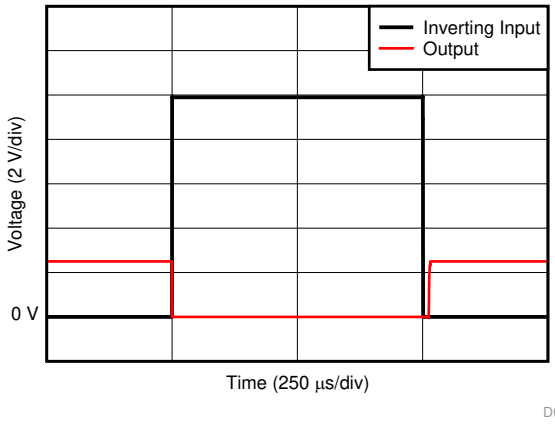


図 29. Inverting Differential Input Overload

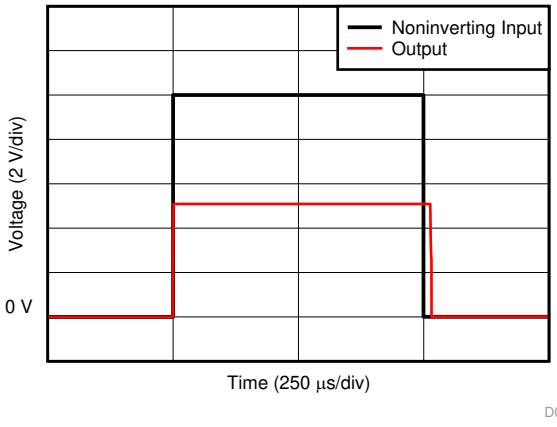


図 30. Noninverting Differential Input Overload

Typical Characteristics (continued)

at T_A = 25°C, V_S = 5 V, V_{IN+} = 12 V, and alert pullup resistor = 10 kΩ (unless otherwise noted)

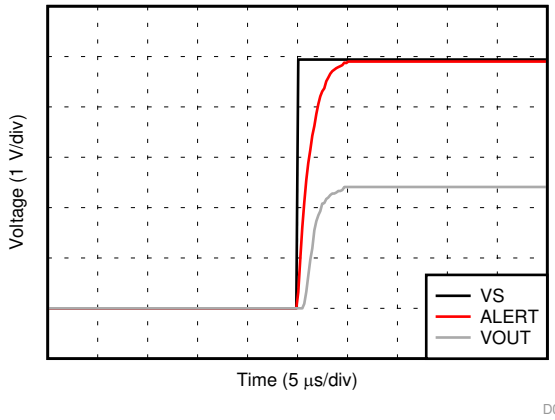


図 31. Start-Up Response

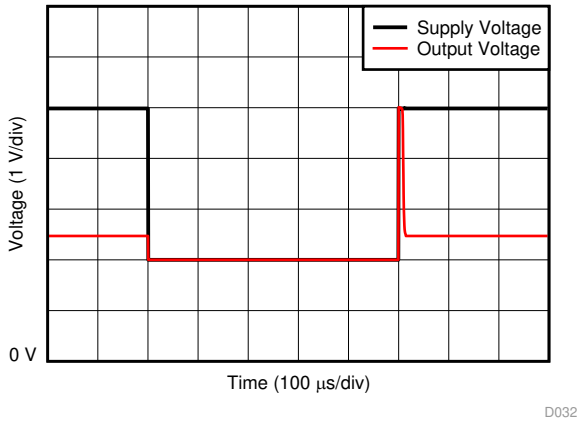


図 32. Brownout Recovery

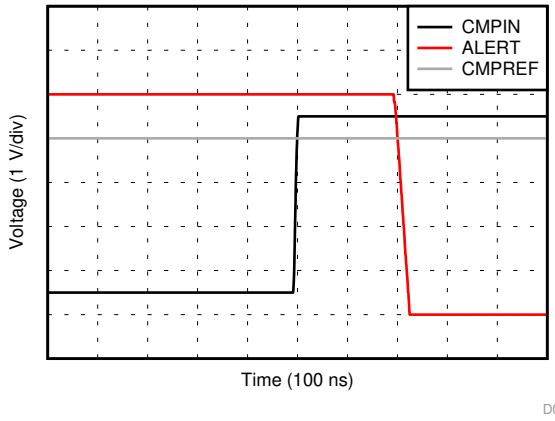


図 33. Comparator Propagation Delay

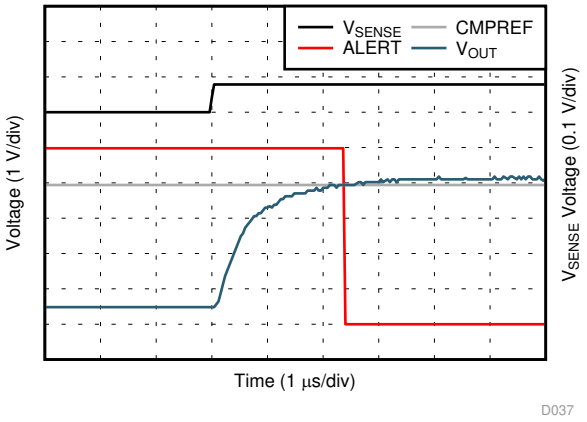


図 34. V_{SENSE} Voltage Response

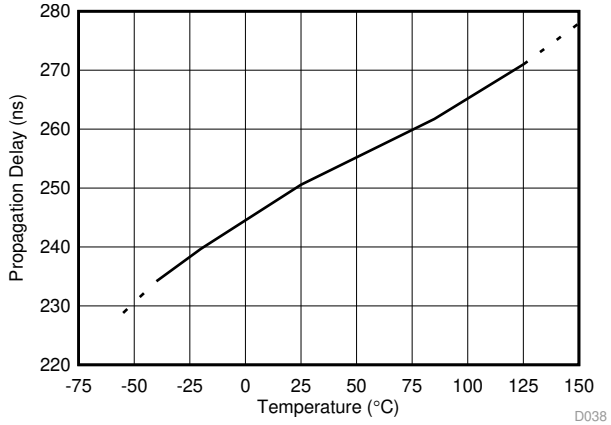


図 35. Comparator Propagation Delay vs Temperature

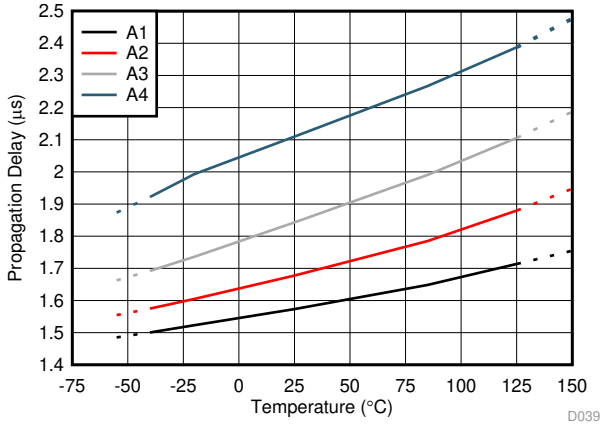


図 36. Total Propagation Delay vs Temperature

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Typical Characteristics (continued)

at T_A = 25°C, V_S = 5 V, V_{IN+} = 12 V, and alert pullup resistor = 10 kΩ (unless otherwise noted)

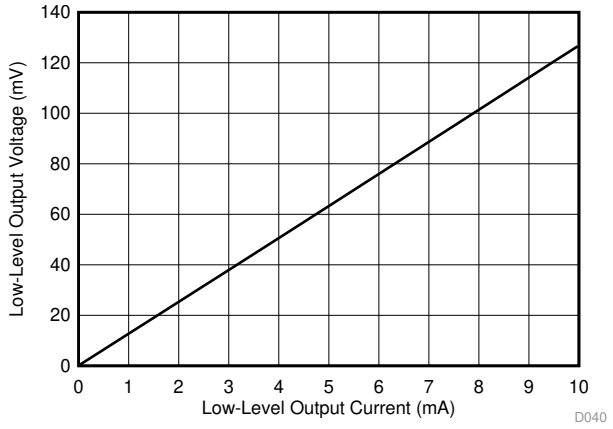


図 37. Low-Level Output Voltage vs Low-Level Output Current

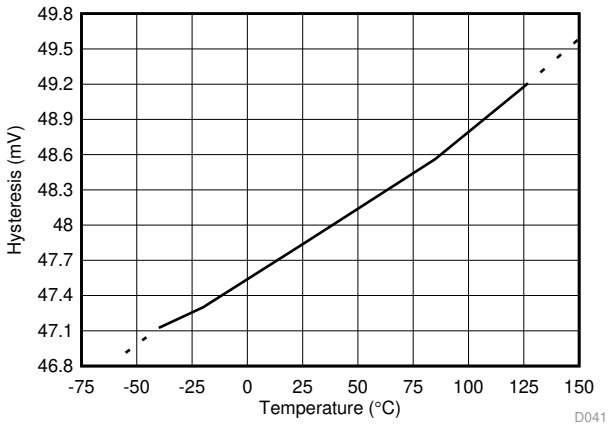


図 38. Hysteresis vs Temperature

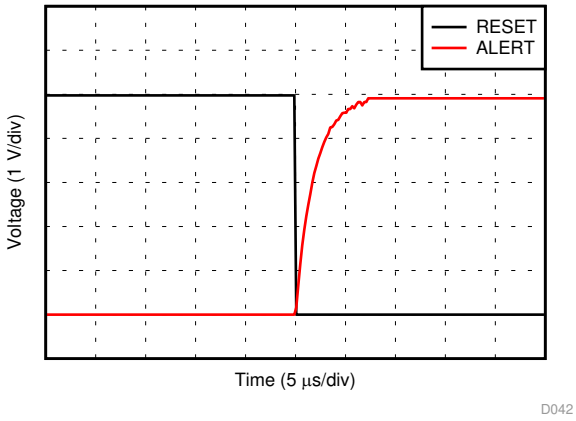


図 39. Reset and Alert Voltage Response

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8 Detailed Description

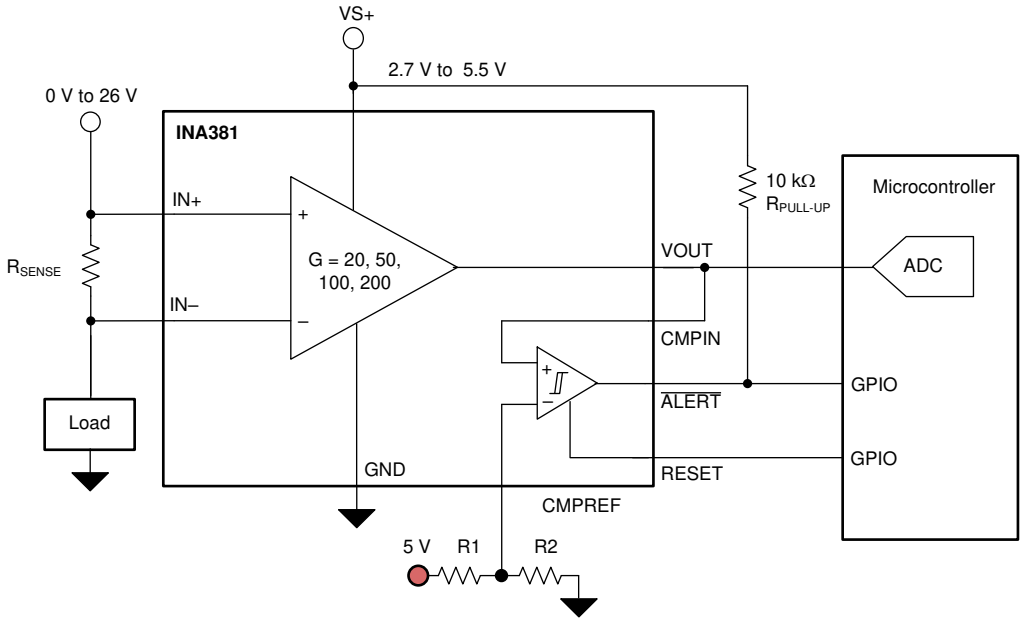
8.1 Overview

The INA381 is a zero-drift topology, current-sensing amplifier with an integrated comparator that can be used in both low-side and high-side current-sensing and protection applications. This specially designed, current-sensing amplifier accurately measures voltages developed across current-sensing resistors (also known as *current-shunt resistors*) on common-mode voltages that far exceed the supply voltage powering the device. Current can be measured on input voltage rails as high as 26 V, and the device can be powered from supply voltages as low as 2.7 V. The device can also withstand the full 26-V common-mode voltage at the input pins when the supply voltage is removed without causing damage.

The zero-drift topology enables high-precision measurements with maximum input offset voltages as low as 150 µV, and a temperature contribution of only 1 µV/°C over the full temperature range of –40°C to +125°C. The low total offset voltage of the INA381 enables the use of smaller current-sense resistor values, and allows for more efficient system operation without sacrificing measurement accuracy due to the smaller input signal.

The device uses a reference input that simplifies setting the corresponding current threshold level to use for out-of-range comparison. Combining the precision measurement of the current-sense amplifier and the onboard comparator enables an all-in-one overcurrent detection device. This combination creates a highly-accurate design that quickly detects out-of-range conditions, and allows the system to take corrective actions to prevent potential component or system-wide damage.

8.2 Functional Block Diagram



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8.3 Feature Description

8.3.1 Wide Input Common-Mode Voltage Range

The INA381 supports input common-mode voltages from –0.2 V to +26 V. As a result of the internal topology, the common-mode range is not restricted by the power-supply voltage (V_S) as long as V_S stays within the operational range of 2.7 V to 5.5 V. As 図 40 shows, the ability to operate with common-mode voltages greater or less than V_S allows the INA381 to be used in high-side, as well as low-side, current-sensing applications.

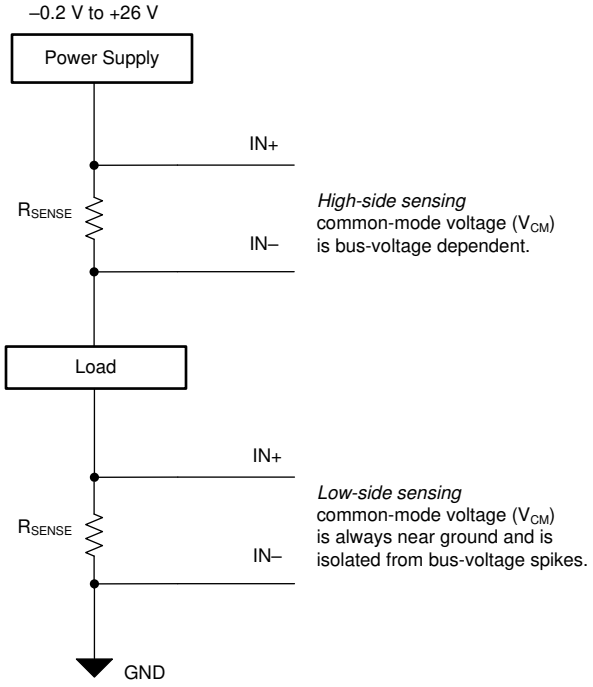


図 40. High-Side and Low-Side Current Sensing

8.3.2 Precise Low-Side Current Sensing

When used in low-side current-sensing applications, the offset voltage of the INA381 is less than 150 µV. The low offset performance of the device has several benefits. First, the low offset allows the device to be used in applications that must measure current over a wide dynamic range. In this case, the low offset voltage improves accuracy when the sense currents are on the low end of the measurement range. Another advantage of low offset voltage is the ability to sense lower voltage drops across the sense resistor accurately, thus allowing for a lower-value shunt resistor. Lower-value shunt resistors reduce power loss in the current-sense circuit, and help improve the power efficiency of the end application.

The gain error of the INA381 is specified to be within 1% of the actual value. As the sensed voltage becomes much larger than the offset voltage, this gain error becomes the dominant source of error in the current-sense measurement.

8.3.3 High Bandwidth and Slew Rate

The INA381 supports small-signal bandwidths as high as 350 kHz, and large-signal slew rates of 2 V/µs. The ability to detect rapid changes in the sensed current, as well as the ability to quickly slew the output, makes the INA381 a good choice for applications that require a quick response to input current changes. One application that requires high bandwidth and slew rate is low-side motor control, where the ability to follow rapid changing current in the motor allows for more accurate control over a wider operating range. Another application that requires higher bandwidth and slew rates is system fault detection. The integrated comparator within the INA381 is designed to quickly detect when the sense current is out-of-range, and provide a digital output on the $\overline{\text{ALERT}}$ pin for quicker and faster responses.

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Feature Description (continued)

8.3.4 Alert Output

The $\overline{\text{ALERT}}$ pin is an active-low, open-drain output pulls low when the input conditions are out-of-range. This open-drain output pin is recommended to include a 10-kΩ pullup resistor to the supply voltage. This open-drain pin can be pulled up to a voltage beyond the supply voltage, V_S, but must not exceed 5.5 V.

図 41 shows the alert output response of the internal comparator. When the output voltage of the amplifier is less than the reference voltage set on CMPREF, the comparator output is in the default high state. When the amplifier output voltage exceeds the reference voltage set at the CMPREF pin, the comparator output becomes active and pulls low. This active low output indicates that the measured signal at the amplifier input has exceeded the programmed threshold level, indicating an overcurrent or out-of-range condition has occurred. See the Alert Modes section for more information about how to set the alert output behavior.

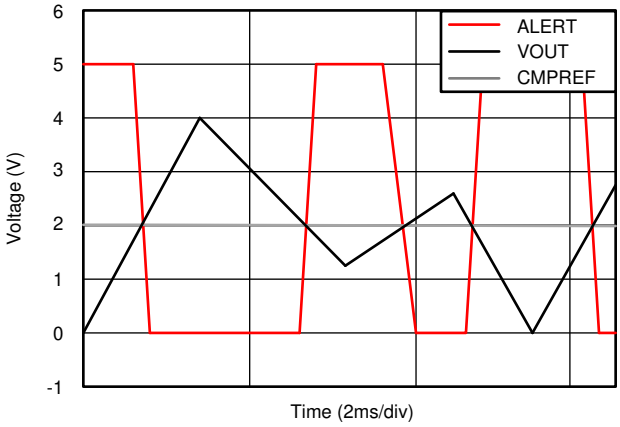


図 41. Overcurrent Alert Response

8.3.5 Adjustable Overcurrent Threshold

The VOUT voltage is the amplified voltage developed across the current-sensing resistor. The signal developed at the VOUT pin is the input voltage across the IN+ and IN– pins multiplied by the gain of the amplifier. The INA381 has four gain options, as shown in 図 42: 20 V/V, 50 V/V, 100 V/V, and 200 V/V. If additional hysteresis is not required, directly connect the VOUT pin to the CMPIN pin.

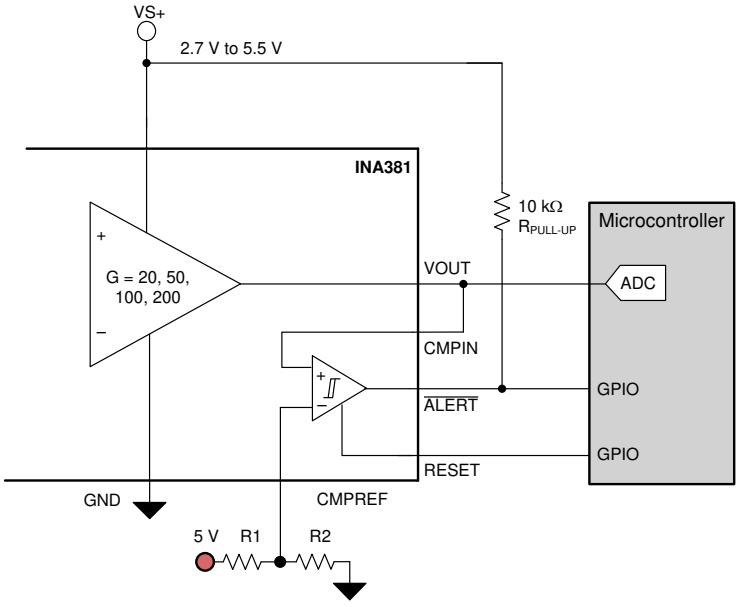


図 42. Resistor Divider Voltage

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Feature Description (continued)

The device determines if an overcurrent event is present by comparing the voltage on the CMPIN pin to the corresponding signal developed at the CMPREF pin. The threshold voltage for the CMPREF pin can be set with a resistive divider, or by connecting an external voltage source (such as a reference generator device). 図 43 depicts the REF3140 used as an external reference source.

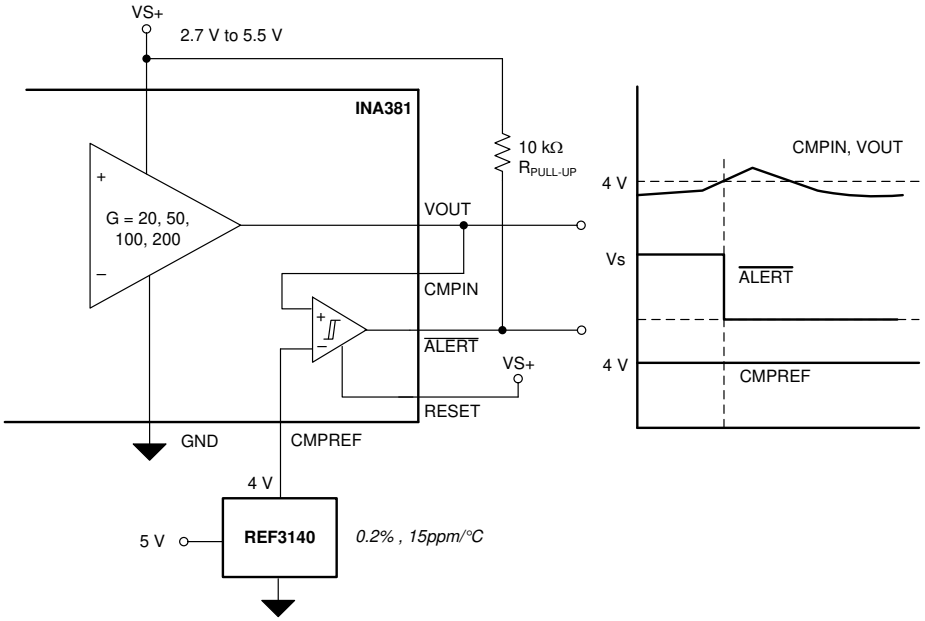


図 43. External Reference Voltage

8.3.6 Comparator Hysteresis

The onboard comparator in the INA381 is designed to reduce the possibility of oscillations in the alert output when the measured signal level is near the overlimit threshold level as a result of noise. When the voltage (V_{CMPIN}) exceeds the voltage developed at the CMPREF pin, the $\overline{ALERT}$ pin asserts and pulls low. The output voltage must drop to less than the CMPREF pin threshold voltage, as shown in 図 44, by the hysteresis level of 50 mV so that the $\overline{ALERT}$ pin deasserts and returns to the nominal high state. The INA381 is designed with a hysteresis of 50 mV.

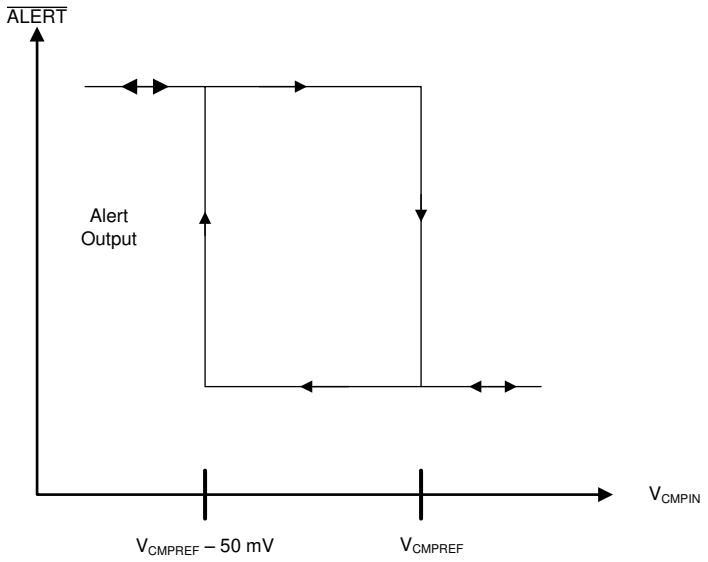


図 44. Typical Comparator Hysteresis

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8.4 Device Functional Modes

8.4.1 Alert Modes

The device has two output operating modes, transparent and latched, that are selected based on the RESET pin setting. These modes change how the ALERT pin responds after an alert when the overcurrent condition is removed.

8.4.1.1 Transparent Output Mode

The device is set to transparent mode when the RESET pin is pulled low, allowing the output alert state to change and follow the input signal with respect to the programmed alert threshold. For example, when the differential input signal exceeds the alert threshold, the alert output pin is pulled low. When the differential input signal drops to less than the alert threshold, the output returns to the default high-output state. A common implementation using the device in transparent mode is to connect the ALERT pin to a hardware interrupt input on a microcontroller. When an overcurrent condition is detected and the ALERT pin is pulled low, the controller interrupt pin detects the output state change and begins making changes to the system operation required to address the overcurrent condition. Under this configuration, the ALERT pin high-to-low transition is captured by the microcontroller, and the output returns to the default high state when the overcurrent event is removed.

8.4.1.2 Latch Output Mode

Some applications cannot continuously monitor the state of the output ALERT pin to detect an overcurrent condition, as described in the *Transparent Output Mode* section. A typical example of this type of application is a system that only periodically polls the ALERT pin state to determine if the system is functioning correctly. If the device is set to transparent mode in this type of application, the state change of the ALERT pin can be missed when ALERT is pulled low if the out-of-range condition does not appear during one of these periodic polling events. Latch output mode is specifically intended to accommodate these applications.

As shown in 表 1, the device is placed into the corresponding output mode based on the signal connected to RESET. The difference between latch mode and transparent mode is how the alert output responds when an overcurrent event ends. In transparent mode (RESET = low), when the differential input signal drops below the limit threshold level after the ALERT pin asserts because of an overcurrent event, the state of the ALERT pin returns to the default high setting to indicate that the overcurrent event is complete.

表 1. Output Mode Settings

OUTPUT MODE	RESET PIN SETTING
Transparent	RESET = low
Latch	RESET = high

In latch mode (RESET = high), when an overlimit condition is detected and the ALERT pin is pulled low, the ALERT pin does not return to the default high state when the differential input signal drops to less than the alert threshold level. To clear the alert, the RESET pin must be pulled low for at least 100 ns. If the differential input signal is less than the alert threshold, pull the RESET pin low to return ALERT to the default high level. If the input signal exceeds the threshold limit when the RESET pin is pulled low, the ALERT pin remains low. When the alert condition is detected by the system controller, set the RESET pin back to high to place the device back in latch mode.

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図 45 shows the latch and transparent modes. In 図 45, when V_{IN} drops to less than the V_{LIMIT} threshold for the first time, the RESET pin pulls high. With the RESET pin pulled high, the device is set to latch mode so that the alert output state does not return high when the input signal drops to less than the V_{LIMIT} threshold. Only when the RESET pin is pulled low does the $\overline{\text{ALERT}}$ pin return to the default high level, thus indicating that the input signal is below the limit threshold. When the input signal drops to less than the limit threshold for the second time, the RESET pin is already pulled low. The device is set to transparent mode at this point, and the $\overline{\text{ALERT}}$ pin is pulled back high when the input signal drops below the alert threshold.

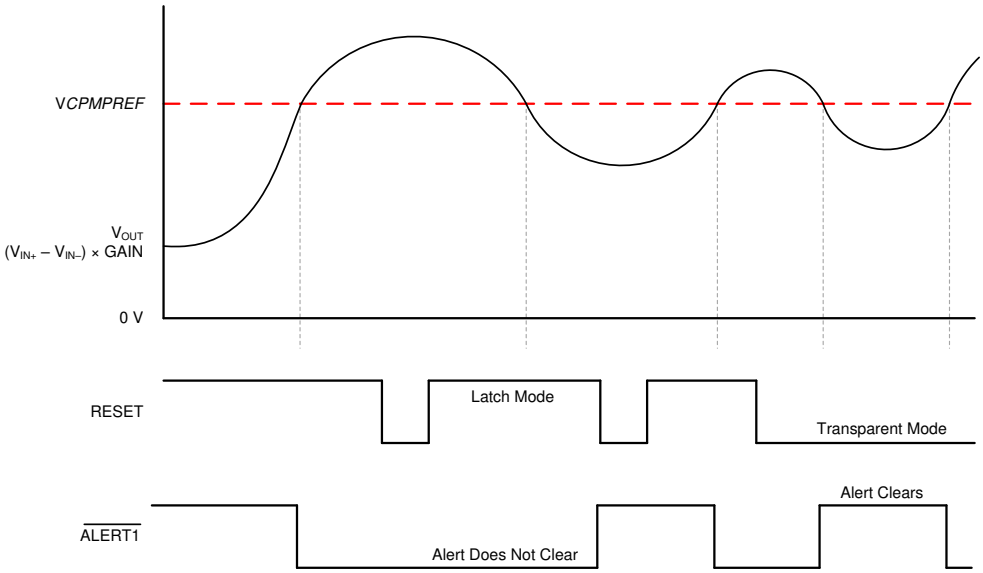


図 45. Transparent Mode Versus Latch Mode

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9 Applications and Implementation

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Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The INA381 is designed to enable easy configuration for detecting overcurrent conditions in an application. This device is individually targeted towards unidirectional overcurrent detection of a single threshold. However, this device can also be paired with additional devices and circuitry to create more complex monitoring functional blocks.

9.1.1 Select a Current-Sensing Resistor

The device measures the differential voltage developed across a resistor when current flows through the component to determine if the current being monitored exceeds a defined limit. This resistor is commonly referred to as a *current-sensing resistor* or a *current-shunt resistor*, with each term commonly used interchangeably. The flexible design of the device allows for measuring a wide differential input signal range across this current-sensing resistor.

Selecting the value of this current-sensing resistor is based primarily on two factors: the required accuracy of the current measurement and the allowable power dissipation across the current-sensing resistor. Larger voltages developed across this resistor allow for more accurate measurements to be made. Amplifiers have fixed internal errors that are largely dominated by the inherent input offset voltage. When the input signal decreases, these fixed internal amplifier errors become a larger portion of the measurement and increase the uncertainty in the measurement accuracy. When the input signal increases, the measurement uncertainty is reduced because the fixed errors are a smaller percentage of the signal being measured. Therefore, the use of larger-value, current-sensing resistors inherently improves measurement accuracy.

However, a system design trade-off must be evaluated through use of larger input signals for improving the measurement accuracy. Increasing the current-sense resistor value results in increased power dissipation across the current-sensing resistor. Increasing the value of the current-shunt resistor increases the differential voltage developed across the resistor when current passes through the component. This increase in voltage across the resistor increases the power that the resistor must be able to dissipate. Decreasing the value of the current-shunt resistor value reduces the power dissipation requirements of the resistor, but increases the measurement errors resulting from the decreased input signal. Selecting the optimal value for the shunt resistor requires factoring both the accuracy requirement for the specific application and the allowable power dissipation of this component.

An increasing number of very low ohmic-value resistors are becoming more widely available with values reaching down as low as 1 mΩ or lower with power dissipations of up to 5 W that enable large currents to be accurately monitored with sensing resistors.

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Application Information (continued)

9.1.1.1 Select a Current-Sensing Resistor: Example

In this example, the trade-offs involved in selecting a current-sensing resistor are discussed. This example requires 5% accuracy for detecting a 10-A overcurrent event under 20 µs where only 250 mW is allowable for the dissipation across the current-sensing resistor at the full-scale current level. Although the maximum power dissipation is defined as 250 mW, a lower dissipation is preferred to improve system efficiency. Given the total error budget of 5%, the INA381 total error is less than 1%. The INA381 is well suited for this application because up to 1% of error is available to be attributed to the measurement error of the device under these conditions.

As shown in 表 2, the maximum value calculated for the current-sensing resistor with these requirements is 2.5 mΩ. Although this value satisfies the maximum power dissipation requirement of 250 mW, headroom is available from the 2.5% maximum total overcurrent detection error to reduce the value of the current-sensing resistor and reduce the power dissipation further. Selecting a 1.5-mΩ, current-sensing resistor value offers a good tradeoff for reducing the power dissipation in this scenario by approximately 40% and still remaining within the accuracy region.

表 2. Calculating the Current-Sensing Resistor (R_{SENSE})

PARAMETER		EQUATION	VALUE	UNIT
I_{MAX}	Maximum current		10	A
P_{D_MAX}	Maximum allowable power dissipation		250	mW
R_{SENSE_MAX}	Maximum allowable R_{SENSE}	P_{D_MAX} / I_{MAX}^2	2.5	mΩ
V_{OS}	Offset voltage, V_{CM} = 12 V		500	µV
V_{OS_ERROR}	Initial offset voltage error	$(V_{OS} / (R_{SENSE_MAX} \times I_{MAX}) \times 100$	2%	
E_G	Gain error		1%	
$ERROR_{TOTAL}$	Total measurement error	$\sqrt{(V_{OS_ERROR}^2 + E_G^2)}$	2.23%	
	Allowable current threshold accuracy		5%	
t_p	Total system overcurrent response time		10	µs
	Allowable overcurrent response		20	µs

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9.1.2 Increase Comparator Hysteresis

The onboard comparator of the device is designed with a hysteresis of 50 mV. The INA381 is designed for the user to change the hysteresis from a preset value of 50 mV by connecting an external resistor between VOUT and CMPIN. 図 46 shows a detailed block diagram of adding additional hysteresis.

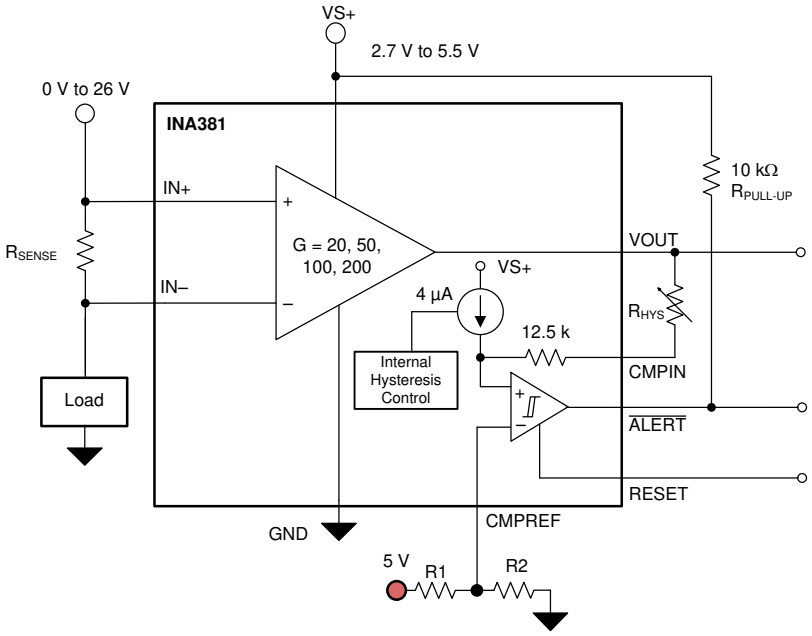


図 46. Increase Hysteresis to the Comparator

The default hysteresis is 50 mV. Internal to the comparator, the INA381 has a current source of 4 µA in series with 12.5 kΩ. The internal current source and hysteresis of the comparator is set by the internal hysteresis control circuit that is enabled only after ALERT is asserted low. ALERT is asserted low during an overcurrent condition when the voltage on VOUT exceeds the threshold set on the CMPREF pin. The internal 4-µA hysteresis circuits are triggered only after ALERT is asserted low.

To increase hysteresis to greater than the default 50 mV, the R_{HYS} resistor must be connected between the VOUT and CMPIN pins. 式 1 describes the internal configuration to set the external hysteresis resistor.

$$R_{HYS} = \frac{V_{HYS} - (4\ \mu A \times 12500\ \Omega)}{4\ \mu A} \quad (1)$$

where

- V_{HYS} is the desired hysteresis voltage
- R_{HYS} is the external resistor on the input of the CMPIN pin

表 3 lists the external resistors required at the input of the CMPIN pin to set the hysteresis.

表 3. Hysteresis Resistor Selection

HYSTERESIS VOLTAGE	EXTERNAL RESISTOR AT THE CMPIN PIN
50 mV	0 Ω
75 mV	6.25 kΩ
100 mV	12.5 kΩ
125 mV	18.75 kΩ
150 mV	25 kΩ
200 mV	37.5 kΩ
250 mV	50 kΩ
300 mV	62.5 kΩ

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9.1.3 Operation With Common-Mode Transients Greater Than 26 V

With a small amount of additional circuitry, the INA381 can be used in circuits subject to transients greater than 26 V. Use only Zener diodes or Zener-type transient absorbers (sometimes referred to as *transorbs*)—any other type of transient absorber has an unacceptable time delay. Start by adding a pair of resistors as shown in 図 47 as a working impedance for the Zener diode. Keep these resistors as small as possible; most often approximately 10 Ω. Larger values can be used with an effect on gain that is discussed in the *Input Filtering* section. This circuit limits only short-term transients and, therefore, many applications are satisfied with a 10-Ω resistor along with conventional Zener diodes of the lowest acceptable power rating. This combination uses the least amount of board space. These diodes can be found in packages as small as SOT-523 or SOD-523.

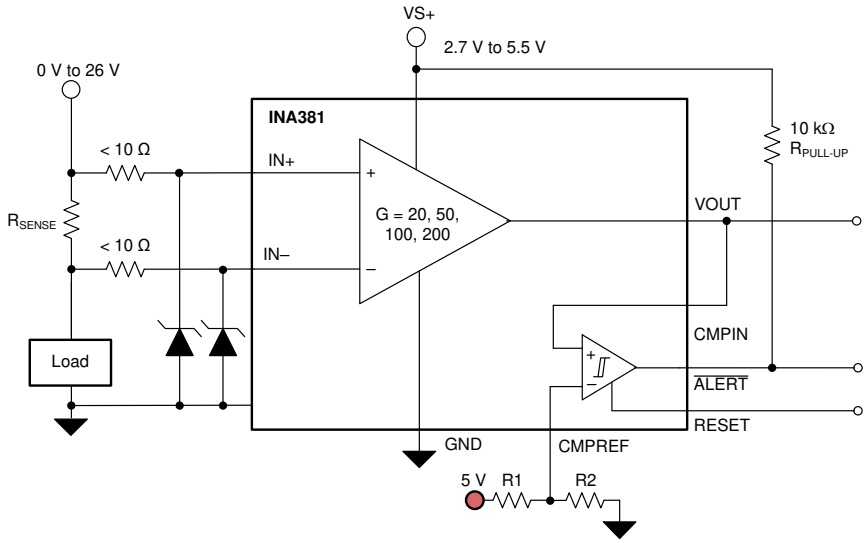


図 47. Transient Protection

In the event that low-power Zener diodes do not have sufficient transient absorption capability, use a higher-power transorb. 図 47 shows that the most package-efficient solution involves using a single transorb and back-to-back diodes between the device inputs. The most space-efficient solutions are dual, series-connected diodes in a single SOT-523 or SOD-523 package. In either of the examples provided in 図 47 and 図 48, the total board area required by the INA381 with all protective components is less than that of an SOIC-8 package, and only slightly greater than that of a VSSOP-8 package.

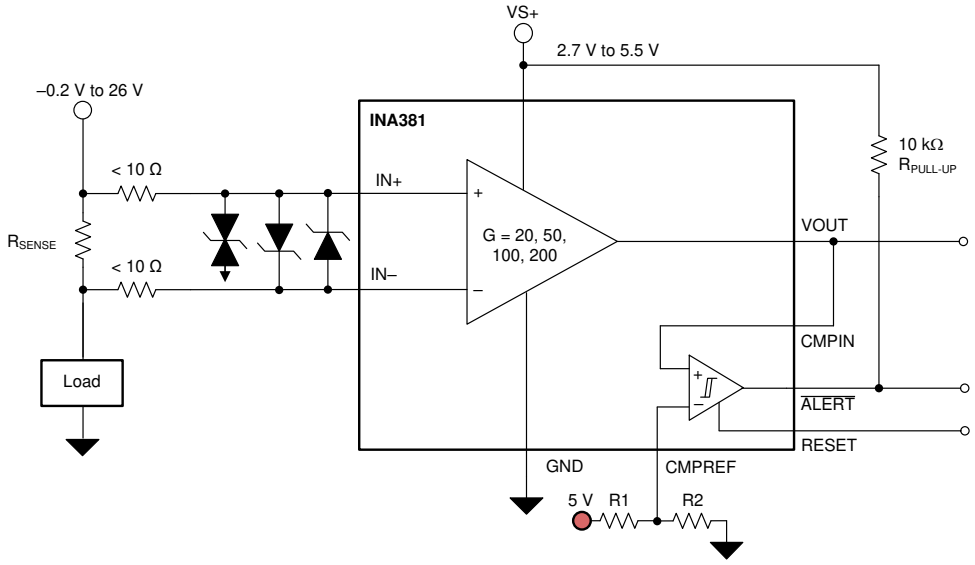


図 48. Transient Protection Using a Single Transorb and Input Clamps

9.1.4 Input Filtering

If the INA381 output is connected to a high-impedance input, the device output is the best location to filter, using a simple RC network from VOUT to GND. Filtering at the output attenuates high-frequency disturbances in the common-mode voltage, differential input signal, and INA381 power-supply voltage. If filtering at the output is not possible, or if only the differential input signal needs filtering, a filter can be applied at the input pins of the device.

External filtering helps reduce the amount of noise that reaches the comparator, and thereby reduces the likelihood of a false alert. The tradeoff to adding this noise filter is that the alert response time is increased because both the input signal and noise are filtered. 図 49 shows the implementation of an input filter for the device.

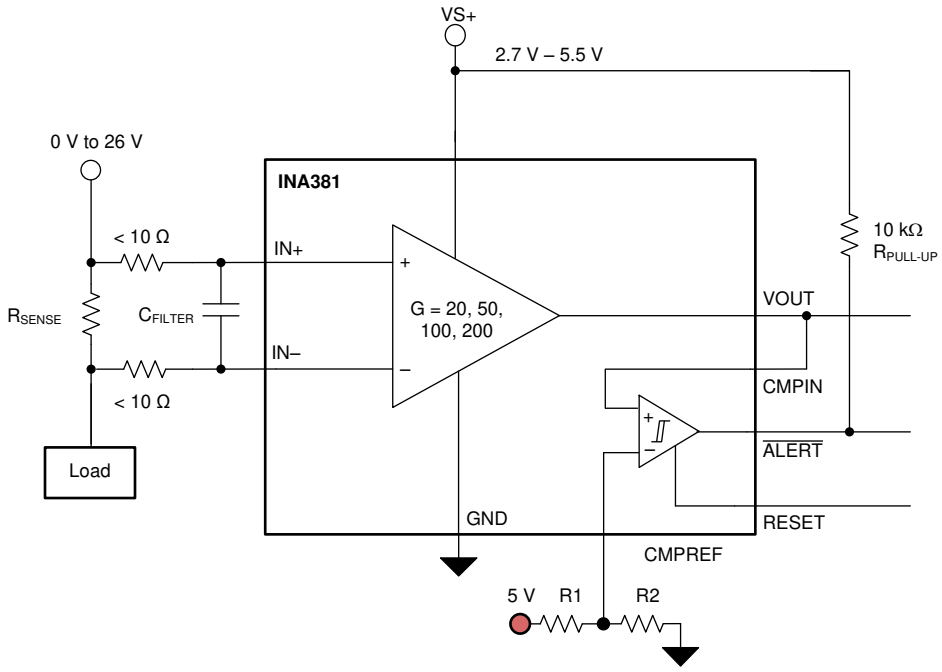


図 49. Input Filter

The addition of external series resistance creates an additional error in the measurement; therefore, the value of these series resistors must be kept to 10 Ω (or less, if possible) to reduce impact to accuracy. As shown in 図 49, the internal bias network present at the input pins creates a mismatch in input bias currents when a differential voltage is applied between the input pins. If additional external series filter resistors are added to the circuit, the mismatch in bias currents results in a mismatch of voltage drops across the filter resistors. This mismatch creates a differential error voltage that subtracts from the voltage developed across the shunt resistor. This error results in a voltage at the device input pins that is different than the voltage developed across the shunt resistor. Without the additional series resistance, the mismatch in input bias currents has negligible effect on device operation. 式 2 is used to calculate the gain error factor that is used with 式 3 to calculate the percentage gain error when using external filter resistors.

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式 2 shows that the amount of variance in the differential voltage present at the device input relative to the voltage developed at the shunt resistor is based both on the external series resistance (R_F) value as well as internal input resistor R_{INT}. The reduction of the shunt voltage reaching the device input pins appears as a gain error when comparing the output voltage relative to the voltage across the shunt resistor. Use 式 2 to calculate the expected deviation from the shunt voltage to what is measured at the device input pins:

$$\text{Gain Error Factor} = \frac{1250 \times R_{INT}}{(1250 \times R_F) + (1250 \times R_{INT}) + (R_F \times R_{INT})} \quad (2)$$

where:

- R_{INT} is the internal input resistor
- R_F is the external series resistance

The adjustment factor from 式 2 including the device internal input resistance shown in 表 4 varies with each gain version. 表 5 lists each individual device gain error factor.

表 4. Input Resistance

PRODUCT	GAIN	R_{INT} (kΩ)
INA381A1	20	25
INA381A2	50	10
INA381A3	100	5
INA381A4	200	2.5

表 5. Device Gain Error Factor

PRODUCT	SIMPLIFIED GAIN ERROR FACTOR
INA381A1	$\frac{25000}{(21 \times R_F) + 25000}$
INA381A2	$\frac{10000}{(9 \times R_F) + 10000}$
INA381A3	$\frac{1000}{R_F + 1000}$
INA381A4	$\frac{2500}{(3 \times R_F) + 2500}$

Use 式 3 to then calculate the gain error that can be expected from the addition of the external series resistors:

$$\text{Gain Error (\%)} = 100 - (100 \times \text{Gain Error Factor}) \quad (3)$$

For example, using an INA381A2 and the corresponding gain error equation from 表 5, a series resistance of 10 Ω results in a gain error factor of 0.991. The corresponding gain error is then calculated using 式 3, resulting in an additional gain error of approximately 0.89% solely because of the external 10-Ω series resistors.

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9.2 Typical Applications

9.2.1 Bidirectional Window Comparator

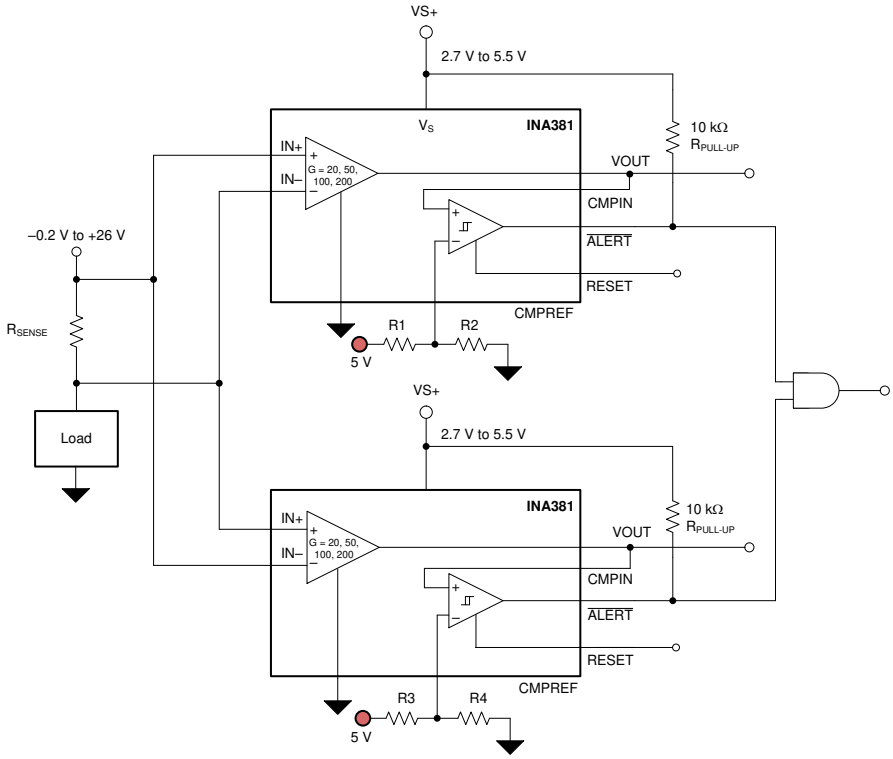


図 50. Bidirectional Window Comparator

9.2.1.1 Design Requirements

表 6 lists the parameters for a design example of a high-side INA381 measuring in the forward direction, and one low-side INA381 measuring in the reverse direction. This example designs for maximum accuracy and also uses the alert function of both devices.

表 6. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
R_{SENSE}	12 mΩ
Power-supply voltage	5 V
Common-mode voltage	20 V
Maximum sense current	20 A
Small-signal bandwidth	> 120 kHz
Alert current threshold	19 A

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9.2.1.2 Detailed Design Procedure

Although the device is only able to measure current through a current-sensing resistor flowing in one direction, a second INA381 can be used to create a bidirectional monitor. With the input pins of a second device reversed across the same current-sensing resistor, the second device is now able to detect current flowing in the other direction relative to the first device; see 図 50. The outputs of each device connect to an AND gate to detect if either of the limit threshold levels are exceeded. As shown in 表 7, the output of the AND gate is high if neither overcurrent limit thresholds are exceeded. A low output state of the AND gate indicates that the positive overcurrent limit or the negative overcurrent limit has been exceeded.

表 7. Bidirectional Overcurrent Output Status

OCP STATUS	OUTPUT
OCP+	0
OCP–	0
No OCP	1

In this scenario, the maximum current expected through the shunt resistor is 20 A in either the forward or reverse direction. Maximum accuracy is desired; therefore, the shunt resistor is maximized by taking the maximum output swing divided by the smallest gain and divided by the maximum current. The design parameters used in 表 6 yield a shunt value of 12.3 mΩ. The closest standard 1% and 0.1% device is 12 mΩ, and this value is used by both INA381 devices.

Because corrective action must be taken when the current exceeds ±19 A, the comparators require a value of 4.56 V (19 A × 0.012 Ω × 20 V/V). In this instance, a voltage divider consisting of two 4.53-kΩ resistors (R1 and R3) and two 5-kΩ resistors (R2 and R4) off the 5-V rail supply a voltage close to this value. To be certain that both device alert functions can trigger a single GPIO pin on a microcontroller, both comparator outputs feed into an AND gate.

9.2.1.3 Application Curve

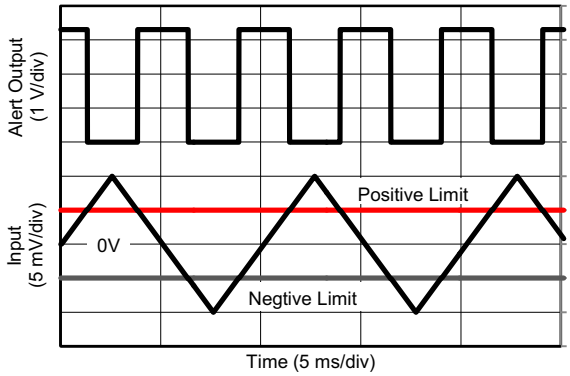


図 51. Bidirectional Operation

9.2.2 Solenoid Low-Side Current Sensing

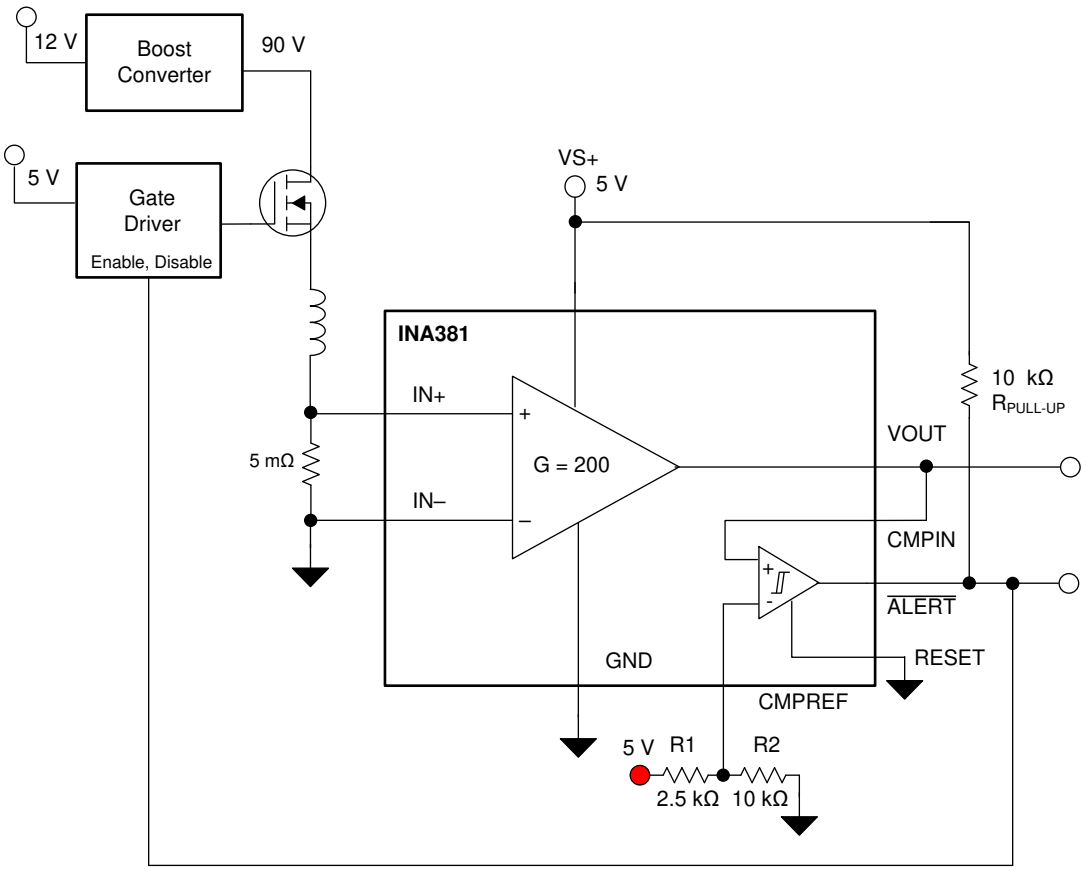


図 52. Solenoid Low-Side Current-Sensing

9.2.2.1 Design Requirements

表 8 lists the parameters of an application design using the INA381 and $\overline{\text{ALERT}}$ functionality to create a low-side current-sense amplifier with less than a 20-µs system shutdown.

表 8. Design Parameters

DESIGN PARAMETERS	EXAMPLE VALUE
Power-supply voltage	5 V
Low-side current sensing	V_{CM} = 0 V
Mode of operation	Unidirectional
Maximum current sense threshold	4.0 A
$\overline{\text{ALERT}}$ response time	< 20 µs
$\overline{\text{ALERT}}$ pin mode	Transparent
R_{SENSE} resistor	5 mΩ
Gain option	200 V/V

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9.2.2.2 Detailed Design Procedure

The INA381 can measure current across a shunt resistor with common-mode voltage ranges from –0.3 V to +26 V. The INA381 is capable of measuring low-side current sensing allowing enough margin below ground to accurately measure current through the load. One common application for low-side current sensing is a solenoid control application. As described in 図 52, a typical high-voltage solenoid application consists of a high-voltage NMOS transistor, a low-ohmic shunt resistor connected to the source of the NMOS transistor, and a solenoid. A solenoid is often used for applications that control a relay that triggers an on-off state. As current flows through the solenoid, the current flowing through the copper windings generate a magnetic field around the iron that can be used to open or close a relay. Industrial valves, electromechanical relays, and PLC control relays are often built of solenoids, and the driver circuitry for solenoids are designed discretely, as shown in 図 52.

A microcontroller unit is often used to control the duty cycle of the NMOS switch to control the position of the solenoid. By controlling the duty cycle of the solenoid driver, the current flowing through the solenoid can be controlled, which in turn can be used to perform position control. However, for applications that need two states, on and off, a microcontroller can be expensive and overkill. If a solenoid is located remotely in specific application, the routing of the current-sense amplifier signal back to the microcontroller can create additional overhead and often increase the cost of the application. The INA381 has a built-in comparator that can be programmed to assert an $\overline{\text{ALERT}}$ when the CMPIN signal exceeds the CMPREF threshold signal. The $\overline{\text{ALERT}}$ signal can be used to feed the $\overline{\text{ALERT}}$ signal back to the gate driver circuitry of the NMOS, which can disable the NMOS switch to turn the circuit off to protect from damage. Effective impedance of a solenoid is an inductor in series with a resistance. If the solenoid is prone to damage, the inductor can lose inductance and behave as a shorted resistor. If not protected, high current can flow through the solenoid and damage the system, causing permanent failure. The INA381, with an $\overline{\text{ALERT}}$ pin that responds in as fast as 10 µs, can be directly connected to the NMOS driver to remove power from the solenoid in the event of an overcurrent condition. When the load current decreases to less than the safe operating limit, the $\overline{\text{ALERT}}$ clears and enables safe operation of the solenoid. This design example can be used as a guideline to implement the INA381 for a solenoid application.

Based on 式 4, the design example for the CMPREF voltage is 4 V. The threshold voltage is set using simple resistor dividers R1 and R2. R1 is set with 2.5 kΩ, and R2 is set with 10 kΩ. This 4-V threshold is set at the CMPREF pin. When the current exceeds 4 A, voltage on VOUT exceeds 4 V, and the $\overline{\text{ALERT}}$ pin asserts a low signal indicating a fault detection. The device is configured in transparent mode by connecting the RESET pin to ground. Because of this configuration, when the current signal falls below 4 A of current, the $\overline{\text{ALERT}}$ pin is pulled high and resets the fault detection, maintaining safe operation of the solenoid. This example explains a methodology where a solenoid can be self-protected and triggered based on a set, safe-operating, current threshold.

In this application, 4 A and higher are considered overcurrent conditions and some corrective action must be taken to prevent the current from destroying the system. The INA381 offers corrective action through an $\overline{\text{ALERT}}$ pin that can be tailored for a specific overcurrent condition through the CMPREF pin. To set the proper CMPREF value, a gain option and an R_{SENSE} value must first be determined. This design example uses a gain of 200 V/V and an R_{SENSE} value of 5 mΩ. CMPREF is calculated according to 式 4 in this particular case. This value is calculated to be approximately 4 V. This value can be achieved through either a voltage divider or LDO. In this particular instance, the voltage divider was chosen.

$$\text{CMPREF (V)} = [\text{Alert Threshold (A)} \times \text{Shunt Resistor } (\Omega) + V_{OS} \text{ (V)}] \times \text{Gain} \quad (4)$$

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9.2.2.3 Application Curve

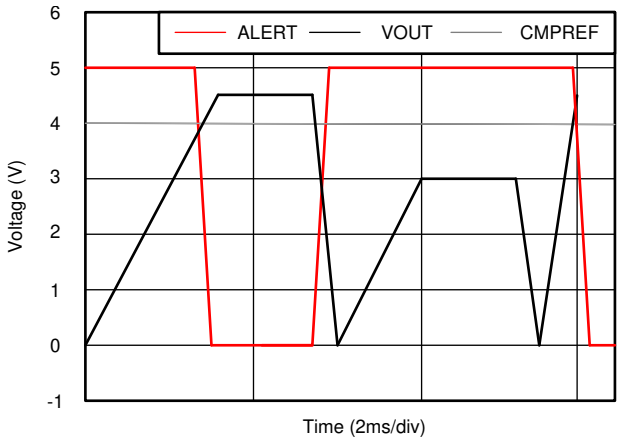


図 53. Low-Side Sensing Application Curve

10 Power Supply Recommendations

The device input circuitry accurately measures signals on common-mode voltages beyond the power-supply voltage, V_S. For example, the voltage applied to the VS+ power-supply pin can be 5 V, whereas the load power-supply voltage being monitored (V_{CM}) can be as high as 26 V. The device can withstand the full –0.2-V to +26-V range at the input pins, regardless of whether the device has power applied or not.

Power-supply bypass capacitors are required for stability and must be placed as closely as possible to the supply and ground pins of the device. A typical value for this supply bypass capacitor is 0.1 µF. Applications with noisy or high-impedance power supplies can require additional decoupling capacitors to reject power-supply noise.

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11 Layout

11.1 Layout Guidelines

- Place the power-supply bypass capacitor as closely as possible to the supply and ground pins. The recommended value of this bypass capacitor is 0.1 µF. Add decoupling capacitance to compensate for noisy or high-impedance power supplies.
- Make sure that the thermal pad and GND are connected to a solid ground plane of the PCB.
- Pull up the open-drain output pin to the supply voltage rail through a 10-kΩ pullup resistor.

11.2 Layout Example

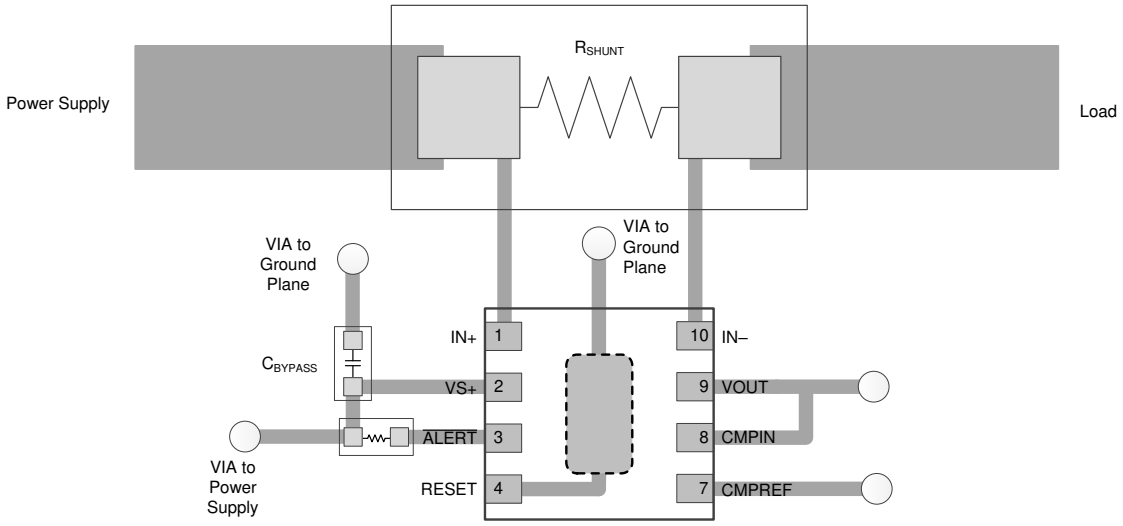


図 54. Recommended Layout for DSG Package

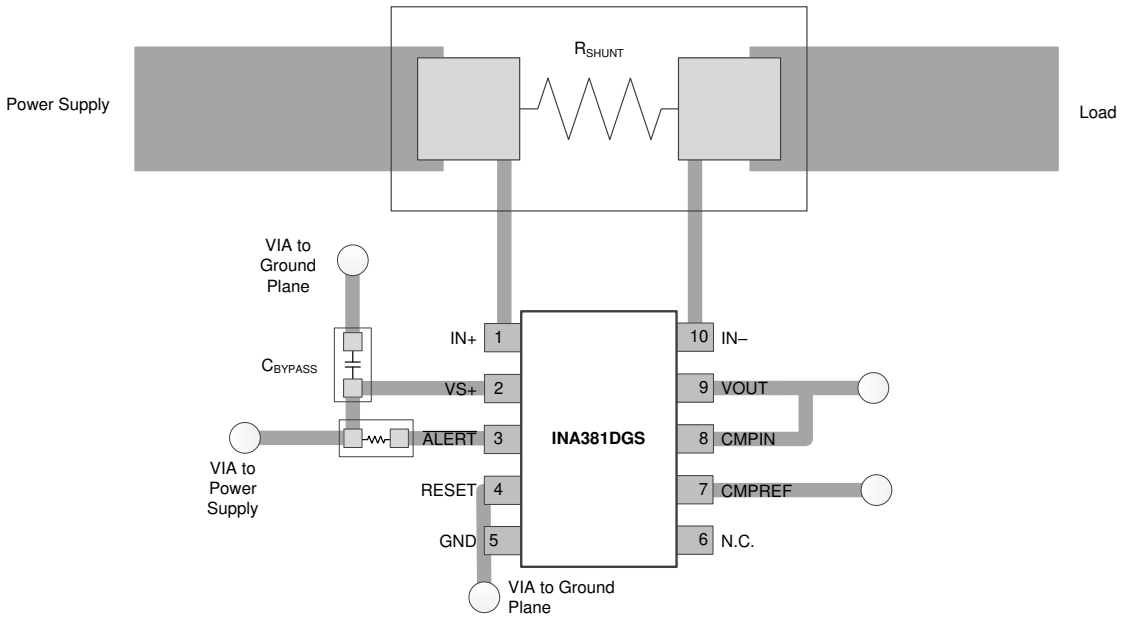


図 55. Recommended Layout for DGS Package

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12 デバイスおよびドキュメントのサポート

12.1 ドキュメントのサポート

12.1.1 関連資料

関連資料については、以下を参照してください。

- テキサス・インスツルメンツ、『REF31xx 15ppm/°C Maximum, 100-µA, SOT-23 Series Voltage Reference』データシート (英語)
- テキサス・インスツルメンツ、『INA381EVM』ユーザー・ガイド (英語)

12.2 ドキュメントの更新通知を受け取る方法

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12.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。この情報は、そのデバイスについて利用可能な最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
INA381A1IDGSR	Active	Production	VSSOP (DGS) | 10	2500 | LARGE T&R	Yes	NIPDAU | SN | NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	1XM6
INA381A1IDGSR.B	Active	Production	VSSOP (DGS) | 10	2500 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	1XM6
INA381A1IDGST	Obsolete	Production	VSSOP (DGS) | 10	-	-	Call TI	Call TI	-40 to 125	1XM6
INA381A1IDSGR	Active	Production	WSON (DSG) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1HWY
INA381A1IDSGR.B	Active	Production	WSON (DSG) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1HWY
INA381A1IDSGT	Obsolete	Production	WSON (DSG) | 8	-	-	Call TI	Call TI	-40 to 125	1HWY
INA381A2IDGSR	Active	Production	VSSOP (DGS) | 10	2500 | LARGE T&R	Yes	NIPDAU | SN | NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	1XN6
INA381A2IDGSR.B	Active	Production	VSSOP (DGS) | 10	2500 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	1XN6
INA381A2IDGST	Obsolete	Production	VSSOP (DGS) | 10	-	-	Call TI	Call TI	-40 to 125	1XN6
INA381A2IDSGR	Active	Production	WSON (DSG) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1HXY
INA381A2IDSGR.B	Active	Production	WSON (DSG) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1HXY
INA381A2IDSGRG4	Active	Production	WSON (DSG) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1HXY
INA381A2IDSGRG4.B	Active	Production	WSON (DSG) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1HXY
INA381A2IDSGT	Obsolete	Production	WSON (DSG) | 8	-	-	Call TI	Call TI	-40 to 125	1HXY
INA381A3IDGSR	Active	Production	VSSOP (DGS) | 10	2500 | LARGE T&R	Yes	NIPDAU | SN | NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	1XO6
INA381A3IDGSR.B	Active	Production	VSSOP (DGS) | 10	2500 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	1XO6
INA381A3IDGST	Obsolete	Production	VSSOP (DGS) | 10	-	-	Call TI	Call TI	-40 to 125	1XO6
INA381A3IDSGR	Active	Production	WSON (DSG) | 8	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	1HZY
INA381A3IDSGR.B	Active	Production	WSON (DSG) | 8	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	1HZY
INA381A3IDSGRG4	Active	Production	WSON (DSG) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1HZY
INA381A3IDSGRG4.B	Active	Production	WSON (DSG) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1HZY
INA381A3IDSGT	Obsolete	Production	WSON (DSG) | 8	-	-	Call TI	Call TI	-40 to 125	1HZY
INA381A4IDGSR	Active	Production	VSSOP (DGS) | 10	2500 | LARGE T&R	Yes	NIPDAU | SN | NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	1XP6
INA381A4IDGSR.B	Active	Production	VSSOP (DGS) | 10	2500 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	1XP6
INA381A4IDGST	Obsolete	Production	VSSOP (DGS) | 10	-	-	Call TI	Call TI	-40 to 125	1XP6
INA381A4IDSGR	Active	Production	WSON (DSG) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1I1Y

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
INA381A4IDSGR.B	Active	Production	WSON (DSG) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1I1Y
INA381A4IDSGRG4	Active	Production	WSON (DSG) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1I1Y
INA381A4IDSGRG4.B	Active	Production	WSON (DSG) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1I1Y
INA381A4IDSGT	Obsolete	Production	WSON (DSG) | 8	-	-	Call TI	Call TI	-40 to 125	1I1Y

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF INA381 :

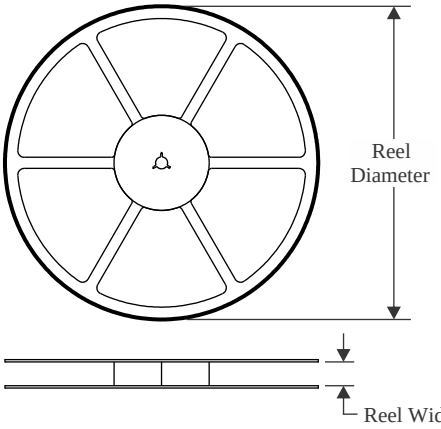
- Automotive : INA381-Q1

NOTE: Qualified Version Definitions:

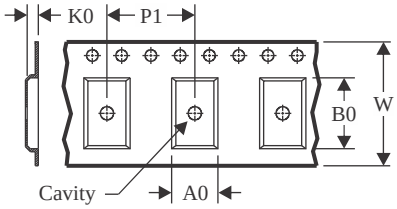
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

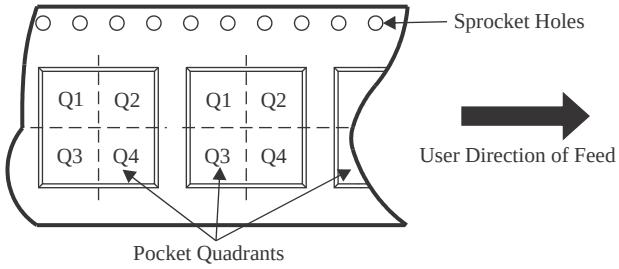


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

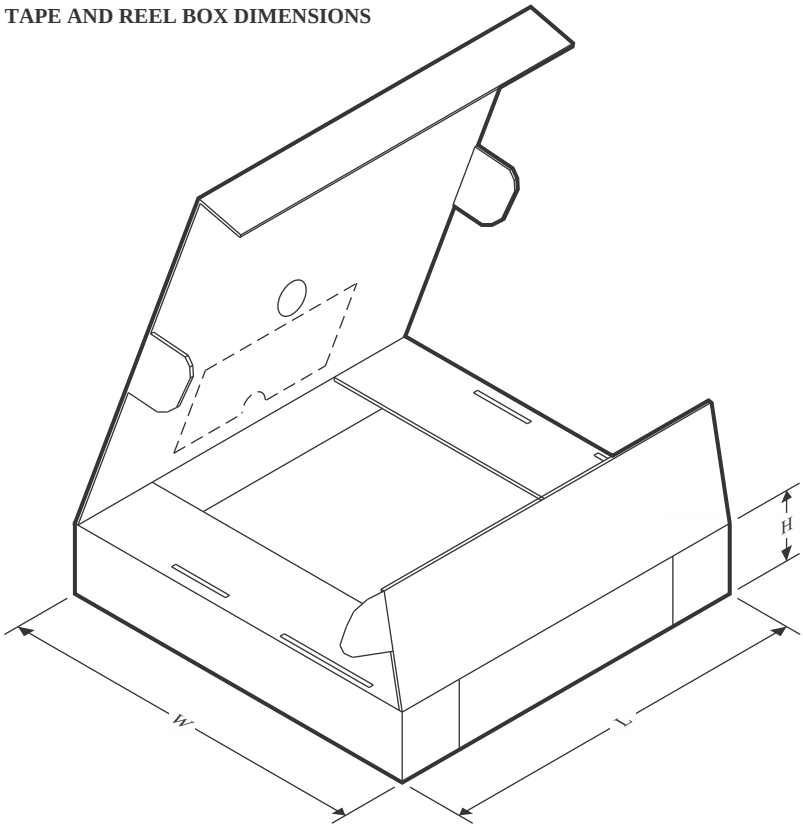
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
INA381A1IDGSR	VSSOP	DGS	10	2500	330.0	12.4	5.25	3.35	1.25	8.0	12.0	Q1
INA381A1IDSGR	WSON	DSG	8	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
INA381A2IDGSR	VSSOP	DGS	10	2500	330.0	12.4	5.25	3.35	1.25	8.0	12.0	Q1
INA381A2IDSGR	WSON	DSG	8	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
INA381A2IDSGRG4	WSON	DSG	8	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
INA381A3IDGSR	VSSOP	DGS	10	2500	330.0	12.4	5.25	3.35	1.25	8.0	12.0	Q1
INA381A3IDSGR	WSON	DSG	8	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
INA381A3IDSGRG4	WSON	DSG	8	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
INA381A4IDGSR	VSSOP	DGS	10	2500	330.0	12.4	5.25	3.35	1.25	8.0	12.0	Q1
INA381A4IDSGR	WSON	DSG	8	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
INA381A4IDSGRG4	WSON	DSG	8	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

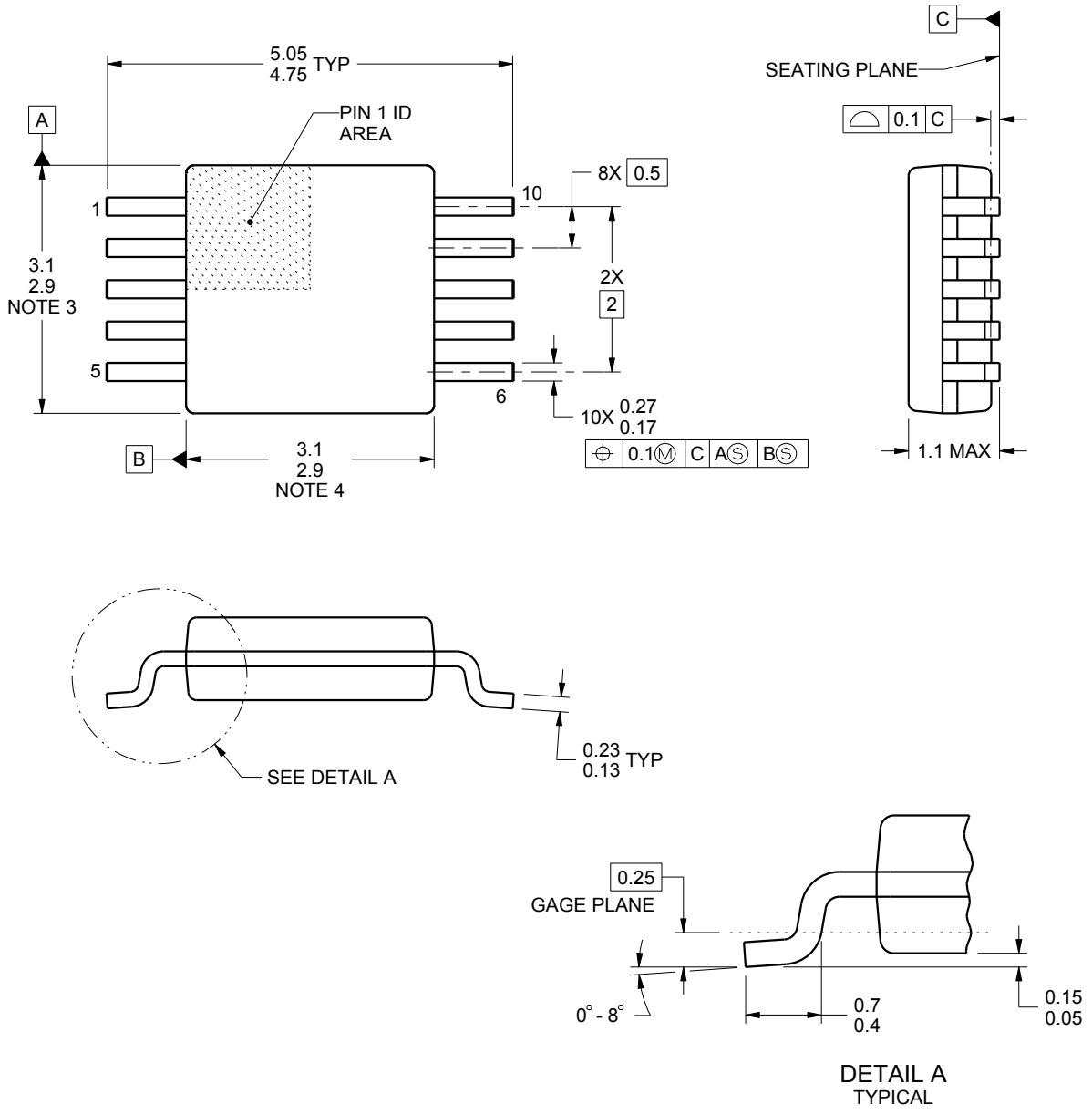
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
INA381A1IDGSR	VSSOP	DGS	10	2500	366.0	364.0	50.0
INA381A1IDSGR	WSON	DSG	8	3000	210.0	185.0	35.0
INA381A2IDGSR	VSSOP	DGS	10	2500	366.0	364.0	50.0
INA381A2IDSGR	WSON	DSG	8	3000	210.0	185.0	35.0
INA381A2IDSGRG4	WSON	DSG	8	3000	210.0	185.0	35.0
INA381A3IDGSR	VSSOP	DGS	10	2500	366.0	364.0	50.0
INA381A3IDSGR	WSON	DSG	8	3000	210.0	185.0	35.0
INA381A3IDSGRG4	WSON	DSG	8	3000	210.0	185.0	35.0
INA381A4IDGSR	VSSOP	DGS	10	2500	366.0	364.0	50.0
INA381A4IDSGR	WSON	DSG	8	3000	210.0	185.0	35.0
INA381A4IDSGRG4	WSON	DSG	8	3000	210.0	185.0	35.0

PACKAGE OUTLINE

DGS0010A

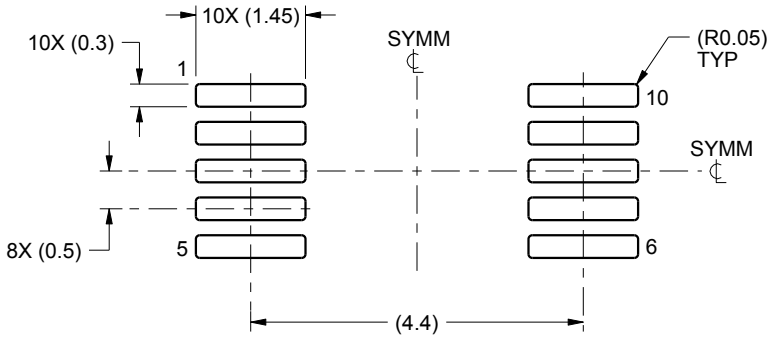
VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE

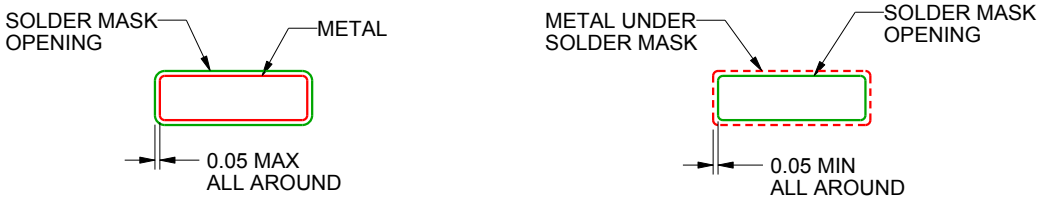


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187, variation BA.



LAND PATTERN EXAMPLE
SCALE:10X

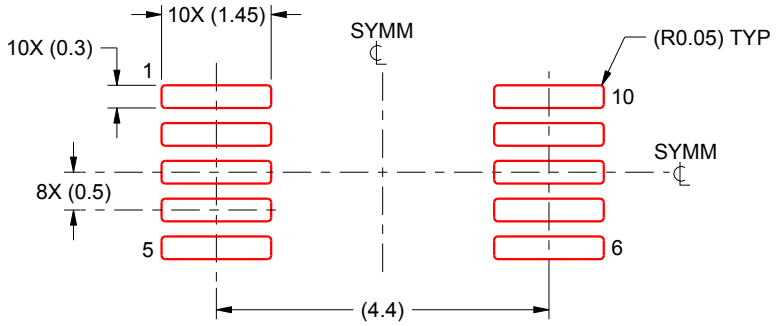


SOLDER MASK DETAILS
NOT TO SCALE

4221984/A 05/2015

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:10X

4221984/A 05/2015

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

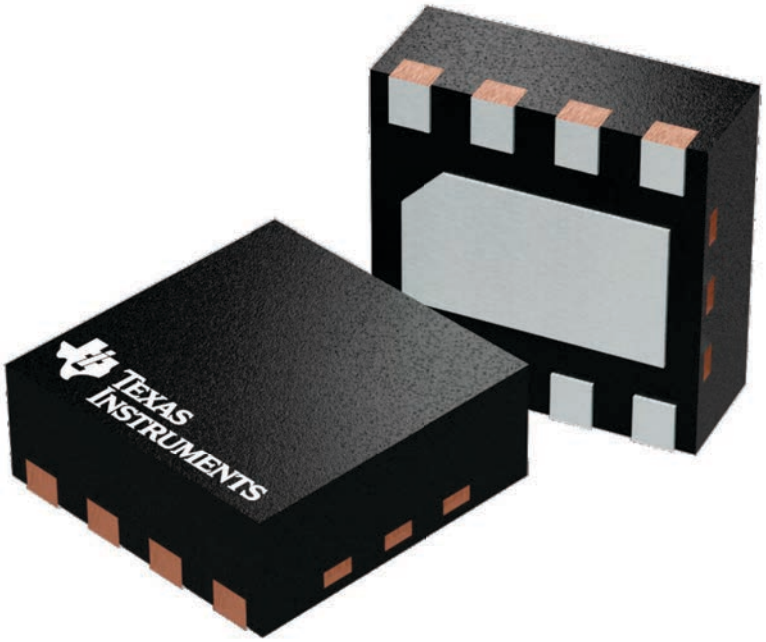
DSG 8

WSON - 0.8 mm max height

2 x 2, 0.5 mm pitch

PLASTIC SMALL OUTLINE - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



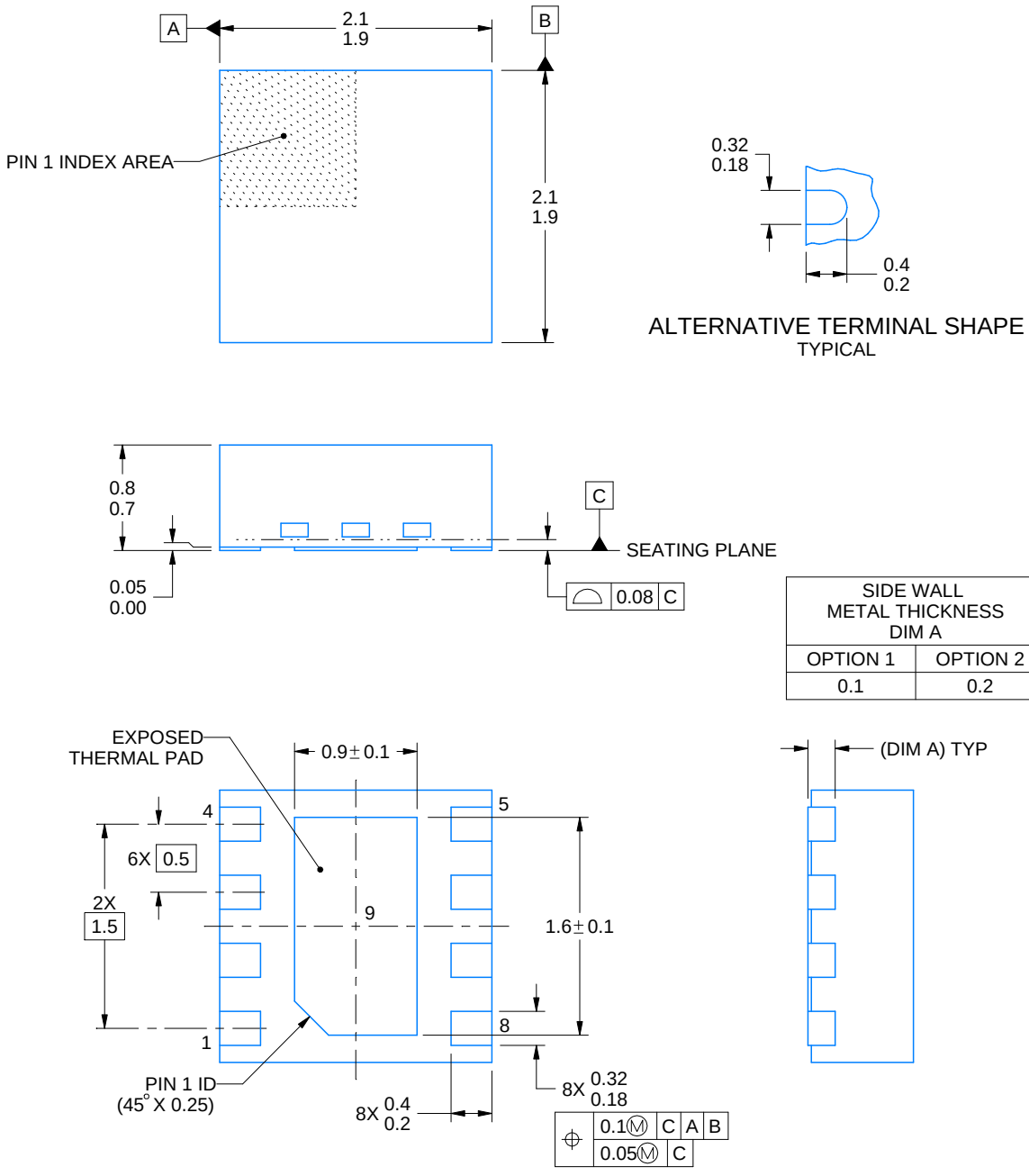
4224783/A

PACKAGE OUTLINE

DSG0008A

WSON - 0.8 mm max height

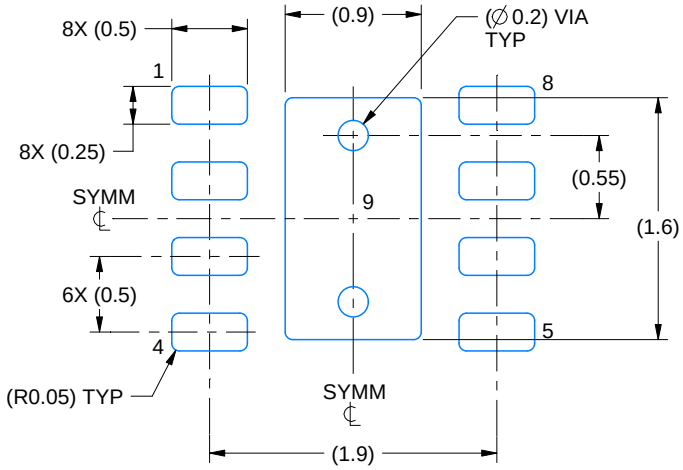
PLASTIC SMALL OUTLINE - NO LEAD



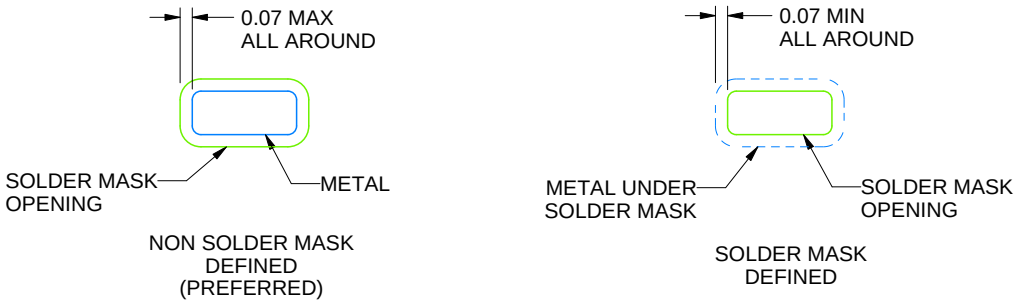
4218900/E 08/2022

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:20X

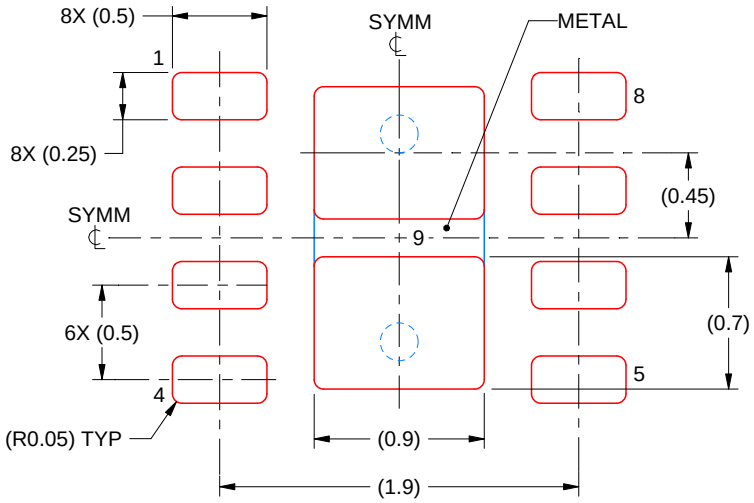


SOLDER MASK DETAILS

4218900/E 08/2022

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 9:
87% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:25X

4218900/E 08/2022

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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