ISO1176T トランス・ドライバ内蔵、絶縁型 Profibus RS-485 トランシーバ

1 特長

- EN 50170 および TIA/EIA-485-A の要件を満たす (または上回る) 性能
- 最大 40Mbps の信号速度
- トランス・ドライバを内蔵した簡単な絶縁型電源設計
- 標準的な効率が 60% 超 (I_{LOAD} = 100mA) - SLUU471 を参照
- 2.1V を超える差動出力 (54Ω 負荷時)
- 10pF の低バス容量 (最大値)
- バスの開放、短絡、またはアイドル時のフェイルセーフを備えるレシーバ
- 50kV/μs の標準過渡耐性
- 安全および規制の認定
  - DIN EN IEC 60747-17 (VDE 0884-17) に準拠した 4242 V_{PK} の基本絶縁
  - UL 1577 に準拠した 2500 V_{RMS} での 1 分間の絶縁
  - CSA 60950-1 および CSA 61010-1 規格

2 アプリケーション

- Profibus®
- ファクトリ・オートメーション
- ネットワーク接続センサ
- モーター / モーション制御
- HVAC およびビルディング・オートメーション・ネットワーク
- ネットワーク接続セキュリティ・ステーション

3 概要

ISO1176T は、絶縁トランスに 1 次電圧を供給する発振器出力を内蔵した絶縁型差動ライン・トランシーバです。このデバイスは、グランド・ループが切断され、はるかに大きな同相電圧範囲で動作できるため、長い伝送ラインに理想的です。

各デバイスの対称型絶縁バリアは、ライン・トランシーバとロジックレベル・インターフェイスとの間で、VDE に従い、4242V_{PK} で 60 秒間の絶縁を行うことがテスト済みです。

ガルバニック絶縁型差動バス・トランシーバは、マルチポイント・バス伝送ライン上での双方向データ通信を目的として設計された集積回路 (IC) です。このトランシーバは、ガルバニック絶縁型の差動ライン・ドライバと差動入力ライン・レシーバを組み合わせたものです。ドライバの ISODE ピン (ピン 10) のアクティブ HIGH イネーブルと絶縁されたイネーブル状態出力で方向の制御を行います。ドライバの差動出力とレシーバの差動入力は、差動入出力 (I/O) バス・ポートを構成するように内部で接続されています。これらのポートは、ドライバがディセーブルされている場合、または V_{CC2} = 0 の場合、バスへの負荷を最小化するように設計されています。

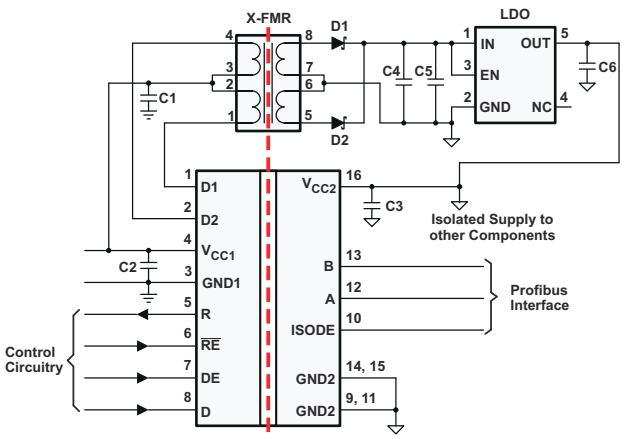
ケーブル接続されたすべての I/O は、各種ノイズ源からの電気的ノイズの過渡現象にさらされる可能性があります。このようなノイズ過渡は、十分な大きさと持続時間を持つ場合、トランシーバや隣接する敏感な回路に損傷を与える可能性があります。ISO1176T は、データの破損や高価な制御回路の損傷のリスクを大幅に低減できます。

このデバイスは、-40℃～85℃の周囲温度範囲で動作が規定されています。

製品情報(1)

部品番号	パッケージ	本体サイズ (公称)
ISO1176T	SOIC (16)	10.30mm × 7.50mm

(1) 利用可能なすべてのパッケージについては、データシートの末尾にある注文情報を参照してください。



代表的なアプリケーション

英語版の TI 製品についての情報を翻訳したこの資料は、製品の概要を確認する目的で便宜的に提供しているものです。該当する正式な英語版の最新情報は、www.ti.com で閲覧でき、その内容が常に優先されます。TI では翻訳の正確性および妥当性につきましては一切保証いたしません。実際の設計などの前には、必ず最新版の英語版をご参照くださいますようお願いいたします。

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4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision G (October 2015) to Revision H (August 2023) — **Page**

- VDE 規格を DIN EN IEC 60747-17 (VDE 0884-17) に変更 ... 1
- Updated Thermal Characteristics, Safety Limiting Values, and Thermal Derating Curves to provide more accurate system-level thermal calculations ... 7
- Updated electrical and switching characteristics to match device performance ... 8

Changes from Revision F (October 2012) to Revision G (October 2015) — **Page**

- 「ピン構成および機能」セクション、「ESD 定格」表、「機能説明」セクション、「デバイスの機能モード」セクション、「アプリケーションと実装」セクション、「電源に関する推奨事項」セクション、「レイアウト」セクション、「デバイスおよびドキュメントのサポート」セクション、「メカニカル、パッケージ、および注文情報」セクションを追加 ... 1
- VDE 規格を DIN V VDE V 0884-10 (VDE V 0884-10):2006-12 に変更 ... 1

Changes from Revision E (August 2011) to Revision F (October 2012) — **Page**

- Changed From "ISO1176T Reference Design SLLU471" To: "ISO1176T Reference Design SLUU471" ... 32

Changes from Revision D (May 2011) to Revision E (August 2011) — **Page**

- Deleted the MIN and MAX values for t_{r_D}, t_{f_D} and t_{BBM} specifications in the Transformer Driver Characteristics table ... 11
- Changed test conditions from 1.9 V to 2.4 V, and changed TYP value from 230 to 350 for f_{St} specification in the Transformer Driver Characteristics table ... 11

Changes from Revision C (February 2011) to Revision D (May 2011) — **Page**

- 図 9-2 を追加 ... 1

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- Moved the Pin Description closer to the Pin drawing..... 4

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5 Pin Configuration and Functions

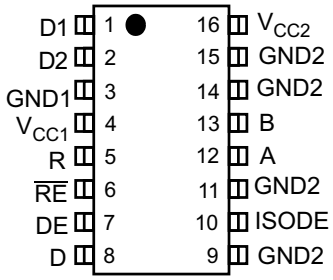


図 5-1. DW Package 16-Pin SOIC Top View

Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
A	12	I/O	Non-inverting Driver Output / Receiver Input
B	13	I/O	Inverting Driver Output / Receiver Input
D	8	I	Driver Input
D1	1	O	Transformer Driver Terminal 1, Open Drain Output
D2	2	O	Transformer Driver Terminal 2, Open Drain Output
DE	7	I	Driver Enable Input
GND1	3	—	Logic-side Ground
GND2	9, 11, 14, 15	—	Bus-side Ground. All pins are internally connected.
ISODE	10	O	Bus-side Driver Enable Output Status
R	5	O	Receiver Output
$\overline{RE}$	6	I	Receiver Enable Input. This pin has complementary logic.
V_{CC1}	4	—	Logic-side Power Supply
V_{CC2}	16	—	Bus-side Power Supply

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6 Specifications

6.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage(2)	V_{CC1}, V_{CC2}	-0.5	6	V
V_O	Voltage at any bus I/O terminal		-9	14	V
	Voltage at D1, D2			14	V
V_I	Voltage input	D, DE or $\overline{RE}$	-0.5	6	V
I_O	Receiver output current	Receiver output current	-10	10	mA
I_{D1}, I_{D2}	Transformer Driver Output Current			450	mA
T_J	Junction temperature			150	℃
T_{stg}	Storage temperature		-65	150	℃

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values except differential I/O bus voltages are with respect to the referenced network ground terminal and are peak voltage values.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$ Electrostatic Discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	Bus pins and GND1	±6000	V
		Bus pins and GND2	±10000	V
		All pins	±4000	V
	Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)		±1500	V
	Machine model (MM), ANSI/ESDS5.2-1996		±200	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Logic-side supply voltage, V_{CC1} (with respect to GND1)		3		5.5	V
V_{CC}	Bus-side supply voltage, V_{CC2} (with respect to GND2)		4.75		5.25	V
V_{CM}	Voltage at either bus I/O terminal	A or B	-7		12	V
V_{IH}	High-level input voltage	PV, $\overline{RE}$	2		5.5	V
V_{IH}	High-level input voltage	D, DE	0.7*V_{CC1}			V
V_{IL}	Low-level input voltage	PV, $\overline{RE}$	0		0.8	V
V_{IL}	Low-level input voltage	D, DE			0.3*Vcc	V
V_{ID}	Differential input voltage	A with respect to B	-12		12	V
I_O	Output current	Driver	-70		70	mA
I_O	Output current	Receiver	-8		8	mA
T_A	Ambient temperature		-40		85	°C

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			MIN	NOM	MAX	UNIT
$1 / t_{UI}$	Signaling Rate				40	Mbps

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6.4 Thermal Information

THERMAL METRIC[1]		ISO1176T DW (SOIC) 16 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	76	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	37.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	44.6	°C/W
ψ_{JT}	Junction-to-top characterization parameter	13.9	°C/W
ψ_{JB}	Junction-to-board characterization parameter	37.9	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	-	°C/W

(1) For more information about traditional and new thermal metrics, see the no.

6.5 Power Ratings

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
P_D	Maximum power dissipation (both sides)	V_{CC1} = V_{CC2} = 5.25 V, T_J = 150°C, C_L = 15 pF, Input at 20 MHz 50% duty cycle square wave			719	mW

6.6 Insulation Specifications

PARAMETER		TEST CONDITIONS	VALUE DW-16	UNIT
CLR	External clearance[1]	Shortest terminal-to-terminal distance through air	8	mm
CPG	External creepage[1]	Shortest terminal-to-terminal distance across the package surface	8	mm
DTI	Distance through the insulation	Minimum internal gap (internal clearance)	8	um
CTI	Comparative tracking index	DIN EN 60112 (VDE 0303-11); IEC 60112	>400	V
	Material group	According to IEC 60664-1	II	
	Overvoltage category per IEC 60664-1	Rated mains voltage ≤ 150 V_{RMS}	I-IV	
		Rated mains voltage ≤ 300 V_{RMS}	I-III	
DIN EN IEC 60747-17 (VDE 0884-17) [2]				
V_{IORM}	Maximum repetitive peak isolation voltage	AC voltage (bipolar)	566	V_{PK}
V_{IOTM}	Maximum transient isolation voltage	V_{TEST} = V_{IOTM}, t = 60 s (qualification); V_{TEST} = 1.2 x V_{IOTM}, t= 1 s (100% production)	4242	V_{PK}
q_{pd}	Apparent charge[3]	Method b; At routine test (100% production) V_{ini} = 1.2 x V_{IOTM}, t_{ini} = 1 s; $V_{pd(m)}$ = 1.5 x V_{IORM}, t_m = 1 s	≤5	pC
C_{IO}	Barrier capacitance, input to output[4]	V_{IO} = 0.4 x sin (2πft), f = 1 MHz	2	pF
C_I	Input capacitance to ground	V_I = VCC/ 2 + 0.4×sin(2πft), f = 1 MHz, VCC = 5 V	2	pF
R_{IO}	Isolation resistance[4]	V_{IO} = 500 V, T_A = 25°C	$>10^{12}$	Ω
		V_{IO} = 500 V, T_S = 150°C	$>10^9$	
	Pollution degree		2	
	Climatic category		40/085/21	
UL 1577				
V_{ISO}	Maximum withstanding isolation voltage	V_{TEST} = V_{ISO} , t = 60 s (qualification), V_{TEST} = 1.2 x V_{ISO} , t = 1 s (100% production)	2500	V_{RMS}

(1) Creepage and clearance requirements should be applied according to the specific equipment isolation standards of an application. Care should be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the

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isolator on the printed-circuit board do not reduce this distance. Creepage and clearance on a printed-circuit board become equal in certain cases. Techniques such as inserting grooves and/or ribs on a printed-circuit board are used to help increase these specifications.

(2) This coupler is suitable for *basic electrical insulation* only within the safety ratings. Compliance with the safety ratings shall be ensured by means of suitable protective circuits.

(3) Apparent charge is electrical discharge caused by a partial discharge (pd).

(4) All pins on each side of the barrier tied together creating a two-terminal device.

6.7 Safety-Related Certifications

VDE	CSA	UL
Certified according to DIN EN IEC 60747-17 (VDE 0884-17)	Certified according to IEC 60950-1 and IEC 61010-1	Certified according to UL 1577 Component Recognition Program
Basic Insulation Maximum Transient Isolation Voltage, 4242 V_{PK} Maximum Surge Isolation Voltage, 4000 V_{PK} Maximum repetitive peak isolation Voltage, 566 V_{PK}	3000 V_{RMS} Isolation Rating; Reinforced insulation per CSA 61010-1 and IEC 61010-1 150 V_{RMS} working voltage; Basic insulation per CSA 61010-1 and IEC 61010-1 600 V_{RMS} working voltage; Basic insulation per CSA 60950-1 and IEC 60950-1 760 V_{RMS} working voltage	Single protection, 2500 V_{RMS}
Certificate number: 40047657	Master contract number: 220991	File number: E181974

6.8 Safety Limiting Values

Safety limiting(1) intends to minimize potential damage to the isolation barrier upon failure of input or output circuitry.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DW-16 PACKAGE						
I_S	Safety input, output, or supply current	$R_{\theta JA}$ = 76°C/W, V_I = 5.5 V, T_J = 150°C, T_A = 25°C,			299	mA
T_S	Maximum safety temperature				150	°C

(1) The maximum safety temperature, T_S, has the same value as the maximum junction temperature, T_J, specified for the device. The I_S and P_S parameters represent the safety current and safety power respectively. The maximum limits of I_S and P_S should not be exceeded. These limits vary with the ambient temperature, T_A.
The junction-to-air thermal resistance, $R_{\theta JA}$, in the table is that of a device installed on a high-K test board for leaded surface-mount packages. Use these equations to calculate the value for each parameter:
$T_J = T_A + R_{\theta JA} \times P$, where P is the power dissipated in the device.
$T_{J(max)} = T_S = T_A + R_{\theta JA} \times P_S$, where $T_{J(max)}$ is the maximum allowed junction temperature.
$P_S = I_S \times V_I$, where V_I is the maximum input voltage.

6.9 Electrical Characteristics: ISODE-Pin

All typical specs are at V_{CC1}=3.3V, V_{CC2}=5V, T_A=27°C, (Min/Max specs are over recommended operating conditions unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = –8 mA	V_{CC2} – 0.8	4.6		V
		I_{OH} = –20 µA	V_{CC2} – 0.1	5		V
V_{OL}	Low-level output voltage	I_{OL} = –8 mA		0.2	0.4	V
		I_{OL} = –20 µA		0	0.1	V

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6.10 Electrical Characteristics: Driver

All typical specs are at V_{CC1}=3.3V, V_{CC2}=5V, T_A=27°C, (Min/Max specs are over recommended operating conditions unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$\|V_{OD}\|$	Open-circuit differential output voltage	$\|V_A-V_B\|$, Figure 9	1.5		V_{CC2}	V
$\|V_{OD(SS)}\|$	Steady state differential output voltage magnitude	See Figure 10 and Figure 14	2.1			V
	Steady state differential output voltage magnitude	Common mode loading with V_{test} from -7V to 12V, See figure 10	2.1			V
$\Delta\|V_{ODSS}\|$	Change in differential output voltage between two states	R_L = 54 ohms, See Figure 12 and Figure 13	–200		200	mV
$V_{OC(SS)}$	Steady state common-mode output voltage	R_L = 54 ohms, See Figure 12 and Figure 13	2		3	V
$\Delta V_{OC(SS)}$	change in steady-state common-mode output voltage between two states	R_L = 54 ohms, See Figure 12 and Figure 13	–200		200	mV
$V_{OC(PP)}$	Peak-to-peak common-mode output voltage	R_L = 54 ohms, See Figure 12 and Figure 13		0.5		V
$V_{OD(RING)}$	Differential output voltage over and undershoot	See Figure 14 and Figure 17			10	$\%V_{OD(PP)}$
I_I	Input current	D, DE at 0 V or V_{CC1}	–10		10	µA
$I_{O(OFF)}$	Output current with power off	Vcc_2 = 0 V	See receiver input current			µA
I_{OZ}	High-impedance state output current	DE at 0 V	See receiver input current			µA
$I_{OS(P)}$	Peak short circuit output current	DE at V_{CC}, See Figure 15 and Figure 16: V_{OS} = -7 to 12 V	–250		250	mA
$I_{OS(SS)}$	Steady state short-circuit output current	DE at V_{CC}, See Figure 15 and Figure 16: V_{OS} = 12 V, D at GND1			150	mA
		DE at V_{CC}, See Figure 15 and Figure 16: V_{OS} = -7 V, D at V_{CC1}	–150			mA
C_{OD}	Differential output capacitance			7	18.8	pF
CMTI	Common-mode transient immunity	See Figure 27	25			kV/µs

6.11 Electrical Characteristics: Receiver

All typical specs are at V_{CC1}=3.3V, V_{CC2}=5V, T_A=27°C, (Min/Max specs are over recommended operating conditions unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IT+}	Positive-going input threshold voltage	I_O = –8 mA, See Figure 22		-80	–10	mV
$V_{IT–}$	Negative-going input threshold voltage	I_O = 8 mA, See Figure 22	–200	-120		mV
V_{hys}	Input hysteresis ($V_{IT+} – V_{IT–}$)			40		mV
V_{OH}	Output Voltage	V_{CC1} at 3.3 V and V_{CC2} at 5V, V_{ID} = 200mV, I_O = -8mA	V_{CC1}-0.4	3		V
V_{OH}	Output Voltage	V_{CC1} at 3.3 V and V_{CC2} at 5V, V_{ID} = 200mV, I_O = -20uA	V_{CC1}-0.1	3.3		V
V_{OL}	Output Voltage	V_{CC1} at 3.3 V and V_{CC2} at 5V, V_{ID} = -200mV, I_O = 8mA		0.2	0.4	V
V_{OL}	Output Voltage	V_{CC1} at 3.3 V and V_{CC2} at 5V, V_{ID} = -200mV, I_O = 20uA		0	0.1	V
V_{OH}	Output Voltage	V_{CC1} at 5 V and V_{CC2} at 5V, V_{ID} = 200mV, I_O = -8mA	V_{CC1}-0.8	4.6		V
V_{OH}	Output Voltage	V_{CC1} at 5 V and V_{CC2} at 5V, V_{ID} = 200mV, I_O = -20uA	V_{CC1}-0.1	5		V
V_{OL}	Output Voltage	V_{CC1} at 5 V and V_{CC2} at 5V, V_{ID} = -200mV, I_O = 8mA		0.2	0.4	V
V_{OL}	Output Voltage	V_{CC1} at 5 V and V_{CC2} at 5V, V_{ID} = -200mV, I_O = 20uA		0	0.1	V

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All typical specs are at V_{CC1}=3.3V, V_{CC2}=5V, T_A=27°C, (Min/Max specs are over recommended operating conditions unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_A or I_B	Bus pin input current	V_I = -7 V or 12 V, other input = 0V: V_{CC} = 4.75 V or 5.25 V	-160		200	µA
		V_I = -7 V or 12 V, other input = 0V: V_{CC2} = 0 V	-160		200	µA
I_I	Receiver enable input current	$\overline{RE}$ = 0 V or V_{CC1}	-50		50	µA
I_{OZ}	High impedance state output current	$\overline{RE}$ = V_{CC1}	–1		1	µA
R_{ID}	Differential input resistance	A, B	60			kohm
C_{ID}	Differential input capacitance	Test input signal is a 1.5MHz sine wave with $1V_{PP}$ amplitude, C_D is measured across A and B		7	18.8	pF
CMR	Common mode rejection	See Figure 26		4		V

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6.12 Supply Current

Bus loaded or unloaded (over recommended operating conditions unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
DRIVER ENABLED, RECEIVER DISABLED					
I_{CC1} (1)	V_{CC1} = 3.3 V ± 10%, DE, $\overline{RE}$ = 0V or V_{CC1}, No Load		4.5	8	mA
	V_{CC1} = 5 V ± 10%, DE, $\overline{RE}$ = 0V or V_{CC1}, No Load		7	11	mA
I_{CC2} (1)	V_{CC2} = 5 V ± 5%, DE, $\overline{RE}$ = 0V or V_{CC1}, No Load		13.5	18	mA

(1) I_{CC1} and I_{CC2} are measured when device is connected to external power supplies. D1 and D2 are disconnected from external transformer.

6.13 Transformer Driver Characteristics

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{OSC}	Oscillator frequency	V_{CC1} = 5 V ± 10%, D1 and D2 connected to transformer	350	450	610	kHz
		V_{CC1} = 3.3 V ± 10%, D1 and D2 connected to transformer	300	400	550	kHz
R_{ON}	Switch on resistance	D1 and D2 connected to 50Ω pullup resistors		1	2.5	ohm
t_{r_D}	D1, D2 output rise time	V_{CC1} = 5 V ± 10%, See Figure 28, D1 and D2 connected to 50-Ω pullup resistors		80		ns
		V_{CC1} = 3.3 V ± 10%, See Figure 28, D1 and D2 connected to 50-Ω pullup resistors		70		ns
t_{f_D}	D1, D2 output fall time	V_{CC1} = 5 V ± 10%, See Figure 28, D1 and D2 connected to 50-Ω pullup resistors		55		ns
		V_{CC1} = 3.3 V ± 10%, See Figure 28, D1 and D2 connected to 50-Ω pullup resistors		80		ns
f_{St}	Startup frequency	V_{CC1} = 2.4 V, D1 and D2 connected to transformer		350		kHz
t_{BBM}	Break before make time delay	V_{CC1} = 5 V ± 10%, See Figure 28, D1 and D2 connected to 50-Ω pullup resistors		38		ns
		V_{CC1} = 3.3 V ± 10%, See Figure 28, D1 and D2 connected to 50-Ω pullup resistors		140		ns

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6.14 Switching Characteristics: Driver

All typical specs are at V_{CC1}=3.3V, V_{CC2}=5V, T_A=27°C, (Min/Max specs are over recommended operating conditions unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ISO1176						
t_{PHL}, t_{PLH}	Propagation delay	V_{CC1} at 5 V, $_{VCC2}$ at 5 V		23	35	ns
tsk(p)	Pulse skew ($\|t_{PHL} - t_{PLH}\|$)	V_{CC1} at 5 V, $_{VCC2}$ at 5 V		2	7.5	ns
t_{PHL}, t_{PLH}	Propagation delay	V_{CC1} at 3.3 V, V_{CC2} at 5 V			40	ns
tsk(p)	Pulse skew ($\|t_{PHL} - t_{PLH}\|$)	V_{CC1} at 3.3 V, V_{CC2} at 5 V		2	7.5	ns
t_r, t_f	Differential output rise time and fall time	See Figure 17	2	3	7.5	ns
t_{pDE}	DE to ISODE prop delay	See Figure 21			30	ns
$t_{t(MLH)}$, $t_{t(MHL)}$	Output transition skew	See Figure 18			1	ns
$t_{P(AZH)}$, $t_{P(BZH)}$, $t_{P(AZL)}$, $t_{P(BZL)}$	Propagation delay, high-impedance-to-active output	C_L = 50 pF, $\overline{RE}$ at 0 V, See Fgure 19 and Figure 20			80	ns
$t_{P(AHZ)}$, $t_{P(BHZ)}$, $t_{P(ALZ)}$, $t_{P(BLZ)}$	Propagation delay time, active-to-high-impedance output	C_L = 50 pF, $\overline{RE}$ at 0 V, See Fgure 19 and Figure 20			80	ns
$\|t_{P(AZL)} - t_{P(BZH)}\|$, $\|t_{P(AZH)} - t_{P(BZL)}\|$	Enable skew time	C_L = 50 pF, $\overline{RE}$ at 0 V, See Fgure 19 and Figure 20		0.55	1.5	ns
$t_{(CFB)}$	Time from application of short-circuit to current foldback	See Figure 16		0.5		µs
$t_{(TSD)}$	Time from application of short-circuit to thermal shutdown	T_A = 25°C, See Figure 16	100			µs

6.15 Switching Characteristics: Receiver

All typical specs are at V_{CC1}=3.3V, V_{CC2}=5V, T_A=27°C, (Min/Max specs are over recommended operating conditions unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ISO1176						
t_{PHL}, t_{PLH}	Propagation delay	V_{CC1} at 5 V, V_{CC2} at 5 V			50	ns
tsk(p)	Pulse skew ($\|t_{PHL} - t_{PLH}\|$)	V_{CC1} at 5 V, V_{CC2} at 5 V		2	7.5	ns
t_{PHL}, t_{PLH}	Propagation delay	V_{CC1} at 3.3 V, V_{CC2} at 5 V			55	ns
tsk(p)	Pulse skew ($\|t_{PHL} - t_{PLH}\|$)	V_{CC1} at 3.3 V, V_{CC2} at 5 V		2	7.5	ns
t_r, t_f	Differential output rise time and fall time	See Figure 17		2	4	ns
t_{PZH}	Propagation delay time, high-impedance-to-high-level output	DE at V_{CC1}, See Figure 24		13	25	ns
t_{PHZ}	Propagation delay time, high-level-to-high-impedance output	DE at V_{CC1}, See Figure 24		13	25	ns
t_{PZL}	Propagation delay time, high-impedance-to-low-level output	DE at V_{CC}, See Figure 25		13	25	ns
t_{PLZ}	Propagation delay time, low-level-to-high-impedance output	DE at V_{CC}, See Figure 25		13	25	ns

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6.16 Insulation Characteristics Curves

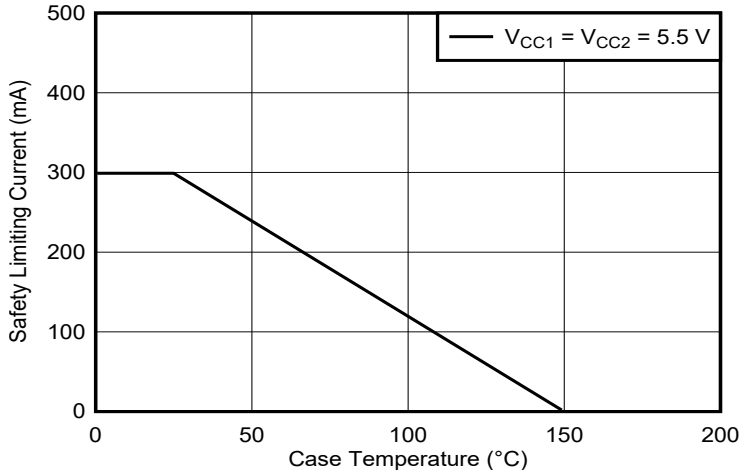


図 6-1. Thermal Derating Curve for Safety Limiting Power for DW-16 Package

6.17 Typical Characteristics

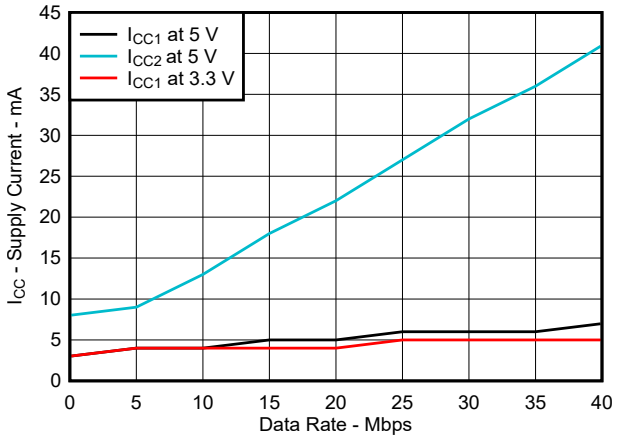
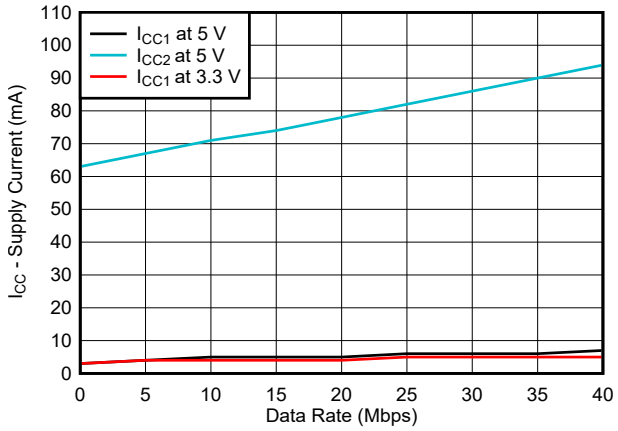


図 6-2. RMS Supply Current (I_{CC1} and I_{CC2}) vs Signaling Rate With No Load



R_L = 54 Ω C_L = 50 pF T_A = 25°C

図 6-3. RMS Supply Current (I_{CC1} and I_{CC2}) vs Signaling Rate With Load

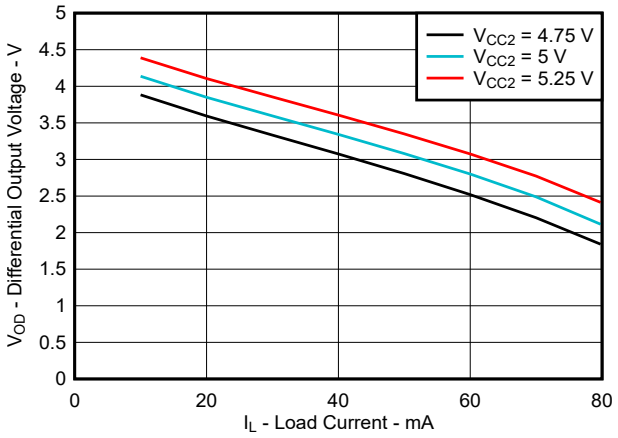
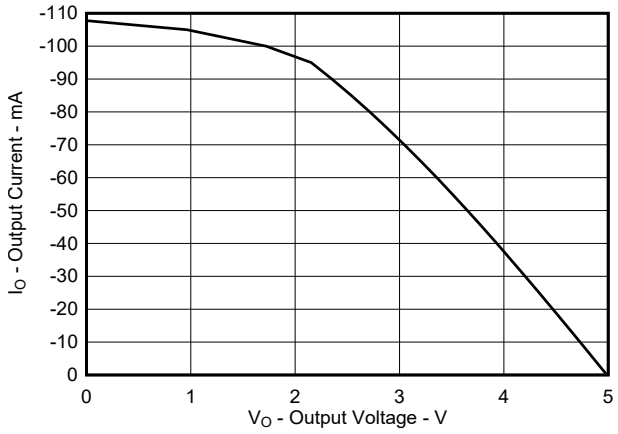


図 6-4. Differential Output Voltage vs Load Current



C_L = 50 pF T_A = 25°C

図 6-5. Receiver High-Level Output Voltage Vs High-Level Output Current

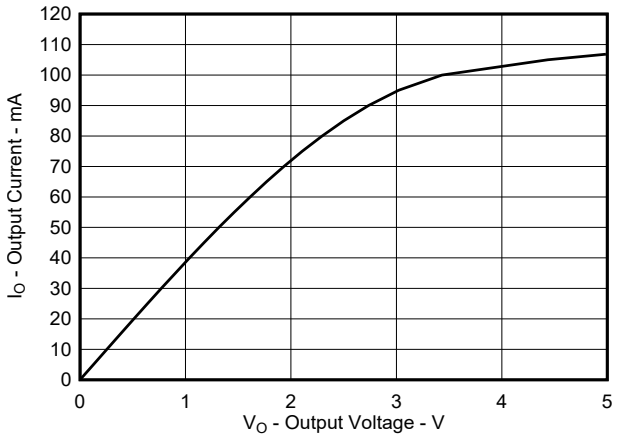


図 6-6. Receiver Low-Level Output Voltage vs Low-Level Output Current

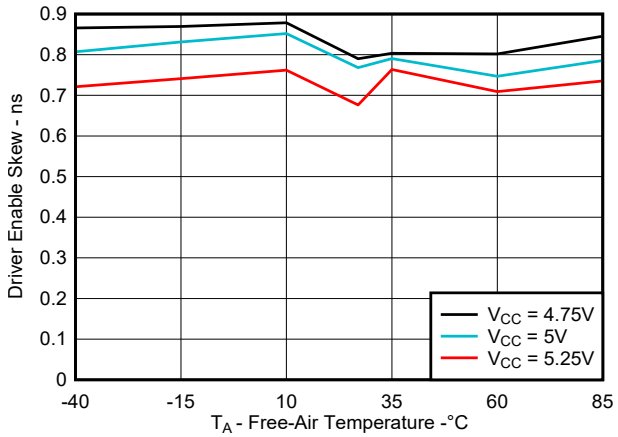


図 6-7. Driver Enable Skew vs Free-Air Temperature

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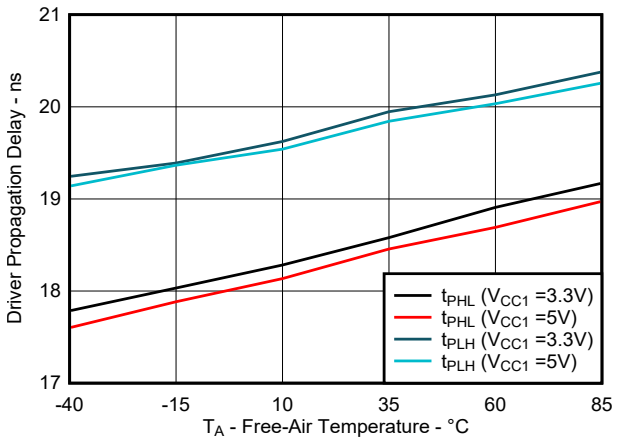


図 6-8. Driver Propagation Delay vs Free-Air Temperature

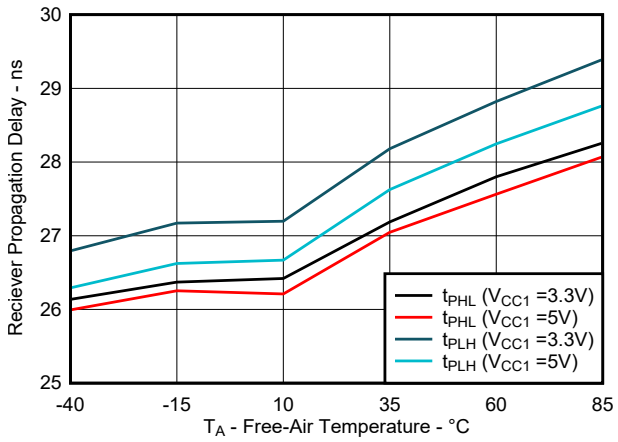


図 6-9. Receiver Propagation Delay vs Free-Air Temperature

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7 Parameter Measurement Information

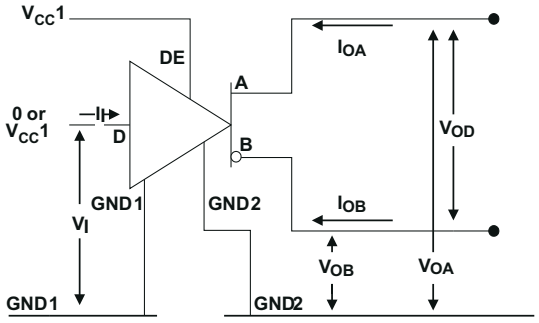


図 7-1. Open Circuit Voltage Test Circuit

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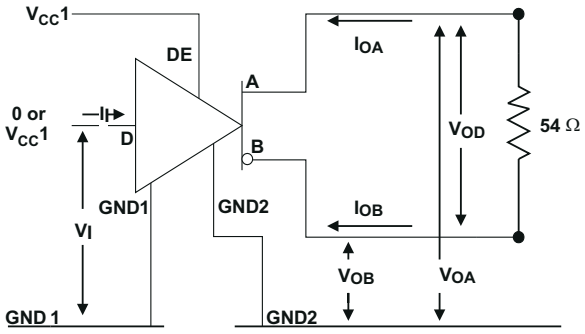


図 7-2. V_{OD} Test Circuit

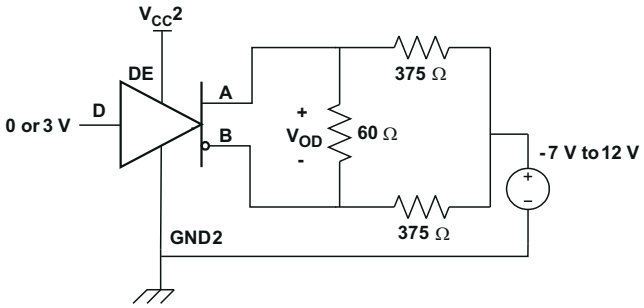


図 7-3. Driver V_{OD} with Common-mode Loading Test Circuit

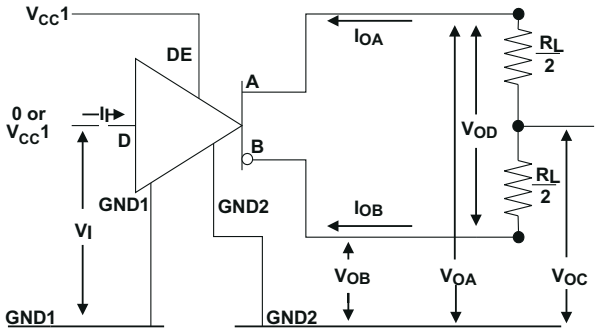


図 7-4. Driver V_{OD} and V_{OC} Without Common-Mode Loading Test Circuit

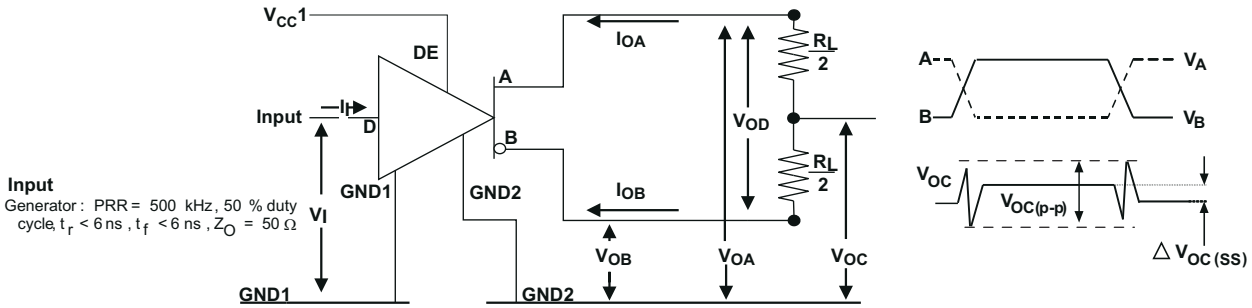


図 7-5. Steady-State Output Voltage Test Circuit and Voltage Waveforms

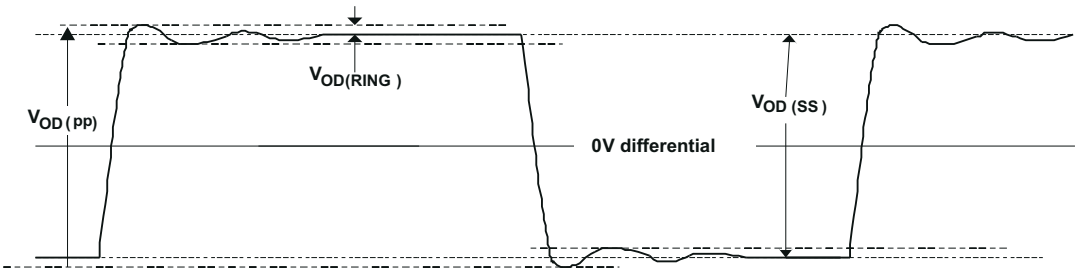


図 7-6. $V_{OD(RING)}$ Waveform and Definitions

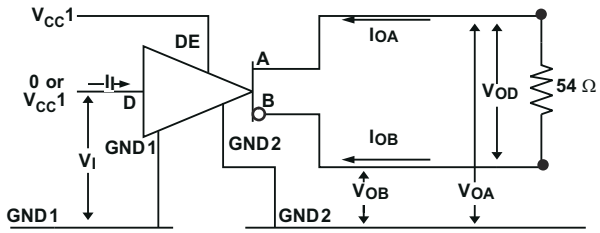


図 7-7. Input Voltage Hysteresis Test Circuit

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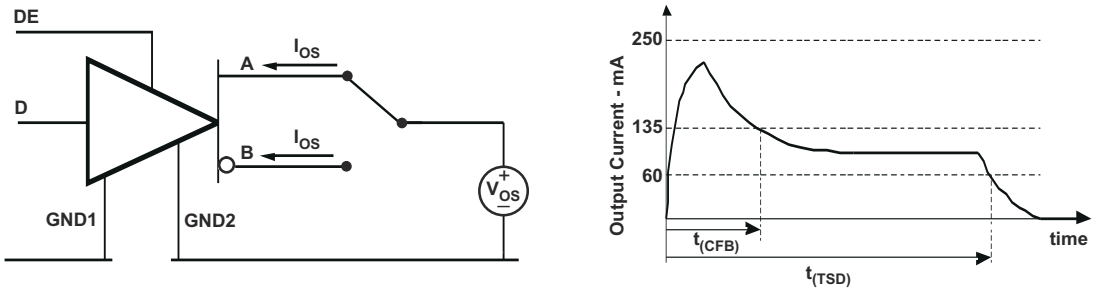


図 7-8. Driver Short-Circuit Test Circuit and Waveforms (Short Circuit applied at Time t=0)

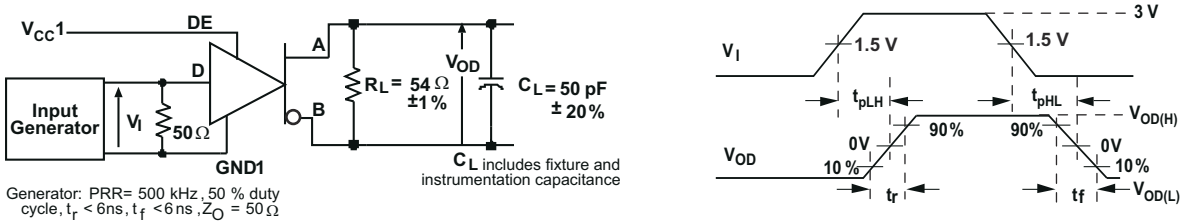


図 7-9. Driver Switching Test Circuit and Waveforms

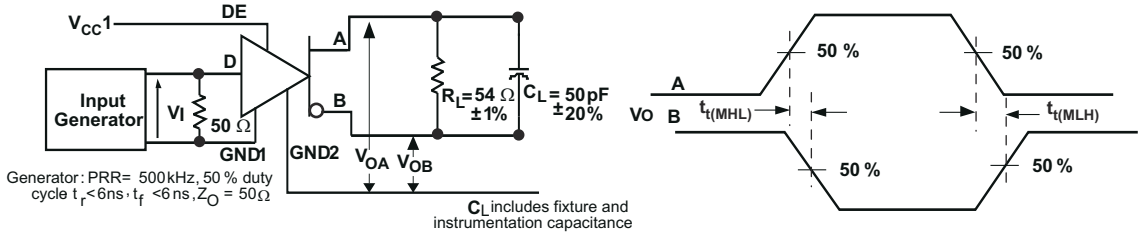


図 7-10. Driver Output Transition Skew Test Circuit and Waveforms

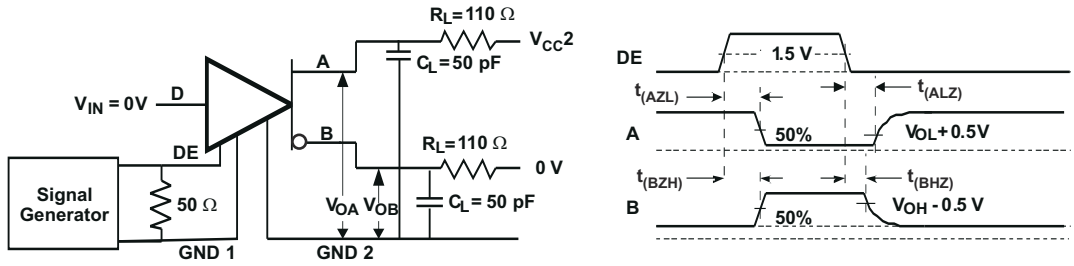


図 7-11. Driver Enable/Disable Test, D at Logic Low Test Circuit and Waveforms

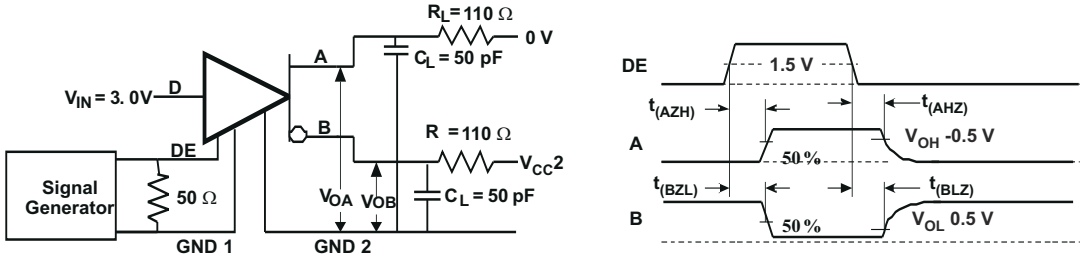


図 7-12. Driver Enable/Disable Test, D at Logic High Test Circuit and Waveforms

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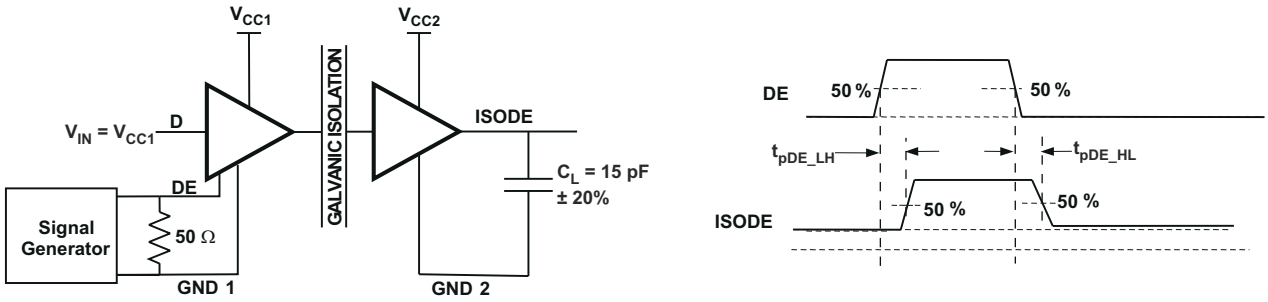


図 7-13. DE to ISODE Prop Delay Test Circuit and Waveforms

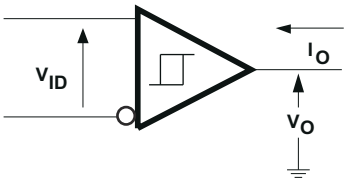


図 7-14. Receiver DC Parameter Definitions

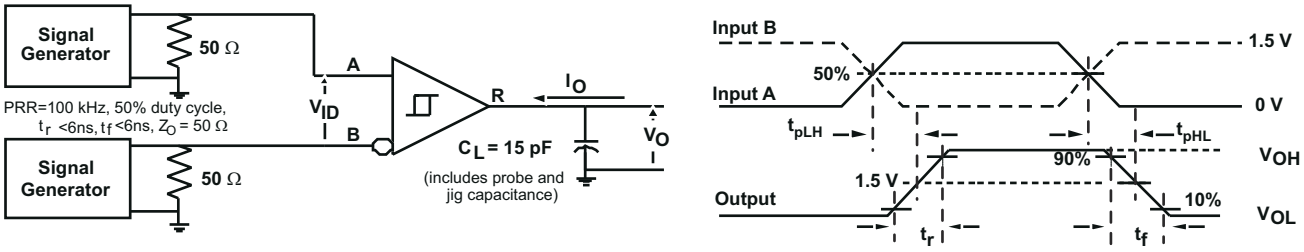


図 7-15. Receiver Switching Test Circuit and Waveforms

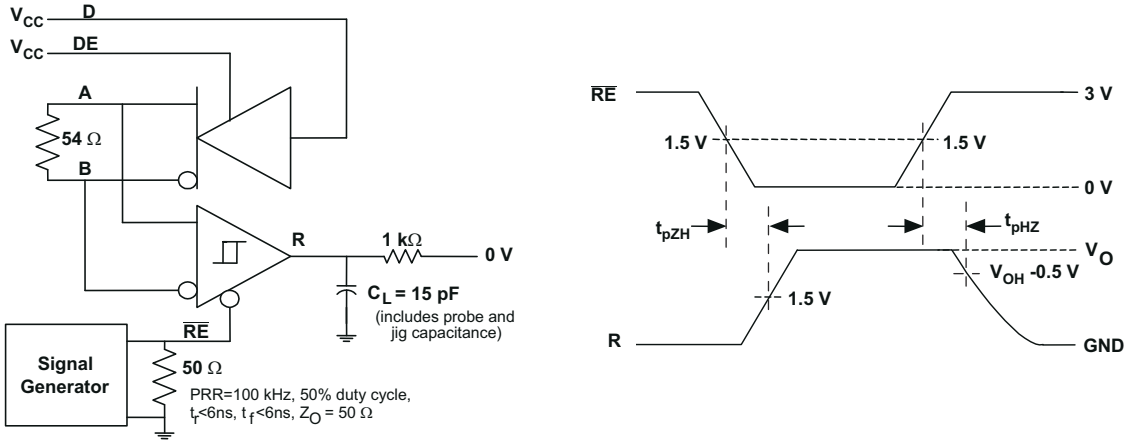


図 7-16. Receiver Enable Test Circuit and Waveforms, Data Output High

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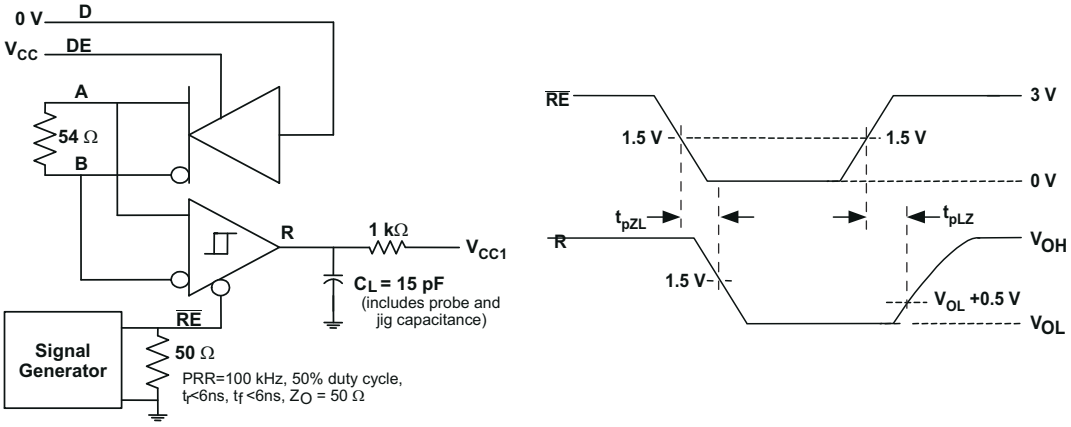


図 7-17. Receiver Enable Test Circuit and Waveforms, Data Output Low

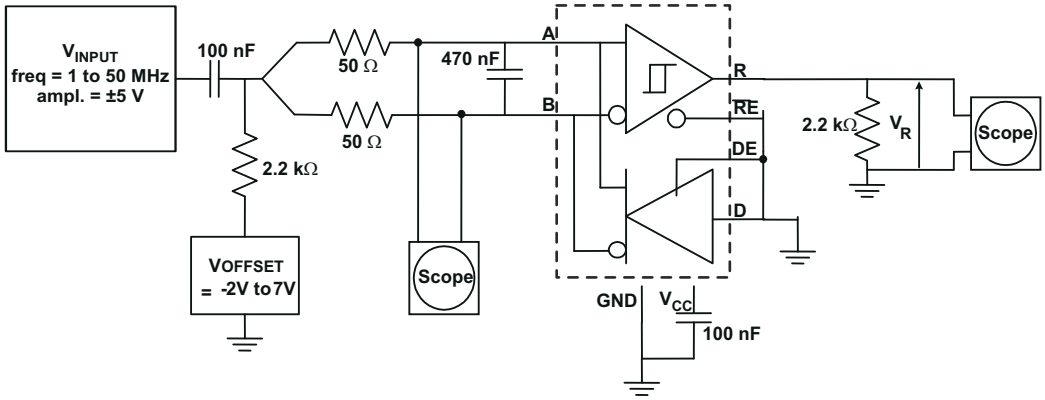


図 7-18. Common-Mode Rejection Test Circuit

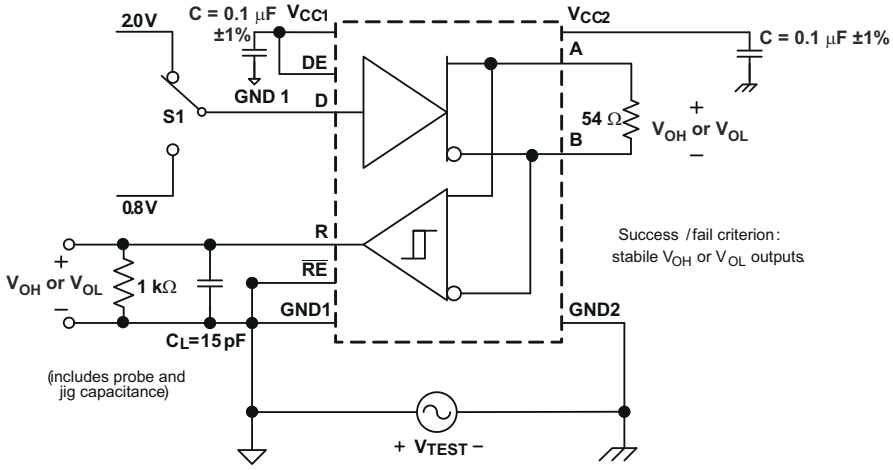


図 7-19. Common-Mode Transient Immunity Test Circuit

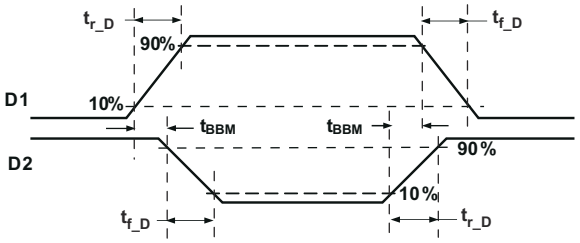


図 7-20. Transition Times and Break-Before-Make Time Delay for D1, D2 Outputs

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8 Detailed Description

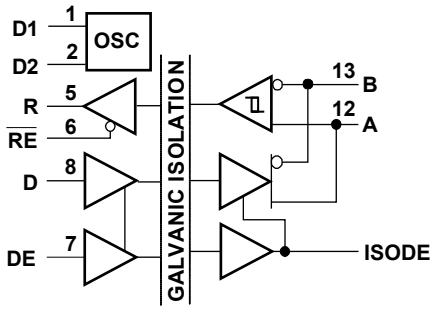
8.1 Overview

The ISO1176T is an isolated half-duplex differential line transceiver that meets the requirements of EN 50170 and TIA/EIA 485/422 applications. It has integrated transformer driver for convenient secondary power supply design. The device is rated to provide galvanic isolation of up to 4242 V_{PK} per VDE and 2500 V_{RMS} per UL 1577. The device has active-high driver enable and active-low receiver enable functions to control the data flow. It has maximum data transmission speed of 40 Mbps.

When the driver enable pin, DE, is logic high, the differential outputs A and B follow the logic states at data input D. A logic high at D causes A to turn high and B to turn low. In this case, the differential output voltage defined as $V_{OD} = V_{(A)} – V_{(B)}$ is positive. When D is low, the output states reverse, B turns high, A becomes low, and V_{OD} is negative. When DE is low, both outputs turn high-impedance. In this condition, the logic state at D is irrelevant. The DE pin has an internal pulldown resistor to ground, thus when left open the driver is disabled (high-impedance) by default. The D pin has an internal pullup resistor to V_{CC}, thus, when left open while the driver is enabled, output A turns high and B turns low.

When the receiver enable pin, $\overline{RE}$, is logic low, the receiver is enabled. When the differential input voltage defined as $V_{ID} = V_{(A)} – V_{(B)}$ is positive and higher than the positive input threshold, V_{IT+}, the receiver output, R, turns high. When V_{ID} is negative and lower than the negative input threshold, $V_{IT–}$, the receiver output, R, turns low. If V_{ID} is between V_{IT+} and $V_{IT–}$ the output is indeterminate. When $\overline{RE}$ is logic high or left open, the receiver output is high-impedance and the magnitude and polarity of V_{ID} are irrelevant. Internal biasing of the receiver inputs causes the output to go failsafe-high when the transceiver is disconnected from the bus (open-circuit), the bus lines are shorted (short-circuit), or the bus is not actively driven (idle bus).

8.2 Functional Block Diagram



8.3 Device Functional Modes

表 8-1 and 表 8-2 are the function tables for the ISO1176T driver and receiver.

表 8-1. Driver Function Table(1)

V_{CC1}	V_{CC2}	INPUT (D)	ENABLE INPUT (DE)	ENABLE OUTPUT (ISODE)	OUTPUTS	
					A	B
PU	PU	H	H	H	H	L
PU	PU	L	H	H	L	H
PU	PU	X	L	L	Z	Z
PU	PU	X	open	L	Z	Z
PU	PU	open	H	H	H	L
PD	PU	X	X	L	Z	Z
PU	PD	X	X	L	Z	Z
PD	PD	X	X	L	Z	Z

(1) PU = Powered Up, PD = Powered Down, H = High Level, L= Low Level, X = Don't Care, Z = High Impedance (off)

表 8-2. Receiver Function Table(1)

V_{CC1}	V_{CC2}	DIFFERENTIAL INPUT $V_{ID} = (V_A – V_B)$	ENABLE ($\overline{RE}$)	OUTPUT (R)
PU	PU	$–0.01V \le V_{ID}$	L	H
PU	PU	$-0.2V < V_{ID} < –0.01V$	L	?
PU	PU	$V_{ID} \le –0.2V$	L	L
PU	PU	X	H	Z
PU	PU	X	open	Z
PU	PU	Open circuit	L	H
PU	PU	Short Circuit	L	H
PU	PU	Idle (terminated) bus	L	H
PD	PU	X	X	Z
PU	PD	X	L	H
PD	PD	X	X	Z

(1) PU = Powered Up, PD = Powered Down, H = High Level, L= Low Level, X = Don't Care, Z = High Impedance (off), ? = Indeterminate

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8.3.1 Device I/O Schematics

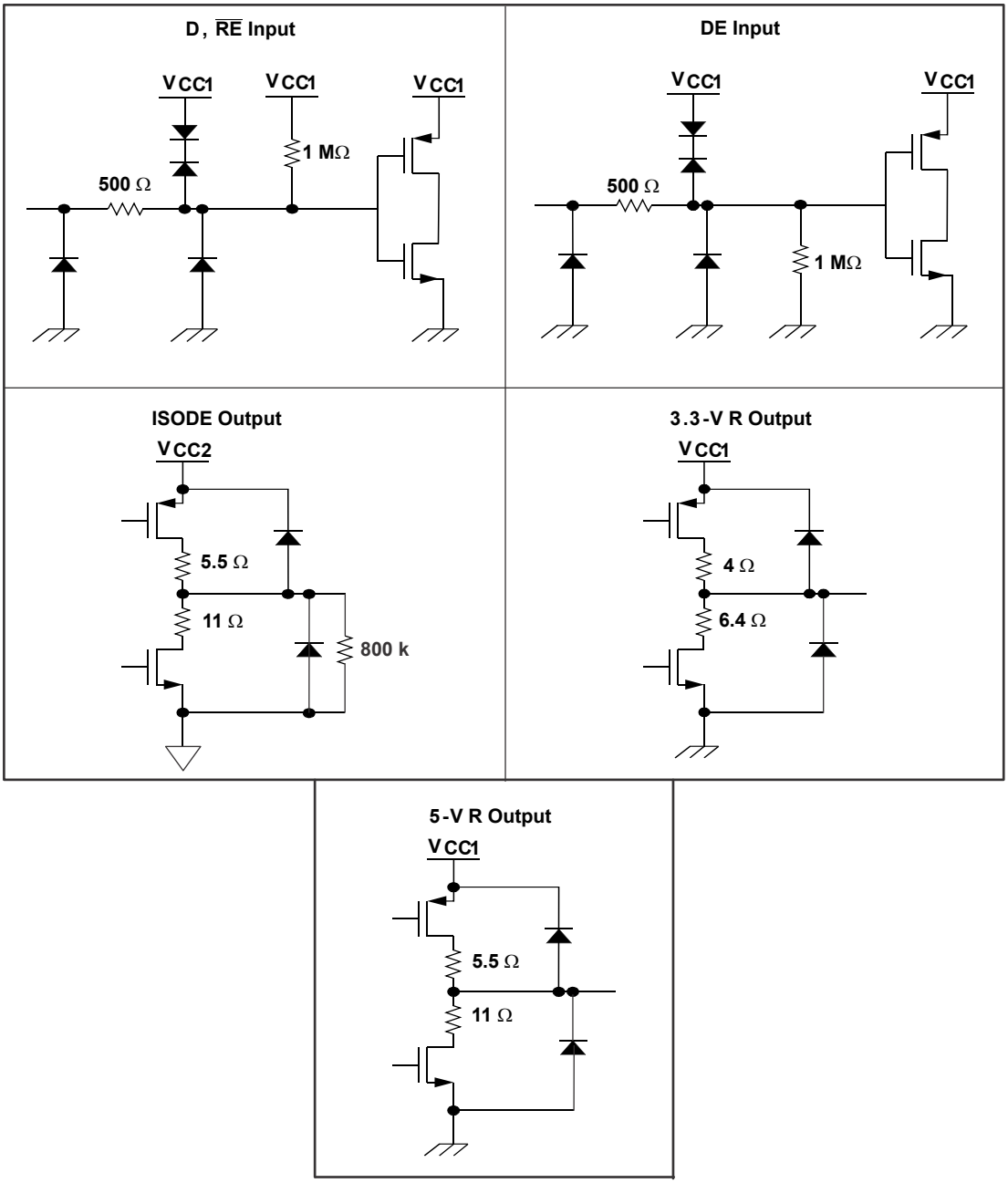


図 8-1. Equivalent Circuit Schematics

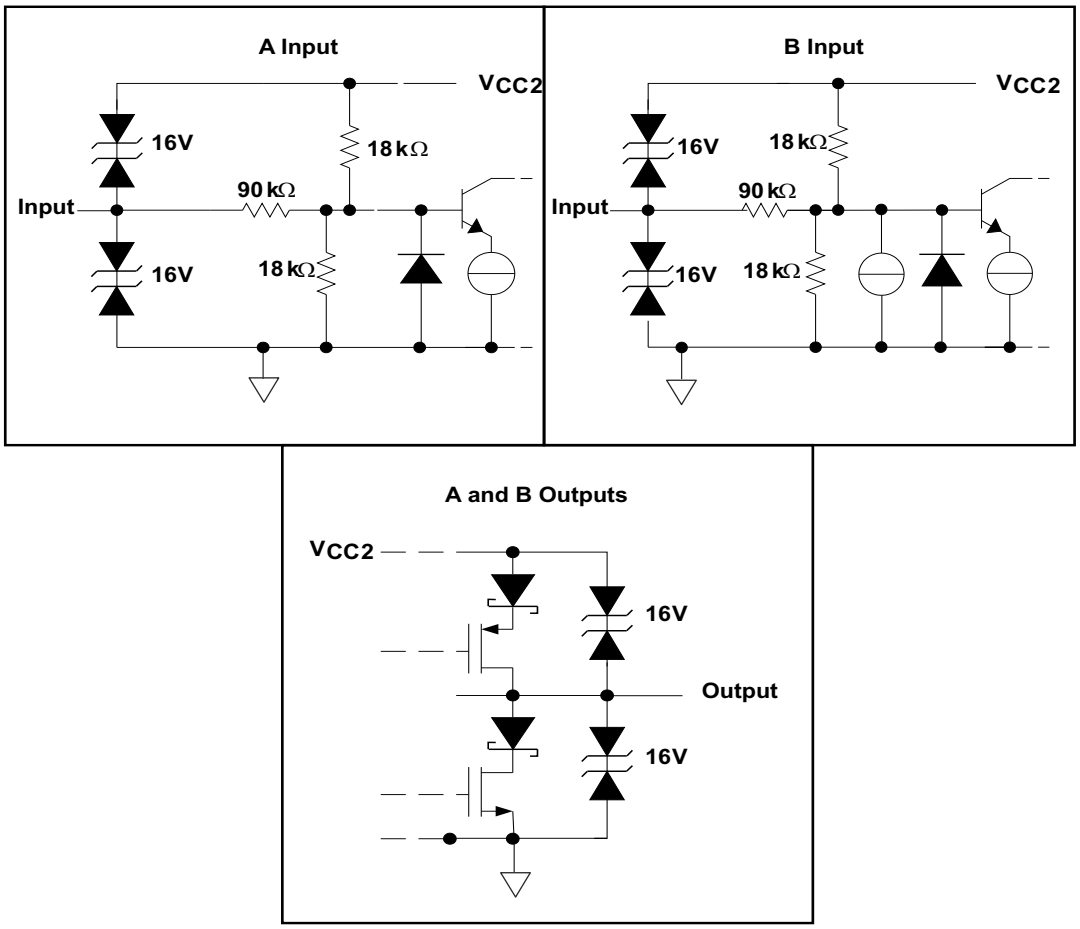


図 8-2. Equivalent Circuit Schematics

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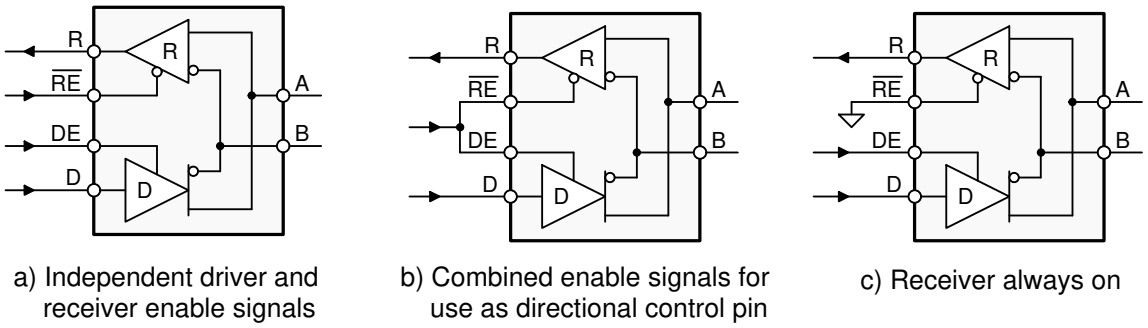
9 Application and Implementation

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9.1 Application Information

The ISO1176T device consists of a RS-485 transceiver, commonly used for asynchronous data transmissions. For half-duplex transmission, only one pair is shared for both transmission and reception of data. To eliminate line reflections, each cable end is terminated with a termination resistor, R(T), whose value matches the characteristic impedance, Z0, of the cable. This method, known as parallel termination, allows for higher data rates over longer cable length.



a) Independent driver and receiver enable signals

b) Combined enable signals for use as directional control pin

c) Receiver always on

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図 9-1. Half-Duplex Transceiver Configurations

9.2 Typical Application

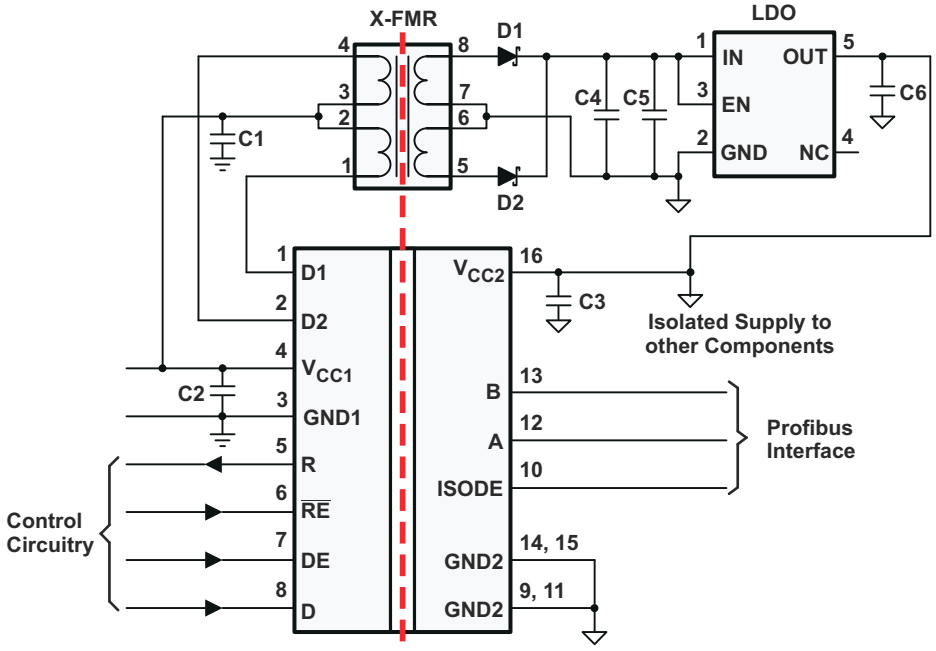


図 9-2. Typical Application

9.2.1 Design Requirements

RS-485 is a robust electrical standard suitable for long-distance networking that may be used in a wide range of applications with varying requirements, such as distance, data rate, and number of nodes.

表 9-1. Design Parameters

PARAMETER	VALUE
Pullup and Pulldown Resistors	1 kΩ to 10 kΩ
Decoupling Capacitors	100 nF

9.2.2 Detailed Design Procedure

9.2.2.1 Transient Voltages

9.2.2.1.1

Isolation of a circuit insulates it from other circuits and earth so that noise develops across the insulation rather than circuit components. The most common noise threat to data-line circuits is voltage surges or electrical fast transients that occur after installation and the transient ratings of ISO1176T are sufficient for all but the most severe installations. However, some equipment manufacturers use their ESD generators to test transient susceptibility of their equipment and can exceed insulation ratings. ESD generators simulate static discharges that may occur during device or equipment handling with low-energy but high voltage transients.

図 9-3 models the ISO1176T bus IO connected to a noise generator. C_{IN} and R_{IN} is the device and any other stray or added capacitance or resistance across the A or B pin to GND2, C_{ISO} and R_{ISO} is the capacitance and resistance between GND1 and GND2 of ISO1176T plus those of any other insulation (transformer, or similar), and we assume stray inductance negligible. From this model, the voltage at the isolated bus return is shown in 式 1:

$$v_{GND2} = v_N \frac{Z_{ISO}}{Z_{ISO} + Z_{IN}} \tag{1}$$

and will always be less than 16 V from V_N. If ISO1176T is tested as a stand-alone device, $R_{IN} = 6 \times 10^4 \Omega$, $C_{IN} = 16 \times 10^{-12}$ F, $R_{ISO} = 10^9 \Omega$ and $C_{ISO} = 10^{-12}$ F.

Note from 図 9-3 that the resistor ratio determines the voltage ratio at low frequency and it is the inverse capacitance ratio at high frequency. In the stand-alone case and for low frequency, as shown in 式 2,

$$\frac{v_{GND2}}{v_N} = \frac{R_{ISO}}{R_{ISO} + R_{IN}} = \frac{10^9}{10^9 + 6 \times 10^4} \tag{2}$$

or essentially all of noise appears across the barrier. At high frequency, as shown in 式 3,

$$\frac{v_{GND2}}{v_N} = \frac{\frac{1}{C_{ISO}}}{\frac{1}{C_{ISO}} + \frac{1}{C_{IN}}} = \frac{1}{1 + \frac{C_{ISO}}{C_{IN}}} = \frac{1}{1 + \frac{1}{16}} = 0.94 \tag{3}$$

and 94% of V_N appears across the barrier. As long as R_{ISO} is greater than R_{IN} and C_{ISO} is less than C_{IN}, most of transient noise appears across the isolation barrier, as it should.

We recommend the reader not test equipment transient susceptibility with ESD generators or consider product claims of ESD ratings above the barrier transient ratings of an isolated interface. ESD is best managed through recessing or covering connector pins in a conductive connector shell and installer training.

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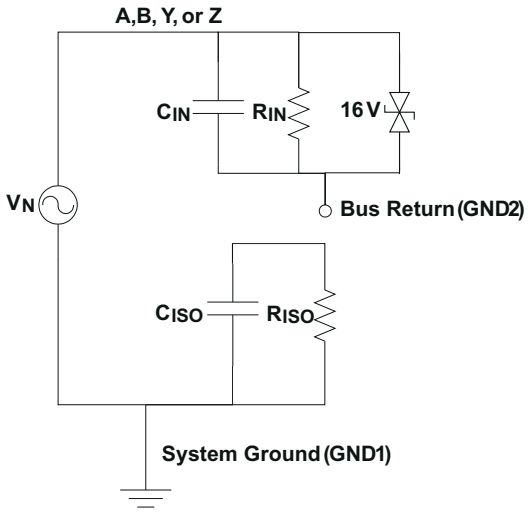


図 9-3. Noise Model

9.2.3 Application Curve

At maximum working voltage, ISO1176T isolation barrier has more than 28 years of life.

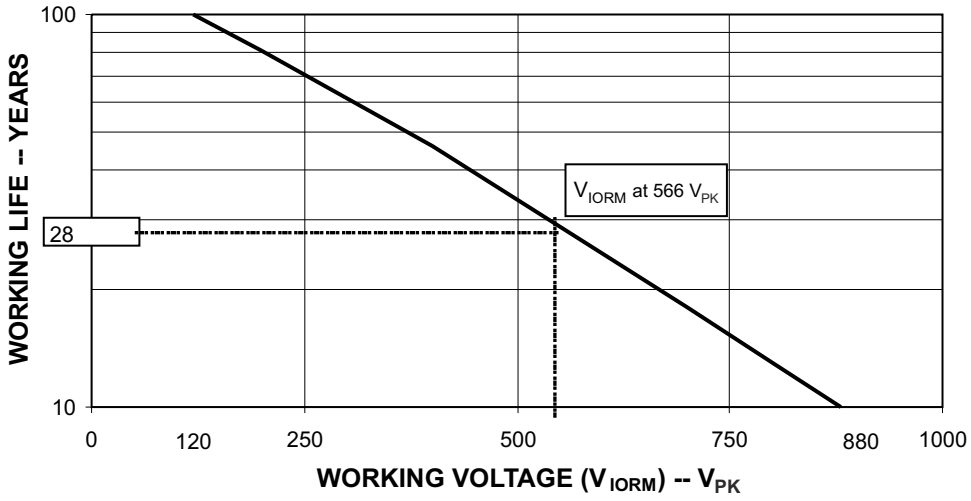


図 9-4. Time-Dependent Dielectric Breakdown Test Results

10 Power Supply Recommendations

To ensure reliable operation at all data rates and supply voltages, TI recommends a 0.1-µF bypass capacitor at input and output supply pins (V_{CC1} and V_{CC2}). The capacitors should be placed as close to the supply pins as possible. This device is used in applications where only a single primary-side power supply is available. Isolated power can be generated for the secondary-side with the help of integrated transformer driver.

11 Layout

11.1 Layout Guidelines

ON-chip IEC-ESD protection is good for laboratory and portable equipment but never sufficient for EFT and surge transients occurring in industrial environments. Therefore, robust and reliable bus node design requires the use of external transient protection devices. Because ESD and EFT transients have a wide frequency bandwidth from approximately 3-MHz to 3-GHz, high-frequency layout techniques must be applied during PCB design. A minimum of four layers is required to accomplish a low EMI PCB design (see 図 11-1).

- Layer stacking should be in the following order (top-to-bottom): high-speed signal layer, ground plane, power plane, and low-frequency signal layer.
- Placing a solid ground plane next to the high-speed signal layer establishes controlled impedance for transmission line interconnects and provides an excellent low-inductance path for the return current flow.
- Placing the power plane next to the ground plane creates additional high-frequency bypass capacitance of approximately 100 pF/in^2.
- Routing the slower speed control signals on the bottom layer allows for greater flexibility as these signal links usually have margin to tolerate discontinuities such as vias.
- Place the protection circuitry close to the bus connector to prevent noise transients from penetrating your board.
- Use V_{CC} and ground planes to provide low-inductance. High-frequency currents might follow the path of least inductance and not necessarily the path of least resistance.
- Design the protection components into the direction of the signal path. Do not force the transient currents to divert from the signal path to reach the protection device.
- Apply 0.1-µF bypass capacitors as close as possible to the V_{CC}-pins of transceiver, UART, and controller ICs on the board.
- Use at least two vias for V_{CC} and ground connections of bypass capacitors and protection devices to minimize effective via-inductance.
- Use 1-kΩ to 10-kΩ pullup and pulldown resistors for enable lines to limit noise currents in these lines during transient events.
- Insert pulse-proof resistors into the A and B bus lines if the TVS clamping voltage is higher than the specified maximum voltage of the transceiver bus pins. These resistors limit the residual clamping current into the transceiver and prevent it from latching up.
- While pure TVS protection is sufficient for surge transients up to 1 kV, higher transients require metal-oxide varistors (MOVs) which reduce the transients to a few hundred volts of clamping voltage, and transient blocking units (TBUs) that limit transient current to less than 1 mA.
- Routing the high-speed traces on the top layer avoids the use of vias (and the introduction of their inductances) and allows for clean interconnects between the isolator and the transmitter and receiver circuits of the data link.

If an additional supply voltage plane or signal layer is needed, add a second power and ground plane system to the stack to keep it symmetrical. This makes the stack mechanically stable and prevents it from warping. Also the power and ground plane of each power system can be placed closer together, thus increasing the high-frequency bypass capacitance significantly.

注

For detailed layout recommendations, see Application Note *Digital Isolator Design Guide*, SLLA284.

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11.2 Layout Example

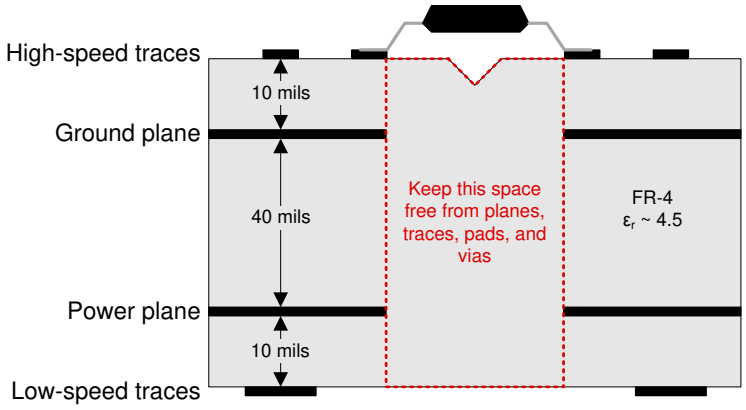


図 11-1. Recommended Layer Stack

12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

For related documentation see the following:

- *Isolated, 40-Mbps, 3.3-V to 5-V Profibus Interface* (SLUU471)
- *Digital Isolator Design Guide* (SLLA284)
- *Isolation Glossary* (SLLA353)

12.2 Community Resources

12.3 Trademarks

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12.5 用語集

テキサス・インスツルメンツ用語集　　この用語集には、用語や略語の一覧および定義が記載されています。

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
ISO1176TDW	Obsolete	Production	SOIC (DW) | 16	-	-	Call TI	Call TI	-40 to 85	ISO1176T
ISO1176TDWR	Active	Production	SOIC (DW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	ISO1176T
ISO1176TDWR.A	Active	Production	SOIC (DW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	ISO1176T
ISO1176TDWRG4	Active	Production	SOIC (DW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	ISO1176T
ISO1176TDWRG4.A	Active	Production	SOIC (DW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	ISO1176T

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

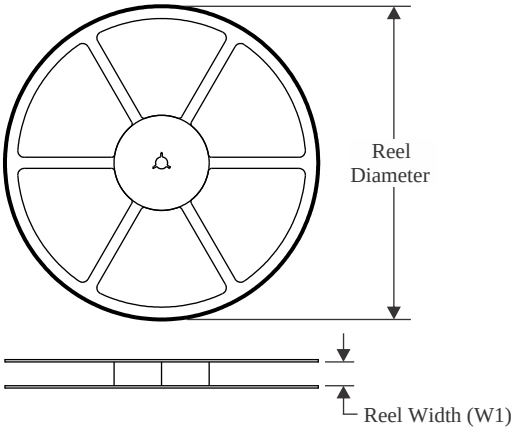
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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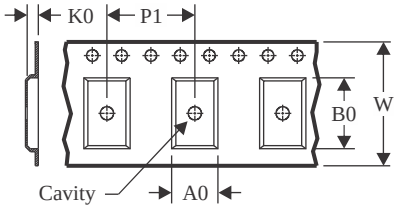
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TAPE AND REEL INFORMATION

REEL DIMENSIONS

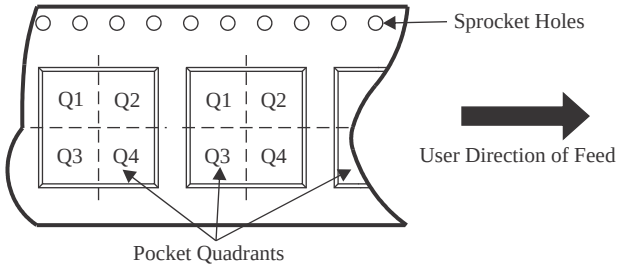


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

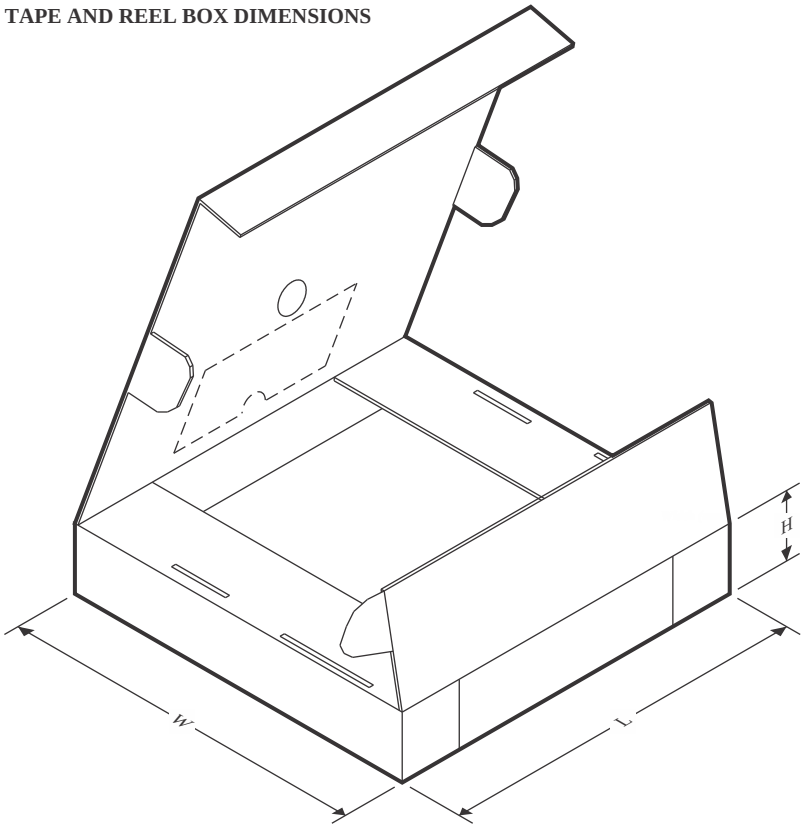
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ISO1176TDWR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
ISO1176TDWRG4	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ISO1176TDWR	SOIC	DW	16	2000	353.0	353.0	32.0
ISO1176TDWRG4	SOIC	DW	16	2000	353.0	353.0	32.0

GENERIC PACKAGE VIEW

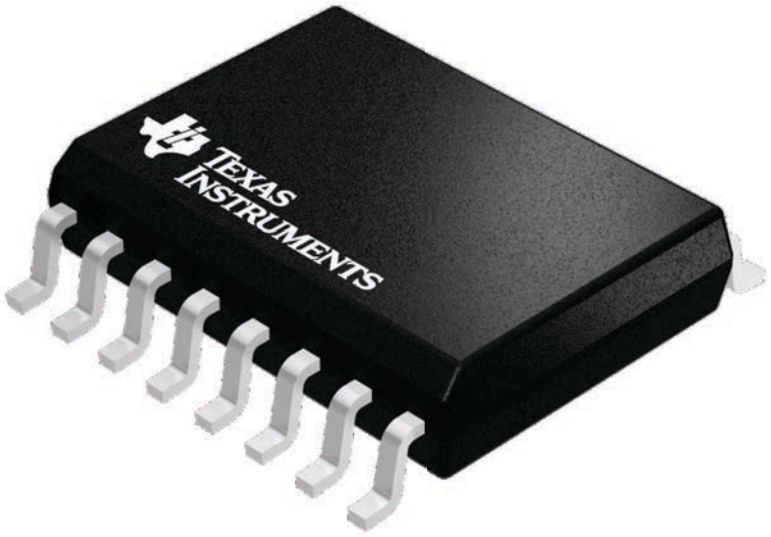
DW 16

SOIC - 2.65 mm max height

7.5 x 10.3, 1.27 mm pitch

SMALL OUTLINE INTEGRATED CIRCUIT

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4224780/A

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