TEXAS INSTRUMENTS
ISO7760-Q1, ISO7761-Q1, ISO7762-Q1, ISO7763-Q1
JAJSGK0E – NOVEMBER 2018 – REVISED JULY 2024

ISO776x-Q1 高速で堅牢な EMC 強化型 6 チャネル デジタル アイソレータ

1 特長

- 車載アプリケーション認定済み
- 以下の結果で AEC-Q100 認定済み:
  - デバイス温度グレード 1:-40℃～+125℃の周囲温度範囲
  - デバイス HBM ESD 分類レベル 3A
  - デバイス CDM ESD 分類レベル C6
- 機能安全対応
  - 機能安全システムの設計に役立つ資料を利用可能:ISO7760-Q1、ISO7761-Q1、ISO7762-Q1、ISO7763-Q1
- 100Mbps のデータ レート
- 堅牢な絶縁バリア:
  - 推定寿命:30 年超
  - 最高 5000V_{RMS} の絶縁定格
  - 最高 12.8kV のサージ耐量
  - CMTI:±100kV/μs (標準値)
- 幅広い電源電圧範囲:2.25V～5.5V
- 2.25V から 5.5V への電圧レベル変換
- デフォルト出力が HIGH (ISO776x) と LOW (ISO776xF) のオプション
- 低い消費電力:1Mbps でチャネルごとに標準値 1.4mA
- 小さい伝搬遅延:11ns (標準値、5V 時)
- 堅牢な電磁環境適合性 (EMC):
  - システム レベルでの ESD、EFT、サージ耐性
  - 絶縁バリアの両側で ±8kV の IEC 61000-4-2 接触放電保護
  - 低い放射
- Wide-SOIC (DW-16) および SSOP (DBQ-16) のパッケージ オプション
- 安全関連認証:
  - DIN EN IEC 60747-17 (VDE 0884-17) に準拠した強化絶縁
  - UL 1577 部品認定プログラム
  - IEC 62368-1 および IEC 60601-1 準拠の CSA 認定
  - GB4943.1 準拠の CQC 認定
  - EN 62368-1 および EN 61010-1 に従った TUV 認定

2 アプリケーション

- ハイブリッド、電気自動車、およびパワー・トレーン・システム (EV/HEV)
  - バッテリ・マネジメント・システム (BMS)
  - オンボード・チャージャ
  - トラクション・インバータ
  - DC/DC コンバータ
  - スタータ / 発電機

3 概要

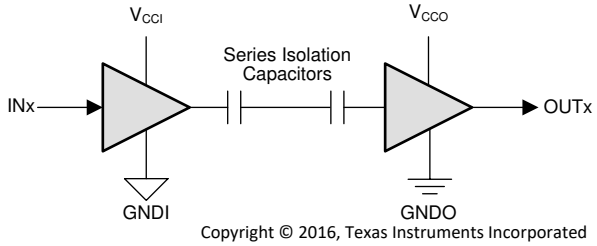
ISO776x-Q1 デバイスは、高性能の 6 チャネル デジタル アイソレータであり、UL 1577 準拠で 5000V_{RMS} (DW パッケージ) および 3000V_{RMS} (DBQ パッケージ) の絶縁定格を備えています。このファミリのデバイスは、VDE、CSA、TUV、CQC についても認定済みです。

ISO776x-Q1 ファミリのデバイスは電磁気耐性が高く、放射が低く、低消費電力を実現し、CMOS または LVCMOS デジタル I/O が絶縁されています。それぞれの絶縁チャネルにはロジック入力およびロジック出力バッファがあり、二重の容量性二酸化ケイ素 (SiO_2) の絶縁バリアによって分離されています。ISO776x-Q1 ファミリのデバイスは、6 つのチャネルすべてが同じ方向、または 1、2、3 チャネルが逆方向で他のチャネルが順方向など、可能なすべてのピン構成で利用可能です。入力電力または入力信号が失われた場合のデフォルト出力は、接尾辞 F のないデバイスでは High、接尾辞 F のあるデバイスでは Low になります。詳細は「デバイスの機能モード」のセクションを参照してください。

パッケージ情報

部品番号	パッケージ(1)	本体サイズ (公称)	パッケージ サイズ (2)
ISO7760-Q1 ISO7761-Q1 ISO7762-Q1 ISO7763-Q1	SOIC (DW、16)	10.30mm × 7.50mm	10.3mm × 10.30mm
	SSOP (DBQ) (16)	4.90mm × 3.90mm	4.90mm × 6.00mm

(1) 詳細については、セクション 13 を参照してください。
(2) パッケージ サイズ (長さ × 幅) は公称値であり、該当する場合はピンも含まれます。



V_{CCI} = 入力 V_{CC}、V_{CCO} = 出力 V_{CC}
GNDI=入力グランド、GNDO=出力グランド

概略回路図

このリソースの元の言語は英語です。翻訳は概要を便宜的に提供するもので、自動化ツール (機械翻訳) を使用していることがあり、TI では翻訳の正確性および妥当性につきましては一切保証いたしません。実際の設計などの前には、ti.com で必ず最新の英語版をご参照くださいますようお願いいたします。

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4 概要 (続き)

絶縁電源と組み合わせて使用することで、このデバイス・ファミリは、データ・バス (たとえば CAN、LIN など) または他の回路からのノイズ電流がローカル・グランドに入り込み、敏感な回路に干渉や損傷を引き起こすことを防ぐのに役立ちます。革新的なチップ設計およびレイアウト技法により、ISO776x-Q1 ファミリのデバイスは電磁環境適合性が大幅に強化されているため、システム・レベルの ESD、EFT、サージ、および放射に関するコンプライアンスを容易に達成できます。ISO776x-Q1 ファミリのデバイスは、16 ピンの SOIC および SSOP パッケージで供給されます。

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5 Pin Configuration and Functions

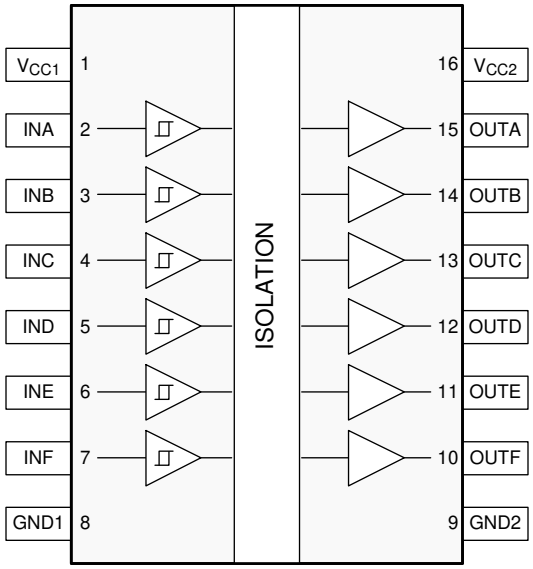


図 5-1. ISO7760-Q1 DW and DBQ Packages 16-Pin SOIC and SSOP Top View

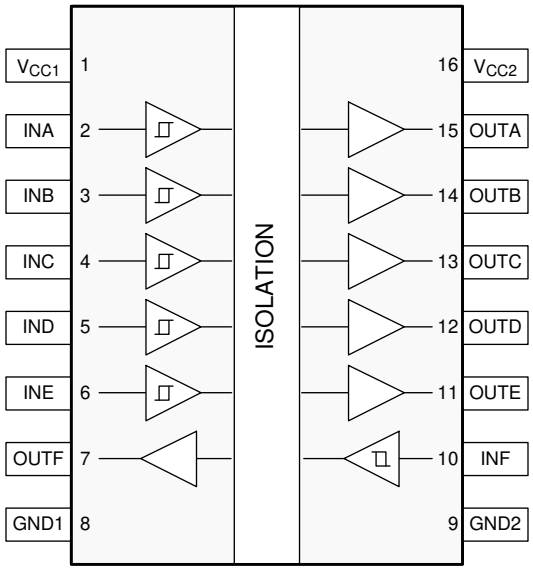


図 5-2. ISO7761-Q1 DW and DBQ Packages 16-Pin SOIC and SSOP Top View

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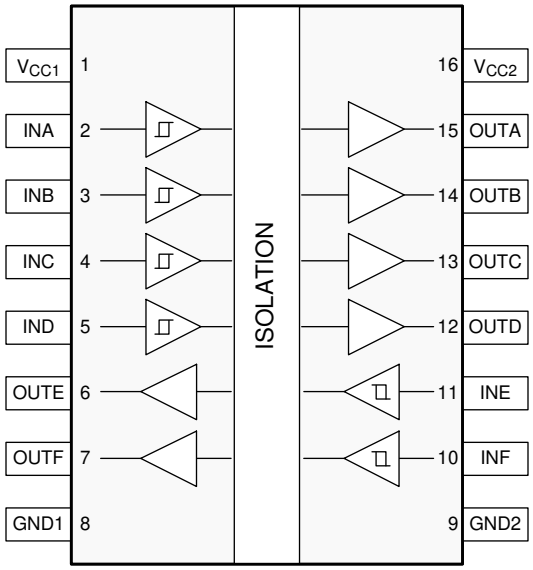


図 5-3. ISO7762-Q1 DW and DBQ Packages 16-Pin SOIC and SSOP Top View

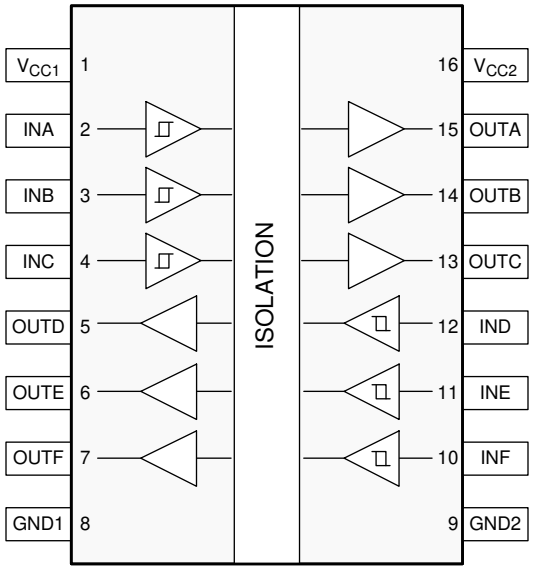


図 5-4. ISO7763-Q1 DW and DBQ Packages 16-Pin SOIC and SSOP Top View

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表 5-1. Pin Functions

PIN					Type	DESCRIPTION
NAME	NO.					
	ISO7760-Q1	ISO7761-Q1	ISO7762-Q1	ISO7763-Q1		
GND1	8	8	8	8	—	Ground connection for V_{CC1}
GND2	9	9	9	9	—	Ground connection for V_{CC2}
INA	2	2	2	2	I	Input, channel A
INB	3	3	3	3	I	Input, channel B
INC	4	4	4	4	I	Input, channel C
IND	5	5	5	12	I	Input, channel D
INE	6	6	11	11	I	Input, channel E
INF	7	10	10	10	I	Input, channel F
OUTA	15	15	15	15	O	Output, channel A
OUTB	14	14	14	14	O	Output, channel B
OUTC	13	13	13	13	O	Output, channel C
OUTD	12	12	12	5	O	Output, channel D
OUTE	11	11	6	6	O	Output, channel E
OUTF	10	7	7	7	O	Output, channel F
V_{CC1}	1	1	1	1	—	Power supply, side 1
V_{CC2}	16	16	16	16	—	Power supply, side 2

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6 Specifications

6.1 Absolute Maximum Ratings

See(1)

		MIN	MAX	UNIT
V_{CC1}, V_{CC2}	Supply voltage (2)	-0.5	6	V
V	Voltage at INx, OUTx	-0.5	V_{CCX} + 0.5 (3)	V
I_o	Output current	-15	15	mA
T_J	Junction temperature		150	°C
T_{stg}	Storage temperature	-65	150	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values except differential I/O bus voltages are with respect to the local ground terminal (GND1 or GND2) and are peak voltage values
(3) Maximum voltage must not exceed 6 V.

6.2 ESD Ratings

(1)

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM),per AEC Q100-002 (1)	±6000	V
		Charged device model (CDM),per AEC Q100-011	±1500	
		Contact discharge per IEC 61000-4-2; Isolation barrier withstand test(2) (3)	±8000	V

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.
(2) IEC ESD strike is applied across the barrier with all pins on each side tied together creating a two-terminal device.
(3) Testing is carried out in air or oil to determine the intrinsic contact discharge capability of the device.

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6.3 Recommended Operating Conditions

			MIN	NOM	MAX	UNIT
V_{CC1}, V_{CC2}	Supply Voltage		2.25		5.5	V
$V_{cc\ (UVLO+)}$	UVLO threshold when supply voltage is rising			2	2.25	V
$V_{cc\ (UVLO-)}$	UVLO threshold when supply voltage is falling		1.7	1.8		V
$V_{HYS\ (UVLO)}$	Supply voltage UVLO hysteresis		100	200		mV
I_{OH}	High level output current	V_{CCO} (1) = 5 V	-4			mA
		V_{CCO} = 3.3 V	-2			
		V_{CCO} = 2.5 V	-1			
I_{OL}	Low level output current	V_{CCO} = 5 V			4	mA
		V_{CCO} = 3.3 V			2	
		V_{CCO} = 2.5 V			1	
V_{IH}	High level Input voltage		0.7 x V_{CCI} (1)		V_{CCI}	V
V_{IL}	Low level Input voltage		0		0.3 x V_{CCI}	V
DR(2)	Data Rate		0		100	Mbps
T_A	Ambient temperature		-55	25	125	°C

(1) V_{CCI} = Input-side V_{CC}; V_{CCO} = Output-side V_{CC}
(2) 100 Mbps is the maximum specified data rate, although higher data rates are possible.

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6.4 Thermal Information

THERMAL METRIC (1)		ISO776x		UNIT
		DW (SOIC)	DBQ (SSOP)	
		16 PINS	16 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	60.3	86.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	24.0	26.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	29.3	36.6	°C/W
ψ_{JT}	Junction-to-top characterization parameter	3.3	1.7	°C/W
ψ_{JB}	Junction-to-board characterization parameter	28.7	36.1	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	n/a	°C/W

(1) For more information about traditional and new thermal metrics, see the no.

6.5 Power Ratings

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ISO7760						
P_D	Maximum power dissipation (both sides)	V_{CC1} = V_{CC2} = 5.5 V, T_J = 150°C, C_L = 15 pF, Input a 50-MHz 50% duty cycle square wave			314	mW
P_{D1}	Maximum power dissipation (side-1)				55	mW
P_{D2}	Maximum power dissipation (side-2)				259	mW
ISO7761						
P_D	Maximum power dissipation (both sides)	V_{CC1} = V_{CC2} = 5.5 V, T_J = 150°C, C_L = 15 pF, Input a 50-MHz 50% duty cycle square wave			314	mW
P_{D1}	Maximum power dissipation (side-1)				88	mW
P_{D2}	Maximum power dissipation (side-2)				226	mW
ISO7762						
P_D	Maximum power dissipation (both sides)	V_{CC1} = V_{CC2} = 5.5 V, T_J = 150°C, C_L = 15 pF, Input a 50-MHz 50% duty cycle square wave			314	mW
P_{D1}	Maximum power dissipation (side-1)				122	mW
P_{D2}	Maximum power dissipation (side-2)				192	mW
ISO7763						
P_D	Maximum power dissipation (both sides)	V_{CC1} = V_{CC2} = 5.5 V, T_J = 150°C, C_L = 15 pF, Input a 50-MHz 50% duty cycle square wave			314	mW
P_{D1}	Maximum power dissipation (side-1)				157	mW
P_{D2}	Maximum power dissipation (side-2)				157	mW

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6.6 Insulation Specifications

PARAMETER		TEST CONDITIONS	VALUE		UNIT
			DW-16	DBQ-16	
CLR	External clearance(1)	Shortest terminal-to-terminal distance through air	>8	>3.7	mm
CPG	External creepage(1)	Shortest terminal-to-terminal distance across the package surface	>8	>3.7	mm
DTI	Distance through the insulation	Minimum internal gap (internal clearance)	>17	>17	µm
CTI	Comparative tracking index	DIN EN 60112 (VDE 0303-11); IEC 60112; UL 746A	>600	>600	V
	Material group	According to IEC 60664-1	I	I	
	Overvoltage category per IEC 60664-1	Rated mains voltage ≤ 150 V_{RMS}	I-IV	I-IV	
		Rated mains voltage ≤ 300 V_{RMS}	I-IV	I-III	
		Rated mains voltage ≤ 600 V_{RMS}	I-IV	n/a	
		Rated mains voltage ≤ 1000 V_{RMS}	I-III	n/a	
DIN EN IEC 60747-17 (VDE 0884-17)(2)					
V_{IORM}	Maximum repetitive peak isolation voltage	AC voltage (bipolar)	2121	566	V_{PK}
V_{IOWM}	Maximum working isolation voltage	AC voltage; Time dependent dielectric breakdown (TDDB) test; See 図 8-7	1500	400	V_{RMS}
		DC voltage	2121	566	V_{DC}
V_{IOTM}	Maximum transient isolation voltage	$V_{TEST} = V_{IOTM}$, t = 60 s (qualification); $V_{TEST} = 1.2 \times V_{IOTM}$, t= 1 s (100% production)	8000	4242	V_{PK}
V_{IMP}	Maximum impulse voltage(3)	Tested in air, 1.2/50-µs waveform per IEC 62368-1	8000	4000	V_{PK}
V_{IOSM}	Maximum surge isolation voltage(4)	$V_{IOSM} \geq 1.3 \times V_{IMP}$; Tested in oil (qualification test), 1.2/50-µs waveform per IEC 62368-1	12800	10000	V_{PK}
q_{pd}	Apparent charge(5)	Method a, After Input-output safety test subgroup 2/3, $V_{ini} = V_{IOTM}$, t_{ini} = 60 s; $V_{pd(m)} = 1.2 \times V_{IORM}$, t_m = 10 s	≤5	≤5	pC
		Method a, After environmental tests subgroup 1, $V_{ini} = V_{IOTM}$, t_{ini} = 60 s; $V_{pd(m)} = 1.6 \times V_{IORM}$, t_m = 10 s	≤5	≤5	
		Method b: At routine test (100% production) and preconditioning (type test); $V_{ini} = 1.2 \times V_{IOTM}$, t_{ini} = 1 s; $V_{pd(m)} = 1.875 \times V_{IORM}$, t_m = 1 s (method b1) or $V_{pd(m)} = V_{ini}$, $t_m = t_{ini}$ (method b2)	≤5	≤5	
C_{IO}	Barrier capacitance, input to output(6)	V_{IO} = 0.4 x sin (2πft), f = 1 MHz	~1.1	~0.9	pF
R_{IO}	Isolation resistance(6)	V_{IO} = 500 V, T_A = 25°C	$>10^{12}$	$>10^{12}$	Ω
		V_{IO} = 500 V, 100°C ≤ T_A ≤ 125°C	$>10^{11}$	$>10^{11}$	
		V_{IO} = 500 V, T_S = 150°C	$>10^{9}$	$>10^{9}$	
	Pollution degree		2	2	
	Climatic category		55/125/21	55/125/21	
UL 1577					
V_{ISO}	Maximum withstanding isolation voltage	$V_{TEST} = V_{ISO}$, t = 60 s (qualification), $V_{TEST} = 1.2 \times V_{ISO}$, t = 1 s (100% production)	5000	3000	V_{RMS}

(1) Creepage and clearance requirements should be applied according to the specific equipment isolation standards of an application. Care should be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed-circuit board do not reduce this distance. Creepage and clearance on a printed-circuit board become equal in certain cases. Techniques such as inserting grooves and/or ribs on a printed-circuit board are used to help increase these specifications.

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(2) This coupler is suitable for *safe electrical insulation* only within the safety ratings. Compliance with the safety ratings shall be ensured by means of suitable protective circuits.
(3) Testing is carried out in air to determine the surge immunity of the package
(4) Testing is carried out in oil to determine the intrinsic surge immunity of the isolation barrier.
(5) Apparent charge is electrical discharge caused by a partial discharge (pd).
(6) All pins on each side of the barrier tied together creating a two-terminal device.

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6.7 Safety-Related Certifications

VDE	CSA	UL	CQC	TUV
Certified according to DIN EN IEC 60747-17 (VDE 0884-17)	Certified according to IEC 62368-1 and IEC 60601-1	Recognized under UL 1577 Component Recognition Program	Certified according to GB 4943.1	Certified according to EN 61010-1 and EN 62368-1
Reinforced Insulation; Maximum transient isolation voltage, 8000 V_{PK} (ISO7760 in DW-16), 7071 V_{PK} (ISO7761, ISO7762, ISO7763 in DW-16) and 4242 V_{PK} (DBQ-16); Maximum repetitive peak isolation voltage, 2121 V_{PK} (DW-16) and 566 V_{PK} (DBQ-16); Maximum surge isolation voltage, 12800 V_{PK} (DW-16) and 10000 V_{PK} (DBQ-16)	Reinforced insulation per CSA 62368-1 and IEC 62368-1 800 V_{RMS} (DW-16) and 370 V_{RMS} (DBQ-16) maximum working voltage (pollution degree 2, material group I); DW-16: 2 MOPP (Means of Patient Protection) per CSA 60601-1 and IEC 60601-1, 250 V_{RMS} maximum working voltage	DW-16: Single protection, 5000 V_{RMS} ; DBQ-16: Single protection, 3000 V_{RMS}	DW-16: Reinforced Insulation, Altitude ≤ 5000 m, Tropical Climate, 700 V_{RMS} maximum working voltage; DBQ-16: Basic Insulation, Altitude ≤ 5000 m, Tropical Climate, 400 V_{RMS} maximum working voltage	5000 V_{RMS} Reinforced insulation per EN 61010-1 up to working voltage of 600 V_{RMS} (DW-16) and 300 V_{RMS} (DBQ-16) 5000 V_{RMS} Reinforced insulation per EN 62368-1 up to working voltage of 600 V_{RMS} (DW-16) and 370 V_{RMS} (DBQ-16)
Certificate number: 40040142	Master contract number: 220991	File number: E181974	Certificate numbers: CQC15001121716 (DW) CQC18001199097 (DBQ)	Client ID number: 77311

6.8 Safety Limiting Values

Safety limiting(1) intends to minimize potential damage to the isolation barrier upon failure of input or output circuitry.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DW-16 PACKAGE						
I_S	Safety input, output, or supply current (1)	$R_{\theta JA}$ = 60.3°C/W, V_I = 5.5 V, T_J = 150°C, T_A = 25°C, see 図 6-1			377	mA
		$R_{\theta JA}$ = 60.3°C/W, V_I = 3.6 V, T_J = 150°C, T_A = 25°C, see 図 6-1			576	
		$R_{\theta JA}$ = 60.3°C/W, V_I = 2.75 V, T_J = 150°C, T_A = 25°C, see 図 6-1			754	
P_S	Safety input, output, or total power (1)	$R_{\theta JA}$ = 60.3°C/W, T_J = 150°C, T_A = 25°C, see 図 6-1			2073	mW
T_S	Maximum safety temperature (1)				150	°C
DBQ-16 PACKAGE						
I_S	Safety input, output, or supply current (1)	$R_{\theta JA}$ = 86.5°C/W, V_I = 5.5 V, T_J = 150°C, T_A = 25°C, see 図 6-2			263	mA
		$R_{\theta JA}$ = 86.5°C/W, V_I = 3.6 V, T_J = 150°C, T_A = 25°C, see 図 6-2			401	
		$R_{\theta JA}$ = 86.5°C/W, V_I = 2.75 V, T_J = 150°C, T_A = 25°C, see 図 6-2			525	
P_S	Safety input, output, or total power (1)	$R_{\theta JA}$ = 86.5°C/W, T_J = 150°C, T_A = 25°C, see 図 6-2			1445	mW
T_S	Maximum safety temperature (1)				150	°C

(1) The maximum safety temperature, T_S, has the same value as the maximum junction temperature, T_J, specified for the device. The I_S and P_S parameters represent the safety current and safety power respectively. The maximum limits of I_S and P_S should not be exceeded. These limits vary with the ambient temperature, T_A.
The junction-to-air thermal resistance, $R_{\theta JA}$, in the table is that of a device installed on a high-K test board for leaded surface-mount packages. Use these equations to calculate the value for each parameter:
$T_J = T_A + R_{\theta JA} \times P$, where P is the power dissipated in the device.
$T_{J(max)} = T_S = T_A + R_{\theta JA} \times P_S$, where $T_{J(max)}$ is the maximum allowed junction temperature.

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$P_S = I_S \times V_I$, where V_I is the maximum input voltage.

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6.9 Electrical Characteristics—5-V Supply

VCC1 = VCC2 = 5 V ± 10% (over recommended operating conditions unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = -4 mA; See 図 7-1	V_{CCO} (1) - 0.4	4.8		V
V_{OL}	Low-level output voltage	I_{OL} = 4 mA; See 図 7-1		0.2	0.4	V
$V_{IT+(IN)}$	Rising input switching threshold			0.6 x V_{CCI}	0.7 x V_{CCI}	V
$V_{IT-(IN)}$	Falling input switching threshold		0.3 x V_{CCI}	0.4 x V_{CCI}		V
$V_{I(HYS)}$	Input threshold voltage hysteresis		0.1 x V_{CCI}	0.2 x V_{CCI}		V
I_{IH}	High-level input current	V_{IH} = V_{CCI} (1) at INx			10	µA
I_{IL}	Low-level input current	V_{IL} = 0 V at INx	-10			µA
CMTI	Common mode transient immunity	V_I = V_{CCI} or 0 V, V_{CM} = 1200 V; See 図 7-3	85	100		kV/µs
C_I	Input Capacitance (2)	V_I = V_{CC}/ 2 + 0.4 × sin(2πft), f = 1 MHz, V_{CC} = 5 V		2		pF

(1) V_{CCI} = Input-side V_{CC}; V_{CCO} = Output-side V_{CC}
(2) Measured from input pin to same side ground.

6.10 Supply Current Characteristics—5-V Supply

V_{CC1} = V_{CC2} = 5 V ±10% (over recommended operating conditions unless otherwise noted).

PARAMETER	TEST CONDITIONS		SUPPLY CURRENT	MIN	TYP	MAX	UNIT
ISO7760-Q1							
Supply current - DC signal	V_I = V_{CC1} (ISO7760-Q1); V_I = 0 V (ISO7760-Q1 with F suffix)		I_{CC1}		1.6	2.9	mA
			I_{CC2}		3	5.3	
	V_I = 0 V (ISO7760-Q1); V_I = V_{CC1} (ISO7760-Q1 with F suffix)		I_{CC1}		8	11.3	
			I_{CC2}		3.3	5.7	
Supply current - AC signal	All channels switching with square wave clock input; C_L = 15 pF	1 Mbps	I_{CC1}		5	6.5	
			I_{CC2}		3.5	5.9	
		10 Mbps	I_{CC1}		5.2	6.7	
			I_{CC2}		6.4	9.7	
		100 Mbps	I_{CC1}		7	9.2	
			I_{CC2}		35	47	
ISO7761-Q1							
Supply current - DC signal	V_I = V_{CCI} (1)(ISO7761-Q1); V_I = 0 V (ISO7761-Q1 with F suffix)		I_{CC1}		1.9	3.5	mA
			I_{CC2}		2.9	5.4	
	V_I = 0 V (ISO7761-Q1); V_I = V_{CCI} (ISO7761-Q1 with F suffix)		I_{CC1}		7.3	10.6	
			I_{CC2}		4.2	6.9	
Supply current - AC signal	All channels switching with square wave clock input; C_L = 15 pF	1 Mbps	I_{CC1}		4.7	6.6	
			I_{CC2}		3.8	6.5	
		10 Mbps	I_{CC1}		5.3	8	
			I_{CC2}		6.3	9.6	
		100 Mbps	I_{CC1}		11.5	15.6	
			I_{CC2}		30.5	40.3	
ISO7762-Q1							

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V_{CC1} = V_{CC2} = 5 V ±10% (over recommended operating conditions unless otherwise noted).

PARAMETER	TEST CONDITIONS		SUPPLY CURRENT	MIN	TYP	MAX	UNIT
Supply current - DC signal	V_I = V_{CCI} (ISO7762-Q1); V_I = 0 V (ISO7762-Q1 with F suffix)		I_{CC1}		2.1	4.1	mA
			I_{CC2}		2.6	4.9	
	V_I = 0 V (ISO7762-Q1); V_I = V_{CCI} (ISO7762-Q1 with F suffix)		I_{CC1}		6.5	9.3	
			I_{CC2}		5	7.6	
Supply current - AC signal	All channels switching with square wave clock input; C_L = 15 pF	1 Mbps	I_{CC1}		4.5	6.7	
			I_{CC2}		4	6.5	
		10 Mbps	I_{CC1}		5.6	8	
			I_{CC2}		6	8.9	
		100 Mbps	I_{CC1}		16.5	21.3	
			I_{CC2}		25.7	34	
ISO7763-Q1							
Supply current - DC signal	V_I = V_{CCI} (ISO7763-Q1); V_I = 0 V (ISO7763-Q1 with F suffix)		I_{CC1}, I_{CC2}		2.4	4.7	mA
	V_I = 0 V (ISO7763-Q1); V_I = V_{CCI} (ISO7763-Q1 with F suffix)		I_{CC1}, I_{CC2}		5.7	8.6	
Supply current - AC signal	All channels switching with square wave clock input; C_L = 15 pF	1 Mbps	I_{CC1}, I_{CC2}		4.2	6.8	
		10 Mbps	I_{CC1}, I_{CC2}		5.8	8.7	
		100 Mbps	I_{CC1}, I_{CC2}		21	28.4	

(1) V_{CCI} = Input-side V_{CC}

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6.11 Electrical Characteristics—3.3-V Supply

V_{CC1} = V_{CC2} = 3.3 V ±10% (over recommended operating conditions unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = -2mA ; See 図 7-1	V_{CCO} (1) - 0.3	3.2		V
V_{OL}	Low-level output voltage	I_{OL} = 2mA ; See 図 7-1		0.1	0.3	V
$V_{IT+(IN)}$	Rising input switching threshold			0.6 x V_{CCI}	0.7 x V_{CCI} (1)	V
$V_{IT-(IN)}$	Falling input switching threshold		0.3 x V_{CCI}	0.4 x V_{CCI}		V
$V_{I(HYS)}$	Input threshold voltage hysteresis		0.1 x V_{CCI}	0.2 x V_{CCI}		V
I_{IH}	High-level input current	V_{IH} = V_{CCI} (1) at INx			10	µA
I_{IL}	Low-level input current	V_{IL} = 0 V at INx	-10			µA
CMTI	Common mode transient immunity	V_I = V_{CC} or 0 V, V_{CM} = 1200 V; See 図 7-3	85	100		kV/us

(1) V_{CCI} = Input-side V_{CC}; V_{CCO} = Output-side V_{CC}

6.12 Supply Current Characteristics—3.3-V Supply

V_{CC1} = V_{CC2} = 3.3 V ±10% (over recommended operating conditions unless otherwise noted).

PARAMETER	TEST CONDITIONS		SUPPLY CURRENT	MIN	TYP	MAX	UNIT
ISO7760-Q1							
Supply current - DC signal	V_I = V_{CC1} (ISO7760-Q1); V_I = 0 V (ISO7760-Q1 with F suffix)		I_{CC1}		1.6	2.9	mA
			I_{CC2}		3	5.3	
	V_I = 0 V (ISO7760-Q1); V_I = V_{CC1} (ISO7760-Q1 with F suffix)		I_{CC1}		8	11.4	
			I_{CC2}		3.3	5.7	
Supply current - AC signal	All channels switching with square wave clock input; C_L = 15 pF	1 Mbps	I_{CC1}		4.9	6.4	
			I_{CC2}		3.4	5.7	
		10 Mbps	I_{CC1}		5	6.6	
			I_{CC2}		5.5	8.5	
		100 Mbps	I_{CC1}		6.3	8.1	
			I_{CC2}		26	35	
ISO7761-Q1							
Supply current - DC signal	V_I = V_{CCI} (1)(ISO7761-Q1); V_I = 0 V (ISO7761-Q1 with F suffix)		I_{CC1}		1.8	3.5	mA
			I_{CC2}		2.9	5.3	
	V_I = 0 V (ISO7761-Q1); V_I = V_{CCI} (ISO7761-Q1 with F suffix)		I_{CC1}		7.2	10.3	
			I_{CC2}		4.2	6.9	
Supply current - AC signal	All channels switching with square wave clock input; C_L = 15 pF	1 Mbps	I_{CC1}		4.6	6.5	
			I_{CC2}		3.7	6.3	
		10 Mbps	I_{CC1}		5.1	7.5	
			I_{CC2}		5.5	8.6	
		100 Mbps	I_{CC1}		9.4	12.7	
			I_{CC2}		22.8	30.5	
ISO7762-Q1							

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V_{CC1} = V_{CC2} = 3.3 V ±10% (over recommended operating conditions unless otherwise noted).

PARAMETER	TEST CONDITIONS		SUPPLY CURRENT	MIN	TYP	MAX	UNIT
Supply current - DC signal	V_I = V_{CCI} (ISO7762-Q1); V_I = 0 V (ISO7762-Q1 with F suffix)		I_{CC1}		2.1	4	mA
			I_{CC2}		2.5	4.8	
	V_I = 0 V (ISO7762-Q1); V_I = V_{CCI} (ISO7762-Q1 with F suffix)		I_{CC1}		6.5	9.4	
			I_{CC2}		5	7.5	
Supply current - AC signal	All channels switching with square wave clock input; C_L = 15 pF	1 Mbps	I_{CC1}		4.4	6.6	
			I_{CC2}		3.9	6.3	
		10 Mbps	I_{CC1}		5.2	7.5	
			I_{CC2}		5.4	8.1	
		100 Mbps	I_{CC1}		12.9	16.9	
			I_{CC2}		19.5	26	
ISO7763-Q1							
Supply current - DC signal	V_I = V_{CCI} (ISO7763-Q1); V_I = 0 V (ISO7763-Q1 with F suffix)		I_{CC1}, I_{CC2}		2.4	4.6	mA
	V_I = 0 V (ISO7763-Q1); V_I = V_{CCI} (ISO7763-Q1 with F suffix)		I_{CC1}, I_{CC2}		5.7	8.4	
Supply current - AC signal	All channels switching with square wave clock input; C_L = 15 pF	1 Mbps	I_{CC1}, I_{CC2}		4.2	6.6	
		10 Mbps	I_{CC1}, I_{CC2}		5.2	8.1	
		100 Mbps	I_{CC1}, I_{CC2}		16	21.9	

(1) V_{CCI} = Input-side V_{CC}

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6.13 Electrical Characteristics—2.5-V Supply

V_{CC1} = V_{CC2} = 2.5 V ±10% (over recommended operating conditions unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = -1mA ; See 図 7-1	V_{CCO} (1) - 0.2	2.45		V
V_{OL}	Low-level output voltage	I_{OL} = 1mA ; See 図 7-1		0.05	0.2	V
$V_{IT+(IN)}$	Rising input switching threshold			0.6 x V_{CCI}	0.7 x V_{CCI} (1)	V
$V_{IT-(IN)}$	Falling input switching threshold		0.3 x V_{CCI}	0.4 x V_{CCI}		V
$V_{I(HYS)}$	Input threshold voltage hysteresis		0.1 x V_{CCI}	0.2 x V_{CCI}		V
I_{IH}	High-level input current	V_{IH} = V_{CCI} (1) at INx			10	µA
I_{IL}	Low-level input current	V_{IL} = 0 V at INx	-10			µA
CMTI	Common mode transient immunity	V_I = V_{CC} or 0 V, V_{CM} = 1200 V; See 図 7-3	85	100		kV/us

(1) V_{CCI} = Input-side V_{CC}; V_{CCO} = Output-side V_{CC}

6.14 Supply Current Characteristics—2.5-V Supply

V_{CC1} = V_{CC2} = 2.5 V ±10% (over recommended operating conditions unless otherwise noted).

PARAMETER	TEST CONDITIONS		SUPPLY CURRENT	MIN	TYP	MAX	UNIT
ISO7760-Q1							
Supply current - DC signal	V_I = V_{CC1} (ISO7760-Q1); V_I = 0 V (ISO7760-Q1 with F suffix)		I_{CC1}		1.6	2.9	mA
			I_{CC2}		3	5.2	
	V_I = 0 V (ISO7760-Q1); V_I = V_{CC1} (ISO7760-Q1 with F suffix)		I_{CC1}		8	11.6	
			I_{CC2}		3.3	5.7	
Supply current - AC signal	All channels switching with square wave clock input; C_L = 15 pF	1 Mbps	I_{CC1}		4.9	6.4	
			I_{CC2}		3.4	5.7	
		10 Mbps	I_{CC1}		5	6.5	
			I_{CC2}		4.9	7.7	
		100 Mbps	I_{CC1}		6	7.7	
			I_{CC2}		20.3	27.9	
ISO7761-Q1							
Supply current - DC signal	V_I = V_{CCI} (1) (ISO7761-Q1); V_I = 0 V (ISO7761-Q1 with F suffix)		I_{CC1}		1.8	3.4	mA
			I_{CC2}		2.9	5.3	
	V_I = 0 V (ISO7761-Q1); V_I = V_{CCI} (ISO7761-Q1 with F suffix)		I_{CC1}		7.2	10.3	
			I_{CC2}		4.2	6.8	
Supply current - AC signal	All channels switching with square wave clock input; C_L = 15 pF	1 Mbps	I_{CC1}		4.6	6.5	
			I_{CC2}		3.7	6.3	
		10 Mbps	I_{CC1}		4.9	7.2	
			I_{CC2}		5	7.9	
		100 Mbps	I_{CC1}		8.3	11.2	
			I_{CC2}		18.1	24.6	
ISO7762-Q1							

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V_{CC1} = V_{CC2} = 2.5 V ±10% (over recommended operating conditions unless otherwise noted).

PARAMETER	TEST CONDITIONS		SUPPLY CURRENT	MIN	TYP	MAX	UNIT
Supply current - DC signal	V_I = V_{CCI} (ISO7762-Q1); V_I = 0 V (ISO7762-Q1 with F suffix)		I_{CC1}		2.1	4	mA
			I_{CC2}		2.6	4.8	
	V_I = 0 V (ISO7762-Q1); V_I = V_{CCI} (ISO7762-Q1 with F suffix)		I_{CC1}		6.5	9.6	
			I_{CC2}		4.9	7.4	
Supply current - AC signal	All channels switching with square wave clock input; C_L = 15 pF	1 Mbps	I_{CC1}		4.4	6.5	
			I_{CC2}		3.9	6.3	
		10 Mbps	I_{CC1}		5	7.2	
			I_{CC2}		5	7.6	
		100 Mbps	I_{CC1}		10.9	14.4	
			I_{CC2}		15.6	21.3	
ISO7763-Q1							
Supply current - DC signal	V_I = V_{CCI} (ISO7763-Q1); V_I = 0 V (ISO7763-Q1 with F suffix)		I_{CC1}, I_{CC2}		2.3	4.6	mA
	V_I = 0 V (ISO7763-Q1); V_I = V_{CCI} (ISO7763-Q1 with F suffix)		I_{CC1}, I_{CC2}		5.7	8.4	
Supply current - AC signal	All channels switching with square wave clock input; C_L = 15 pF	1 Mbps	I_{CC1}, I_{CC2}		4.1	6.6	
		10 Mbps	I_{CC1}, I_{CC2}		4.9	7.6	
		100 Mbps	I_{CC1}, I_{CC2}		13	18.1	

(1) V_{CCI} = Input-side V_{CC}

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6.15 Switching Characteristics—5-V Supply

V_{CC1} = V_{CC2} = 5 V ±10% (over recommended operating conditions unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ISO776x-Q1						
t_{PLH}, t_{PHL}	Propagation delay time	See 図 7-1	6	11	17	ns
PWD	Pulse width distortion(1) $\lvert t_{PHL} - t_{PLH} \rvert$	See 図 7-1		0.4	5.9	ns
$t_{sk(o)}$	Channel-to-channel output skew time(2)	Same-direction channels			4	ns
$t_{sk(pp)}$	Part-to-part skew time(3)				4.5	ns
t_r	Output signal rise time	See 図 7-1		1.1	3.9	ns
t_f	Output signal fall time	See 図 7-1		1.4	3.9	ns
t_{DO}	Default output delay time from input power loss	Measured from the time V_{CC} goes below 1.7V. See 図 7-2		0.2	0.3	µs
t_{ie}	Time interval error	2^{16} – 1 PRBS data at 100 Mbps		1.3		ns

(1) Also known as pulse skew.
(2) $t_{sk(o)}$ is the skew between outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical loads.
(3) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any terminals of different devices switching in the same direction while operating at identical supply voltages, temperature, input signals and loads.

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6.16 Switching Characteristics—3.3-V Supply

V_{CC1} = V_{CC2} = 3.3 V ±10% (over recommended operating conditions unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ISO776x-Q1						
t_{PLH}, t_{PHL}	Propagation delay time	See 図 7-1	6	12	18.5	ns
PWD	Pulse width distortion(1) $\lvert t_{PHL} - t_{PLH} \rvert$			0.5	5.9	ns
$t_{sk(o)}$	Channel-to-channel output skew time(2)	Same-direction channels			4.4	ns
$t_{sk(pp)}$	Part-to-part skew time(3)				5	ns
t_r	Output signal rise time	See 図 7-1		1	3	ns
t_f	Output signal fall time			1	3	ns
t_{DO}	Default output delay time from input power loss	Measured from the time V_{CC} goes below 1.7V. See 図 7-2		0.2	0.3	µs
t_{ie}	Time interval error	2^{16} – 1 PRBS data at 100 Mbps		1.3		ns

(1) Also known as pulse skew.
(2) $t_{sk(o)}$ is the skew between outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical loads.
(3) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any terminals of different devices switching in the same direction while operating at identical supply voltages, temperature, input signals and loads.

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6.17 Switching Characteristics—2.5-V Supply

V_{CC1} = V_{CC2} = 2.5 V ±10% (over recommended operating conditions unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ISO776x-Q1						
t_{PLH}, t_{PHL}	Propagation delay time	See 図 7-1	7.5	13	21	ns
PWD	Pulse width distortion(1) $\lvert t_{PHL} - t_{PLH} \rvert$	See 図 7-1		0.6	5.9	ns
$t_{sk(o)}$	Channel-to-channel output skew time(2)	Same-direction channels			4.4	ns
$t_{sk(pp)}$	Part-to-part skew time(3)				5.3	ns
t_r	Output signal rise time	See 図 7-1		1	3.5	ns
t_f	Output signal fall time	See 図 7-1		1	3.5	ns
t_{DO}	Default output delay time from input power loss	Measured from the time V_{CC} goes below 1.7V. See 図 7-2		0.1	0.3	µs
t_{ie}	Time interval error	2^{16} – 1 PRBS data at 100 Mbps		1.3		ns

(1) Also known as pulse skew.
(2) $t_{sk(o)}$ is the skew between outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical loads.
(3) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any terminals of different devices switching in the same direction while operating at identical supply voltages, temperature, input signals and loads.

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6.18 Insulation Characteristics Curves

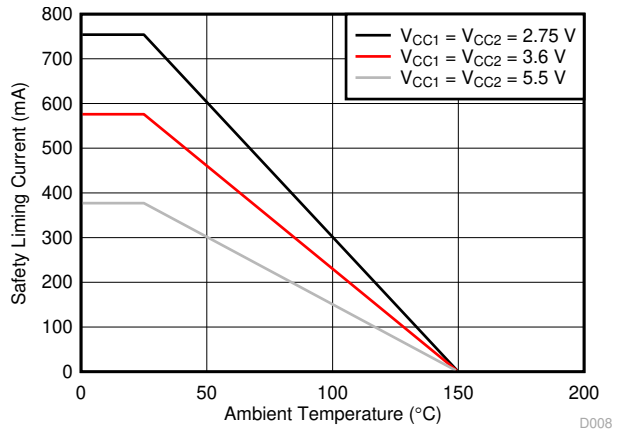


図 6-1. Thermal Derating Curve for Limiting Current per VDE for DW-16 Package

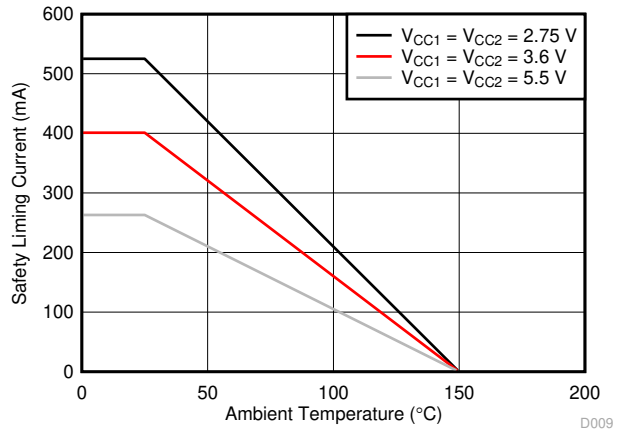


図 6-2. Thermal Derating Curve for Limiting Current per VDE for DBQ-16 Package

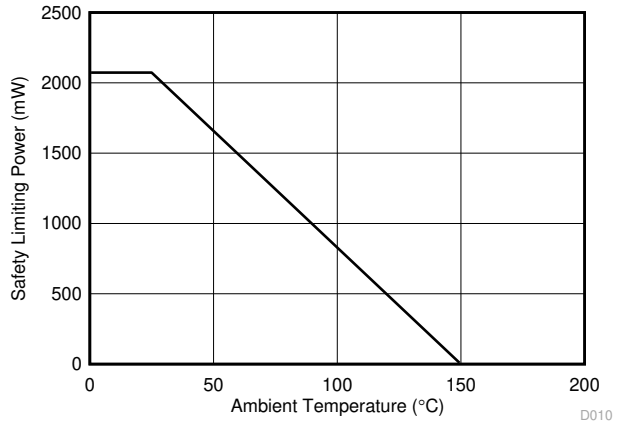


図 6-3. Thermal Derating Curve for Limiting Power per VDE for DW-16 Package

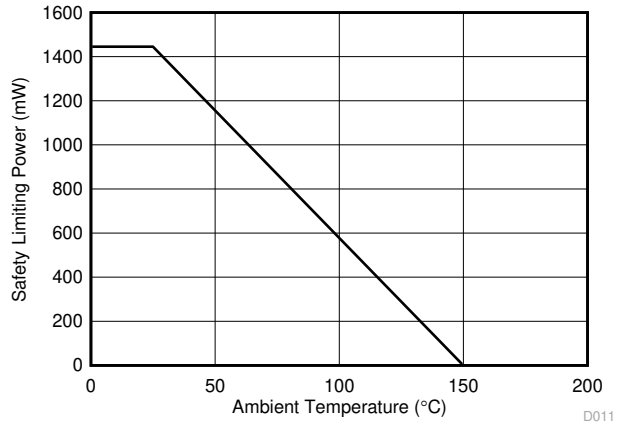
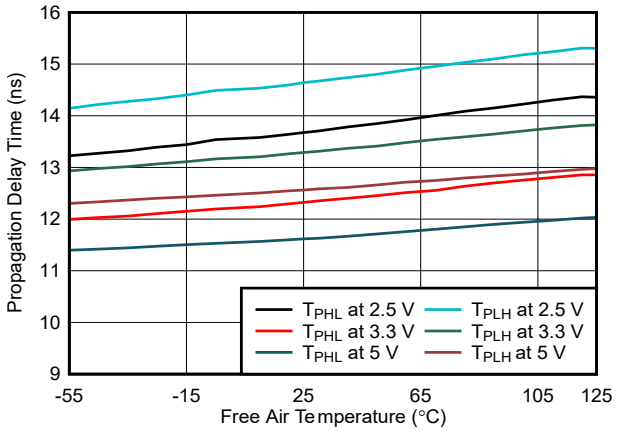


図 6-4. Thermal Derating Curve for Limiting Power per VDE for DBQ-16 Package

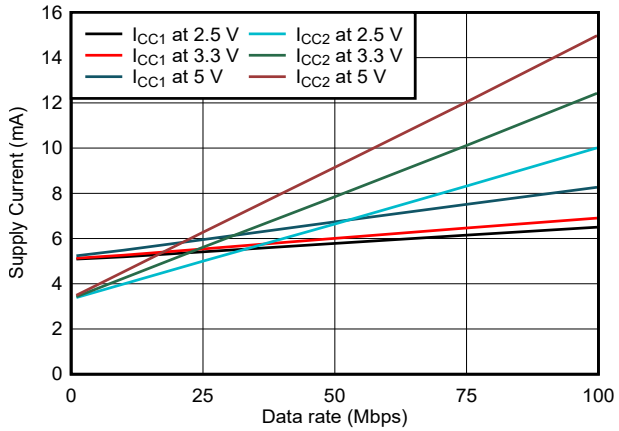
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6.19 Typical Characteristics



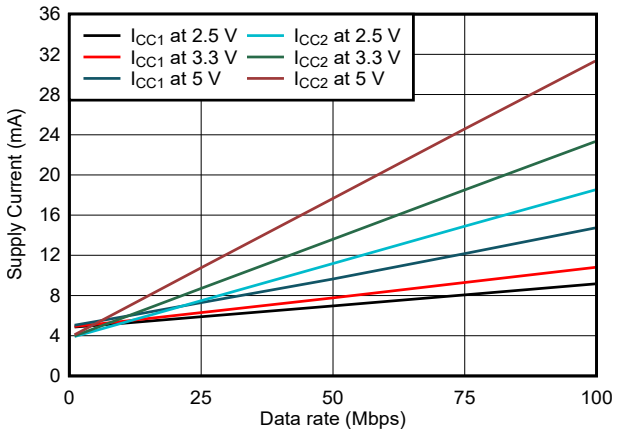
T_A = 25°C C_L = 15 pF

図 6-5. ISO7760-Q1 Supply Current vs Data Rate (With 15-pF Load)



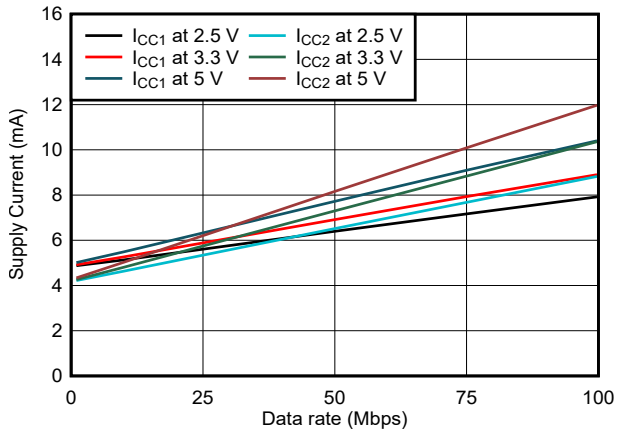
T_A = 25°C C_L = No Load

図 6-6. ISO7760-Q1 Supply Current vs Data Rate (With No Load)



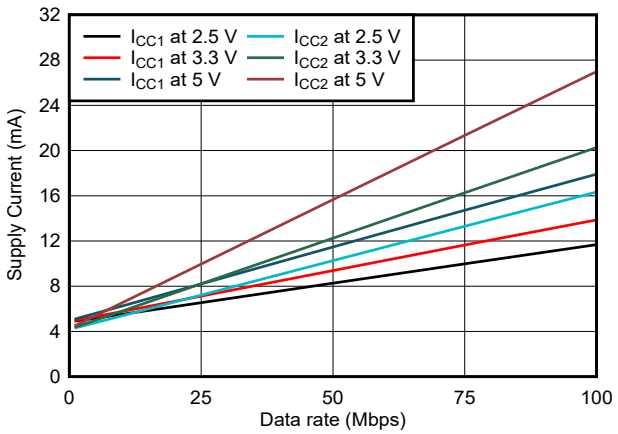
T_A = 25°C C_L = 15 pF

図 6-7. ISO7761-Q1 Supply Current vs Data Rate (With 15-pF Load)



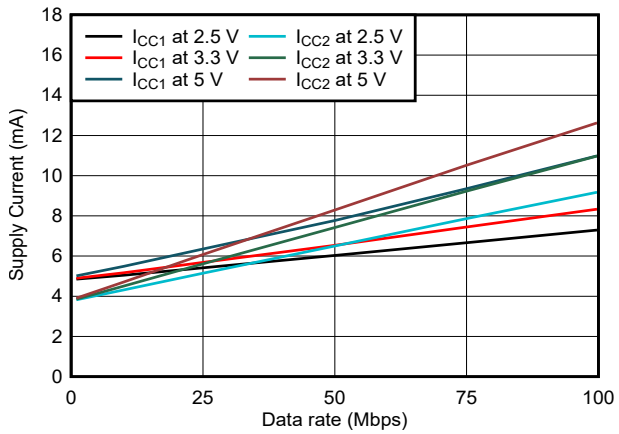
T_A = 25°C C_L = No Load

図 6-8. ISO7761-Q1 Supply Current vs Data Rate (With No Load)



T_A = 25°C C_L = 15 pF

図 6-9. ISO7762-Q1 Supply Current vs Data Rate (With 15-pF Load)



T_A = 25°C C_L = No Load

図 6-10. ISO7762-Q1 Supply Current vs Data Rate (With No Load)

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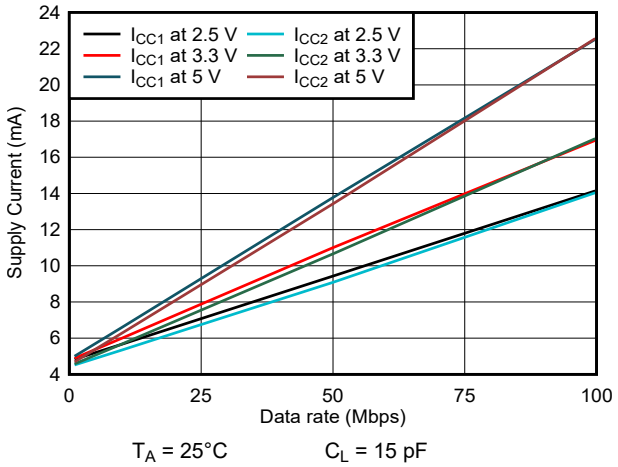


図 6-11. ISO7763-Q1 Supply Current vs Data Rate (With 15-pF Load)

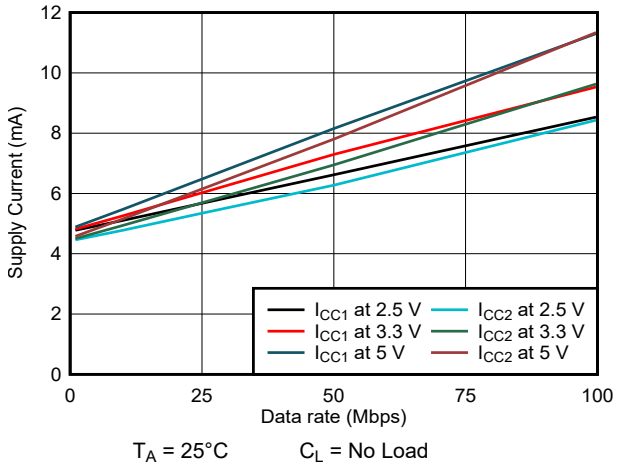


図 6-12. ISO7763-Q1 Supply Current vs Data Rate (With No Load)

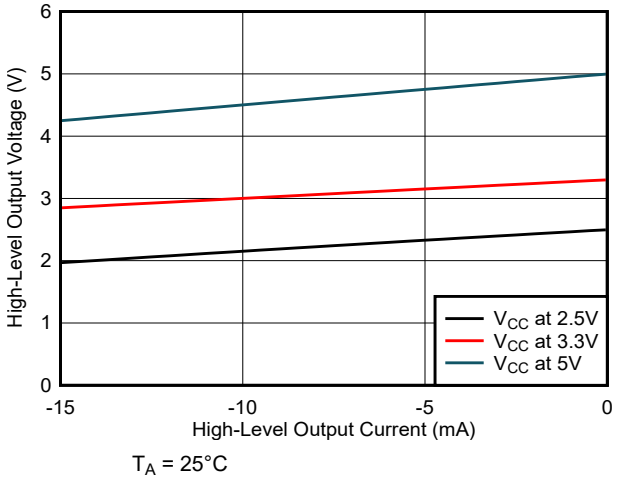


図 6-13. High-Level Output Voltage vs High-Level Output Current

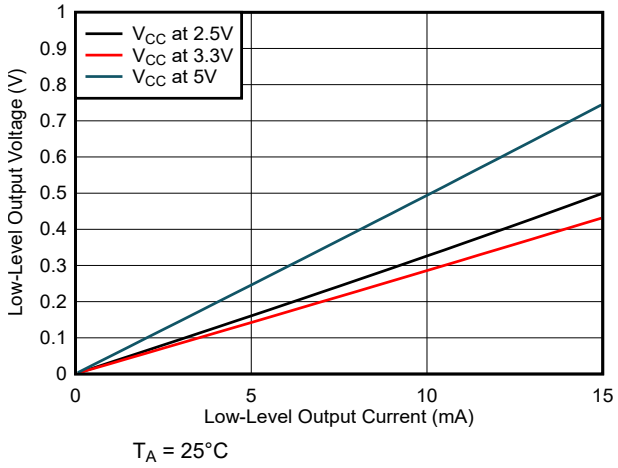


図 6-14. Low-Level Output Voltage vs Low-Level Output Current

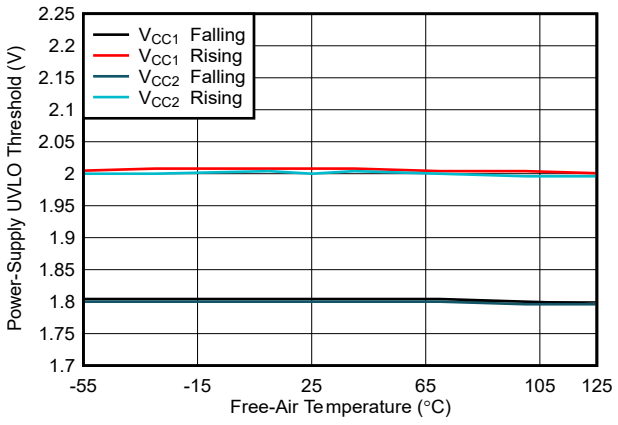


図 6-15. Power Supply Undervoltage Threshold vs Free-Air Temperature

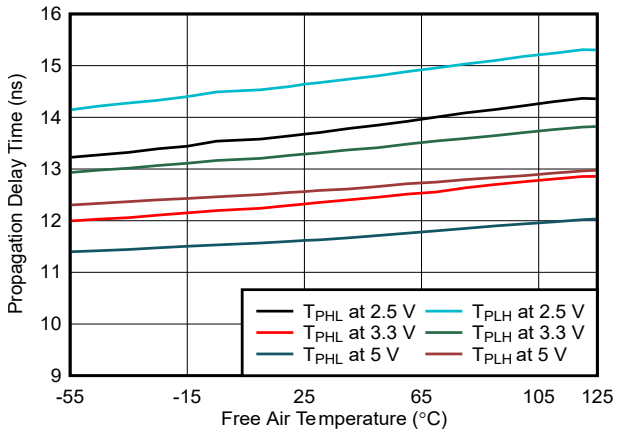
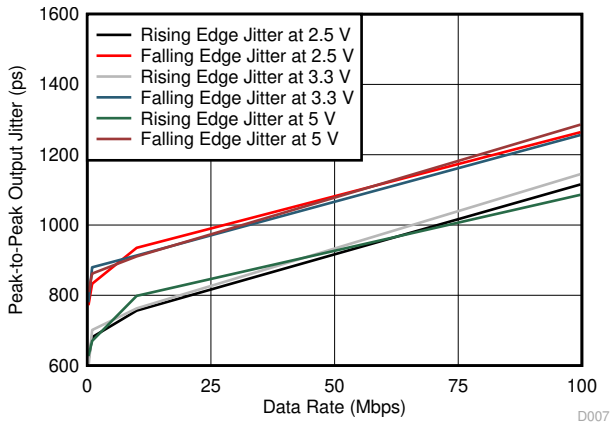


図 6-16. Propagation Delay Time vs Free-Air Temperature

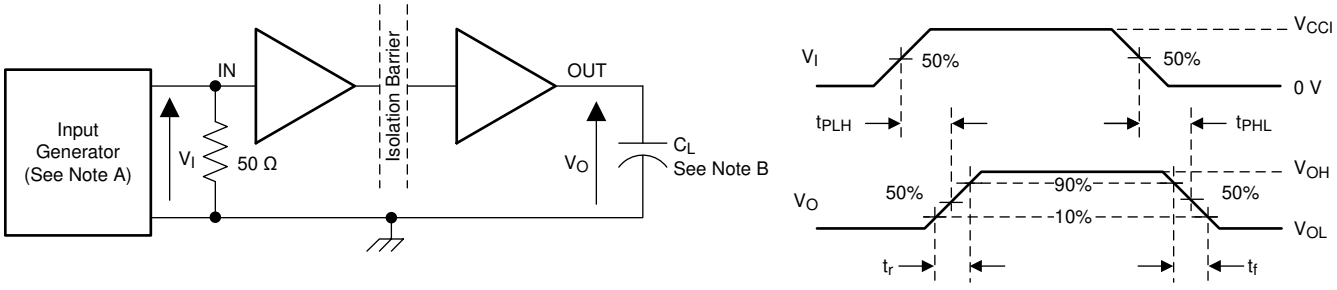
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T_A = 25°C

図 6-17. Peak-to-Peak Output Jitter vs Data Rate

Parameter Measurement Information

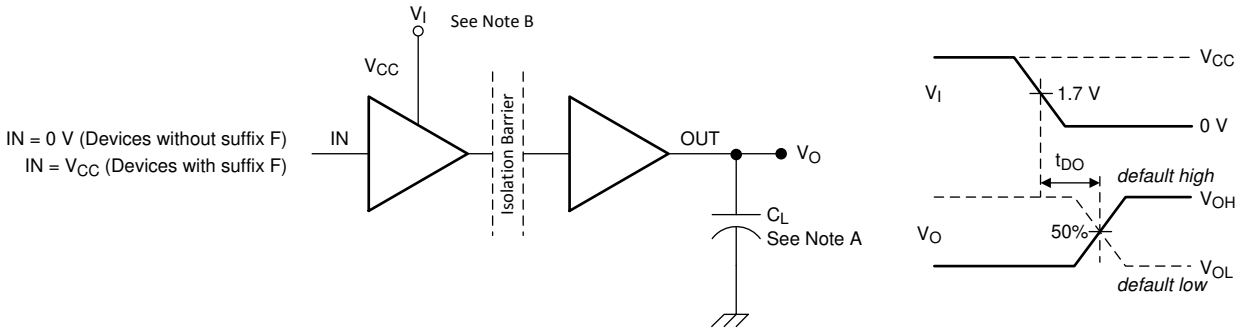


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A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 50 kHz, 50% duty cycle, t_r ≤ 3 ns, t_f ≤ 3 ns, Z_O = 50 Ω. At the input, a 50-Ω resistor is required to terminate Input Generator signal. It is not needed in actual application.

B. C_L = 15 pF and includes instrumentation and fixture capacitance within ±20%.

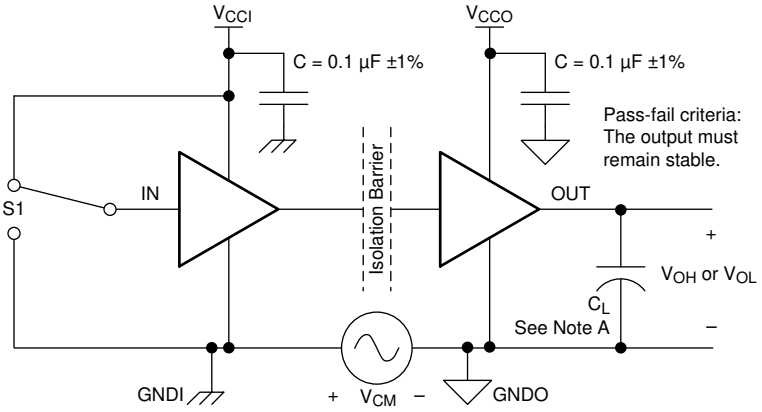
図 7-1. Switching Characteristics Test Circuit and Voltage Waveforms



A. C_L = 15 pF and includes instrumentation and fixture capacitance within ±20%.

B. Power-supply ramp rate = 10 mV/ns

図 7-2. Default Output Delay Time Test Circuit and Voltage Waveforms



A. C_L = 15 pF and includes instrumentation and fixture capacitance within ±20%.

図 7-3. Common-Mode Transient Immunity Test Circuit

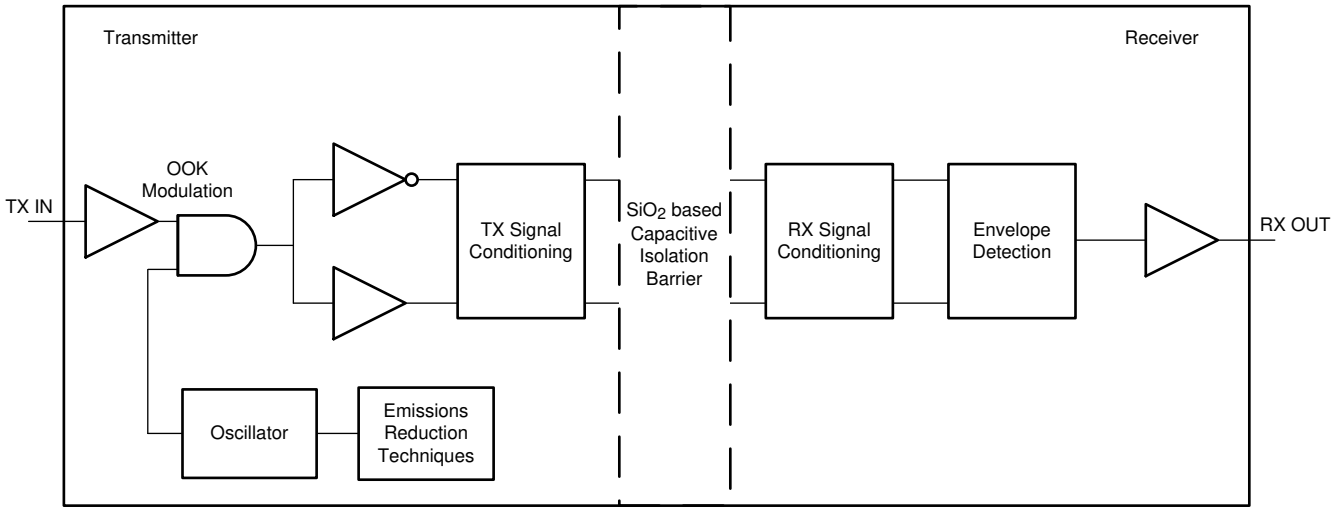
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7 Detailed Description

7.1 Overview

The ISO776x-Q1 family of devices uses an ON-OFF keying (OOK) modulation scheme to transmit the digital data across a silicon-dioxide based isolation barrier. The transmitter sends a high-frequency carrier across the barrier to represent one digital state and sends no signal to represent the other digital state. The receiver demodulates the signal after advanced signal conditioning and produces the output through a buffer stage. The ISO776x-Q1 family of devices also incorporates advanced circuit techniques to maximize the CMTI performance and minimize the radiated emissions because of the high-frequency carrier and IO buffer switching. The conceptual block diagram of a digital capacitive isolator, 図 7-1, shows a functional block diagram of a typical channel. 図 7-2 shows a conceptual detail of how the ON-OFF keying scheme works.

7.2 Functional Block Diagram



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図 7-1. Conceptual Block Diagram of a Digital Capacitive Isolator

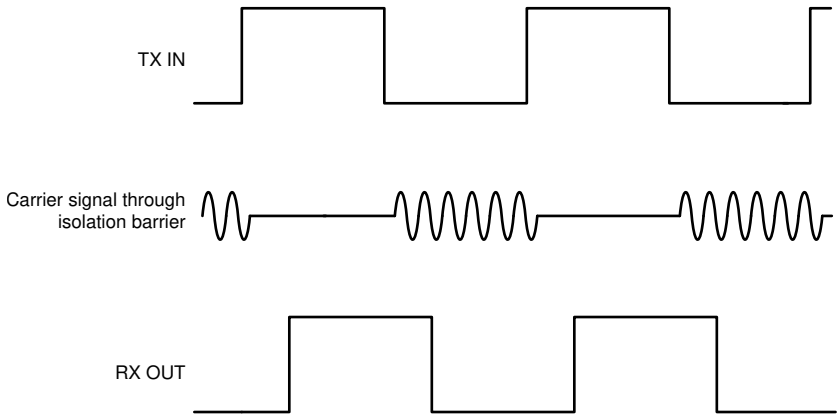


図 7-2. ON-OFF Keying (OOK) Based Modulation Scheme

7.3 Feature Description

表 7-1 lists the device features.

表 7-1. Device Features

PART NUMBER	CHANNEL DIRECTION	MAXIMUM DATA RATE	DEFAULT OUTPUT	PACKAGE	RATED ISOLATION(1)
ISO7760-Q1	6 Forward, 0 Reverse	100 Mbps	High	DW-16	5000 V_{RMS} / 8000 V_{PK}
				DBQ-16	3000 V_{RMS} / 4242 V_{PK}
ISO7760-Q1 with F suffix	6 Forward, 0 Reverse	100 Mbps	Low	DW-16	5000 V_{RMS} / 8000 V_{PK}
				DBQ-16	3000 V_{RMS} / 4242 V_{PK}
ISO7761-Q1	5 Forward, 1 Reverse	100 Mbps	High	DW-16	5000 V_{RMS} / 8000V_{PK}
				DBQ-16	3000 V_{RMS} / 4242 V_{PK}
ISO7761-Q1 with F suffix	5 Forward, 1 Reverse	100 Mbps	Low	DW-16	5000 V_{RMS} / 8000 V_{PK}
				DBQ-16	3000 V_{RMS} / 4242 V_{PK}
ISO7762-Q1	4 Forward, 2 Reverse	100 Mbps	High	DW-16	5000 V_{RMS} / 8000V_{PK}
				DBQ-16	3000 V_{RMS} / 4242 V_{PK}
ISO7762-Q1 with F suffix	4 Forward, 2 Reverse	100 Mbps	Low	DW-16	5000 V_{RMS} / 8000V_{PK}
				DBQ-16	3000 V_{RMS} / 4242 V_{PK}
ISO7763-Q1	3 Forward, 3 Reverse	100 Mbps	High	DW-16	5000 V_{RMS} / 8000V_{PK}
				DBQ-16	3000 V_{RMS} / 4242 V_{PK}
ISO7763-Q1 with F suffix	3 Forward, 3 Reverse	100 Mbps	Low	DW-16	5000 V_{RMS} / 8000 V_{PK}
				DBQ-16	3000 V_{RMS} / 4242 V_{PK}

(1) See *セクション 6.7* for detailed isolation ratings.

7.3.1 Electromagnetic Compatibility (EMC) Considerations

Many applications in harsh industrial environment are sensitive to disturbances such as electrostatic discharge (ESD), electrical fast transient (EFT), surge and electromagnetic emissions. These electromagnetic disturbances are regulated by international standards such as IEC 61000-4-x and CISPR 22. Although system-level performance and reliability depends, to a large extent, on the application board design and layout, the ISO776x-Q1 family of devices incorporates many chip-level design improvements for overall system robustness. Some of these improvements include:

- Robust ESD protection for input and output signal pins and inter-chip bond pads.
- Low-resistance connectivity of ESD cells to supply and ground pins.
- Enhanced performance of high voltage isolation capacitor for better tolerance of ESD, EFT and surge events.
- Bigger on-chip decoupling capacitors to bypass undesirable high energy signals through a low impedance path.
- PMOS and NMOS devices isolated from each other by using guard rings to avoid triggering of parasitic SCRs.
- Reduced common mode currents across the isolation barrier by ensuring purely differential internal operation.

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7.4 Device Functional Modes

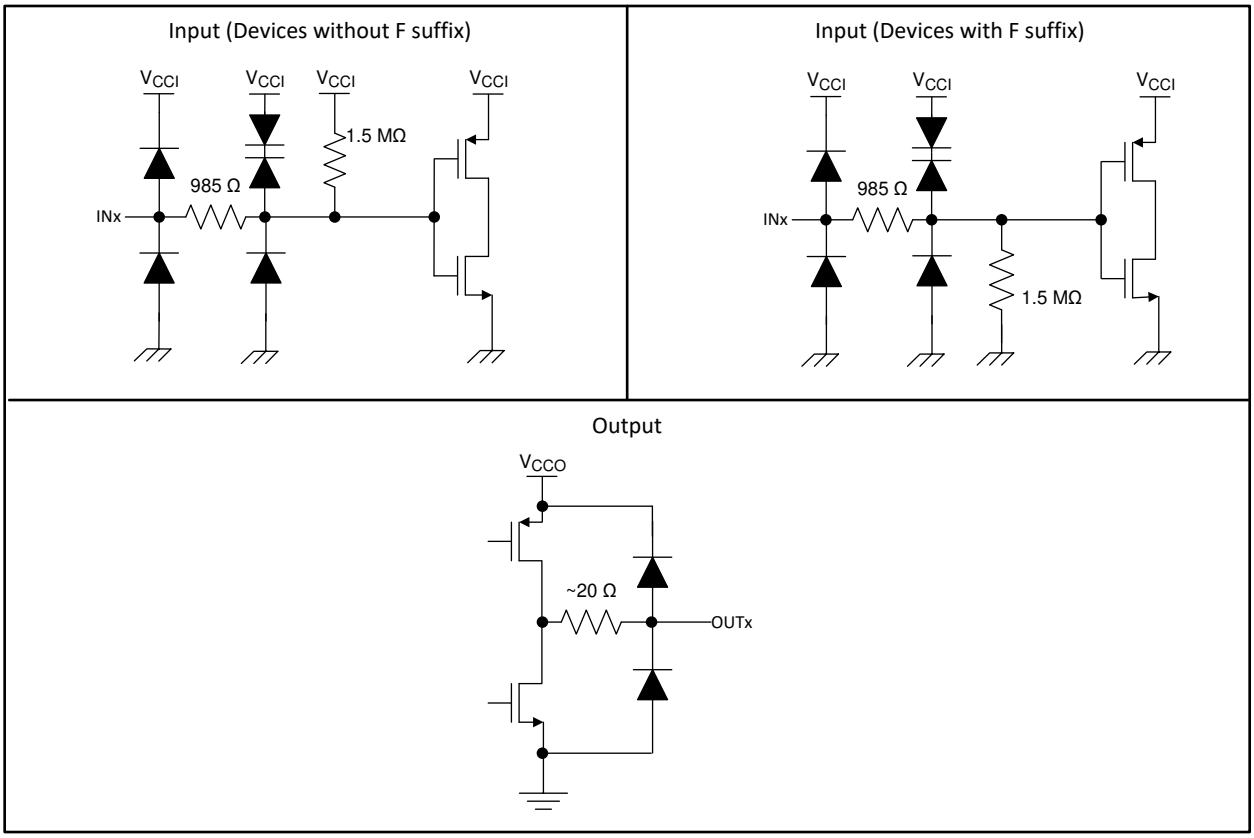
表 7-2 lists the functional modes for the ISO776x-Q1.

表 7-2. Function Table

V_{CCI} (1)	V_{CCO}	INPUT (INx)(3)	OUTPUT (OUTx)	COMMENTS
PU	PU	H	H	Normal Operation: A channel output assumes the logic state of the input.
		L	L	
		Open	Default	Default mode: When INx is open, the corresponding channel output goes to its default logic state. Default is *High* for ISO776x-Q1 and *Low* for ISO776x-Q1 with F suffix.
PD	PU	X	Default	Default mode: When V_{CCI} is unpowered, a channel output assumes the logic state based on the selected default option. Default is *High* for ISO776x-Q1 and *Low* for ISO776x-Q1 with F suffix. When V_{CCI} transitions from unpowered to powered-up, a channel output assumes the logic state of its input. When V_{CCI} transitions from powered-up to unpowered, channel output assumes the selected default state.
X	PD	X	Undetermined	When V_{CCO} is unpowered, a channel output is undetermined (2). When V_{CCO} transitions from unpowered to powered-up, a channel output assumes the logic state of the input

(1) V_{CCI} = Input-side V_{CC}; V_{CCO} = Output-side V_{CC}; PU = Powered up (V_{CC} ≥ 2.25 V); PD = Powered down (V_{CC} ≤ 1.7 V); X = Irrelevant; H = High level; L = Low level
(2) The outputs are in undetermined state when 1.7 V < V_{CCI}, V_{CCO} < 2.25 V.
(3) A strongly driven input signal can weakly power the floating V_{CC} via an internal protection diode and cause undetermined output.

7.4.1 Device I/O Schematics



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図 7-3. Device I/O Schematics

8 Application and Implementation

注

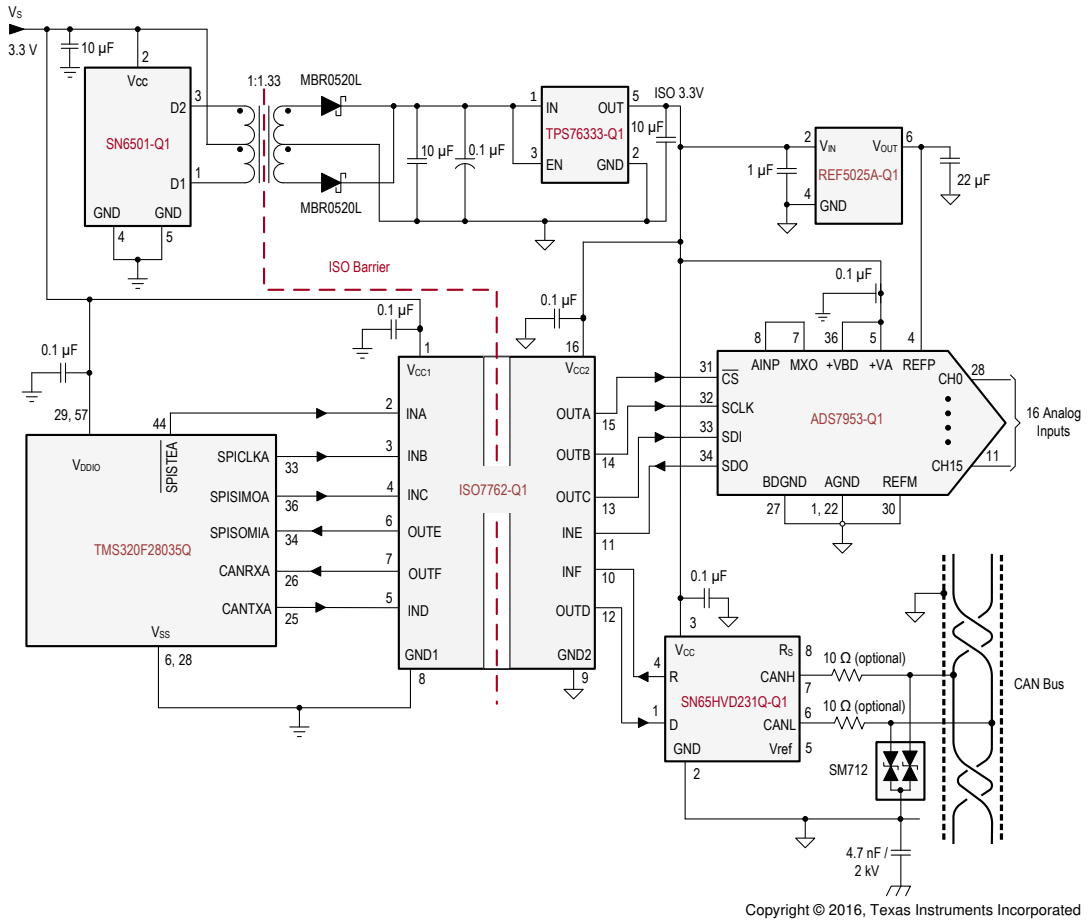
Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The ISO776x-Q1 family of devices is a high-performance, six-channel digital isolators. The ISO776x-Q1 family of devices uses single-ended CMOS-logic switching technology. The voltage range is from 2.25 V to 5.5 V for both supplies, V_{CC1} and V_{CC2}. When designing with digital isolators, keep in mind that because of the single-ended design structure, digital isolators do not conform to any specific interface standard and are only intended for isolating single-ended CMOS or TTL digital signal lines. The isolator is typically placed between the data controller (that is, µC or UART), and a data converter or a line transceiver, regardless of the interface type or standard.

8.2 Typical Application

図 8-1 shows the isolated serial-peripheral interface (SPI) and controller-area network (CAN) interface implementation.



Multiple pins and discrete components omitted for clarity purpose.

図 8-1. Isolated SPI and CAN Interface

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8.2.1 Design Requirements

For this design example, use the parameters listed in 表 8-1.

表 8-1. Design Parameters

PARAMETER	VALUE
Supply voltage, V_{CC1} and V_{CC2}	2.25 to 5.5 V
Decoupling capacitor between V_{CC1} and GND1	0.1 µF
Decoupling capacitor from V_{CC2} and GND2	0.1 µF

8.2.2 Detailed Design Procedure

Unlike optocouplers, which require external components to improve performance, provide bias, or limit current, the ISO776x-Q1 family of devices only requires two external bypass capacitors to operate.

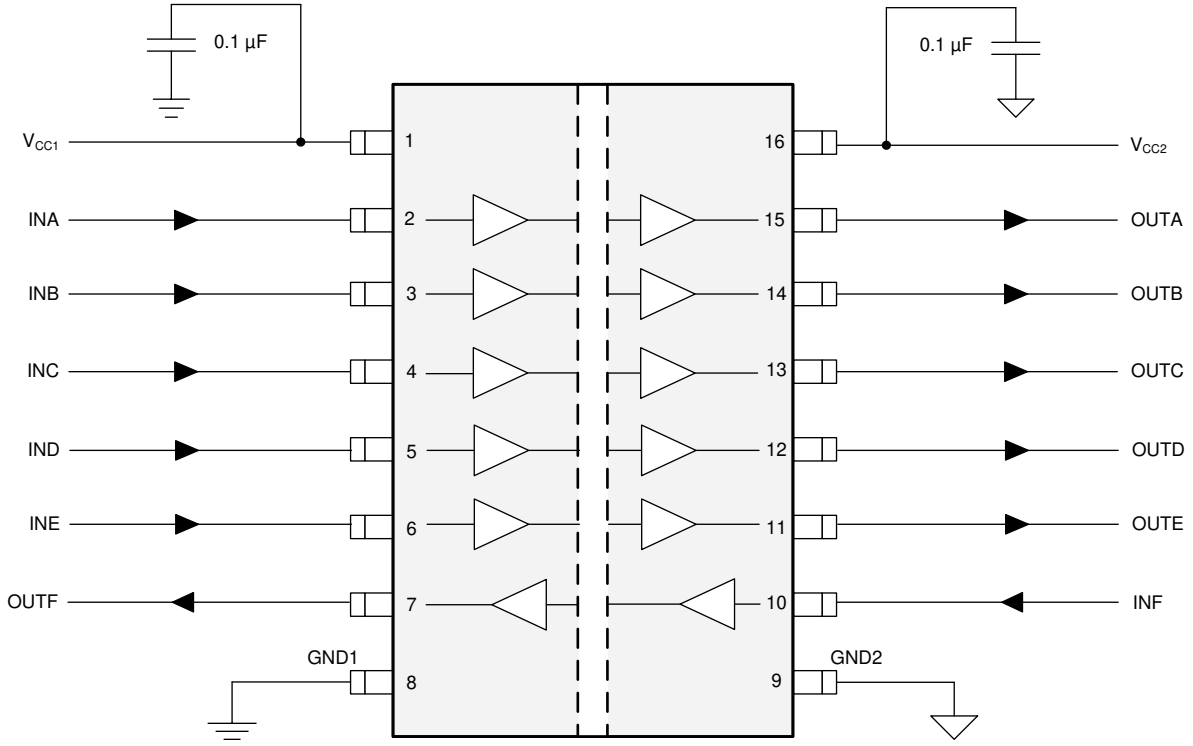


図 8-2. Typical ISO7761-Q1 Circuit Hook-up

8.2.3 Application Curves

The typical eye diagram of the ISO776x-Q1 family of devices indicates low jitter and a wide open eye at the maximum data rate of 100 Mbps.

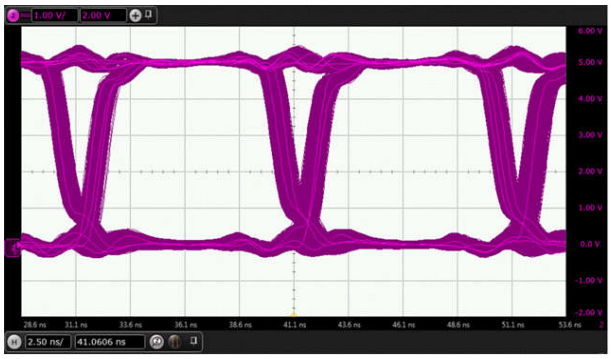


図 8-3. Eye Diagram at 100 Mbps PRBS 2^{16} – 1 Data, 5 V and 25°C

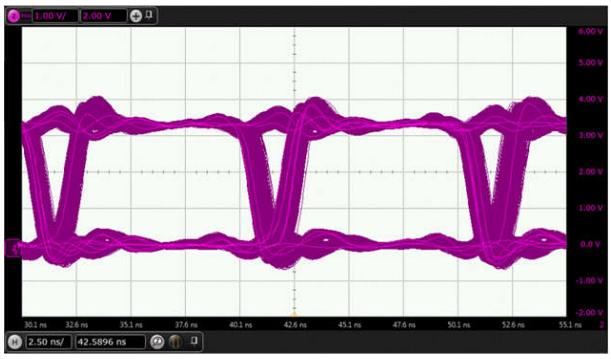


図 8-4. Eye Diagram at 100 Mbps PRBS 2^{16} – 1 Data, 3.3 V and 25°C

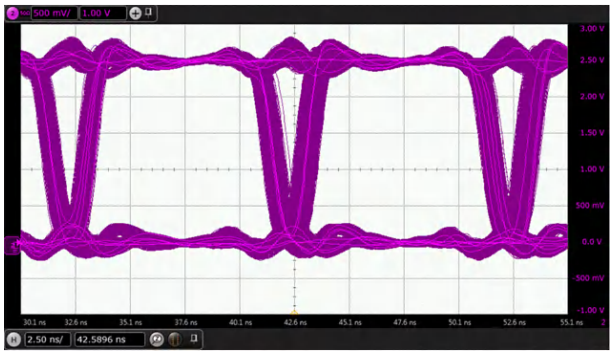


図 8-5. Eye Diagram at 100 Mbps PRBS 2^{16} – 1 Data, 2.5 V and 25°C

8.2.3.1 *Insulation Lifetime*

Insulation lifetime projection data is collected by using industry-standard Time Dependent Dielectric Breakdown (TDDB) test method. In this test, all pins on each side of the barrier are tied together creating a two-terminal device and high voltage applied between the two sides; See 図 8-6 for TDDB test setup. The insulation breakdown data is collected at various high voltages switching at 60 Hz over temperature. For reinforced insulation, VDE standard requires the use of TDDB projection line with failure rate of less than 1 part per million (ppm). Even though the expected minimum insulation lifetime is 20 years at the specified working isolation voltage, VDE reinforced certification requires additional safety margin of 20% for working voltage and 50% for lifetime which translates into minimum required insulation lifetime of 30 years at a working voltage that's 20% higher than the specified value.

図 8-7 shows the intrinsic capability of the isolation barrier to withstand high voltage stress over its lifetime. Based on the TDDB data, the intrinsic capability of the insulation is 1500 V_{RMS} with a lifetime of 36 years. Other factors, such as package size, pollution degree, material group, etc. can further limit the working voltage of the component. The working voltage of DW-16 package is specified upto 1500 V_{RMS} and DBQ-16 package up to 400 V_{RMS}. At the lower working voltages, the corresponding insulation lifetime is much longer than 36 years.

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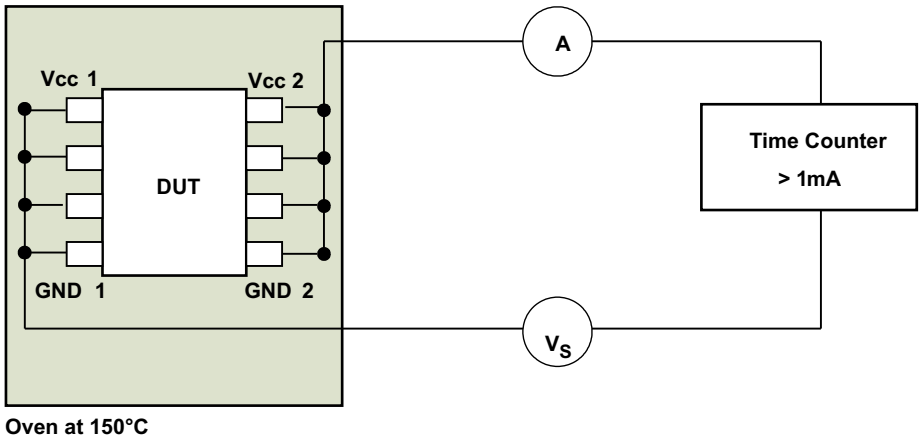


図 8-6. Test Setup for Insulation Lifetime Measurement

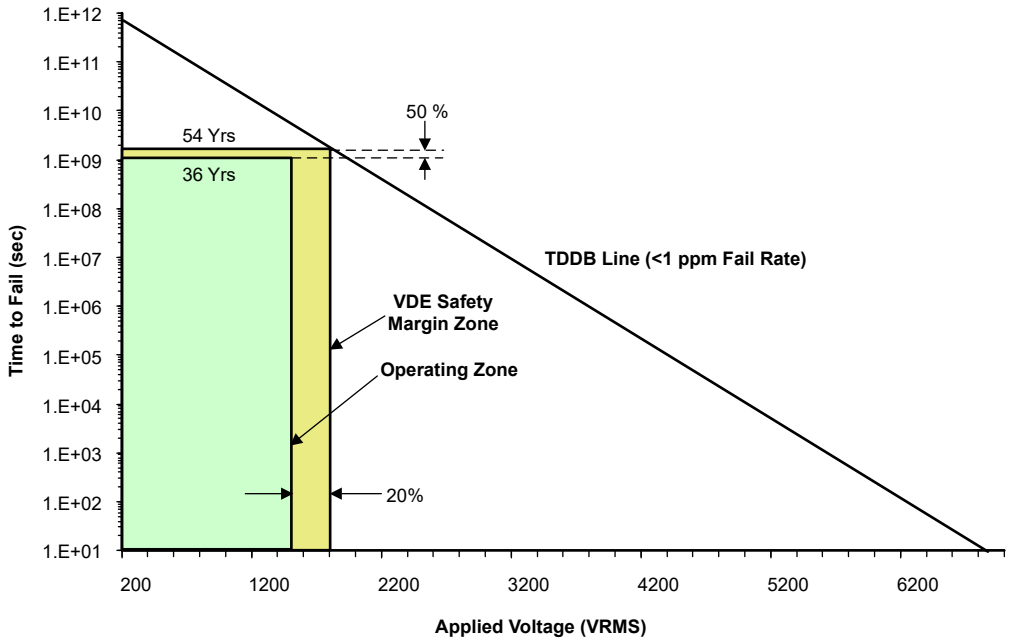


図 8-7. Insulation Lifetime Projection Data

9 Power Supply Recommendations

To help ensure reliable operation at data rates and supply voltages, a 0.1-µF bypass capacitor is recommended at input and output supply pins (V_{CC1} and V_{CC2}). The capacitors should be placed as close to the supply pins as possible. If only a single primary-side power supply is available in an application, isolated power can be generated for the secondary-side with the help of a transformer driver such as Texas Instruments' SN6501 or SN6505. For such applications, detailed power supply design and transformer selection recommendations are available in the *SN6501 Transformer Driver for Isolated Power Supplies* data sheet or the *SN6505 Low-Noise 1-A Transformer Drivers for Isolated Power Supplies* data sheet.

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10 Layout

10.1 Layout Guidelines

A minimum of four layers is required to accomplish a low EMI PCB design (see 図 10-1). Layer stacking should be in the following order (top-to-bottom): high-speed signal layer, ground plane, power plane and low-frequency signal layer.

- Routing the high-speed traces on the top layer avoids the use of vias (and the introduction of their inductances) and allows for clean interconnects between the isolator and the transmitter and receiver circuits of the data link.
- Placing a solid ground plane next to the high-speed signal layer establishes controlled impedance for transmission line interconnects and provides an excellent low-inductance path for the return current flow.
- Placing the power plane next to the ground plane creates additional high-frequency bypass capacitance of approximately 100 pF/inch^2.
- Routing the slower speed control signals on the bottom layer allows for greater flexibility as these signal links usually have margin to tolerate discontinuities such as vias.

If an additional supply voltage plane or signal layer is needed, add a second power or ground plane system to the stack to keep it symmetrical. This makes the stack mechanically stable and prevents it from warping. Also the power and ground plane of each power system can be placed closer together, thus increasing the high-frequency bypass capacitance significantly.

For detailed layout recommendations, see the *Digital Isolator Design Guide* application report.

10.1.1 PCB Material

For digital circuit boards operating at less than 150 Mbps, (or rise and fall times greater than 1 ns), and trace lengths of up to 10 inches, use standard FR-4 UL94V-0 printed circuit board. This PCB is preferred over cheaper alternatives because of lower dielectric losses at high frequencies, less moisture absorption, greater strength and stiffness, and the self-extinguishing flammability-characteristics.

10.2 Layout Example

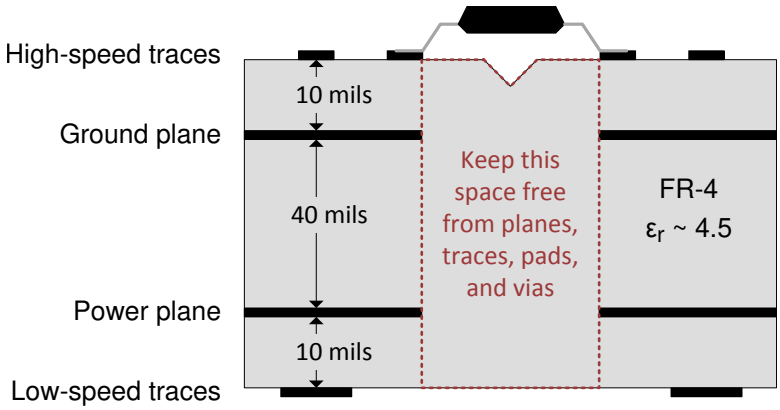


図 10-1. Layout Example Schematic

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11 Device and Documentation Support

11.1 Documentation Support

11.1.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *Digital Isolator Design Guide* application report
- Texas Instruments, *How to use isolation to improve ESD, EFT and Surge immunity in industrial systems* application report
- Texas Instruments, *Isolation Glossary*
- Texas Instruments, *TMS320F2803x Piccolo™ Microcontrollers* data sheet
- Texas Instruments, *ADS7953-Q1 Automotive 12-Bit, 1MSPS, 16-Channel Single-Ended Micropower, Serial Interface ADC* data sheet
- Texas Instruments, *REF50xxA-Q1 Low-Noise, Very Low Drift, Precision Voltage Reference* data sheet
- Texas Instruments, *SN6501-Q1 Transformer Driver for Isolated Power Supplies* data sheet
- Texas Instruments, *SN65HVD231Q-Q1 3.3-V CAN Transceiver* data sheet
- Texas Instruments, *TPS76333-Q1 Low-Power 150-mA Low-Dropout Linear Regulators* data sheet

11.2 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

表 11-1. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
ISO7760-Q1	Click here	Click here	Click here	Click here	Click here
ISO7761-Q1	Click here	Click here	Click here	Click here	Click here
ISO7762-Q1	Click here	Click here	Click here	Click here	Click here
ISO7763-Q1	Click here	Click here	Click here	Click here	Click here

11.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

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11.7 用語集

テキサス・インスツルメンツ用語集　この用語集には、用語や略語の一覧および定義が記載されています。

12 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision D (January 2024) to Revision E (July 2024) **Page**

- ドキュメント全体にわたって表、図、相互参照の採番方法を更新 1
- Updated Thermal Characteristics, Safety Limiting Values, and Thermal Derating Curves to provide more accurate system-level thermal calculations 8
- Changed CPG parameter description from "External clearance" to "External creepage" 9
- Updated electrical and switching characteristics to match device performance 13

Changes from Revision C (October 2022) to Revision D (January 2024) **Page**

- Added table note to Data rate specification 7
- Changed V_{IORM} value for DW-16 package from "1414 V_{PK}" to "2121 V_{PK} 9
- Changed V_{IOWM} values for DW-16 package from "1000 V_{RMS}" and "1414 V_{DC}" to "1500 V_{RMS}" and "2121 V_{DC}" 9
- Updated certification information 11

Changes from Revision B (October 2020) to Revision C (October 2022) **Page**

- ドキュメント全体にわたって表、図、相互参照の採番方法を更新。 1
- ドキュメント全体を通して標準名を以下のように変更：「DIN V VDE V 0884-11:2017-01」から次のものに変更：「DIN EN IEC 60747-17 (VDE 0884-17)」 1
- ドキュメント全体を通して、IEC/EN/CSA 60950-1 規格への参照を削除 1
- Updated Thermal characteristics, Safety Limiting Values, and Thermal derating Curves to provide more accurate system-level thermal calculations 6
- Updated electrical and switching characteristics to match device performance 6
- Changed the C_{IO} value for the DBQ package from 1.1 to 0.9 pF 9
- Changed working voltage lifetime margin From: 87.5% To: 50%, minimum required insulation lifetime From: 37.5 years To: 30 years and insulation lifetime per TDDB From: 135 years To: 169 years in Insulation Lifetime per DIN EN IEC 60747-17 (VDE 0884-17) 32
- Changed Figure 9-7 per DIN EN IEC 60747-17 (VDE 0884-17) 32

Changes from Revision A (February 2019) to Revision B (October 2020) **Page**

- 機能安全の箇条書き項目を追加。 1
- Added the maximum transient isolation voltage for the DW-16 package of the ISO7761, ISO7762, and ISO7763 devices and changed the maximum value for the DBQ-16 package from 3600 to 4242 for all devices 9
- Changed table note and table condition of safety limiting values 11

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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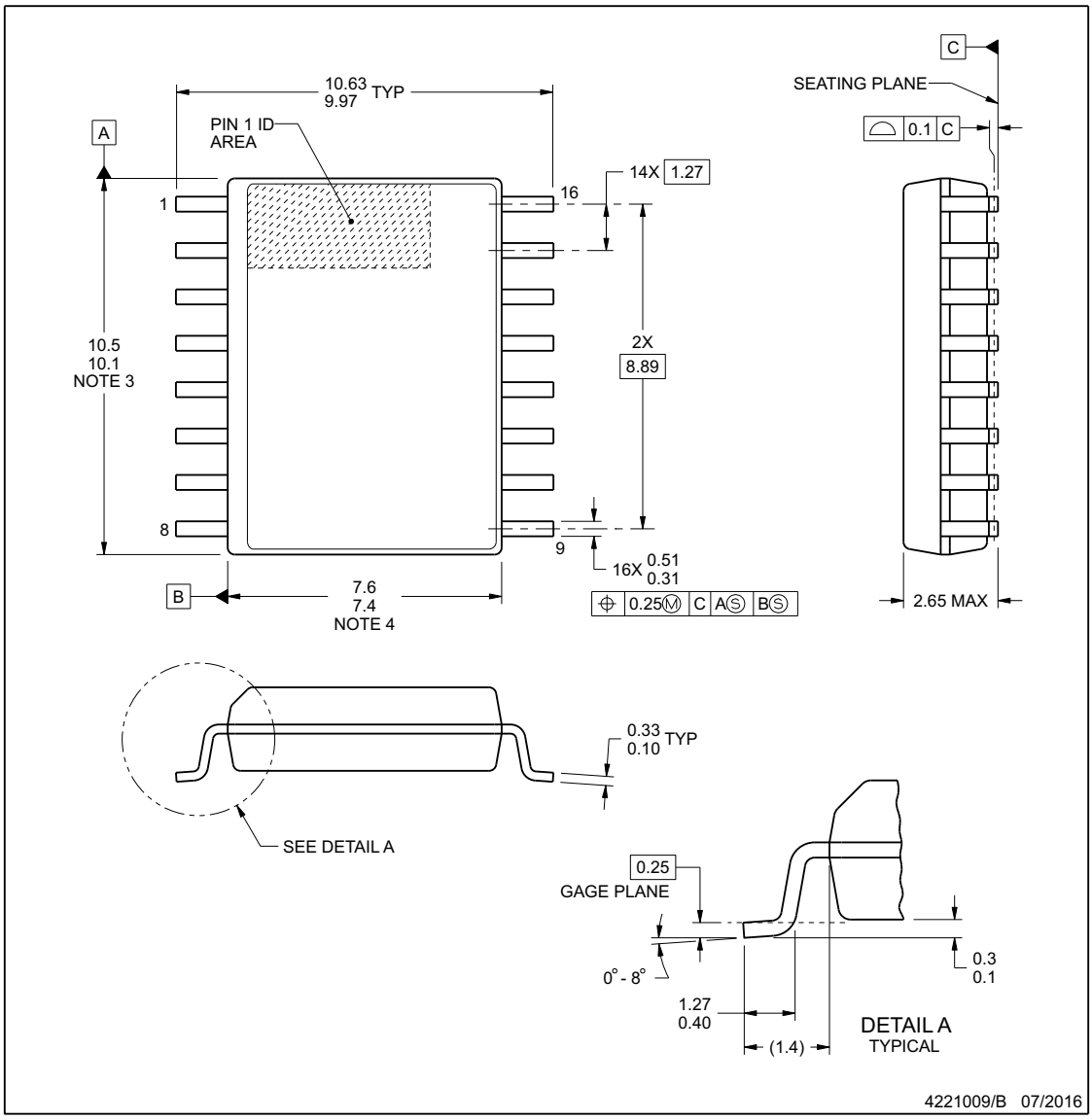


PACKAGE OUTLINE

DW0016B

SOIC - 2.65 mm max height

SOIC



NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.
5. Reference JEDEC registration MS-013.

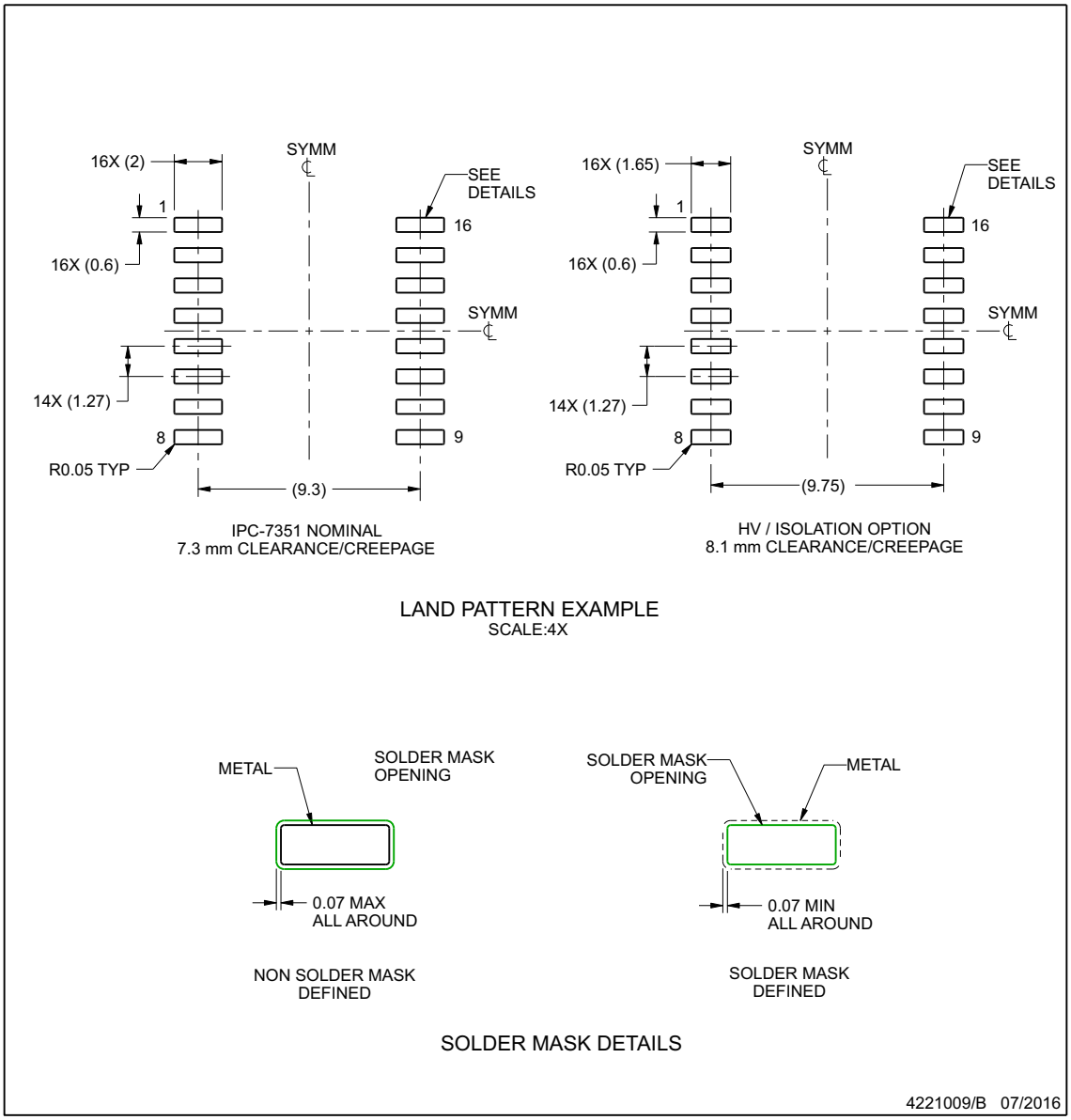
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EXAMPLE BOARD LAYOUT

DW0016B

SOIC - 2.65 mm max height

SOIC



NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

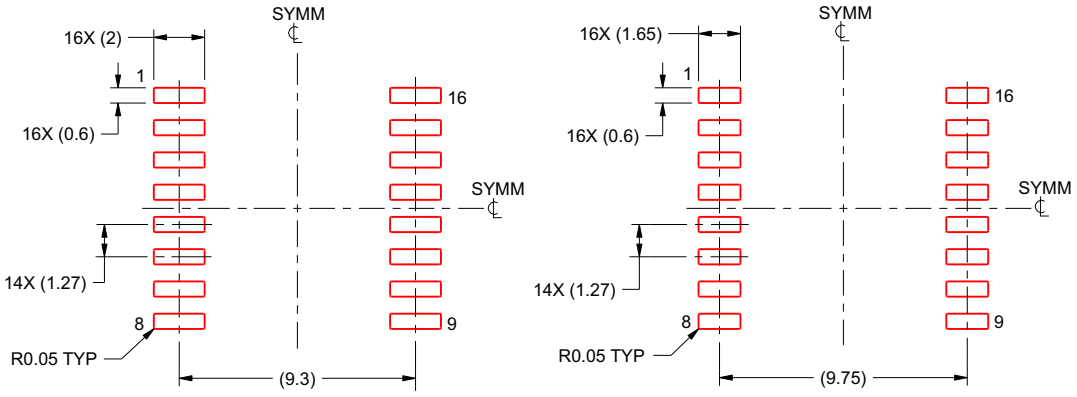
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EXAMPLE STENCIL DESIGN

DW0016B

SOIC - 2.65 mm max height

SOIC



IPC-7351 NOMINAL
7.3 mm CLEARANCE/CREEPAGE

HV / ISOLATION OPTION
8.1 mm CLEARANCE/CREEPAGE

SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:4X

4221009/B 07/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
ISO7760FQDBQRQ1	Active	Production	SSOP (DBQ) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	(7760F, 7760FQ)
ISO7760FQDBQRQ1.A	Active	Production	SSOP (DBQ) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	(7760F, 7760FQ)
ISO7760FQDWRQ1	Active	Production	SOIC (DW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	(ISO7760F, ISO7760 FQ)
ISO7760FQDWRQ1.A	Active	Production	SOIC (DW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	(ISO7760F, ISO7760 FQ)
ISO7760QDBQRQ1	Active	Production	SSOP (DBQ) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	(7760, 7760Q)
ISO7760QDBQRQ1.A	Active	Production	SSOP (DBQ) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	(7760, 7760Q)
ISO7760QDWRQ1	Active	Production	SOIC (DW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	(ISO7760, ISO7760Q)
ISO7760QDWRQ1.A	Active	Production	SOIC (DW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	(ISO7760, ISO7760Q)
ISO7761FQDBQRQ1	Active	Production	SSOP (DBQ) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	(7761F, 7761FQ)
ISO7761FQDBQRQ1.A	Active	Production	SSOP (DBQ) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	(7761F, 7761FQ)
ISO7761FQDWRQ1	Active	Production	SOIC (DW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	(ISO7761F, ISO7761 FQ)
ISO7761FQDWRQ1.A	Active	Production	SOIC (DW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	(ISO7761F, ISO7761 FQ)
ISO7761QDBQRQ1	Active	Production	SSOP (DBQ) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	(7761, 7761Q)
ISO7761QDBQRQ1.A	Active	Production	SSOP (DBQ) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	(7761, 7761Q)
ISO7761QDWRQ1	Active	Production	SOIC (DW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	(ISO7761, ISO7761Q)
ISO7761QDWRQ1.A	Active	Production	SOIC (DW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	(ISO7761, ISO7761Q)
ISO7762FQDBQRQ1	Active	Production	SSOP (DBQ) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	(7762F, 7762FQ)
ISO7762FQDBQRQ1.A	Active	Production	SSOP (DBQ) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	(7762F, 7762FQ)
ISO7762FQDWRQ1	Active	Production	SOIC (DW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	(ISO7762F, ISO7762 FQ)
ISO7762FQDWRQ1.A	Active	Production	SOIC (DW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	(ISO7762F, ISO7762 FQ)
ISO7762QDBQRQ1	Active	Production	SSOP (DBQ) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	(7762, 7762Q)
ISO7762QDBQRQ1.A	Active	Production	SSOP (DBQ) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	(7762, 7762Q)

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
ISO7762QDWRQ1	Active	Production	SOIC (DW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	(ISO7762, ISO7762Q)
ISO7762QDWRQ1.A	Active	Production	SOIC (DW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	(ISO7762, ISO7762Q)
ISO7763FQDBQRQ1	Active	Production	SSOP (DBQ) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	(7763F, 7763FQ)
ISO7763FQDBQRQ1.A	Active	Production	SSOP (DBQ) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	(7763F, 7763FQ)
ISO7763FQDWRQ1	Active	Production	SOIC (DW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	(ISO7763F, ISO7763 FQ)
ISO7763FQDWRQ1.A	Active	Production	SOIC (DW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	(ISO7763F, ISO7763 FQ)
ISO7763QDBQRQ1	Active	Production	SSOP (DBQ) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	(7763, 7763Q)
ISO7763QDBQRQ1.A	Active	Production	SSOP (DBQ) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	(7763, 7763Q)
ISO7763QDWRQ1	Active	Production	SOIC (DW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	(ISO7763, ISO7763Q)
ISO7763QDWRQ1.A	Active	Production	SOIC (DW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	(ISO7763, ISO7763Q)

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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OTHER QUALIFIED VERSIONS OF ISO7760-Q1, ISO7761-Q1, ISO7762-Q1, ISO7763-Q1 :

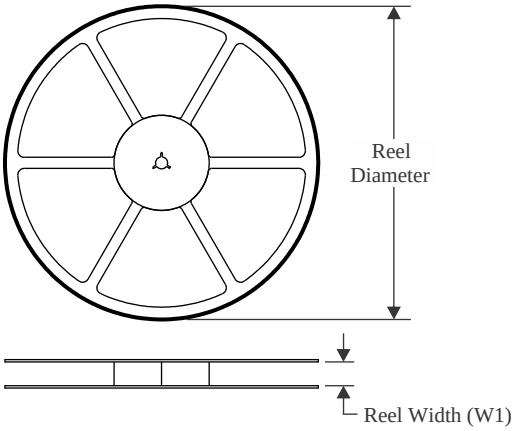
- Catalog : ISO7760, ISO7761, ISO7762, ISO7763

NOTE: Qualified Version Definitions:

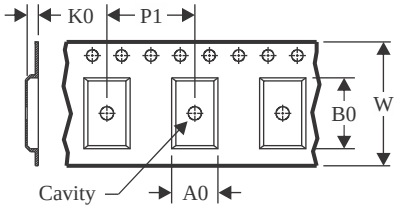
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

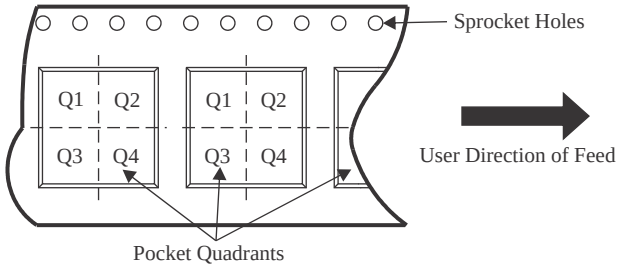


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

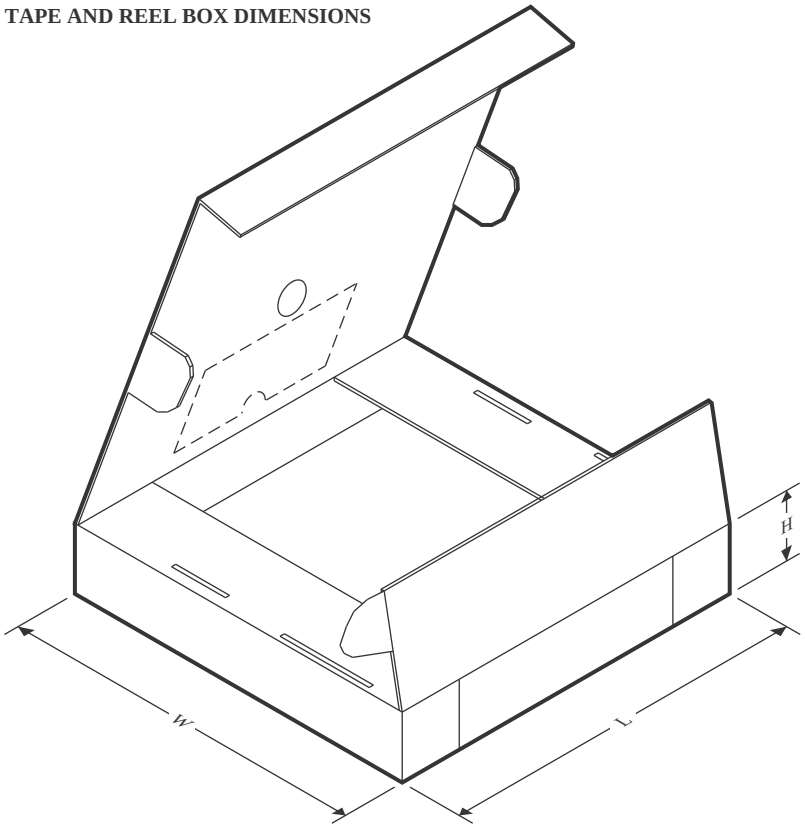


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ISO7760FQDBQRQ1	SSOP	DBQ	16	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
ISO7760FQDBQRQ1	SSOP	DBQ	16	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
ISO7760FQDWRQ1	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
ISO7760FQDWRQ1	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
ISO7760QDBQRQ1	SSOP	DBQ	16	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
ISO7760QDWRQ1	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
ISO7760QDWRQ1	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
ISO7761FQDBQRQ1	SSOP	DBQ	16	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
ISO7761FQDWRQ1	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
ISO7761FQDWRQ1	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
ISO7761QDBQRQ1	SSOP	DBQ	16	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
ISO7761QDWRQ1	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
ISO7761QDWRQ1	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
ISO7762FQDBQRQ1	SSOP	DBQ	16	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
ISO7762FQDBQRQ1	SSOP	DBQ	16	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
ISO7762FQDWRQ1	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ISO7762FQDWRQ1	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
ISO7762QDBQRQ1	SSOP	DBQ	16	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
ISO7762QDWRQ1	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
ISO7762QDWRQ1	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
ISO7763FQDBQRQ1	SSOP	DBQ	16	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
ISO7763FQDBQRQ1	SSOP	DBQ	16	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
ISO7763FQDWRQ1	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
ISO7763FQDWRQ1	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
ISO7763QDBQRQ1	SSOP	DBQ	16	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
ISO7763QDWRQ1	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ISO7760FQDBQRQ1	SSOP	DBQ	16	2500	353.0	353.0	32.0
ISO7760FQDBQRQ1	SSOP	DBQ	16	2500	350.0	350.0	43.0
ISO7760FQDWRQ1	SOIC	DW	16	2000	356.0	356.0	36.0
ISO7760FQDWRQ1	SOIC	DW	16	2000	353.0	353.0	32.0
ISO7760QDBQRQ1	SSOP	DBQ	16	2500	353.0	353.0	32.0
ISO7760QDWRQ1	SOIC	DW	16	2000	353.0	353.0	32.0
ISO7760QDWRQ1	SOIC	DW	16	2000	356.0	356.0	36.0
ISO7761FQDBQRQ1	SSOP	DBQ	16	2500	353.0	353.0	32.0
ISO7761FQDWRQ1	SOIC	DW	16	2000	353.0	353.0	32.0
ISO7761FQDWRQ1	SOIC	DW	16	2000	356.0	356.0	36.0
ISO7761QDBQRQ1	SSOP	DBQ	16	2500	353.0	353.0	32.0
ISO7761QDWRQ1	SOIC	DW	16	2000	356.0	356.0	36.0
ISO7761QDWRQ1	SOIC	DW	16	2000	353.0	353.0	32.0
ISO7762FQDBQRQ1	SSOP	DBQ	16	2500	353.0	353.0	32.0
ISO7762FQDBQRQ1	SSOP	DBQ	16	2500	367.0	367.0	38.0
ISO7762FQDWRQ1	SOIC	DW	16	2000	353.0	353.0	32.0
ISO7762FQDWRQ1	SOIC	DW	16	2000	356.0	356.0	36.0
ISO7762QDBQRQ1	SSOP	DBQ	16	2500	353.0	353.0	32.0

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ISO7762QDWRQ1	SOIC	DW	16	2000	356.0	356.0	36.0
ISO7762QDWRQ1	SOIC	DW	16	2000	353.0	353.0	32.0
ISO7763FQDBQRQ1	SSOP	DBQ	16	2500	353.0	353.0	32.0
ISO7763FQDBQRQ1	SSOP	DBQ	16	2500	350.0	350.0	43.0
ISO7763FQDWRQ1	SOIC	DW	16	2000	356.0	356.0	36.0
ISO7763FQDWRQ1	SOIC	DW	16	2000	353.0	353.0	32.0
ISO7763QDBQRQ1	SSOP	DBQ	16	2500	353.0	353.0	32.0
ISO7763QDWRQ1	SOIC	DW	16	2000	353.0	353.0	32.0

GENERIC PACKAGE VIEW

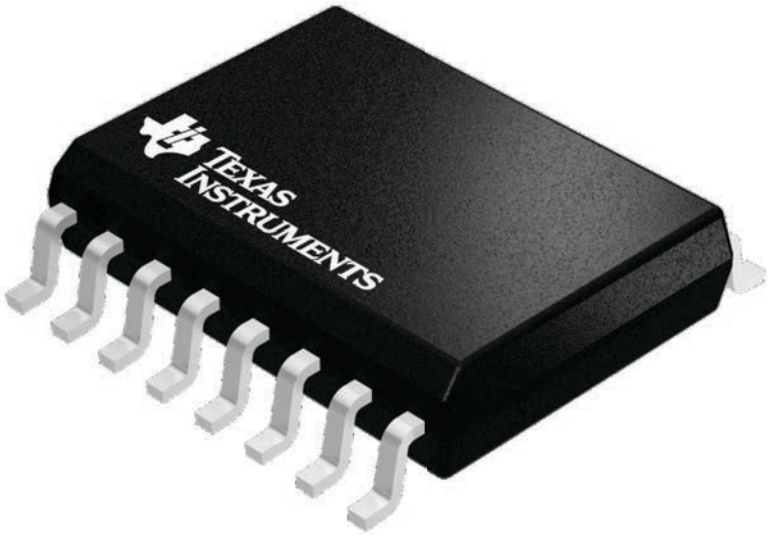
DW 16

SOIC - 2.65 mm max height

7.5 x 10.3, 1.27 mm pitch

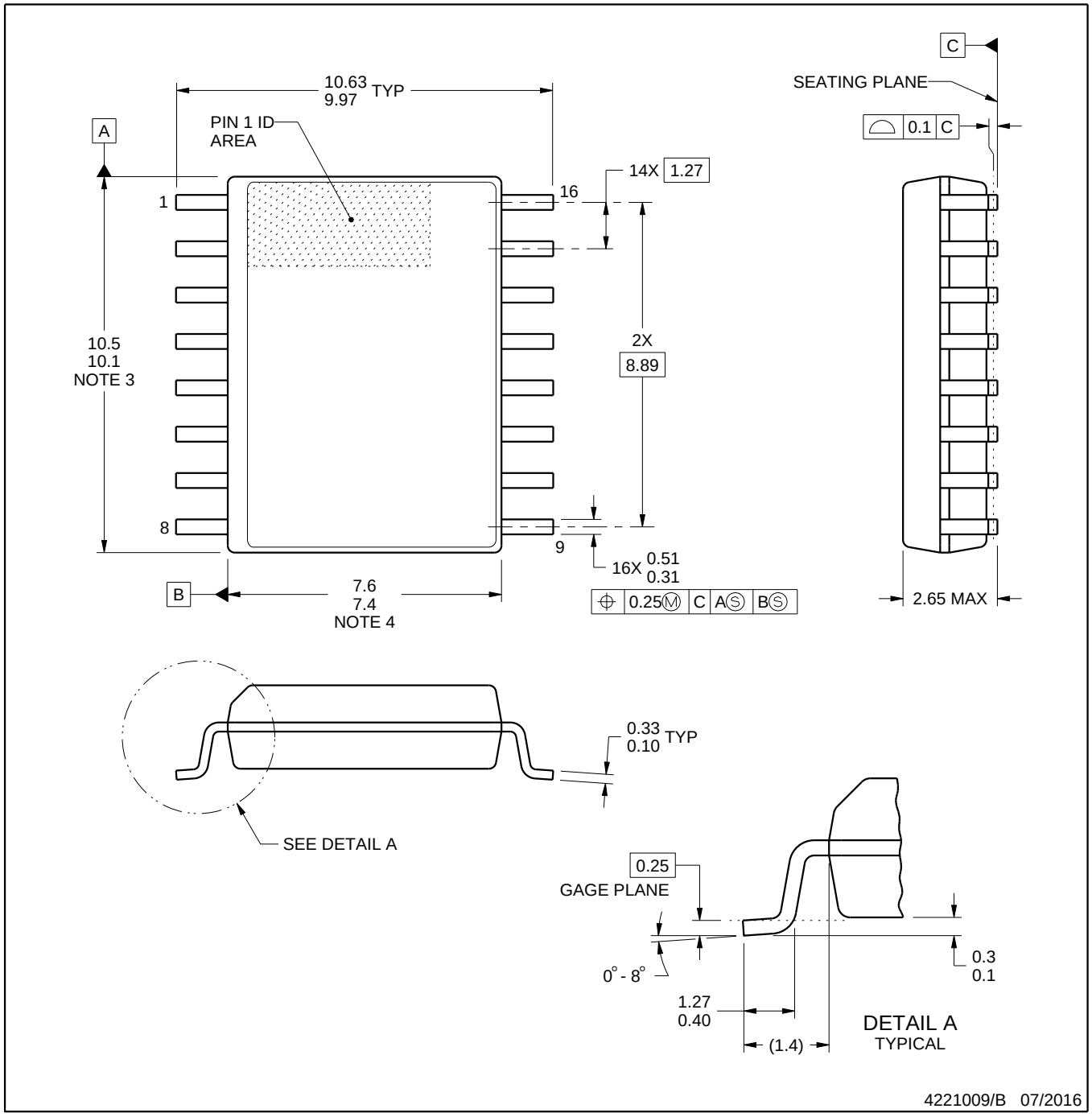
SMALL OUTLINE INTEGRATED CIRCUIT

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



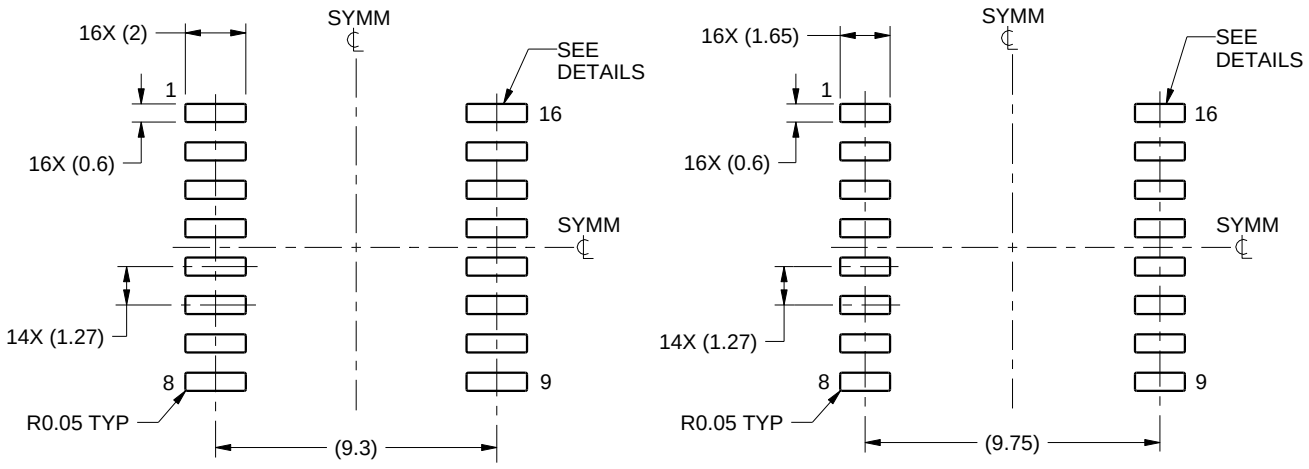
4224780/A

SOIC



NOTES:

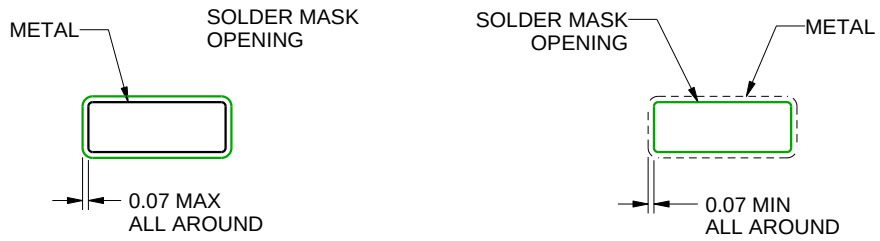
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.
5. Reference JEDEC registration MS-013.



IPC-7351 NOMINAL
7.3 mm CLEARANCE/CREEPAGE

HV / ISOLATION OPTION
8.1 mm CLEARANCE/CREEPAGE

LAND PATTERN EXAMPLE
SCALE:4X



NON SOLDER MASK DEFINED

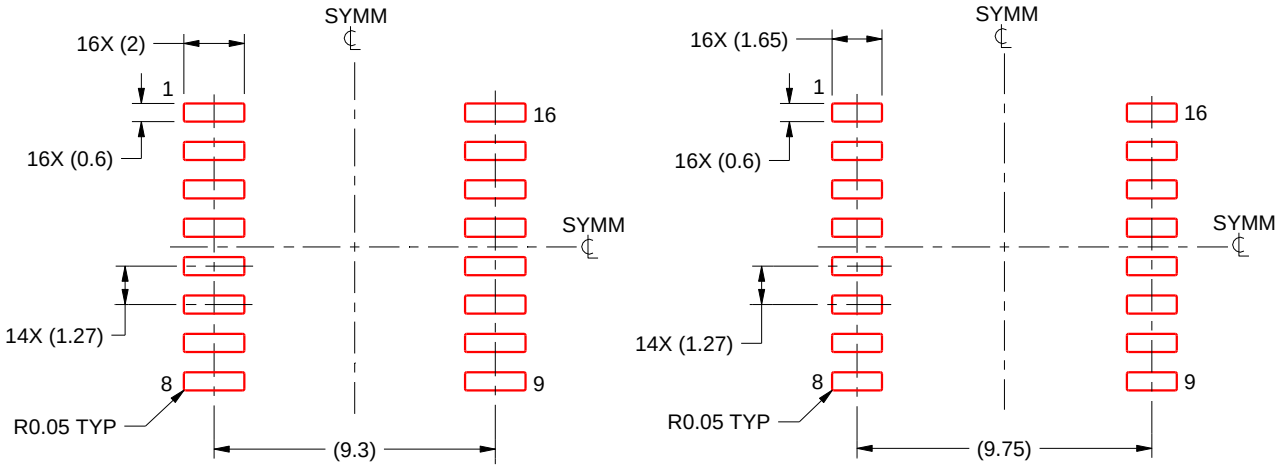
SOLDER MASK DEFINED

SOLDER MASK DETAILS

4221009/B 07/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



IPC-7351 NOMINAL
7.3 mm CLEARANCE/CREEPAGE

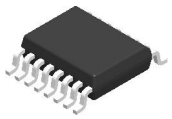
HV / ISOLATION OPTION
8.1 mm CLEARANCE/CREEPAGE

SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:4X

4221009/B 07/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

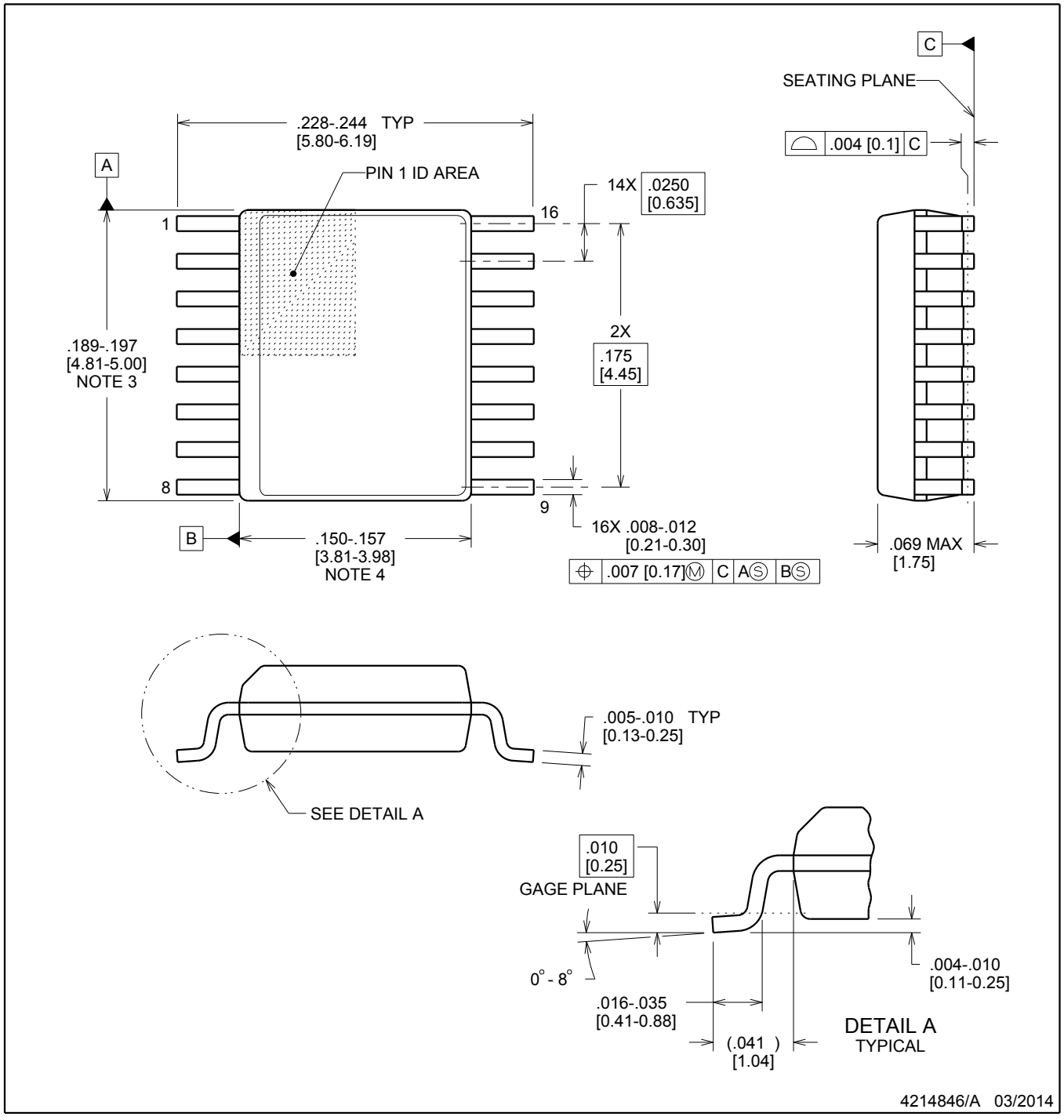


PACKAGE OUTLINE

DBQ0016A

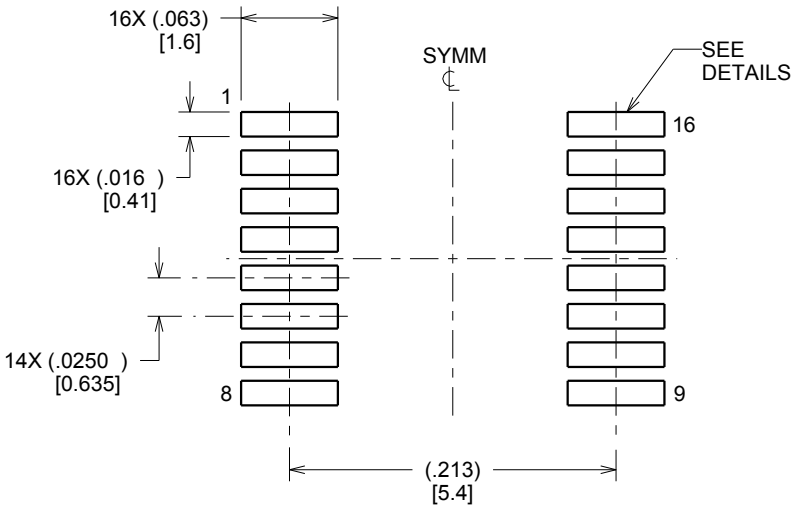
SSOP - 1.75 mm max height

SHRINK SMALL-OUTLINE PACKAGE

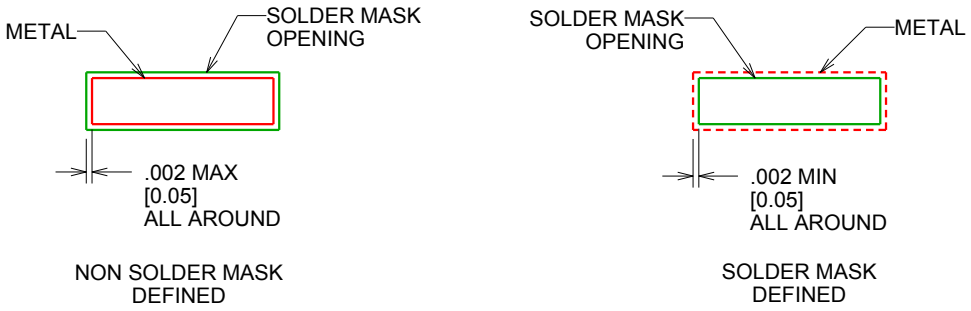


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 inch, per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MO-137, variation AB.



LAND PATTERN EXAMPLE
SCALE:8X



SOLDER MASK DETAILS

4214846/A 03/2014

NOTES: (continued)

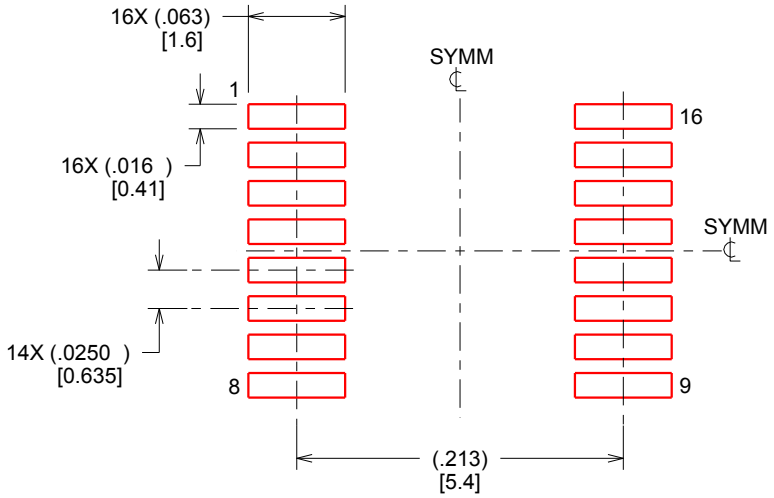
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DBQ0016A

SSOP - 1.75 mm max height

SHRINK SMALL-OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.127 MM] THICK STENCIL
SCALE:8X

4214846/A 03/2014

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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