IWR1443 シングルチップ、76～81GHzミリ波センサ

1 デバイスの概要

1.1 特長

- FMCWトランシーバ
  - PLL、トランスミッタ、レシーバ、ベースバンド、ADCを内蔵
  - 76～81GHz帯で連続帯域幅4GHz
  - 4つの受信チャネル
  - 3つの送信チャネル(2つを同時に使用可能)
  - フラクショナルN PLLを使用した超高精度のチャープエンジン
  - TX電力: 12dBm
  - RXノイズ指数:
    - 14dB (76～77GHz)
    - 15dB (77～81GHz)
  - 1MHzでの位相ノイズ:
    - −95dBc/Hz (76～77GHz)
    - −93dBc/Hz (77～81GHz)
- 較正および自己テストを内蔵
  - ARM® Cortex®-R4Fを搭載した無線制御システム
  - 内蔵ファームウェア(ROM)
  - 周波数および温度での自己較正システム
- 組み込み機器向けのオンチップ・プログラマブル・コア
  - 200MHzクロックで動作するCortex®-R4Fマイクロコントローラを内蔵
  - オンチップ・ブートローダにより、自律モード(QSPIフラッシュ・メモリからのユーザー・アプリケーションのロード)をサポート
  - 内蔵ペリフェラル
    - ECC付き内部メモリ
    - レーダー・ハードウェア・アクセラレータ(FFT、対数振幅の計算など)
    - 内蔵タイマ(ウォッチドッグおよび最大4つの32ビットまたは2つの64ビット・タイマ)
    - I2C (マスタ・モードとスレーブ・モードをサポート)
    - 2つのSPIポート
    - CANポート
    - 最大6つの汎用ADCポート
- 高速データ・インターフェイスにより分散アプリケーションをサポート
- ホスト・インターフェイス
  - SPIを介した外部プロセッサとの制御インターフェイス
  - MIPI D-PHYおよびCSI2 V1.1を介した外部プロセッサとのデータ・インターフェイス
  - フォルト・レポート用の割り込み
- IWR1443の高度な機能
  - ホスト・プロセッサの介在を伴わない組み込み自己監視機能
  - 複素ベースバンド・アーキテクチャ
  - 内蔵された干渉検出機能
- 電源管理
  - 内蔵されたLDOネットワークによりPSRRの向上を実現
  - I/Oがデュアル電圧3.3V/1.8Vに対応
- クロック・ソース
  - 40MHzの外部発振器をサポート
  - 40MHzの外部駆動クロック(方形波/正弦波)をサポート
- ハードウェア設計が簡単
  - 0.65mmピッチ、161ピン、10.4mm×10.4mmのフリップチップBGAパッケージにより組み立てが簡単で、低コストのPCBを設計可能
  - 小型ソリューション
- 動作条件
  - 接合部温度範囲: −40℃～105℃

1.2 アプリケーション

- 範囲/速度/角度測定用の産業用センサ
- タンクレベル・プロービング・レーダー
- 変位検出
- フィールド・トランスミッタ
- 交通監視
- 近接および位置センシング
- セキュリティと監視
- ファクトリ・オートメーション
- 安全保護

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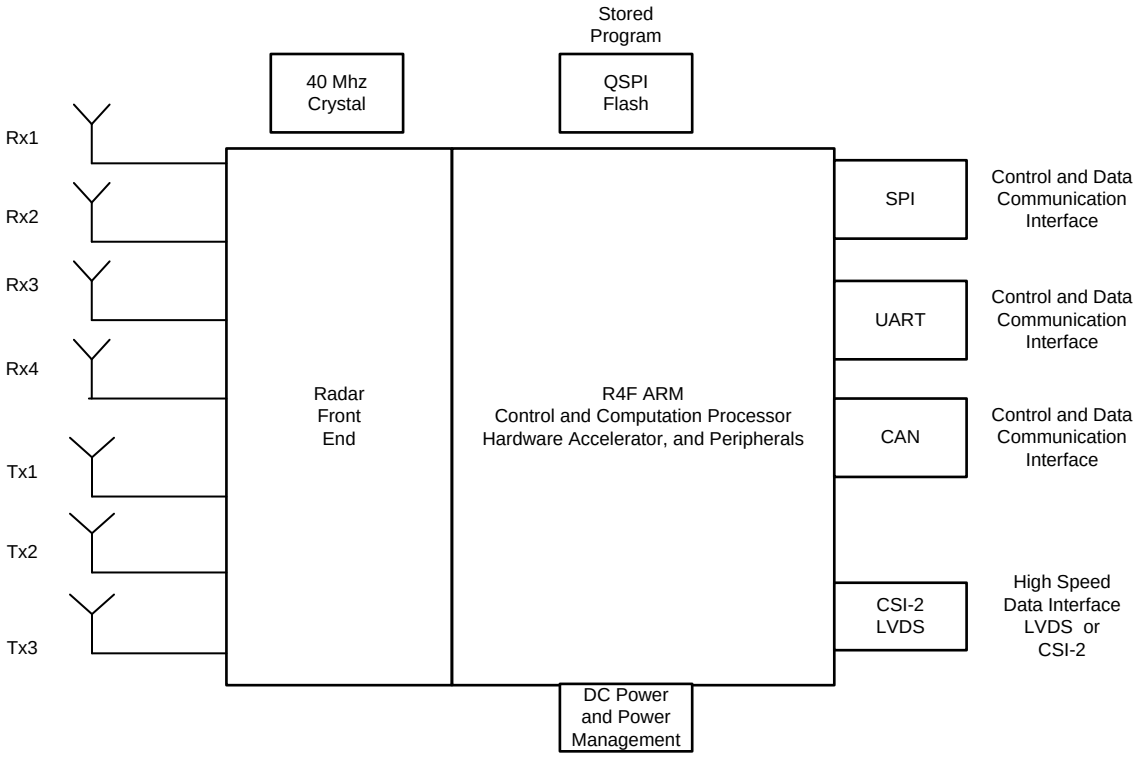


図 1-1. 産業用の自律センサ・アプリケーション

1.3 概要

IWR1443は、FMCWレーダー・テクノロジを採用した統合型シングルチップ・ミリ波センサであり、最高4GHzの連続チャープにより76～81GHz帯で動作可能です。TIの低消費電力45nm RFCMOSプロセスで製造されるこのソリューションは、超小型のフォームファクタで、かつてないレベルの統合を実現しています。IWR1443は、ビル・オートメーション、ファクトリ・オートメーション、ドローン、マテリアル・ハンドリング、交通監視、サーベイランスといった産業アプリケーションにおける、低消費電力で自己監視機能を備えた、超高精度の産業用レーダー・システムに最適なソリューションです。

自己完結型のシングルチップ・ソリューションであることから、76～81GHz帯のミリ波センサを簡単に実装できます。PLLおよびA/Dコンバータを内蔵する3TX/4RXシステムのモノリシック実装を実現しています。複素FFTおよびCFAR検出をサポートする、完全に構成可能なハードウェア・アクセラレータも搭載しています。また、2つのARM R4Fプロセッサ・サブシステムを搭載しており、一方のプロセッサ・システムはマスタ制御と追加アルゴリズム用、もう一方のプロセッサ・サブシステムはフロントエンドの構成、制御、較正用となります。プログラミング・モデルを変更するだけで、さまざまなセンサを実装でき、マルチモード・センサの実装においては動的再構成にも対応します。また、リファレンス・ハードウェア・デザイン、ソフトウェア・ドライバ、サンプル構成、APIガイド、トレーニング、ユーザー・マニュアルを含む、完全なプラットフォーム・ソリューションとして供給されます。

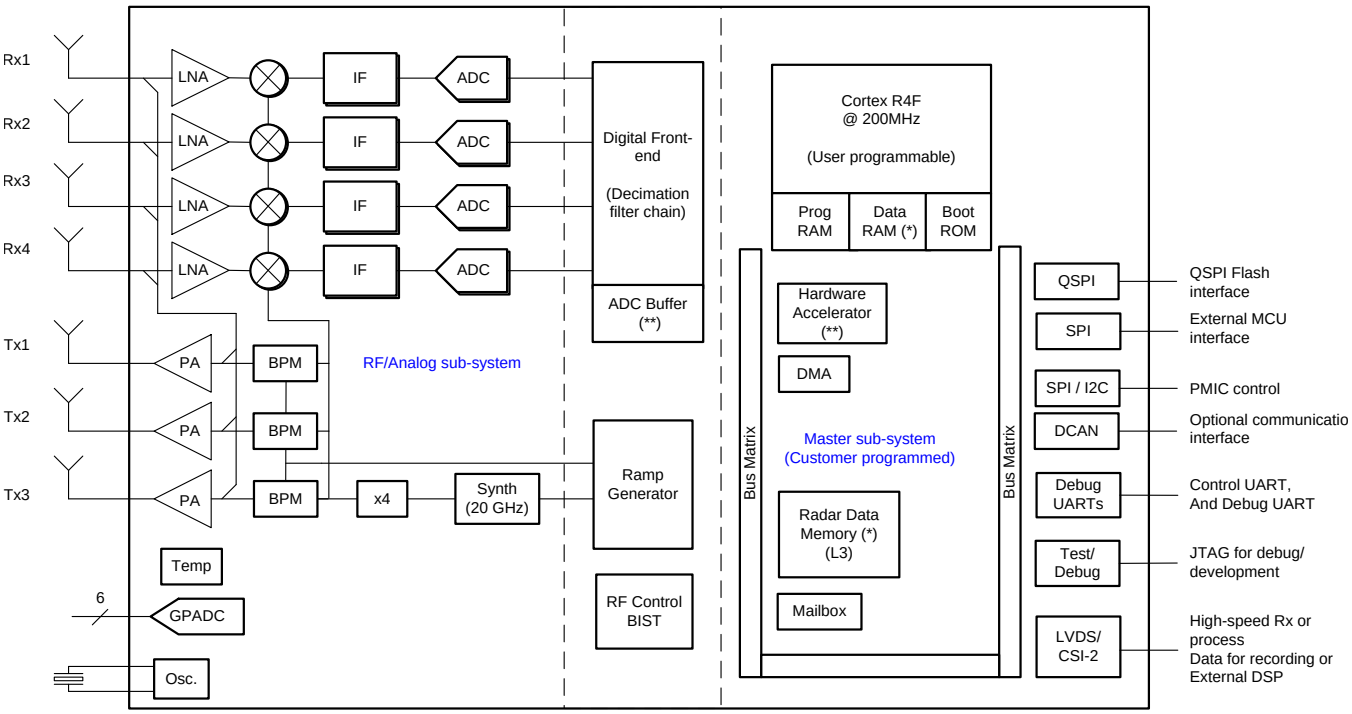
製品情報(1)

型番	パッケージ	本体サイズ
IWR1443FQAGABLR（テープ・アンド・リール）	FCBGA (161)	10.4mm×10.4mm
IWR1443FQAGABL（トレイ）		

(1) 詳細については、9、「*メカニカル、パッケージ、および注文情報*」を参照してください。

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1.4 機能ブロック図



(*) Total RAM available in Master subsystem is divided into ARM-Data RAM, Tightly Coupled Memory, Radar Data Memory, Patch Memory
(**) Shared Memory for ADC Buffer and Hardware Accelerator

Table of Contents

1 デバイスの概要 1
1.1 特長 1
1.2 アプリケーション 1
1.3 概要 2
1.4 機能ブロック図 3
2 改訂履歴 5
3 Device Comparison 7
3.1 Related Products 8
4 Terminal Configuration and Functions 9
4.1 Pin Diagram 9
4.2 Signal Descriptions 13
4.3 Pin Multiplexing 16
5 Specifications 21
5.1 Absolute Maximum Ratings 21
5.2 ESD Ratings 21
5.3 Power-On Hours (POH) 21
5.4 Recommended Operating Conditions 22
5.5 Power Supply Specifications 22
5.6 Power Consumption Summary 23
5.7 RF Specification 24
5.8 Thermal Resistance Characteristics for FCBGA Package [ABL0161] 25
5.9 Timing and Switching Characteristics 25
6 Detailed Description 51
6.1 Overview 51
6.2 Functional Block Diagram 51
6.3 External Interfaces 52
6.4 Subsystems 52
6.5 Accelerators and Coprocessors 57
6.6 Other Subsystems 58
6.7 Identification 62
6.8 Boot Modes 62
7 Applications, Implementation, and Layout 65
7.1 Application Information 65
7.2 Reference Schematic 65
7.3 Layout 66
8 Device and Documentation Support 67
8.1 Device Nomenclature 67
8.2 Tools and Software 68
8.3 Documentation Support 68
8.4 Community Resources 69
8.5 商標 69
8.6 静電気放電に関する注意事項 69
8.7 Export Control Notice 69
8.8 Glossary 69
9 Mechanical, Packaging, and Orderable Information 70
9.1 Packaging Information 70

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2 改訂履歴

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

2018年2月20日発行分から2018年10月31日発行分への変更 (from B Revision (February 2018) to C Revision) **Page**

- RXノイズ指数を「15dB (76～77GHz)」から「14dB (76～77GHz)」に更新 1
- RXノイズ指数を「16dB (77～81GHz)」から「15dB (77～81GHz)」に更新 1
- 1MHzでの位相ノイズを「－94dBc/Hz (76～77GHz)」から「－95dBc/Hz (76～77GHz)」に更新 1
- 1MHzでの位相ノイズを「－91dBc/Hz (77～81GHz)」から「－93dBc/Hz (77～81GHz)」に更新 1
- 「高速データ・インターフェイス」箇条書き項目から「（中間データ）」を削除 1
- 外部駆動の発振器、および外部駆動のクロックから、50MHzを削除 1
- 製品情報を更新 2
- 「*機能ブロック図*」からVMOSブロックを削除 3
- Added table note to "Number of transmitters" in Device Features Comparison 7
- Updated IWR1443 and IWR1642 Product status from AI to PD 7
- Updated OSC_CLKOUT 13
- Updated P7 from "Open Drain" to "Pull Up' 13
- Updated B10 DESCRIPTION 14
- Updated A10, A13, A2, and B2 DESCRIPTION 14
- Removed footnote from Flash programming and RS232 UART 15
- Updated ESD Ratings 21
- Updated/Changed Power-On Hours (POH) 21
- Updated VIOIN in Recommended Operating Conditions 22
- Updated V_{IL} 1.8V MAX from "3*VIOIN" to "0.3*VIOIN" 22
- Updated V_{OH} in Recommended Operating Conditions 22
- Updated V_{OH} in Recommended Operating Conditions 22
- Updated Recommended Operating Conditions 22
- Added "VNWA" to 1.2 V Supply in Power Supply Rails Characteristics 22
- Completely updated Ripple Specifications table 23
- Updated Receiver Noise figure values in RF Specification 24
- Updated Receiver 1-dB compression point value from "–5" to "–8" 24
- Updated "IQ gain mismatch" to "Image Rejection Ratio (IMRR)" 24
- Removed IQ phase mismatch from RF Specification 24
- Updated RF Specification table 24
- Updated footnote in RF Specification 25
- Removed 1v4 signal from Device Wakeup 26
- Updated Device Wake-up Sequence 26
- Updated Synchronized Frame Triggering text 27
- Added Synchronized Frame Triggering subsection 27
- Removed T_{Lag} from Frame Trigger Timing table 27
- Updated Crystal Implementation note 28
- Updated/Changed f_P Parallel resonance crystal frequency from " 40, 50" to "40" 28
- Completely updated External Clock Mode Specifications 29
- Updated SPI Slave Mode Timing Requirements 35
- Added LVDS Interface Configuration 38
- Updated LVDS Interface Lane Config image 38
- Updated Timing Parameters 38
- Updated LVDS Electrical Characteristics 39
- Updated Timing Requirements for QSPI Input (Read) Timings 44
- Added Q12, Q13, Q14, and Q15 to QSPI Switching Characteristics 45
- Updated Data bit rate from 900 Mbps to 600 Mbps 48
- Removed $T_{CLK-SETTLE}$ and $T_{HS-SETTLE}$ 48
- Updated *Clock Subsystem* diagram 53
- Updated/Changed Transmit Subsystem (Per Channel) 54
- Removed Master System Memory Map 56
- Updated Host Interface 57
- Updated text in "A2D Data Format Over CSI2 Interface" 58
- Updated text in ADC Channels (Service) for User Application 60
- Completely updated GP-ADC Parameter table 60

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- Updated text in Functional Mode 64
- Updated Application Information 65
- Updated Device Nomenclature 68

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3 Device Comparison

Table 3-1. Device Features Comparison

FUNCTION		IWR1443	IWR1642
Number of receivers		4	4
Number of transmitters		3	2
On-chip memory		576KB	1.5MB
Max I/F (Intermediate Frequency) (MHz)		15	5
Max real sampling rate (Msps)		37.5	12.5
Max complex sampling rate (Msps)		18.75	6.25
Processor			
MCU (R4F)		Yes	Yes
DSP (C674x)		—	Yes
Peripherals			
Serial Peripheral Interface (SPI) ports		1	2
Quad Serial Peripheral Interface (QSPI)		Yes	Yes
Inter-Integrated Circuit (I^2C) interface		1	1
Controller Area Network (DCAN) interface		Yes	Yes
Trace		—	Yes
PWM		—	Yes
Hardware In Loop (HIL/DMM)		—	Yes
GPADC		Yes	Yes
LVDS/Debug		Yes	Yes
CSI2		Yes	—
Hardware accelerator		Yes	—
1-V bypass mode		Yes	Yes
JTAG		Yes	Yes
Product status	Product Preview (PP), Advance Information (AI), or Production Data (PD)	PD(1)	PD(1)

(1) PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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3.1 Related Products

For information about other devices in this family of products or related products see the links that follow.

mmWave Sensors TI's mmWave sensors rapidly and accurately sense range, angle and velocity with less power using the smallest footprint mmWave sensor portfolio for industrial applications.

mmWave IWR The Texas Instruments IWR1xxx family of mmWave Sensors are highly integrated and built on RFCMOS technology operating in 76- to 81-GHz frequency band. The devices have a closed-loop PLL for precise and linear chirp synthesis, includes a built-in radio processor (BIST) for RF calibration and safety monitoring. The devices have a very small-form factor, low power consumption, and are highly accurate. Industrial applications from long range to ultra short range can be realized using these devices.

Companion Products for IWR1443 Review products that are frequently purchased or used in conjunction with this product.

IWR1443 Reference Designs The IWR1443 TI Designs Reference Design Library is a robust reference design library spanning analog, embedded processor and connectivity. Created by TI experts to help you jump-start your system design, all TI Designs include schematic or block diagrams, BOMs, and design files to speed your time to market. Search and download designs at ti.com/tidesigns.

Power Optimization for IWR1443 77GHz-Level Transmitter Reference Design The TIDEP-0091 highlights strategies for power optimization of a IWR1443 76- to 81-GHz mmWave sensor in tank level-probing applications, displacement sensors, 4- to 20-mA sensors, and other low-power applications for detecting range with high accuracy in minimal power envelope.

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4 Terminal Configuration and Functions

4.1 Pin Diagram

Figure 4-1 shows the pin locations for the 161-pin FCBGA package. Figure 4-2, Figure 4-3, Figure 4-4, and Figure 4-5 show the same pins, but split into four quadrants.

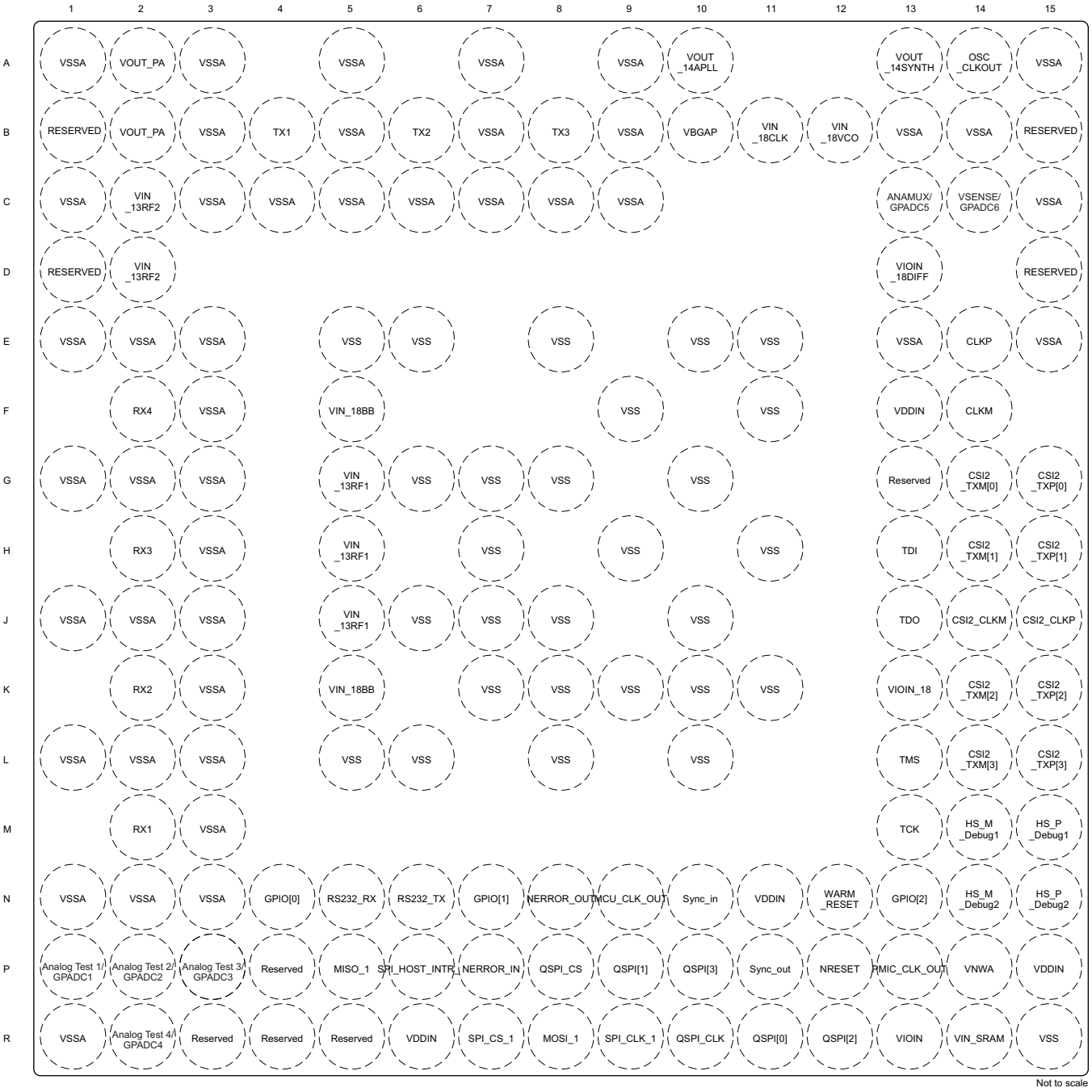


Figure 4-1. Pin Diagram

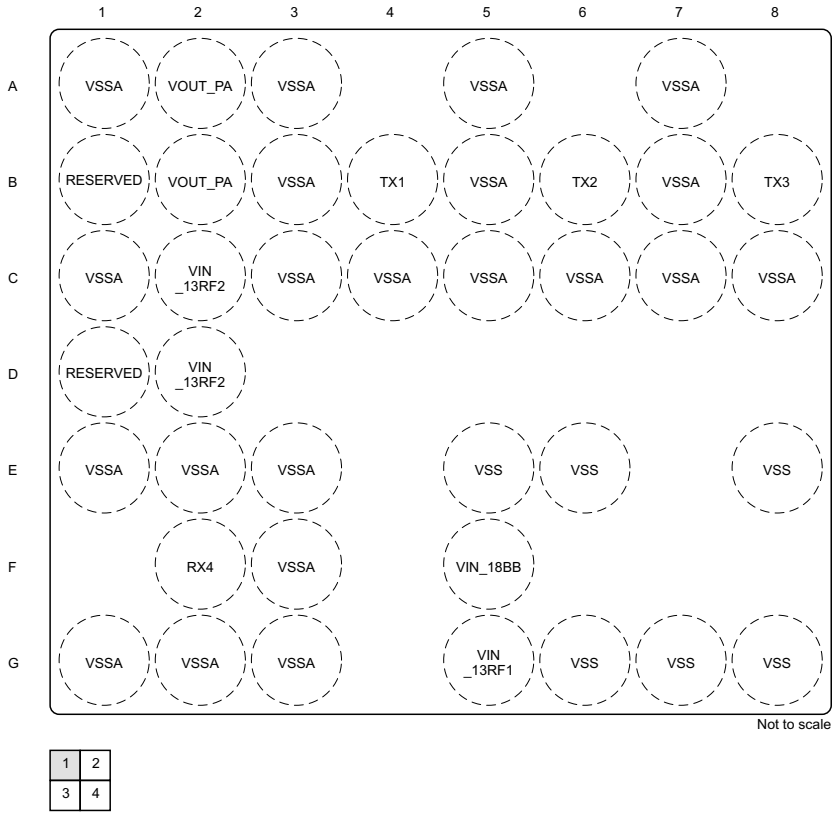


Figure 4-2. Top Left Quadrant

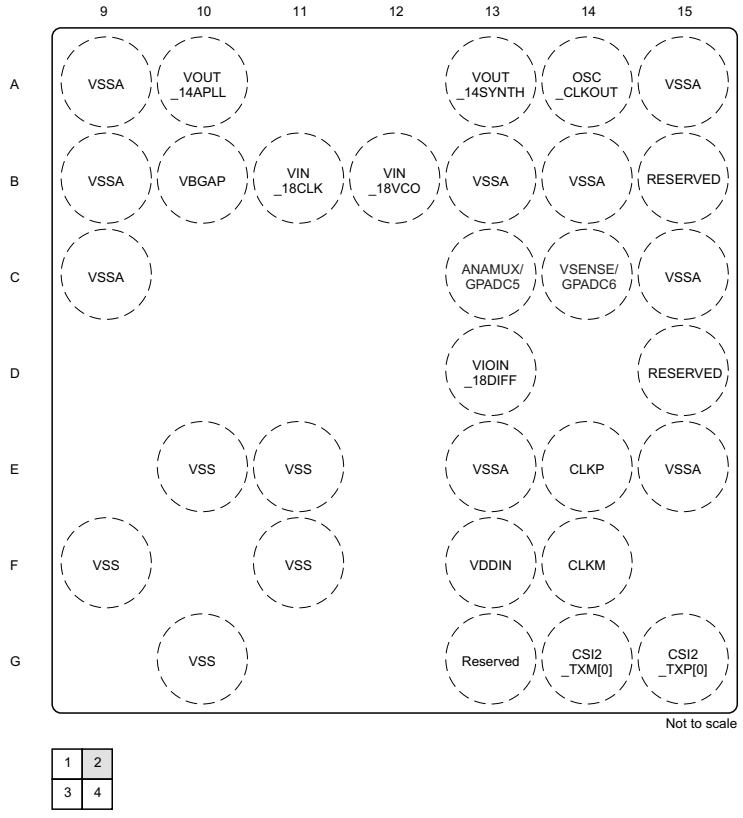


Figure 4-3. Top Right Quadrant

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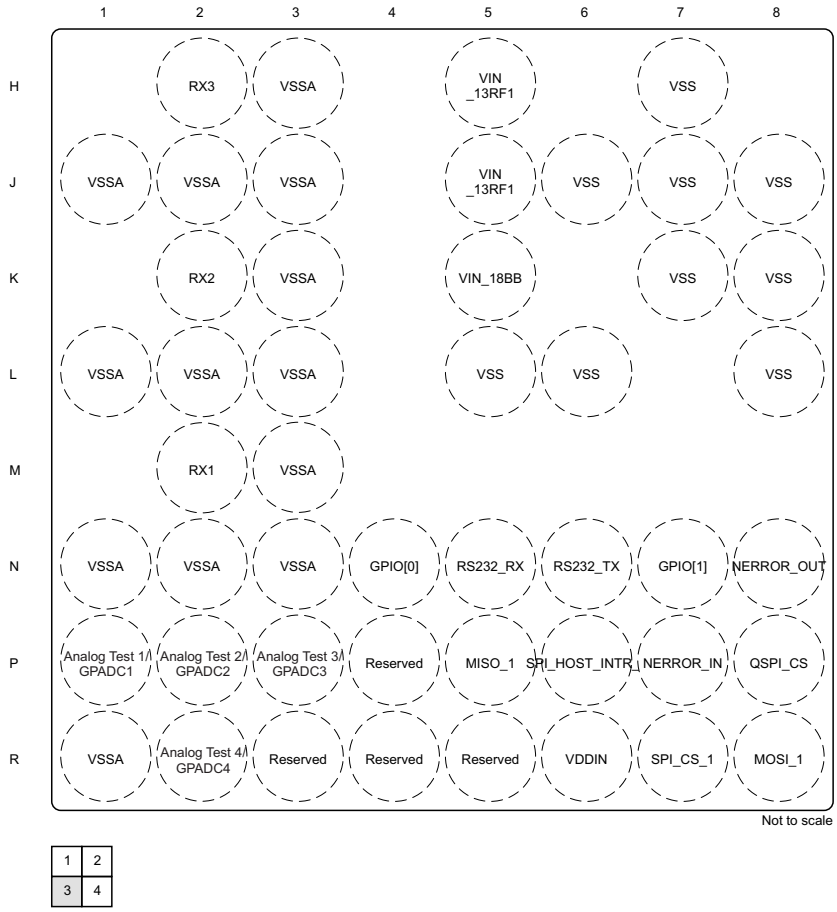


Figure 4-4. Bottom Left Quadrant

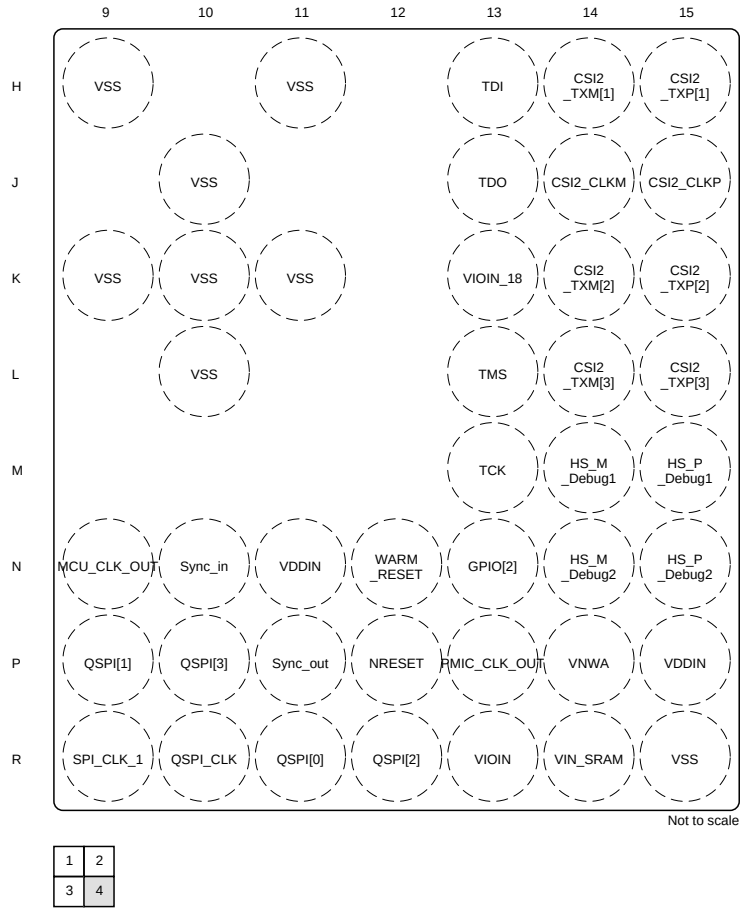


Figure 4-5. Bottom Right Quadrant

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4.2 Signal Descriptions

Table 4-1. Signal Descriptions

FUNCTION	SIGNAL NAME	PIN NUMBER	PIN TYPE	DEFAULT PULL STATUS(1)	DESCRIPTION
Transmitters	TX1	B4	O	—	Single-ended transmitter1 o/p
	TX2	B6	O	—	Single-ended transmitter2 o/p
	TX3	B8	O	—	Single-ended transmitter3 o/p
Receivers	RX1	M2	I	—	Single-ended receiver1 i/p
	RX2	K2	I	—	Single-ended receiver2 i/p
	RX3	H2	I	—	Single-ended receiver3 i/p
	RX4	F2	I	—	Single-ended receiver4 i/p
CSI2 TX/LVDS TX	CSI2_TXP[0]	G15	O	—	Differential data Out – Lane 0
	CSI2_TXM[0]	G14	O	—	
	CSI2_CLKP	J15	O	—	Differential clock Out
	CSI2_CLKM	J14	O	—	
	CSI2_TXP[1]	H15	O	—	Differential data Out – Lane 1
	CSI2_TXM[1]	H14	O	—	
	CSI2_TXP[2]	K15	O	—	Differential data Out – Lane 2
	CSI2_TXM[2]	K14	O	—	
	CSI2_TXP[3]	L15	O	—	Differential data Out – Lane 3
	CSI2_TXM[3]	L14	O	—	
	HS_DEBUG1_P	M15	O	—	Differential debug port 1
	HS_DEBUG1_M	M14	O	—	
	HS_DEBUG2_P	N15	O	—	Differential debug port 2
	HS_DEBUG2_M	N14	O	—	
	RESERVED	B1, B15, D1, D15		—	
Reference clock	OSC_CLKOUT	A14	O	—	Reference clock output from clocking subsystem after cleanup PLL.
System synchronization	SYNC_OUT	P11	O	Pull Down	Low-frequency frame synchronization signal output. Can be used by slave chip in multichip cascading
	SYNC_IN	N10	I	Pull Down	Low-frequency frame synchronization signal input.
SPI control interface from external MCU (default slave mode)	SPI_CS_1	R7	I	Pull Up	SPI chip select
	SPI_CLK_1	R9	I	Pull Down	SPI clock
	MOSI_1	R8	I	Pull Up	SPI data input
	MISO_1	P5	O	Pull Up	SPI data output
	SPI_HOST_INTR_1	P6	O	Pull Down	SPI interrupt to host
	RESERVED	R3, R4, R5, P4		—	
Reset	NRESET	P12	I	Open Drain	Power on reset for chip. Active low
	WARM_RESET	N12	IO	Open Drain	Open-drain fail-safe warm reset signal. Can be driven from PMIC for diagnostic or can be used as status signal that the device is going through reset.
Safety	NERROR_OUT	N8	O	Open Drain	Open-drain fail-safe output signal. Connected to PMIC/Processor/MCU to indicate that some severe criticality fault has happened. Recovery would be through reset.
	NERROR_IN	P7	I	Pull Up	Fail-safe input to the device. Error output from any other device can be concentrated in the error signaling monitor module inside the device and appropriate action can be taken by firmware

(1) Status of PULL structures associated with the IO after device POWER UP.

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Table 4-1. Signal Descriptions (continued)

FUNCTION	SIGNAL NAME	PIN NUMBER	PIN TYPE	DEFAULT PULL STATUS(1)	DESCRIPTION
JTAG	TMS	L13	I	Pull Up	JTAG port for standard boundary scan
	TCK	M13	I	Pull Down	
	TDI	H13	I	Pull Up	
	TDO	J13	O	—	
Reference oscillator	CLKP	E14	I	—	In XTAL mode: Differential port for reference crystal In External clock mode: Single ended input reference clock port (Output CLKM is grounded in this case)
	CLKM	F14	O	—	
Band-gap voltage	VBGAP	B10	O	—	Internal voltage reference 0.9V
Power supply	VDDIN	F13,N11,P15,R6	POW	—	1.2-V digital power supply
	VIN_SRAM	R14	POW	—	1.2-V power rail for internal SRAM
	VNWA	P14	POW	—	1.2-V power rail for SRAM array back bias
	VIOIN	R13	POW	—	I/O supply (3.3-V or 1.8-V): All CMOS I/Os would operate on this supply.
	VIOIN_18	K13	POW	—	1.8-V supply for CMOS IO
	VIN_18CLK	B11	POW	—	1.8-V supply for clock module
	VIOIN_18DIFF	D13	POW	—	1.8-V supply for CSI2 port
	Reserved	G13	POW	—	No connect
	VIN_13RF1	G5,J5,H5	POW	—	1.3-V Analog and RF supply,VIN_13RF1 and VIN_13RF2 could be shorted on the board 1.0-V Analog and RF supply input if RFLDO is bypassed
	VIN_13RF2	C2,D2	POW	—	
	VIN_18BB	K5,F5	POW	—	1.8-V Analog baseband power supply
	VIN_18VCO	B12	POW	—	1.8-V RF VCO supply
	VSS	E5,E6,E8,E10,E11,F9,F11,G6,G7,G8,G10,H7,H9,H11,J6,J7,J8,J10,K7,K8,K9,K10,K11,L5,L6,L8,L10,R15	GND	—	Digital ground
	VSSA	A1,A3,A5,A7,A9,A15,B3,B5,B7,B9,B13,B14,C1,C3,C4,C5,C6,C7,C8,C9,C15,E1,E2,E3,E13,E15,F3,G1,G2,G3,H3,J1,J2,J3,K3,L1,L2,L3,M3,N1,N2,N3,R1	GND	—	Analog ground
Internal LDO output/inputs	VOUT_14APLL	A10	O	—	1.4V internal regulator
	VOUT_14SYNTH	A13	O	—	1.4V internal regulator
	VOUT_PA	A2,B2	O	—	1.0V internal regulator
External clock out	PMIC_CLK_OUT	P13	O	—	Dithered clock input to PMIC
	MCU_CLK_OUT	N9	O	—	Programmable clock given out to external MCU or the processor

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Table 4-1. Signal Descriptions (continued)

FUNCTION	SIGNAL NAME	PIN NUMBER	PIN TYPE	DEFAULT PULL STATUS(1)	DESCRIPTION
General-purpose I/Os	GPIO[0]	N4	IO	Pull Down	General-purpose IO
	GPIO[1]	N7	IO	Pull Down	General-purpose IO
	GPIO[2]	N13	IO	Pull Down	General-purpose IO
QSPI for Serial Flash	QSPI_CS	P8	O	Pull Up	Chip-select output from the device. Device is a master connected to serial flash slave.
	QSPI_CLK	R10	O	Pull Down	Clock output from the device. Device is a master connected to serial flash slave.
	QSPI[0]	R11	IO	Pull Down	Data IN/OUT
	QSPI[1]	P9	IO	Pull Down	Data IN/OUT
	QSPI[2]	R12	IO	Pull Up	Data IN/OUT
	QSPI[3]	P10	IO	Pull Up	Data IN/OUT
Flash programming and RS232 UART	RS232_TX	N6	O	Pull Down	UART pins for programming external flash in preproduction/debug hardware.
	RS232_RX	N5	I	Pull Up	
Test and Debug output for preproduction phase. Can be pinned out on production hardware for field debug	Analog Test1 / GPADC1	P1	IO	—	GP ADC channel 1
	Analog Test2 / GPADC2	P2	IO	—	GP ADC channel 2
	Analog Test3 / GPADC3	P3	IO	—	GP ADC channel 3
	Analog Test4 / GPADC4	R2	IO	—	GP ADC channel 4
	ANAMUX / GPADC5	C13	IO	—	GP ADC channel 5
	VSENSE / GPADC6	C14	IO	—	GP ADC channel 6

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4.3 Pin Multiplexing

Table 4-2. Pin Multiplexing

REGISTER ADDRESS(1)	PIN NAME	PIN	DIGITAL PIN MUX CONFIG VALUE [Bits3:0]	FUNCTION			PAD STATE nReset = 0 [ASSERTED]	
				SIGNAL NAME	SIGNAL DESCRIPTION	SIGNAL TYPE	STATE	INTERNAL WEAK PULL STATE
EA00h	GPIO_12	P6	0	GPIO_12	General Purpose IO	IO	Hi-Z	Weak Pull Down
			1	SPI_HOST1_INTR	General Purpose IO [IWR14xx]	O		
EA04h	GPIO_0	N4	0	GPIO_13	General Purpose IO	IO	Hi-Z	Weak Pull Down
			1	GPIO_0	General Purpose IO	IO		
			2	PMIC_CLKOUT	Dithered Clock Output for PMIC	O		
EA08h	GPIO_1	N7	0	GPIO_16	General Purpose IO	IO	Hi-Z	Weak Pull Down
			1	GPIO_1	General Purpose IO	IO		
			2	SYNC_OUT	Low Frequency Synchronization Signal output	O		
EA0Ch	MOSI_1	R8	0	GPIO_19	General Purpose IO	IO	Hi-Z	Weak Pull Up
			1	MOSI_1	SPI Channel#1 Data Input	IO		
			2	CAN_RX	CAN Interface	I		
EA10h	MISO_1	P5	0	GPIO_20	General Purpose IO	IO	Hi-Z	Weak Pull Up
			1	MISO_1	SPI Channel#1 Data Output	IO		
			2	CAN_TX	CAN Interface	O		
EA14h	SPI_CLK_1	R9	0	GPIO_3	General Purpose IO	IO	Hi-Z	Weak Pull Up
			1	SPI_CLK_1	SPI Channel#1 Clock	IO		
				RCOSC_CLK		O		
EA18h	SPI_CS_1	R7	0	GPIO_30	General Purpose IO	IO	Hi-Z	Weak Pull Up
			1	SPI_CS_1	SPI Channel#1 Chip Select	IO		
				RCOSC_CLK		O		
EA1Ch	MOSI_2	R3	0	GPIO_21	General Purpose IO	IO	Hi-Z	
			1	MOSI_2	SPI Channel#2 Data Input	IO		
			2	I2C_SDA	I2C Data	IO		
EA20h	MISO_2	P4	0	GPIO_22	General Purpose IO	IO	Hi-Z	
			1	MISO_2	SPI Channel#2 Data Output	IO		
			2	I2C_SCL	I2C Clock	IO		

(1) Register addresses are of the form FFFF XXXXh, where XXXX is listed here.

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Table 4-2. Pin Multiplexing (continued)

REGISTER ADDRESS(1)	PIN NAME	PIN	DIGITAL PIN MUX CONFIG VALUE [Bits3:0]	FUNCTION			PAD STATE nReset = 0 [ASSERTED]	
				SIGNAL NAME	SIGNAL DESCRIPTION	SIGNAL TYPE	STATE	INTERNAL WEAK PULL STATE
EA24h	SPI_CLK_2	R5	0	GPIO_5	General Purpose IO	IO	Hi-Z	
			1	SPI_CLK_2	SPI Channel#2 Clock	IO		
				MSS_UARTA_RX		IO		
			6	MSS_UARTB_TX	Debug: Firmware Trace	O		
			7	BSS_UART_TX	Debug: Firmware Trace	O		
EA28h	SPI_CS_2	R4	0	GPIO_4	General Purpose IO	IO	Hi-Z	
			1	SPI_CS_2	SPI Channel#2 Chip Select	IO		
				MSS_UARTA_TX		IO		
			6	MSS_UARTB_TX	Debug: Firmware Trace	O		
			7	BSS_UART_TX	Debug: Firmware Trace	O		
EA2Ch	QSPI[0]	R11	0	GPIO_8	General Purpose IO	IO	Hi-Z	Weak Pull Down
			1	QSPI[0]	QSPI Data IN/OUT	IO		
			2	MISO_2	SPI Channel#1 Data Output	IO		
EA30h	QSPI[1]	P9	0	GPIO_9	General Purpose IO	IO	Hi-Z	Weak Pull Down
			1	QSPI[1]	QSPI Data IN/OUT	IO		
			2	MOSI_2	SPI Channel#2 Data Input	IO		
EA34h	QSPI[2]	R12	0	GPIO_10	General Purpose IO	IO	Hi-Z	Weak Pull Down
			1	QSPI[2]	QSPI Data IN/OUT	IO		
EA38h	QSPI[3]	P10	0	GPIO_11	General Purpose IO	IO	Hi-Z	Weak Pull Down
			1	QSPI[3]	QSPI Data IN/OUT	I		
EA3Ch	QSPI_CLK	R10	0	GPIO_7	General Purpose IO	IO	Hi-Z	Weak Pull Down
			1	QSPI_CLK	QSPI Clock output from the device. Device operates as a master with the serial flash being a slave	O		
			2	SPI_CLK_2	SPI Channel#2 Clock	IO		
EA40h	QSPI_CS	P8	0	GPIO_6	General Purpose IO	IO	Hi-Z	Weak Pull Up
			1	QSPI_CS	QSPI Chip Select output from the device. Device operates as a master with the serial flash being a slave	O		
			2	SPI_CS_2	SPI Channel#2 Chip Select	IO		

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Table 4-2. Pin Multiplexing (continued)

REGISTER ADDRESS[1]	PIN NAME	PIN	DIGITAL PIN MUX CONFIG VALUE [Bits3:0]	FUNCTION			PAD STATE nReset = 0 [ASSERTED]	
				SIGNAL NAME	SIGNAL DESCRIPTION	SIGNAL TYPE	STATE	INTERNAL WEAK PULL STATE
	NERROR_IN	P7		NERROR_IN	Failsafe input to the device. Nerror output from any other device can be concentrated in the error signaling monitor module inside the device and appropriate action can be taken by Firmware	I	Hi-Z	
	WARM_RESET	N12		WARM_RESET	Open drain fail safe warm reset signal. Can be driven from PMIC for diagnostic or can be used as status signal that the device is going through reset.	IO	Hi-Z Input	Open Drain
	NERROR_OUT	N8		NERROR_OUT	Open drain fail safe output signal. Connected to PMIC/Processor/MCU to indicate that some severe criticality fault has happened. Recovery would be through reset.	O	Hi-Z	Open Drain
EA50h	TCK	M13	0	GPIO_17	General Purpose IO	IO	Hi-Z	Weak Pull Down
			1	TCK	JTAG Clock	I		
			2	MSS_UARTB_TX	Debug: Firmware Trace	O		
			6	BSS_UART_RX	Debug: Firmware Trace	I		
EA54h	TMS	L13	0	GPIO_18	General Purpose IO	IO	Hi-Z	Weak Pull Up
			1	TMS	JTAG Test Mode Select	IO		
			2	BSS_UART_TX	Debug: Firmware Trace	O		
EA58h	TDI	H13	0	GPIO_23	General Purpose IO	IO	Hi-Z	Weak Pull Up
			1	TDI	JTAG Test Data In	I		
				MSS_UARTA_RX		IO		
EA5Ch	TDO	J13	0	GPIO_24	General Purpose IO	IO	Hi-Z	
			1	TDO	JTAG Test Data Out	O		
				MSS_UARTA_TX		IO		
			6	MSS_UARTB_TX	Debug: Firmware Trace	O		
			7	BSS_UART_TX	Debug: Firmware Trace	O		
				SOP0	Sense On Power [Reset] Line Impacts boot mode	I		

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Table 4-2. Pin Multiplexing (continued)

REGISTER ADDRESS(1)	PIN NAME	PIN	DIGITAL PIN MUX CONFIG VALUE [Bits3:0]	FUNCTION			PAD STATE nReset = 0 [ASSERTED]	
				SIGNAL NAME	SIGNAL DESCRIPTION	SIGNAL TYPE	STATE	INTERNAL WEAK PULL STATE
EA60h	MCU_CLKOUT	N9	0	GPIO_25	General Purpose IO	IO	Hi-Z	Weak Pull Down
			1	MCU_CLKOUT	Programmable clock given out to external MCU or the processor	O		
			10	BSS_UART_RX	Debug: Firmware Trace	I		
EA64h	GPIO_2	N13	0	GPIO_26	General Purpose IO	IO	Hi-Z	Weak Pull Down
			1	GPIO_2	General Purpose IO	IO		
			7	MSS_UARTB_TX	Debug: Firmware Trace	O		
			8	BSS_UART_TX	Debug: Firmware Trace	O		
			9	SYNC_OUT	Low frequency Synchronization signal output	O		
			10	PMIC_CLKOUT	Dithered clock input to PMIC	O		
EA68h	PMIC_CLKOUT	P13	0	GPIO_27	General Purpose IO	IO	Hi-Z	Weak Pull Down
			1	PMIC_CLKOUT	Dithered Clock Output for PMIC	O		
				SOP2	Sense On Power [Reset] Line Impacts boot mode	I		
EA6Ch	SYNC_IN	N10	0	GPIO_28	General Purpose IO	IO	Hi-Z	Weak Pull Down
			1	SYNC_IN	Low frequency Synchronization signal input	I		
			6	MSS_UARTB_RX	Debug: Firmware Trace	I		
EA70h	SYNC_OUT	P11	0	GPIO_29	General Purpose IO	IO	Hi-Z	Weak Pull Down
			1	SYNC_OUT	Low frequency Synchronization signal output	O		
				RCOSC_CLK		O		
				SOP1	Sense On Power [Reset] Line Impacts boot mode	I		
EA74h	RS232_RX	N5	0	GPIO_15	General Purpose IO	IO	Hi-Z	Weak Pull Up
			1	RS232_RX	Debug: Firmware load to RAM	IO		
			2	MSS_UARTA_RX	FLASH Programming Bootloader Controlled	I		
			6	BSS_UART_TX	Debug: Firmware Trace	O		
			7	MSS_UARTB_RX	Debug: Firmware Trace	I		

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Table 4-2. Pin Multiplexing (continued)

REGISTER ADDRESS(1)	PIN NAME	PIN	DIGITAL PIN MUX CONFIG VALUE [Bits3:0]	FUNCTION			PAD STATE nReset = 0 [ASSERTED]	
				SIGNAL NAME	SIGNAL DESCRIPTION	SIGNAL TYPE	STATE	INTERNAL WEAK PULL STATE
EA78h	RS232_TX	N6	0	GPIO_14	General Purpose IO	IO		
			1	RS232_TX	Debug: Firmware load to RAM	IO		
			5	MSS_UARTA_TX	FLASH Programming Bootloader Controlled	O		
			6	MSS_UARTB_TX	Debug: Firmware Trace	O		
			7	BSS_UART_TX	Debug: Firmware Trace	O		

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5 Specifications

5.1 Absolute Maximum Ratings(1)(2)

over operating Tj temperature range (unless otherwise noted)

PARAMETERS		MIN	MAX	UNIT
VDDIN	1.2 V digital power supply	–0.5	1.4	V
VIN_SRAM	1.2 V power rail for internal SRAM	–0.5	1.4	V
VNWA	1.2 V power rail for SRAM array back bias	–0.5	1.4	V
VIOIN	I/O supply (3.3 V or 1.8 V): All CMOS I/Os would operate on this supply.	–0.5	3.8	V
VIOIN_18	1.8 V supply for CMOS IO	–0.5	2	V
VIN_18CLK	1.8 V supply for clock module	–0.5	2	V
VIOIN_18DIFF	1.8 V supply for CSI2 port	–0.5	2	V
VIN_13RF1	1.3 V Analog and RF supply, VIN_13RF1 and VIN_13RF2 could be shorted on the board.	–0.5	1.45	V
VIN_13RF2				
VIN_13RF1	1-V Internal LDO bypass mode. Device supports mode where external Power Management block can supply 1 V on VIN_13RF1 and VIN_13RF2 rails. In this configuration, the internal LDO of the device would be kept bypassed.	–0.5	1.4	V
VIN_13RF2				
VIN_18BB	1.8-V Analog baseband power supply	–0.5	2	V
VIN_18VCO supply	1.8-V RF VCO supply	–0.5	2	V
Input and output voltage range	Dual-voltage LVCMOS inputs, 3.3 V or 1.8 V (Steady State)	–0.3V	VIOIN + 0.3	V
	Dual-voltage LVCMOS inputs, operated at 3.3 V/1.8 V (Transient Overshoot/Undershoot) or external oscillator input		VIOIN + 20% up to 20% of signal period	
CLKP, CLKM	Input ports for reference crystal	–0.5	2	V
Clamp current	Input or Output Voltages 0.3 V above or below their respective power rails. Limit clamp current that flows through the internal diode protection cells of the I/O.	–20	20	mA
T_J	Operating junction temperature range	–40	105	ºC
T_{STG}	Storage temperature range after soldered onto PC board	–55	150	ºC

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to V_{SS}, unless otherwise noted.

5.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM)		±2000	V
		Charged-device model (CDM)	All other pins	±500	
			Corner pins	±750	

5.3 Power-On Hours (POH)(1)

JUNCTION TEMPERATURE (T_j)	OPERATING CONDITION	NOMINAL CVDD VOLTAGE (V)	POWER-ON HOURS [POH] (HOURS)
90% at 85ºC T_j 10% at 105ºC T_j	50% duty cycle	1.2	80,000
100% at 85ºC T_j			100,000

(1) This information is provided solely for your convenience and does not extend or modify the warranty provided under TI's standard terms and conditions for TI semiconductor products.

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5.4 Recommended Operating Conditions

Tjunction temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
VDDIN	1.2 V digital power supply	1.14	1.2	1.32	V
VIN_SRAM	1.2 V power rail for internal SRAM	1.14	1.2	1.32	V
VNWA	1.2 V power rail for SRAM array back bias	1.14	1.2	1.32	V
VIOIN	I/O supply (3.3 V)	3.15	3.3	3.45	V
	I/O supply (1.8 V)	1.71	1.8	1.89	
VIOIN_18	1.8 V supply for CMOS IO	1.71	1.8	1.9	V
VIN_18CLK	1.8 V supply for clock module	1.71	1.8	1.9	V
VIOIN_18DIFF	1.8 V supply for CSI2 port	1.71	1.8	1.9	V
VIN_13RF1	1.3 V Analog and RF supply. VIN_13RF1 and VIN_13RF2 could be shorted on the board	1.23	1.3	1.36	V
VIN_13RF2					
VIN_13RF1 (1-V Internal LDO bypass mode)	Device supports mode where external Power Management block can supply 1 V on VIN_13RF1 and VIN_13RF2 rails. In this configuration, the internal LDO of the device would be kept bypassed.	0.95	1	1.05	V
VIN_13RF2 (1-V Internal LDO bypass mode)					
VIN18BB	1.8-V Analog baseband power supply	1.71	1.8	1.9	V
VIN_18VCO	1.8V RF VCO supply	1.71	1.8	1.9	V
V_{IH}	Voltage Input High (1.8 V mode)	1.17			V
	Voltage Input High (3.3 V mode)	2.25			
V_{IL}	Voltage Input Low (1.8 V mode)			0.3*VIOIN	V
	Voltage Input Low (3.3 V mode)			0.62	
V_{OH}	High-level output threshold (I_{OH} = 6 mA) (1.8V)	85%*VIOIN			mV
	High-level output threshold (I_{OH} = 6 mA) (3.3V)	VIOIN – 450mV			
V_{OL}	Low-level output threshold (I_{OL} = 6 mA)			450	mV
NRESET SOP[2:0]	V_{IL} (1.8V Mode)			0.2	V
	V_{IH} (1.8V Mode)	0.96			
	V_{IL} (3.3V Mode)			0.3	
	V_{IH} (3.3V Mode)	1.57			

5.5 Power Supply Specifications

Table 5-1 describes the four rails from an external power supply block of the IWR1443 device.

Table 5-1. Power Supply Rails Characteristics

SUPPLY	DEVICE BLOCKS POWERED FROM THE SUPPLY	RELEVANT IOS IN THE DEVICE
1.8 V	Synthesizer and APLL VCOs, crystal oscillator, IF Amplifier stages, ADC, LVDS	Input: VIN_18VCO, VIN18CLK, VIN_18BB, VIOIN_18DIFF, VIOIN_18IO LDO Output: VOUT_14SYNTH, VOUT_14APLL
1.3 V (or 1 V in internal LDO bypass mode)	Power Amplifier, Low Noise Amplifier, Mixers and LO Distribution	Input: VIN_13RF2, VIN_13RF1 LDO Output: VOUT_PA
3.3 V (or 1.8 V for 1.8 V I/O mode)	Digital I/Os	Input VIOIN
1.2 V	Core Digital and SRAMs	Input: VDDIN, VIN_SRAM, VNWA

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The 1.3V (1.0V) and 1.8V power supply ripple specifications mentioned in Table 5-2 are defined to meet a target spur level of –105dBc (RF Pin = –15dBm) at the RX. The spur and ripple levels have a dB to dB relationship, for example, a 1dB increase in supply ripple leads to a ~1dB increase in spur level. Values quoted are rms levels for a sinusoidal input applied at the specified frequency.

Table 5-2. Ripple Specifications

FREQUENCY (kHz)	RF RAIL		VCO/IF RAIL
	1.0 V (INTERNAL LDO BYPASS) (μV_{RMS})	1.3 V (μV_{RMS})	1.8 V (μV_{RMS})
137.5	744	648	83
275	4	76	21
550	3	22	11
1100	2	4	6
2200	11	82	13
4400	13	93	19
6600	22	117	29

5.6 Power Consumption Summary

Table 5-3 and Table 5-4 summarize the power consumption at the power terminals.

Table 5-3. Maximum Current Ratings at Power Terminals

PARAMETER	SUPPLY NAME	DESCRIPTION	MIN	TYP	MAX	UNIT
Current consumption	VDDIN, VIN_SRAM, VNWA	Total current drawn by all nodes driven by 1.2V rail			500	mA
	VIN_13RF1, VIN_13RF2	Total current drawn by all nodes driven by 1.3V rail			2000	
	VIOIN_18, VIN_18CLK, VIOIN_18DIFF, VIN_18BB, VIN_18VCO	Total current drawn by all nodes driven by 1.8V rail			850	
	VIOIN	Total current drawn by all nodes driven by 3.3V rail			50	

Table 5-4. Average Power Consumption at Power Terminals

PARAMETER	CONDITION		DESCRIPTION	MIN	TYP	MAX	UNIT
Average power consumption	1.0-V internal LDO bypass mode	1TX, 4RX	Sampling: 16.66 MSps complex Transceiver, 40-ms frame time, 512 chirps, 512 samples/chirp, 8.5-µs interchirp time (50% duty cycle) Data Port: MIPI-CSI-2		1.73		W
		2TX, 4RX			1.88		
	1.3-V internal LDO enabled mode	1TX, 4RX			1.92		
		2TX, 4RX			2.1		

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5.7 RF Specification

over recommended operating conditions (unless otherwise noted)

PARAMETER			MIN	TYP	MAX	UNIT
Receiver	Noise figure	76 to 77 GHz		14		dB
		77 to 81 GHz		15		
	1-dB compression point(1)			–8		dBm
	Maximum gain			48		dB
	Gain range			24		dB
	Gain step size			2		dB
	Image Rejection Ratio (IMRR)			30		dB
	IF bandwidth(2)				15	MHz
	A2D sampling rate (real)				37.5	Msps
	A2D sampling rate (complex)				18.75	Msps
	A2D resolution			12		Bits
	Return loss (S11)			–10		dB
	Gain mismatch variation (over temperature)			±0.5		dB
	Phase mismatch variation (over temperature)			±3		°
	In-band IIP2	RX gain = 30dB IF = 1.5, 2 MHz at –12 dBFS		16		dBm
	Out-of-band IIP2	RX gain = 24dB IF = 10 kHz at -10dBm, 1.9 MHz at -30 dBm		24		dBm
	Idle Channel Spurs			–90		dBFS
Transmitter	Output power			12		dBm
	Amplitude noise			–145		dBc/Hz
Clock subsystem	Frequency range		76		81	GHz
	Ramp rate				100	MHz/µs
	Phase noise at 1-MHz offset	76 to 77 GHz		–95		dBc/Hz
		77 to 81 GHz		–93		

(1) 1-dB Compression Point (Out Of Band) is measured by feed a Continuous wave Tone below the lowest HPF cut-off frequency (50 kHz).
(2) The analog IF stages include high-pass filtering, with two independently configurable first-order high-pass corner frequencies. The set of available HPF corners is summarized as follows:

Available HPF Corner Frequencies (kHz)

HPF1	HPF2
175, 235, 350, 700	350, 700, 1400, 2800

The filtering performed by the digital baseband chain is targeted to provide:

- Less than ±0.5 dB pass-band ripple/droop, and
- Better than 60 dB anti-aliasing attenuation for any frequency that can alias back into the pass-band.

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Figure 5-1 shows variations of noise figure and in-band P1dB parameters with respect to receiver gain programmed.

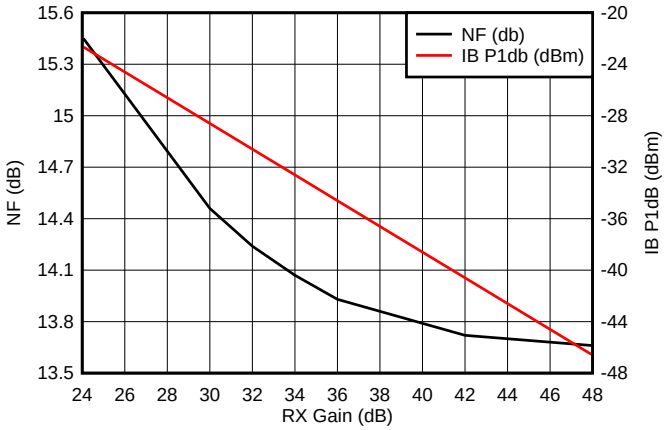


Figure 5-1. Noise Figure, In-band P1dB vs Receiver Gain

5.8 Thermal Resistance Characteristics for FCBGA Package [ABL0161](1)

THERMAL METRICS(2)		°C/W(3) (4)
$R\Theta_{JC}$	Junction-to-case	4.92
$R\Theta_{JB}$	Junction-to-board	6.57
$R\Theta_{JA}$	Junction-to-free air	22.3
$R\Theta_{JMA}$	Junction-to-moving air	N/A(1)
Psi_{JT}	Junction-to-package top	4.92
Psi_{JB}	Junction-to-board	6.4

(1) N/A = not applicable
(2) For more information about traditional and new thermal metrics, see *Semiconductor and IC Package Thermal Metrics*.
(3) °C/W = degrees Celsius per watt.
(4) These values are based on a JEDEC-defined 2S2P system (with the exception of the Theta JC [$R\Theta_{JC}$] value, which is based on a JEDEC-defined 1S0P system) and will change based on environment as well as application. For more information, see these EIA/JEDEC standards:
- JESD51-2, *Integrated Circuits Thermal Test Method Environmental Conditions - Natural Convection (Still Air)*
- JESD51-3, *Low Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*
- JESD51-7, *High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*
- JESD51-9, *Test Boards for Area Array Surface Mount Package Thermal Measurements*

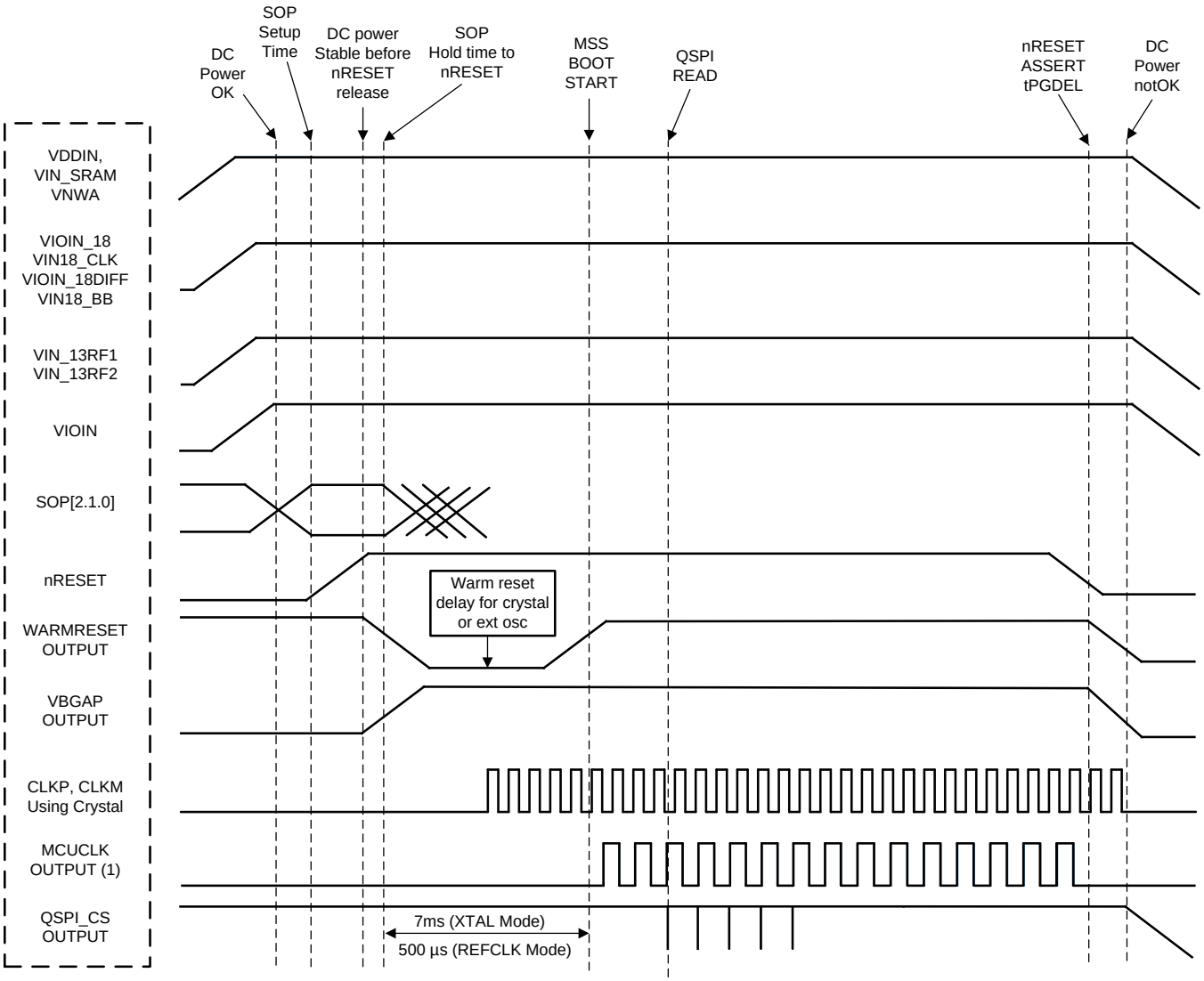
A junction temperature of 105ºC is assumed.

5.9 Timing and Switching Characteristics

5.9.1 Power Supply Sequencing and Reset Timing

The IWR1443 device expects all external voltage rails to be stable before reset is deasserted. Figure 5-2 describes the device wake-up sequence.

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(1) MCU_CLK_OUT in autonomous mode, where IWR1443 application is booted from the serial flash, MCU_CLK_OUT is not enabled by default by the device bootloader.

Figure 5-2. Device Wake-up Sequence

5.9.2 Synchronized Frame Triggering

The IWR1443 device supports a hardware based mechanism to trigger radar frames. An external host can pulse the SYNC_IN signal to start radar frames. The typical time difference between the rising edge of the external pulse and the frame transmission on air (Tlag) is about 160 ns. There is also an additional programmable delay that the user can set to control the frame start time.

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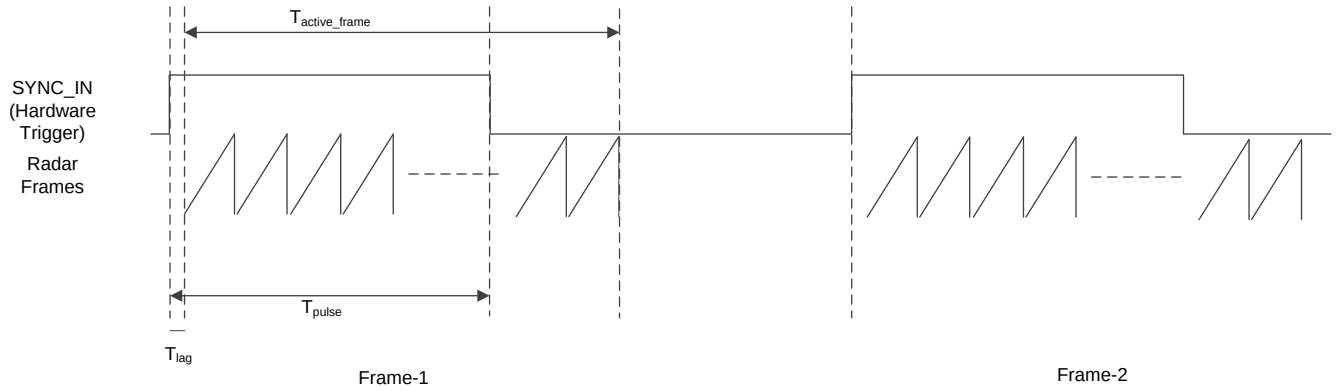


Figure 5-3. Sync In Hardware Trigger

Table 5-5. Frame Trigger Timing

PARAMETER	DESCRIPTION	MIN	MAX	UNIT
T_{active_frame}	Active frame duration	User defined		ns
T_{pulse}		25	< T_{active_frame}	

5.9.3 Input Clocks and Oscillators

5.9.3.1 Clock Specifications

An external crystal is connected to the device pins. Figure 5-4 shows the crystal implementation.

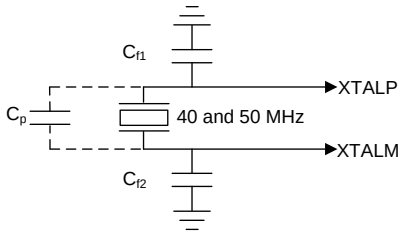


Figure 5-4. Crystal Implementation

NOTE

The load capacitors, C_{f1} and C_{f2} in Figure 5-4, should be chosen such that Equation 1 is satisfied. C_L in the equation is the load specified by the crystal manufacturer. All discrete components used to implement the oscillator circuit should be placed as close as possible to the associated oscillator CLKP and CLKM pins.Note that Cf1 and Cf2 include the parasitic capacitances due to PCB routing.

$$C_L = C_{f1} \times \frac{C_{f2}}{C_{f1} + C_{f2}} + C_P \quad (1)$$

Table 5-6 lists the electrical characteristics of the clock crystal.

Table 5-6. Crystal Electrical Characteristics (Oscillator Mode)

NAME	DESCRIPTION	MIN	TYP	MAX	UNIT
f_P	Parallel resonance crystal frequency		40		MHz
C_L	Crystal load capacitance	5	8	12	pF
ESR	Crystal ESR			50	Ω
Temperature range	Expected temperature range of operation	–40		105	ºC
Frequency tolerance	Crystal frequency tolerance (1) (2) (3)	–50		50	ppm
Drive level			50	200	µW

(1) The crystal manufacturer's specification must satisfy this requirement.
(2) Includes initial tolerance of the crystal, drift over temperature, aging and frequency pulling due to incorrect load capacitance.
(3) Crystal tolerance affects radar sensor accuracy.

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In the case where an external clock is used as the clock resource, the signal is fed to the CLKP pin only; CLKM is grounded. The phase noise requirement is very important when a 40-MHz clock is fed externally. Table 5-7 lists the electrical characteristics of the external clock signal.

Table 5-7. External Clock Mode Specifications

PARAMETER		SPECIFICATION			UNIT
		MIN	TYP	MAX	
Input Clock: External AC-coupled sine wave or DC-coupled square wave Phase Noise referred to 40 MHz	Frequency		40		MHz
	AC-Amplitude	700		1200	mV (pp)
	Phase Noise at 1 kHz			–132	dBc/Hz
	Phase Noise at 10 kHz			–143	dBc/Hz
	Phase Noise at 100 kHz			–152	dBc/Hz
	Phase Noise at 1 MHz			–153	dBc/Hz
	Duty Cycle	35		65	%
	Freq Tolerance	–50		50	ppm

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5.9.4 Multibuffered / Standard Serial Peripheral Interface (MibSPI)

5.9.4.1 Peripheral Description

The MibSPI/SPI is a high-speed synchronous serial input/output port that allows a serial bit stream of programmed length (2 to 16 bits) to be shifted into and out of the device at a programmed bit-transfer rate. The MibSPI/SPI is normally used for communication between the microcontroller and external peripherals or another microcontroller.

Standard and MibSPI modules have the following features:

- 16-bit shift register
- Receive buffer register
- 8-bit baud clock generator
- SPICLK can be internally-generated (master mode) or received from an external clock source (slave mode)
- Each word transferred can have a unique format.
- SPI I/Os not used in the communication can be used as digital input/output signals

5.9.4.2 MibSPI Transmit and Receive RAM Organization

The Multibuffer RAM is comprised of 256 buffers. Each entry in the Multibuffer RAM consists of 4 parts: a 16-bit transmit field, a 16-bit receive field, a 16-bit control field and a 16-bit status field. The Multibuffer RAM can be partitioned into multiple transfer group with variable number of buffers each.

Table 5-9 to assume the operating conditions stated in Table 5-8.

Table 5-8. SPI Timing Conditions

		MIN	TYP	MAX	UNIT
Input Conditions					
t_R	Input rise time	1		3	ns
t_F	Input fall time	1		3	ns
Output Conditions					
C_{LOAD}	Output load capacitance	2		15	pF

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Table 5-9. SPI Master Mode Switching Parameters (CLOCK PHASE = 0, SPICLK = output, SPISIMO = output, and SPISOMI = input)(1)(2)(3)

NO.	PARAMETER			MIN	TYP	MAX	UNIT
1	$t_{c(SPC)M}$	Cycle time, SPICLK(4)		25		$256t_{c(VCLK)}$	ns
2(4)	$t_{w(SPCH)M}$	Pulse duration, SPICLK high (clock polarity = 0)		$0.5t_{c(SPC)M} - 4$		$0.5t_{c(SPC)M} + 4$	ns
	$t_{w(SPCL)M}$	Pulse duration, SPICLK low (clock polarity = 1)		$0.5t_{c(SPC)M} - 4$		$0.5t_{c(SPC)M} + 4$	
3(4)	$t_{w(SPCL)M}$	Pulse duration, SPICLK low (clock polarity = 0)		$0.5t_{c(SPC)M} - 4$		$0.5t_{c(SPC)M} + 4$	ns
	$t_{w(SPCH)M}$	Pulse duration, SPICLK high (clock polarity = 1)		$0.5t_{c(SPC)M} - 4$		$0.5t_{c(SPC)M} + 4$	
4(4)	$t_{d(SPCH-SIMO)M}$	Delay time, SPISIMO valid before SPICLK low, (clock polarity = 0)		$0.5t_{c(SPC)M} - 3$			ns
	$t_{d(SPCL-SIMO)M}$	Delay time, SPISIMO valid before SPICLK high, (clock polarity = 1)		$0.5t_{c(SPC)M} - 3$			
5(4)	$t_{v(SPCL-SIMO)M}$	Valid time, SPISIMO data valid after SPICLK low, (clock polarity = 0)		$0.5t_{c(SPC)M} - 10.5$			ns
	$t_{v(SPCH-SIMO)M}$	Valid time, SPISIMO data valid after SPICLK high, (clock polarity = 1)		$0.5t_{c(SPC)M} - 10.5$			
6(5)	$t_{C2TDELAY}$	Setup time CS active until SPICLK high (clock polarity = 0)	CSHOLD = 0	$(C2TDELAY+2)*t_{c(VCLK)} - 7.5$		$(C2TDELAY+2) * t_{c(VCLK)} + 7$	ns
			CSHOLD = 1	$(C2TDELAY+3) * t_{c(VCLK)} - 7.5$		$(C2TDELAY+3) * t_{c(VCLK)} + 7$	
		Setup time CS active until SPICLK low (clock polarity = 1)	CSHOLD = 0	$(C2TDELAY+2)*t_{c(VCLK)} - 7.5$		$(C2TDELAY+2) * t_{c(VCLK)} + 7$	
			CSHOLD = 1	$(C2TDELAY+3) * t_{c(VCLK)} - 7.5$		$(C2TDELAY+3) * t_{c(VCLK)} + 7$	
7(5)	$t_{T2CDELAY}$	Hold time, SPICLK low until CS inactive (clock polarity = 0)		$0.5*t_{c(SPC)M} + (T2CDELAY + 1) *t_{c(VCLK)} - 7$		$0.5*t_{c(SPC)M} + (T2CDELAY + 1) * t_{c(VCLK)} + 7.5$	ns
		Hold time, SPICLK high until CS inactive (clock polarity = 1)		$0.5*t_{c(SPC)M} + (T2CDELAY + 1) *t_{c(VCLK)} - 7$		$0.5*t_{c(SPC)M} + (T2CDELAY + 1) * t_{c(VCLK)} + 7.5$	
8(4)	$t_{su(SOMI-SPCL)M}$	Setup time, SPISOMI before SPICLK low (clock polarity = 0)		5			ns
	$t_{su(SOMI-SPCH)M}$	Setup time, SPISOMI before SPICLK high (clock polarity = 1)		5			
9(4)	$t_{h(SPCL-SOMI)M}$	Hold time, SPISOMI data valid after SPICLK low (clock polarity = 0)		3			ns
	$t_{h(SPCH-SOMI)M}$	Hold time, SPISOMI data valid after SPICLK high (clock polarity = 1)		3			

(1) The MASTER bit (SPIGCRx.0) is set and the CLOCK PHASE bit (SPIFMTx.16) is cleared (where x= 0 or 1).
(2) $t_{c(MSS_VCLK)}$ = master subsystem clock time = 1 / $f_{(MSS_VCLK)}$. For more details, see the Technical Reference Manual.
(3) When the SPI is in Master mode, the following must be true: For PS values from 1 to 255: $t_{c(SPC)M} \geq (PS + 1)t_{c(MSS_VCLK)} \geq 25ns$, where PS is the prescale value set in the SPIFMTx.[15:8] register bits. For PS values of 0: $t_{c(SPC)M} = 2t_{c(MSS_VCLK)} \geq 25ns$.
(4) The active edge of the SPICLK signal referenced is controlled by the CLOCK POLARITY bit (SPIFMTx.17).
(5) C2TDELAY and T2CDELAY is programmed in the SPIDELAY register

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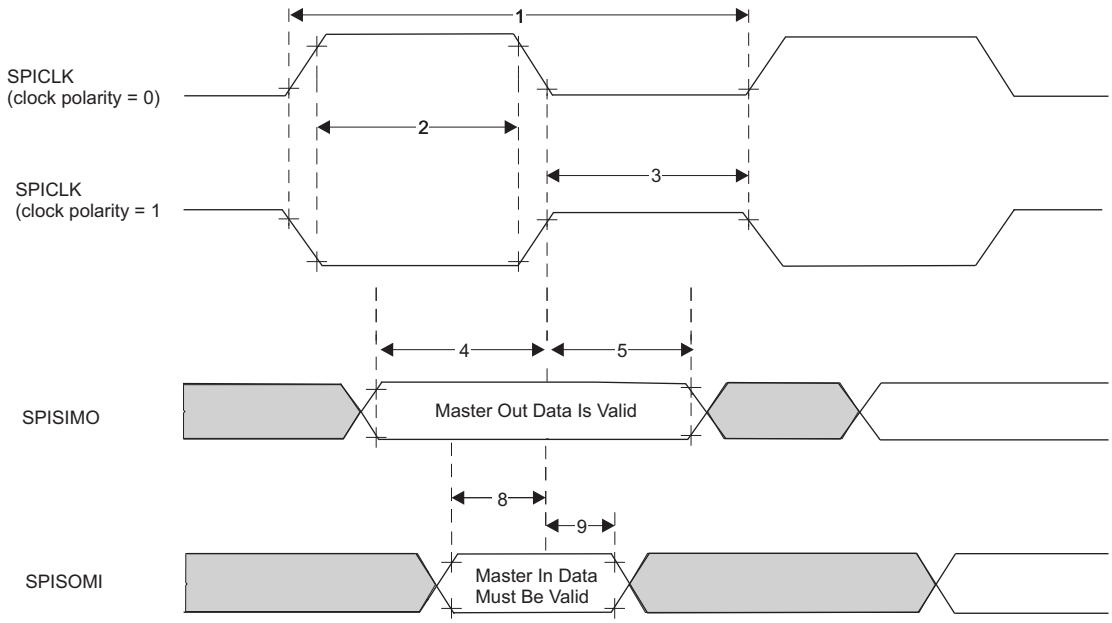


Figure 5-5. SPI Master Mode External Timing (CLOCK PHASE = 0)

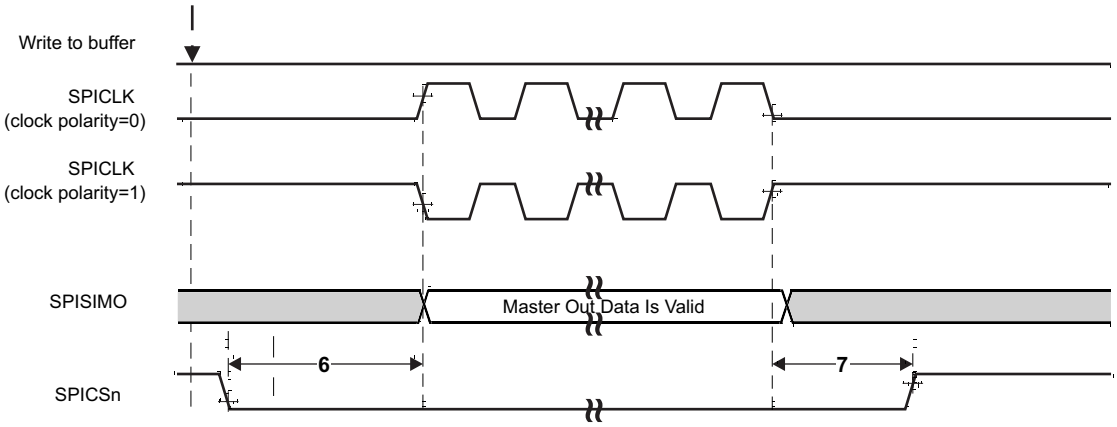


Figure 5-6. SPI Master Mode Chip Select Timing (CLOCK PHASE = 0)

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Table 5-10. SPI Master Mode Switching Parameters (CLOCK PHASE = 1, SPICLK = output, SPISIMO = output, and SPISOMI = input)(1)(2)(3)

NO.	PARAMETER			MIN	TYP	MAX	UNIT
1	$t_{c(SPC)M}$	Cycle time, SPICLK(4)		25		$256t_{c(VCLK)}$	ns
2(4)	$t_{w(SPCH)M}$	Pulse duration, SPICLK high (clock polarity = 0)		$0.5t_{c(SPC)M} - 4$		$0.5t_{c(SPC)M} + 4$	ns
	$t_{w(SPCL)M}$	Pulse duration, SPICLK low (clock polarity = 1)		$0.5t_{c(SPC)M} - 4$		$0.5t_{c(SPC)M} + 4$	
3(4)	$t_{w(SPCL)M}$	Pulse duration, SPICLK low (clock polarity = 0)		$0.5t_{c(SPC)M} - 4$		$0.5t_{c(SPC)M} + 4$	ns
	$t_{w(SPCH)M}$	Pulse duration, SPICLK high (clock polarity = 1)		$0.5t_{c(SPC)M} - 4$		$0.5t_{c(SPC)M} + 4$	
4(4)	$t_{d(SPCH-SIMO)M}$	Delay time, SPISIMO valid before SPICLK low, (clock polarity = 0)		$0.5t_{c(SPC)M} - 3$			ns
	$t_{d(SPCL-SIMO)M}$	Delay time, SPISIMO valid before SPICLK high, (clock polarity = 1)		$0.5t_{c(SPC)M} - 3$			
5(4)	$t_{v(SPCL-SIMO)M}$	Valid time, SPISIMO data valid after SPICLK low, (clock polarity = 0)		$0.5t_{c(SPC)M} - 10.5$			ns
	$t_{v(SPCH-SIMO)M}$	Valid time, SPISIMO data valid after SPICLK high, (clock polarity = 1)		$0.5t_{c(SPC)M} - 10.5$			
6(5)	$t_{C2TDELAY}$	Setup time CS active until SPICLK high (clock polarity = 0)	CSHOLD = 0	$0.5*t_{c(SPC)M} + (C2TDELAY + 2)*t_{c(VCLK)} - 7$		$0.5*t_{c(SPC)M} + (C2TDELAY+2) * t_{c(VCLK)} + 7.5$	ns
			CSHOLD = 1	$0.5*t_{c(SPC)M} + (C2TDELAY + 2)*t_{c(VCLK)} - 7$		$0.5*t_{c(SPC)M} + (C2TDELAY+2) * t_{c(VCLK)} + 7.5$	
		Setup time CS active until SPICLK low (clock polarity = 1)	CSHOLD = 0	$0.5*t_{c(SPC)M} + (C2TDELAY+2)*t_{c(VCLK)} - 7$		$0.5*t_{c(SPC)M} + (C2TDELAY+2) * t_{c(VCLK)} + 7.5$	
			CSHOLD = 1	$0.5*t_{c(SPC)M} + (C2TDELAY+3)*t_{c(VCLK)} - 7$		$0.5*t_{c(SPC)M} + (C2TDELAY+3) * t_{c(VCLK)} + 7.5$	
7(5)	$t_{T2CDELAY}$	Hold time, SPICLK low until CS inactive (clock polarity = 0)		$(T2CDELAY + 1) *t_{c(VCLK)} - 7.5$		$(T2CDELAY + 1) *t_{c(VCLK)} + 7$	ns
		Hold time, SPICLK high until CS inactive (clock polarity = 1)		$(T2CDELAY + 1) *t_{c(VCLK)} - 7.5$		$(T2CDELAY + 1) *t_{c(VCLK)} + 7$	
8(4)	$t_{su(SOMI-SPCL)M}$	Setup time, SPISOMI before SPICLK low (clock polarity = 0)		5			ns
	$t_{su(SOMI-SPCH)M}$	Setup time, SPISOMI before SPICLK high (clock polarity = 1)		5			
9(4)	$t_{h(SPCL-SOMI)M}$	Hold time, SPISOMI data valid after SPICLK low (clock polarity = 0)		3			ns
	$t_{h(SPCH-SOMI)M}$	Hold time, SPISOMI data valid after SPICLK high (clock polarity = 1)		3			

(1) The MASTER bit (SPIGCRx.0) is set and the CLOCK PHASE bit (SPIFMTx.16) is set (where x = 0 or 1).
(2) $t_{c(MSS_VCLK)}$ = master subsystem clock time = 1 / $f_{(MSS_VCLK)}$. For more details, see the Technical Reference Manual.
(3) When the SPI is in Master mode, the following must be true: For PS values from 1 to 255: $t_{c(SPC)M} \geq (PS +1)t_{c(MSS_VCLK)} \geq 25$ ns, where PS is the prescale value set in the SPIFMTx.[15:8] register bits. For PS values of 0: $t_{c(SPC)M} = 2t_{c(MSS_VCLK)} \geq 25$ ns.
(4) The active edge of the SPICLK signal referenced is controlled by the CLOCK POLARITY bit (SPIFMTx.17).
(5) C2TDELAY and T2CDELAY is programmed in the SPIDELAY register

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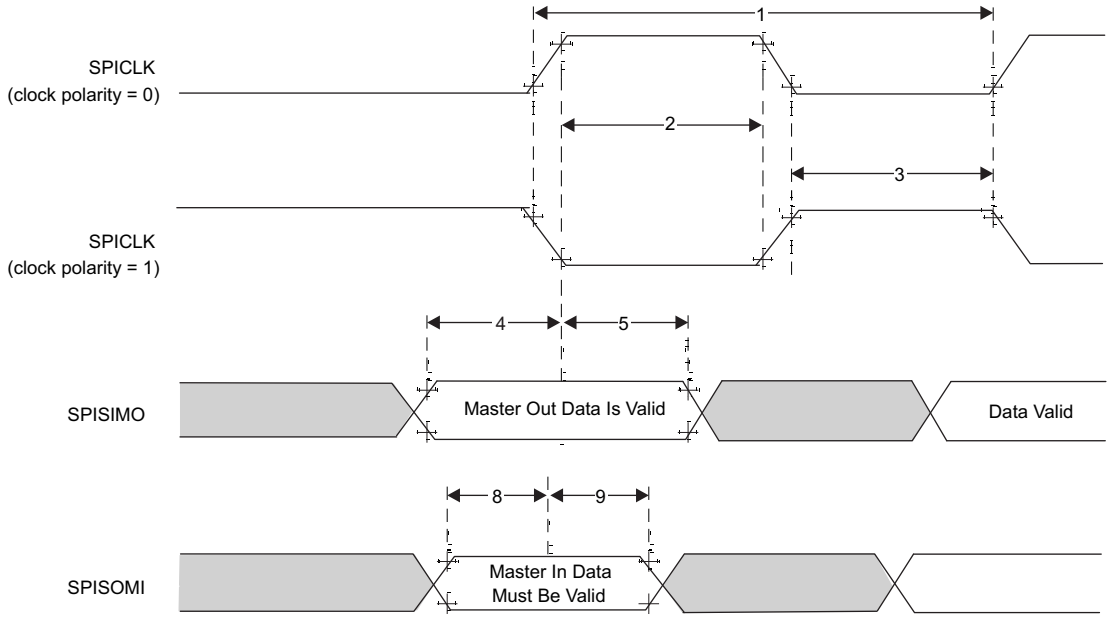


Figure 5-7. SPI Master Mode External Timing (CLOCK PHASE = 1)

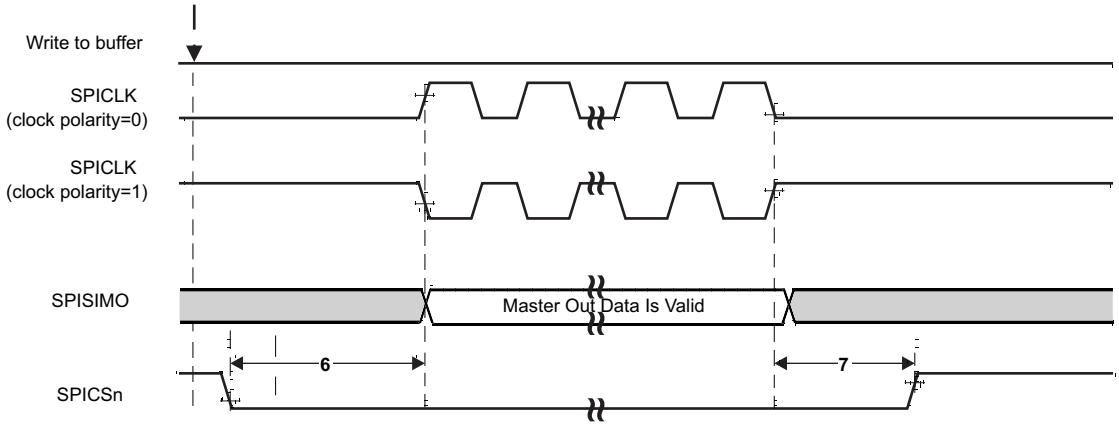


Figure 5-8. SPI Master Mode Chip Select Timing (CLOCK PHASE = 1)

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5.9.4.3 SPI Slave Mode I/O Timings

Table 5-11. SPI Slave Mode Switching Parameters (SPICLK = input, SPISIMO = input, and SPISOMI = output)(1)(2)(3)

NO.	PARAMETER		MIN	TYP	MAX	UNIT
1	$t_{c(SPC)S}$	Cycle time, SPICLK(4)	25			ns
2(5)	$t_{w(SPCH)S}$	Pulse duration, SPICLK high (clock polarity = 0)	10			ns
	$t_{w(SPCL)S}$	Pulse duration, SPICLK low (clock polarity = 1)	10			
3(5)	$t_{w(SPCL)S}$	Pulse duration, SPICLK low (clock polarity = 0)	10			ns
	$t_{w(SPCH)S}$	Pulse duration, SPICLK high (clock polarity = 1)	10			
4(5)	$t_{d(SPCH-SOMI)S}$	Delay time, SPISOMI valid after SPICLK high (clock polarity = 0)			10	ns
	$t_{d(SPCL-SOMI)S}$	Delay time, SPISOMI valid after SPICLK low (clock polarity = 1)			10	
5(5)	$t_{h(SPCH-SOMI)S}$	Hold time, SPISOMI data valid after SPICLK high (clock polarity = 0)	2			ns
	$t_{h(SPCL-SOMI)S}$	Hold time, SPISOMI data valid after SPICLK low (clock polarity = 1)	2			
6(5)	$t_{su(SIMO-SPCL)S}$	Setup time, SPISIMO before SPICLK low (clock polarity = 0; clock phase = 0) OR (clock polarity = 1; clock phase = 1)	3			ns
	$t_{su(SIMO-SPCH)S}$	Setup time, SPISIMO before SPICLK high (clock polarity = 1; clock phase = 0) OR (clock polarity = 0; clock phase = 1)	3			
7(5)	$t_{h(SPCL-SIMO)S}$	Hold time, SPISIMO data valid after SPICLK low (clock polarity = 0; clock phase = 0) OR (clock polarity = 1; clock phase = 1)	1			ns
	$t_{h(SPCL-SIMO)S}$	Hold time, SPISIMO data valid after SPICLK high (clock polarity = 1; clock phase = 0) OR (clock polarity = 0; clock phase = 1)	1			

(1) The MASTER bit (SPIGCRx.0) is cleared (where x = 0 or 1).
(2) The CLOCK PHASE bit (SPIFMTx.16) is either cleared or set for CLOCK PHASE = 0 or CLOCK PHASE = 1 respectively.
(3) $t_{c(MSS_VCLK)}$ = master subsystem clock time = 1 / $f_{(MSS_VCLK)}$. For more details, see the Technical Reference Manual.
(4) When the SPI is in Slave mode, the following must be true: For PS values from 1 to 255: $t_{c(SPC)S} \geq (PS+1)t_{c(MSS_VCLK)} \geq 25$ ns, where PS is the prescale value set in the SPIFMTx.[15:8] register bits.For PS values of 0: $t_{c(SPC)S} = 2t_{c(MSS_VCLK)} \geq 25$ ns.
(5) The active edge of the SPICLK signal referenced is controlled by the CLOCK POLARITY bit (SPIFMTx.17).

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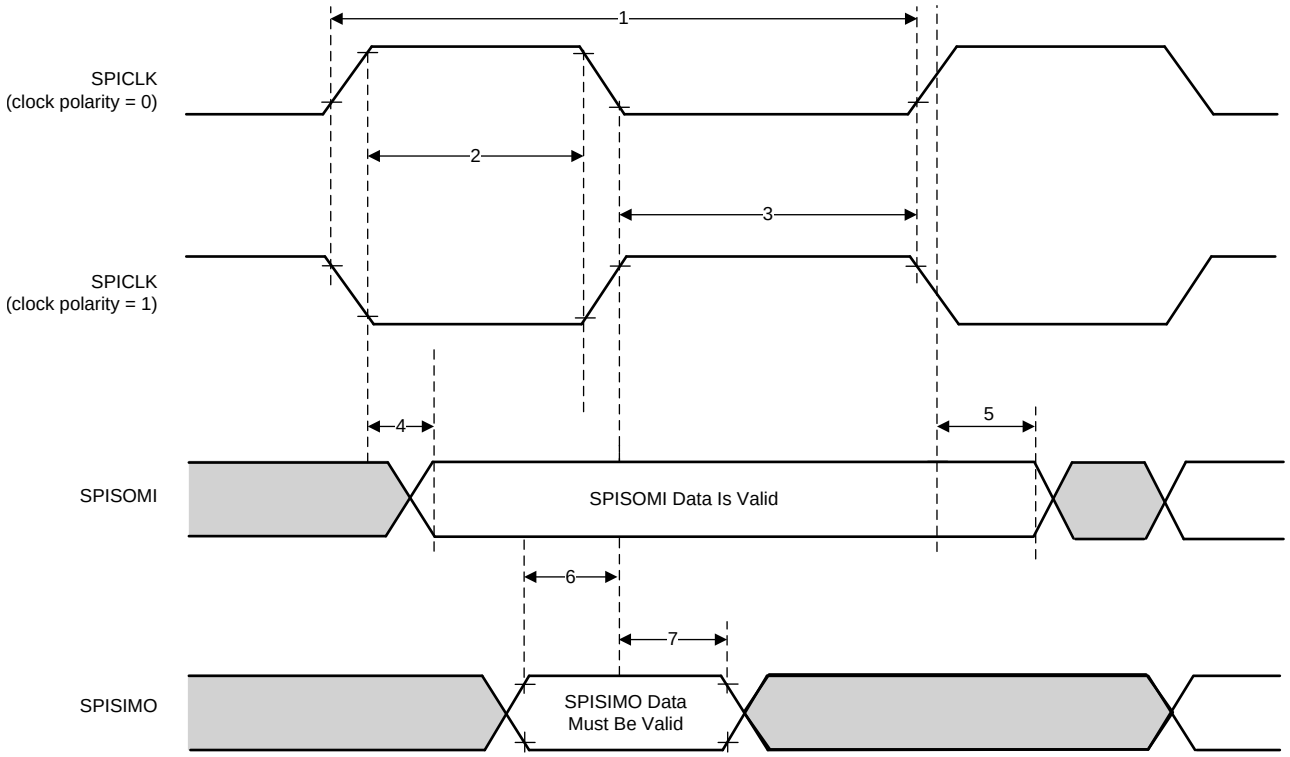


Figure 5-9. SPI Slave Mode External Timing (CLOCK PHASE = 0)

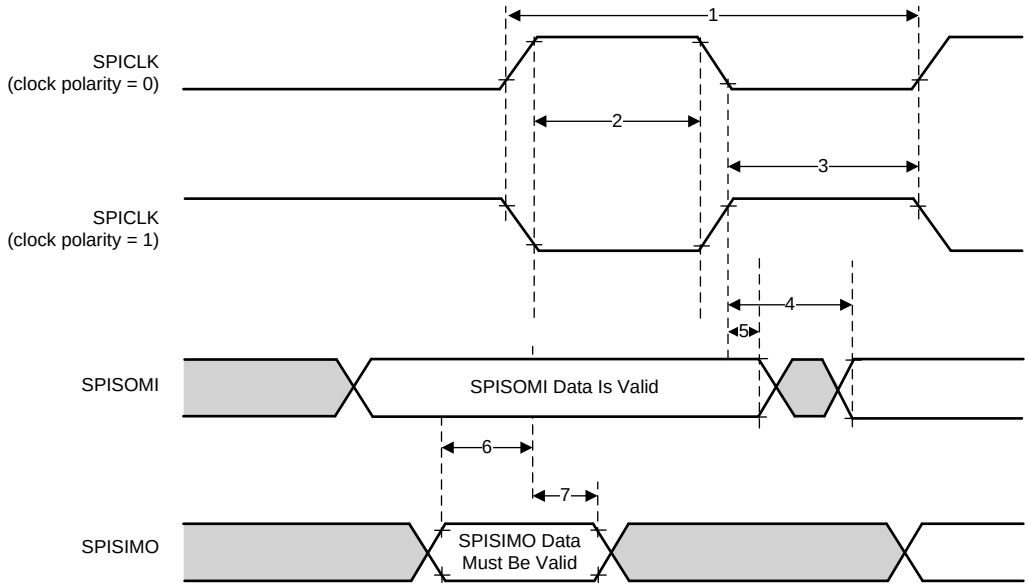


Figure 5-10. SPI Slave Mode External Timing (CLOCK PHASE = 1)

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5.9.4.4 Typical Interface Protocol Diagram (Slave Mode)

1. Host should ensure that there is a delay of two SPI clocks between CS going low and start of SPI clock.
2. Host should ensure that CS is toggled for every 16 bits of transfer through SPI.

Figure 5-11 shows the SPI communication timing of the typical interface protocol.

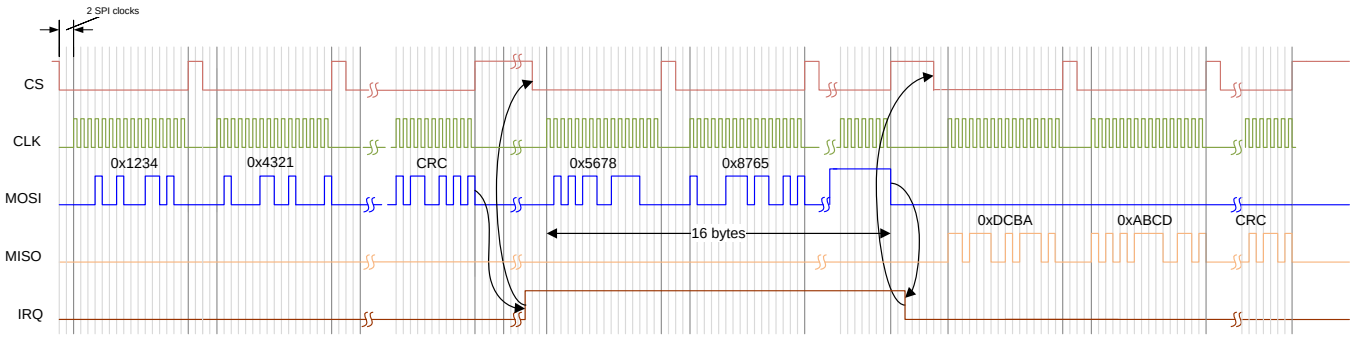


Figure 5-11. SPI Communication

5.9.5 LVDS Interface Configuration

The IWR1443 supports seven differential LVDS IOs/Lanes. The lane configuration supported is four Data lanes (LVDS_TXP/M), one Bit Clock lane (LVDS_CLKP/M) and one Frame clock lane (LVDS_FRCLKP/M), and one HS_DEBUG LVDS pair. The LVDS interface is used for debugging. The LVDS interface supports the following data rates:

- 900 Mbps (450 MHz DDR Clock)
- 600 Mbps (300 MHz DDR Clock)
- 450 Mbps (225 MHz DDR Clock)
- 400 Mbps (200 MHz DDR Clock)
- 300 Mbps (150 MHz DDR Clock)
- 225 Mbps (112.5 MHz DDR Clock)
- 150 Mbps (75 MHz DDR Clock)

Note that the bit clock is in DDR format and hence the numbers of toggles in the clock is equivalent to data.

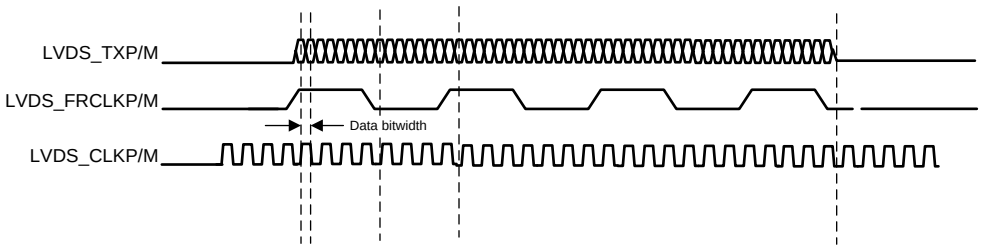


Figure 5-12. LVDS Interface Lane Configuration And Relative Timings

5.9.5.1 LVDS Interface Timings

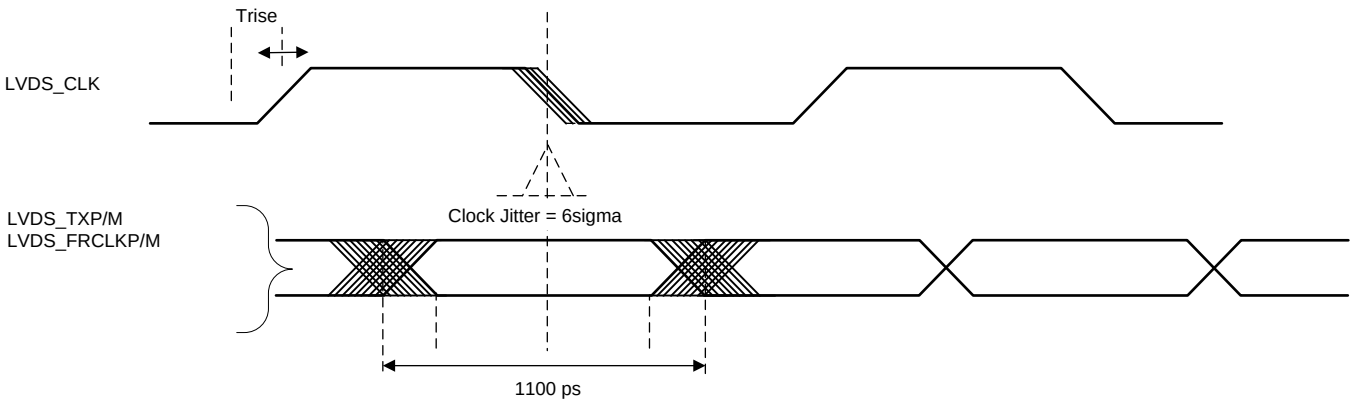


Figure 5-13. Timing Parameters

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Table 5-12. LVDS Electrical Characteristics

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Duty Cycle Requirements	max 1 pF lumped capacitive load on LVDS lanes	48%		52%	
Output Differential Voltage	peak-to-peak single-ended with 100 Ω resistive load between differential pairs	250		450	mV
Output Offset Voltage		1125		1275	mV
Trise and Tfall	20%-80%, 900 Mbps		500		ps
Jitter (pk-pk)	900 Mbps		80		ps

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5.9.6 General-Purpose Input/Output

Table 5-13 lists the switching characteristics of output timing relative to load capacitance.

Table 5-13. Switching Characteristics for Output Timing versus Load Capacitance (C_L)(1)(2)

PARAMETER		TEST CONDITIONS		VIOIN = 1.8V	VIOIN = 3.3V	UNIT
t_r	Max rise time	Slew control = 0	C_L = 20 pF	2.8	3.0	ns
			C_L = 50 pF	6.4	6.9	
			C_L = 75 pF	9.4	10.2	
t_f	Max fall time		C_L = 20 pF	2.8	2.8	ns
			C_L = 50 pF	6.4	6.6	
			C_L = 75 pF	9.4	9.8	
t_r	Max rise time	Slew control = 1	C_L = 20 pF	3.3	3.3	ns
			C_L = 50 pF	6.7	7.2	
			C_L = 75 pF	9.6	10.5	
t_f	Max fall time		C_L = 20 pF	3.1	3.1	ns
			C_L = 50 pF	6.6	6.6	
			C_L = 75 pF	9.6	9.6	

(1) Slew control, which is configured by PADxx_CFG_REG, changes behavior of the output driver (faster or slower output slew rate).
(2) The rise/fall time is measured as the time taken by the signal to transition from 10% and 90% of VIOIN voltage.

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5.9.7 Controller Area Network Interface (DCAN)

The DCAN supports the CAN 2.0B protocol standard and uses a serial, multimaster communication protocol that efficiently supports distributed real-time control with robust communication rates of up to 1 Mbps. The DCAN is ideal for applications operating in noisy and harsh environments that require reliable serial communication or multiplexed wiring.

The DCAN has the following features:

- Supports CAN protocol version 2.0 part A, B
- Bit rates up to 1 Mbps
- Configurable Message objects
- Individual identifier masks for each message object
- Programmable FIFO mode for message objects
- Suspend mode for debug support
- Programmable loop-back modes for self-test operation
- Direct access to Message RAM in test mode
- Supports two interrupt lines - Level 0 and Level 1
- Automatic Message RAM initialization

Table 5-14. Dynamic Characteristics for the DCANx TX and RX Pins

PARAMETER		MIN	TYP	MAX	UNIT
$t_{d(CAN_tx)}$	Delay time, transmit shift register to CAN_tx pin(1)			15	ns
$t_{d(CAN_rx)}$	Delay time, CAN_rx pin to receive shift register(1)			10	ns

(1) These values do not include rise/fall times of the output buffer.

describes the CSI-2 DPHY electrical specifications.

5.9.8 Serial Communication Interface (SCI)

The SCI has the following features:

- Standard universal asynchronous receiver-transmitter (UART) communication
- Standard non-return to zero (NRZ) format
- Double-buffered receive and transmit functions
- Asynchronous or iso-synchronous communication modes with no CLK pin
- Capability to use Direct Memory Access (DMA) for transmit and receive data
- Two external pins: RS232_RX and RS232_TX

Table 5-15. SCI Timing Requirements

		MIN	TYP	MAX	UNIT
f(baud)	Supported baud rate at 20 pF		921.6		kHz

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5.9.9 Inter-Integrated Circuit Interface (I2C)

The inter-integrated circuit (I2C) module is a multimaster communication module providing an interface between devices compliant with Philips Semiconductor I2C-bus specification version 2.1 and connected by an I^2C-bus™. This module will support any slave or master I2C compatible device.

The I2C has the following features:

- Compliance to the Philips I2C bus specification, v2.1 (The I2C Specification, Philips document number 9398 393 40011)
  - Bit/Byte format transfer
  - 7-bit and 10-bit device addressing modes
  - General call
  - START byte
  - Multi-master transmitter/ slave receiver mode
  - Multi-master receiver/ slave transmitter mode
  - Combined master transmit/receive and receive/transmit mode
  - Transfer rates of 100 kbps up to 400 kbps (Phillips fast-mode rate)
- Free data format
- Two DMA events (transmit and receive)
- DMA event enable/disable capability
- Module enable/disable capability
- The SDA and SCL are optionally configurable as general purpose I/O
- Slew rate control of the outputs
- Open drain control of the outputs
- Programmable pullup/pulldown capability on the inputs
- Supports Ignore NACK mode

NOTE

This I2C module does not support:

- High-speed (HS) mode
- C-bus compatibility mode
- The combined format in 10-bit address mode (the I2C sends the slave address second byte every time it sends the slave address first byte)

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Table 5-16. I2C Timing Requirements(1)

		STANDARD MODE		FAST MODE		UNIT
		MIN	MAX	MIN	MAX	
$t_{c(SCL)}$	Cycle time, SCL	10		2.5		µs
$t_{su(SCLH-SDAL)}$	Setup time, SCL high before SDA low (for a repeated START condition)	4.7		0.6		µs
$t_{h(SCLL-SDAL)}$	Hold time, SCL low after SDA low (for a START and a repeated START condition)	4		0.6		µs
$t_{w(SCLL)}$	Pulse duration, SCL low	4.7		1.3		µs
$t_{w(SCLH)}$	Pulse duration, SCL high	4		0.6		µs
$t_{su(SDA-SCLH)}$	Setup time, SDA valid before SCL high	250		100		µs
$t_{h(SCLL-SDA)}$	Hold time, SDA valid after SCL low	0	3.45(1)	0	0.9	µs
$t_{w(SDAH)}$	Pulse duration, SDA high between STOP and START conditions	4.7		1.3		µs
$t_{su(SCLH-SDAH)}$	Setup time, SCL high before SDA high (for STOP condition)	4		0.6		µs
$t_{w(SP)}$	Pulse duration, spike (must be suppressed)			0	50	ns
C_b(2)(3)	Capacitive load for each bus line		400		400	pF

(1) The I2C pins SDA and SCL do not feature fail-safe I/O buffers. These pins could potentially draw current when the device is powered down.
(2) The maximum th(SDA-SCLL) for I2C bus devices has only to be met if the device does not stretch the low period (tw(SCLL)) of the SCL signal.
(3) C_b = total capacitance of one bus line in pF. If mixed with fast-mode devices, faster fall-times are allowed.

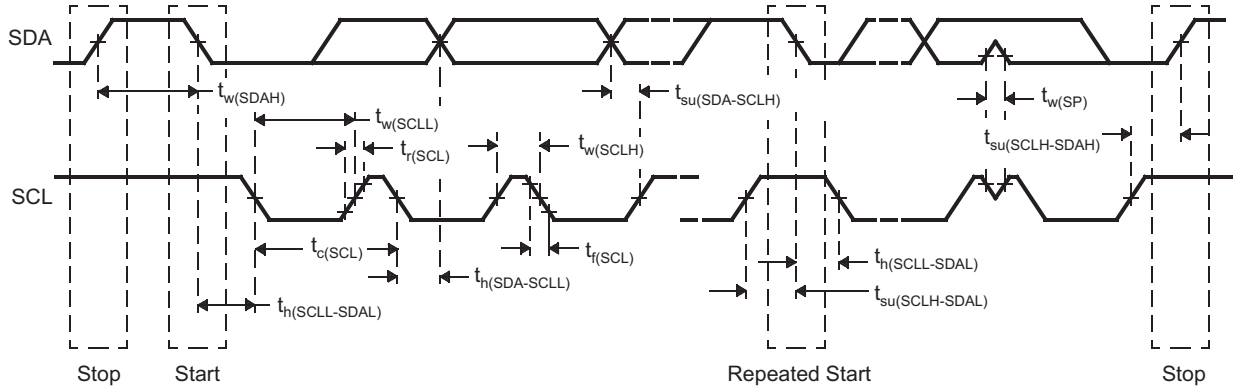


Figure 5-14. I2C Timing Diagram

NOTE

- A device must internally provide a hold time of at least 300 ns for the SDA signal (referred to the VIHmin of the SCL signal) to bridge the undefined region of the falling edge of SCL.
- The maximum th(SDA-SCLL) has only to be met if the device does not stretch the LOW period (tw(SCLL)) of the SCL signal. E.A Fast-mode I2C-bus device can be used in a Standard-mode I2C-bus system, but the requirement $t_{su(SDA-SCLH)} \geq 250$ ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line tr max + $t_{su(SDA-SCLH)}$.

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5.9.10 Quad Serial Peripheral Interface (QSPI)

The quad serial peripheral interface (QSPI™) module is a kind of SPI module that allows single, dual, or quad read access to external SPI devices. This module has a memory mapped register interface, which provides a direct interface for accessing data from external SPI devices and thus simplifying software requirements. The QSPI works as a master only. The QSPI in the device is primarily intended for fast booting from quad-SPI flash memories.

The QSPI supports the following features:

- Programmable clock divider
- Six-pin interface
- Programmable length (from 1 to 128 bits) of the words transferred
- Programmable number (from 1 to 4096) of the words transferred
- Support for 3-, 4-, or 6-pin SPI interface
- Optional interrupt generation on word or frame (number of words) completion
- Programmable delay between chip select activation and output data from 0 to 3 QSPI clock cycles

Table 5-18 and Table 5-19 assume the operating conditions stated in Table 5-17.

Table 5-17. QSPI Timing Conditions

		MIN	TYP	MAX	UNIT
Input Conditions					
t_R	Input rise time	1		3	ns
t_F	Input fall time	1		3	ns
Output Conditions					
C_{LOAD}	Output load capacitance	2		15	pF

Table 5-18. Timing Requirements for QSPI Input (Read) Timings(1)(2)

		MIN	TYP	MAX	UNIT
$t_{su(D-SCLK)}$	Setup time, d[3:0] valid before falling sclk edge	7.3			ns
$t_{h(SCLK-D)}$	Hold time, d[3:0] valid after falling sclk edge	1.5			ns
$t_{su(D-SCLK)}$	Setup time, final d[3:0] bit valid before final falling sclk edge	7.3 – P(3)			ns
$t_{h(SCLK-D)}$	Hold time, final d[3:0] bit valid after final falling sclk edge	1.5 + P(3)			ns

(1) Clock Mode 0 (clk polarity = 0 ; clk phase = 0) is the mode of operation.
(2) The Device captures data on the falling clock edge in Clock Mode 0, as opposed to the traditional rising clock edge. Although non-standard, the falling-edge-based setup and hold time timings have been designed to be compatible with standard SPI devices that launch data on the falling edge in Clock Mode 0.
(3) P = SCLK period in ns.

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Table 5-19. QSPI Switching Characteristics

NO.	PARAMETER		MIN	TYP	MAX	UNIT
Q1	$t_{c(SCLK)}$	Cycle time, sclk	25			ns
Q2	$t_{w(SCLKL)}$	Pulse duration, sclk low	Y*P – 3 (1) (2)			ns
Q3	$t_{w(SCLKH)}$	Pulse duration, sclk high	Y*P – 3 (1)			ns
Q4	$t_{d(CS-SCLK)}$	Delay time, sclk falling edge to cs active edge	–M*P – 1 (1) (3)		–M*P + 2.5 (1) (3)	ns
Q5	$t_{d(SCLK-CS)}$	Delay time, sclk falling edge to cs inactive edge	N*P – 1 (1) (3)		N*P + 2.5 (1) (3)	ns
Q6	$t_{d(SCLK-D1)}$	Delay time, sclk falling edge to d[1] transition	–3.5		7	ns
Q7	$t_{ena(CS-D1LZ)}$	Enable time, cs active edge to d[1] driven (lo-z)	–P – 4 (3)		–P +1 (3)	ns
Q8	$t_{dis(CS-D1Z)}$	Disable time, cs active edge to d[1] tri-stated (hi-z)	–P – 4 (3)		–P +1 (3)	ns
Q9	$t_{d(SCLK-D1)}$	Delay time, sclk first falling edge to first d[1] transition (for PHA = 0 only)	–3.5 – P (3)		7 – P (3)	ns
Q12	$t_{su(D-SCLK)}$	Setup time, d[3:0] valid before falling sclk edge	7.3			ns
Q13	$t_{h(SCLK-D)}$	Hold time, d[3:0] valid after falling sclk edge	1.5			ns
Q14	$t_{su(D-SCLK)}$	Setup time, final d[3:0] bit valid before final falling sclk edge	7.3 — P (3)			ns
Q15	$t_{h(SCLK-D)}$	Hold time, final d[3:0] bit valid after final falling sclk edge	1.5 + P (3)			ns

(1) The Y parameter is defined as follows: If DCLK_DIV is 0 or ODD then, Y equals 0.5. If DCLK_DIV is EVEN then, Y equals (DCLK_DIV/2) / (DCLK_DIV+1). For best performance, it is recommended to use a DCLK_DIV of 0 or ODD to minimize the duty cycle distortion. The HSDIVIDER on CLKOUTX2_H13 output of DPLL_PER can be used to achieve the desired clock divider ratio. All required details about clock division factor DCLK_DIV can be found in the device-specific Technical Reference Manual.
(2) P = SCLK period in ns.
(3) M = QSPI_SPI_DC_REG.DDx + 1, N = 2

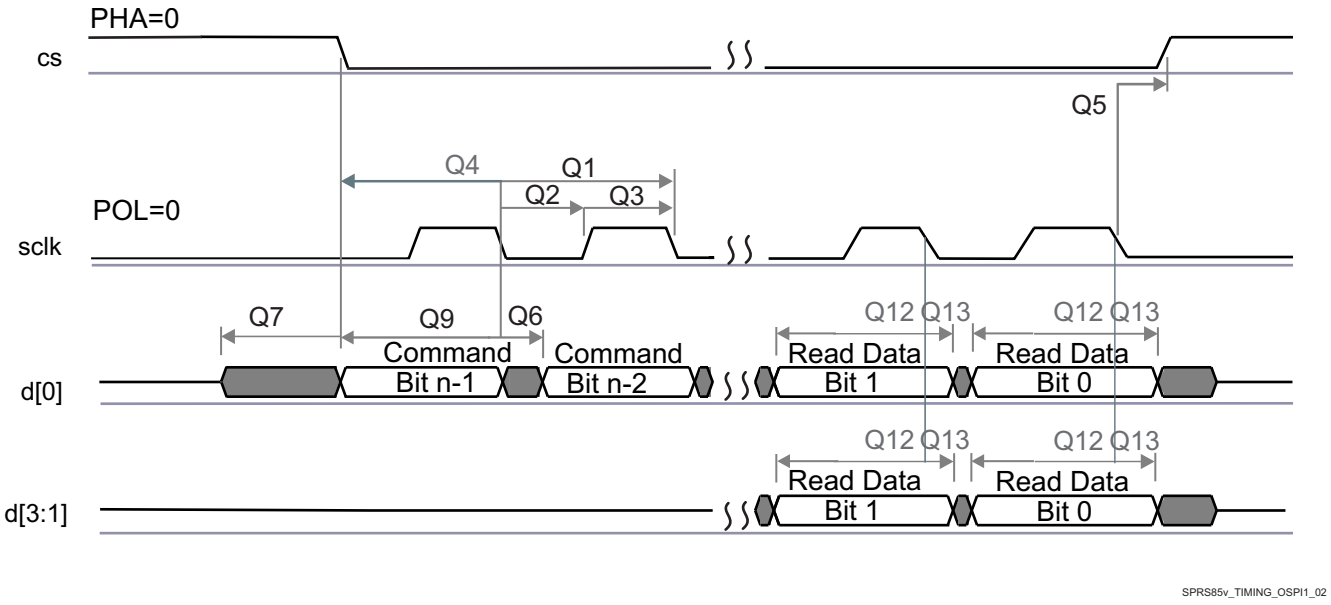


Figure 5-15. QSPI Read (Clock Mode 0)

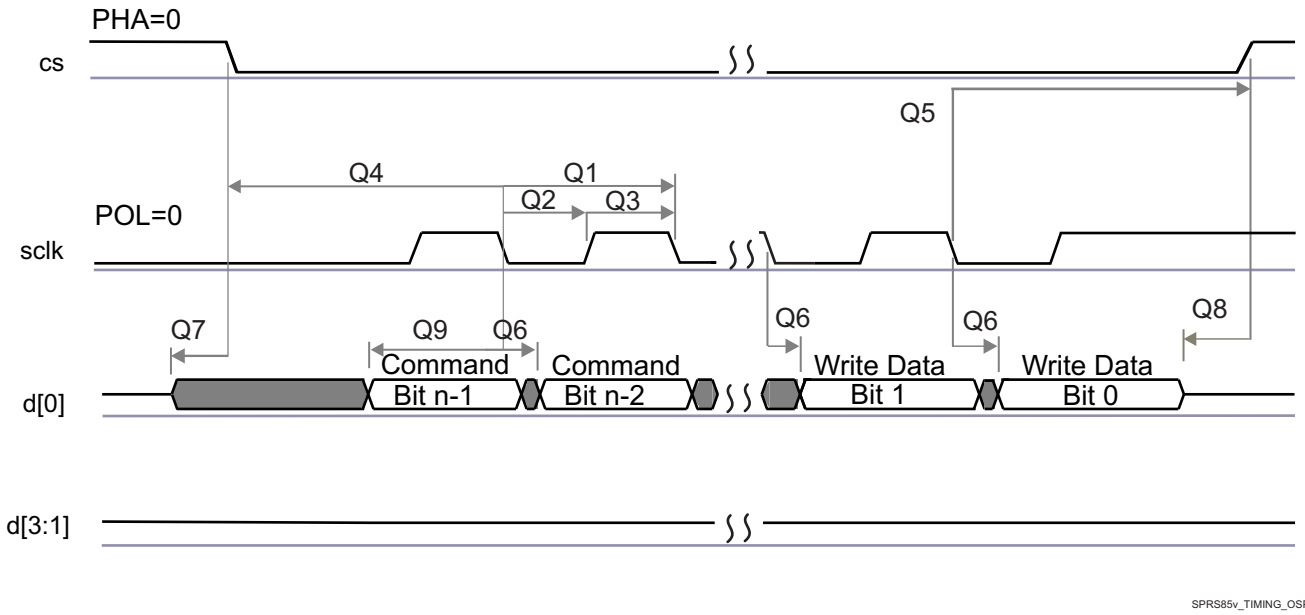


Figure 5-16. QSPI Write (Clock Mode 0)

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5.9.11 JTAG Interface

Table 5-21 and Table 5-22 assume the operating conditions stated in Table 5-20.

Table 5-20. JTAG Timing Conditions

		MIN	TYP	MAX	UNIT
Input Conditions					
t_R	Input rise time	1		3	ns
t_F	Input fall time	1		3	ns
Output Conditions					
C_{LOAD}	Output load capacitance	2		15	pF

Table 5-21. Timing Requirements for IEEE 1149.1 JTAG

NO.			MIN	TYP	MAX	UNIT
1	$t_{c(TCK)}$	Cycle time TCK	66.66			ns
1a	$t_{w(TCKH)}$	Pulse duration TCK high (40% of tc)	26.67			ns
1b	$t_{w(TCKL)}$	Pulse duration TCK low(40% of tc)	26.67			ns
3	$t_{su(TDI-TCK)}$	Input setup time TDI valid to TCK high	2.5			ns
	$t_{su(TMS-TCK)}$	Input setup time TMS valid to TCK high	2.5			ns
4	$t_{h(TCK-TDI)}$	Input hold time TDI valid from TCK high	18			ns
	$t_{h(TCK-TMS)}$	Input hold time TMS valid from TCK high	18			ns

Table 5-22. Switching Characteristics Over Recommended Operating Conditions for IEEE 1149.1 JTAG

NO.	PARAMETER		MIN	TYP	MAX	UNIT
2	$t_{d(TCKL-TDOV)}$	Delay time, TCK low to TDO valid	0		25	ns

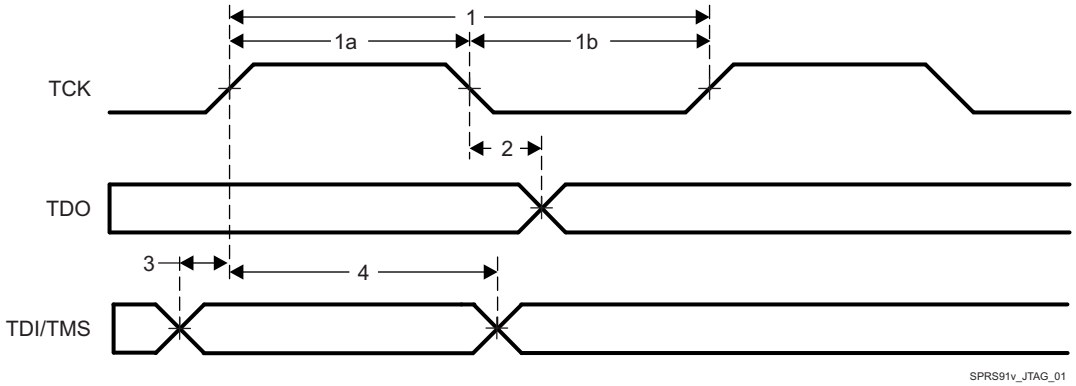


Figure 5-17. JTAG Timing

5.9.12 Camera Serial Interface (CSI)

The CSI is a MIPI D-PHY compliant interface for connecting this device to a camera receiver module. This interface is made of four differential lanes; each lane is configurable for carrying data or clock. The polarity of each wire of a lane is also configurable. Table 5-23, Figure 5-18, Figure 5-19, and Figure 5-20 describe the clock and data timing of the CSI.

Table 5-23. CSI Switching Characteristics

over operating Tj temperature range (unless otherwise noted)

PARAMETER			MIN	TYP	MAX	UNIT
HPTX						
$HSTX_{DBR}$	Data bit rate	(1 or 2 data lane PHY)	150		600	Mbps
		(4 data lane PHY)	150		600	
f_{CLK}	DDR clock frequency	(1 or 2 data lane PHY)	75		450	MHz
		(4 data lane PHY)	75		300	
$\Delta_{VCMTX(LF)}$	Common-level variation from 75 to 450 MHz of CSI2 clock frequency		–50		50	mVpeak
t_R and t_F	20% to 80% rise time and fall time		150			ns
					0.3	UI
LPTX DRIVER						
t_{RLP} and t_{FLP}	15% to 85% rise time and fall time				25	ns
t_{EOT} (1)	Time from start of THS-TRAIL period to start of LP-11 state				105 + 12*UI	ns
$\delta V/\delta t_{SR}$ (2)(3)(4)	Slew rate. C_{LOAD} = 0 to 5 pF				500	mV/ns
	Slew rate. C_{LOAD} = 5 to 20 pF				200	
	Slew rate. C_{LOAD} = 20 to 70 pF				100	
C_{LOAD} (2)	Load capacitance		0		70	pF
DATA-CLOCK Timing Specification						
UINOM	Nominal Unit Interval (1, 2, or 3 data lane PHY)		1.11		13.33	ns
	Nominal Unit Interval (4 data lane PHY)		1.67		13.33	
UIINST,MIN	Minimum instantaneous Unit Interval (1, 2, or 3 data lane PHY)		1.033	0.975*UINOM – 0.05		ns
	Minimum instantaneous Unit Interval (4 data lane PHY)		1.131			
TSKEW[TX]	Data to clock skew measured at transmitter		–0.15		0.15	UIINST, MIN
CSI2 TIMING SPECIFICATION						
$T_{CLK-MISS}$	Time-out for receiver to detect absence of clock transitions and disable the clock lane HS-RX.				60	ns
$T_{CLK-POST}$	Time that the transmitter continues to send HS clock after the last associated data lane has transitioned to lp mode. Interval is defined as the period from the end of $T_{HS-TRAIL}$ to the beginning of $T_{CLK-TRAIL}$.		60 ns + 52*UI			ns
$T_{CLK-PRE}$	Time that the HS clock shall be driven by the transmitter before any associated data lane beginning the transition from LP to HS mode.		8			ns
$T_{CLK-PREPARE}$	Time that the transmitter drives the clock lane LP-00 line state immediately before the HS-0 line state starting the HS transmission.		38		95	ns
$T_{CLK-TERM-EN}$	Time for the clock lane receiver to enable the HS line termination, starting from the time point when Dn crosses VIL,MAX.		Time for Dn to reach VTERM-EN		38	ns

(1) With an additional load capacitance CCM of 0 to 60 pF on the termination center tap at RX side of the lane
(2) While driving C_{LOAD}. Load capacitance includes 50 pF of transmission line capacitance, and 10 pF each for TX and RX.
(3) When the output voltage is from 15% to 85% of the fully settled LP signal levels
(4) Measured as average across any 50 mV segment of the output signal transition

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Table 5-23. CSI Switching Characteristics (continued)

over operating Tj temperature range (unless otherwise noted)

PARAMETER		MIN	TYP	MAX	UNIT
$T_{CLK-TRAIL}$	Time that the transmitter drives the HS-0 state after the last payload clock bit of a HS transmission burst.	60			ns
$T_{CLK-PREPARE}$ + $T_{CLK-ZERO}$	$T_{CLK-PREPARE}$ + time that the transmitter drives the HS-0 state before starting the clock.	300			ns
$T_{D-TERM-EN}$	Time for the data lane receiver to enable the HS line termination, starting from the time point when Dn crosses VIL,MAX.	Time for Dn to reach VTERM-EN		35 ns + 4*UI	ns
T_{EOT}	Transmitted time interval from the start of $T_{HS-TRAIL}$ or $T_{CLKTRAIL}$, to the start of the LP-11 state following a HS burst.			105 ns + n*12*UI	ns
$T_{HS-PREPARE}$	Time that the transmitter drives the data lane LP-00 line state immediately before the HS-0 line state starting the HS transmission	40 + 4*UI		85 + 6*UI	ns
$T_{HS-PREPARE}$ + $T_{HS-ZERO}$	$T_{HS-PREPARE}$ + time that the transmitter drives the HS-0 state prior to transmitting the Sync sequence.	145 ns + 10*UI			ns
$T_{HS-SKIP}$	Time interval during which the HS-RX should ignore any transitions on the data lane, following a HS burst. The end point of the interval is defined as the beginning of the LP-11 state following the HS burst.	40		55 ns + 4*UI	ns
$T_{HS-EXIT}$	Time that the transmitter drives LP-11 following a HS burst.	100			ns
$T_{HS-TRAIL}$	Time that the transmitter drives the flipped differential state after last payload data bit of a HS transmission burst	max(n*8*UI, 60 ns + n*4*UI)(5)(6)			ns
T_{LPX}	Transmitted length of any low-power state period	50(7)			ns

(5) If a > b then max(a, b) = a, otherwise max(a, b) = b.
(6) Where n = 1 for Forward-direction HS mode and n = 4 for Reverse-direction HS mode
(7) T_{LPX} is an internal state machine timing reference. Externally measured values may differ slightly from the specified values due to asymmetrical rise and fall times.

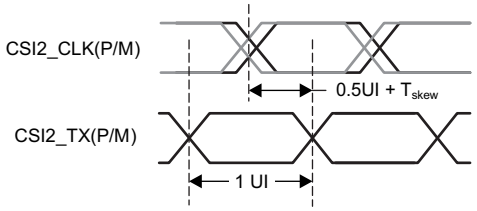


Figure 5-18. Clock and Data Timing in HS Transmission

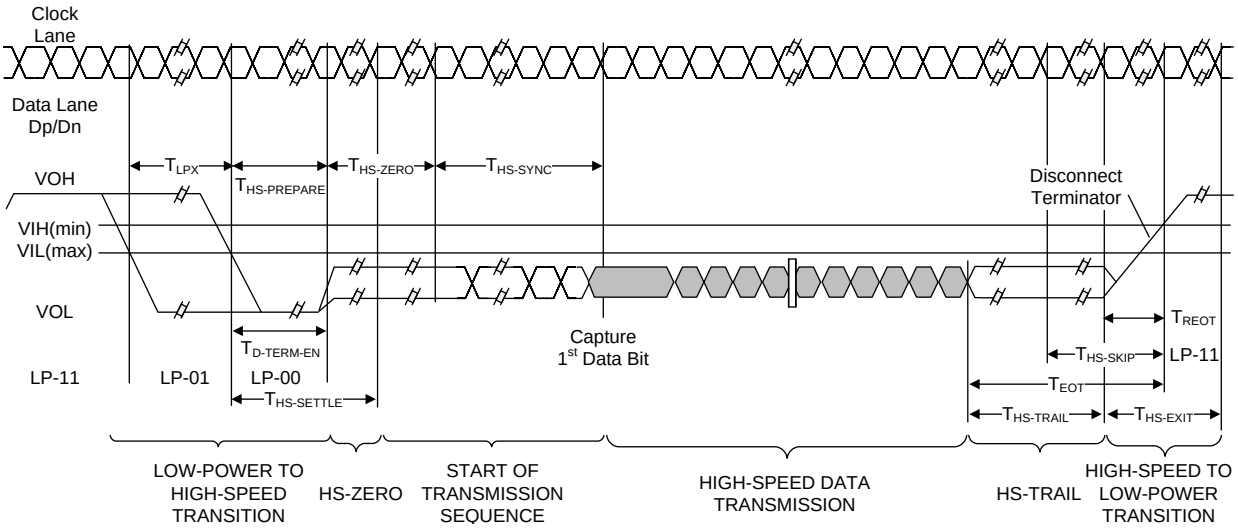
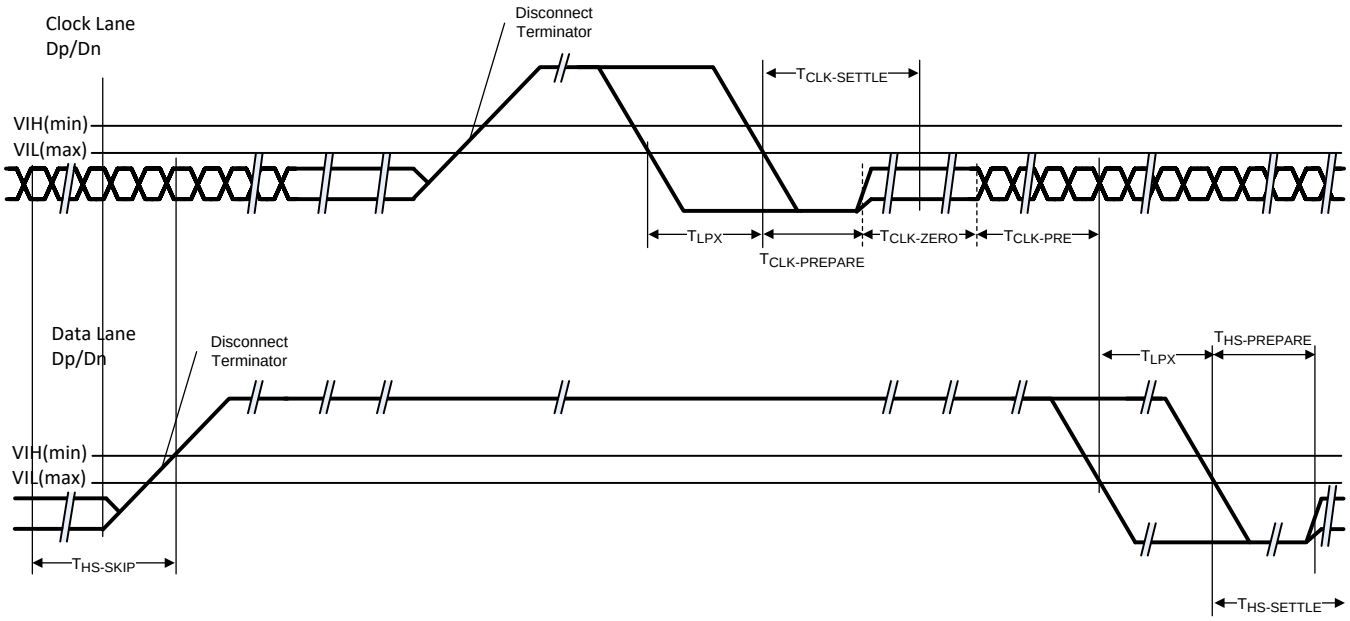


Figure 5-19. High-Speed Data Transmission Burst



(1) The HS to LP transition of the CLK does not actually take place since the CLK is always ON in HS mode.

Figure 5-20. Switching the Clock Lane Between Clock Transmission and Low-Power Mode

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6 Detailed Description

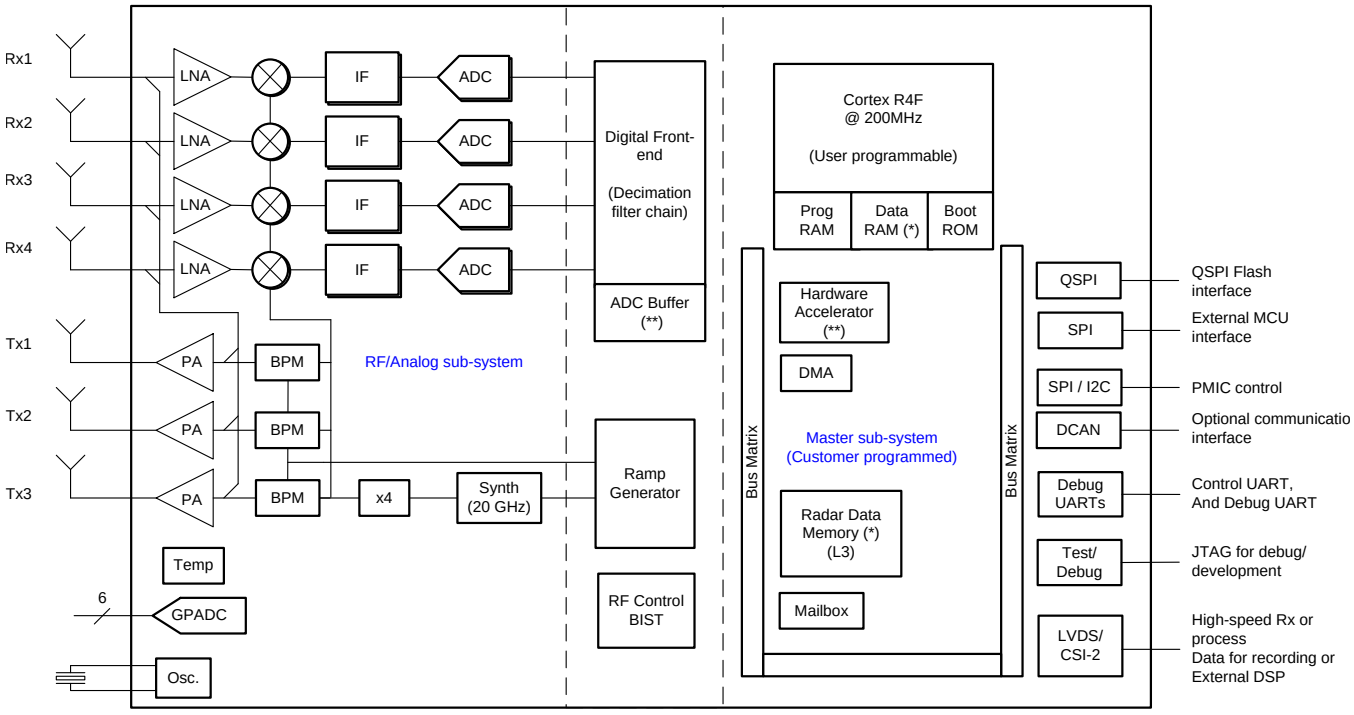
6.1 Overview

The IWR1443 device includes the entire Millimeter Wave blocks and analog baseband signal chain for three transmitters (two usable at the same instance) and four receivers, as well as a customer-programmable MCU with a hardware accelerator for radar signal processing. This device is applicable as a radar-on-a-chip in use-cases with modest requirements for memory, processing capacity and application code size. These could be cost-sensitive industrial radar sensing applications. Examples are:

- Industrial level sensing
- Industrial automation sensor fusion with radar
- traffic intersection monitoring with radar
- Industrial radar-proximity monitoring.

In terms of scalability, the IWR1443 device could be paired with a low-end external MCU, to address more complex applications that might require additional memory for larger application software footprint and faster interfaces. Because the IWR1443 device also provides high speed data interfaces like MIPI-CSI2, it is suitable for interfacing with more capable external processing blocks. Here system designers can choose the IWR1443 to provide raw ADC data or use the on-chip Hardware Accelerator for partial processing viz. first stage Fast Fourier Transform.

6.2 Functional Block Diagram



(*) Total RAM available in Master subsystem is divided into ARM-Data RAM, Tightly Coupled Memory, Radar Data Memory, Patch Memory
(**) Shared Memory for ADC Buffer and Hardware Accelerator

6.3 External Interfaces

The IWR1443 device provides the following external interfaces:

- Reference Clock – Reference clock available for Host Processor after device wakeup.
- Low speed control information
  - Up to two 4-line standard SPI interface
  - One I^2C interface (Pin multiplexed with one of the SPI ports)
- One Controller Area Network (CAN) Port for Industrial Interfacing
- Data – High-Speed serial port following the MIPI CSI2 format. 4 data and 1 clock lane (all differential). Data from different receive channels can be multiplexed on a single data lane in order to optimize board routing. This is a unidirectional interface used for data transfer only.
- Reset – Active Low reset for device wakeup from host General Purpose IOs
- Error Signaling – Used for notifying the host in case the Radio Controller detects a fault

The IWR1443 device comprises of three main blocks – Radar (or the Millimeter Wave) System, Master (or the Control) System and Processing System.

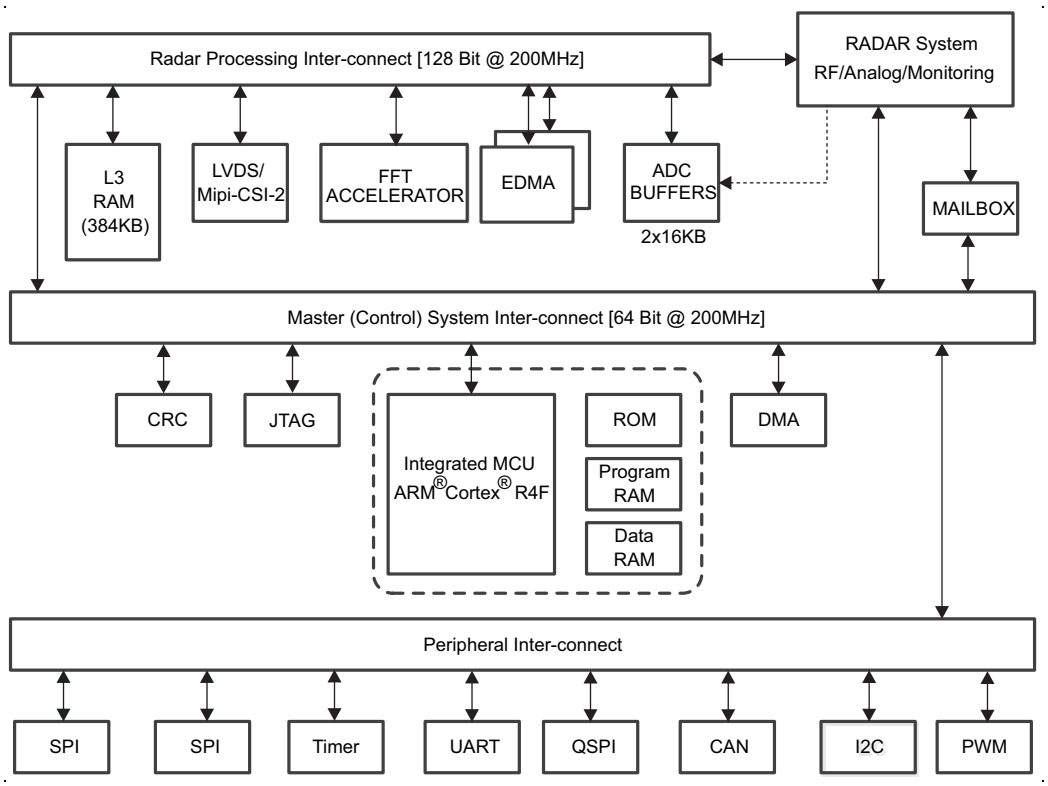


Figure 6-1. System Interconnect

6.4 Subsystems

6.4.1 RF and Analog Subsystem

The RF and analog subsystem includes the RF and analog circuitry – namely, the synthesizer, PA, LNA, mixer, IF, and ADC. This subsystem also includes the crystal oscillator and temperature sensors. The three transmit channels can be operated up to a maximum of two at a time (simultaneously) for transmit beamforming purpose as required; whereas the four receive channels can all be operated simultaneously.

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6.4.1.1 Clock Subsystem

The IWR1443 clock subsystem generates 76 to 81 GHz from an input reference of 40-MHz crystal or external clock. It has a built-in oscillator circuit followed by a clean-up PLL and a RF synthesizer circuit. The output of the RF synthesizer is then processed by an X4 multiplier to create the required frequency in the 76 to 81 GHz spectrum. The RF synthesizer output is modulated by the timing engine block to create the required waveforms for effective sensor operation.

The clean-up PLL also provides a reference clock for the host processor after system wakeup.

The clock subsystem also has built-in mechanisms for detecting the presence of a crystal and monitoring the quality of the generated clock.

Figure 6-2 describes the clock subsystem.

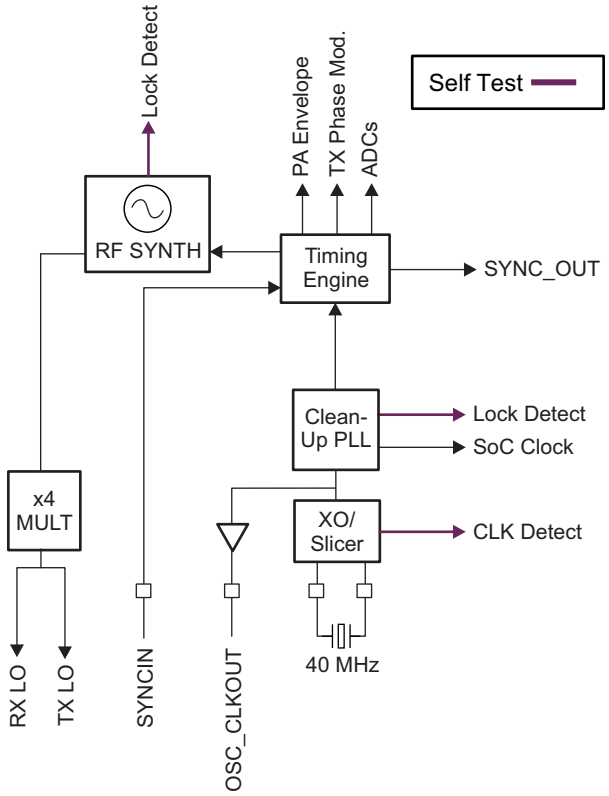


Figure 6-2. Clock Subsystem

6.4.1.2 Transmit Subsystem

The IWR1443 transmit subsystem consists of three parallel transmit chains, each with independent phase and amplitude control. A maximum of 2 transmit chains can be operational at the same time. However all 3 chains can be operated together in a time multiplexed fashion.The device supports binary phase modulation for MIMO radar and interference mitigation.

Each transmit chain can deliver a maximum of 12 dBm at the antenna port on the PCB. The transmit chains also support programmable backoff for system optimization.

Figure 6-3 describes the transmit subsystem.

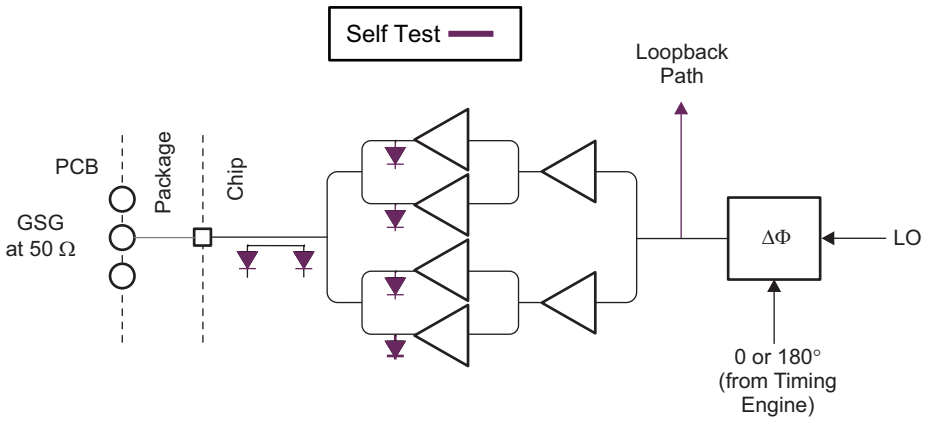


Figure 6-3. Transmit Subsystem (Per Channel)

6.4.1.3 Receive Subsystem

The IWR1443 receive subsystem consists of four parallel channels. A single receive channel consists of an LNA, mixer, IF filtering, A2D conversion, and decimation. All four receive channels can be operational at the same time an individual power-down option is also available for system optimization.

Unlike conventional real-only receivers, the IWR1443 device supports a complex baseband architecture, which uses quadrature mixer and dual IF and ADC chains to provide complex I and Q outputs for each receiver channel. The IWR1443 is targeted for fast chirp systems. The band-pass IF chain has configurable lower cutoff frequencies above 175 kHz and can support bandwidths up to 15 MHz.

Figure 6-4 describes the receive subsystem.

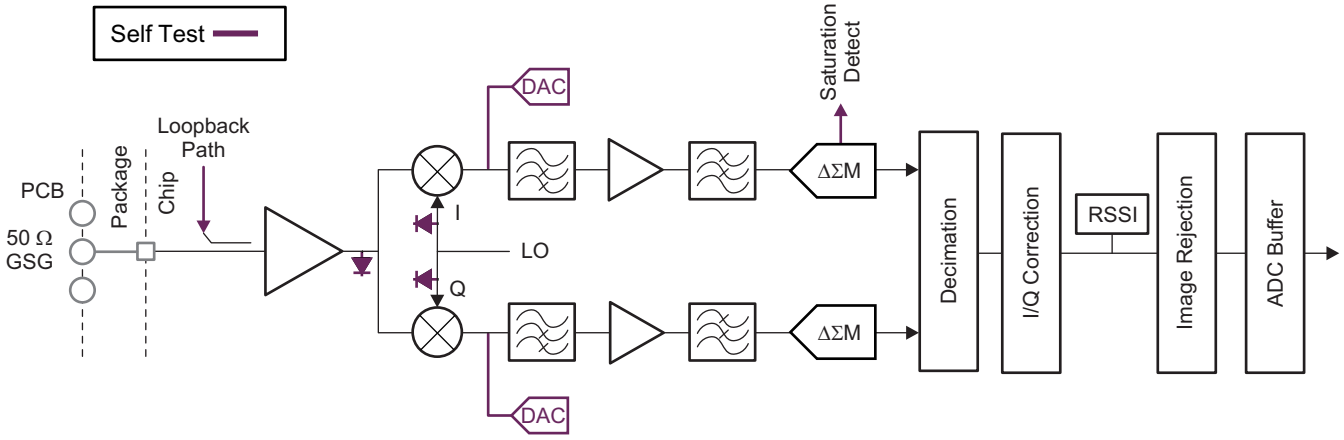


Figure 6-4. Receive Subsystem (Per Channel)

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6.4.1.4 Radio Processor Subsystem

The Radio Processor subsystem (also referred to as BIST Subsystem in this document) includes the digital front-end, the ramp generator and an internal processor for control / configuration of the low-level RF/analog and ramp generator registers. The Radar Processor also schedules periodic monitoring tasks. User applications, running on

Master (Control) System, do not have direct access to Radar System; access is based on well-defined API messages (over a hardware channel) from the master subsystem.

NOTE

This radio processor is programmed by TI and takes care of RF calibration and self-test/monitoring functions (BIST). This processor is not available directly for customer use/application.

The digital front-end takes care of filtering and decimating the raw sigma-delta ADC output and provides the final ADC data samples at a programmable sampling rate.

6.4.2 Master (Control) System

The Master (Control) System includes ARM's Cortex-R4F processor clocked at 200 MHz, which is user programmable. User applications executing on this processor control the overall operation of the device, including Radar Control via well-defined API messages, radar signal processing (assisted by the radar hardware accelerator) and peripherals for external interface.

The Master (Control) System plays a big role in enabling autonomous operation of IWR1443 as a radar-on-a-chip sensor. The device includes a quad serial peripheral interface (QSPI) which can be used to download customer code directly from a serial flash. A (classic) CAN interface is included that can be used to communicate directly from the device to a CAN bus. An SPI/I2C interface is available for power management IC (PMIC) control when the IWR1443 is used as an autonomous sensor.

For more complex applications, the device can operate under the control of an external MCU, which can communicate with IWR1443 device over an SPI interface. In this case, it is possible to use the IWR14xx as a radar sensor, providing raw detected objects to the external MCU. External MCU could reduce the application code complexity residing in the device and makes more memory available for radar data cube inside the IWR1443. This configuration also eliminates the need for a separate serial flash to be connected to the IWR1443.

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The IWR1443 provides for several digital communications outputs; CSI-2 Clk, 4 data formats – can be connected to a remote processor for additional processing. Note: CSI-2 data is from the digital front end or accelerator. When the MSS is used for preprocessing / or another MCU is used in industrial settings the Serial Tx/Rx or CAN bus can provide lower speed communication than CSI-2. The IWR1443 has additional serial Tx/Rx for HART protocol for industrial sensors, or Modbus serial protocol. The SPI port can also provide additional communications or IO control. Additional industrial IO can be Industrial Ethernet or Wifi.

Note that although four interfaces – one CAN, one I2C and two SPI interfaces – are present in the IWR1443 device for external communication and PMIC control, only two of these interfaces are usable at any point in time.

The total memory (RAM) available in the master subsystem is 576 KB. This is partitioned between the R4F program RAM, R4F data RAM and radar data memory. The maximum usable size for R4F is 448 KB and this is partitioned between the R4F's tightly coupled interfaces TCMA (320 KB) and TCMB (128 KB). Although the complete 448 KB is unified memory and can be used for program or data, typical applications use TCMA as program and TCMB as data memory.

The remaining memory, starting at a minimum of 128 KB, is available to be used as radar data memory for storing the 'radar data cube'. It is possible to increase the radar data memory size in 64 KB increments, at the cost of corresponding reduction in R4F program or data RAM size. The maximum size of radar data memory possible is 384 KB. A few example configurations supported are listed in Table 6-1.

Table 6-1. R4F RAM(1)

OPTION	R4F PROGRAM RAM	R4F DATA RAM	RADAR DATA MEMORY
1	320KB	128KB	128KB
2	256KB	128KB	192KB
3	256KB	64KB	256KB
4	128KB	64KB	384KB

(1) For IWR1443 ES1.0 and ES2.0, available RAM is 448 KB instead of 576KB.

The Master Subsystem Memory Map is shown in the Technical Reference Manual.

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6.4.3 Host Interface

The IWR1443 device communicates with the host radar processor over the following main interfaces:

- Reference Clock – Reference clock available for host processor after device wakeup
- Control – 4-port standard SPI (slave) for host control. Control UART or CAN can be used as a control interface
  . All radio control commands (and response) flow through this interface.
- Data – High-speed serial port following the MIPI CSI2 format (LVDS format can also be used). Four data and one clock lane (all differential). Data from different receive channels can be multiplexed on a single data lane to optimize board routing. This is a unidirectional interface used for data transfer only.
- Reset – Active-low reset for device wakeup from host
- Out-of-band interrupt
- Error – Used for notifying the host in case the radio controller detects a fault

6.5 Accelerators and Coprocessors

The Processing System in the IWR1443 device is an accelerator for FFT operations. The Radar Hardware Accelerator is an IP that enables off-loading the burden of certain frequently used computations in FMCW radar signal processing from the main processor. It is well-known that FMCW radar signal processing involves the use of FFT and Log-Magnitude computations in order to obtain a radar image across the range, velocity and angle dimensions. Some of the frequently used functions in FMCW radar signal processing can be done within the Radar Hardware Accelerator, while still retaining the flexibility of implementing other proprietary algorithms in the Master System processor.

Key features of the Radar Processing Accelerator are:

- FFT computation, with programmable FFT sizes (powers of 2) up to 1024-pt complex FFT
- Internal FFT bit-width of 24 bits (each for I and Q) for good SQNR performance, with fully programmable butterfly scaling at every radix-2 stage for user flexibility
- Built-in capabilities for simple pre-FFT processing – specifically, programmable windowing, basic interference zeroing-out and basic BPM removal
- Magnitude (absolute value) and Log-Magnitude computation capability
- Flexible data flow and data sample arrangement to support efficient multi-dimensional FFT operations and transpose accesses as required
- Chaining and Looping mechanism to sequence a set of accelerator operations one-after-another with minimal intervention from the main processor
- CFAR-CA detector support (linear and logarithmic)
- Miscellaneous other capabilities of the accelerator
  - Stitching two or four 1024-point FFTs to get the equivalent of 2048-point or 4096-point FFT for industrial level sensing applications where large FFT sizes are required
  - Slow DFT mode, with resolution equivalent to 16K size FFT, for FFT peak interpolation (eg. range interpolation) purpose
  - Complex Vector Multiplication and Dot product capability for vectors of size up to 512

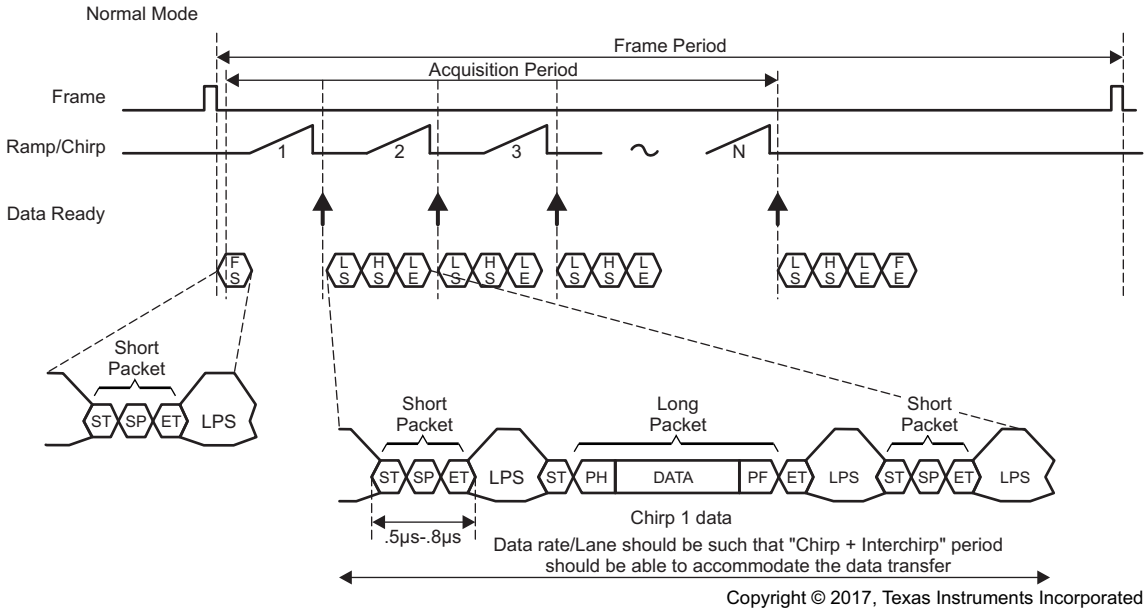
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6.6 Other Subsystems

6.6.1 A2D Data Format Over CSI2 Interface

The IWR1443 device uses MIPI D-PHY / CSI2-based format to transfer the raw A2D samples to the external MCU. This is shown in Figure 6-5.

- Supports four data lanes
- CSI-2 data rate scalable from 150 Mbps to 600 Mbps per lane
- Virtual channel based
- CRC generation



Frame **S**tart – CSi2 VSYNC Start Short Packet
Line **S**tart – CSI2 HSYNC Start Short Packet
Line **E**nd – CSI2 HSYNC End Short Packet
Frame **E**nd – CSi2 VSYNC End Short Packet

Figure 6-5. CSI-2 Transmission Format

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The data payload is constructed with the following three types of information:

- Chirp profile information
- The actual chirp number
- A2D data corresponding to chirps of all four channels
  - Interleaved fashion
- Chirp quality data (configurable)

The payload is then split across the four physical data lanes and transmitted to the receiving D-PHY. The data packet packing format is shown in Figure 6-6

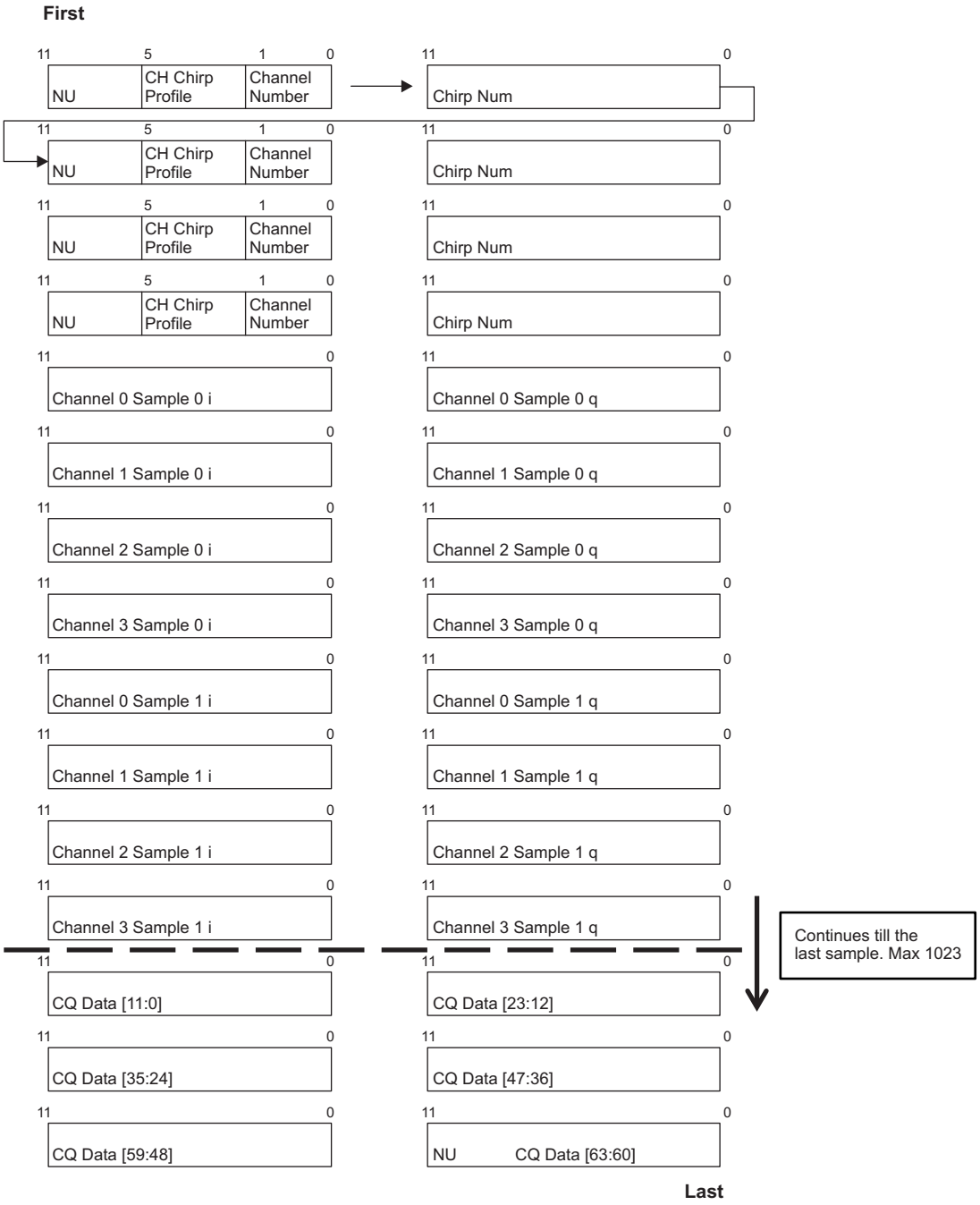


Figure 6-6. Data Packet Packing Format for 12-Bit Complex Configuration

6.6.2 ADC Channels (Service) for User Application

The IWR1443 device includes provision for an ADC service for user application, where the

GPADC engine present inside the device can be used to measure up to six external voltages. The GPADC1, GPADC2, GPADC3, GPADC4, GPADC5, and GPADC6 pins are used for this purpose.

- ADC itself is controlled by TI firmware running inside the BIST subsystem and access to it for customer's external voltage monitoring purpose is via 'monitoring API' calls routed to the BIST subsystem. This API could be linked with the user application running on the Master R4.
- BIST subsystem firmware will internally schedule these measurements along with other RF and Analog monitoring operations. The API allows configuring the settling time (number of ADC samples to skip) and number of consecutive samples to take. At the end of a frame, the minimum, maximum and average of the readings will be reported for each of the monitored voltages.

GPADC Specifications:

- 625 Ksps SAR ADC
- 0 to 1.8V input range
- 10-bit resolution
- For 5 out of the 6 inputs, an optional internal buffer (0.4-1.3V input range) is available. Without the buffer, the ADC has a switched capacitor input load modeled with 5pF of sampling capacitance and 12pF parasitic capacitance (ADC channel mapped to C14, the internal buffer is not available).

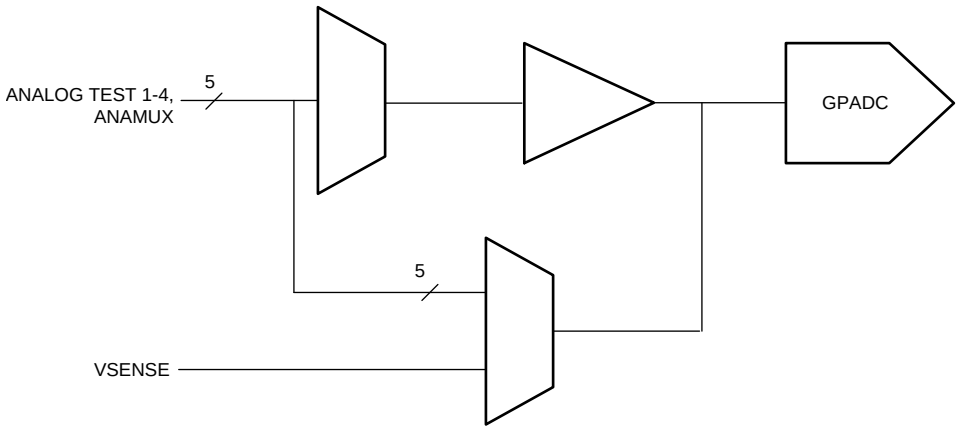


Figure 6-7. ADC Path

Table 6-2. GP-ADC Parameter

PARAMETER	TYP	UNIT
ADC supply	1.8	V
ADC unbuffered input voltage range	0 – 1.8	V
ADC buffered input voltage range (1)	0.4 – 1.3	V
ADC resolution	10	bits
ADC offset error	±5	LSB
ADC gain error	±5	LSB
ADC DNL	–1/+2.5	LSB
ADC INL	±2.5	LSB
ADC sample rate (2)	625	Ksps
ADC sampling time (2)	400	ns
ADC internal cap	10	pF
ADC buffer input capacitance	2	pF

(1) Outside of given range, the buffer output will become nonlinear.
(2) ADC itself is controlled by TI firmware running inside the BIST subsystem. For more details please refer to the API calls.

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Table 6-2. GP-ADC Parameter (continued)

PARAMETER	TYP	UNIT
ADC input leakage current	3	uA

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6.7 Identification

The JTAG identification code is described in the IWR1443 Errata.

The JTAG interface provides the XDS emulator and boundary scan connectivity to the IWR1443.

Table 6-3. JTAG Interface

Signal	SoC Pin	Name	Type	Function
TCK	M13	Test Clock	Input	Free Running clock when used with emulators viz. Spectrum Digital's XDS200 or TI's XDS110
TMS	L13	Test Mode Select	Input	Directs the next state of the JTAG state machine
TDI	H13	Test Data Input	Input	Scan Data Input to the device
TDO	J13	Test Data Output	Output	Scan Data Output of the device

6.8 Boot Modes

As soon as device reset is de-asserted, the R4F processor of the Master (Control) system starts executing its bootloader from an on-chip ROM memory.

The bootloader of the Master system operates in two basic modes and these are specified on the user hardware (Printed Circuit Board) by configuring what are termed as "Sense on Power" (SOP) pins. These pins on the device boundary are scanned by the bootloader firmware and choice of mode for bootloader operation is made.

Table 6-4 enumerates the relevant SOP combinations and how these map to bootloader operation.

Table 6-4. SOP Combinations

SOP2 (P13)	SOP1 (P11)	SOP0 (J13)	BOOTLOADER MODE AND OPERATION
0	0	1	Functional Mode Device Bootloader loads user application from QSPI Serial Flash to internal RAM and switches the control to it
1	0	1	Flashing Mode Device Bootloader spins in loop to allow flashing of user application (or device firmware patch – Supplied by TI) to the serial flash
0	1	1	Debug Mode Bootloader is bypassed and R4F processor is halted. This allows user to connect emulator at a known point

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6.8.1 Flashing Mode

In Flashing Mode, the Master System's bootloader enables the UART driver and expects a data stream comprising of User Application (Binary Image) and Device Firmware (referred to as Device Firmware Patch or Service Pack) from an external flashing utility. Figure 6-8 shows the flashing utility executing on a PC platform, but the protocol can be accomplished on an embedded platform as well.

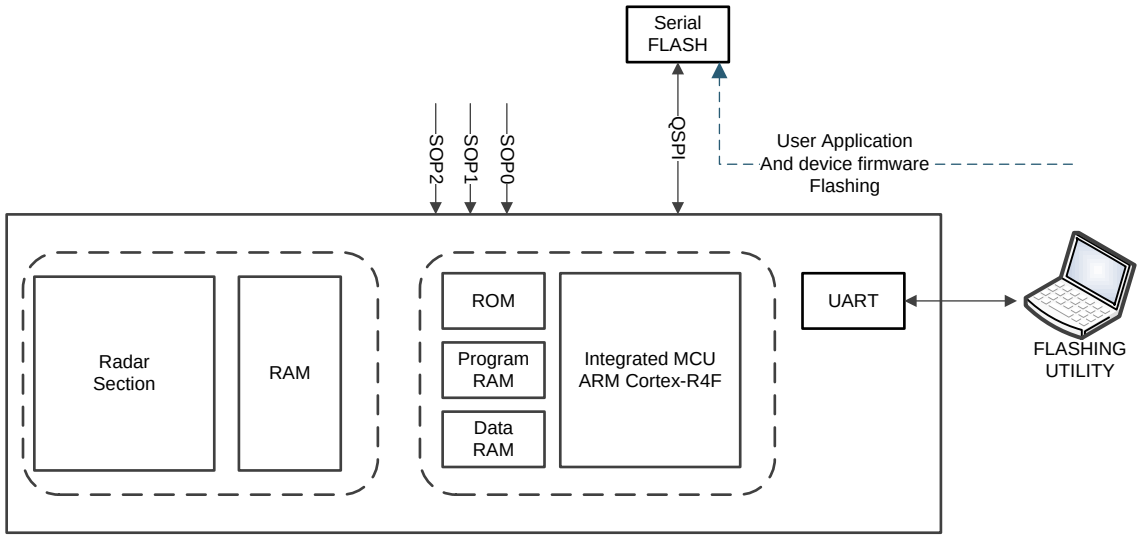


Figure 6-8. Figure 5. Bootloader Flashing Mode

6.8.2 Functional Mode

In Functional Mode, the Master System's bootloader looks for a valid image in the serial flash memory, interfaced over the QSPI port. If a valid image is found, the bootloader transfers the same to Master System's memory subsystem. The image format contains the MSS application code and the radar subsystem patch code.

If a valid image (or the QSPI Serial Flash is not found), the bootloader initializes the SPI port and awaits for the image transfer. This operation comes handy for configurations where the IWR1443 is interfaced to an external processor which has its own nonvolatile storage hence can store the user application and the IWR1443 device's firmware image.

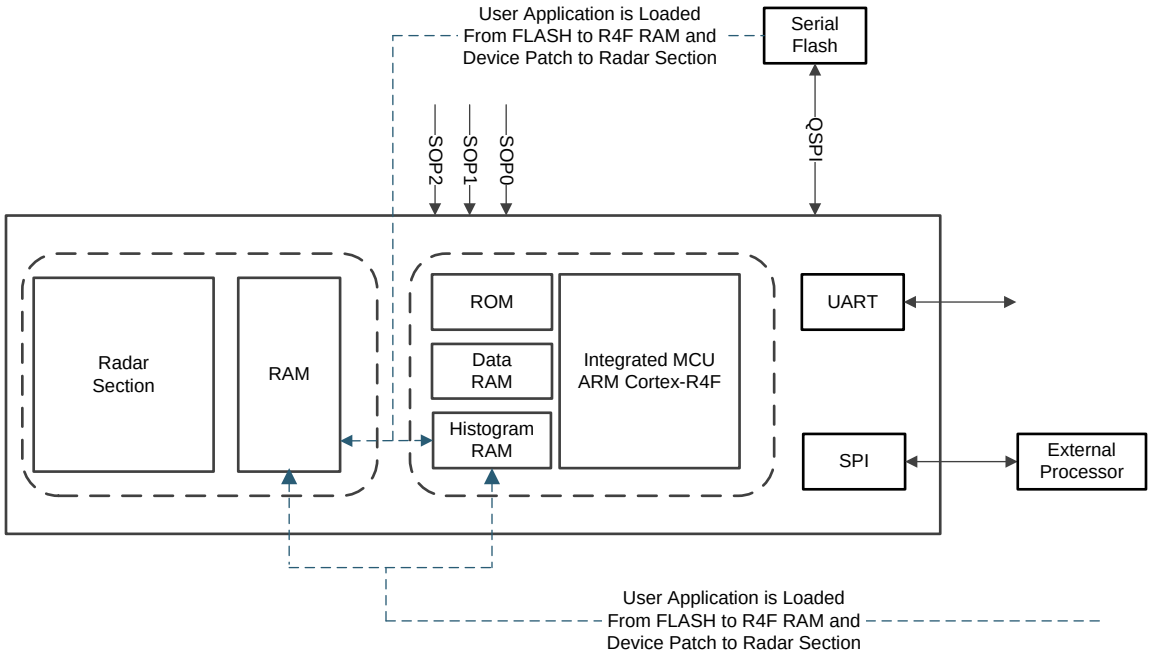


Figure 6-9. Bootloader's Functional Mode

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7 Applications, Implementation, and Layout

NOTE

Information in the following Applications section is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

7.1 Application Information

Application information can be found on IWR Application web page.

7.2 Reference Schematic

The reference schematic and power supply information can be found in the IWR1443 EVM Documentation.

7.3 Layout

7.3.1 Layout Guidelines

General layout guidelines can be found in the IWR1443 EVM Documentation, IWR1443BOOST Layout and Design Files, and IWR1443BOOST Schematics, Assembly Files, and BOM.

7.3.2 Layout Example

The IWR1443 EVM, RF layout can be found in the IWR1443BOOST Layout and Design Files and IWR1443BOOST Schematics, Assembly Files, and BOM.

7.3.3 Stackup Details

Layout Stackup details can be found in the IWR1443BOOST Layout and Design Files and IWR1443BOOST Schematics, Assembly Files, and BOM.

There are specific RF guidelines for the RF Tx and Rx. There are additional layout guidelines for other sections in the IWR1443 Checklist for Schematic Review, Layout Review, Bringup/Wakeup.

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8 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions follow.

8.1 Device Nomenclature

To designate the stages in the product development cycle, TI assigns prefixes to the part numbers of all microprocessors (MPUs) and support tools. Each device has one of three prefixes: X, P, or null (no prefix) (for example, *IWR1443*). Texas Instruments recommends two of three possible prefix designators for its support tools: TMDX and TMDS. These prefixes represent evolutionary stages of product development from engineering prototypes (TMDX) through fully qualified production devices and tools (TMDS).

Device development evolutionary flow:

X Experimental device that is not necessarily representative of the final device's electrical specifications and may not use production assembly flow.

P Prototype device that is not necessarily the final silicon die and may not necessarily meet final electrical specifications.

null Production version of the silicon die that is fully qualified.

Support tool development evolutionary flow:

TMDX Development-support product that has not yet completed Texas Instruments internal qualification testing.

TMDS Fully-qualified development-support product.

X and P devices and TMDX development-support tools are shipped against the following disclaimer:

"Developmental product is intended for internal evaluation purposes."

Production devices and TMDS development-support tools have been characterized fully, and the quality and reliability of the device have been demonstrated fully. TI's standard warranty applies.

Predictions show that prototype devices (X or P) have a greater failure rate than the standard production devices. Texas Instruments recommends that these devices not be used in any production system because their expected end-use failure rate still is undefined. Only qualified production devices are to be used.

TI device nomenclature also includes a suffix with the device family name. This suffix indicates the package type (for example, ABL0161), the temperature range (for example, blank is the default commercial temperature range). Figure 8-1 provides a legend for reading the complete device name for any *IWR1443* device.

For orderable part numbers of *IWR1443* devices in the ABL0161 package types, see the Package Option Addendum of this document, the TI website (www.ti.com), or contact your TI sales representative.

For additional description of the device nomenclature markings on the die, see the *IWR1443 Device Errata*.

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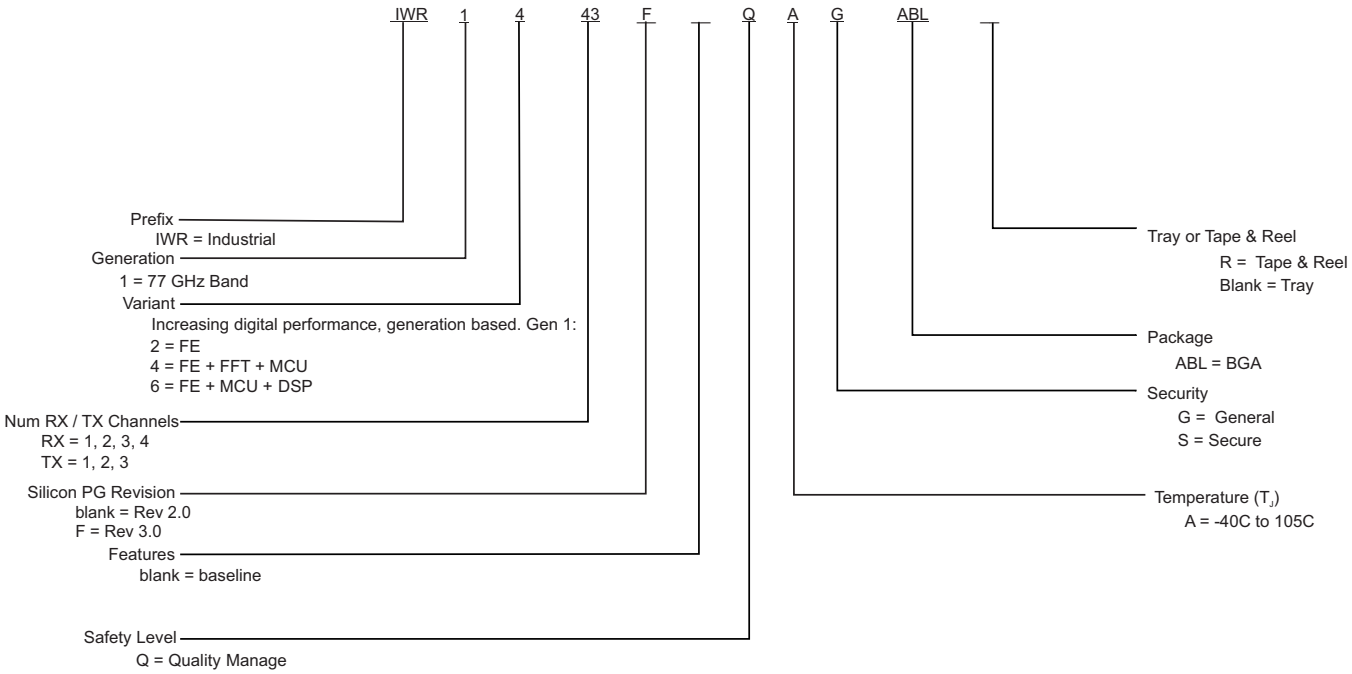


Figure 8-1. Device Nomenclature

8.2 Tools and Software

Models

IWR1443 BSDL Model Boundary scan database of testable input and output pins for IEEE 1149.1 of the specific device.

IWR1443 IBIS Model IO buffer information model for the IO buffers of the device. For simulation on a circuit board, see IBIS Open Forum.

I\WR1443 Checklist for Schematic Review, Layout Review, Bringup/Wakeup A set of steps in spreadsheet form to select system functions and pinmux options. Specific EVM schematic and layout notes to apply to customer engineering. A bringup checklist is suggested for customers.

8.3 Documentation Support

To receive notification of documentation updates—including silicon errata—go to the product folder for your device on ti.com (IWR1443). In the upper right corner, click the "Alert me" button. This registers you to receive a weekly digest of product information that has changed (if any). For change details, check the revision history of any revised document.

The current documentation that describes the DSP, related peripherals, and other technical collateral follows.

Errata

IWR1443 Device Errata Describes known advisories, limitations, and cautions on silicon and provides workarounds.

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8.4 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community The TI engineer-to-engineer (E2E) community was created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

TI Embedded Processors Wiki Established to help developers get started with Embedded Processors from Texas Instruments and to foster innovation and growth of general knowledge about the hardware and software surrounding these devices.

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8.8 Glossary

TI Glossary This glossary lists and explains terms, acronyms, and definitions.

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9 Mechanical, Packaging, and Orderable Information

9.1 Packaging Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

注意

The following package information is subject to change without notice.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
IWR1443FQAGABL	Active	Production	FCCSP (ABL) | 161	176 | JEDEC TRAY (10+1)	Yes	Call TI | Snagcu	Level-3-260C-168 HR	-40 to 105	IWR1443 QG 964FC
IWR1443FQAGABL.B	Active	Production	FCCSP (ABL) | 161	176 | JEDEC TRAY (10+1)	Yes	Call TI	Level-3-260C-168 HR	-40 to 105	IWR1443 QG 964FC
IWR1443FQAGABLR	Active	Production	FCCSP (ABL) | 161	1000 | LARGE T&R	-	Call TI | Snagcu	Level-3-260C-168 HR	-40 to 105	IWR1443 QG 964FC
IWR1443FQAGABLR.B	Active	Production	FCCSP (ABL) | 161	1000 | LARGE T&R	-	Call TI	Level-3-260C-168 HR	-40 to 105	IWR1443 QG 964FC

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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GENERIC PACKAGE VIEW

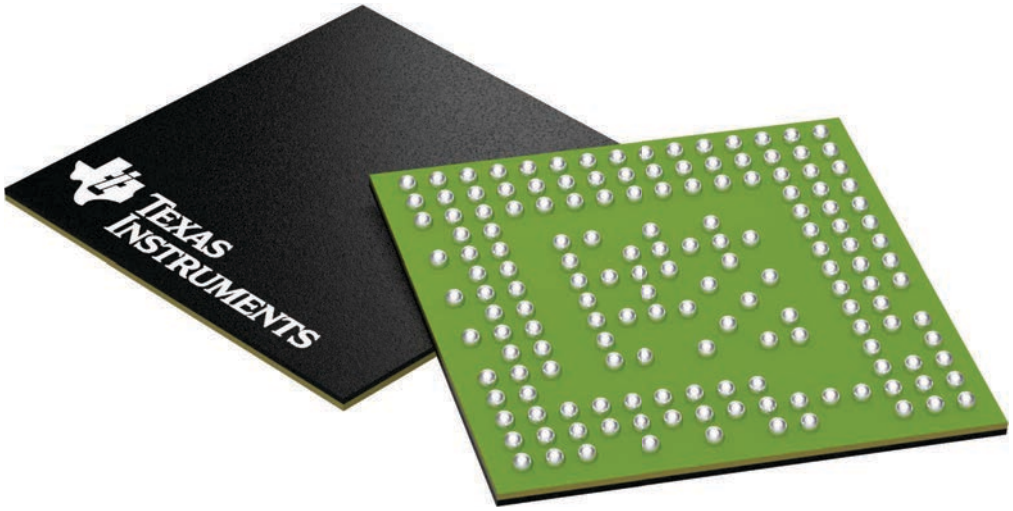
ABL 161

FCBGA - 1.17 mm max height

10.4 x 10.4, 0.65 mm pitch

PLASTIC BALL GRID ARRAY

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4225978/A

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