TEXAS INSTRUMENTS
LF412-N-MIL
JAJSDH1 – JUNE 2017

LF412-N-MIL 低オフセット、低ドリフト、デュアルJFET入力オペアンプ

1 特長

- 内部的にオフセット電圧をトリム: 1mV (最大値)
- 入力オフセット電圧ドリフト: 7µV/℃ (標準値)
- 低い入力バイアス電流: 50pA
- 低い入力ノイズ電流: 0.01pA/$\sqrt{Hz}$
- 広いゲイン帯域幅: 3MHz (最小値)
- 高いスルー・レート: 10V/µs (最小値)
- 低い消費電流: 1.8mA/アンプ
- 高い入力インピーダンス: $10^{12}\Omega$
- 低い全高調波歪み: 0.02%以下
- 低い1/fノイズ・コーナー: 50Hz
- 短いセトリング時間: 0.01%まで2µs

2 アプリケーション

- 高速積分器
- 高速D/Aコンバータ
- サンプル・アンド・ホールド回路

3 概要

これらのデバイスは低コスト、高速のJFET入力オペアンプで、入力オフセット電圧と入力オフセット電圧ドリフトが非常に低いことが特長です。低い消費電力で、大きなゲイン帯域幅積と高速なスルー・レートを維持します。さらに、高電圧JFET入力デバイスとの適切なマッチングにより、非常に低い入力バイアスとオフセット電流を実現しています。LF412-N-MILデュアルはLM1558とピン互換で、設計者は既存の設計の総合的な性能をすぐにアップグレードできます。

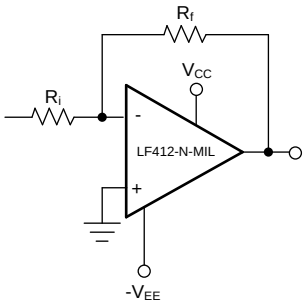
これらのアンプは、高速積分器、高速D/Aコンバータ、サンプル・アンド・ホールド回路、その他低い入力オフセット電圧とドリフト、低い入力バイアス電流、高い入力インピーダンス、高いスルー・レート、広い帯域幅を必要とする多くの回路のアプリケーションに使用できます。

製品情報(1)

型番	パッケージ	本体サイズ(公称)
LF412-N-MIL	PDIP (8)	9.59mm×6.35mm
	TO (8)	直径9.14mm

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。

反転アンプ



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English Data Sheet: SNOSD56

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4 改訂履歴

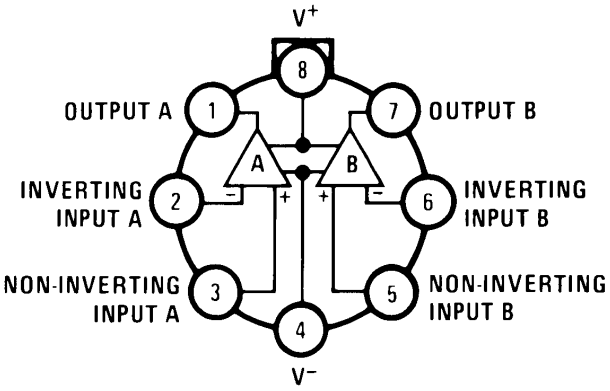
資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

日付	改訂内容	注
2017年6月	*	初版

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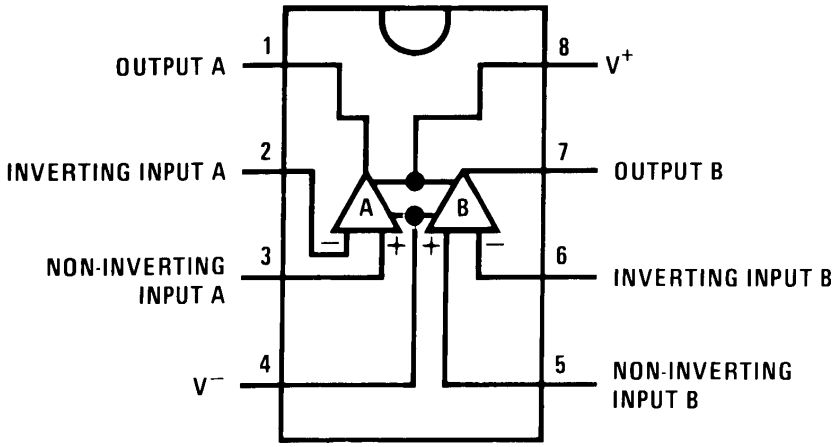
5 Pin Configuration and Functions

LMC Package
8-Pin TO
Top View



Note. Pin 4 connected to case.

P Package
8-Pin PDIP
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
Inverting input A	2	I	Amplifier A inverting input
Inverting input B	6	I	Amplifier B inverting input
Noninverting input A	3	I	Amplifier A noninverting input
Noninverting input B	5	I	Amplifier B noninverting input
Output A	1	O	Amplifier A output
Output B	7	O	Amplifier B output
V+	8	P	Positive supply
V-	4	P	Negative supply

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

	MIN	MAX	UNIT
Supply voltage	–18	18	V
Differential input voltage	–30	30	V
Input voltage range			
Output short circuit duration	Continuous		
Power dissipation	670		mW
T_J maximum		115	°C
Operating temperature range	See *Thermal Information*		
Storage temperature, T_{stg}	−65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

		VALUE	UNIT
$V_{(ESD)}$ Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±1700	V
	Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1700	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 500-V HBM is possible with the necessary precautions. Pins listed as ±1700 V may actually have higher performance.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 250-V CDM is possible with the necessary precautions. Pins listed as ±1700 V may actually have higher performance.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	NOM	MAX	UNIT
Supply voltage			±15	V

6.4 Thermal Information

THERMAL METRIC(1)		LF412-N-MIL		UNIT
		LMC (TO)	P (PDIP)	
		8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance (typical)	152	115	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

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6.5 DC Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		LF412-N-MIL (1)			UNIT
				MIN	TYP	MAX	
V_{OS}	Input offset voltage	R_S =10 kΩ, T_A = 25°C			1	3	mV
$\Delta V_{OS}/\Delta T$	Average TC of input offset voltage	R_S = 10 kΩ			7		μV/°C
I_{OS}	Input offset current	V_S = ±15 V (2)	T_J = 25°C		25	100	pA
			T_J = 70°C			2	nA
			T_J = 125°C			25	nA
I_B	Input bias current	V_S=±15V (2) (2)	T_J = 25°C		50	200	pA
			T_J = 70°C			4	nA
			T_J = 125°C			50	nA
R_{IN}	Input resistance	T_J = 25°C			10^{12}		Ω
A_{VOL}	Large signal voltage gain	R_L = 2 k, T_A = 25°C, V_S = ±15 V, V_O = ±10 V		25	200		V/mV
		Over temperature		15	200		
V_O	Output voltage swing	V_S = ±15 V, R_L = 10 k		±12	±13.5		V
V_{CM}	Input common-mode voltage range			±11	14.5		V
					−11.5		V
CMRR	Common-mode rejection ratio	R_S ≤ 10 k		70	100		dB
PSRR	Supply voltage rejection ratio			(3)70	100		dB
I_S	Supply current	V_O = 0 V, R_L = ∞			3.6	6.5	mA

(1) Unless otherwise specified, the specifications apply over the full temperature range and for V_S = ±15 V for the LF412-N-MIL. V_{OS}, I_B, and I_{OS} are measured at V_{CM} = 0.

(2) The input bias currents are junction leakage currents which approximately double for every 10°C increase in the junction temperature, T_J. Due to limited production test time, the input bias currents measured are correlated to junction temperature. In normal operation the junction temperature rises above the ambient temperature as a result of internal power dissipation, P_D. $T_J = T_A + \theta_{JA} P_D$ where θ_{JA} is the thermal resistance from junction to ambient. Use of a heat sink is recommended if input bias current is to be kept to a minimum.

(3) Supply voltage rejection ratio is measured for both supply magnitudes increasing or decreasing simultaneously in accordance with common practice. V_S = ±6 V to ±15 V.

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6.6 AC Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	LF412-N-MIL (1)			UNIT
			MIN	TYP	MAX	
	Amplifier to amplifier coupling	T_A = 25°C f = 1 Hz – 20 kHz (Input referred)		−120		dB
SR	Slew rate	V_S = ±15 V T_A = 25°C	8	15		V/μs
GBW	Gain-bandwidth product	V_S = ±15 V T_A = 25°C	2.7	4		MHz
THD	Total harmonic dist	A_V = 10 R_L = 10 k V_O = 20 Vp-p BW = 20 Hz – 20 kHz		≤0.02%		
e_n	Equivalent input noise voltage	T_A = 25°C R_S = 100 Ω f = 1 kHz		25		nV / $\sqrt{Hz}$
i_n	Equivalent input noise current	T_A = 25°C, f = 1 kHz		0.01		pA / $\sqrt{Hz}$

(1) Unless otherwise specified, the specifications apply over the full temperature range and for V_S = ±15 V for the LF412-N-MIL. V_{OS}, I_B, and I_{OS} are measured at V_{CM} = 0.

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6.7 Typical Characteristics

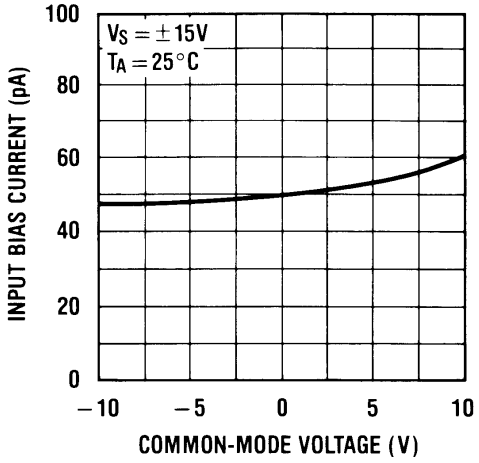


図 1. Input Bias Current

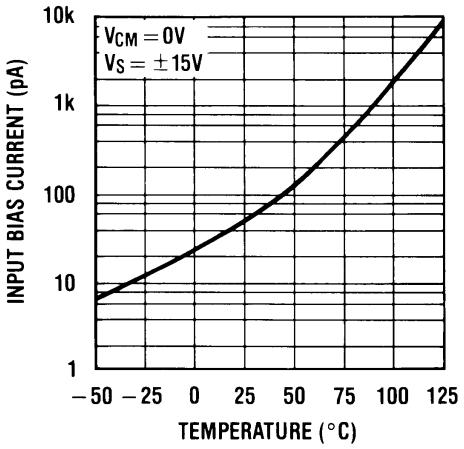


図 2. Input Bias Current

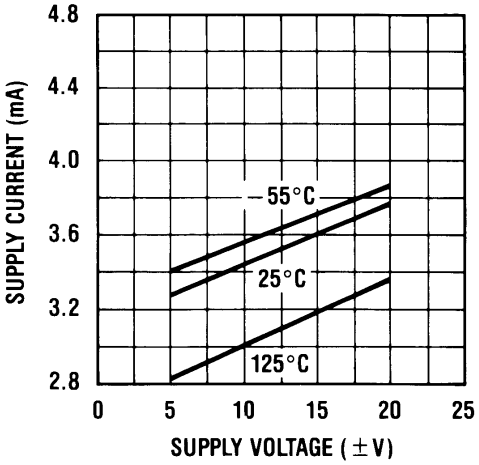


図 3. Supply Current

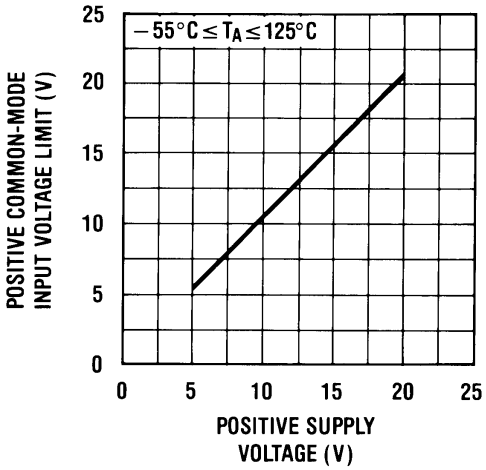


図 4. Positive Common-Mode Input Voltage Limit

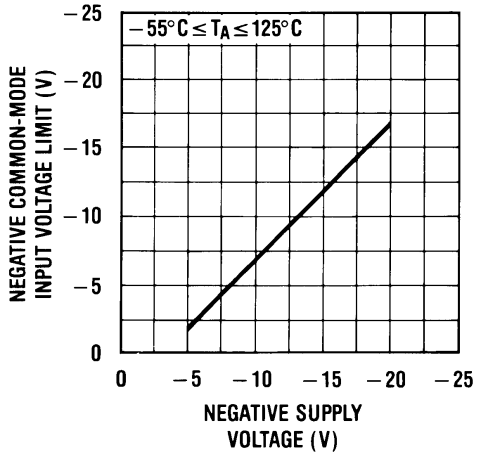


図 5. Negative Common-Mode Input Voltage Limit

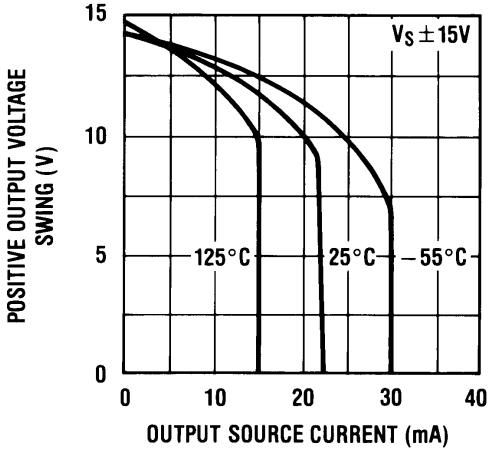


図 6. Positive Current Limit

Typical Characteristics (continued)

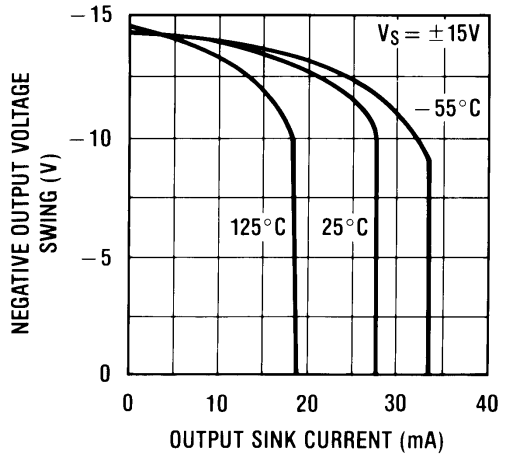


図 7. Negative Current Limit

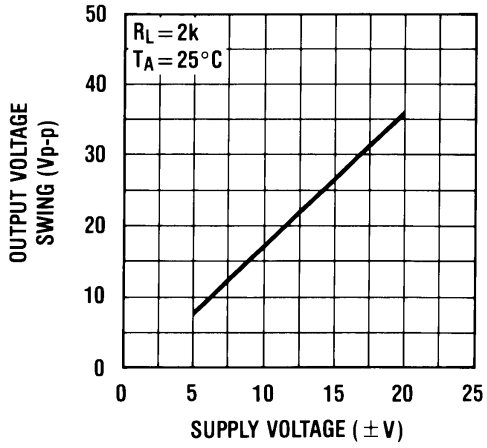


図 8. Output Voltage Swing

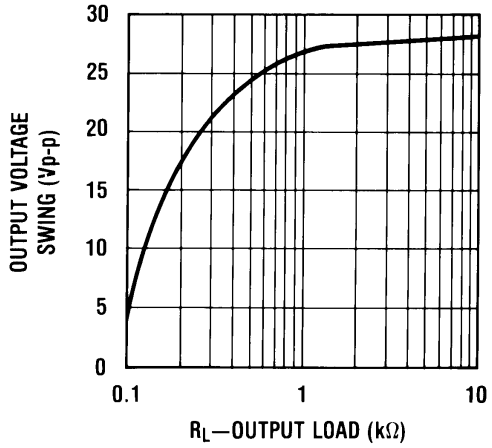


図 9. Output Voltage Swing

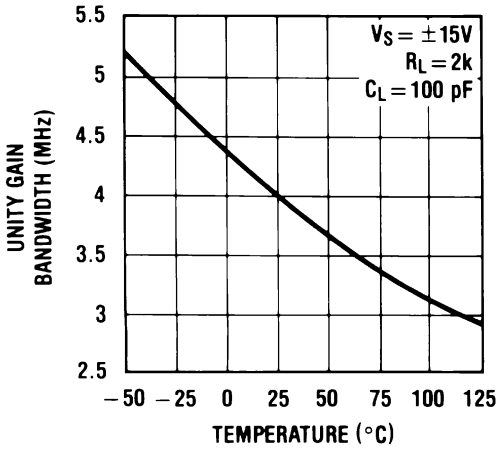


図 10. Gain Bandwidth

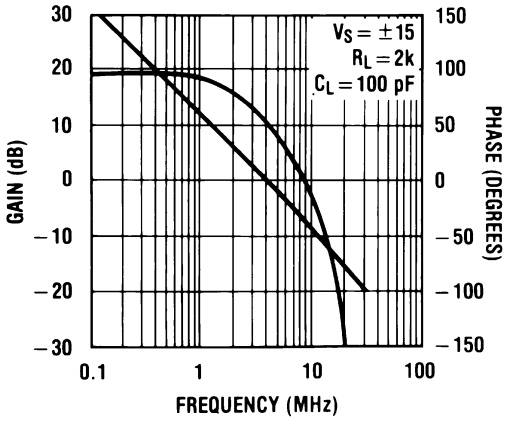


図 11. Bode Plot

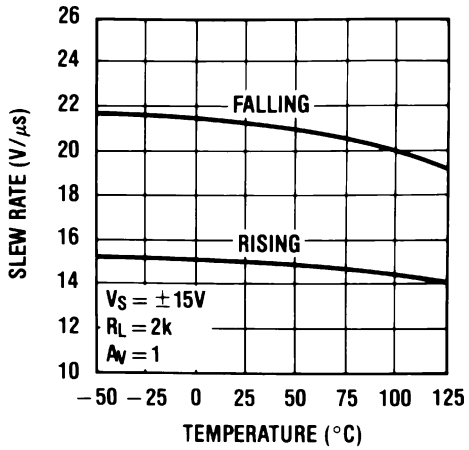


図 12. Slew Rate

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Typical Characteristics (continued)

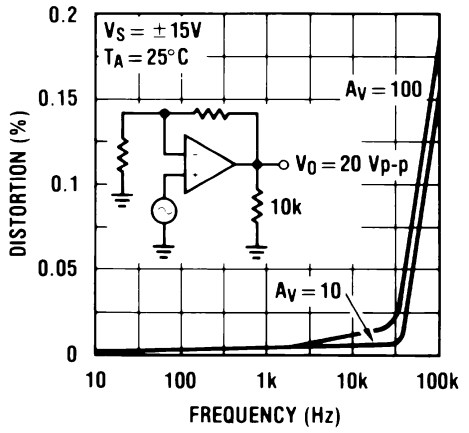


図 13. Distortion vs Frequency

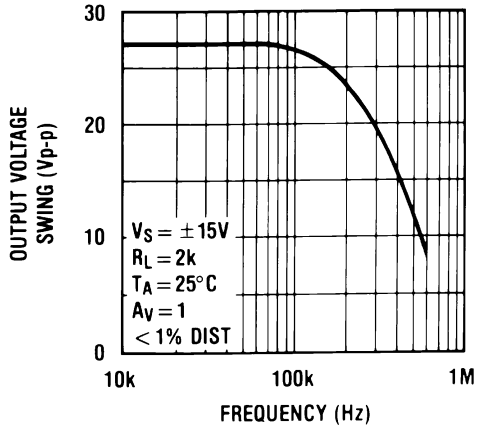


図 14. Undistorted Output Voltage Swing

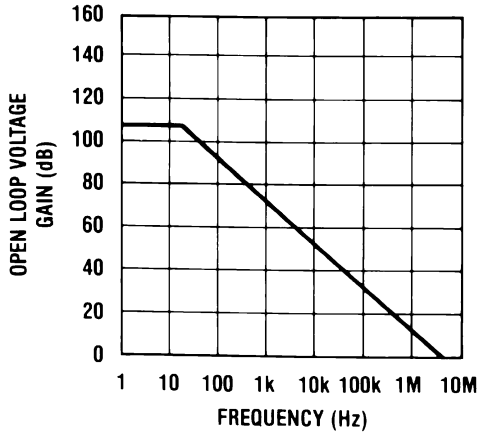


図 15. Open Loop Frequency Response

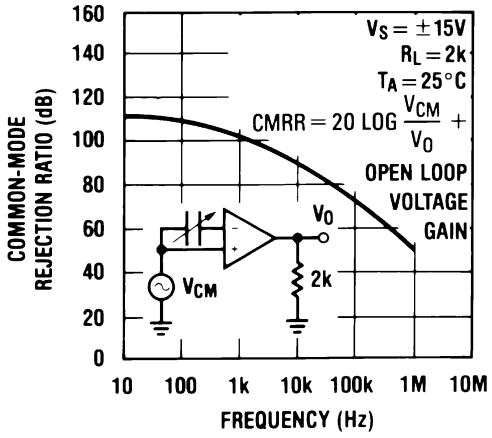


図 16. Common-Mode Rejection Ratio

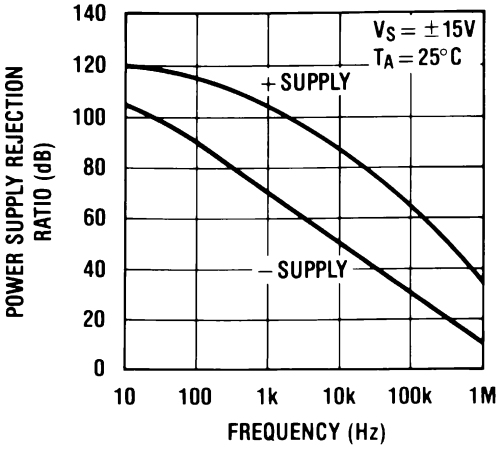


図 17. Power Supply Rejection Ratio

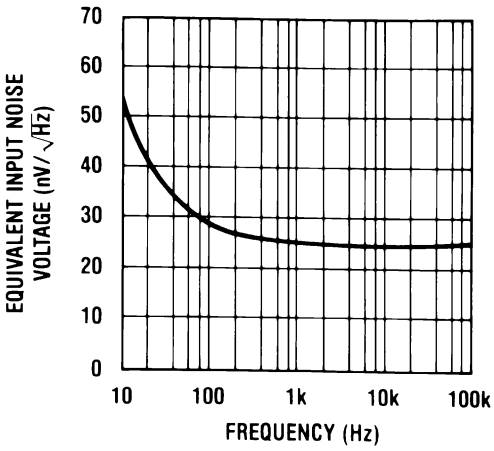


図 18. Equivalent Input Noise Voltage

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Typical Characteristics (continued)

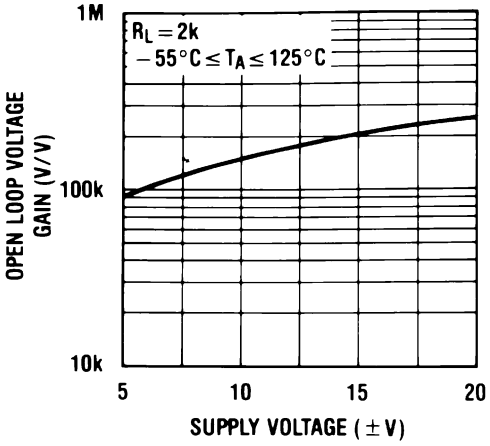


図 19. Open Loop Voltage Gain

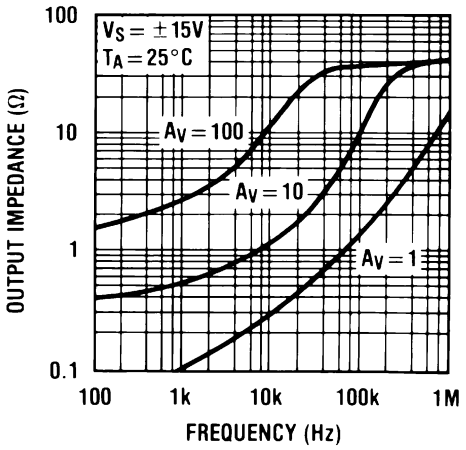


図 20. Output Impedance

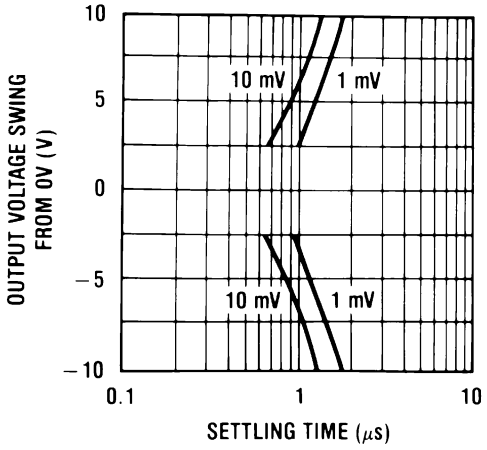
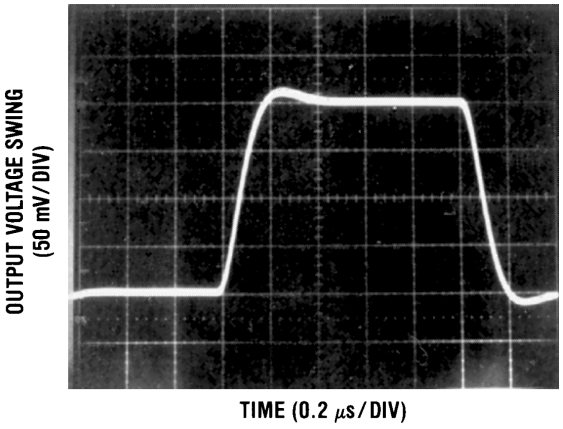
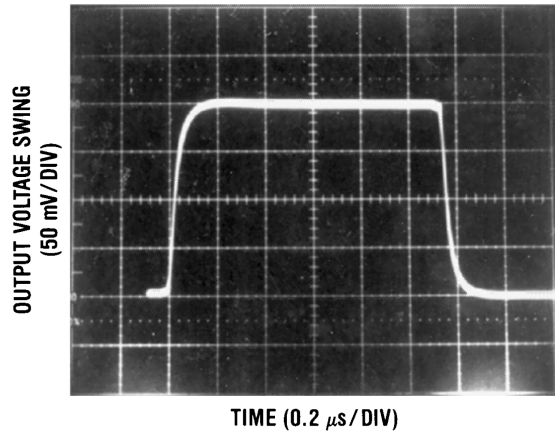


図 21. Inverter Settling Time



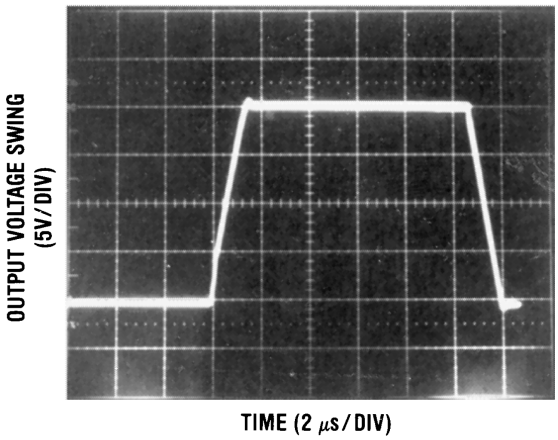
R_L = 2 kΩ C_L = 10 pF

図 22. Small Signal Inverting



R_L = 2 kΩ C_L = 10 pF

図 23. Small Signal Non-Inverting

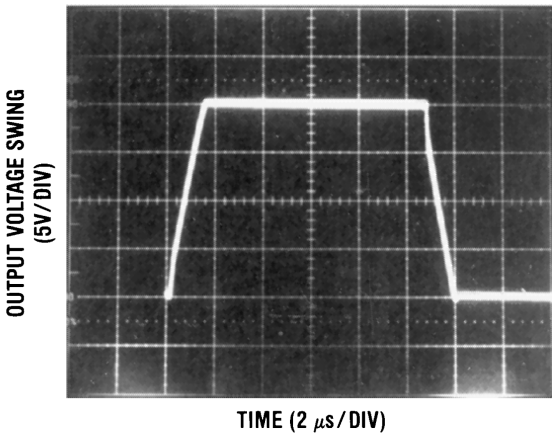


R_L = 2 kΩ C_L = 10 pF

図 24. Large Signal Inverting

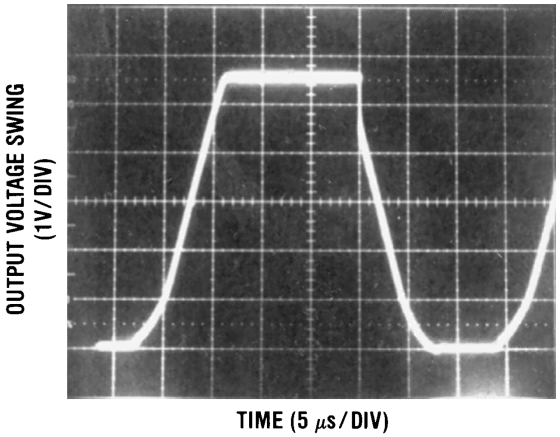
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Typical Characteristics (continued)



R_L = 2 kΩ C_L = 10 pF

図 25. Large Signal Non-Inverting



R_L = 100 Ω C_L = 10 pF

図 26. Current Limit

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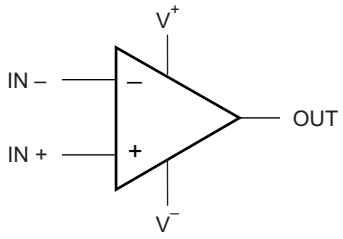
7 Detailed Description

7.1 Overview

The LF412-N-MIL devices are low cost, high speed, JFET input operational amplifiers with very low input offset voltage and input offset voltage drift. They require low supply current yet maintain a large gain bandwidth product and fast slew rate. In addition, well matched high voltage JFET input devices provide very low input bias and offset currents. The LF412-N-MIL dual is pin compatible with the LM1558, allowing designers to immediately upgrade the overall performance of existing designs.

These amplifiers may be used in applications such as high speed integrators, fast D/A converters, sample and hold circuits and many other circuits requiring low input offset voltage and drift, low input bias current, high input impedance, high slew rate and wide bandwidth.

7.2 Functional Block Diagram



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図 27. Each Amplifier

7.3 Feature Description

The amplifier's differential inputs consist of a non-inverting input (+IN) and an inverting input (-IN). The amplifier amplifies only the difference in voltage between the two inputs, which is called the differential input voltage. The output voltage of the op-amp V_{OUT} is given by the equation $V_{OUT} = A_{OL}(IN+ - IN-)$.

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7.4 Device Functional Modes

7.4.1 Input and Output Stage

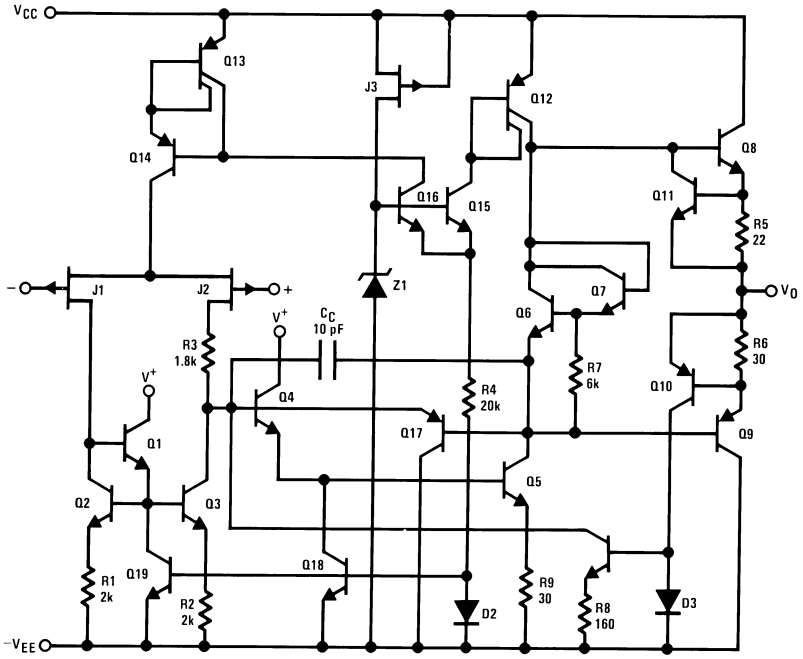


図 28. 1/2 Dual LF412-N-MIL

8 Application and Implementation

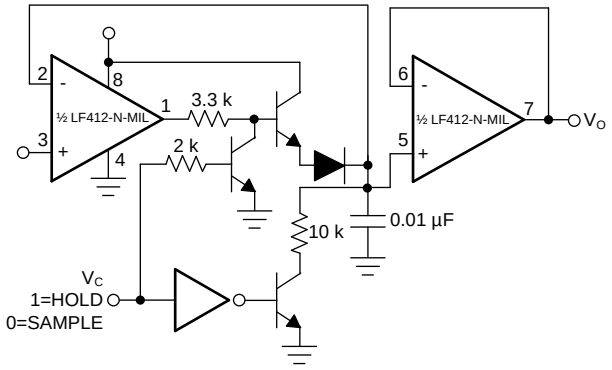
注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The LF412-N-MIL series of JFET input dual op amps are internally trimmed (BI-FET II™) providing very low input offset voltages and input offset voltage drift. These JFETs have large reverse breakdown voltages from gate to source and drain eliminating the need for clamps across the inputs. Therefore, large differential input voltages can easily be accommodated without a large increase in input current. The maximum differential input voltage is independent of the supply voltages. However, neither of the input voltages should be allowed to exceed the negative supply as this will cause large currents to flow which can result in a destroyed unit.

8.2 Typical Application



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図 29. Single-Supply Sample and Hold

8.2.1 Design Requirements

Single-supply.

8.2.2 Detailed Design Procedure

Exceeding the negative common-mode limit on either input will cause a reversal of the phase to the output and force the amplifier output to the corresponding high or low state.

Exceeding the negative common-mode limit on both inputs will force the amplifier output to a high state. In neither case does a latch occur since raising the input back within the common-mode range again puts the input stage and thus the amplifier in a normal operating mode.

Exceeding the positive common-mode limit on a single input will not change the phase of the output, however, if both inputs exceed the limit, the output of the amplifier may be forced to a high state.

The amplifiers will operate with a common-mode input voltage equal to the positive supply; however, the gain bandwidth and slew rate may be decreased in this condition. When the negative common-mode voltage swings to within 3V of the negative supply, an increase in input offset voltage may occur.

Each amplifier is individually biased by a zener reference which allows normal circuit operation on ±6 V power supplies. Supply voltages less than these may result in lower gain bandwidth and slew rate.

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Typical Application (continued)

The amplifiers will drive a 2 kΩ load resistance to ±10 V over the full temperature range. If the amplifier is forced to drive heavier load currents, however, an increase in input offset voltage may occur on the negative voltage swing and finally reach an active current limit on both positive and negative swings.

Precautions should be taken to ensure that the power supply for the integrated circuit never becomes reversed in polarity or that the unit is not inadvertently installed backwards in a socket as an unlimited current surge through the resulting forward diode within the IC could cause fusing of the internal conductors and result in a destroyed unit.

As with most amplifiers, care should be taken with lead dress, component placement and supply decoupling in order to ensure stability. For example, resistors from the output to an input should be placed with the body close to the input to minimize “pick-up” and maximize the frequency of the feedback pole by minimizing the capacitance from the input to ground.

A feedback pole is created when the feedback around any amplifier is resistive. The parallel resistance and capacitance from the input of the device (usually the inverting input) to AC ground set the frequency of the pole. In many instances the frequency of this pole is much greater than the expected 3 dB frequency of the closed loop gain and consequently there is negligible effect on stability margin. However, if the feedback pole is less than approximately 6 times the expected 3 dB frequency a lead capacitor should be placed from the output to the input of the op amp. The value of the added capacitor should be such that the RC time constant of this capacitor and the resistance it parallels is greater than or equal to the original feedback pole time constant.

8.2.3 Application Curves

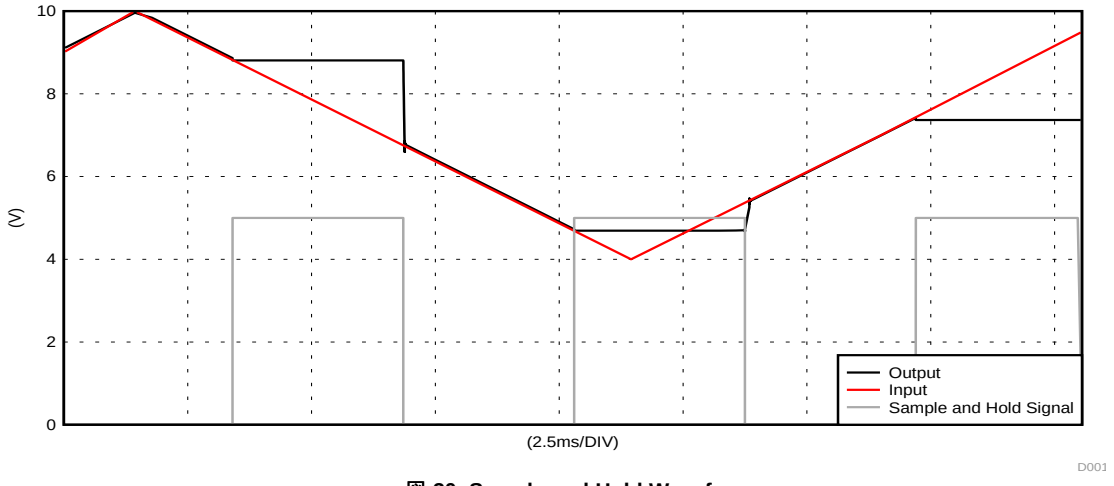


図 30. Sample and Hold Waveforms

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9 Power Supply Recommendations

For proper operation, the power supplies must be properly decoupled. For decoupling the supply lines it is suggested that 0.1 µF capacitors be placed as close as possible to the op amp power supply pins. The minimum power supply voltage is ±5 V.

10 Layout

10.1 Layout Guidelines

As with most amplifiers, care should be taken with lead dress, component placement and supply decoupling in order to ensure stability. For example, resistors from the output to an input should be placed with the body close to the input to minimize “pick-up” and maximize the frequency of the feedback pole by minimizing the capacitance from the input to ground.

10.2 Layout Example

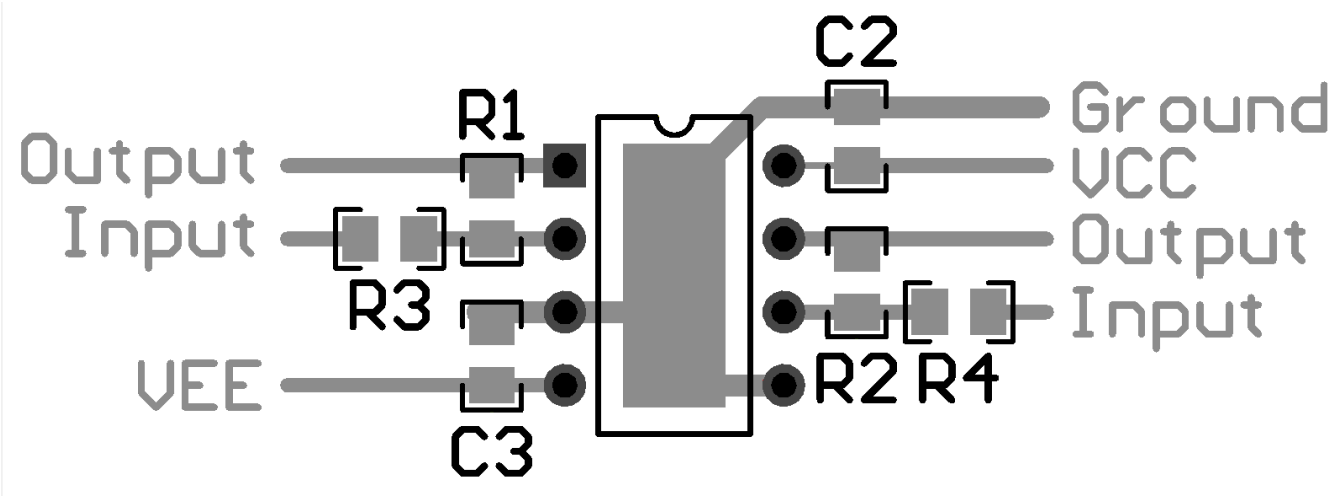


図 31. LF412-N-MIL Layout

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11.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LF412MH	Active	Production	TO-99 (LMC) | 8	500 | OTHER	No	Call TI	Level-1-NA-UNLIM	-55 to 125	(LF412MH, LF412MH)
LF412MH/NOPB	Active	Production	TO-99 (LMC) | 8	500 | OTHER	Yes	Call TI	Level-1-NA-UNLIM	-55 to 125	(LF412MH, LF412MH)

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

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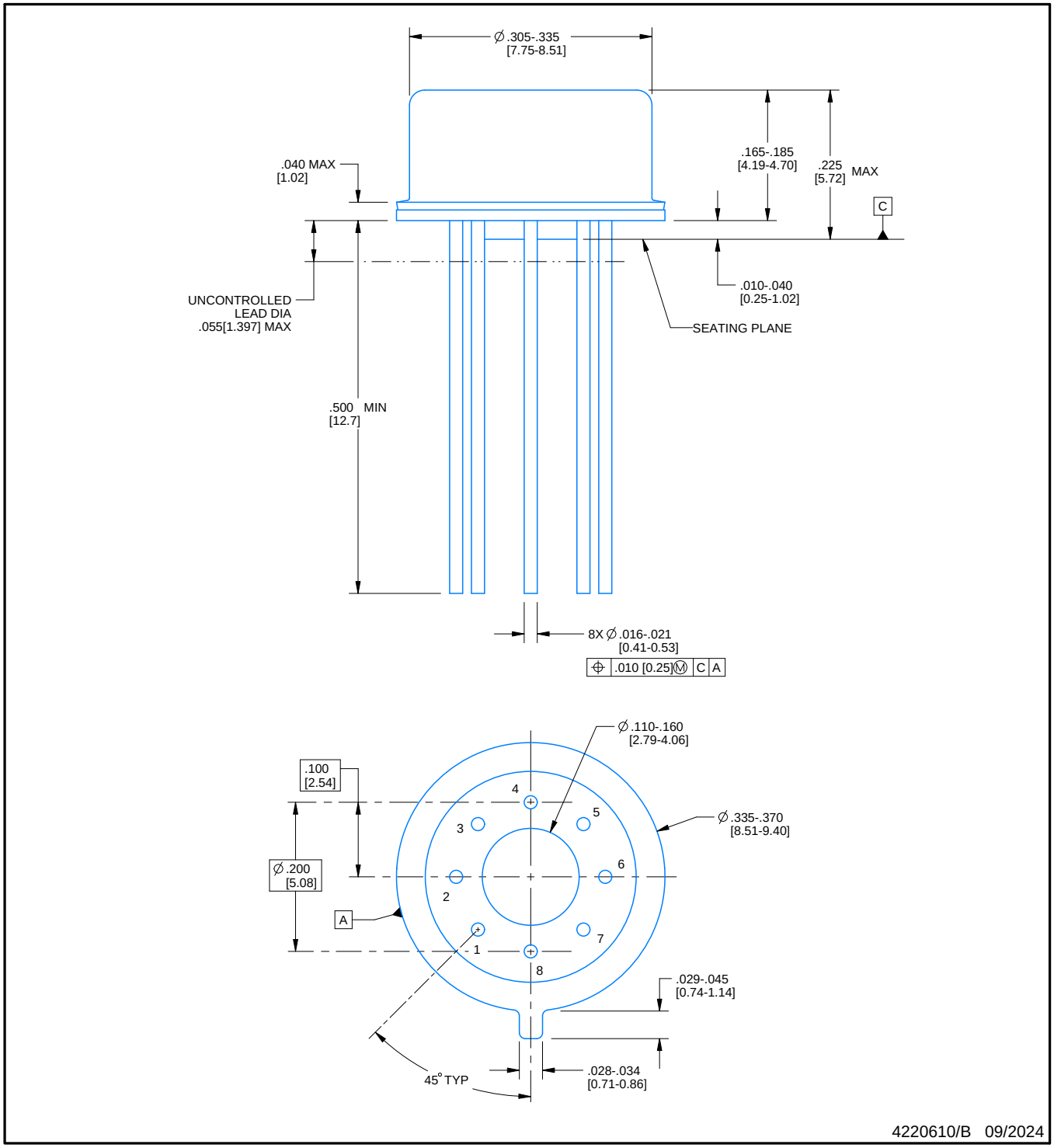
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LMC0008A

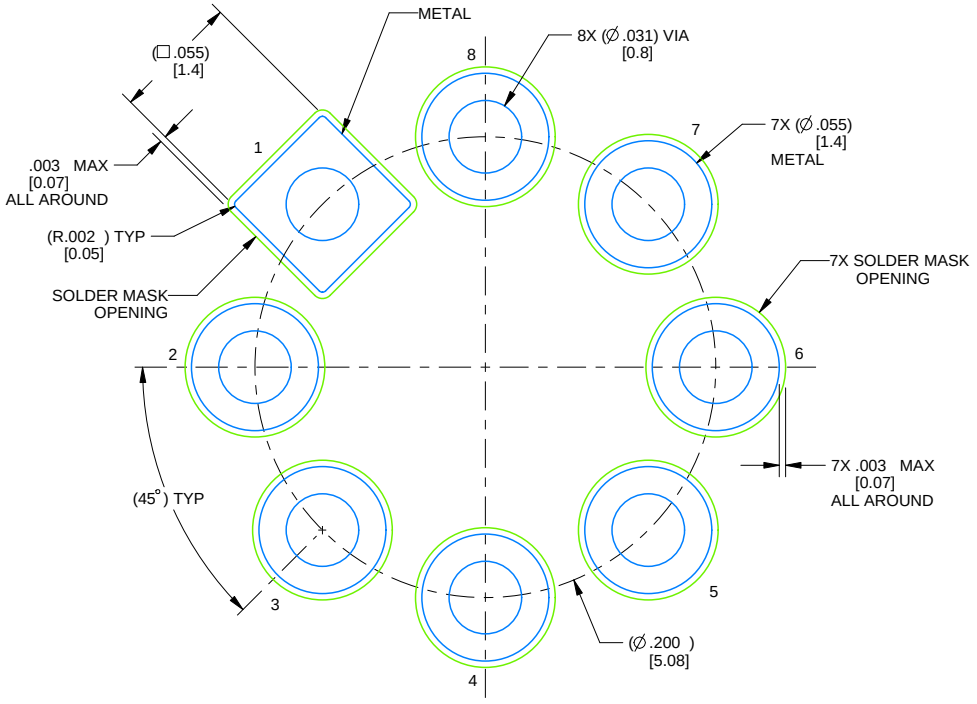
TO-CAN - 5.72 mm max height

TRANSISTOR OUTLINE



NOTES:

1. All linear dimensions are in inches [millimeters]. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Pin numbers shown for reference only. Numbers may not be marked on package.
4. Reference JEDEC registration MO-002/TO-99.



LAND PATTERN EXAMPLE
NON-SOLDER MASK DEFINED
SCALE: 12X

4220610/B 09/2024

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