LM117HVQML-SP RHA 4.25V～60V 3 端子可変レギュレータ

1 特長

- 吸収線量 (TID) 100krad(Si) までの放射線耐性保証 (RHA)
  - 50～300rad(Si)/s の高線量率 (HDR) オプション
  - 10mrad(Si)/s の低線量率 (LDR) オプション
- 0.5A の出力電流を規定
- 可変出力電圧：最小 1.2V
- 温度に対して一定の電流制限
- 出力の短絡保護

2 アプリケーション

- 衛星用電源システム (EPS)

3 概要

LM117HVQML-SP 3 端子正電圧可変リニア・レギュレータは 1.2V～57V の出力範囲で 0.5A を供給できます。本デバイスは簡単に使用でき、2 つの外付け抵抗だけで出力電圧を設定できます。

本レギュレータはフローティング状態で実装され、入出力電圧差のみを監視するため、入出力電圧差の最大値を超過しない限り、数百ボルトの電源でもレギュレート可能です。

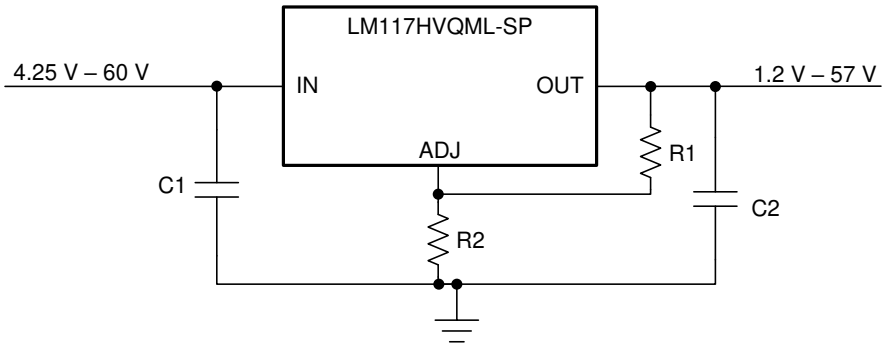
フライトで実証済みの LM117HVQML-SP には、電流制限、熱過負荷保護、安全領域保護など、完全な過負荷保護機能が搭載されています。本デバイスは非常に多目的であり、可変スイッチング・レギュレータ、プログラマブル出力レギュレータ、高精度電流レギュレータなどとしても使用できます。

低電圧アプリケーション向けに、41.25V 以下に適したピン互換ドロップイン代替品として LM117QML-SP を提供しています。負電圧の補完製品については、LM137QML-SP データシートを参照してください。

製品情報

部品番号 (1)	グレード (2)	パッケージ (3)
LM117HVGWRLQMLV	フライト・グレードの QMLV、LDR (10mrad/s) で RHA 100krad(Si)	CFP SOIC (NAC) 16 ピン 6.35mm × 9.91mm 質量 = 0.467g (5)
5962R0722962VZA		
LM117HVGWRQMLV	フライト・グレードの QMLV、HDR (50～300rad/s) で RHA 100krad(Si)	
5962R0722902VZA		
LM117HVNAC/EM	エンジニアリング・サンプル (4)	
LM117HVHRLQMLV	フライト・グレードの QMLV、LDR (10mrad/s) で RHA 100krad(Si)	TO-39 (NDT) 3 ピン 8.26mm × 8.26mm 質量 = 1.036g (5)
5962R0722961VXA		
LM117HVHRQMLV	フライト・グレードの QMLV、HDR (50～300rad/s) で RHA 100krad(Si)	
5962R0722901VXA		
LM117HVH MDE	フライト・グレードの QMLV、LDR (10mrad/s) で RHA 100krad(Si)	ダイ 2.18mm × 2.36mm
5962R0722961V9A		
LM117HVH MDR	フライト・グレードの QMLV、HDR (50～300rad/s) で RHA 100krad(Si)	
5962R0722901V9A		

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。
(2) 部品のグレードの詳細は、SLYB235 をご覧ください。
(3) 梱包の詳細は、TI のパッケージのページを参照してください。
(4) これらのユニットは、エンジニアリング評価のみを目的としており、標準とは異なるフローに従って処理されています。認定、量産、放射線テスト、航空での使用には適していません。MIL に規定されている温度範囲全体 (–55℃～125℃) にわたる性能も動作寿命全体にわたる性能も保証されていません。
(5) 質量の精度は ±10% です。



概略回路図

英語版の TI 製品についての情報を翻訳したこの資料は、製品の概要を確認する目的で便宜的に提供しているものです。該当する正式な英語版の最新情報は、www.ti.com で閲覧でき、その内容が常に優先されます。TI では翻訳の正確性および妥当性につきましては一切保証いたしません。実際の設計などの前には、必ず最新版の英語版をご参照くださいますようお願いいたします。

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4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

DATE	REVISION	NOTES
October 2021	*	Initial release. Device split from shared data sheet (SNVS357).

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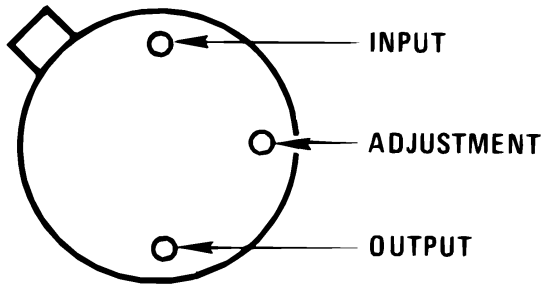
5 Related Products

PART NUMBER	INPUT VOLTAGE RANGE	I_{OUT}	PART NUMBER SUFFIX	PACKAGE	RADIATION TESTING (1)
LM117QML-SP	4.25 V to 41.25 V	1.5 A	K	TO-3 (K) 2 pin	HDR 100 krad(Si)
		0.5 A	H	TO-39 (NDT) 3 pin	LDR 100 krad(Si)
					HDR 100 krad(Si)
				Die	LDR 100 krad(Si)
					HDR 100 krad(Si)
			GW	CFP SOIC (NAC) 16 pin	LDR 100 krad(Si)
					HDR 100 krad(Si)
LM117HVQML-SP	4.25 V to 60 V	0.5 A	H	TO-39 (NDT) 3 pin	LDR 100 krad(Si)
					HDR 100 krad(Si)
				Die	LDR 100 krad(Si)
					HDR 100 krad(Si)
			GW	CFP SOIC (NAC) 16 pin	LDR 100 krad(Si)
					HDR 100 krad(Si)
LM137QML-SP	–41.25 V to –4.25 V	1.5 A	H	TO-39 (NDT) 3 pin	HDR 30 krad(Si)

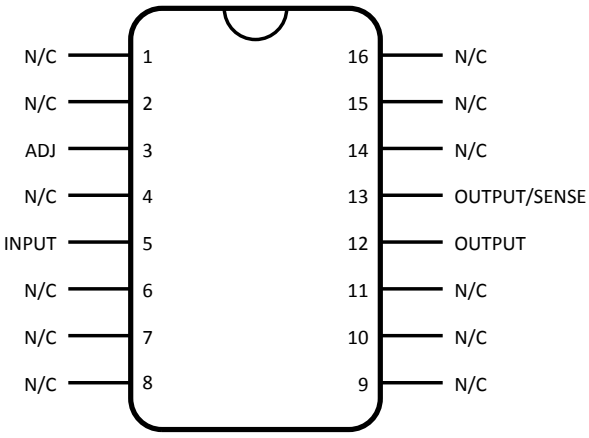
(1) The 製品情報 table can be referenced for information on which part numbers correspond to LDR or HDR options.

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6 Pin Configurations and Functions



LM117H, LM117NDTTO-39 (NDT) 3-Pin Metal Can Package (Bottom View)



LM117GW CFP SOIC (NAC) 16-Pin Ceramic Package (Top View)

表 6-1. Pin Functions

PIN			I/O[1]	DESCRIPTION
NAME	TO-39 (NDT)	CFP SOIC (NAC)		
ADJ	2	3	–	Adjust pin.
V_{IN}	1	5	I	Input voltage pin for the regulator.
V_{OUT}	3, CASE	12	O	Output voltage pin for the regulator.
OUTPUT/SENSE	–	13	–	Used to sense the output voltage. Must be connected to VOUT for proper operation.
N/C	–	1, 2, 4, 6, 7, 8, 9, 10, 11, 14, 15, 16	–	No connection. These pins have no internal connections and may be grounded or left floating. They may also be connected to the board heatsink and used for thermal dissipation.

(1) I = input, O = output, P = power, FB = feedback, GND = ground, NC = no connect

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7 Specifications

7.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
	Power dissipation(2)	Internally Limited		
	Input-output voltage differential	–0.3	60	V
T_{stg}	Storage temperature	–65	150	°C
T_{jmax}	Maximum junction temperature		150	°C
	Lead temperature metal package		300	°C

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

(2) The maximum power dissipation must be derated at elevated temperatures and is dictated by T_{Jmax} (maximum junction temperature), θ_{JA} (package junction to ambient thermal resistance), and T_A (ambient temperature). The maximum allowable power dissipation at any temperature is $P_{Dmax} = (T_{Jmax} – T_A) / \theta_{JA}$ or the number given in the *Absolute Maximum Ratings*, whichever is lower. Although power dissipation is internally limited, these specifications are applicable for power dissipations of 2 W for the TO-39 and CFP packages, and 20 W for the TO-3 package.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1) (2)	±2000	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) Human-body model, 100 pF discharged through a 1.5-kΩ resistor.

7.3 Recommended Operating Conditions

Over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
T_A	Operating temperature	–55	125	°C
V_{IN}	Input voltage	4.25	60	V

7.4 Thermal Information

THERMAL METRIC(1)			LM117HVQML-SP		UNIT
			TO-39 (NDT)	CFP (NAC)	
			3 PINS (LM117H)	16 PINS (LM117GW)	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	Still air	186	130	°C/W
		500 LF/min air flow	64	80	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance		21	7	°C/W

(1) For more information, see the *Semiconductor and IC package thermal metrics* application report.

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7.5 Electrical Characteristics

The following conditions apply, unless otherwise specified. V_{Diff} = (V_I − V_O), I_L = 8 mA, V_O = 1.25 V (nominal), over operating temperature range (T = –55°C to 125°C).

PARAMETER		TEST CONDITIONS (1)		SUBGROUP (2)	MIN	MAX	UNIT
V_{Ref}	Reference voltage	V_{Diff} = 3 V		1	1.2	1.3	V
			25°C, Post-radiation	1		1.45	
		V_{Diff} = 3.3 V		2, 3	1.2	1.3	
		V_{Diff} = 40 V		1, 2, 3	1.2	1.3	
			25°C, Post-radiation	1		1.45	
V_{RLine}	Line regulation	3 V ≤ V_{Diff} ≤ 40 V, V_O = V_{Ref}	25°C	1	–8.64	8.64	mV
			25°C, Post-radiation	1	–40	40	
		3.3 V ≤ V_{Diff} ≤ 40 V, V_O = V_{Ref}	125°C, –55°C	2, 3	–18	18	
		40 V ≤ V_{Diff} ≤ 60 V, I_L = 60 mA	25°C	1	–25	25	
V_{RLoad}	Load regulation	V_{Diff} = 3 V, 10 mA ≤ I_L ≤ 500 mA	25°C	1	–15	15	mV
			25°C, Post-radiation	1	–27	27	
		V_{Diff} = 3.3 V, 10 mA ≤ I_L ≤ 500 mA	125°C, –55°C	2, 3	–15	15	
		V_{Diff} = 40 V, 10 mA ≤ I_L ≤ 150 mA	25°C	1	–15	15	
		V_{Diff} = 40 V, 10 mA ≤ I_L ≤ 100 mA	125°C, –55°C	2, 3	–15	15	
V_{RTh}	Thermal regulation	V_{Diff} = 40 V, I_L = 150 mA, t = 20 ms	25°C	1		6	mV
I_{Adj}	Adjust pin current	V_{Diff} = 3 V	25°C	1		100	µA
		V_{Diff} = 3.3 V	125°C, –55°C	2, 3		100	
		V_{Diff} = 40 V		1, 2, 3		100	
ΔI_{Adj}/ Line	Adjust pin current change	3 V ≤ V_{Diff} ≤ 40 V	25°C	1	–5	5	µA
		3.3 V ≤ V_{Diff} ≤ 40 V	125°C, –55°C	2, 3	–5	5	
ΔI_{Adj} / Load	Adjust pin current change	V_{Diff} = 3 V, 10 mA ≤ I_L ≤ 500 mA	25°C	1	–5	5	µA
		V_{Diff} = 3.3 V, 10 mA ≤ I_L ≤ 500 mA	125°C, –55°C	2, 3	–5	5	
		V_{Diff} = 40 V, 10 mA ≤ I_L ≤ 150 mA	25°C	1	–5	5	
		V_{Diff} = 40 V, 10 mA ≤ I_L ≤ 100 mA	125°C, –55°C	2, 3	–5	5	
I_Q	Minimum load current	V_{Diff} = 3 V V_O = 1.7 V	25°C	1		5	mA
		V_{Diff} = 3.3 V V_O = 1.7 V	125°C, –55°C	2, 3		5	
		V_{Diff} = 40 V V_O = 1.7 V		1, 2, 3		5	
		V_{Diff} = 60 V V_O = 1.7 V	25°C	1		8.2	

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PARAMETER		TEST CONDITIONS (1)		SUBGROUP (2)	MIN	MAX	UNIT
I_{OS}	Output short circuit current	V_I = 4.25 V	25°C	1	0.5	1.8	A
		V_I = 60 V	25°C	1	0	0.4	
$\Delta V_I / \Delta V_O$	Ripple rejection	V_I = 6.25 V, I_L = 125 mA, e_I = 1 V_{RMS}, f = 120 Hz	25°C	4	66		dB
			25°C Post-radiation	4	55		

(1) Pre- and post-irradiation limits are identical for the parameters above unless specified by the test conditions.
(2) For subgroup definitions, see Quality Conformance Inspection table.

7.6 Parameter Drift

The following deltas are for Group C (Life Test). Data is measured at 25°C.

PARAMETER		TEST CONDITIONS	SUBGROUP (1)	MIN	MAX	UNIT
V_{Ref}	Reference voltage	V_{Diff} = 3 V	1	–0.01	0.01	V
		V_{Diff} = 40 V	1	–0.01	0.01	V
V_{RLine}	Line regulation	3 V ≤ V_{Diff} ≤ 40 V, V_O = V_{Ref}	1	–4	4	mV
		40 V ≤ V_{Diff} ≤ 60 V, I_L = 60 mA	1	–6	6	
I_{Adj}	Adjust pin current	V_{Diff} = 3 V	1	–10	10	µA
		V_{Diff} = 40 V	1	–10	10	µA

(1) For subgroup definitions, see Qualirt Conformance Inspection table.

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7.7 Quality Conformance Inspection

MIL-STD-883, Method 5005 - Group A

SUBGROUP	DESCRIPTION	TEMP (°C)
1	Static tests at	25
2	Static tests at	125
3	Static tests at	–55
4	Dynamic tests at	25
5	Dynamic tests at	125
6	Dynamic tests at	–55
7	Functional tests at	25
8A	Functional tests at	125
8B	Functional tests at	–55
9	Switching tests at	25
10	Switching tests at	125
11	Switching tests at	–55

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7.8 Typical Characteristics

Output capacitor = 0 µF unless otherwise noted

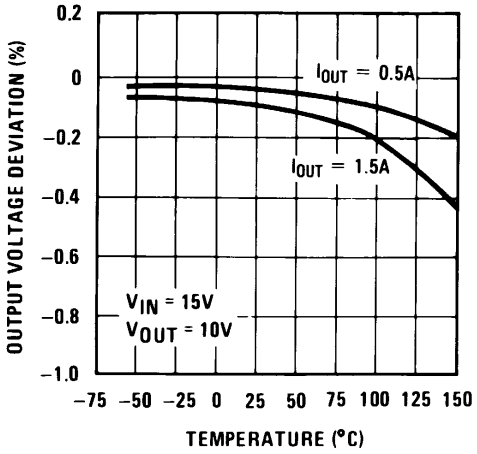


図 7-1. Load Regulation

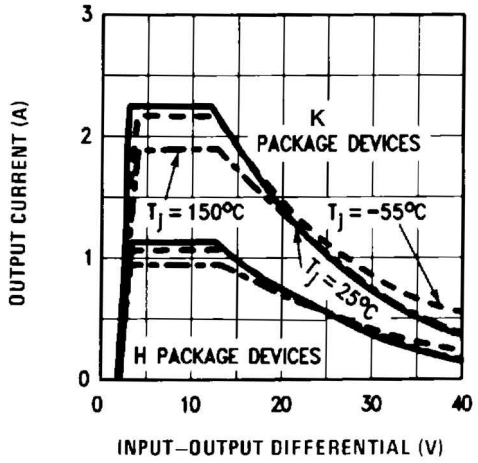


図 7-2. Current Limit

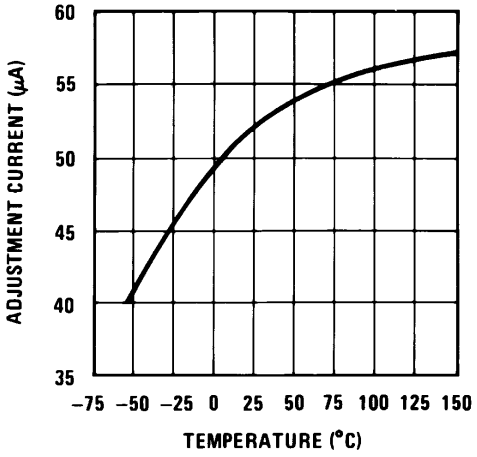


図 7-3. Adjustment Current

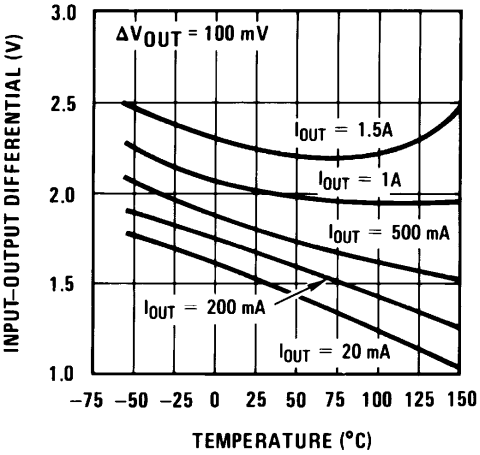


図 7-4. Dropout Voltage

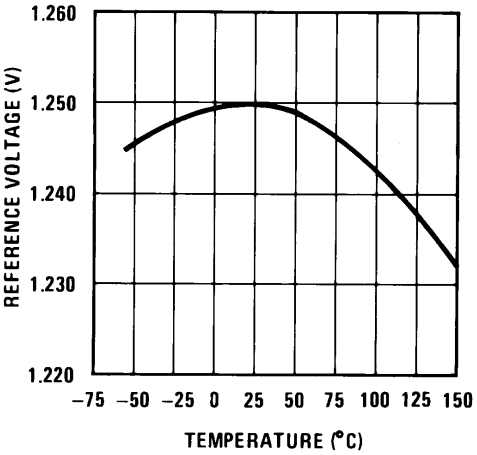


図 7-5. Temperature Stability

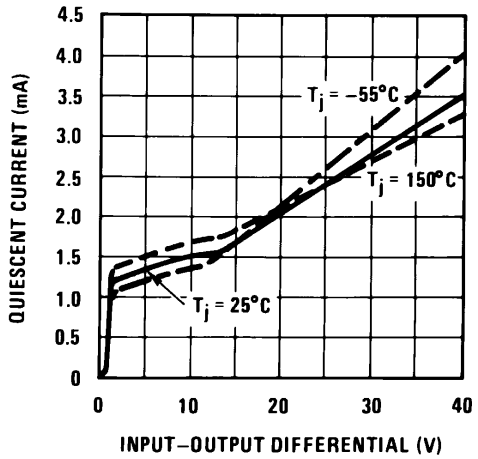


図 7-6. Minimum Operating Current

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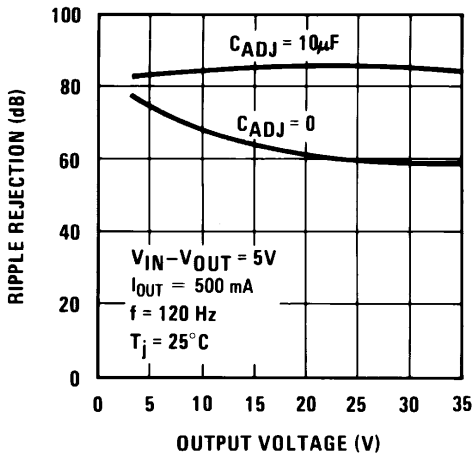


図 7-7. Ripple Rejection

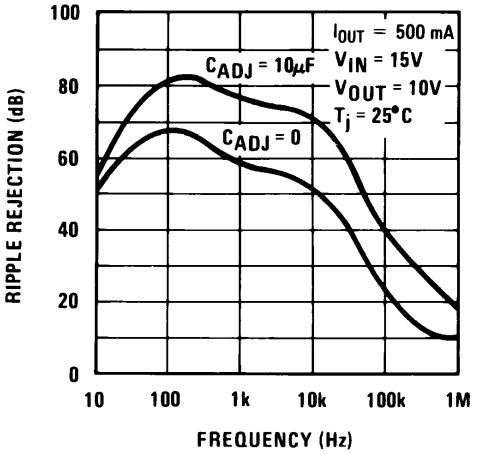


図 7-8. Ripple Rejection

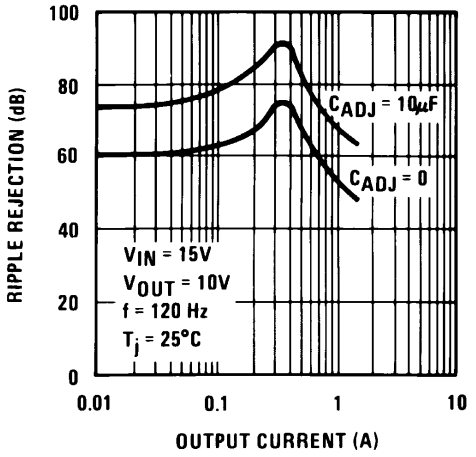


図 7-9. Ripple Rejection

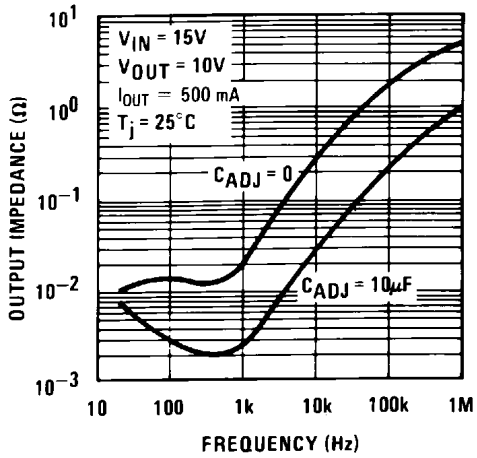


図 7-10. Output Impedance

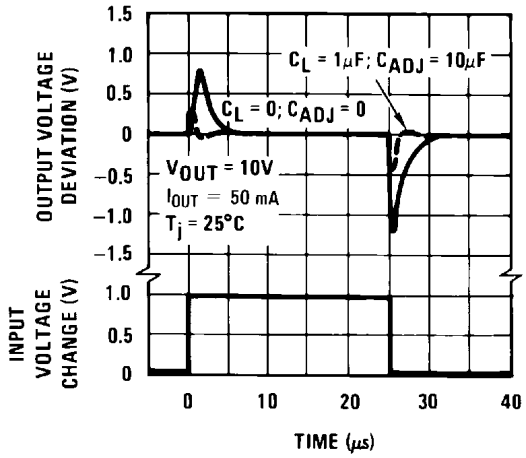


図 7-11. Line Transient Response

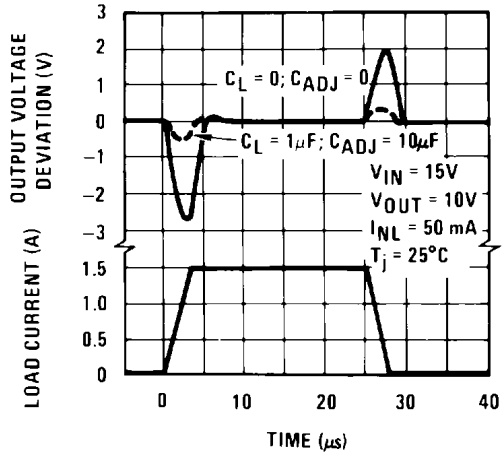


図 7-12. Load Transient Response

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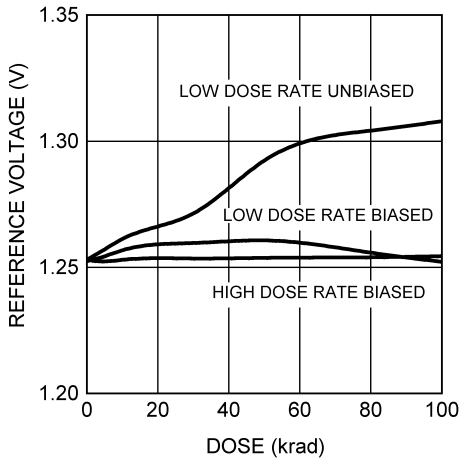


図 7-13. Reference Voltage

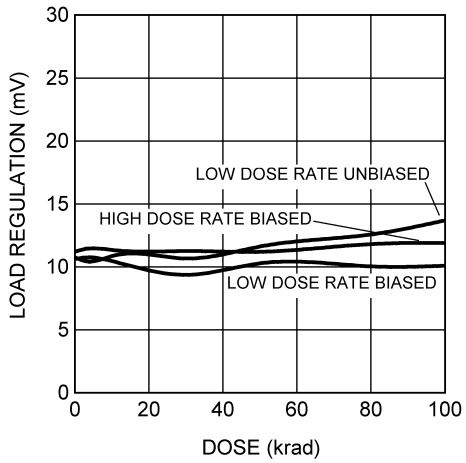


図 7-14. Load Regulation

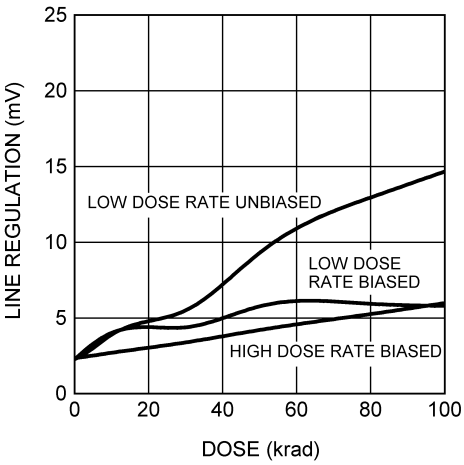


図 7-15. Line Regulation

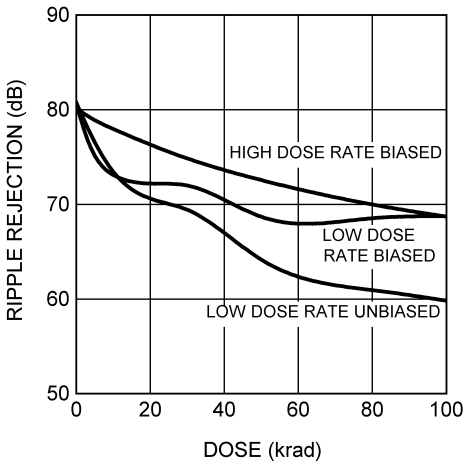


図 7-16. Ripple Rejection

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8 Detailed Description

8.1 Overview

The LM117HVQML-SP 3-terminal positive voltage linear regulator is capable of supplying 0.5 A over a 1.2-V to 57-V output range. It is simple to use and requires only two external resistors to set the output voltage. Further, both line and load regulation are better than standard fixed regulators.

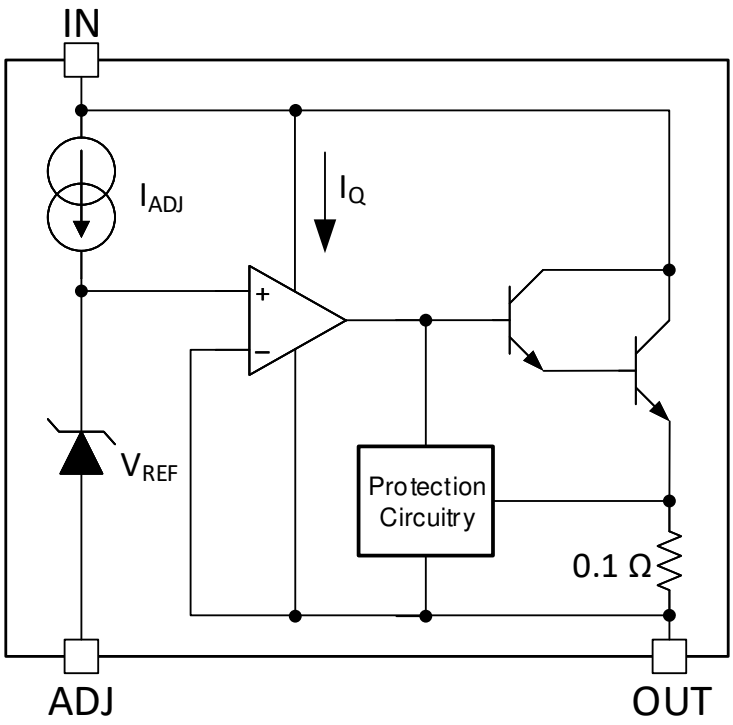
The regulator is "floating" and sees only the input-to-output differential voltage, thus enabling supplies of several hundred volts to be regulated as long as the maximum input-to-output differential is not exceeded (i.e. don't short circuit the output).

The LM117HVQML-SP offers full overload protection such as current limit, thermal overload protection, and safe area protection. All overload protection circuitry remains fully functional even if the adjustment terminal is disconnected.

Typically, no capacitors are needed unless the device is situated more than 6 in from the input filter capacitors in which case an input bypass is needed. An optional output capacitor can be added to improve transient response. The adjustment terminal can be bypassed to achieve very high ripple rejection ratios which are difficult to achieve with standard 3-terminal regulators.

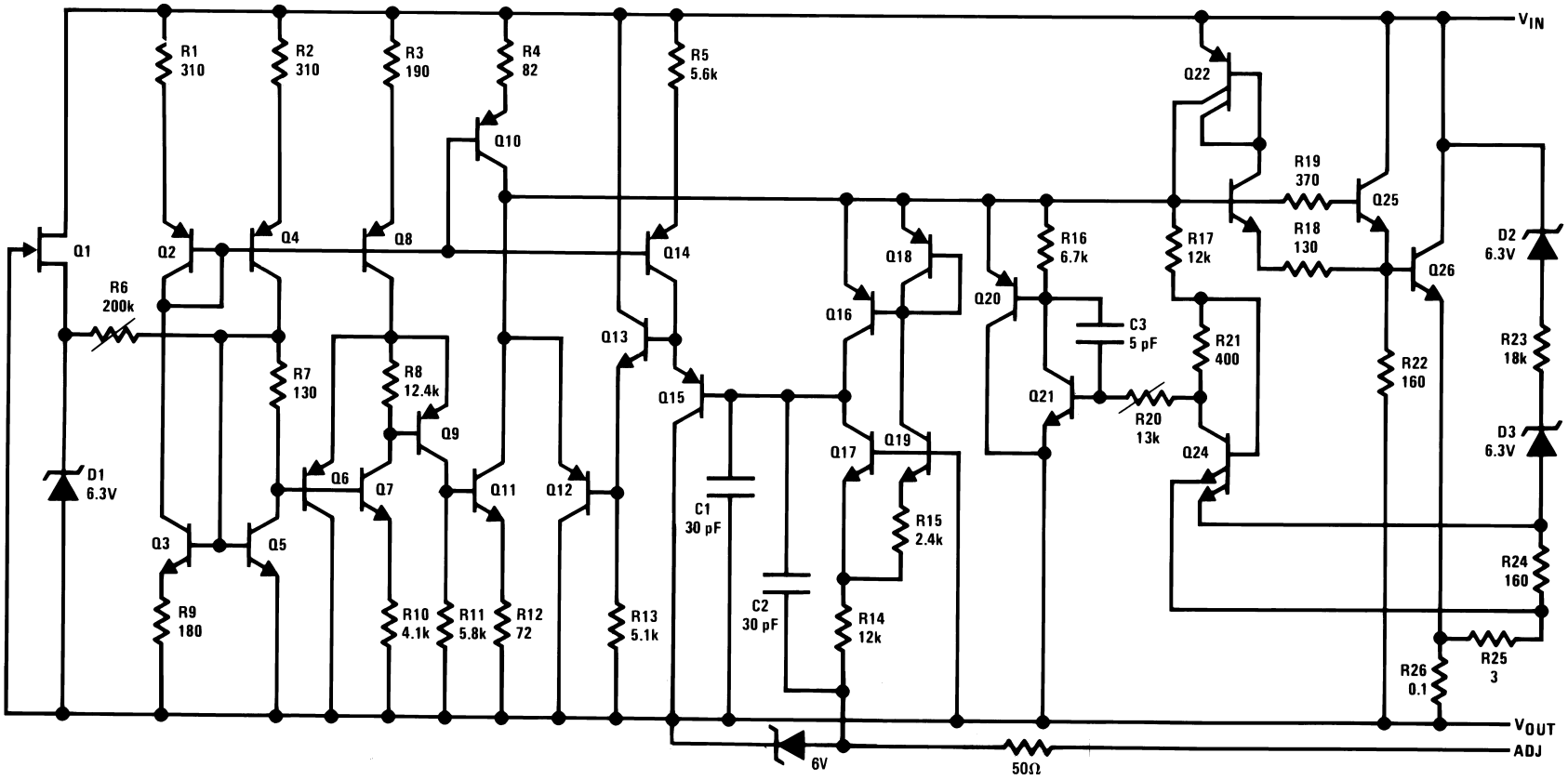
This device makes an especially simple adjustable switching regulator, a programmable output regulator, or by connecting a fixed resistor between the adjustment pin and output it can be used as a precision current regulator. Supplies with electronic shutdown can be achieved by clamping the adjustment terminal to ground which programs the output to 1.2 V where most loads draw little current.

8.2 Functional Block Diagram



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8.2.1 Simplified Device Schematic

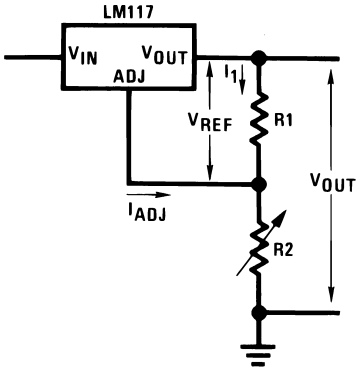


8.3 Feature Description

8.3.1 Setting Output Voltage

In operation, the LM117HVQML-SP develops a nominal 1.25-V reference voltage, V_{REF}, between the output and adjustment terminal. The reference voltage is expressed across R1 and, since the voltage is constant, a constant current I_1 then flows through R2, giving an output voltage of:

$$V_{OUT} = V_{REF}\left(1 + \frac{R2}{R1}\right) + I_{ADJ}R2 \quad (1)$$



Since the 100-µA current from the adjustment terminal represents an error term, the LM117HVQML-SP was designed to minimize I_{ADJ} and make it very constant with line and load changes. To do this, all quiescent operating current is returned to the output establishing a minimum load current requirement. If there is insufficient load on the output, the output will rise.

To mitigate the requirement for an added load to sink the required output current, the resistor divider may be selected so that it alone can sink the largest specified output load current of 5 mA (nominal). This has the additional benefit of minimizing the I_{ADJ} error term (which varies over temperature).

8.3.2 Load Regulation

The LM117HVQML-SP is capable of providing extremely good load regulation but a few precautions are needed to obtain maximum performance. The current set resistor connected between the adjustment terminal and the output terminal (usually 240 Ω) should be tied directly to the output (case) of the regulator rather than near the load. This eliminates line drops from appearing effectively in series with the reference and degrading regulation. For example, a 15-V regulator with 0.05-Ω resistance between the regulator and load will have a load regulation due to line resistance of 0.05 Ω × I_L. If the set resistor is connected near the load the effective line resistance will be 0.05 Ω (1 + R2 / R1) or in this case, 11.5 times worse.

図 8-1 shows the effect of resistance between the regulator and 240-Ω set resistor.

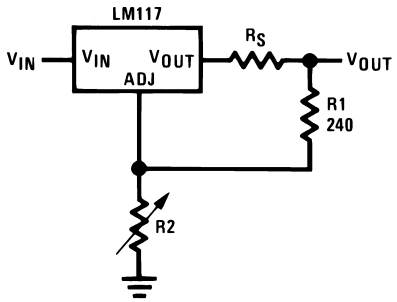


図 8-1. Regulator With Line Resistance in Output Lead

With the TO-39 package, care should be taken to minimize the wire length of the output lead. The ground of R2 can be returned near the ground of the load to provide remote ground sensing and improve load regulation.

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8.3.3 External Capacitors

An input bypass capacitor is recommended. A 0.1-µF disc or 1-µF solid tantalum on the input is suitable input bypassing for almost all applications. The device is more sensitive to the absence of input bypassing when adjustment or output capacitors are used but the above values will eliminate the possibility of problems.

The adjustment terminal can be bypassed to ground on the LM117HVQML-SP to improve ripple rejection. This bypass capacitor prevents ripple from being amplified as the output voltage is increased. With a 10-µF bypass capacitor 80-dB ripple rejection is obtainable at any output level. Increases over 10-µF do not appreciably improve the ripple rejection at frequencies above 120 Hz. If the bypass capacitor is used, it is sometimes necessary to include protection diodes to prevent the capacitor from discharging through internal low current paths and damaging the device (see セクション 8.3.4).

In general, the best type of capacitors to use are solid tantalum. Solid tantalum capacitors have low impedance even at high frequencies. Depending upon capacitor construction, it takes about 25-µF in aluminum electrolytic to equal 1-µF solid tantalum at high frequencies. Ceramic capacitors are also good at high frequencies; but some types have a large decrease in capacitance at frequencies around 0.5 MHz. For this reason, 0.01-µF disc may seem to work better than a 0.1-µF disc as a bypass.

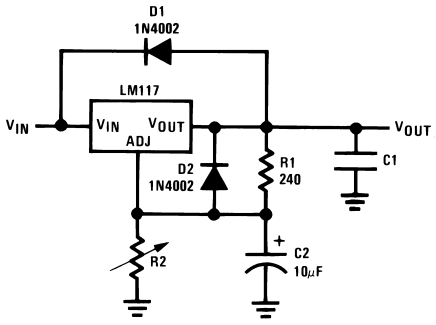
Although the LM117HVQML-SP is stable with no output capacitors, like any feedback circuit, certain values of external capacitance can cause excessive ringing. This occurs with values between 500 pF and 5000 pF. A 1-µF solid tantalum (or 25-µF aluminum electrolytic) on the output swamps this effect and insures stability. Any increase of the load capacitance larger than 10 µF will merely improve the loop stability and output impedance.

8.3.4 Protection Diodes

When external capacitors are used with an IC regulator it is sometimes necessary to add protection diodes to prevent the capacitors from discharging through low current points into the regulator. Most 10-µF capacitors have low enough internal series resistance to deliver 20-A spikes when shorted. Although the surge is short, there is enough energy to damage parts of the IC.

When an output capacitor is connected to a regulator and the input is shorted, the output capacitor will discharge into the output of the regulator. The discharge current depends on the value of the capacitor, the output voltage of the regulator, and the rate of decrease of V_{IN}. In the LM117HVQML-SP, this discharge path is through a large junction that is able to sustain 15-A surge. This is not true of other types of positive regulators. For output capacitors of 25 µF or less, there is no need to use diodes.

The bypass capacitor on the adjustment terminal can discharge through a low current junction. Discharge occurs when *either* the input or output is shorted. Internal to the LM117HVQML-SP is a 50-Ω resistor which limits the peak discharge current. No protection is needed for output voltages of 25 V or less and 10-µF capacitance. 図 8-2 shows an LM117HVQML-SP with protection diodes included for use with outputs greater than 25 V and high values of output capacitance.



D1 protects against C1 (such as due to a VIN short),
D2 protects against C2 (Such as due to a VOUT short).

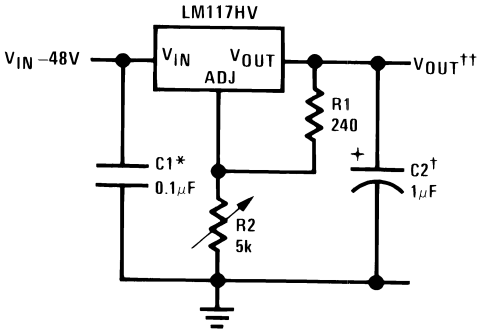
図 8-2. Regulator With Protection Diodes

9 Application and Implementation

Note

以下のアプリケーション情報は、TI の製品仕様に含まれるものではなく、TI ではその正確性または完全性を保証いたしません。個々の目的に対する製品の適合性については、お客様の責任で判断していただくことになります。お客様は自身の設計実装を検証しテストすることで、システムの機能を確認する必要があります。

9.1 Typical Applications



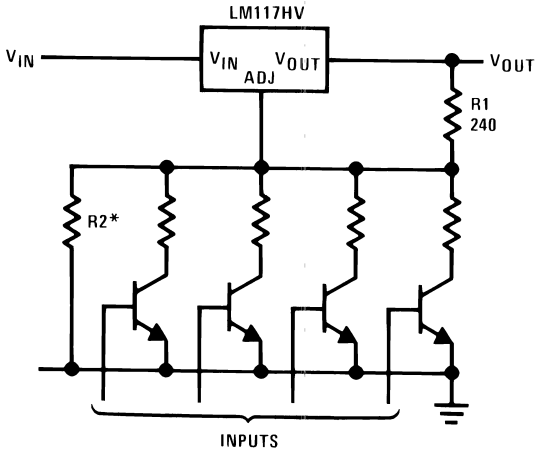
Full output current not available at high input-output voltages

†Optional—improves transient response. Output capacitors in the range of 1 µF to 1000 µF of aluminum or tantalum electrolytic are commonly used to provide improved output impedance and rejection of transients.

*Needed if device is more than 6 in from filter capacitors.

$$\dagger\dagger V_{OUT} = 1.25V \left(1 + \frac{R2}{R1}\right) + I_{ADJ} R_2$$

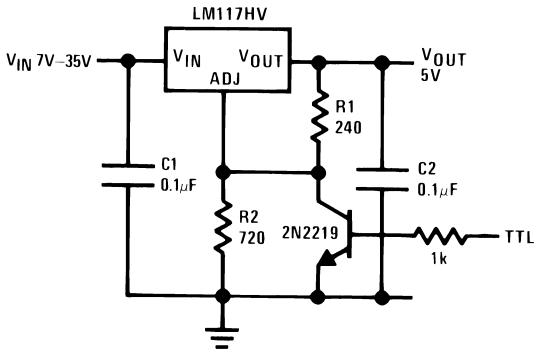
図 9-1. 1.2-V–45-V Adjustable Regulator



*Sets maximum V_{OUT}

図 9-2. Digitally Selected Outputs

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*Min. output ≈ 1.2 V

図 9-3. 5-V Logic Regulator With Electronic Shutdown*

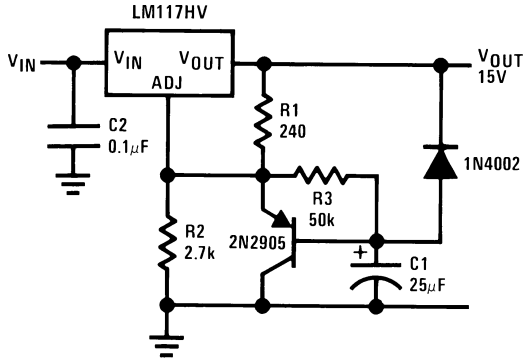
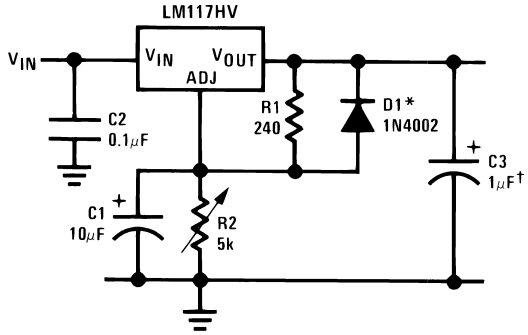


図 9-4. Slow Turn-On 15-V Regulator



†Solid tantalum

*Discharges C1 if output is shorted to ground

図 9-5. Adjustable Regulator With Improved Ripple Rejection

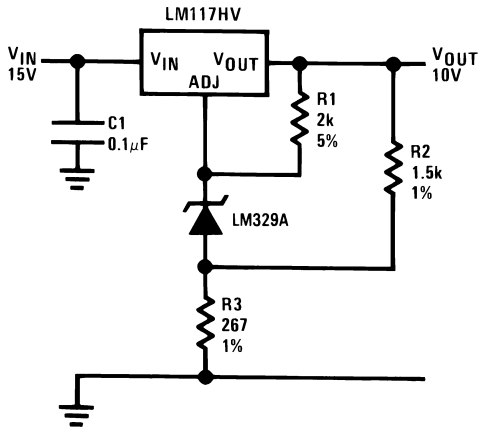
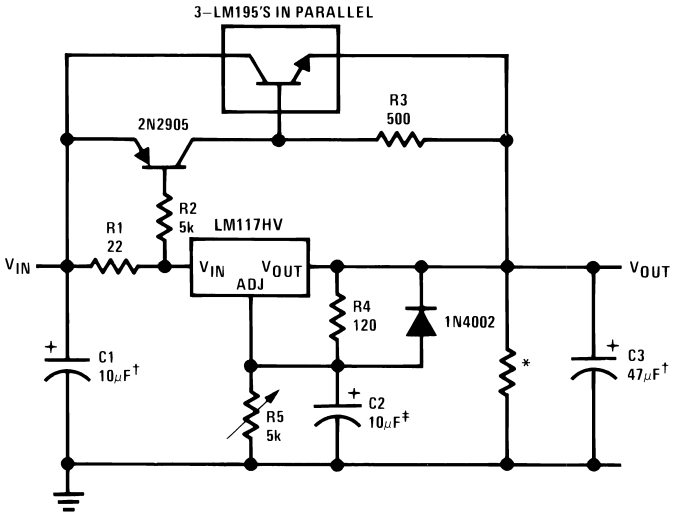


図 9-6. High Stability 10-V Regulator



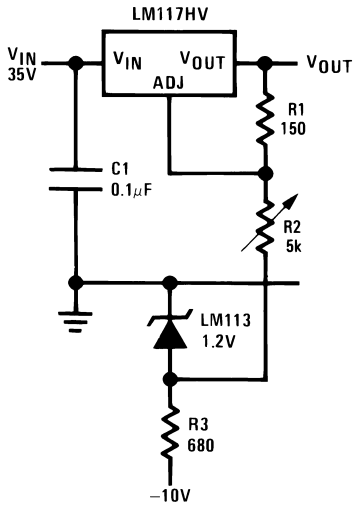
†Solid tantalum

*Minimum load current = 30 mA

‡Optional—improves ripple rejection

図 9-7. High Current Adjustable Regulator

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Full output current not available at high input-output voltages

図 9-8. 0-V to 30-V Regulator

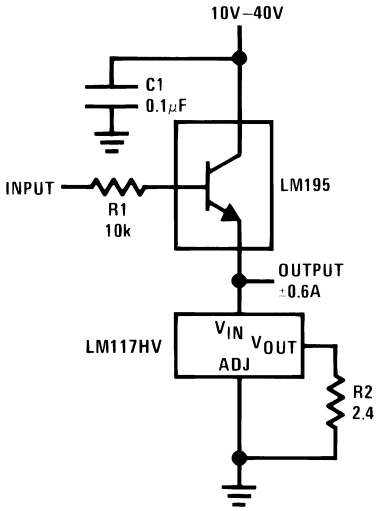
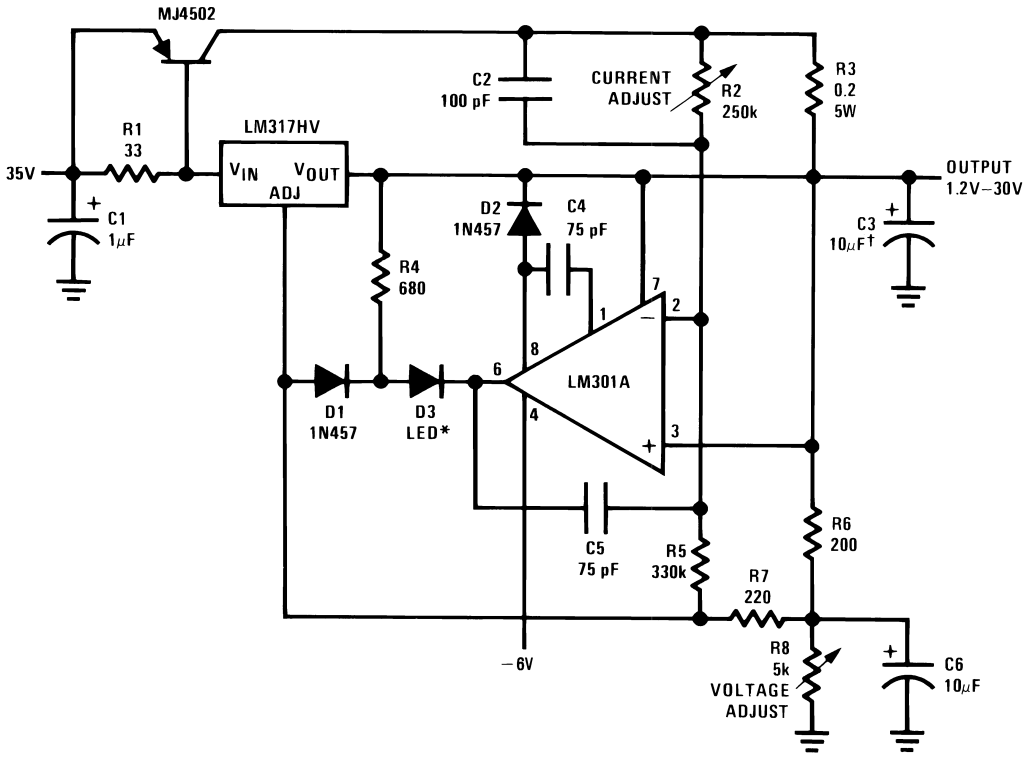


図 9-9. Power Follower



†Solid tantalum

*Lights in constant current mode

図 9-10. 5-A Constant Voltage/Constant Current Regulator

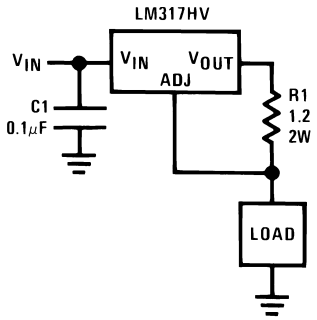
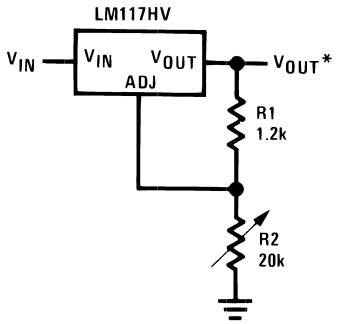


図 9-11. 1-A Current Regulator



*Minimum load current ≈ 5 mA

図 9-12. 1.2-V–20-V Regulator With Minimum Program Current

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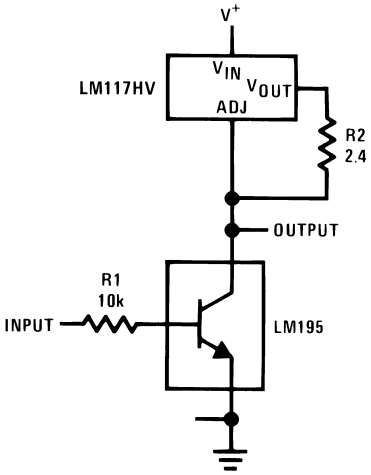
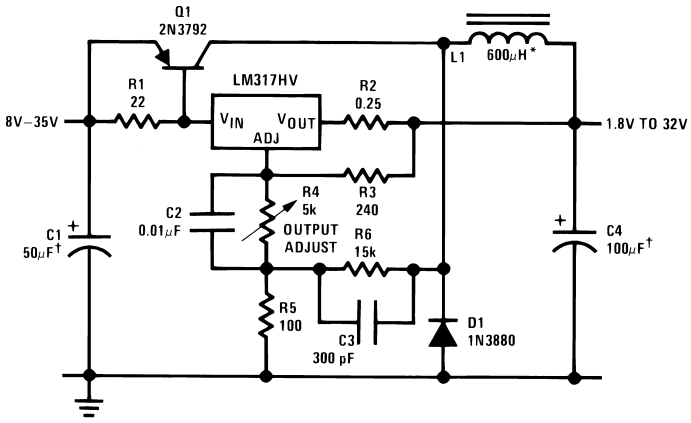


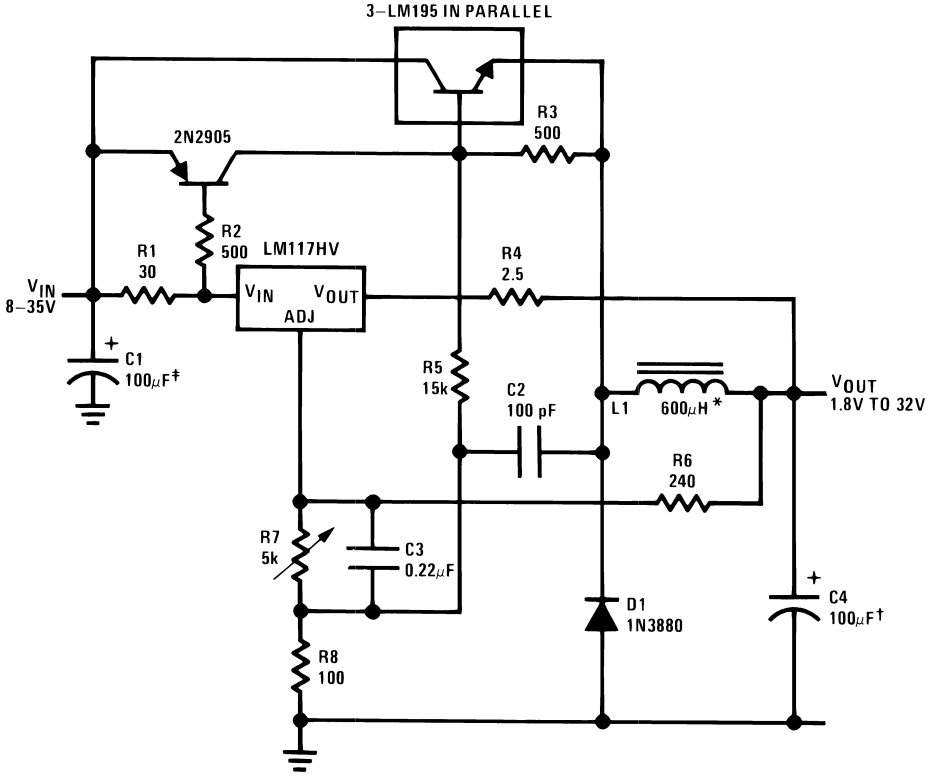
図 9-13. High Gain Amplifier



†Solid tantalum

*Core—Arnold A-254168-2 60 turns

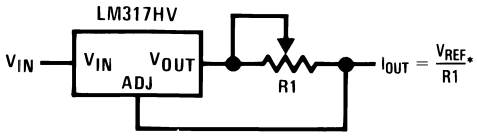
図 9-14. Low Cost 3-A Switching Regulator



†Solid tantalum

*Core—Arnold A-254168-2 60 turns

図 9-15. 4-A Switching Regulator With Overload Protection



* 0.8 Ω ≤ R1 ≤ 120 Ω

図 9-16. Precision Current Limiter

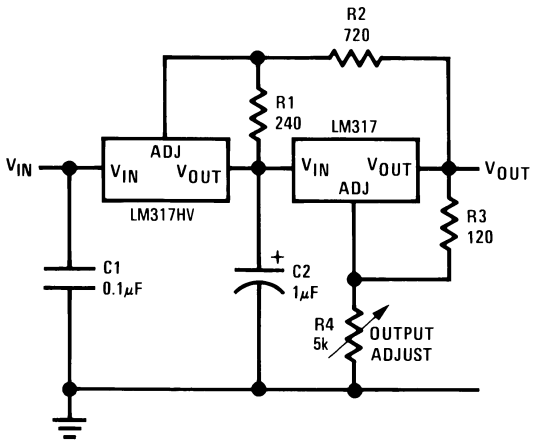
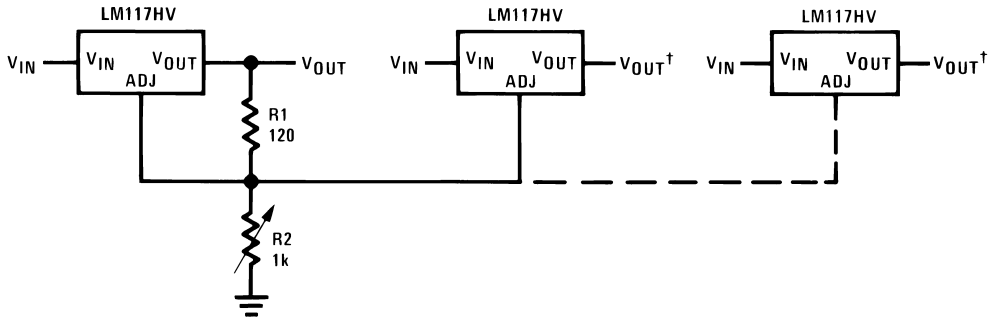


図 9-17. Tracking Preregulator

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*All outputs within ±100 mV
†Minimum load = 10 mA

図 9-18. Adjustable Multiple On-card Regulators With Single Control*

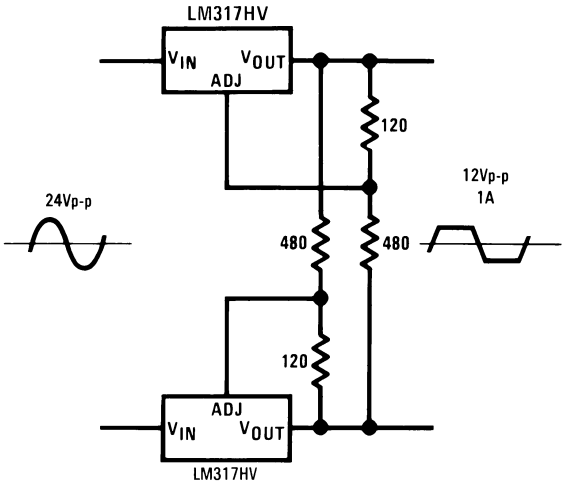
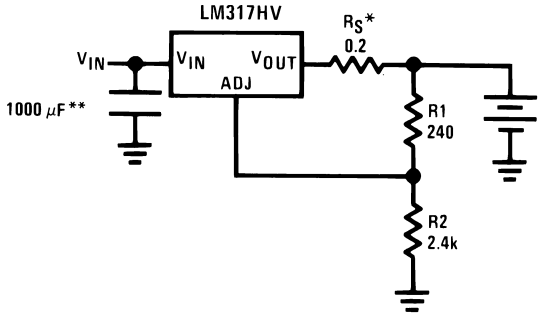


図 9-19. AC Voltage Regulator



*R_S—sets output impedance of charger $Z_{OUT} = R_S \left(1 + \frac{R2}{R1}\right)$

Use of R_S allows low charging rates with fully charged battery.
**The 1000 µF is recommended to filter out input transients

図 9-20. 12-V Battery Charger

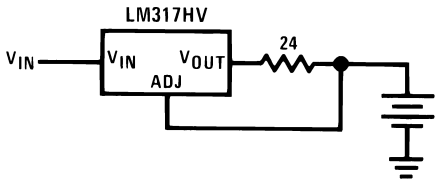


図 9-21. 50-mA Constant Current Battery Charger

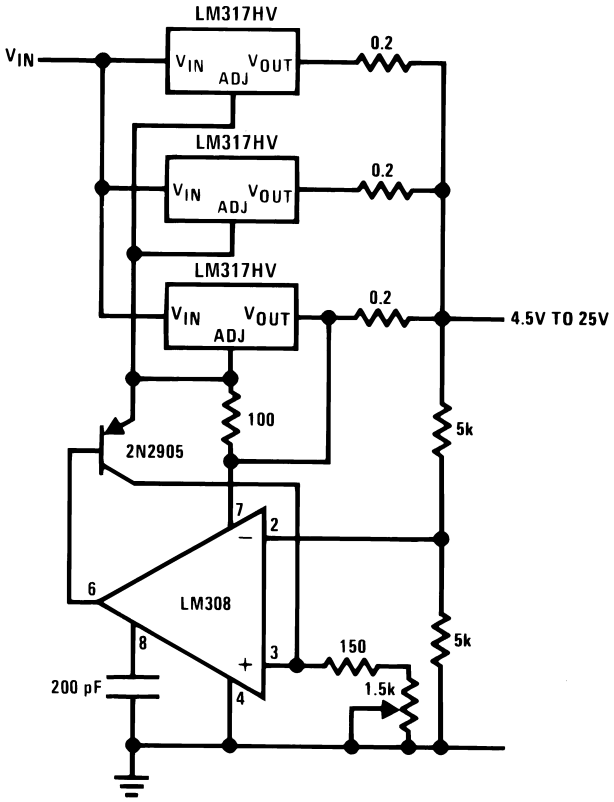
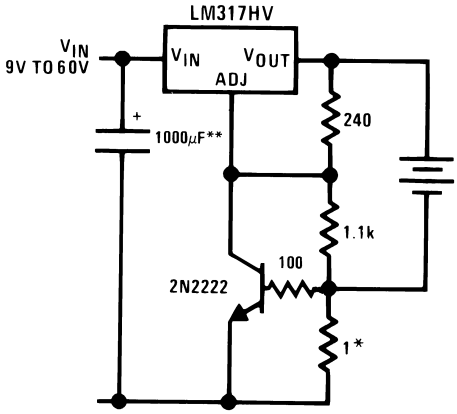


図 9-22. Adjustable 4-A Regulator



*Sets peak current (0.6 A for 1 Ω)

**The 1000 µF is recommended to filter out input transients

図 9-23. Current Limited 6-V Charger

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10 Power Supply Recommendations

The input supply to the LM117HVQML-SP must be kept at a voltage level such that its maximum input to output differential voltage is not exceeded. The minimum dropout voltage must also be met with extra headroom when possible to keep the LM117HVQML-SP in regulation. An input capacitor is recommended, especially when the input pin is located more than 6 in away from the power supply source. For more information regarding capacitor selection, refer to External Capacitors.

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11 Layout

11.1 Layout Guidelines

Ensure wide enough traces for those carrying the load current in order to reduce the amount of parasitic trace inductance. Keep the feedback loop from VOUT to ADJ as short as possible. To improve PSRR, a bypass capacitor can be placed at the ADJ pin and must be located as close as possible to the IC. In cases when VIN shorts to ground, an external diode must be placed from VOUT to VIN to divert the surge current from the output capacitor and protect the IC. Similarly, in cases when a large bypass capacitor is placed at the ADJ pin and VOUT shorts to ground, an external diode must be placed from ADJ to VOUT to provide a path for the bypass capacitor to discharge. These diodes must be placed close to the corresponding LM117HVQML-SP pins to increase their effectiveness.

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12 Device and Documentation Support

12.1 Device Support

12.1.1 Third-Party Products Disclaimer

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12.2 Documentation Support

12.2.1 Related Documentation

1. LM117HVQML-SP NDD (Neutron Displacement Damage) Characterization
2. LM117HVQML-SP SMD 5962R0722961V9A
3. Die Datasheet LM117HVKG MD8 3-Terminal Adj Regulator
4. High Reliability Part Numbering System
5. Applications for an Adjustable IC Power Regulator
6. Improving Power Supply Reliability with IC Power Regulators
7. A New Production Technique for Trimming Voltage Regulators
8. LDO basics: capacitor vs. capacitance
9. LDO Basics: Preventing reverse current

12.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.4 サポート・リソース

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12.6 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.7 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

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13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
5962R0722901V9A	Active	Production	DIESALE (Y) | 0	42 | NOT REQUIRED	Yes	Call TI	Level-1-NA-UNLIM	-55 to 125	
5962R0722901VXA	Active	Production	TO (NDT) | 3	20 | JEDEC TRAY (5+1)	-	Call TI	Call TI	-55 to 125	LM117HVHRQMLV 5962R0722901VXA Q ACO 5962R0722901VXA Q >T
5962R0722902VXA	Active	Production	TO (NDT) | 3	20 | JEDEC TRAY (5+1)	-	Call TI	Call TI	-55 to 125	LM117HVHRLQMLV 5962R0722961VXA Q ACO 5962R0722961VXA Q >T
5962R0722902VZA	Active	Production	CFP (NAC) | 16	88 | JEDEC TRAY (5+1)	No	SNPB	Level-1-NA-UNLIM	-55 to 125	LM117HVGWR QMLV Q 5962R07229 02VZA ACO 02VZA >T
5962R0722961V9A	Active	Production	DIESALE (Y) | 0	42 | NOT REQUIRED	-	Call TI	Call TI	-55 to 125	
5962R0722961VXA	Active	Production	TO (NDT) | 3	20 | JEDEC TRAY (5+1)	-	Call TI	Call TI	-55 to 125	LM117HVHRLQMLV 5962R0722961VXA Q ACO 5962R0722961VXA Q >T
5962R0722962VZA	Active	Production	CFP (NAC) | 16	88 | JEDEC TRAY (5+1)	No	SNPB	Level-1-NA-UNLIM	-55 to 125	LM117HVGWRL QMLV Q 5962R07229 62VZA ACO 62VZA >T
LM117HVGWRLQMLV	Active	Production	CFP (NAC) | 16	88 | JEDEC TRAY (5+1)	No	SNPB	Level-1-NA-UNLIM	-55 to 125	LM117HVGWRL QMLV Q 5962R07229 62VZA ACO 62VZA >T

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LM117HVGWRQMLV	Active	Production	CFP (NAC) | 16	88 | JEDEC TRAY (5+1)	No	SNPB	Level-1-NA-UNLIM	-55 to 125	LM117HVGWR QMLV Q 5962R07229 02VZA ACO 02VZA >T
LM117HVH MDE	Active	Production	DIESALE (Y) | 0	42 | NOT REQUIRED	-	Call TI	Call TI	-55 to 125	
LM117HVH MDR	Active	Production	DIESALE (Y) | 0	42 | NOT REQUIRED	Yes	Call TI	Level-1-NA-UNLIM	-55 to 125	
LM117HVHRLQMLV	Active	Production	TO (NDT) | 3	20 | JEDEC TRAY (5+1)	No	Call TI	Level-1-NA-UNLIM	-55 to 125	LM117HVHRLQMLV 5962R0722961VXA Q ACO 5962R0722961VXA Q >T
LM117HVHRQMLV	Active	Production	TO (NDT) | 3	20 | JEDEC TRAY (5+1)	No	Call TI	Level-1-NA-UNLIM	-55 to 125	LM117HVHRQMLV 5962R0722901VXA Q ACO 5962R0722901VXA Q >T
LM117HVNAC/EM	Active	Production	CFP (NAC) | 16	88 | JEDEC TRAY (5+1)	No	SNPB	Level-1-NA-UNLIM	25 to 25	LM117HVNAC/EM EVAL ONLY T

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

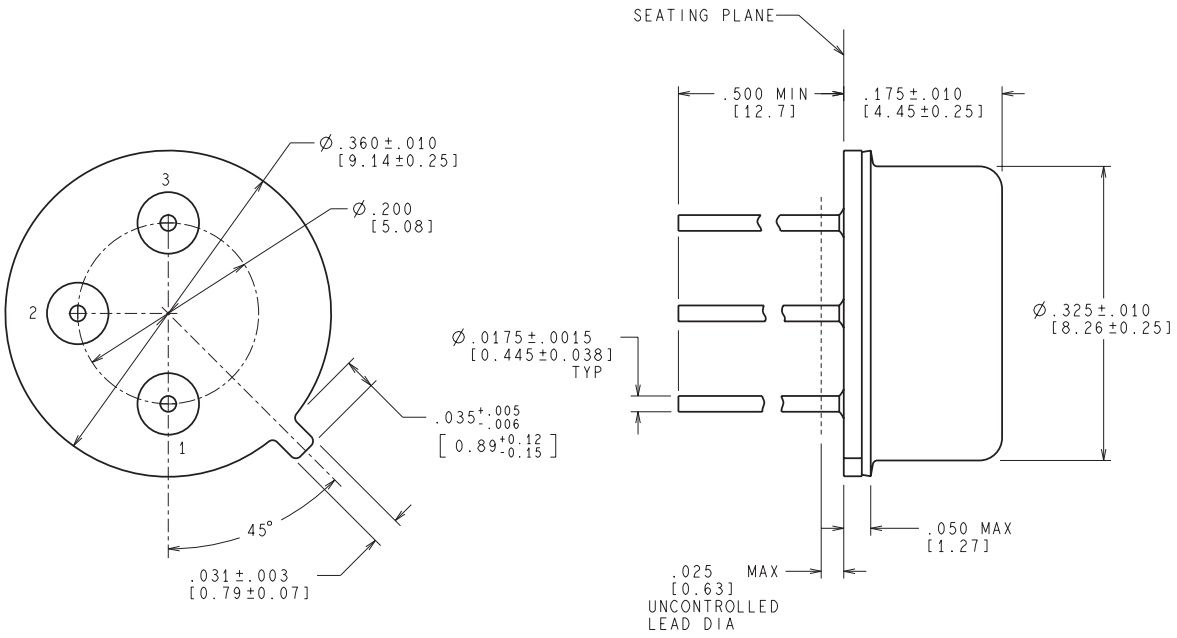
OTHER QUALIFIED VERSIONS OF LM117HVQML-SP :

- Military : LM117HVQML

NOTE: Qualified Version Definitions:

- Military - QML certified for Military and Defense Applications

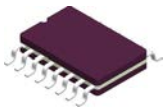
NDT0003A



CONTROLLING DIMENSION IS INCH
VALUES IN [ ] ARE MILLIMETERS

MIL-PRF-38535
CONFIGURATION CONTROL

H03A (Rev D)

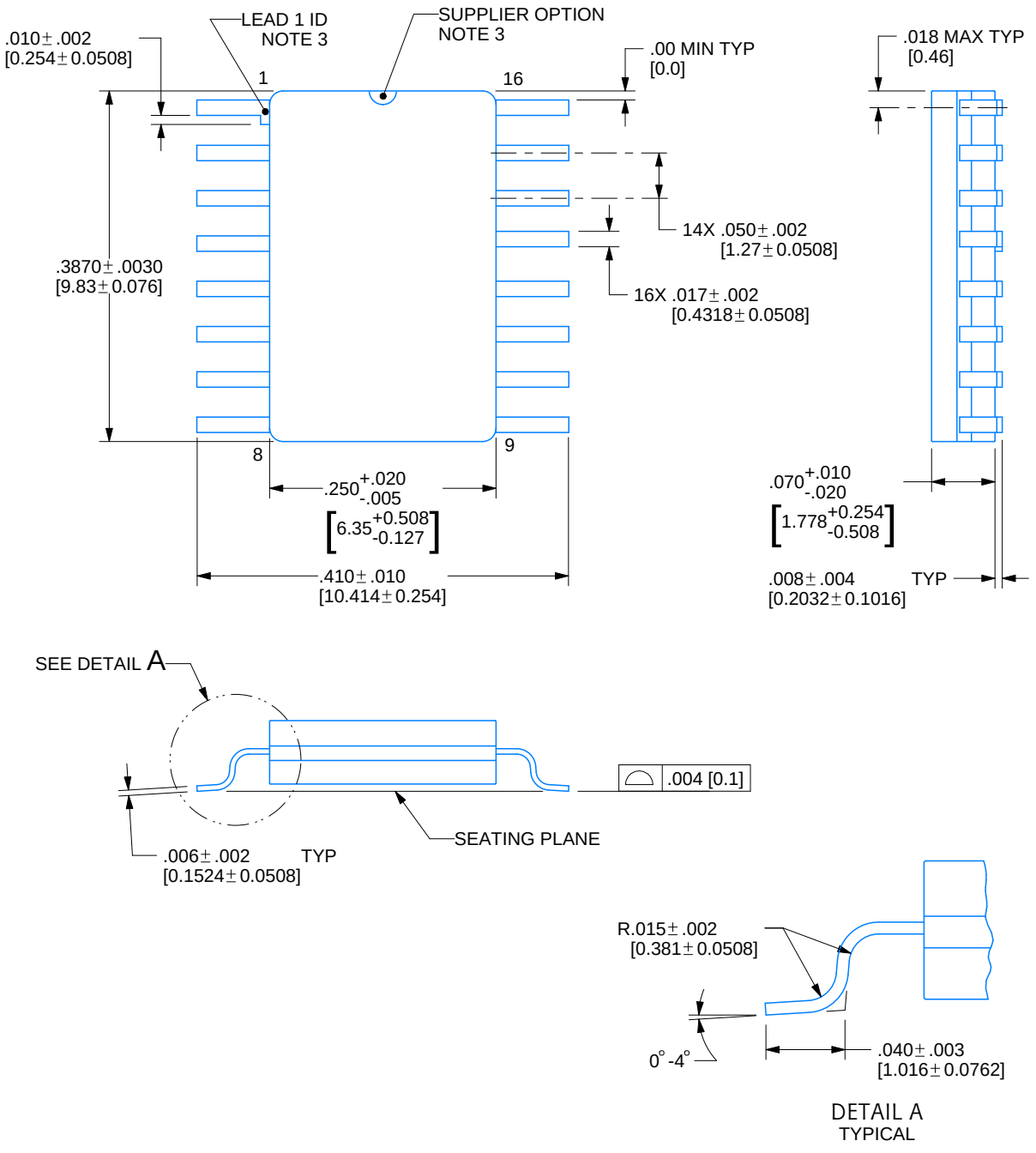


PACKAGE OUTLINE

NAC0016A

CFP - 2.33mm max height

CERAMIC FLATPACK



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NOTES:

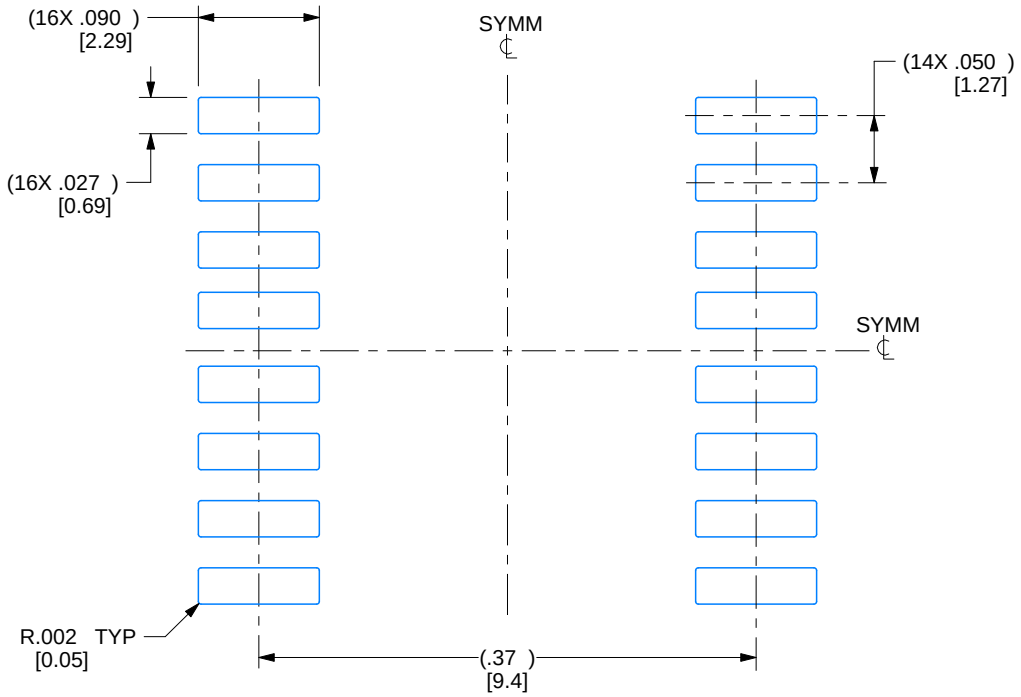
1. Controlling dimension is Inch. Values in [ ] are milimeters. Dimensions in ( ) for reference only.
2. For solder thickness and composition, see the "Lead Finish Composition/Thickness" link in the packaging section of the Texas Instruments website
3. Lead 1 identification shall be:
   a) A notch or other mark within this area
   b) A tab on lead 1, either side
4. No JEDEC registration as of December 2021

EXAMPLE BOARD LAYOUT

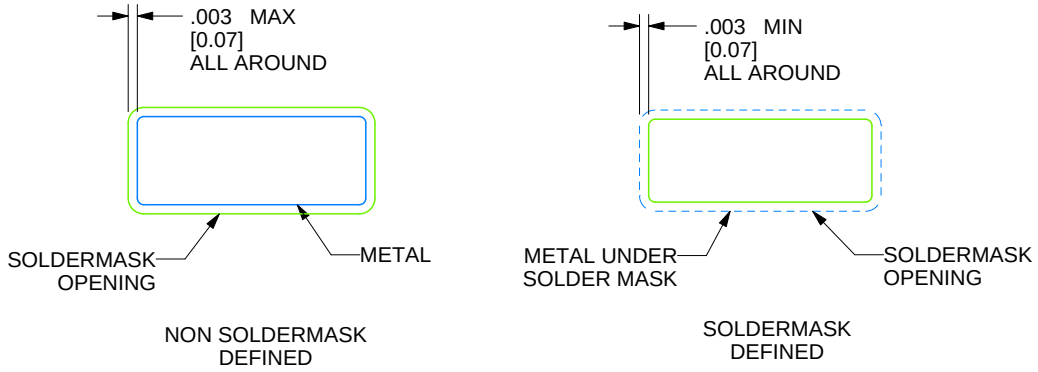
NAC0016A

CFP - 2.33mm max height

CERAMIC FLATPACK



RECOMMENDED LAND PATTERN



4215198/C 08/2022

REVISIONS

REV	DESCRIPTION	E.C.N.	DATE	BY/APP'D
A	RELEASE TO DOCUMENT CONTROL	2197879	12/30/2021	TINA TRAN / ANIS FAUZI
B	NO CHANGE TO DRAWING; REVISION FOR YODA RELEASE;	2198832	02/15/2022	K. SINCERBOX
C	.387± .003 WAS .39000± .00012;	2200917	08/08/2022	D. CHIN / K. SINCERBOX

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最終更新日：2025 年 10 月