LM339B、LM2901B、LM339、LM239、LM139、LM2901 クワッド差動コンパレータ

1 特長

- 新しい LM339B および LM2901B
- B バージョンの仕様を改善
  - 最大定格:最大 38V
  - ESD 定格 (HBM):2kV
  - 低入力オフセット:0.37mV
  - 低い入力バイアス電流:3.5nA
  - 低消費電流:200µA (コンパレータあたり)
  - 1µsec の短い応答時間
  - 拡張温度範囲 (LM339B)
- B バージョンは、LM239、LM339、LM2901 の A および V バージョンをそのまま置き換えることが可能
- 同相入力電圧範囲にグランドを含む
- 差動入力電圧範囲が最大定格電源電圧と同じ:±38V
- 低い出力飽和電圧
- TTL、MOS、CMOS 互換出力
- シングル バージョンについては、TL331B を参照してください
- デュアル バージョンについては、LM393B または LM2903B を参照してください

2 アプリケーション

- ロボット掃除機
- 単相 UPS
- サーバー PSU
- コードレス電動工具
- ワイヤレス インフラ
- 電化製品
- ビル オートメーション
- ファクトリ オートメーション / 制御
- モーター ドライブ
- インフォテインメントおよびクラスタ

3 概要

LM339B および LM2901B デバイスは、業界標準の LM339 および LM2901 コンパレータ ファミリの次世代バージョンです。これらの次世代 B バージョン コンパレータは、小さいオフセット電圧、高い電源電圧への対応、小さい消費電流、小さい入力バイアス電流、短い伝搬遅延、および専用の ESD クランプによる優れた 2kV の ESD 性能と入力の耐久性が特長です。LM339B および LM2901B は、LM239、LM339 および LM2901 (「A」および「V」グレード) をそのまま置き換えることができます。

すべてのデバイスは、広い電圧範囲にわたって単一電源で動作するように設計された 4 つの独立した電圧コンパレータで構成されています。静止電流は、電源電圧にかかわらず一定です。

製品情報

部品番号	パッケージ (1)	本体サイズ (公称)
LM139x、LM239x、LM339x、LM2901x、LM339B、LM2901B	SOIC (14)	8.70mm × 3.90mm
LM239、LM339x、LM2901	PDIP (14)	19.30mm × 6.40mm
LM239、LM2901、LM339B、LM2901B	TSSOP (14)	5.00mm × 4.40mm
LM339x、LM2901	SOP (14)	10.20mm × 5.30mm
LM339x、LM2901	SSOP (14)	6.50mm × 5.30mm
LM2901B	SOT-23 (14)	4.20mm × 2.00mm
LM339B、LM2901B	WQFN (16)	3.00mm × 3.00 mm

(1) 利用可能なすべてのパッケージについては、データシートの末尾にある注文情報を参照してください。

ファミリ比較表

仕様	LM339B	LM2901B	LM339 LM339A	LM2901 LM2901A	LM2901V LM2901AV	LM139 LM139A	LM239 LM239A	単位
電源電圧	2～36	2～36	2～30	2～30	2～32	2～30	2～30	V
総電源電流 (5V～36V、最大値)	0.8～1	0.8～1	1～2.5	1～2.5	1～2.5	1～2.5	1～2.5	mA
温度範囲	-40～85	-40～125	0～70	-40～125	-40～125	-55～125	-25～85	℃
静電気放電 (HBM)	2000	2000	2000	2000	2000	2000	2000	V
オフセット電圧 (全温度範囲での最大値)	±5.5	±5.5	±9 ±4	±15 ±4	±15 ±4	±9 ±4	±9 ±4	mV
入力バイアス電流 (標準値 / 最大値)	3.5 / 25	3.5 / 25	25 / 250	25 / 250	25 / 250	25 / 100	25 / 250	nA
応答時間 (標準値)	1	1	1.3	1.3	1.3	1.3	1.3	µsec

このリソースの元の言語は英語です。翻訳は概要を便宜的に提供するもので、自動化ツール (機械翻訳) を使用していることがあり、TI では翻訳の正確性および妥当性につきましては一切保証いたしません。実際の設計などの前には、ti.com で必ず最新の英語版をご参照くださいますようお願いいたします。

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4 Other Versions

OTHER QUALIFIED VERSIONS OF LM139-SP, LM239A, LM2901, LM2901AV, LM2901V:

- Automotive Q100: LM239A-Q1, LM2901B-Q1, LM2901-Q1, LM2901AV-Q1, LM2901V-Q1
- Enhanced Product: LM239A-EP
- Space: LM139-SP

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5 Pin Configuration and Functions

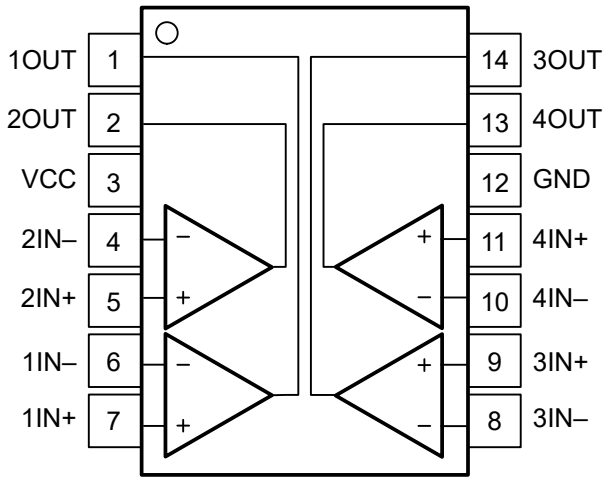
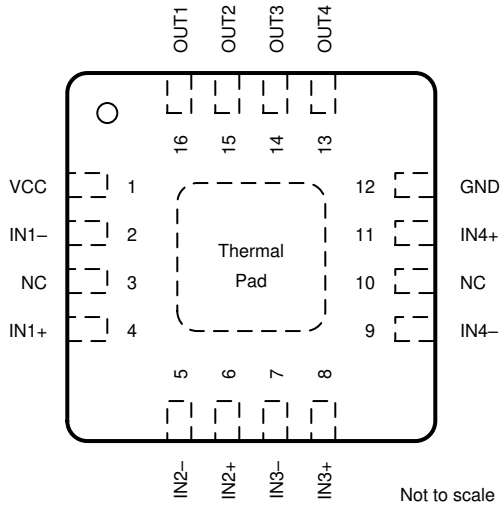


図 5-1. D, DB, N, NS, PW Packages
14-Pin SOIC, SSOP, PDIP, SOP, TSSOP
Top View



NOTE: Connect exposed thermal pad directly to GND pin.

図 5-2. RTE Package
16-Pad WQFN With Exposed Thermal Pad
Top View

表 5-1. Pin Functions

PIN			I/O	DESCRIPTION
NAME[1]	D, DB, N, NS, PW, DYY, J	WQFN		
OUT1 [1]	1	16	Output	Output pin of the comparator 2
OUT2 [1]	2	15	Output	Output pin of the comparator 1
V_{CC}	3	1	—	Positive supply
IN2– [1]	4	5	Input	Negative input pin of the comparator 1
IN2+ [1]	5	6	Input	Positive input pin of the comparator 1
IN1– [1]	6	2	Input	Negative input pin of the comparator 2
IN1+ [1]	7	4	Input	Positive input pin of the comparator 2
IN3–	8	7	Input	Negative input pin of the comparator 3
IN3+	9	8	Input	Positive input pin of the comparator 3
IN4–	10	9	Input	Negative input pin of the comparator 4
IN4+	11	11	Input	Positive input pin of the comparator 4
GND	12	12	—	Negative supply
OUT4	13	13	Output	Output pin of the comparator 4
OUT3	14	14	Output	Output pin of the comparator 3
NC	—	3	—	No Internal Connection - Leave floating or GND
NC	—	10	—	No Internal Connection - Leave floating or GND
Thermal Pad	—	PAD	—	Connect directly to GND pin

(1) Some manufacturers transpose the names of channels 1 & 2. Electrically the pinouts are identical, just a difference in the channel naming convention.

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6 Specifications

6.1 Absolute Maximum Ratings for LM339B and LM2901B

over operating free-air temperature range (unless otherwise noted)(1)

	MIN	MAX	UNIT
Supply voltage: V_S = (V+) – (V–)	-0.3	38	V
Differential input voltage : V_{ID} (2)		±38	V
Input pins (IN+, IN–)	-0.3	38	V
Current into input pins (IN+, IN–)		-50	mA
Output pin (OUT)	-0.3	38	V
Output sink current		25	mA
Output short-circuit duration(3)		Unlimited	s
Junction temperature, T_J		150	°C
Storage temperature, T_{stg}	-65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* can cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods can affect device reliability.
(2) Differential voltages are at IN+ with respect to IN-
(3) Short circuits from outputs to V+ can cause excessive heating and eventual destruction.

6.2 Absolute Maximum Ratings for Non-B Versions

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage(2)			36	V
V_{ID}	Differential input voltage(3)			±36	V
V_I	Input voltage range (either input)		–0.3	36	V
I_K	Input current(5)			–50	mA
V_O	Output voltage			36	V
I_O	Output current			20	mA
	Duration of output short circuit to ground(4)		Unlimited		
T_J	Operating virtual-junction temperature			150	°C
	Case temperature for 60s	FK package		260	°C
	Lead temperature 1.6mm (1/16in) from case for 60s	J package		300	°C
T_{stg}	Storage temperature		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* can cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods can affect device reliability.
(2) All voltage values, except differential voltages, are with respect to network ground.
(3) Differential voltages are at xIN+ with respect to xIN–.
(4) Short circuits from outputs to V_{CC} can cause excessive heating and eventual destruction.
(5) Input current flows through parasitic diode to ground and can turn on parasitic transistors that can increase I_{CC} and can cause output to be incorrect. Normal operation resumes when the input is removed.

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6.3 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Human-body model (CDM), per ANSI/ESDA/JEDEC JS-002(2)	±1000	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process

6.4 Recommended Operating Conditions for LM339B and LM2901B

over operating free-air temperature range (unless otherwise noted)

	MIN	MAX	UNIT
Supply voltage: $V_S = (V+) – (V–)$	2	36	V
Ambient temperature, T_A, LM339B	–40	85	°C
Ambient temperature, T_A, LM2901B	–40	125	°C
Input Voltage Range, V_{IVR}	(V–) – 0.1	(V+) – 2.0	V

6.5 Recommended Operating Conditions, Non-B Versions

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CC}	Supply voltage	Non-V devices	2	30	V
		V devices	2	32	V
T_J	Junction temperature	LM139x	–55	125	°C
		LM239x	–25	85	
		LM339x	–0	70	
		LM2901x	–40	125	

6.6 Thermal Information

THERMAL METRIC(1)		All Devices						UNIT
		N (PDIP)	D (SOIC)	PW (TSSOP)	DB (SSOP)	NS (SOP)	RTE (QFN)	
		14 PINS	14 PINS	14 PINS	14 PINS	14 PINS	16 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	114.9	111.2	136.6	111.8	96.2	67.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	93.8	66.9	66.6	63.6	56.1	72.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	77.7	67.8	79.8	60.5	56.9	43.1	°C/W
ψ_{JT}	Junction-to-top characterization parameter	60.4	28.0	17.8	26.2	24.8	6.3	°C/W
ψ_{JB}	Junction-to-board characterization parameter	76.7	67.4	79.3	58.5	56.4	42.8	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	-	-	-	-	-	26.4	°C/W

(1) For more information about traditional and new thermal metrics, see the Semicondctor and IC Package Thermal Metrics report, SPRA953.

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6.7 Electrical Characteristics for LM339B

V_S = 5V, V_{CM} = (V–) ; T_A = 25°C (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	V_S = 5 to 36V	–3.5	±0.37	3.5	mV
		V_S = 5 to 36V, T_A = –40°C to +85°C	–5.5		5.5	
I_B	Input bias current			–3.5	–25	nA
		T_A = –40°C to +85°C			–50	nA
I_{OS}	Input offset current		–25	±0.5	25	nA
		T_A = –40°C to +85°C	–50		50	nA
V_{CM}	Common mode range (1)	V_S = 3 to 36V	(V–)		(V+) – 1.5	V
		V_S = 3 to 36V, T_A = –40°C to +85°C	(V–)		(V+) – 2.0	V
A_{VD}	Large signal differential voltage amplification	V_S = 15V, V_O = 1.4V to 11.4V; R_L ≥ 15k to (V+)	50	200		V/mV
V_{OL}	Low level output Voltage {swing from (V–)}	I_{SINK} ≤ 4mA, V_{ID} = -1V		110	400	mV
		I_{SINK} ≤ 4mA, V_{ID} = -1V T_A = –40°C to +85°C			550	mV
I_{OH-LKG}	High-level output leakage current	(V+) = V_O = 5V; V_{ID} = 1V		0.1	50	nA
		(V+) = V_O = 36V; V_{ID} = 1V			100	nA
I_{OL}	Low level output current	V_{OL} = 1.5V; V_{ID} = -1V; V_S = 5V	6	21		mA
I_Q	Quiescent current (all comparators)	V_S = 5V, no load		0.8	1.2	mA
		V_S = 36V, no load, T_A = –40°C to +85°C		1	1.6	mA

(1) When the voltage at either input goes negative by more than 0.3V, the output can be incorrect and excessive input current can flow. The upper end of the common-mode voltage range is limited by V_{CC} – 2V. However only one input needs to be in the valid common mode range, the other input can go up the maximum V_{CC} level and the comparator provides a proper output state. Either or both inputs can go to maximum V_{CC} level without damage.

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6.8 Electrical Characteristics for LM2901B

V_S = 5V, V_{CM} = (V–) ; T_A = 25°C (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	V_S = 5 to 36V	–3.5	±0.37	3.5	mV
		V_S = 5 to 36V, T_A = –40°C to +125°C	–5.5		5.5	
I_B	Input bias current			–3.5	–25	nA
		T_A = –40°C to +125°C			–50	nA
I_{OS}	Input offset current		–25	±0.5	25	nA
		T_A = –40°C to +125°C	–50		50	nA
V_{CM}	Common mode range (1)	V_S = 3 to 36V	(V–)		(V+) – 1.5	V
		V_S = 3 to 36V, T_A = –40°C to +125°C	(V–)		(V+) – 2.0	V
A_{VD}	Large signal differential voltage amplification	V_S = 15V, V_O = 1.4V to 11.4V; R_L ≥ 15k to (V+)	50	200		V/mV
V_{OL}	Low level output Voltage {swing from (V–)}	I_{SINK} ≤ 4mA, V_{ID} = -1V		110	400	mV
		I_{SINK} ≤ 4mA, V_{ID} = -1V T_A = –40°C to +125°C			550	mV
I_{OH-LKG}	High-level output leakage current	(V+) = V_O = 5V; V_{ID} = 1V		0.1	50	nA
		(V+) = V_O = 36V; V_{ID} = 1V			100	nA
I_{OL}	Low level output current	V_{OL} = 1.5V; V_{ID} = -1V; V_S = 5V	6	21		mA
I_Q	Quiescent current (all comparators)	V_S = 5V, no load		0.8	1.2	mA
		V_S = 36V, no load, T_A = –40°C to +125°C		1	1.6	mA

(1) When the voltage at either input goes negative by more than 0.3V, the output can be incorrect and excessive input current can flow. The upper end of the common-mode voltage range is limited by V_{CC} – 2V. However only one input needs to be in the valid common mode range, the other input can go up the maximum V_{CC} level and the comparator provides a proper output state. Either or both inputs can go to maximum V_{CC} level without damage.

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6.9 Electrical Characteristics for LM139 and LM139A

at specified free-air temperature, V_{CC} = 5V (unless otherwise noted)

PARAMETER		TEST CONDITIONS(1)		T_A (2)	LM139			LM139A			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_{CC} = 5V to 30V, V_{IC} = V_{ICR} min, V_O = 1.4V		25°C		2	5		1	2	mV
				Full range			9			4	
I_{IO}	Input offset current	V_O = 1.4V		25°C		3	25		3	25	nA
				Full range			100			100	
I_{IB}	Input bias current	V_O = 1.4V		25°C		–25	–100		–25	–100	nA
				Full range			–300			–300	
V_{ICR}	Common-mode input-voltage range(3)			25°C	0 to V_{CC} – 1.5			0 to V_{CC} – 1.5			V
				Full range	0 to V_{CC} – 2			0 to V_{CC} – 2			
A_{VD}	Large-signal differential-voltage amplification	V_{CC+} = ±7.5V, V_O = –5V to 5V		25°C		200		50	200		V/mV
I_{OH}	High-level output current	V_{ID} = 1V	V_{OH} = 5V	25°C		0.1			0.1		nA
			V_{OH} = 30V	Full range			1			1	µA
V_{OL}	Low-level output voltage	V_{ID} = –1V,	I_{OL} = 4mA	25°C		150	400		150	400	mV
				Full range			700			700	
I_{OL}	Low-level output current	V_{ID} = –1V,	V_{OL} = 1.5V	25°C	6	16		6	16		mA
I_{CC}	Supply current (four comparators)	V_O = 2.5V,	No load	25°C		0.8	2		0.8	2	mA

(1) All characteristics are measured with zero common-mode input voltage, unless otherwise specified.
(2) Full range (MIN to MAX) for LM139 and LM139A is –55°C to +125°C. All characteristics are measured with zero common-mode input voltage, unless otherwise specified.
(3) The voltage at either input or common-mode must not be allowed to go negative by more than 0.3V. The upper end of the common-mode voltage range is V_{CC+} – 1.5V; however, one input can exceed V_{CC}, and the comparator provides a proper output state as long as the other input remains in the common-mode range. Either or both inputs can go to 30V without damage.

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6.10 Electrical Characteristics for LMx39 and LMx39A

at specified free-air temperature, V_{CC} = 5V (unless otherwise noted)

PARAMETER		TEST CONDITIONS(1)		T_A (2)	LM239 LM339			LM239A LM339A			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_{CC} = 5V to 30V, V_{IC} = V_{ICR} min, V_O = 1.4V		25°C		2	5		1	3	mV
				Full range			9			4	
I_{IO}	Input offset current	V_O = 1.4V		25°C		5	50		5	50	nA
				Full range			150			150	
I_{IB}	Input bias current	V_O = 1.4V		25°C		–25	–250		–25	–250	nA
				Full range			–400			–400	
V_{ICR}	Common-mode input-voltage range(3)			25°C	0 to V_{CC} – 1.5			0 to V_{CC} – 1.5			V
				Full range	0 to V_{CC} – 2			0 to V_{CC} – 2			
A_{VD}	Large-signal differential-voltage amplification	V_{CC} = 15V, V_O = 1.4V to 11.4V, R_L ≥ 15kΩ to V_{CC}		25°C	50	200		50	200		V/mV
I_{OH}	High-level output current	V_{ID} = 1V	V_{OH} = 5V	25°C		0.1	50		0.1	50	nA
			V_{OH} = 30V	Full range			1			1	µA
V_{OL}	Low-level output voltage	V_{ID} = –1V,	I_{OL} = 4mA	25°C		150	400		150	400	mV
				Full range			700			700	
I_{OL}	Low-level output current	V_{ID} = –1V,	V_{OL} = 1.5V	25°C	6	16		6	16		mA
I_{CC}	Supply current (four comparators)	V_O = 2.5V,	No load	25°C		0.8	2		0.8	2	mA

(1) All characteristics are measured with zero common-mode input voltage, unless otherwise specified.
(2) Full range (MIN to MAX) for LM239/LM239A is –25°C to +85°C, and for LM339/LM339A is 0°C to 70°C. All characteristics are measured with zero common-mode input voltage, unless otherwise specified.
(3) The voltage at either input or common-mode must not be allowed to go negative by more than 0.3V. The upper end of the common-mode voltage range is V_{CC+} – 1.5V; however, one input can exceed V_{CC}, and the comparator provides a proper output state as long as the other input remains in the common-mode range. Either or both inputs can go to 30V without damage.

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6.11 Electrical Characteristics for LM2901, LM2901V and LM2901AV

at specified free-air temperature, V_{CC} = 5V (unless otherwise noted)

PARAMETER		TEST CONDITIONS[1]		T_A [2]	LM2901			UNIT
					MIN	TYP	MAX	
V_{IO}	Input offset voltage	$V_{IC} = V_{ICR}$ min, V_O = 1.4V, V_{CC} = 5V to MAX[3]	Non-A devices	25°C		2	7	mV
				Full range			15	
			A-suffix devices	25°C		1	2	
				Full range			4	
I_{IO}	Input offset current	V_O = 1.4V		25°C		5	50	nA
				Full range			200	
I_{IB}	Input bias current	V_O = 1.4V		25°C		–25	–250	nA
				Full range			–500	
V_{ICR}	Common-mode input-voltage range[4]			25°C	0 to V_{CC} – 1.5			V
				Full range	0 to V_{CC} – 2			
A_{VD}	Large-signal differential-voltage amplification	V_{CC} = 15V, V_O = 1.4V to 11.4V, R_L ≥ 15kΩ to V_{CC}		25°C	25	100		V/mV
I_{OH}	High-level output current	V_{ID} = 1V	V_{OH} = 5V	25°C		0.1	50	nA
			V_{OH} = V_{CC} MAX[3]	Full range			1	µA
V_{OL}	Low-level output voltage	V_{ID} = –1V, I_{OL} = 4mA	Non-V devices	25°C		150	500	mV
			V-suffix devices			150	400	
			All devices	Full range			700	
I_{OL}	Low-level output current	V_{ID} = –1V,	V_{OL} = 1.5V	25°C	6	16		mA
I_{CC}	Supply current (four comparators)	V_O = 2.5V, No load	V_{CC} = 5V	25°C		0.8	2	mA
			V_{CC} = MAX[3]			1	2.5	

(1) All characteristics are measured with zero common-mode input voltage, unless otherwise specified.
(2) Full range (MIN to MAX) for LM2901 is –40°C to +125°C. All characteristics are measured with zero common-mode input voltage, unless otherwise specified.
(3) V_{CC} MAX = 30V for non-V devices, and 32V for V-suffix devices
(4) The voltage at either input or common-mode must not be allowed to go negative by more than 0.3V. The upper end of the common-mode voltage range is V_{CC+} – 1.5V; however, one input can exceed V_{CC}, and the comparator provides a proper output state as long as the other input remains in the common-mode range. Either or both inputs can go to V_{CC} MAX without damage.

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6.12 Switching Characteristics for LM139 and LM139A

V_{CC} = 5V, T_A = 25°C

PARAMETER	TEST CONDITIONS		LM139 LM139A	UNIT
			TYP	
Response time	R_L connected to 5V through 5.1kΩ, C_L = 15pF(1) (2)	100mV input step with 5mV overdrive	1.3	µs
		TTL-level input step	0.3	

(1) C_L includes probe and jig capacitance.
(2) The response time specified is the interval between the input step function and the instant when the output crosses 1.4V.

6.13 Switching Characteristics for LM339B and LM2901B

V_S = 5V, V_{O_PULLUP} = 5V, V_{CM} = V_S/2, C_L = 15pF, R_L = 5.1kOhm, T_A = 25°C (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{response}$	Propagation delay time, high-to-low; Small scale input signal (1)	Input overdrive = 5mV, Input step = 100mV		1000		ns
$t_{response}$	Propagation delay time, high-to-low; TTL input signal (1)	TTL input with V_{ref} = 1.4V		300		ns

(1) High-to-low and low-to-high refers to the transition at the input.

6.14 Switching Characteristics for LMx39 and LMx39A

V_{CC} = 5V, T_A = 25°C

PARAMETER	TEST CONDITIONS		LM239 LM239A LM339 LM339A	UNIT
			TYP	
Response time	R_L connected to 5V through 5.1kΩ, C_L = 15pF(1) (2)	100mV input step with 5mV overdrive	1.3	µs
		TTL-level input step	0.3	

(1) C_L includes probe and jig capacitance.
(2) The response time specified is the interval between the input step function and the instant when the output crosses 1.4V.

6.15 Switching Characteristics for LM2901

V_{CC} = 5V, T_A = 25°C

PARAMETER	TEST CONDITIONS		LM2901	UNIT
			TYP	
Response time	R_L connected to 5V through 5.1kΩ, C_L = 15pF(1) (2)	100mV input step with 5mV overdrive	1.3	µs
		TTL-level input step	0.3	

(1) C_L includes probe and jig capacitance.
(2) The response time specified is the interval between the input step function and the instant when the output crosses 1.4V.

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6.16 Typical Characteristics

T_A = 25°C, V_S = 5V, R_{PULLUP} = 5.1k, C_L = 15pF, V_{CM} = 0V, $V_{UNDERDRIVE}$ = 100mV, $V_{OVERDRIVE}$ = 100mV unless otherwise noted.

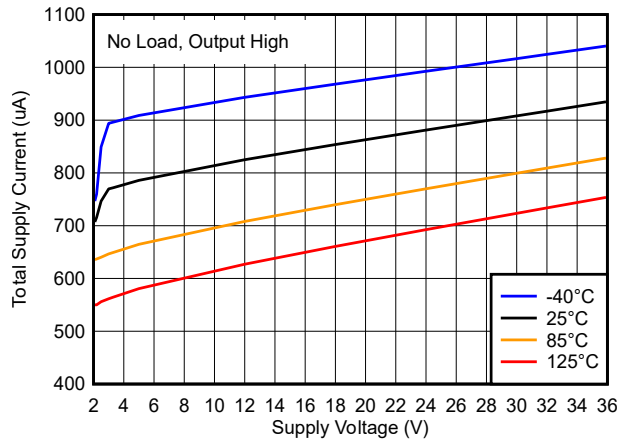


図 6-1. Total Supply Current vs. Supply Voltage

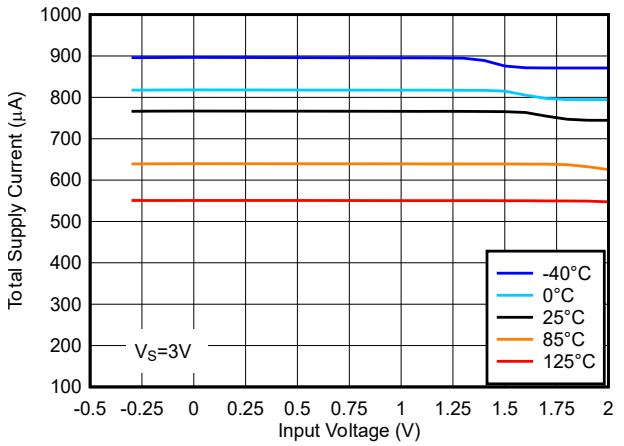


図 6-2. Total Supply Current vs. Input Voltage at 3V

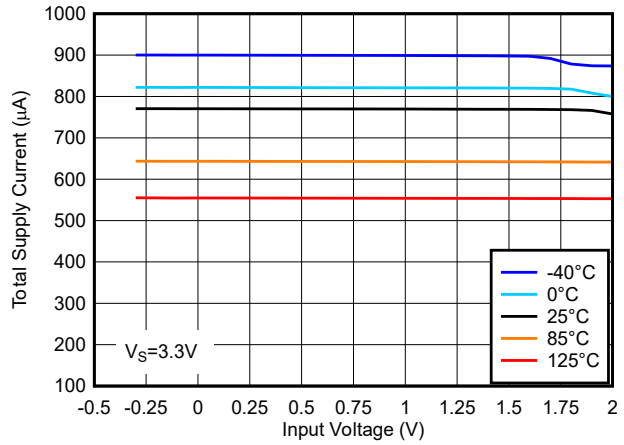


図 6-3. Total Supply Current vs. Input Voltage at 3.3V

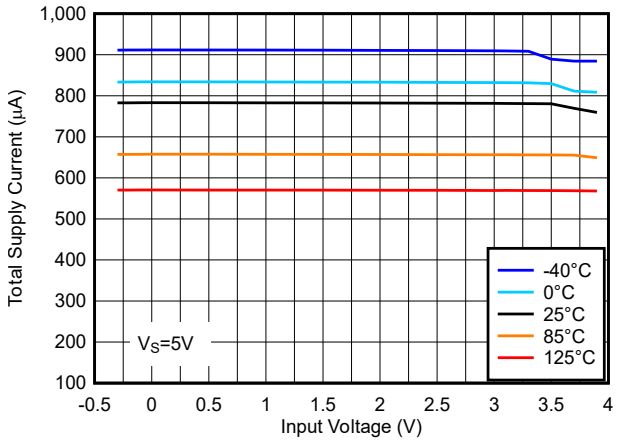


図 6-4. Total Supply Current vs. Input Voltage at 5V

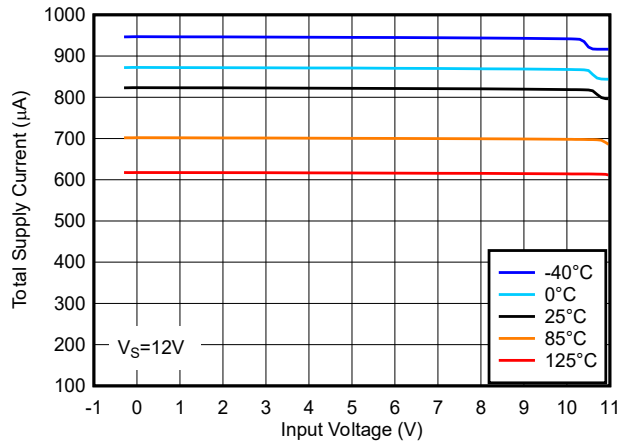


図 6-5. Total Supply Current vs. Input Voltage at 12V

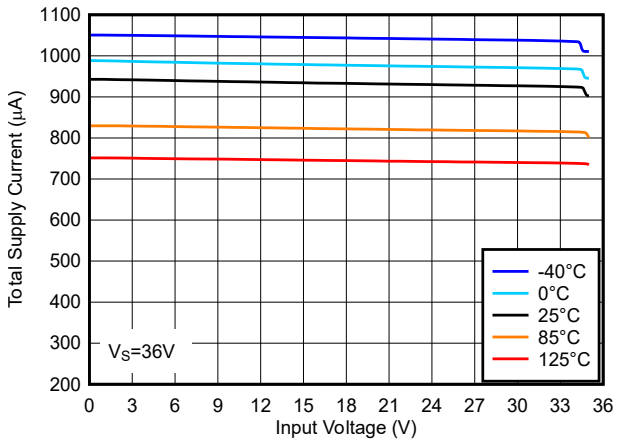


図 6-6. Total Supply Current vs. Input Voltage at 36V

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6.16 Typical Characteristics (continued)

T_A = 25°C, V_S = 5V, R_{PULLUP} = 5.1k, C_L = 15pF, V_{CM} = 0V, $V_{UNDERDRIVE}$ = 100mV, $V_{OVERDRIVE}$ = 100mV unless otherwise noted.

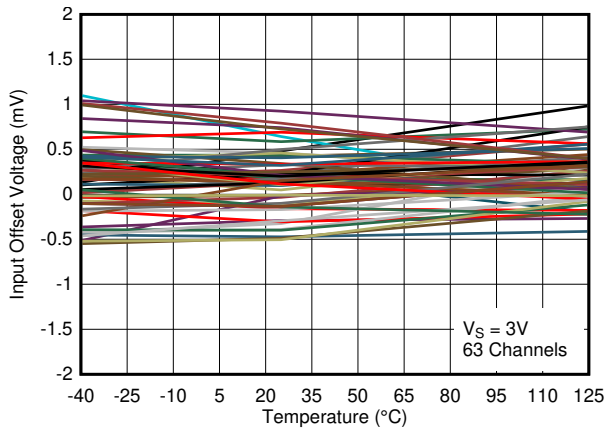


図 6-7. Input Offset Voltage vs. Temperature at 3V

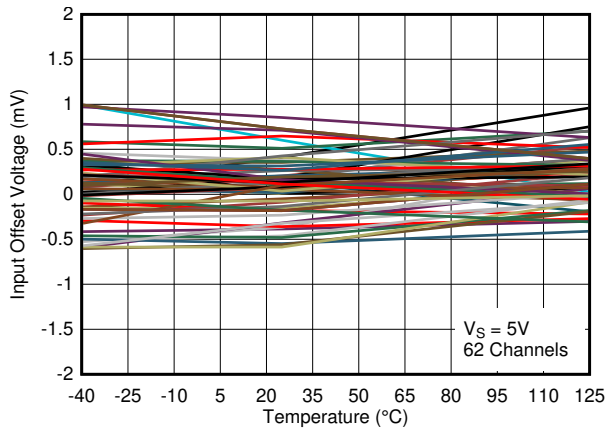


図 6-8. Input Offset Voltage vs. Temperature at 5V

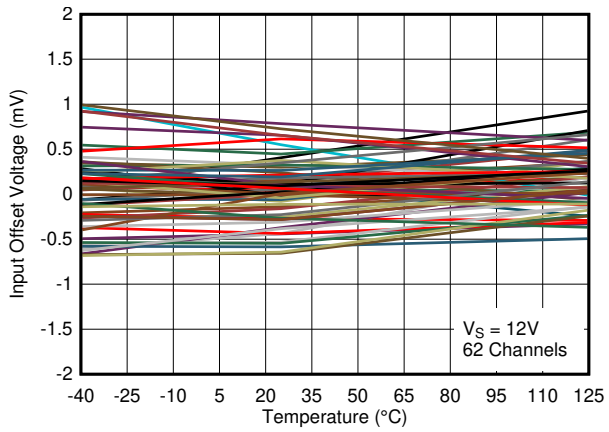


図 6-9. Input Offset Voltage vs. Temperature at 12V

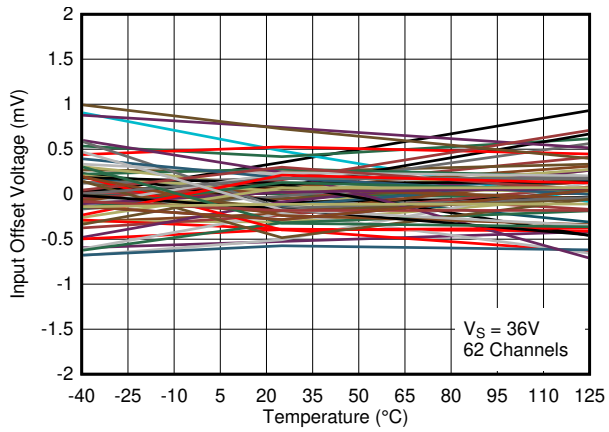


図 6-10. Input Offset Voltage vs. Temperature at 36V

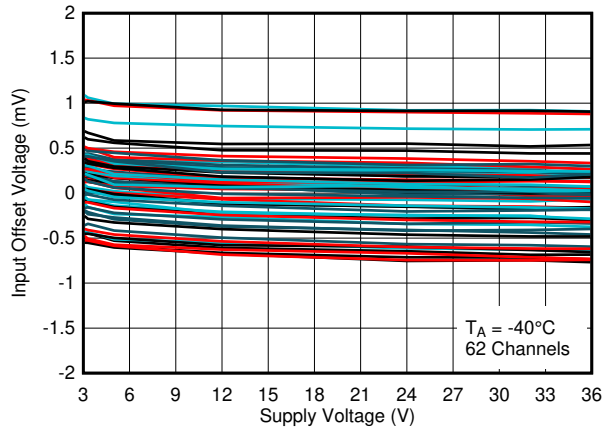


図 6-11. Input Offset Voltage vs. Supply Voltage at -40°C

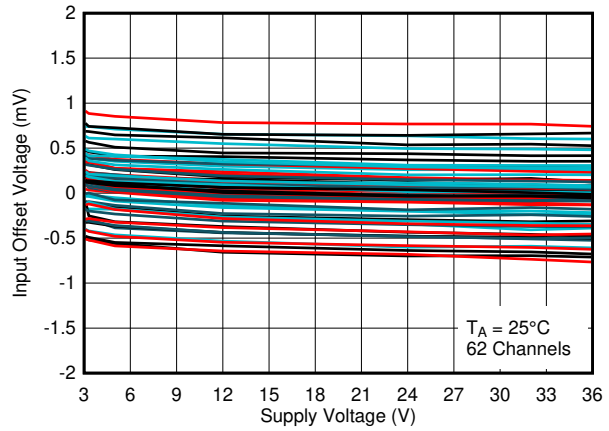


図 6-12. Input Offset Voltage vs. Supply Voltage at 25°C

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6.16 Typical Characteristics (continued)

T_A = 25°C, V_S = 5V, R_{PULLUP} = 5.1k, C_L = 15pF, V_{CM} = 0V, $V_{UNDERDRIVE}$ = 100mV, $V_{OVERDRIVE}$ = 100mV unless otherwise noted.

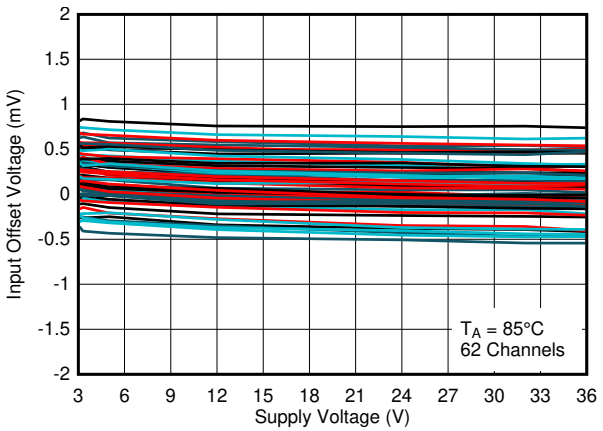


図 6-13. Input Offset Voltage vs. Supply Voltage at 85°C

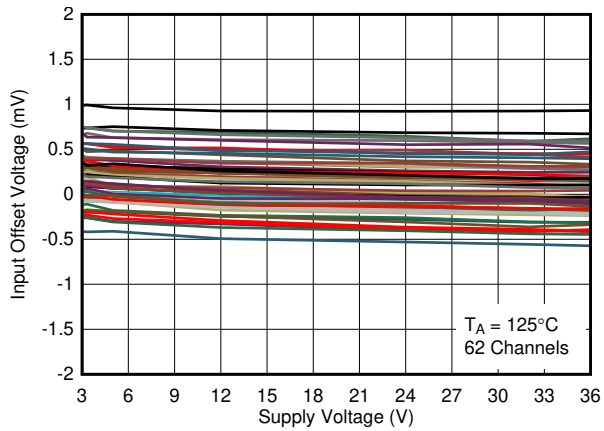


図 6-14. Input Offset Voltage vs. Supply Voltage at 125°C

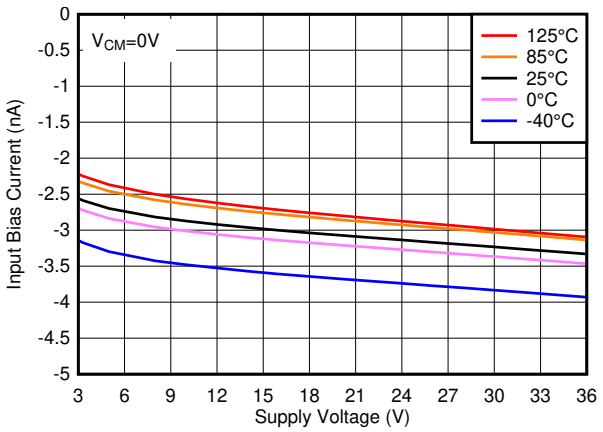


図 6-15. Input Bias Current vs. Supply Voltage

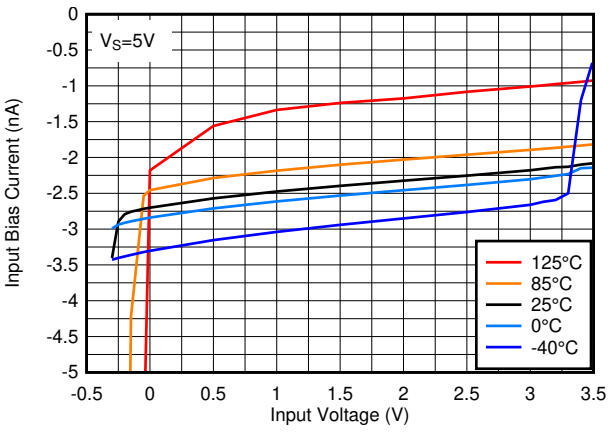


図 6-16. Input Bias Current vs. Input Voltage at 5V

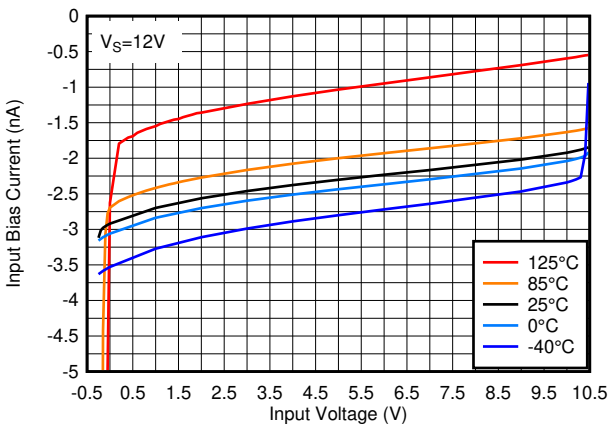


図 6-17. Input Bias Current vs. Input Voltage at 12V

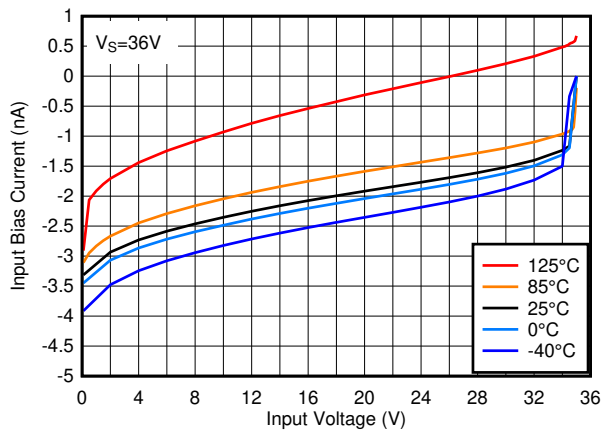


図 6-18. Input Bias Current vs. Input Voltage at 36V

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6.16 Typical Characteristics (continued)

T_A = 25°C, V_S = 5V, R_{PULLUP} = 5.1k, C_L = 15pF, V_{CM} = 0V, $V_{UNDERDRIVE}$ = 100mV, $V_{OVERDRIVE}$ = 100mV unless otherwise noted.

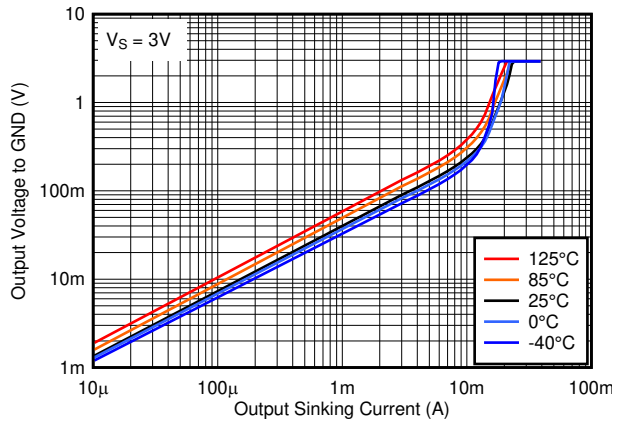


図 6-19. Output Low Voltage vs. Output Sinking Current at 3V

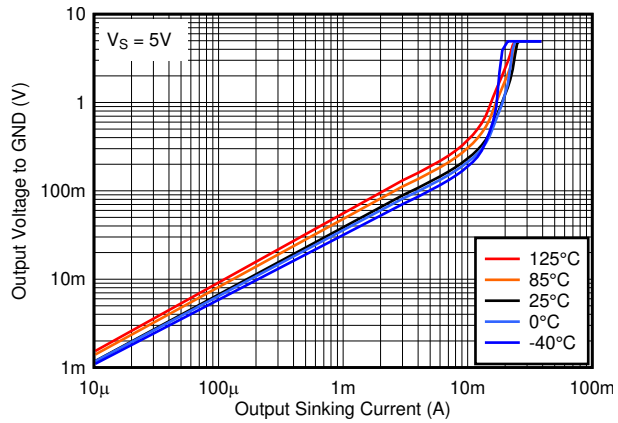


図 6-20. Output Low Voltage vs. Output Sinking Current at 5V

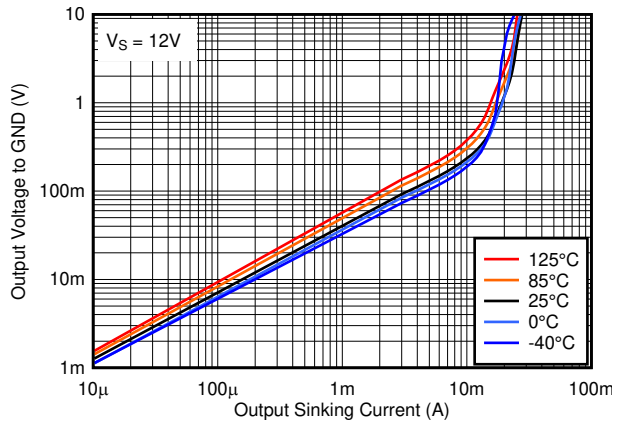


図 6-21. Output Low Voltage vs. Output Sinking Current at 12V

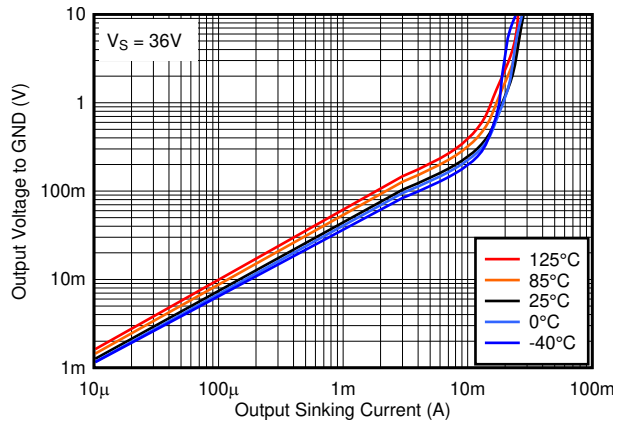


図 6-22. Output Low Voltage vs. Output Sinking Current at 36V

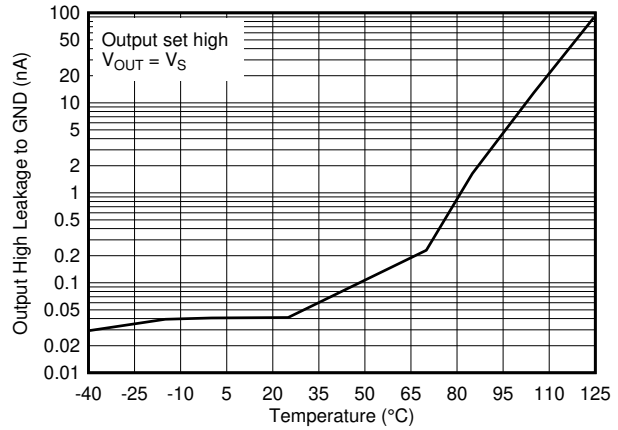


図 6-23. Output High Leakage Current vs. Temperature at 5V

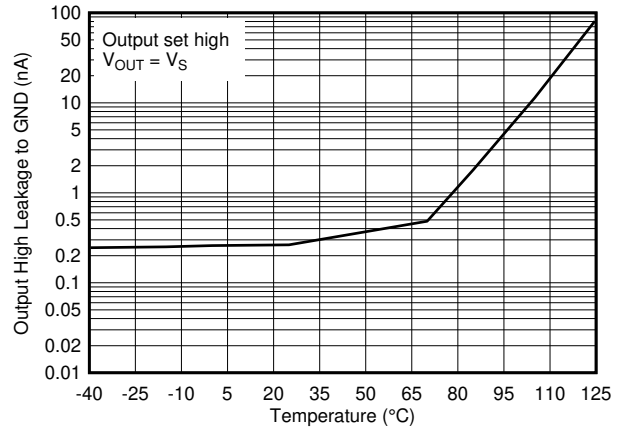


図 6-24. Output High Leakage Current vs. Temperature at 36V

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6.16 Typical Characteristics (continued)

T_A = 25°C, V_S = 5V, R_{PULLUP} = 5.1k, C_L = 15pF, V_{CM} = 0V, $V_{UNDERDRIVE}$ = 100mV, $V_{OVERDRIVE}$ = 100mV unless otherwise noted.

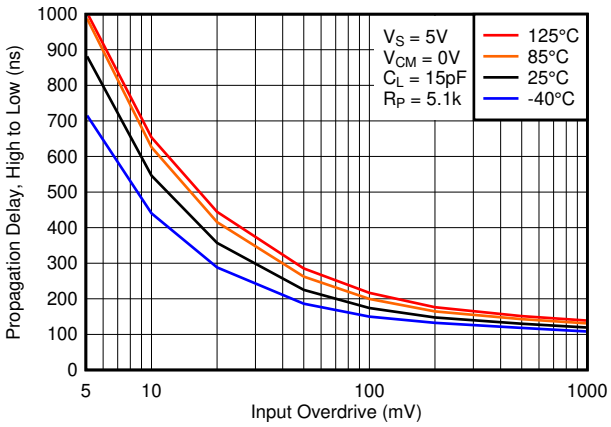


図 6-25. High to Low Propagation Delay vs. Input Overdrive Voltage, 5V

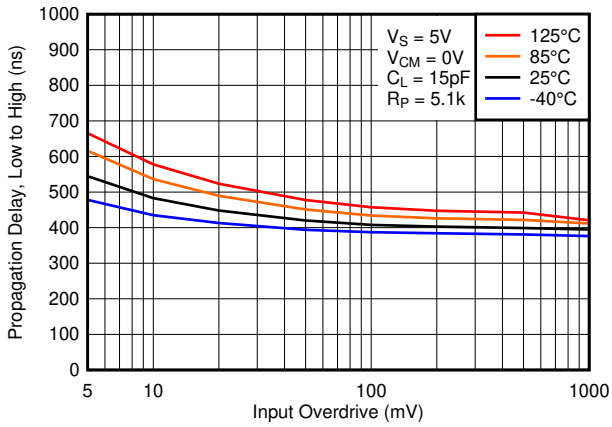


図 6-26. Low to High Propagation Delay vs. Input Overdrive Voltage, 5V

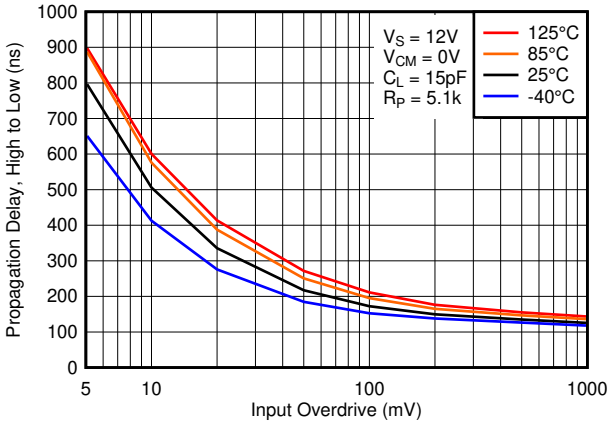


図 6-27. High to Low Propagation Delay vs. Input Overdrive Voltage, 12V

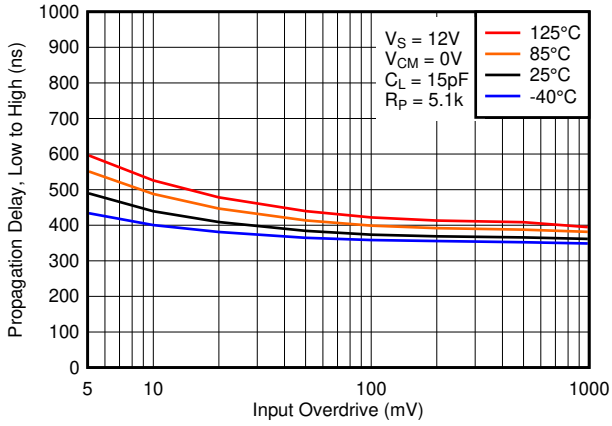


図 6-28. Low to High Propagation Delay vs. Input Overdrive Voltage, 12V

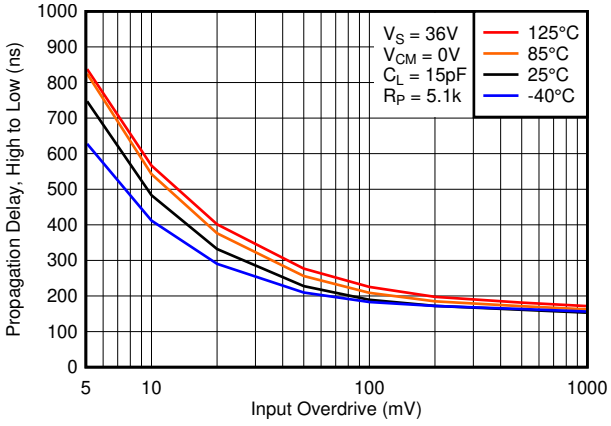


図 6-29. High to Low Propagation Delay vs. Input Overdrive Voltage, 36V

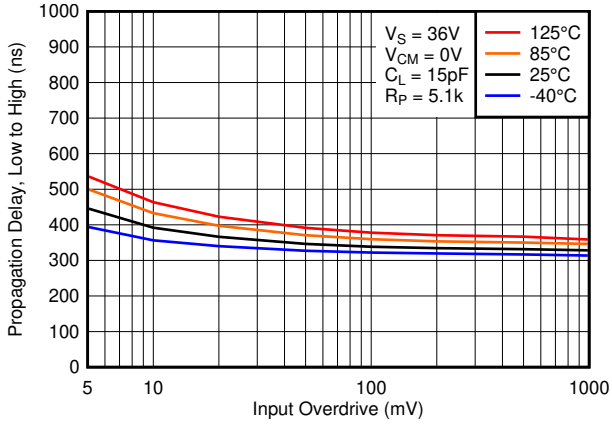


図 6-30. Low to High Propagation Delay vs. Input Overdrive Voltage, 36V

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6.16 Typical Characteristics (continued)

T_A = 25°C, V_S = 5V, R_{PULLUP} = 5.1k, C_L = 15pF, V_{CM} = 0V, $V_{UNDERDRIVE}$ = 100mV, $V_{OVERDRIVE}$ = 100mV unless otherwise noted.

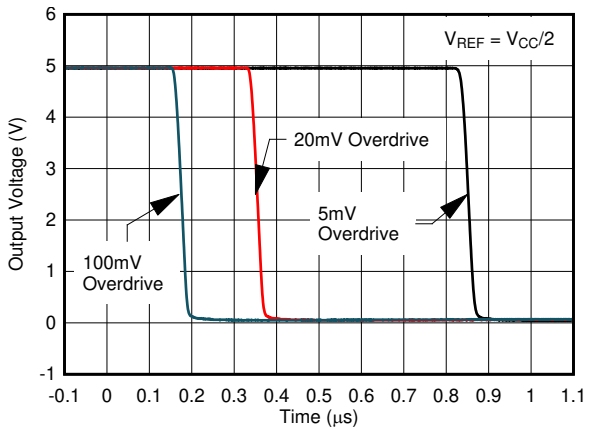


図 6-31. Response Time for Various Overdrives, High-to-Low Transition

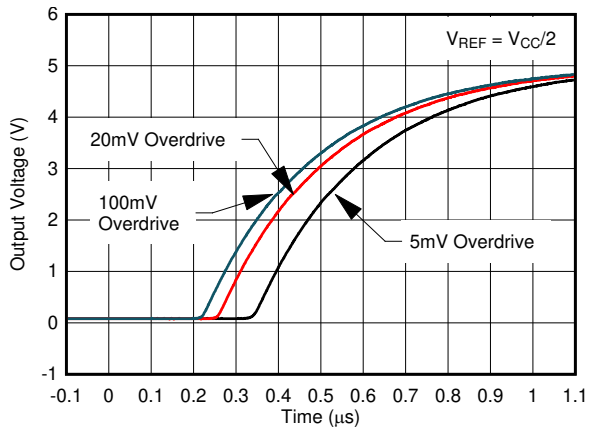


図 6-32. Response Time for Various Overdrives, Low-to-High Transition

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7 Detailed Description

7.1 Overview

These dual comparators have the ability to operate up to absolute maximum of 36V (38V for the "B" version) on the supply pin. This device has proven ubiquity and versatility across a wide range of applications. This is due to very wide supply voltages range, low Iq and fast response of the devices.

The open-collector outputs allow the user to level shift to the desired logic level indpendent of VCC, while also enabling AND functionality when multiple outputs are connected together.

7.2 Functional Block Diagram

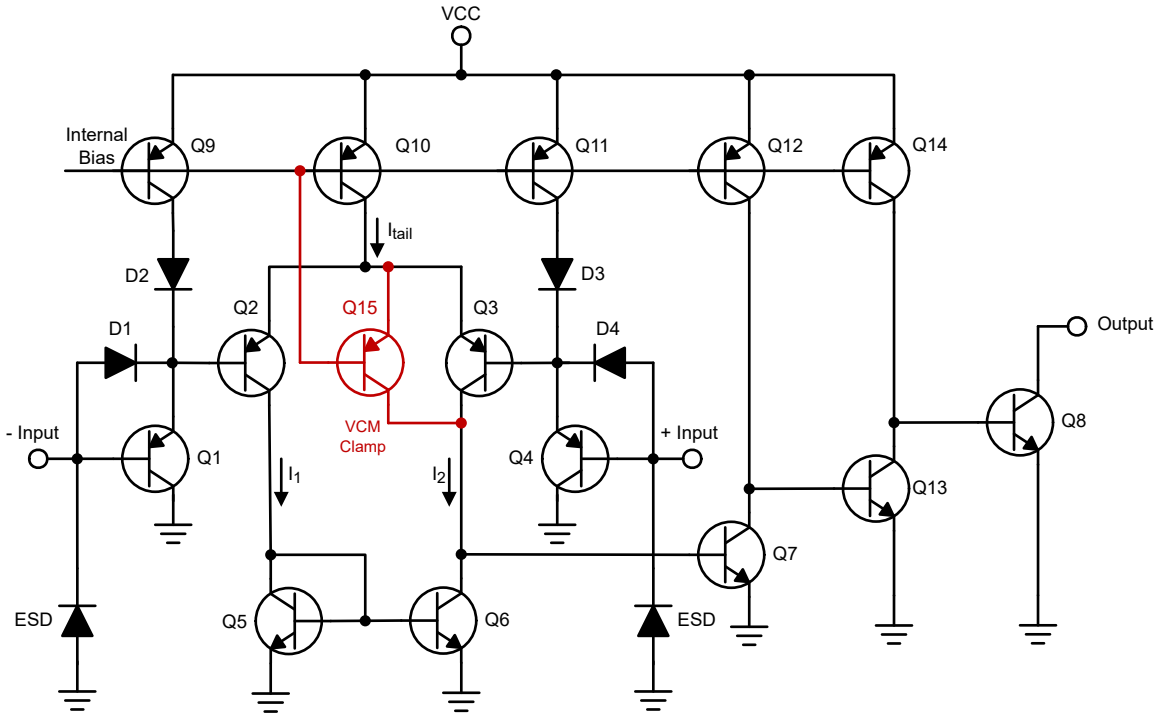


図 7-1. Schematic (Each Comparator)

7.3 Feature Description

The comparator consists of a PNP Darlington pair input, allowing the device to operate with very high gain and fast response with minimal input bias current. The input Darlington pair creates a limit on the input common mode voltage capability, allowing the comparator to accurately function from ground to V_{CC} – 2V over temperature. A clamp is added around Q3 to mimic the both inputs above input voltage range behavior of the original classic silicon.

The output consists of an open drain NPN (pull-down or low side) transistor. The output NPN sinks current when the negative input voltage is higher than the positive input voltage and the offset voltage. The V_{OL} is resistive and scales with the output current. Please see the "Output Low Voltage vs. Output Sinking Current" graphs for V_{OL} values with respect to the output current.

7.4 Device Functional Modes

7.4.1 Voltage Comparison

The comparator operates solely as a voltage comparator, comparing the differential voltage between the positive and negative pins and outputting a logic low or high impedance (logic high with pullup) based on the input differential polarity.

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8 Application and Implementation

注

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8.1 Application Information

Typically, a comparator compares either a single signal to a reference, or to two differnt signals. Many users take advantage of the open-drain output to drive the comparison logic output to a logic voltage level to an MCU or logic device. The wide supply range and high voltage capability makes LMx39 or LM2901x an excellent choice for level shifting to a higher or lower voltage.

8.2 Typical Application

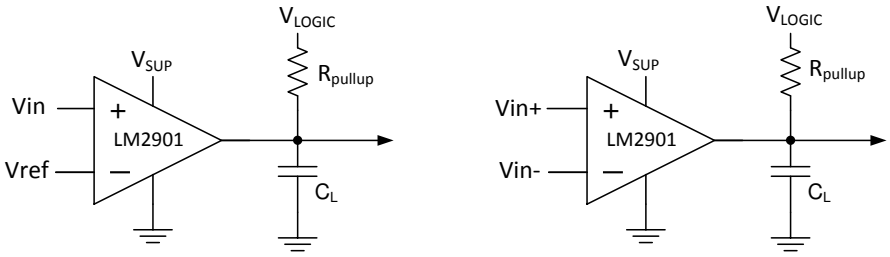


図 8-1. Single-ended and Differential Comparator Configurations

8.2.1 Design Requirements

For this design example, use the parameters listed in 表 8-1 as the input parameters.

表 8-1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input Voltage Range	0V to Vsup-2V
Supply Voltage	4.5V to V_{CC} maximum
Logic Supply Voltage	0V to V_{CC} maximum
Output Current (R_{PULLUP})	1µA to 4mA
Input Overdrive Voltage	100mV
Reference Voltage	2.5V
Load Capacitance (C_L)	15pF

8.2.2 Detailed Design Procedure

When using the LMx39 in a general comparator application, determine the following:

- Input voltage range
- Minimum overdrive voltage
- Output and drive current
- Response time

8.2.2.1 Input Voltage Range

When choosing the input voltage range, the input common mode voltage range (V_{ICR}) must be taken in to account. If temperature operation is below 25°C the V_{ICR} can range from 0V to V_{CC}– 2.0V. This limits the input voltage range to as high as V_{CC}– 2.0V and as low as 0V. Operation outside of this range can yield incorrect comparisons.

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The following is a list of input voltage situation and the outcomes:

1. When both IN- and IN+ are both within the common-mode range:
   a. If IN- is higher than IN+ and the offset voltage, the output is low and the output transistor is sinking current
   b. If IN- is lower than IN+ and the offset voltage, the output is high impedance and the output transistor is not conducting
2. When IN- is higher than common-mode and IN+ is within common-mode, the output is low and the output transistor is sinking current
3. When IN+ is higher than common-mode and IN- is within common-mode, the output is high impedance and the output transistor is not conducting
4. When IN- and IN+ are both higher than common-mode, see Section 2 of Application Design Guidelines for LM339, LM393, TL331 Family Comparators Including the New B-versions.

8.2.2.2 Minimum Overdrive Voltage

Overdrive voltage is the differential voltage produced between the positive and negative inputs of the comparator over the offset voltage (V_{IO}). To make an accurate comparison, the overdrive voltage (V_{OD}) must be higher than the input offset voltage (V_{IO}). Overdrive voltage can also determine the response time of the comparator, with the response time decreasing with increasing overdrive. 図 8-2 and 図 8-3 show positive and negative response times with respect to overdrive voltage.

8.2.2.3 Output and Drive Current

Output current is determined by the load and pullup resistance and logic and pullup voltage. The output current produces a low-level output voltage (V_{OL}) from the comparator, where V_{OL} is proportional to the output current.

The output current can also effect the transient response.

8.2.2.4 Response Time

Response time is a function of input over-drive. See the Typical Characteristics graphs for typical response times. The rise and fall times can be determined by the load capacitance (C_L), load/pull-up resistance (R_{PULLUP}) and equivalent collector-emitter resistance (R_{CE}).

- The rise time (τ_R) is approximately $\tau_R = R_{PULLUP} \times C_L$
- The fall time (τ_F) is approximately $\tau_F = R_{CE} \times C_L$
  – R_{CE} can be determined by taking the slope of 図 6-31 in the linear region at the desired temperature, or by dividing the V_{OL} by I_{OUT}

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8.2.3 Application Curves

図 8-2 and 図 8-3 were generated with scope probe parasitic capacitance of 50pF.

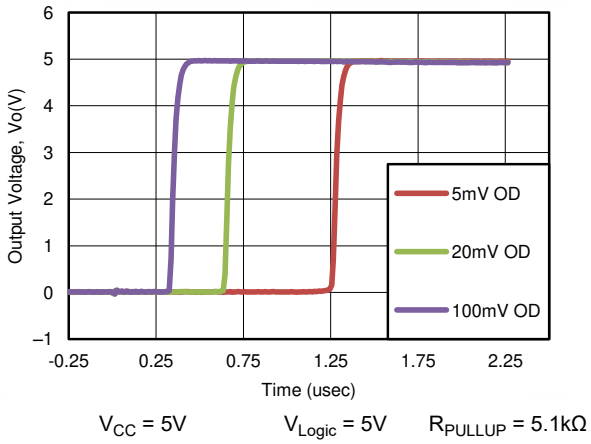


図 8-2. Response Time vs Output Voltage (Positive Transition)

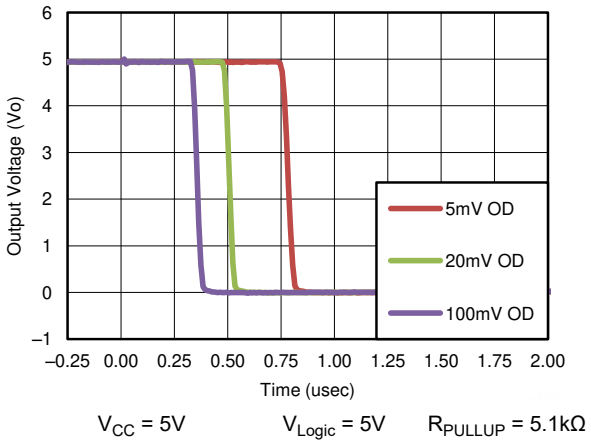


図 8-3. Response Time vs Output Voltage (Negative Transition)

8.3 Power Supply Recommendations

For fast response and comparison applications with noisy or AC inputs, use a bypass capacitor on the supply pin to reject any variation on the supply voltage. This variation can affect the common-mode range of the comparator input and create an inaccurate comparison.

8.4 Layout

8.4.1 Layout Guidelines

For accurate comparator applications without hysteresis maintaining a stable power supply with minimized noise and glitches is critical. Best practice is to add a bypass capacitor between the supply voltage and ground. This can be implemented on the positive power supply and negative supply (if available). If a negative supply is not being used, do not put a capacitor between the GND pin and system ground.

Minimize coupling between outputs and inverting inputs to prevent output oscillations. Do not run output and inverting input traces in parallel unless there is a V_{CC} or GND trace between output and inverting input traces to reduce coupling. When series resistance is added to inputs, place resistor close to the device.

8.4.2 Layout Example

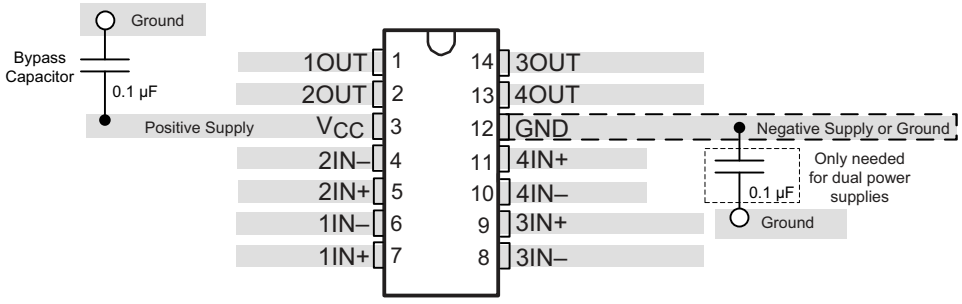


図 8-4. LMx39 Layout Example

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9 Device and Documentation Support

9.1 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

表 9-1. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
LM139	Click here	Click here	Click here	Click here	Click here
LM239	Click here	Click here	Click here	Click here	Click here
LM339	Click here	Click here	Click here	Click here	Click here
LM339B	Click here	Click here	Click here	Click here	Click here
LM139A	Click here	Click here	Click here	Click here	Click here
LM239A	Click here	Click here	Click here	Click here	Click here
LM339A	Click here	Click here	Click here	Click here	Click here
LM2901	Click here	Click here	Click here	Click here	Click here
LM2901B	Click here	Click here	Click here	Click here	Click here
LM2901AV	Click here	Click here	Click here	Click here	Click here
LM2901V	Click here	Click here	Click here	Click here	Click here

9.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

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9.6 用語集

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10 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision Y (March 2025) to Revision Z (May 2025) **Page**

- Added missing *Revision History* entry for "Updated Thermal Information" table in revision "Y"..... 5
- Fixed duplicated Fig 6-4 graph..... 5

Changes from Revision X (October 2023) to Revision Y (March 2025) **Page**

- 「*製品情報*」表からレガシーデバイスを削除..... 1
- 最初のページの ESD 値を「*ファミリ比較表*」で更新..... 1
- Updated *Thermal Information* table..... 5
- Removed legacy device graphs..... 13
- Updated internal schematic..... 19

Changes from Revision W (October 2023) to Revision X (October 2023) **Page**

- SOT-23/QFN の「製品情報」表に LM339B および LM2901B を追加..... 1

Changes from Revision V (December 2022) to Revision W (October 2023) **Page**

- Updated thermal tables for new package releases..... 5
- Changed Apps Input Voltage Range text to reference appnote..... 20

Changes from Revision U (November 2018) to Revision V (December 2022) **Page**

- ドキュメント全体にわたって表、図、相互参照の採番方法を更新。..... 1
- 全体を通して「B」バージョンを追加「製品ファミリ」表を追加..... 1

Changes from Revision T (June 2015) to Revision U (November 2018) **Page**

- 「概要」セクションで LM239x の最大温度仕様を 125℃から 85℃に変更..... 1
- データシートのタイトルを変更..... 1
- Changed LM293AD to LM239AD in *Device Comparison Table* 3
- Added Input Current and related footnote in *Absolute Maximum Ratings* 5
- Changed layout of *Recommended Operating Conditions* temperatures to separate rows..... 6
- Added LM2901V and LMV2901AV to LM2901 Elect Char Table title to make more clear which devices are covered..... 11
- Changed "Dual" to "Quad" and removed "Absolute Maximum" wording and mention of Q100 in *Overview* section text..... 19
- Changed and corrected text in *Feature Description* section..... 19
- Changed Example Values in *Typical Application Design Parameters* table 20
- Added *Receiving Notification of Documentation Updates* section..... 23

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Changes from Revision S (August 2012) to Revision T (June 2015) **Page**

- 「*注文情報*」表を削除。 1
- 「*特長*」の一覧に軍事利用についての免責事項を追加。 1
- 「アプリケーション」、「製品情報」表、「ピン構成および機能」セクション、「ESD 定格」表、「熱に関する情報」表、「機能説明」セクション、「デバイスの機能モード」、「アプリケーションと実装」セクション、「電源に関する推奨事項」セクション、「レイアウト」セクション、「デバイスおよびドキュメントのサポート」セクション、「メカニカル、パッケージ、および注文情報」セクションを追加。仕様の変更はなし。 1

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11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser based versions of this data sheet, refer to the left hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LM139AD	Obsolete	Production	SOIC (D) | 14	-	-	Call TI	Call TI	-55 to 125	LM139A
LM139ADG4	Obsolete	Production	SOIC (D) | 14	-	-	Call TI	Call TI	-55 to 125	LM139A
LM139ADR	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	LM139A
LM139ADR.A	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	LM139A
LM139ADRG4	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	LM139A
LM139ADRG4.A	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	LM139A
LM139D	Obsolete	Production	SOIC (D) | 14	-	-	Call TI	Call TI	-55 to 125	LM139
LM139DG4	Obsolete	Production	SOIC (D) | 14	-	-	Call TI	Call TI	-55 to 125	LM139
LM139DR	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	LM139
LM139DR.A	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	LM139
LM139DRG4	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	LM139
LM139DRG4.A	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	LM139
LM239AD	Obsolete	Production	SOIC (D) | 14	-	-	Call TI	Call TI	-25 to 85	LM239A
LM239ADR	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-25 to 85	LM239A
LM239ADR.A	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-25 to 85	LM239A
LM239ADRE4	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	-	Call TI	Call TI	-25 to 85	
LM239ADRG4	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	-	Call TI	Call TI	-25 to 85	
LM239D	Obsolete	Production	SOIC (D) | 14	-	-	Call TI	Call TI	-25 to 85	LM239
LM239DR	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-25 to 85	LM239
LM239DR.A	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-25 to 85	LM239
LM239DRG3	Obsolete	Production	SOIC (D) | 14	-	-	Call TI	Call TI	-25 to 85	LM239
LM239DRG4	Obsolete	Production	SOIC (D) | 14	-	-	Call TI	Call TI	-25 to 85	LM239
LM239N	Active	Production	PDIP (N) | 14	25 | TUBE	Yes	NIPDAU | SN	N/A for Pkg Type	-25 to 85	LM239N
LM239N.A	Active	Production	PDIP (N) | 14	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-25 to 85	LM239N
LM239NE4	Active	Production	PDIP (N) | 14	25 | TUBE	-	Call TI	Call TI	-25 to 85	
LM239PW	Obsolete	Production	TSSOP (PW) | 14	-	-	Call TI	Call TI	-25 to 85	L239
LM239PWR	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-25 to 85	L239
LM239PWR.A	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-25 to 85	L239
LM239PWRG4	Obsolete	Production	TSSOP (PW) | 14	-	-	Call TI	Call TI	-25 to 85	L239

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LM2901AVQDR	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(2901AV, L2901AV)
LM2901AVQDR.A	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(2901AV, L2901AV)
LM2901AVQDRG4	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(2901AV, L2901AV)
LM2901AVQDRG4.A	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(2901AV, L2901AV)
LM2901AVQPWR	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(2901AV, L2901AV)
LM2901AVQPWR.A	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(2901AV, L2901AV)
LM2901AVQPWRG4	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(2901AV, L2901AV)
LM2901AVQPWRG4.A	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(2901AV, L2901AV)
LM2901BIDR	Active	Production	SOIC (D) | 14	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LM2901B
LM2901BIDR.A	Active	Production	SOIC (D) | 14	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LM2901B
LM2901BIPWR	Active	Production	TSSOP (PW) | 14	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LM2901B
LM2901BIPWR.A	Active	Production	TSSOP (PW) | 14	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LM2901B
LM2901BIRTER	Active	Production	WQFN (RTE) | 16	5000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	M2901B
LM2901BIRTER.A	Active	Production	WQFN (RTE) | 16	5000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	M2901B
LM2901D	Obsolete	Production	SOIC (D) | 14	-	-	Call TI	Call TI	-40 to 125	LM2901
LM2901DR	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LM2901
LM2901DR.A	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LM2901
LM2901DRE4	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LM2901
LM2901DRG3	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	LM2901
LM2901DRG3.A	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	LM2901
LM2901DRG4	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LM2901
LM2901DRG4.A	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LM2901
LM2901N	Active	Production	PDIP (N) | 14	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 125	LM2901N
LM2901N.A	Active	Production	PDIP (N) | 14	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 125	LM2901N
LM2901NSR	Active	Production	SOP (NS) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LM2901
LM2901NSR.A	Active	Production	SOP (NS) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LM2901
LM2901PW	Obsolete	Production	TSSOP (PW) | 14	-	-	Call TI	Call TI	-40 to 125	L2901
LM2901PWR	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	L2901
LM2901PWR.A	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	L2901
LM2901PWRG3	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	L2901
LM2901PWRG3.A	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	L2901

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LM2901PWRG4	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	L2901
LM2901PWRG4.A	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	L2901
LM2901VQDR	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	L2901V
LM2901VQDR.A	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	L2901V
LM2901VQPWR	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	L2901V
LM2901VQPWR.A	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	L2901V
LM2901VQPWRG4	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	L2901V
LM2901VQPWRG4.A	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	L2901V
LM339AD	Obsolete	Production	SOIC (D) | 14	-	-	Call TI	Call TI	0 to 70	LM339A
LM339ADBR	Active	Production	SSOP (DB) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	L339A
LM339ADBR.A	Active	Production	SSOP (DB) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	L339A
LM339ADR	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	0 to 70	LM339A
LM339ADR.A	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	LM339A
LM339ADRG4	Obsolete	Production	SOIC (D) | 14	-	-	Call TI	Call TI	0 to 70	LM339A
LM339AN	Active	Production	PDIP (N) | 14	25 | TUBE	Yes	NIPDAU | SN	N/A for Pkg Type	0 to 70	LM339AN
LM339AN.A	Active	Production	PDIP (N) | 14	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	LM339AN
LM339ANE4	Active	Production	PDIP (N) | 14	25 | TUBE	-	Call TI	Call TI	0 to 70	
LM339ANSR	Active	Production	SOP (NS) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	LM339A
LM339ANSR.A	Active	Production	SOP (NS) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	LM339A
LM339APW	Obsolete	Production	TSSOP (PW) | 14	-	-	Call TI	Call TI	0 to 70	L339A
LM339APWR	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	0 to 70	L339A
LM339APWR.A	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	L339A
LM339APWRG4	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	L339A
LM339APWRG4.A	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	L339A
LM339BIDR	Active	Production	SOIC (D) | 14	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LM339B
LM339BIDR.A	Active	Production	SOIC (D) | 14	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LM339B
LM339BIPWR	Active	Production	TSSOP (PW) | 14	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LM339B
LM339BIPWR.A	Active	Production	TSSOP (PW) | 14	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LM339B
LM339BIRTER	Active	Production	WQFN (RTE) | 16	5000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	LM339B
LM339BIRTER.A	Active	Production	WQFN (RTE) | 16	5000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	LM339B
LM339D	Obsolete	Production	SOIC (D) | 14	-	-	Call TI	Call TI	0 to 70	LM339

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LM339DBR	Active	Production	SSOP (DB) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	LM339
LM339DBR.A	Active	Production	SSOP (DB) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	LM339
LM339DR	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	0 to 70	LM339
LM339DR.A	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	LM339
LM339DRE4	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	LM339
LM339DRG3	Obsolete	Production	SOIC (D) | 14	-	-	Call TI	Call TI	0 to 70	LM339
LM339DRG4	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	LM339
LM339DRG4.A	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	LM339
LM339N	Active	Production	PDIP (N) | 14	25 | TUBE	Yes	NIPDAU | SN	N/A for Pkg Type	0 to 70	LM339N
LM339N.A	Active	Production	PDIP (N) | 14	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	LM339N
LM339NE3	Active	Production	PDIP (N) | 14	25 | TUBE	Yes	SN	N/A for Pkg Type	0 to 70	LM339N
LM339NE3.A	Active	Production	PDIP (N) | 14	25 | TUBE	Yes	SN	N/A for Pkg Type	0 to 70	LM339N
LM339NE4	Active	Production	PDIP (N) | 14	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	LM339N
LM339NE4.A	Active	Production	PDIP (N) | 14	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	LM339N
LM339NSR	Active	Production	SOP (NS) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	LM339
LM339NSR.A	Active	Production	SOP (NS) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	LM339
LM339PW	Obsolete	Production	TSSOP (PW) | 14	-	-	Call TI	Call TI	0 to 70	L339
LM339PWR	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	0 to 70	L339
LM339PWR.A	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	L339
LM339PWRE4	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	L339
LM339PWRG3	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	0 to 70	L339
LM339PWRG3.A	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	0 to 70	L339
LM339PWRG4	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	L339
LM339PWRG4.A	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	L339

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF LM139, LM239A, LM2901, LM2901AV, LM2901B, LM2901V :

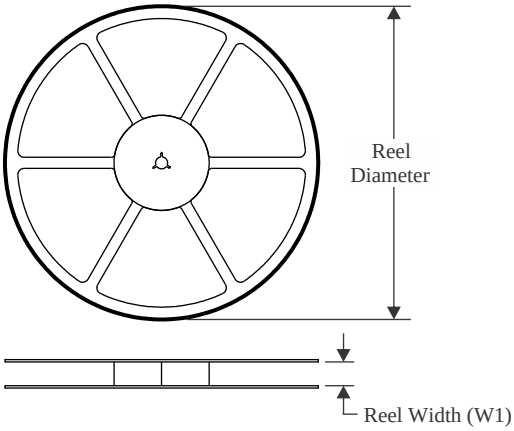
- Automotive : LM239A-Q1, LM2901-Q1, LM2901AV-Q1, LM2901B-Q1, LM2901V-Q1
- Enhanced Product : LM239A-EP
- Space : LM139-SP

NOTE: Qualified Version Definitions:

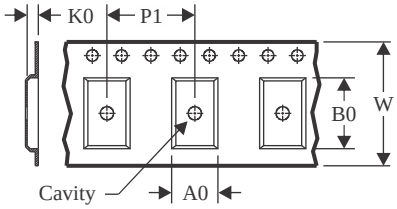
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Enhanced Product - Supports Defense, Aerospace and Medical Applications
- Space - Radiation tolerant, ceramic packaging and qualified for use in Space-based application

TAPE AND REEL INFORMATION

REEL DIMENSIONS

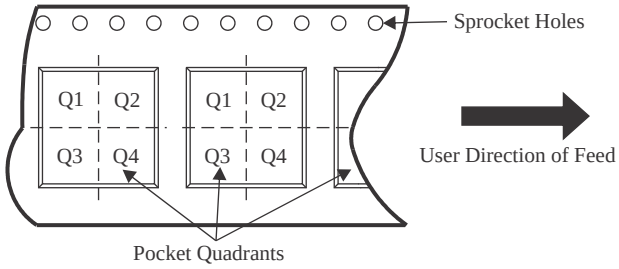


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



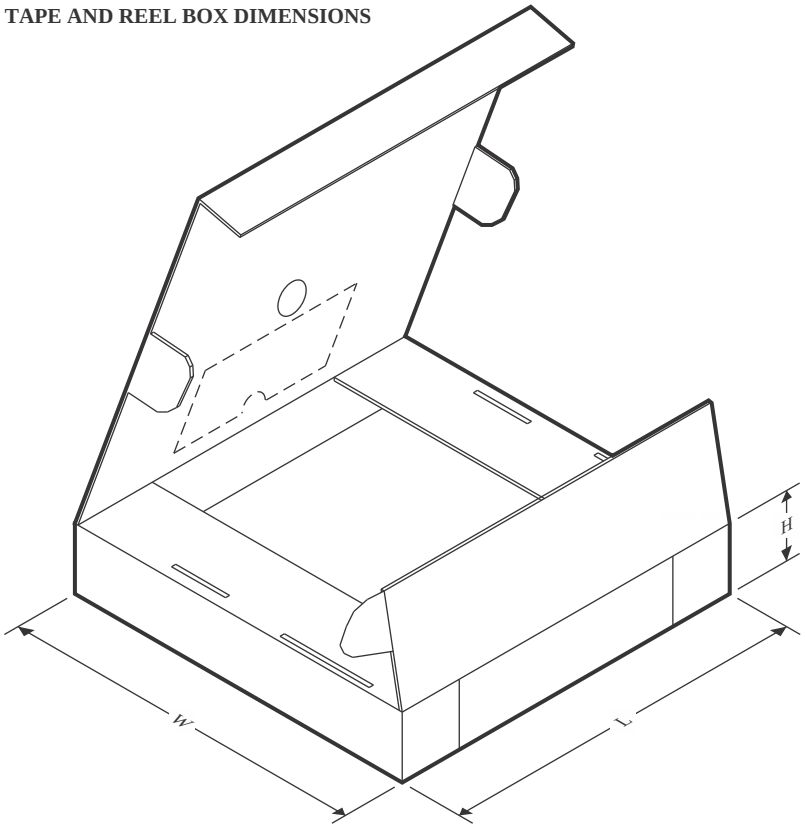
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM139ADR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
LM139ADRG4	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
LM139DR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
LM139DRG4	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
LM239ADR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
LM239DR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
LM239DR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
LM239DR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
LM239PWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
LM239PWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
LM239PWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
LM2901AVQDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
LM2901AVQDRG4	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
LM2901AVQPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
LM2901AVQPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
LM2901AVQPWRG4	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM2901AVQPWRG4	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
LM2901BIDR	SOIC	D	14	3000	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
LM2901BIDR	SOIC	D	14	3000	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
LM2901BIPWR	TSSOP	PW	14	3000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
LM2901BIRTER	WQFN	RTE	16	5000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
LM2901DR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
LM2901DR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
LM2901DRG3	SOIC	D	14	2500	330.0	16.8	6.5	9.5	2.1	8.0	16.0	Q1
LM2901DRG4	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
LM2901DRG4	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
LM2901NSR	SOP	NS	14	2000	330.0	16.4	8.1	10.4	2.5	12.0	16.0	Q1
LM2901PWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
LM2901PWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
LM2901PWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
LM2901PWRG3	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
LM2901PWRG4	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
LM2901PWRG4	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
LM2901VQDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
LM2901VQPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
LM2901VQPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
LM2901VQPWRG4	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
LM2901VQPWRG4	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
LM339ADBR	SSOP	DB	14	2000	330.0	16.4	8.35	6.6	2.4	12.0	16.0	Q1
LM339ADR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
LM339ANSR	SOP	NS	14	2000	330.0	16.4	8.1	10.4	2.5	12.0	16.0	Q1
LM339APWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
LM339APWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
LM339APWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
LM339APWRG4	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
LM339APWRG4	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
LM339BIDR	SOIC	D	14	3000	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
LM339BIDR	SOIC	D	14	3000	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
LM339BIPWR	TSSOP	PW	14	3000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
LM339BIRTER	WQFN	RTE	16	5000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
LM339DBR	SSOP	DB	14	2000	330.0	16.4	8.35	6.6	2.4	12.0	16.0	Q1
LM339DR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
LM339DR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
LM339DRG4	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
LM339DRG4	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
LM339NSR	SOP	NS	14	2000	330.0	16.4	8.1	10.4	2.5	12.0	16.0	Q1
LM339PWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.3	1.6	8.0	12.0	Q1

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM339PWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
LM339PWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
LM339PWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
LM339PWRG3	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
LM339PWRG4	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



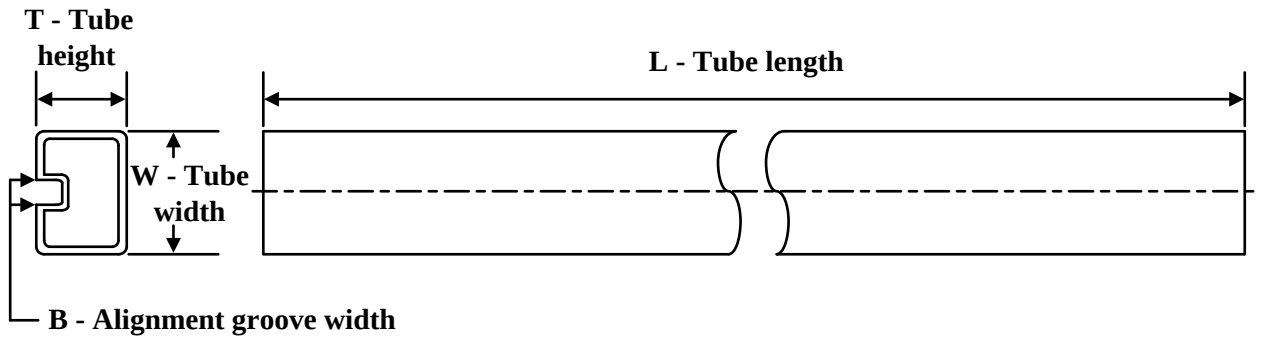
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM139ADR	SOIC	D	14	2500	353.0	353.0	32.0
LM139ADRG4	SOIC	D	14	2500	353.0	353.0	32.0
LM139DR	SOIC	D	14	2500	353.0	353.0	32.0
LM139DRG4	SOIC	D	14	2500	353.0	353.0	32.0
LM239ADR	SOIC	D	14	2500	353.0	353.0	32.0
LM239DR	SOIC	D	14	2500	353.0	353.0	32.0
LM239DR	SOIC	D	14	2500	353.0	353.0	32.0
LM239DR	SOIC	D	14	2500	353.0	353.0	32.0
LM239PWR	TSSOP	PW	14	2000	353.0	353.0	32.0
LM239PWR	TSSOP	PW	14	2000	353.0	353.0	32.0
LM239PWR	TSSOP	PW	14	2000	356.0	356.0	35.0
LM2901AVQDR	SOIC	D	14	2500	353.0	353.0	32.0
LM2901AVQDRG4	SOIC	D	14	2500	353.0	353.0	32.0
LM2901AVQPWR	TSSOP	PW	14	2000	353.0	353.0	32.0
LM2901AVQPWR	TSSOP	PW	14	2000	353.0	353.0	32.0
LM2901AVQPWRG4	TSSOP	PW	14	2000	353.0	353.0	32.0
LM2901AVQPWRG4	TSSOP	PW	14	2000	353.0	353.0	32.0
LM2901BIDR	SOIC	D	14	3000	353.0	353.0	32.0

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM2901BIDR	SOIC	D	14	3000	353.0	353.0	32.0
LM2901BIPWR	TSSOP	PW	14	3000	353.0	353.0	32.0
LM2901BIRTER	WQFN	RTE	16	5000	360.0	360.0	36.0
LM2901DR	SOIC	D	14	2500	353.0	353.0	32.0
LM2901DR	SOIC	D	14	2500	353.0	353.0	32.0
LM2901DRG3	SOIC	D	14	2500	364.0	364.0	27.0
LM2901DRG4	SOIC	D	14	2500	353.0	353.0	32.0
LM2901DRG4	SOIC	D	14	2500	353.0	353.0	32.0
LM2901NSR	SOP	NS	14	2000	353.0	353.0	32.0
LM2901PWR	TSSOP	PW	14	2000	356.0	356.0	35.0
LM2901PWR	TSSOP	PW	14	2000	353.0	353.0	32.0
LM2901PWR	TSSOP	PW	14	2000	353.0	353.0	32.0
LM2901PWRG3	TSSOP	PW	14	2000	364.0	364.0	27.0
LM2901PWRG4	TSSOP	PW	14	2000	353.0	353.0	32.0
LM2901PWRG4	TSSOP	PW	14	2000	353.0	353.0	32.0
LM2901VQDR	SOIC	D	14	2500	353.0	353.0	32.0
LM2901VQPWR	TSSOP	PW	14	2000	353.0	353.0	32.0
LM2901VQPWR	TSSOP	PW	14	2000	353.0	353.0	32.0
LM2901VQPWRG4	TSSOP	PW	14	2000	353.0	353.0	32.0
LM2901VQPWRG4	TSSOP	PW	14	2000	353.0	353.0	32.0
LM339ADBR	SSOP	DB	14	2000	353.0	353.0	32.0
LM339ADR	SOIC	D	14	2500	353.0	353.0	32.0
LM339ANSR	SOP	NS	14	2000	353.0	353.0	32.0
LM339APWR	TSSOP	PW	14	2000	353.0	353.0	32.0
LM339APWR	TSSOP	PW	14	2000	353.0	353.0	32.0
LM339APWR	TSSOP	PW	14	2000	356.0	356.0	35.0
LM339APWRG4	TSSOP	PW	14	2000	353.0	353.0	32.0
LM339APWRG4	TSSOP	PW	14	2000	353.0	353.0	32.0
LM339BIDR	SOIC	D	14	3000	353.0	353.0	32.0
LM339BIDR	SOIC	D	14	3000	353.0	353.0	32.0
LM339BIPWR	TSSOP	PW	14	3000	353.0	353.0	32.0
LM339BIRTER	WQFN	RTE	16	5000	360.0	360.0	36.0
LM339DBR	SSOP	DB	14	2000	353.0	353.0	32.0
LM339DR	SOIC	D	14	2500	353.0	353.0	32.0
LM339DR	SOIC	D	14	2500	353.0	353.0	32.0
LM339DRG4	SOIC	D	14	2500	353.0	353.0	32.0
LM339DRG4	SOIC	D	14	2500	353.0	353.0	32.0
LM339NSR	SOP	NS	14	2000	353.0	353.0	32.0
LM339PWR	TSSOP	PW	14	2000	367.0	367.0	35.0
LM339PWR	TSSOP	PW	14	2000	353.0	353.0	32.0
LM339PWR	TSSOP	PW	14	2000	356.0	356.0	35.0
LM339PWR	TSSOP	PW	14	2000	353.0	353.0	32.0
LM339PWRG3	TSSOP	PW	14	2000	364.0	364.0	27.0

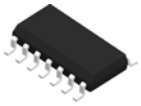
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM339PWRG4	TSSOP	PW	14	2000	353.0	353.0	32.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
LM239N	N	PDIP	14	25	506.1	9	600	5.4
LM239N	N	PDIP	14	25	506	13.97	11230	4.32
LM239N	N	PDIP	14	25	506	13.97	11230	4.32
LM239N.A	N	PDIP	14	25	506	13.97	11230	4.32
LM239N.A	N	PDIP	14	25	506.1	9	600	5.4
LM239N.A	N	PDIP	14	25	506	13.97	11230	4.32
LM2901N	N	PDIP	14	25	506	13.97	11230	4.32
LM2901N	N	PDIP	14	25	506	13.97	11230	4.32
LM2901N.A	N	PDIP	14	25	506	13.97	11230	4.32
LM2901N.A	N	PDIP	14	25	506	13.97	11230	4.32
LM339AN	N	PDIP	14	25	506	13.97	11230	4.32
LM339AN	N	PDIP	14	25	506.1	9	600	5.4
LM339AN	N	PDIP	14	25	506	13.97	11230	4.32
LM339AN.A	N	PDIP	14	25	506	13.97	11230	4.32
LM339AN.A	N	PDIP	14	25	506	13.97	11230	4.32
LM339AN.A	N	PDIP	14	25	506.1	9	600	5.4
LM339N	N	PDIP	14	25	506	13.97	11230	4.32
LM339N	N	PDIP	14	25	506	13.97	11230	4.32
LM339N	N	PDIP	14	25	506.1	9	600	5.4
LM339N.A	N	PDIP	14	25	506	13.97	11230	4.32
LM339N.A	N	PDIP	14	25	506	13.97	11230	4.32
LM339N.A	N	PDIP	14	25	506.1	9	600	5.4
LM339NE3	N	PDIP	14	25	506.1	9	600	5.4
LM339NE3.A	N	PDIP	14	25	506.1	9	600	5.4
LM339NE4	N	PDIP	14	25	506	13.97	11230	4.32
LM339NE4	N	PDIP	14	25	506	13.97	11230	4.32
LM339NE4.A	N	PDIP	14	25	506	13.97	11230	4.32
LM339NE4.A	N	PDIP	14	25	506	13.97	11230	4.32

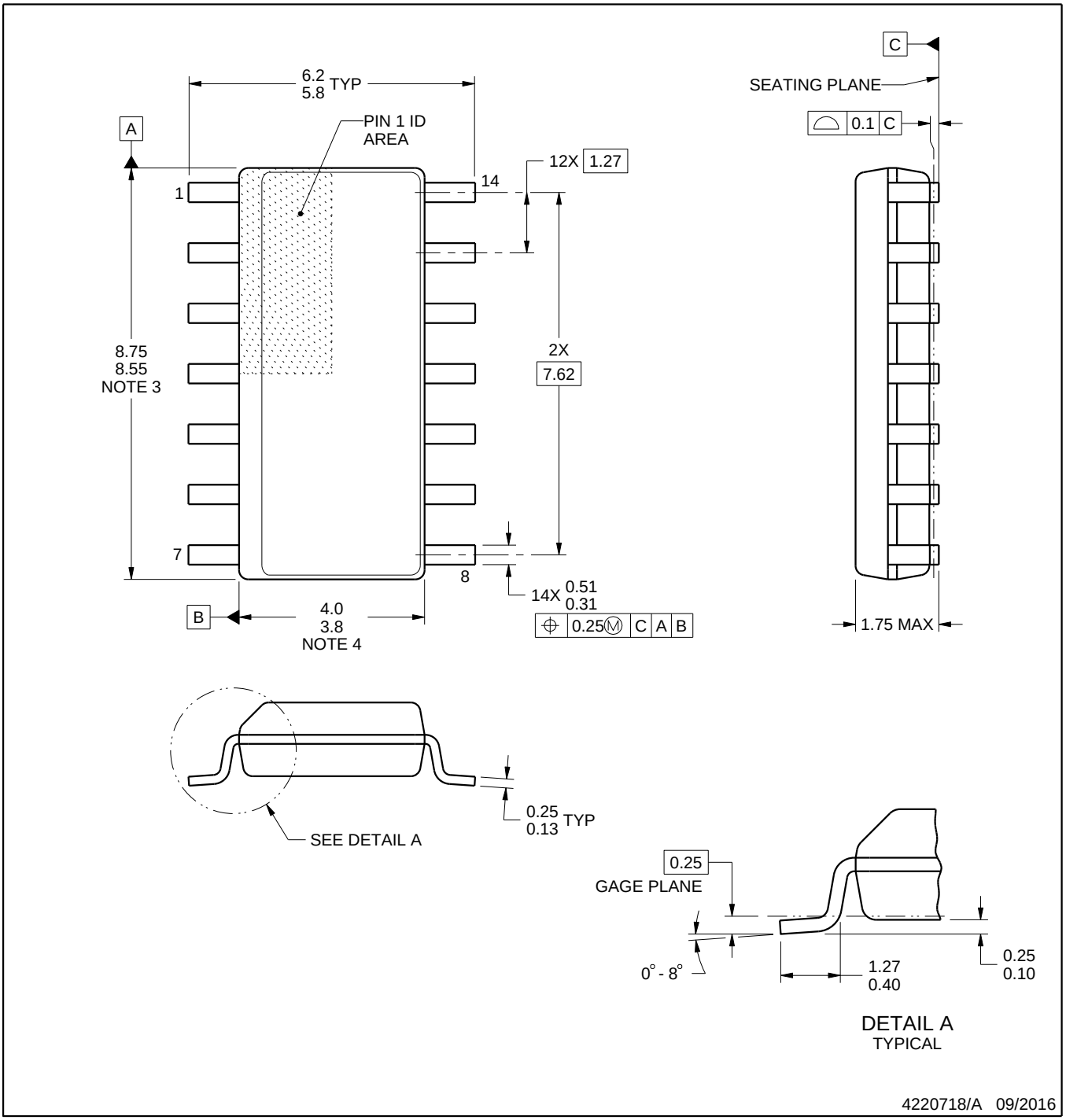


PACKAGE OUTLINE

D0014A

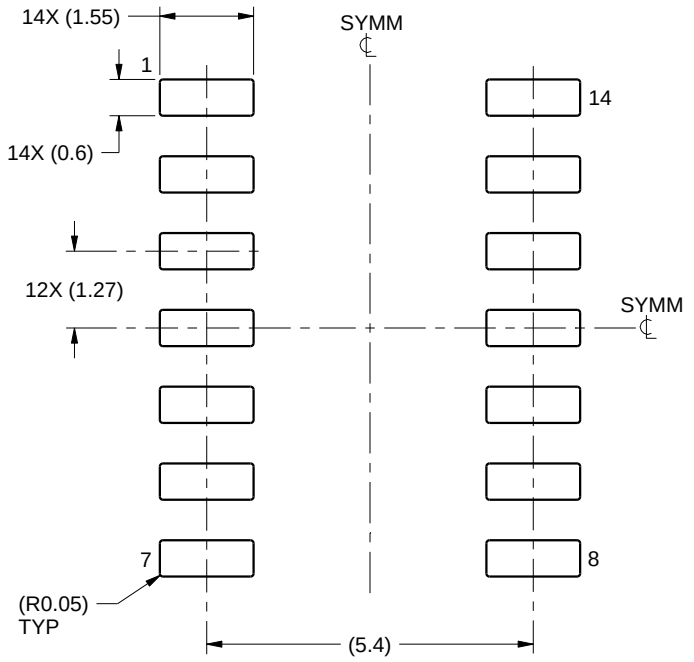
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

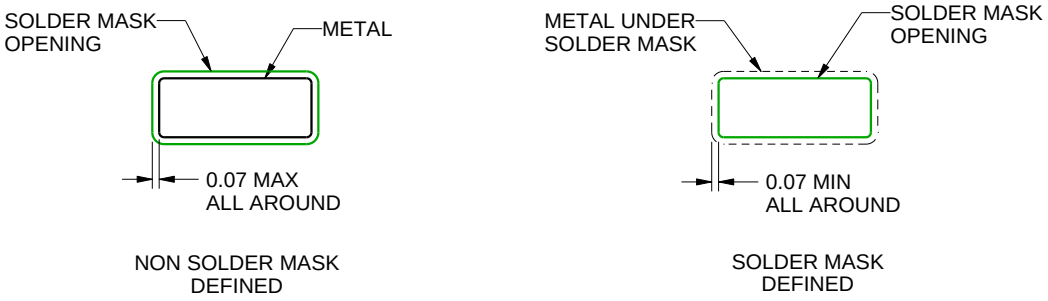


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.



LAND PATTERN EXAMPLE
SCALE:8X



SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

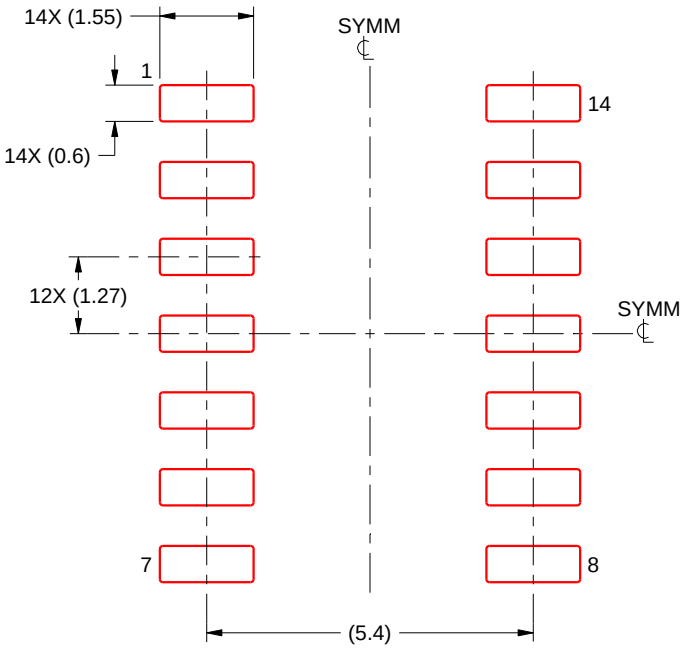
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

4220718/A 09/2016

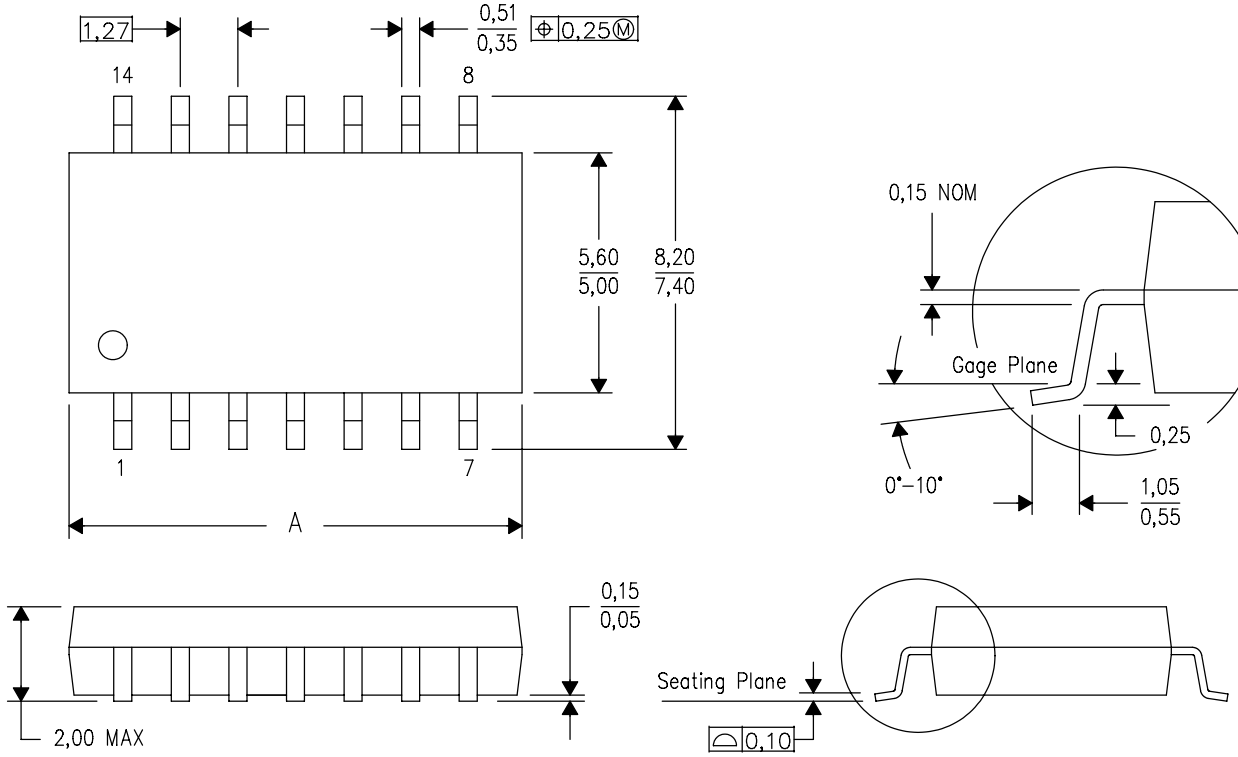
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

MECHANICAL DATA

NS (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14-PINS SHOWN



DIM \ PINS **	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

4040062/C 03/03

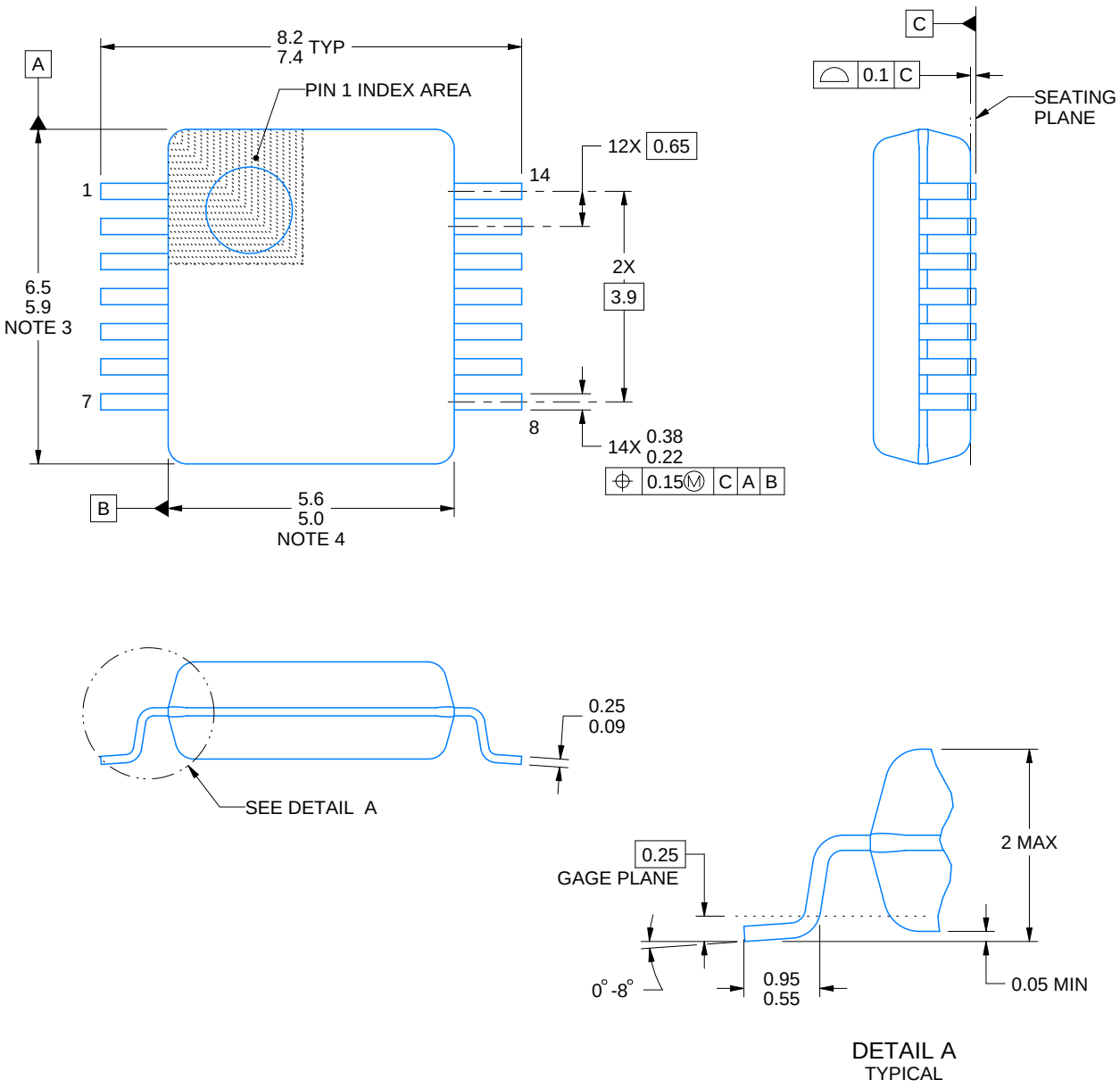
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

PACKAGE OUTLINE

DB0014A

SSOP - 2 mm max height

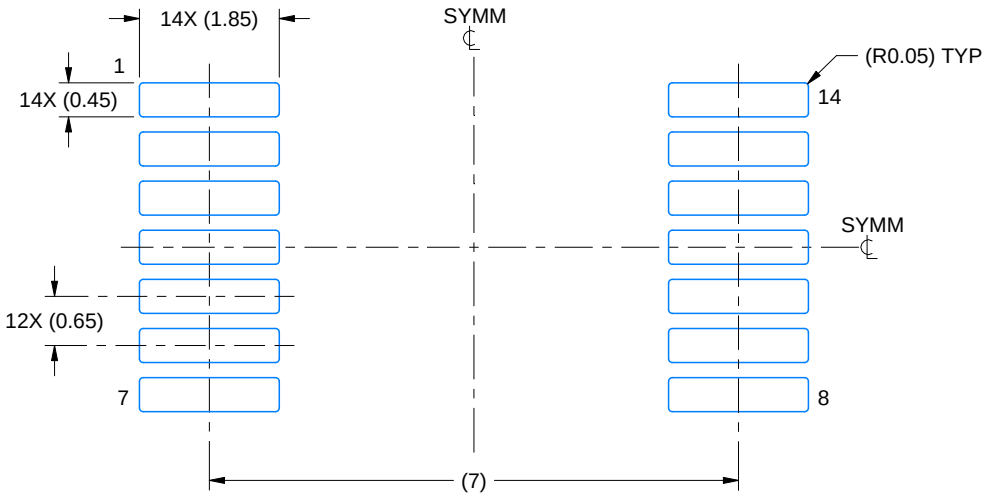
SMALL OUTLINE PACKAGE



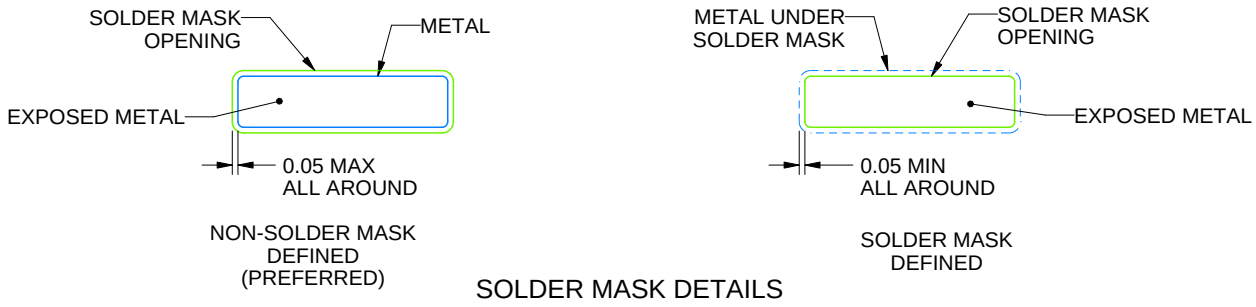
4220762/A 05/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-150.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

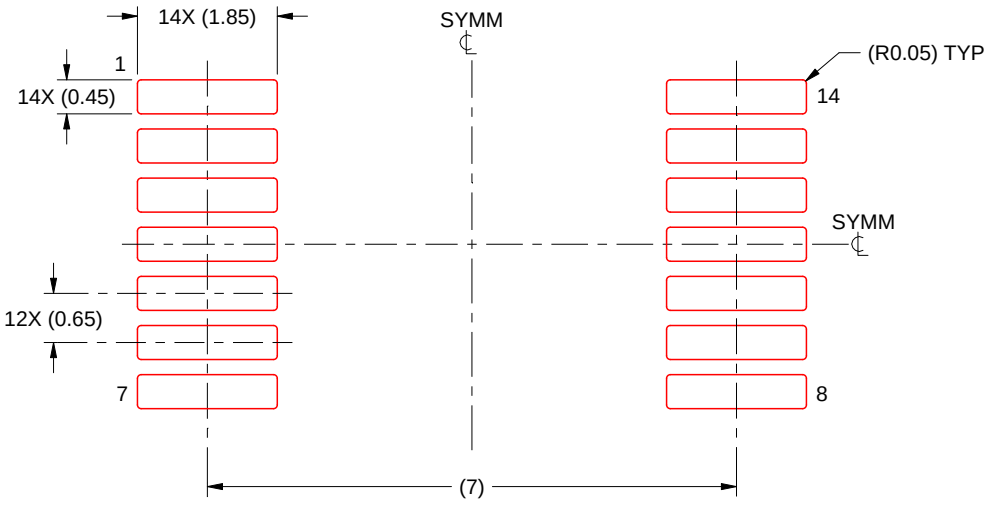


SOLDER MASK DETAILS

4220762/A 05/2024

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220762/A 05/2024

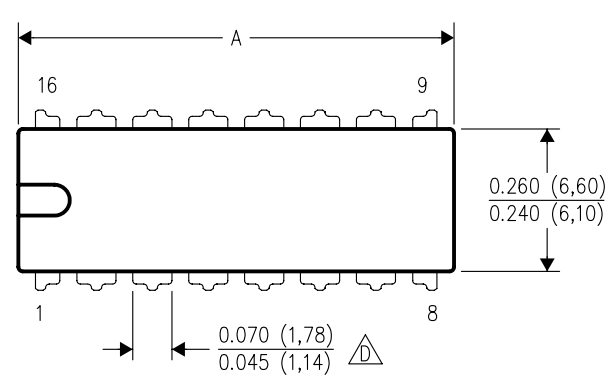
NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

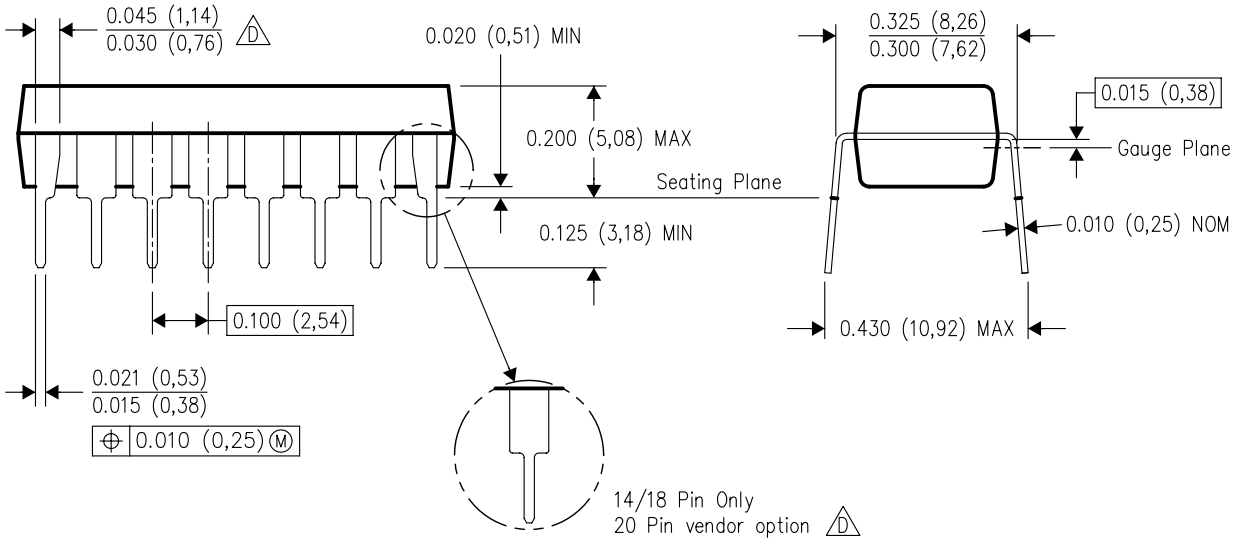
N (R–PDIP–T**)

PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN



DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD



4040049/E 12/2002

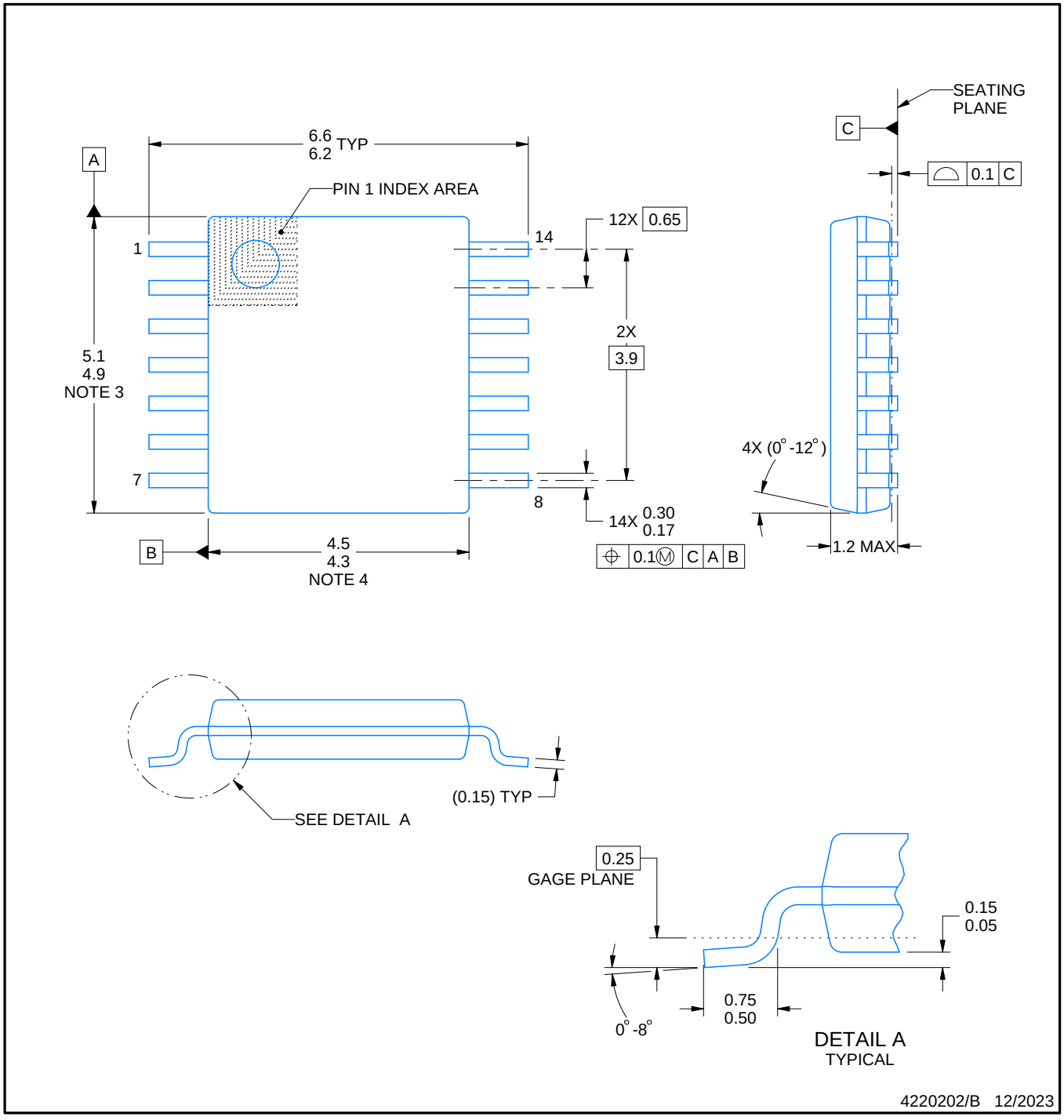
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

PACKAGE OUTLINE

PW0014A

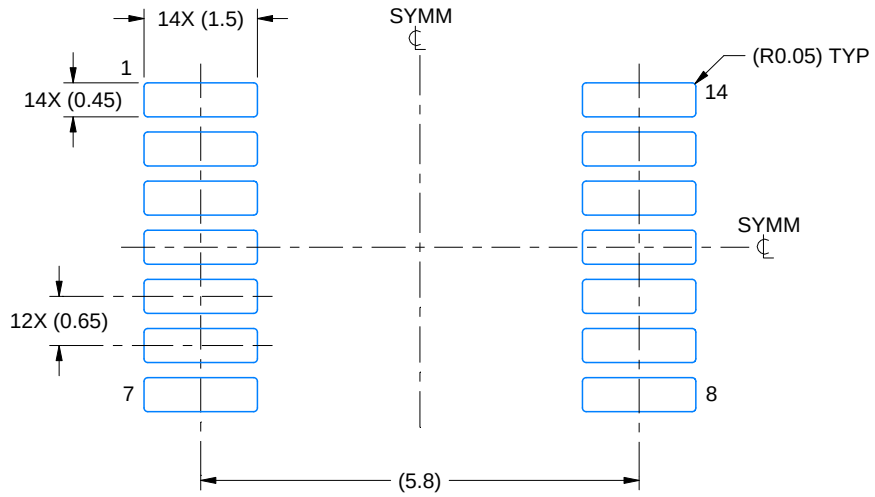
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

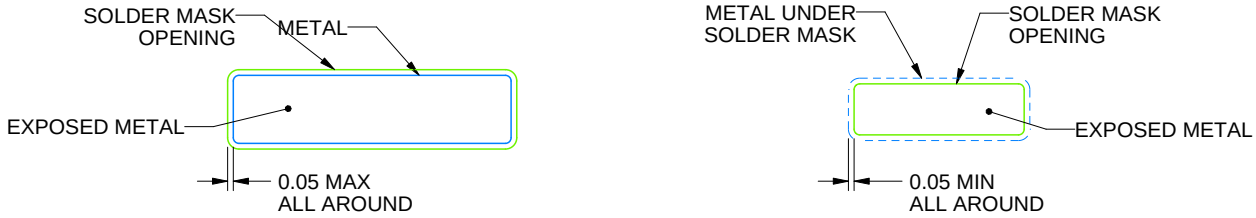


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

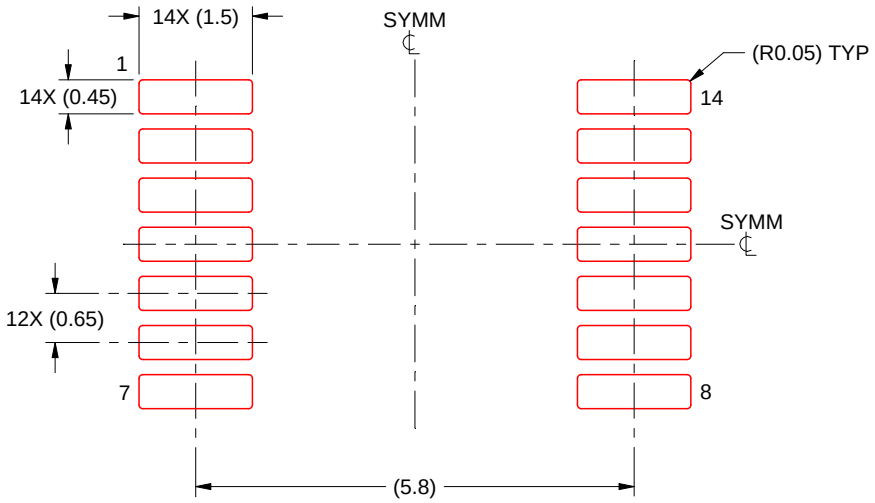


SOLDER MASK DETAILS

4220202/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220202/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

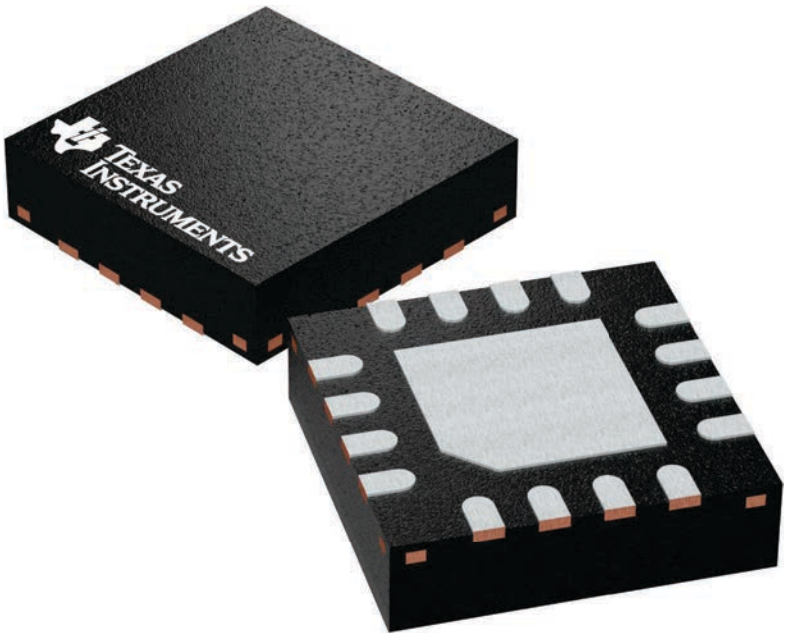
RTE 16

WQFN - 0.8 mm max height

3 x 3, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

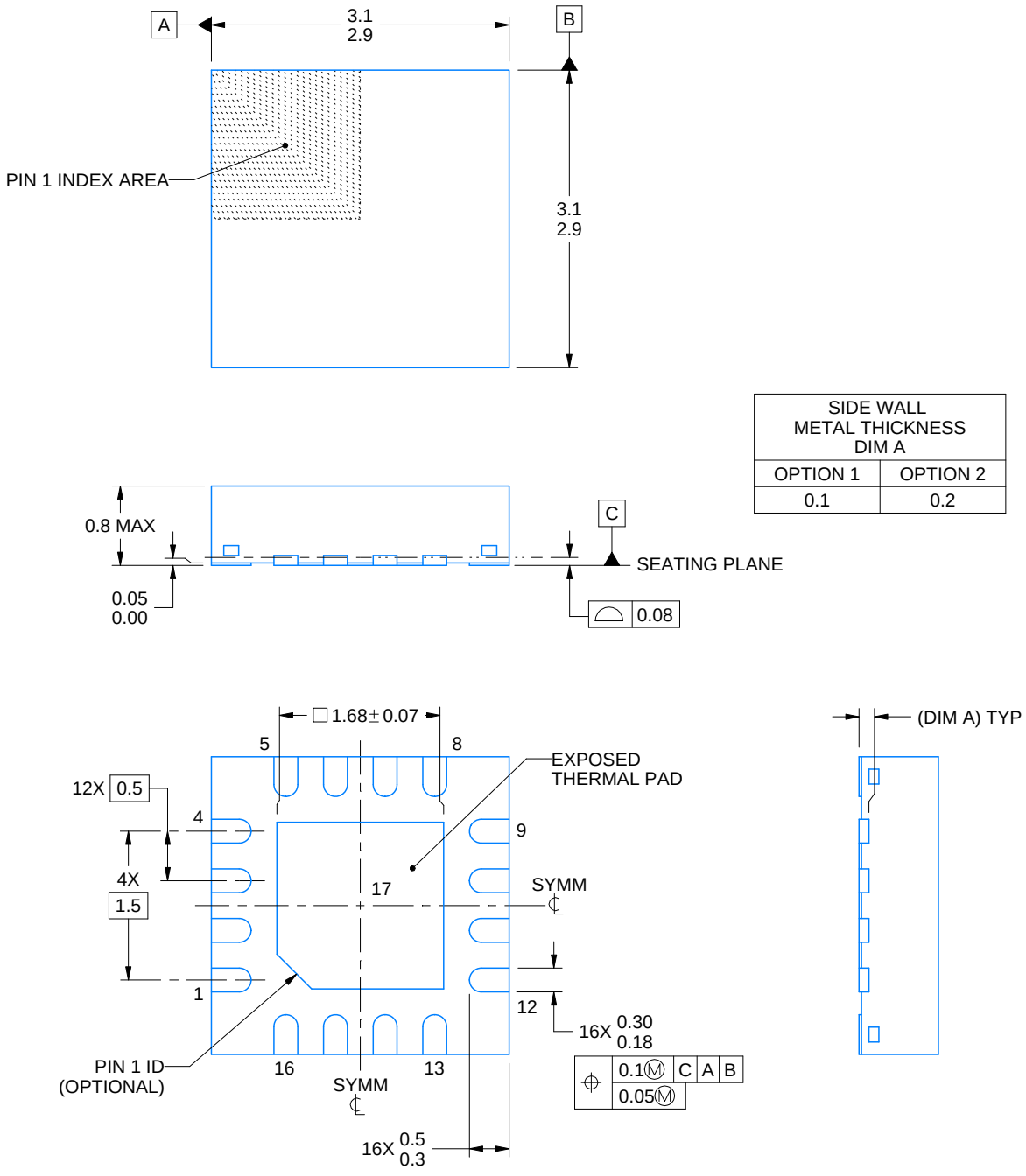


RTE0016C

PACKAGE OUTLINE

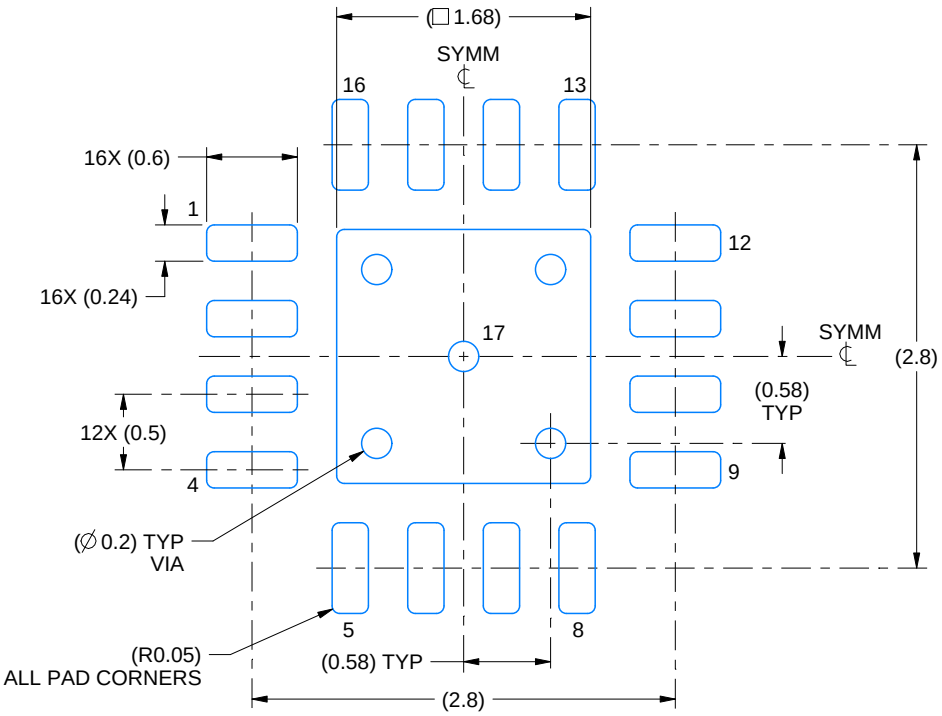
WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

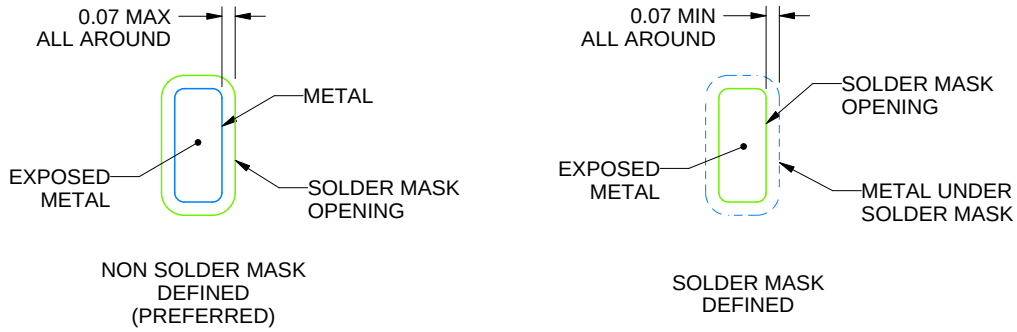


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X

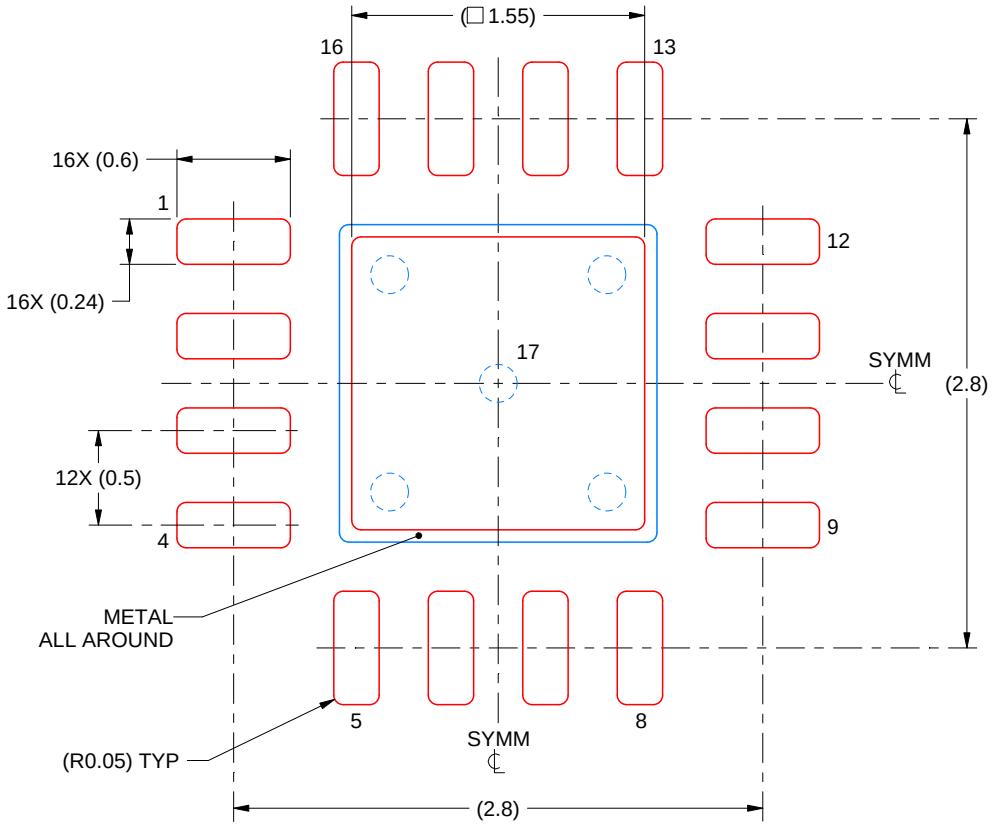


SOLDER MASK DETAILS

4219117/B 04/2022

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 17:
85% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:25X

4219117/B 04/2022

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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最終更新日：2025 年 10 月