LM21212-2 周波数可変の 2.95V～5.5V、12A の電圧モード同期整流降圧レギュレータ

1 特長

- 7mΩ ハイサイドおよび 4.3mΩ ローサイドの FET スイッチを内蔵
- 周波数を 300kHz～1.55MHz の範囲で抵抗により変更可能
- 出力電圧を 0.6V～V_{IN} の範囲で変更可能 (100% デューティ・サイクルが可能)、±1% の基準電圧
- 入力電圧範囲: 2.95V～5.5V
- プリバイアス負荷へのスタートアップ
- 出力電圧トラッキング機能
- 広い帯域幅の電圧ループ誤差アンプ
- 外付けコンデンサにより可変のソフトスタート
- ヒステリシス付きの高精度イネーブル・ピン
- OVP、OCP、OTP、UVLO、パワー・グッドを搭載
- 熱的に強化された 20 ピン HTSSOP 露出パッド・パッケージ
- WEBENCH® Power Designer により、LM21212-2 を使用するカスタム設計を作成

2 アプリケーション

- ブロードバンド、ネットワーク、およびワイヤレス通信
- 高性能の FPGA、ASIC、マイクロプロセッサ
- 5V または 3.3V のバスから高効率のポイント・オブ・ロード・レギュレーションを簡単に設計可能

3 概要

LM21212-2 はモノリシックな同期整流降圧レギュレータで、非常に優れた効率で最低 0.6V の出力電圧を生成し、最大 12A の連続出力電流を供給できます。このデバイスは 2.95V～5.5V の入力電圧範囲で動作するよう最適化されており、広範な低電圧システムに適しています。電圧モード制御ループによりノイズ耐性が高く、狭いデューティ・サイクルが可能で、あらゆる種類の出力容量による補償で安定するため、最大の柔軟性を持ち、簡単に使用できます。

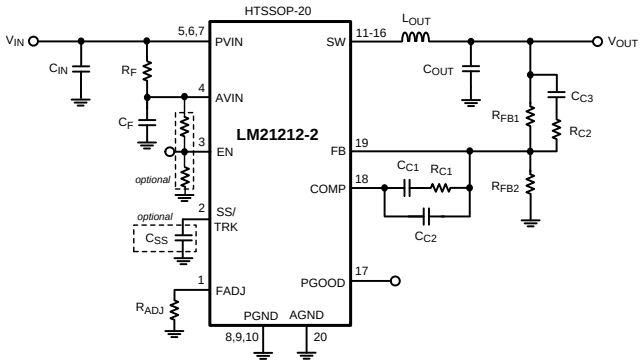
LM21212-2 には、過電圧保護 (OVP) および過電流保護 (OCP) 機能が内蔵され、システムの高い信頼性を実現しています。高精度のイネーブル・ピンと内蔵の UVLO により、デバイスの電源オンを厳格に制御し、シーケンシングできます。スタートアップ時の突入電流は、内部的に固定および外部で設定可能なソフトスタート回路により制限されます。内蔵のパワー・グッド回路により、フォルト検出と電源シーケンシングが可能です。

製品情報(1)

型番	パッケージ	本体サイズ (公称)
LM21212-2	HTSSOP (20)	6.50mm×4.40mm

(1) 提供されているすべてのパッケージについては、巻末の注文情報を参照してください。

アプリケーションの簡略回路図



目次

4 改訂履歴

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Revision A (March 2013) から Revision B に変更 **Page**

- 編集上の変更のみ、技術上の変更なし、WEBENCH へのリンクを追加 ... 1

2013年3月発行のものから更新 **Page**

- Changed layout of National Semiconductor data sheet to TI format ... 4

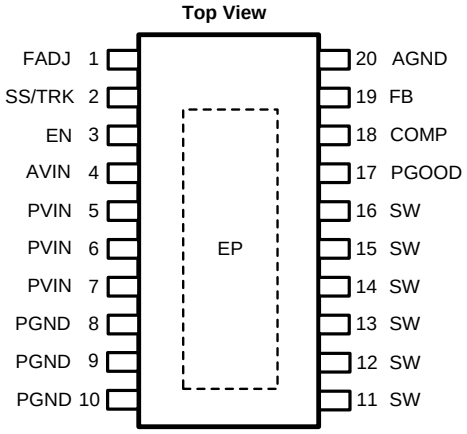
5 概要(続き)

LM21212-2 は、マルチレールの電源アーキテクチャで適切に動作するよう設計されています。デバイスの出力電圧は、SS/TRK ピンを使用して、外部電圧レールを追跡するように構成可能です。スイッチング周波数は、外付けの抵抗を使用して 300kHz～1.55MHz の範囲にプログラムできます。

スタートアップ時に出力がプリバイアスされている場合、電流がシンクされず、出力はプリバイアスされた電圧を超えてスムーズに上昇できます。このレギュレータは 20 ピンの HTSSOP パッケージで供給され、付属の露出パッドを PCB にハンダ付け可能なため、大きなヒートシンクが必要ありません。

6 Pin Configuration and Functions

PWP Package
20-Pin HTSSOP Package
Top View



Pin Descriptions

PIN		
NO.	**NAME**	**Description**
1	FADJ	Frequency Adjust pin. The switching frequency can be set to a predetermined rate by connecting a resistor between FADJ and AGND.
2	SS/TRK	Soft-start control pin. An internal 2 µA current source charges an external capacitor connected between this pin and AGND to set the output voltage ramp rate during startup. This pin can also be used to configure the tracking feature.
3	EN	Active high enable input for the device. If not used, the EN pin can be left open, which will go high due to an internal current source.
4	AVIN	Analog input voltage supply that generates the internal bias. It is recommended to connect PVIN to AVIN through a low pass RC filter to minimize the influence of input rail ripple and noise on the analog control circuitry.
5,6,7	PVIN	Input voltage to the power switches inside the device. These pins should be connected together at the device. A low ESR input capacitance should be located as close as possible to these pins.
8,9,10	PGND	Power ground pins for the internal power switches.
11-16	SW	Switch node pins. These pins should be tied together locally and connected to the filter inductor.
17	PGOOD	Open-drain power good indicator.
18	COMP	Compensation pin is connected to the output of the voltage loop error amplifier.
19	FB	Feedback pin is connected to the inverting input of the voltage loop error amplifier.
20	AGND	Quiet analog ground for the internal reference and bias circuitry.
EP	Exposed Pad	Exposed metal pad on the underside of the package with an electrical and thermal connection to PGND. It is recommended to connect this pad to the PC board ground plane in order to improve thermal dissipation.

7 Specifications

7.1 Absolute Maximum Ratings

See (1)(2)

PVIN(3), AVIN to GND	−0.3V to +6V
SW(4), EN, FB, COMP, PGOOD, SS/TRK, FADJ to GND	−0.3V to PVIN + 0.3V
Storage Temperature	−65°C to 150°C
Soldering Specification for TSSOP Pb-Free Infrared or Convection (30 sec)	260°C

(1) Absolute Maximum Ratings indicate limits beyond witch damage to the device may occur. Recommended operating ratings indicate conditions for which the device is intended to be functional, but do not ensure specific performance limits. For ensured specifications and test conditions, see the *Electrical Characteristics*.
(2) If Military/Aerospace specified devices are required, contact the Texas Instruments Sales Office/Distributors for availability and specifications.
(3) The PVIN pin can tolerate transient voltages up to 6.5 V for a period of up to 6ns. These transients can occur during the normal operation of the device.
(4) The SW pin can tolerate transient voltages up to 9 V for a period of up to 6 ns, and -1 V for a duration of 4 ns. These transients can occur during the normal operation of the device.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Ratings

PVIN, AVIN to GND	+2.95V to +5.5V
Junction Temperature	−40°C to +125°C
θ_{JA}(1)	24°C/W

(1) Thermal measurements were performed on a 2x2 inch, 4 layer, 2 oz. copper outer layer, 1 oz.copper inner layer board with twelve 8 mil. vias underneath the EP of the device and an additional sixteen 8 mil. vias under the unexposed package.

7.4 Electrical Characteristics

Unless otherwise stated, the following conditions apply: $V_{PVIN,\ AVIN}$ = 5V. Limits in standard type are for T_J = 25°C only, limits in **boldface type** apply over the junction temperature (T_J) range of −40°C to +125°C. Minimum and maximum limits are specified through test, design, or statistical correlation. Typical values represent the most likely parametric norm at T_J = 25°C, and are provided for reference purposes only.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SYSTEM						
V_{FB}	Feedback pin voltage	V_{IN} = 2.95V to 5.5V	**-1%**	0.6	**1%**	V
$\Delta V_{OUT}/\Delta I_{OUT}$	Load Regulation			0.02		$\%V_{OUT}$/A
$\Delta V_{OUT}/\Delta V_{IN}$	Line Regulation			0.1		$\%V_{OUT}$/V
$R_{DSON\ HS}$	High Side Switch On Resistance	I_{SW} = 12A		7.0	**9.0**	mΩ
$R_{DSON\ LS}$	Low Side Switch On Resistance	I_{SW} = 12A		4.3	**6.0**	mΩ
I_{CLR}	HS Rising Switch Current Limit		**15**	17	**19**	A
I_{CLF}	LS Falling Switch Current Limit			12		A
V_{ZX}	Zero Cross Voltage		-8	3	12	mV
I_Q	Operating Quiescent Current			1.5	**3**.0	mA
I_{SD}	Shutdown Quiescent Current	V_{EN} = 0V		50	**70**	µA
V_{UVLO}	AVIN Undervoltage Lockout	AVIN Rising	**2.45**	2.70	**2.95**	V
$V_{UVLOHYS}$	AVIN Undervoltage Lockout Hysteresis		**140**	200	**280**	mV
$V_{TRACKOS}$	SS/TRACK PIN accuracy (V_{SS} - V_{FB})	0 < V_{TRACK} < 0.55V	**-10**	6	**20**	mV
I_{SS}	Soft-Start Pin Source Current		**1.3**	1.9	**2.5**	µA

Electrical Characteristics (continued)

Unless otherwise stated, the following conditions apply: $V_{PVIN, AVIN}$ = 5V. Limits in standard type are for T_J = 25°C only, limits in **boldface type** apply over the junction temperature (T_J) range of −40°C to +125°C. Minimum and maximum limits are specified through test, design, or statistical correlation. Typical values represent the most likely parametric norm at T_J = 25°C, and are provided for reference purposes only.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{INTSS}	Internal Soft-Start Ramp to Vref	C_{SS} = 0	**350**	500	**675**	µs
$t_{RESETSS}$	Device Reset to Soft-Start Ramp		**50**	110	**200**	µs
OSCILLATOR						
f_{RNG}	FADJ Frequency Range		**300**		**1550**	kHz
f_{SW}	Switching Frequency	R_{ADJ} = 22.6kΩ	**1400**	1550	**1700**	kHz
		R_{ADJ} = 95.3kΩ	**465**	500	**535**	
$t_{HSBLANK}$	HS OCP Blanking Time	Rising edge of SW to I_{CLR} comparison		55		ns
$t_{LSBLANK}$	LS OCP Blanking Time	Falling edge of SW to I_{CLF} comparison		400		ns
$t_{ZXBLANK}$	Zero Cross Blanking Time	Falling edge of SW to V_{ZX} comparison		120		ns
t_{MINON}	Minimum HS on-time			140		ns
ΔVramp	PWM Ramp p-p Voltage			0.8		V
ERROR AMPLIFIER						
V_{OL}	Error Amplifier Open Loop Voltage Gain	ICOMP = -65µA to 1mA		95		dBV/V
GBW	Error Amplifier Gain-Bandwidth Product			11		MHz
I_{FB}	Feedback Pin Bias Current	V_{FB} = 0.6V		1		nA
$I_{COMPSRC}$	COMP Output Source Current			1		mA
$I_{COMPSINK}$	COMP Output Sink Current			65		µA
POWERGOOD						
V_{OVP}	Overvoltage Protection Rising Threshold	V_{FB} Rising	**105**	112.5	**120**	$\%V_{FB}$
V_{OVPHYS}	Overvoltage Protection Hysteresis	V_{FB} Falling		2		$\%V_{FB}$
V_{UVP}	Undervoltage Protection Rising Threshold	V_{FB} Rising	**82**	90	**97**	$\%V_{FB}$
V_{UVPHYS}	Undervoltage Protection Hysteresis	V_{FB} Falling		2.5		$\%V_{FB}$
t_{PGDGL}	PGOOD Deglitch Low (OVP/UVP Condition Duration to PGOOD Falling)			15		µs
t_{PGDGH}	PGOOD Deglitch High (minimum low pulse)			12		µs
R_{PGOOD}	PGOOD Pulldown Resistance		**10**	20	**40**	Ω
$I_{PGOODLEAK}$	PGOOD Leakage Current	V_{PGOOD} = 5V		1		nA
LOGIC						
V_{IHSYNC}	SYNC Pin Logic High		2.0			V
V_{ILSYNC}	SYNC Pin Logic Low				0.8	V
V_{IHENR}	EN Pin Rising Threshold	V_{EN} Rising	**1.20**	1.35	**1.45**	V
V_{ENHYS}	EN Pin Hysteresis		**50**	110	**180**	mV
I_{EN}	EN Pin Pullup Current	V_{EN} = 0V		2		µA
THERMAL SHUTDOWN						
$T_{THERMSD}$	Thermal Shutdown			165		°C
$T_{THERMSDHYS}$	Thermal Shutdown Hysteresis			10		°C

7.5 Typical Characteristics

Unless otherwise specified: V_{VIN} = 5 V, V_{OUT} = 1.2 V, L= 0.56 µH (1.8-mΩ R_{DCR}), C_{SS} = 33 nF, f_{SW} = 500 kHz (R_{ADJ}= 95.3 kΩ), T_A = 25°C for efficiency curves, loop gain plots and waveforms, and T_J = 25°C for all others.

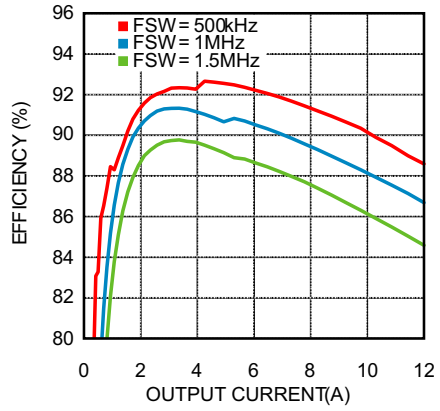


Figure 1. Efficiency

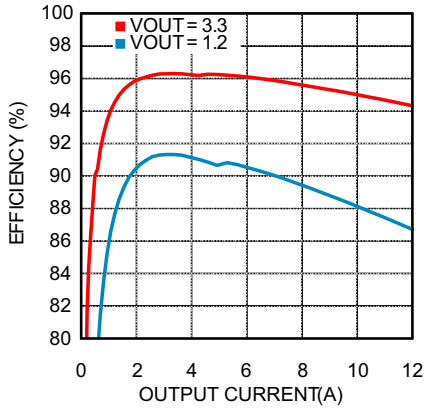


Figure 2. Efficiency

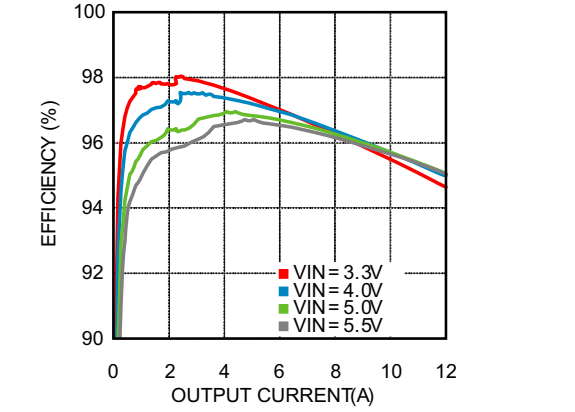


Figure 3. Efficiency

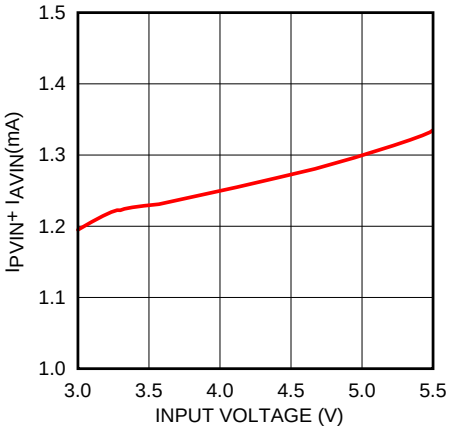


Figure 4. Non-Switching I_{QTOTAL} vs V_{IN}

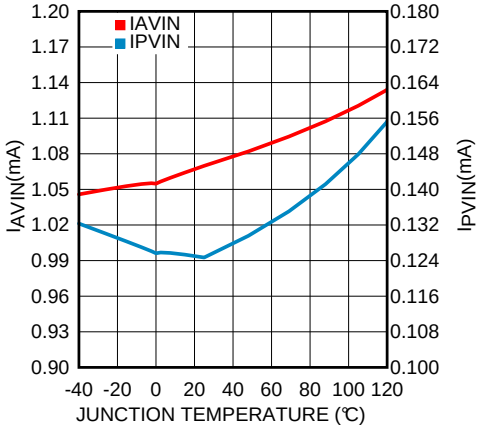


Figure 5. Non-Switching I_{AVIN} and I_{PVIN} vs Temperature

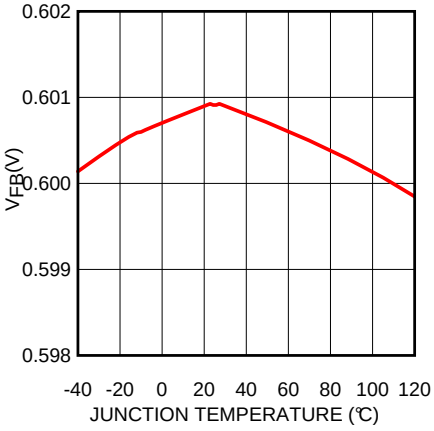


Figure 6. V_{FB} vs Temperature

Typical Characteristics (continued)

Unless otherwise specified: V_{VIN} = 5 V, V_{OUT} = 1.2 V, L= 0.56 µH (1.8-mΩ R_{DCR}), C_{SS} = 33 nF, f_{SW} = 500 kHz (R_{ADJ}= 95.3 kΩ), T_A = 25°C for efficiency curves, loop gain plots and waveforms, and T_J = 25°C for all others.

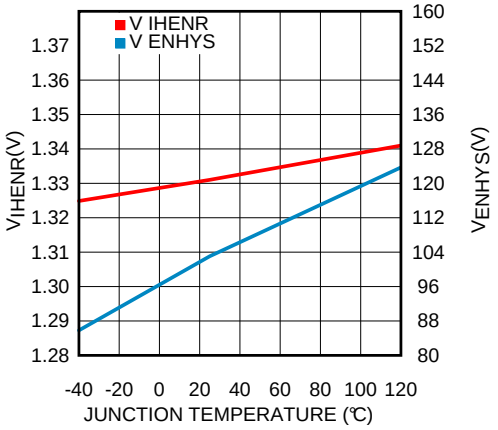


Figure 7. Enable Threshold and Hysteresis vs Temperature

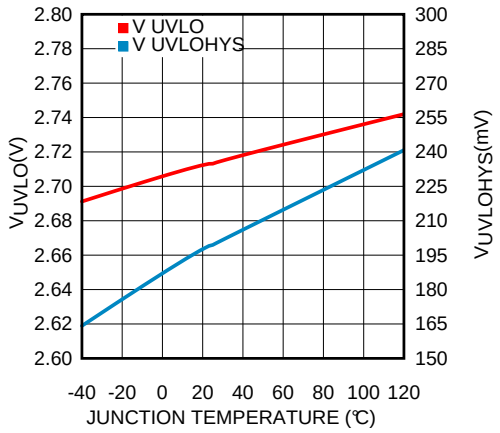


Figure 8. UVLO Threshold and Hysteresis vs Temperature

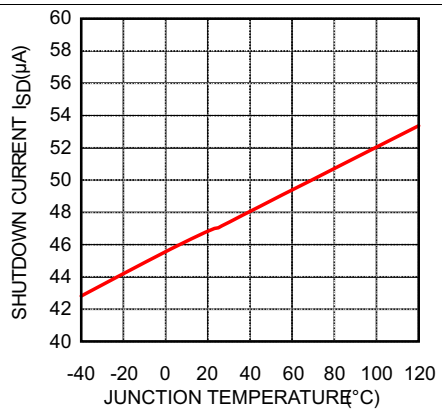


Figure 9. Enable Low Current vs Temperature

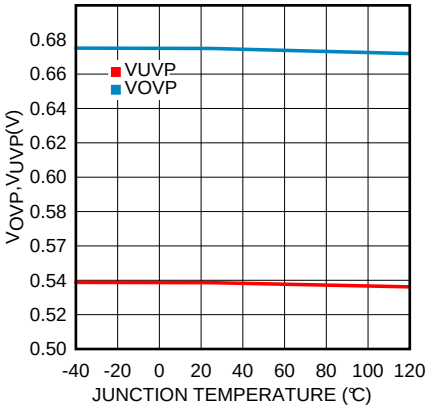


Figure 10. OVP/UVP Threshold vs Temperature

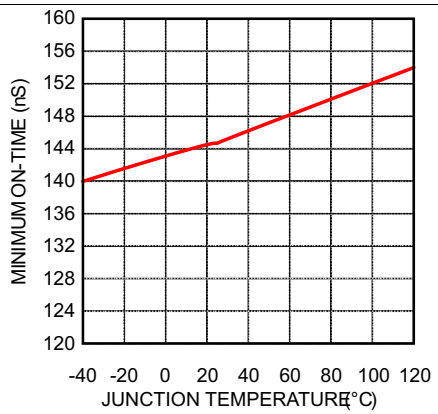


Figure 11. Minimum On-Time vs Temperature

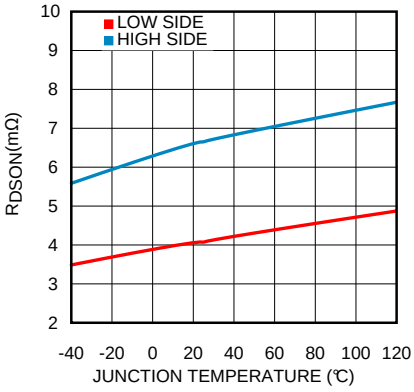


Figure 12. FET Resistance vs Temperature

Typical Characteristics (continued)

Unless otherwise specified: V_{VIN} = 5 V, V_{OUT} = 1.2 V, L= 0.56 µH (1.8-mΩ R_{DCR}), C_{SS} = 33 nF, f_{SW} = 500 kHz (R_{ADJ}= 95.3 kΩ), T_A = 25°C for efficiency curves, loop gain plots and waveforms, and T_J = 25°C for all others.

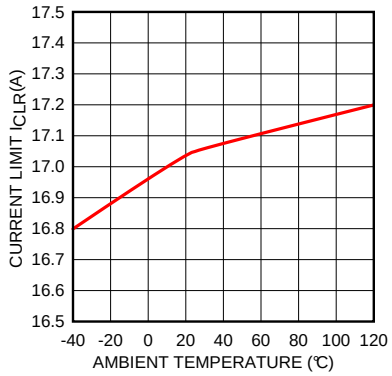


Figure 13. Peak Current Limit vs Temperature

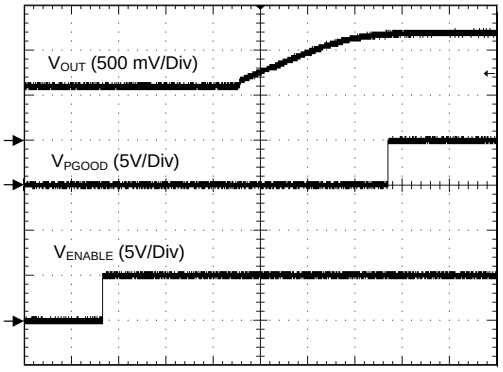


Figure 14. Start-up With Prebiased Output

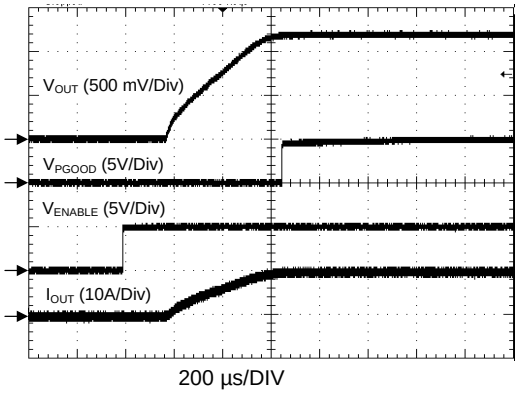


Figure 15. Start-up With SS/TRK Open Circuit

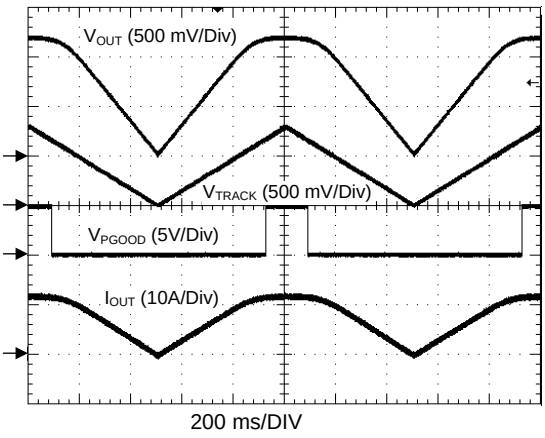


Figure 16. Start-up With Applied Track Signal

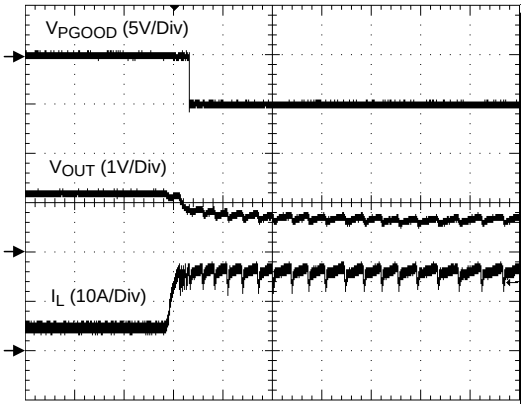


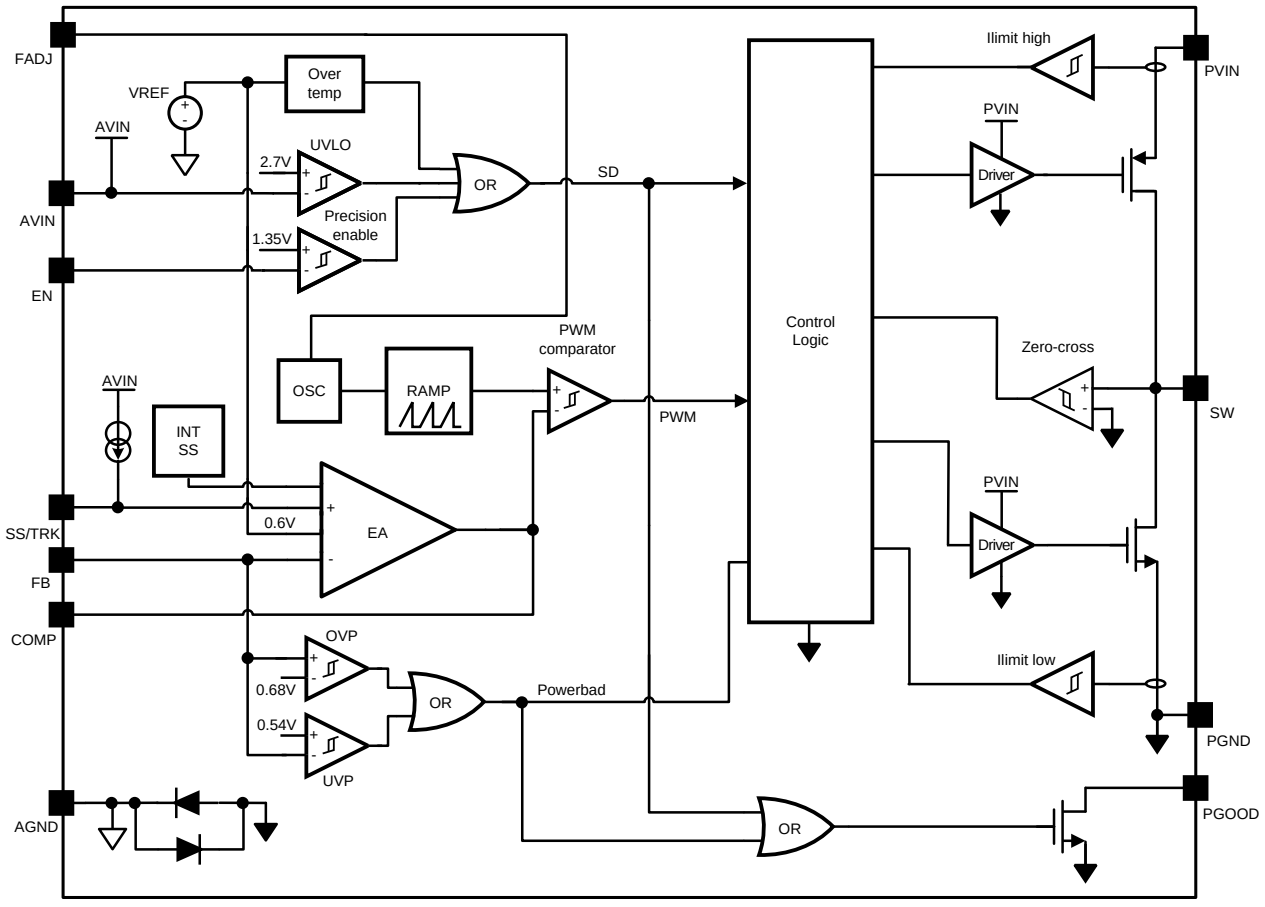
Figure 17. Output Overcurrent Condition

8 Detailed Description

8.1 Overview

The LM21212-2 switching regulator features all of the functions necessary to implement an efficient low voltage buck regulator using a minimum number of external components. This easy-to-use regulator features two integrated switches and is capable of supplying up to 12 A of continuous output current. The regulator utilizes voltage mode control with trailing edge modulation to optimize stability and transient response over the entire output voltage range. The device can operate at high switching frequency allowing use of a small inductor while still achieving high efficiency. The precision internal voltage reference allows the output to be set as low as 0.6 V. Fault protection features include: current limiting, thermal shutdown, overvoltage protection, and shutdown capability. The device is available in the 20-pin HTSSOP package featuring an exposed pad to aid thermal dissipation. The LM21212-2 can be used in numerous applications to efficiently step-down from a 5-V or 3.3-V bus.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Precision Enable

The enable (EN) pin allows the output of the device to be enabled or disabled with an external control signal. This pin is a precision analog input that enables the device when the voltage exceeds 1.35V (typical). The EN pin has 110 mV of hysteresis and will disable the output when the enable voltage falls below 1.24 V (typical). If the EN pin is not used, it can be left open, and will be pulled high by an internal 2-µA current source. Since the enable pin has a precise turn-on threshold it can be used along with an external resistor divider network from VIN to configure the device to turn on at a precise input voltage.

8.3.2 UVLO

The LM21212-2 has a built-in undervoltage lockout protection circuit that keeps the device from switching until the input voltage reaches 2.7V (typical). The UVLO threshold has 200 mV of hysteresis that keeps the device from responding to power-on glitches during start up. If desired the turnon point of the supply can be changed by using the precision enable pin and a resistor divider network connected to VIN as shown in Figure 23 in the design guide.

8.3.3 Current Limit

The LM21212-2 has current limit protection to avoid dangerous current levels on the power FETs and inductor. A current limit condition is met when the current through the high side FET exceeds the rising current limit level (I_{CLR}). The control circuitry will respond to this event by turning off the high side FET and turning on the low side FET. This forces a negative voltage on the inductor, thereby causing the inductor current to decrease. The high-side FET does not conduct again until the lower current limit level (I_{CLF}) is sensed on the low side FET. At this point, the device resumes normal switching.

A current limit condition will cause the internal soft-start voltage to ramp downward. After the internal soft-start ramps below the feedback (FB) pin voltage, (nominally 0.6 V), FB begins to ramp downward, as well. This voltage foldback limits the power consumption in the device, thereby protecting the device from continuously supplying power to the load under a condition that does not fall within the device SOA. After the current limit condition is cleared, the internal soft-start voltage will ramp up again. Figure 18 shows current limit behavior with V_{SS}, V_{FB}, V_{OUT} and V_{SW}.

8.3.4 Short-Circuit Protection

In the unfortunate event that the output is shorted with a low impedance to ground, the LM21212-2 will limit the current into the short by resetting the device. A short-circuit condition is sensed by a current-limit condition coinciding with a voltage on the FB pin that is lower than 100 mV. When this condition occurs, the device will begin its reset sequence, turning off both power FETs and discharging the soft-start capacitor after $t_{RESETSS}$ (nominally 110 µs). The device will then attempt to restart. If the short-circuit condition still exists, it will reset again, and repeat until the short-circuit is cleared. The reset prevents excess current flowing through the FETs in a highly inefficient manner, potentially causing thermal damage to the device or the bus supply.

Feature Description (continued)

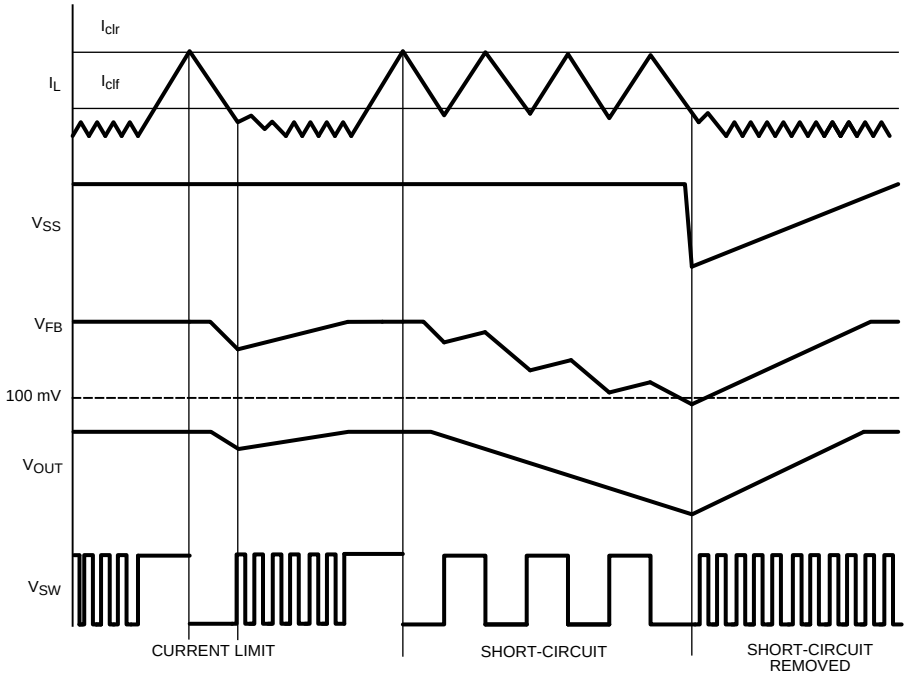


Figure 18. Current Limit Conditions

8.3.5 Thermal Protection

Internal thermal shutdown circuitry is provided to protect the integrated circuit in the event that the maximum junction temperature is exceeded. When activated, typically at 165°C, the LM21212-2 tri-states the power FETs and resets soft start. After the junction cools to approximately 155°C, the device starts up using the normal start up routine. This feature is provided to prevent catastrophic failures from accidental device overheating. Note that thermal limit will not stop the die from operating above the specified operating maximum temperature,125°C. The die should be kept under 125°C to ensure correct operation.

8.3.6 Power-Good Flag

The PGOOD pin provides the user with a way to monitor the status of the LM21212-2. In order to use the PGOOD pin, the application must provide a pullup resistor to a desired DC voltage (in other words, V_{IN}). PGOOD responds to a fault condition by pulling the PGOOD pin low with the open-drain output. PGOOD will pull low on the following conditions – 1) V_{FB} moves above or below the V_{OVP} or V_{UVP}, respectively 2) The enable pin is brought below the enable threshold 3) The device enters a prebiased output condition (V_{FB}>V_{SS}).

Figure 19 shows the conditions that will cause PGOOD to fall.

Feature Description (continued)

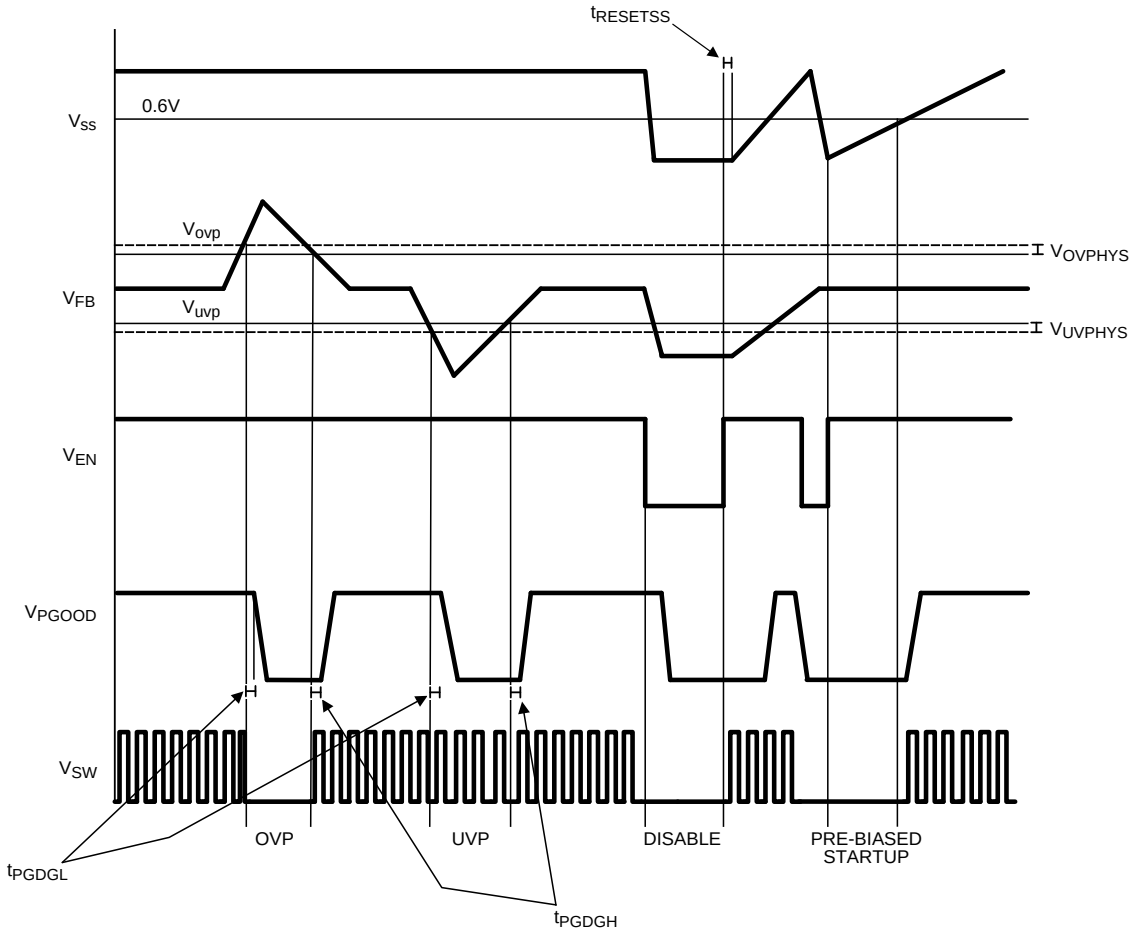


Figure 19. PGOOD Conditions

8.3.7 Light Load Operation

The LM21212-2 offers increased efficiency when operating at light loads. Whenever the load current is reduced to a point where the peak-to-peak inductor ripple current is greater than two times the load current, the device will enter the diode emulation mode preventing significant negative inductor current. The output current at which this occurs is the critical conduction boundary and can be calculated by Equation 1:

$$I_{BOUNDARY} = \frac{(V_{IN} - V_{OUT}) \times D}{2 \times L \times f_{SW}} \quad (1)$$

It can be seen that in diode emulation mode, whenever the inductor current reaches zero the SW node becomes high impedance. Ringing will occur on this pin as a result of the LC tank circuit formed by the inductor and the parasitic capacitance at the node. If this ringing is of concern an additional RC snubber circuit can be added from the switch node to ground.

At very light loads, usually below 500 mA, several pulses may be skipped in between switching cycles, effectively reducing the switching frequency and further improving light-load efficiency.

8.4 Device Functional Modes

Several diagrams are shown in Figure 20 illustrating continuous conduction mode (CCM), discontinuous conduction mode (DCM), and the boundary condition.

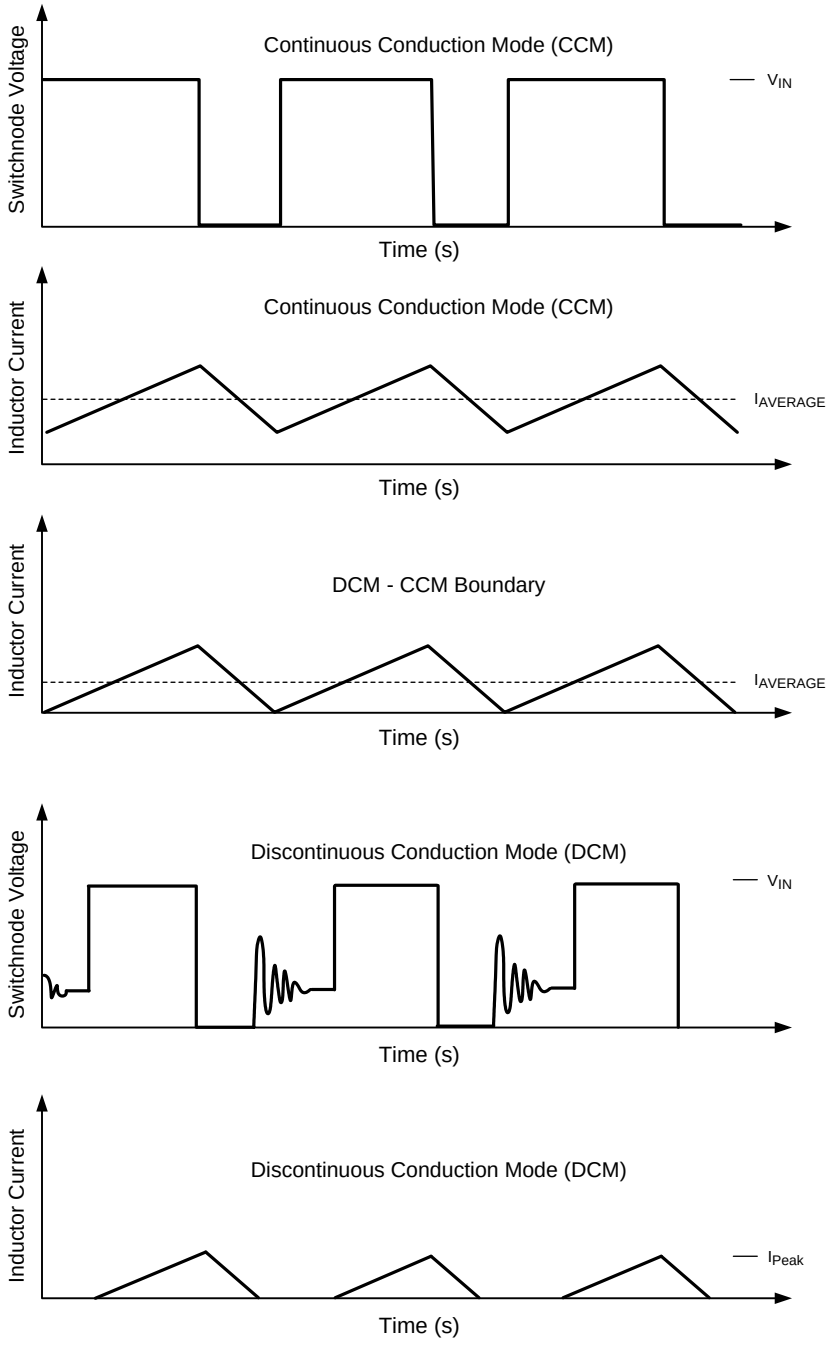


Figure 20. Modes Of Operation for LM21212-2

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The LM21212-2 switching regulator features all of the functions necessary to implement an efficient low voltage buck regulator using a minimum number of external components. This easy-to-use regulator features two integrated switches and is capable of supplying up to 12 A of continuous output current. The regulator utilizes voltage mode control with trailing edge modulation to optimize stability and transient response over the entire output voltage range. The device can operate at high switching frequency allowing use of a small inductor while still achieving high efficiency.

9.2 Typical Application

9.2.1 Typical Application 1

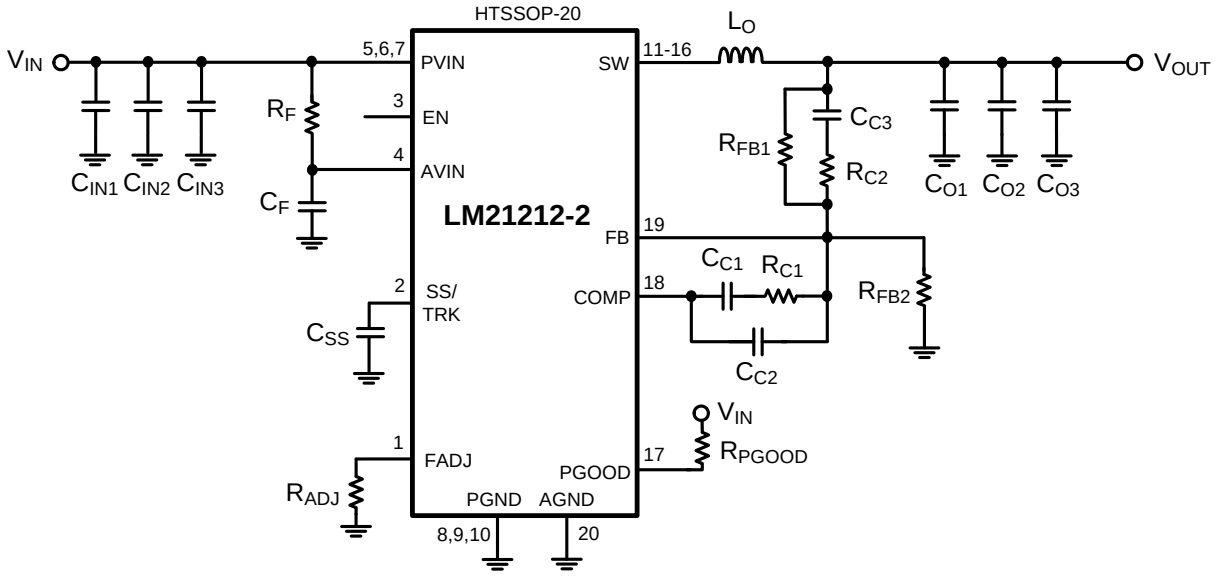


Figure 21. Typical Application Schematic 1

Typical Application (continued)

9.2.1.1 Design Requirements

Table 1. Bill Of Materials (V_{IN} = 3.3 V - 5.5 V, V_{OUT} = 1.2 V, I_{OUT} = 12 A, F_{SW} = 500 kHz)

ID	DESCRIPTION	VENDOR	PART NUMBER	QUANTITY
C_F	CAP, CERM, 1 uF, 10V, +/-10%, X7R, 0603	MuRata	GRM188R71A105KA61D	1
C_{IN1}, C_{IN2}, C_{IN3}, C_{O1}, C_{O2}, C_{O3}	CAP, CERM, 100 uF, 6.3V, +/-20%, X5R, 1206	MuRata	GRM31CR60J107ME39L	6
C_{C1}	CAP, CERM, 1800 pF, 50V, +/-5%, C0G/NP0, 0603	TDK	C1608C0G1H182J	1
C_{C2}	CAP, CERM, 68 pF, 50V, +/-5%, C0G/NP0, 0603	TDK	C1608C0G1H680J	1
C_{C3}	CAP, CERM, 820 pF, 50V, +/-5%, C0G/NP0, 0603	TDK	C1608C0G1H821J	1
C_{SS}	CAP, CERM, 0.033 uF, 16V, +/-10%, X7R, 0603	MuRata	GRM188R71C333KA01D	1
L_O	Inductor, Shielded Drum Core, Powdered Iron, 560nH, 27.5A, 0.0018 ohm, SMD	Vishay-Dale	IHLP4040DZERR56M01	1
R_F	RES, 1.0 ohm, 5%, 0.1W, 0603	Vishay-Dale	CRCW06031R00JNEA	1
R_{C1}	RES, 9.31 kohm, 1%, 0.1W, 0603	Vishay-Dale	CRCW06039K31FKEA	1
R_{C2}	RES, 165 ohm, 1%, 0.1W, 0603	Vishay-Dale	CRCW0603165RFKEA	1
R_{FB1}, R_{FB2}, R_{PGOOD}	RES, 10 kohm, 1%, 0.1W, 0603	Vishay-Dale	CRCW060310K0FKEA	3
R_{ADJ}	RES, 95.3 kohm, 1%, 0.1W, 0603	Vishay-Dale	CRCW060395K3FKEA	1

9.2.1.2 Detailed Design Procedure

9.2.1.2.1 Custom Design With WEBENCH® Tools

Click here to create a custom design using the LM21212-2 device with the WEBENCH® Power Designer.

1. Start by entering the input voltage (V_{IN}), output voltage (V_{OUT}), and output current (I_{OUT}) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance
- Run thermal simulations to understand board thermal performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

9.2.1.2.2 Output Voltage

The first step in designing the LM21212-2 application is setting the output voltage. This is done by using a voltage divider between V_{OUT} and AGND, with the middle node connected to V_{FB}. When operating under steady-state conditions, the LM21212-2 will force V_{OUT} such that V_{FB} is driven to 0.6 V.

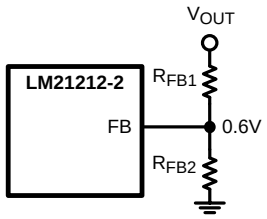


Figure 22. Setting V_{OUT}

A good starting point for the lower feedback resistor, R_{FB2}, is 10kΩ. R_{FB1} can then be calculated the following equation:

$$V_{OUT} = \frac{R_{FB1} + R_{FB2}}{R_{FB2}} 0.6V \quad (2)$$

9.2.1.2.3 Precision Enable

The enable (EN) pin of the LM21212-2 allows the output to be toggled on and off. This pin is a precision analog input. When the voltage exceeds 1.35V, the controller will try to regulate the output voltage as long as the input voltage has exceeded the UVLO voltage of 2.70V. There is an internal current source connected to EN so if enable is not used, the device will turn on automatically. If EN is not toggled directly the device can be preprogrammed to turn on at a certain input voltage higher than the UVLO voltage. This can be done with an external resistor divider from AVIN to EN and EN to AGND as shown below in Figure 23.

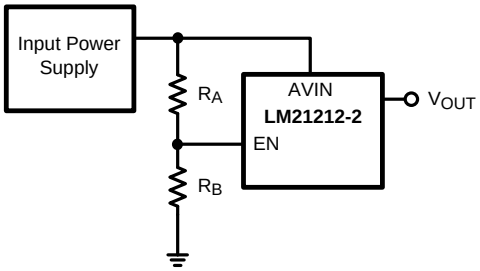


Figure 23. Enable Start-up Through V_{IN}

The resistor values of R_A and R_B can be relatively sized to allow EN to reach the enable threshold voltage depending on the input supply voltage. With the enable current source accounted for, the equation solving for R_A is shown below:

$$R_A = \frac{R_B(V_{PVIN} - 1.35V)}{1.35V - I_{EN}R_B} \quad (3)$$

In the Equation 3 R_A is the resistor from V_{IN} to enable, R_B is the resistor from enable to ground, I_{EN} is the internal enable pullup current (2 µA) and 1.35 V is the fixed precision enable threshold voltage. Typical values for R_B range from 10 kΩ to 100 kΩ.

9.2.1.2.4 Soft Start

When EN has exceeded 1.35 V, and both PVIN and AVIN have exceeded the UVLO threshold, the LM21212-2 begins charging the output linearly to the voltage level dictated by the feedback resistor network. The LM21212-2 has a user adjustable soft-start circuit to lengthen the charging time of the output set by a capacitor from the soft start pin to ground. After enable exceeds 1.35 V, an internal 2-µA current source begins to charge the soft start capacitor. This allows the user to limit inrush currents due to a high output capacitance and not cause an over current condition. Adding a soft-start capacitor can also reduce the stress on the input rail. Larger capacitor values will result in longer start-up times. Use the equation below to approximate the size of the soft-start capacitor:

$$\frac{t_{SS} \times I_{SS}}{0.6V} = C_{SS}$$

where

- $I_{SS}$is nominally 2 µA
- t_{SS} is the desired start-up time (4)

If V_{IN} is higher than the UVLO level and enable is toggled high the soft start sequence will begin. There is a small delay between enable transitioning high and the beginning of the soft-start sequence. This delay allows the LM21212-2 to initialize its internal circuitry. Once the output has charged to 90% of the nominal output voltage the power-good flag will transition high. This behavior is illustrated in Figure 24.

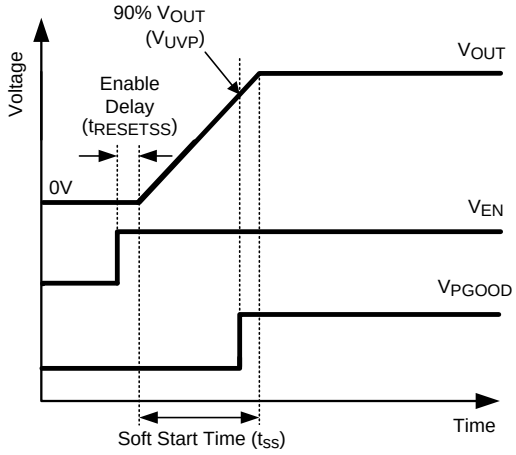


Figure 24. Soft Start Timing

As shown above, the size of the capacitor is influenced by the nominal feedback voltage level 0.6 V, the soft-start charging current I_{SS} (2 µA), and the desired soft start time. If no soft-start capacitor is used then the LM21212-2 defaults to a minimum startup time of 500 µs. The LM21212-2 will not start up faster than 500 µs. When enable is cycled or the device enters UVLO, the charge developed on the soft-start capacitor is discharged to reset the startup process. This also happens when the device enters short circuit mode from an overcurrent event.

9.2.1.2.5 Resistor-Adjustable Frequency

The frequency adjust (FADJ) pin allows the LM21212-2 to be programmed to a predetermined switching frequency between 300 kHz to 1.55 MHz by connecting a resistor between FADJ and AGND. To determine the resistor (R_{ADJ}) value for a desired frequency, the following equation can be used:

$$R_{ADJ} = \frac{54680}{f_{SW}} - 13.15$$

where

- R_{ADJ} is resistance in kΩ
- f_{SW} is frequency in kHz (5)

The desired frequency must fall within the operational frequency range, 300 kHz to 1550 kHz, and a corresponding resistor must be used for normal operation.

9.2.1.2.6 Inductor Selection

The inductor (L) used in the application will influence the ripple current and the efficiency of the system. The first selection criteria is to define a ripple current, ΔI_L. In a buck converter, it is typically selected to run between 20% to 30% of the maximum output current. Figure 25 shows the ripple current in a standard buck converter operating in continuous conduction mode. Larger ripple current results in a smaller inductance value, which will lead to lower inductor series resistance, and improved efficiency. However, larger ripple current will also cause the device to operate in discontinuous conduction mode at a higher average output current.

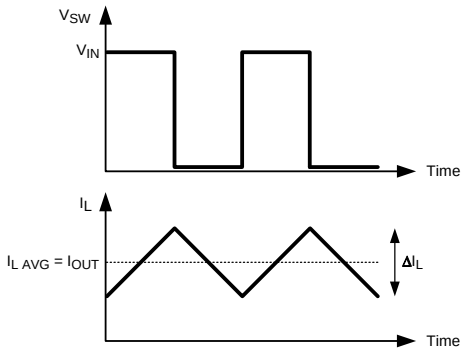


Figure 25. Switch And Inductor Current Waveforms

Once the ripple current has been determined, the appropriate inductor size can be calculated using the following equation:

$$L = \frac{(V_{IN} - V_{OUT}) \cdot D}{\Delta I_L \cdot f_{SW}} \tag{6}$$

9.2.1.2.7 Output Capacitor Selection

The output capacitor, C_{OUT}, filters the inductor ripple current and provides a source of charge for transient load conditions. A wide range of output capacitors may be used with the LM21212-2 that provide various advantages. The best performance is typically obtained using ceramic, SP or OSCON type chemistries. Typical trade-offs are that the ceramic capacitor provides extremely low ESR to reduce the output ripple voltage and noise spikes, while the SP and OSCON capacitors provide a large bulk capacitance in a small volume for transient loading conditions.

When selecting the value for the output capacitor, the two performance characteristics to consider are the output voltage ripple and transient response. The output voltage ripple can be approximated by using the following formula:

$$\Delta V_{OUT} \approx \Delta I_L \times \left[R_{ESR} + \frac{1}{8 \times f_{SW} \times C_{OUT}} \right]$$

where

- ΔV_{OUT} (V) is the amount of peak to peak voltage ripple at the power supply output
- R_{ESR} (Ω) is the series resistance of the output capacitor
- f_{SW} (Hz) is the switching frequency
- C_{OUT} (F) is the output capacitance used in the design (7)

The amount of output ripple that can be tolerated is application specific; however a general recommendation is to keep the output ripple less than 1% of the rated output voltage. Keep in mind ceramic capacitors are sometimes preferred because they have very low ESR; however, depending on package and voltage rating of the capacitor the value of the capacitance can drop significantly with applied voltage. The output capacitor selection will also affect the output voltage droop during a load transient. The peak droop on the output voltage during a load transient is dependent on many factors; however, an approximation of the transient droop ignoring loop bandwidth can be obtained using the following equation:

$$V_{DROOP} = \Delta I_{OUTSTEP} \times R_{ESR} + \frac{L \times \Delta I_{OUTSTEP}^2}{C_{OUT} \times (V_{IN} - V_{OUT})}$$

where

- C_{OUT} (F) is the minimum required output capacitance
- L (H) is the value of the inductor
- V_{DROOP} (V) is the output voltage drop ignoring loop bandwidth considerations

- $\Delta I_{OUTSTEP}$ (A) is the load step change
- R_{ESR} (Ω) is the output capacitor ESR
- V_{IN} (V) is the input voltage
- V_{OUT} (V) is the set regulator output voltage (8)

Both the tolerance and voltage coefficient of the capacitor must be examined when designing for a specific output ripple or transient droop target.

9.2.1.2.8 Input Capacitor Selection

Quality input capacitors are necessary to limit the ripple voltage at the PVIN pin while supplying most of the switch current during the on-time. Additionally, they help minimize input voltage droop in an output current transient condition. In general, it is recommended to use a ceramic capacitor for the input as it provides both a low impedance and small footprint. Use of a high-grade dielectric for the ceramic capacitor, such as X5R or X7R, will provide improved performance over temperature and also minimize the DC voltage derating that occurs with Y5V capacitors. The input capacitors should be placed as close as possible to the PVIN and PGND pins.

Non-ceramic input capacitors should be selected for RMS current rating and minimum ripple voltage. A good approximation for the required ripple current rating is given by the relationship:

$$I_{IN\text{-}RMS} = I_{OUT} \sqrt{D(1 - D)} \quad (9)$$

As indicated by the RMS ripple current equation, highest requirement for RMS current rating occurs at 50% duty cycle. For this case, the RMS ripple current rating of the input capacitor should be greater than half the output current. For best performance, place low ESR ceramic capacitors in parallel with higher capacitance capacitors to provide the best input filtering for the device.

When operating at low input voltages (3.3 V or lower), additional capacitance may be necessary to protect from triggering an under-voltage condition on an output current transient. This will depend on the impedance between the input voltage supply and the LM21212-2, as well as the magnitude and slew rate of the output transient.

The AVIN pin requires a 1-µF ceramic capacitor to AGND and a 1-Ω resistor to PVIN. This RC network filter inherent noise on PVIN from the sensitive analog circuitry connected to AVIN.

9.2.1.2.9 Control Loop Compensation

The LM21212-2 incorporates a high bandwidth amplifier between the FB and COMP pins to allow the user to design a compensation network that matches the application. This section will walk through the various steps in obtaining the open loop transfer function.

There are three main blocks of a voltage mode buck switcher that the power supply designer must consider when designing the control system; the power train, modulator, and the compensated error amplifier. A closed loop diagram is shown in Figure 26.

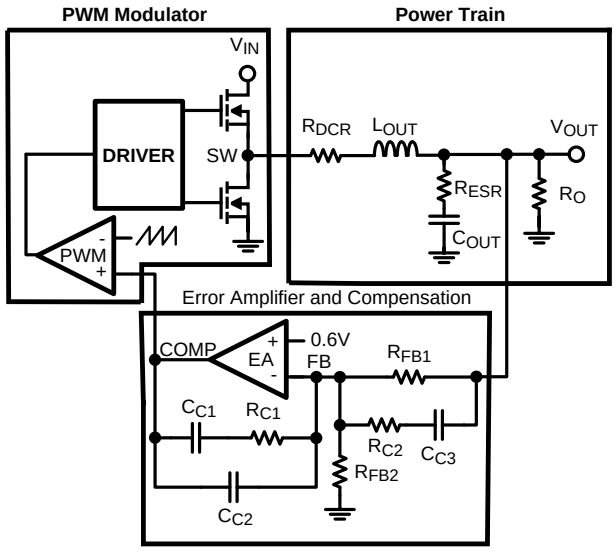


Figure 26. Loop Diagram

The power train consists of the output inductor (L) with DCR (DC resistance R_{DCR}), output capacitor (C_0) with ESR (effective series resistance R_{ESR}), and load resistance (R_o). The error amplifier (EA) constantly forces FB to 0.6 V. The passive compensation components around the error amplifier help maintain system stability. The modulator creates the duty cycle by comparing the error amplifier signal with an internally generated ramp set at the switching frequency.

There are three transfer functions that must be taken into consideration when obtaining the total open loop transfer function; COMP to SW (modulator) , SW to V_{OUT} (power train), and V_{OUT} to COMP (error amplifier). The COMP to SW transfer function is simply the gain of the PWM modulator.

$$G_{PWM} = \frac{V_{in}}{\Delta V_{ramp}}$$

where

- ΔV_{RAMP} is the oscillator peak-to-peak ramp voltage (nominally 0.8 V) (10)

The SW-to-COMP transfer function includes the output inductor, output capacitor, and output load resistance. The inductor and capacitor create two complex poles at a frequency described by:

$$f_{LC} = \frac{1}{2\pi}\sqrt{\frac{R_O + R_{DCR}}{L_{OUT}C_{OUT}(R_O + R_{ESR})}} \quad (11)$$

In addition to two complex poles, a left half plane zero is created by the output capacitor ESR located at a frequency described by:

$$f_{ESR} = \frac{1}{2\pi C_{OUT}R_{ES}} \quad (12)$$

A Bode plot showing the power train response is shown in Figure 27

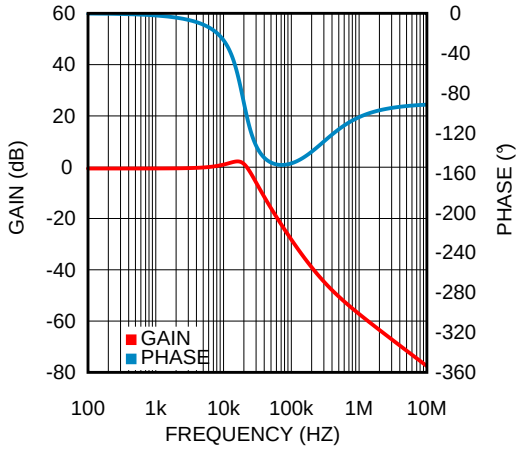


Figure 27. Power Train Bode Plot

The complex poles created by the output inductor and capacitor cause a 180° phase shift at the resonant frequency as seen in Figure 27. The phase is boosted back up to –90° because of the output capacitor ESR zero. The 180° phase shift must be compensated out and phase boosted through the error amplifier to stabilize the closed loop response. The compensation network shown around the error amplifier in Figure 26 creates two poles, two zeros and a pole at the origin. Placing these poles and zeros at the correct frequencies will stabilize the closed loop response. The Compensated Error Amplifier transfer function is:

$$G_{EA} = K_m \frac{\left(\frac{s}{2\pi f_{Z1}} + 1\right)\left(\frac{s}{2\pi f_{Z2}} + 1\right)}{s\left(\frac{s}{2\pi f_{P1}} + 1\right)\left(\frac{s}{2\pi f_{P2}} + 1\right)} \tag{13}$$

The pole located at the origin gives high open loop gain at DC, translating into improved load regulation accuracy. This pole occurs at a very low frequency due to the limited gain of the error amplifier; however, it can be approximated at DC for the purposes of compensation. The other two poles and two zeros can be located accordingly to stabilize the voltage mode loop depending on the power stage complex poles and Q. Figure 28 is an illustration of what the Error Amplifier Compensation transfer function will look like.

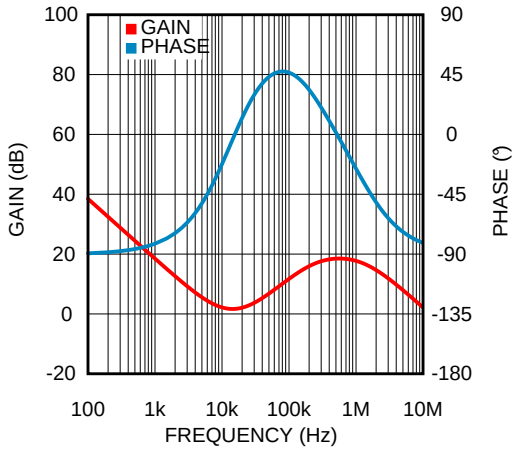


Figure 28. Type 3 Compensation Network Bode Plot

As seen in Figure 28, the two zeros ($f_{LC}/2$, f_{LC}) in the comensation network give a phase boost. This will cancel out the effects of the phase loss from the output filter. The compensation network also adds two poles to the system. One pole should be located at the zero caused by the output capacitor ESR (f_{ESR}) and the other pole should be at half the switching frequency ($f_{SW}/2$) to roll off the high frequency response. The dependancy of the pole and zero locations on the compensation components is described below.

$$f_{Z1} = \frac{f_{LC}}{2} = \frac{1}{2\pi R_{C1} C_{C1}}$$

$$f_{Z2} = f_{LC} = \frac{1}{2\pi (R_{C1} + R_{FB1}) C_{C3}}$$

$$f_{P1} = f_{ESR} = \frac{1}{2\pi R_{C2} C_{C3}}$$

$$f_{P2} = \frac{f_{sw}}{2} = \frac{C_{C1} + C_{C2}}{2\pi R_{C1} C_{C1} C_{C2}} \quad (14)$$

An example of the step-by-step procedure to generate compensation component values using the typical application setup (see Figure 21) is given. The parameters needed for the compensation values are given in the table below.

PARAMETER	VALUE
V_{IN}	5 V
V_{OUT}	1.2 V
I_{OUT}	12 A
$f_{CROSSOVER}$	100 kHz
L	0.56 µH
R_{DCR}	1.8 mΩ
C_O	150 µF
R_{ESR}	1 mΩ
ΔV_{RAMP}	0.8 V
f_{SW}	500 kHz

where ΔV_{RAMP} is the oscillator peak-to-peak ramp voltage (nominally 0.8V), and $f_{CROSSOVER}$ is the frequency at which the open-loop gain is a magnitude of 1. It is recommended that the $f_{crossover}$ not exceed one-fifth of the switching frequency. The output capacitance, C_O, depends on capacitor chemistry and bias voltage. For Multi-Layer Ceramic Capacitors (MLCC), the total capacitance will degrade as the DC bias voltage is increased. Measuring the actual capacitance value for the output capacitors at the output voltage is recommended to accurately calculate the compensation network. The example given here is the total output capacitance using the three MLCC output capacitors biased at 1.2V, as seen in the typical application schematic, . Note that it is more conservative, from a stability standpoint, to err on the side of a smaller output capacitance value in the compensation calculations rather than a larger, as this will result in a lower bandwidth but increased phase margin.

First, a the value of R_{FB1} should be chosen. A typical value is 10 kΩ. From this, the value of R_{C1} can be calculated to set the mid-band gain so that the desired crossover frequency is achieved:

$$R_{C1} = \frac{f_{CROSSOVER}}{f_{LC}} \bullet \frac{\Delta V_{RAMP}}{V_{IN}} \bullet R_{FB1}$$

$$= \frac{100\ kHz}{17.4\ kHz} \frac{0.8\ V}{5.0\ V} 10\ k\Omega$$

$$= 9.2\ k\Omega \quad (15)$$

Next, the value of C_{C1} can be calculated by placing a zero at half of the LC double pole frequency (f_{LC}):

$$C_{C1} = \frac{1}{\pi f_{LC} R_{C1}} = 1.99\ \text{nF} \quad (16)$$

Now the value of C_{C2} can be calculated to place a pole at half of the switching frequency (f_{SW}):

$$C_{C2} = \frac{C_{C1}}{\pi f_{SW} R_{C1} C_{C1} - 1} = 71\ \text{pF} \quad (17)$$

R_{C2} can then be calculated to set the second zero at the LC double pole frequency:

$$R_{C2} = \frac{R_{FB1} f_{LC}}{f_{ESR} - f_{LC}} = 166\Omega \quad (18)$$

Last, C_{C3} can be calculated to place a pole at the same frequency as the zero created by the output capacitor ESR:

$$C_{C3} = \frac{1}{2\pi f_{ESR} R_{C2}} = 898\ \text{pF} \quad (19)$$

An illustration of the total loop response can be seen in Figure 29.

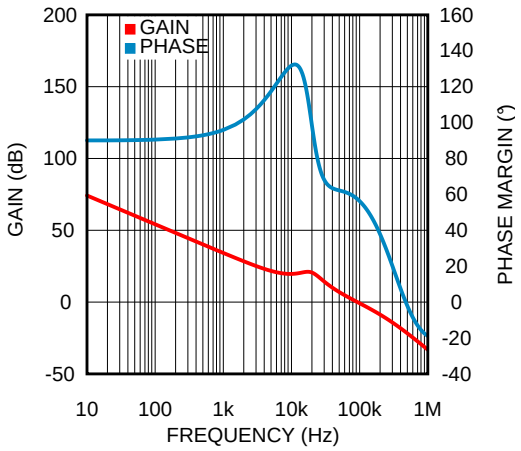


Figure 29. Loop Response

It is important to verify the stability by either observing the load transient response or by using a network analyzer. A phase margin between 45° and 70° is usually desired for voltage mode systems. Excessive phase margin can cause slow system response to load transients and low phase margin may cause an oscillatory load transient response. If the load step response peak deviation is larger than desired, increasing $f_{CROSSOVER}$ and recalculating the compensation components may help but usually at the expense of phase margin.

9.2.1.3 Application Curves

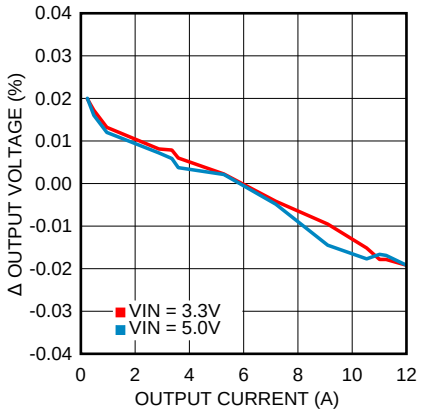


Figure 30. Load Regulation

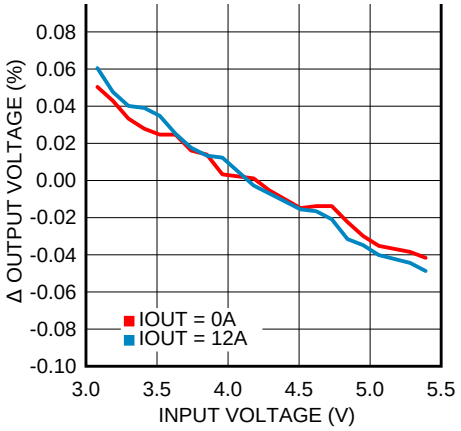


Figure 31. Line Regulation

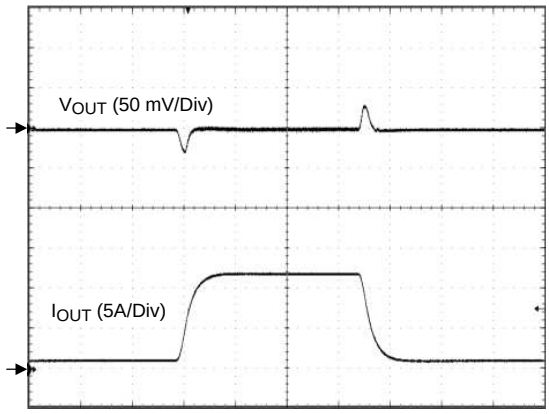


Figure 32. Load Transient Response (F_{SW} = 650 kHz)

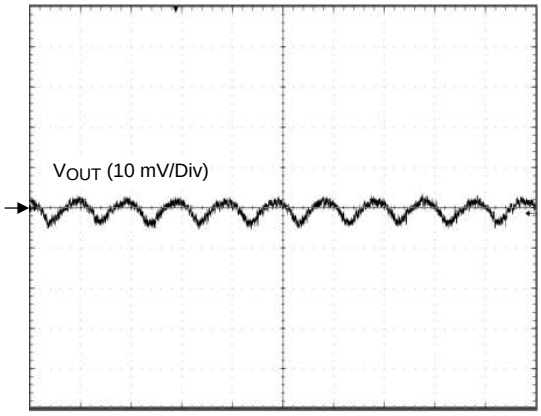


Figure 33. Output Voltage Ripple

9.2.2 Typical Application Schematic 2

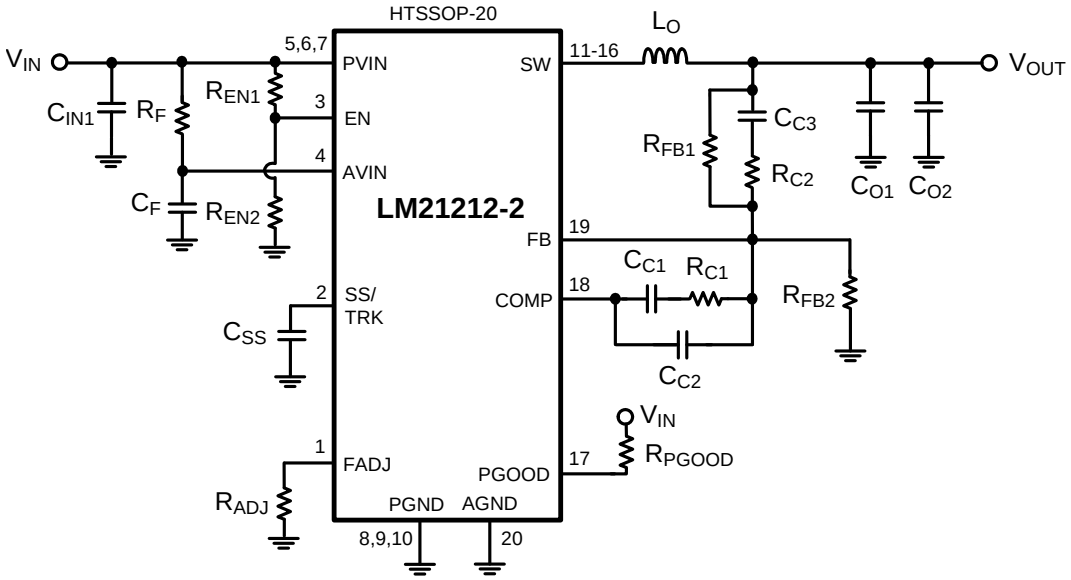


Figure 34. Typical Application Schematic 2

9.2.2.1 Design Requirements

Table 2. Bill Of Materials (V_{IN} = 4 V- 5.5 V, V_{OUT} = 0.9 V, I_{OUT} = 8 A, F_{SW} = 1 MHz)

ID	DESCRIPTION	VENDOR	PART NUMBER	QUANTITY
C_F	CAP, CERM, 1 uF, 10V, +/-10%, X7R, 0603	MuRata	GRM188R71A105KA61D	1
C_{IN1}, C_{O1}, C_{O2}	CAP, CERM, 100 uF, 6.3V, +/-20%, X5R, 1206	MuRata	GRM31CR60J107ME39L	3
C_{C1}	CAP, CERM, 1800 pF, 50V, +/-5%, C0G/NP0, 0603	MuRata	GRM1885C1H182JA01D	1
C_{C2}	CAP, CERM, 68 pF, 50V, +/-5%, C0G/NP0, 0603	TDK	C1608C0G1H680J	1
C_{C3}	CAP, CERM, 470 pF, 50V, +/-5%, C0G/NP0, 0603	TDK	C1608C0G1H471J	1
C_{SS}	CAP, CERM, 0.033 uF, 16V, +/-10%, X7R, 0603	MuRata	GRM188R71C333KA01D	1
L_O	Inductor, Shielded Drum Core, Superflux, 240nH, 20A, 0.001 ohm, SMD	Wurth Elektronik	744314024	1
R_F	RES, 1.0 ohm, 5%, 0.1W, 0603	Vishay-Dale	CRCW06031R00JNEA	1
R_{C1}	RES, 4.87 kohm, 1%, 0.1W, 0603	Vishay-Dale	CRCW06034K87FKEA	1
R_{C2}	RES, 210 ohm, 1%, 0.1W, 0603	Vishay-Dale	CRCW0603210RFKEA	1
R_{EN1}, R_{FB1}, R_{PGOOD}	RES, 10k ohm, 1%, 0.1W, 0603	Vishay-Dale	CRCW060310K0FKEA	3
R_{EN2}	RES, 19.6 kohm, 1%, 0.1W, 0603	Vishay-Dale	CRCW060319K6FKEA	1
R_{FB2}	RES, 20.0 kohm, 1%, 0.1W, 0603	Vishay-Dale	CRCW060320K0FKEA	1
R_{ADJ}	RES, 41.2 kohm, 1%, 0.1W, 0603	Vishay-Dale	CRCW060341K2FKEA	1

9.2.2.2 Detailed Design Procedure

See *Detailed Design Procedure*

10 Layout

10.1 Layout Considerations

PC board layout is an important part of DC/DC converter design. Poor board layout can disrupt the performance of a DC/DC converter and surrounding circuitry by contributing to EMI, ground bounce, and resistive voltage loss in the traces. These can send erroneous signals to the DC/DC converter resulting in poor regulation or instability.

Good layout can be implemented by following a few simple design rules.

1. Minimize area of switched current loops. In a buck regulator there are two loops where currents are switched at high slew rates. The first loop starts from the input capacitor, to the regulator PVIN pin, to the regulator SW pin, to the inductor then out to the output capacitor and load. The second loop starts from the output capacitor ground, to the regulator GND pins, to the inductor and then out to the load (see Figure 35). To minimize both loop areas, the input capacitor must be placed as close as possible to the VIN pin. Grounding for both the input and output capacitor must be close. Ideally, a ground plane must be placed on the top layer that connects the PGND pins, the exposed pad (EP) of the device, and the ground connections of the input and output capacitors in a small area near pins 10 and 11 of the device. The inductor must be placed as close as possible to the SW pin and output capacitor.
2. Minimize the copper area of the switch node. The six SW pins must be routed on a single top plane to the pad of the inductor. The inductor must be placed as close as possible to the switch pins of the device with a wide trace to minimize conductive losses. The inductor can be placed on the bottom side of the PCB relative to the LM21212-2, but care must be taken to not allow any coupling of the magnetic field of the inductor into the sensitive feedback or compensation traces.
3. Have a solid ground plane between PGND, the EP and the input and output cap. ground connections. The ground connections for the AGND, compensation, feedback, and soft-start components must be physically isolated (located near pins 1 and 20) from the power ground plane but a separate ground connection is not necessary. If not properly handled, poor grounding can result in degraded load regulation or erratic switching behavior.
4. Carefully route the connection from the VOUT signal to the compensation network. This node is high impedance and can be susceptible to noise coupling. The trace must be routed away from the SW pin and inductor to avoid contaminating the feedback signal with switch noise. Additionally,feedback resistors R_{FB1} and R_{FB2} must be located near the device to minimize the trace length to FB between these resistors.
5. Make input and output bus connections as wide as possible. This reduces any voltage drops on the input or output of the converter and can improve efficiency. Voltage accuracy at the load is important so make sure feedback voltage sense is made at the load. Doing so will correct for voltage drops at the load and provide the best output accuracy.
6. Provide adequate device heatsinking. For most 12A designs a four layer board is recommended. Use as many vias as possible to connect the EP to the power plane heatsink. The vias located underneath the EP will wick solder into them if they are not filled. Complete solder coverage of the EP to the board is required to achieve the θ_{JA} values described in the previous section. Either an adequate amount of solder must be applied to the EP pad to fill the vias, or the vias must be filled during manufacturing. See the Thermal Considerations section to ensure enough copper heatsinking area is used to keep the junction temperature below 125°C.

10.2 Layout Example

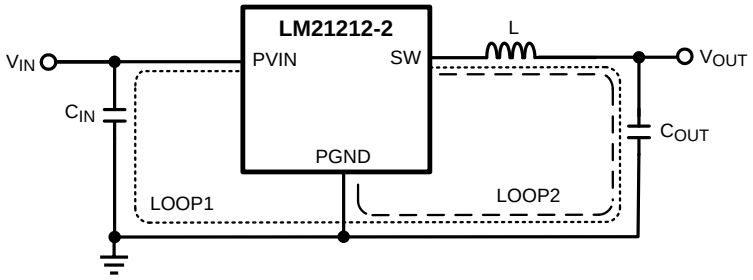


Figure 35. Schematic of LM21212-2 Highlighting Layout Sensitive Nodes

10.3 Thermal Considerations

The thermal characteristics of the LM21212-2 are specified using the parameter θ_{JA}, which relates the junction temperature to the ambient temperature. Although the value of θ_{JA} is dependant on many variables, it still can be used to approximate the operating junction temperature of the device.

To obtain an estimate of the device junction temperature, one may use the following relationship:

$$T_J = P_D \bullet \theta_{JA} + T_A \tag{20}$$

where

- T_J is the junction temperature in °C
- θ_{JA} is the junction to ambient thermal resistance for the LM21212-2
- T_A is the ambient temperature in °C

and

$$P_D = P_{IN} \bullet (1 - \text{Efficiency}) - I_{OUT}^2 \bullet R_{DCR} \tag{21}$$

where

- P_{IN} is the input power in Watts ($P_{IN} = V_{IN} \times I_{IN}$)
- I_{OUT} is the output load current in A

It is important to always keep the operating junction temperature (T_J) below 125°C for reliable operation. If the junction temperature exceeds 165°C the device will cycle in and out of thermal shutdown. If thermal shutdown occurs it is a sign of inadequate heatsinking or excessive power dissipation in the device.

Figure 36, shown below, provides a better approximation of the θ_{JA} for a given PCB copper area. The PCB used in this test consisted of 4 layers: 1 oz. copper was used for the internal layers while the external layers were plated to 2 oz. copper weight. To provide an optimal thermal connection, a 3 × 4 array of 8 mil. vias under the thermal pad were used, and an additional sixteen 8 mil. vias under the rest of the device were used to connect the 4 layers.

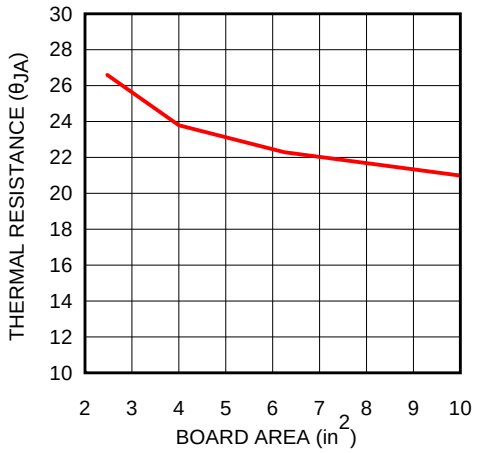


Figure 36. Thermal Resistance vs PCB Area (4-Layer Board)

Thermal Considerations (continued)

Figure 37 shows a plot of the maximum ambient temperature vs output current for the typical application circuit shown in , assuming a θ_{JA} value of 24°C/W.

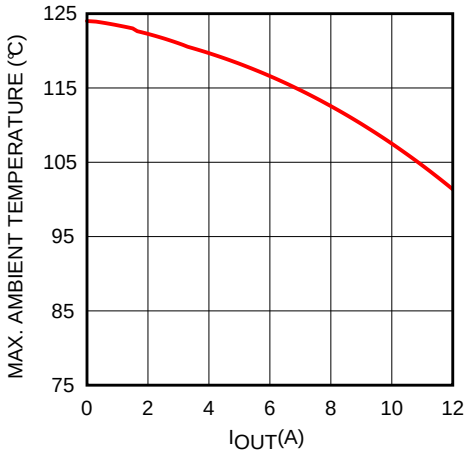


Figure 37. Maximum Ambient Temperature vs Output Current (0 LFM)

11 デバイスおよびドキュメントのサポート

11.1 デバイス・サポート

11.1.1 デベロッパー・ネットワークの製品に関する免責事項

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11.1.2 開発サポート

11.1.2.1 WEBENCH®ツールによるカスタム設計

ここをクリックすると、WEBENCH® Power Designer により、LM21212-2 デバイスを使用するカスタム設計を作成できます。

1. 最初に、入力電圧(V_{IN})、出力電圧(V_{OUT})、出力電流(I_{OUT})の要件を入力します。
2. オプティマイザのダイヤルを使用して、効率、占有面積、コストなどの主要なパラメータについて設計を最適化します。
3. 生成された設計を、テキサス・インスツルメンツが提供する他の方式と比較します。

WEBENCH Power Designerでは、カスタマイズされた回路図と部品リストを、リアルタイムの価格と部品の在庫情報と併せて参照できます。

通常、次の操作を実行可能です。

- 電気的なシミュレーションを実行し、重要な波形と回路の性能を確認する。
- 熱シミュレーションを実行し、基板の熱特性を把握する。
- カスタマイズされた回路図やレイアウトを、一般的なCADフォーマットで出力する。
- 設計のレポートをPDFで印刷し、設計を共有する。

WEBENCHツールの詳細は、www.ti.com/WEBENCHでご覧になれます。

11.2 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、ti.comのデバイス製品フォルダを開いてください。右上の「アラートを受け取る」をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

11.3 コミュニティ・リソース

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

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WEBENCH is a registered trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

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静電気放電はわずかな性能の低下から完全なデバイスの故障に至るまで、様々な損傷を与えます。高精度の集積回路は、損傷に対して敏感であり、極めてわずかなパラメータの変化により、デバイスに規定された仕様に適合しなくなる場合があります。

11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。この情報は、そのデバイスについて利用可能な最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LM21212MH-2/NOPB	Active	Production	HTSSOP (PWP) | 20	73 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LM21212 MH-2
LM21212MH-2/NOPB.A	Active	Production	HTSSOP (PWP) | 20	73 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LM21212 MH-2
LM21212MHE-2/NOPB	Active	Production	HTSSOP (PWP) | 20	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LM21212 MH-2
LM21212MHE-2/NOPB.A	Active	Production	HTSSOP (PWP) | 20	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LM21212 MH-2
LM21212MHX-2/NOPB	Active	Production	HTSSOP (PWP) | 20	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LM21212 MH-2
LM21212MHX-2/NOPB.A	Active	Production	HTSSOP (PWP) | 20	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LM21212 MH-2
LM21212MHX2/NOPBG4.A	Active	Production	HTSSOP (PWP) | 20	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LM21212 MH-2

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

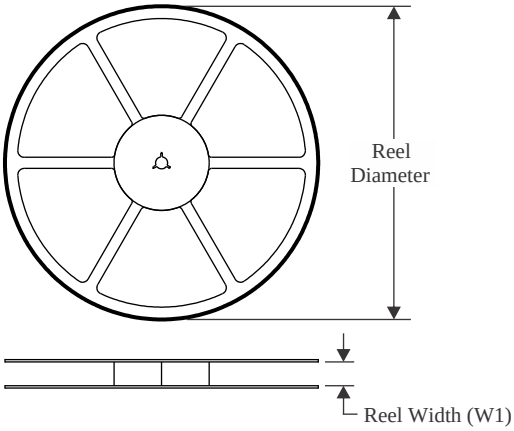
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

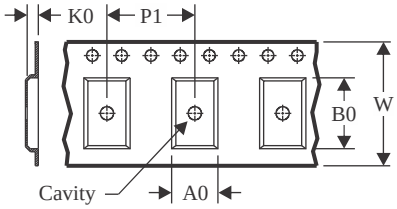
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

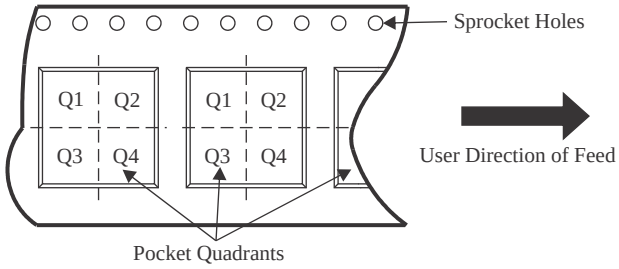


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

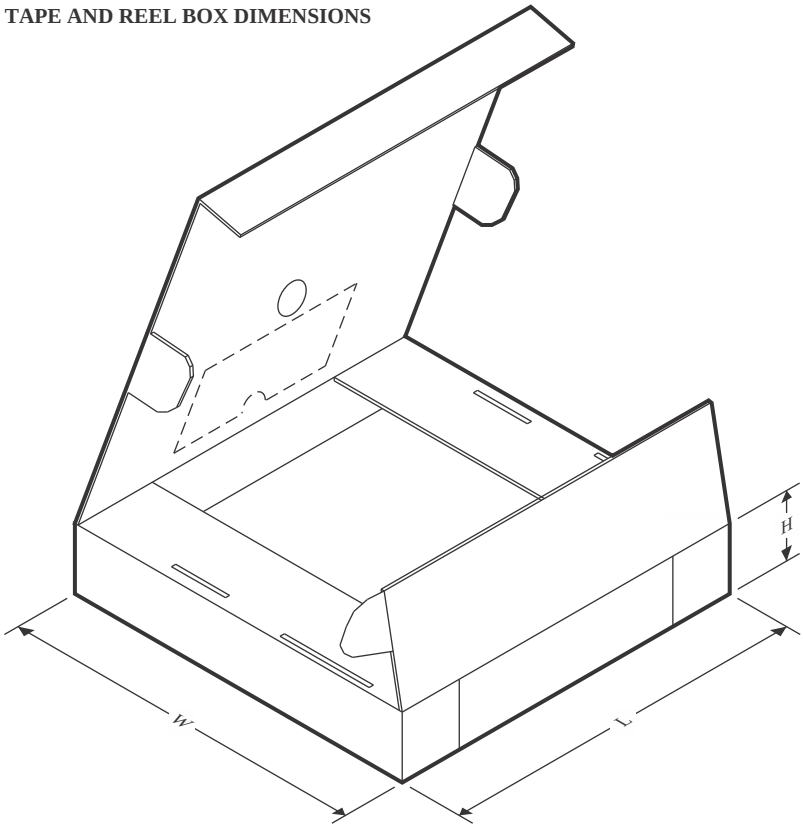
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM21212MHE-2/NOPB	HTSSOP	PWP	20	250	178.0	16.4	6.95	7.0	1.4	8.0	16.0	Q1
LM21212MHX-2/NOPB	HTSSOP	PWP	20	2500	330.0	16.4	6.95	7.0	1.4	8.0	16.0	Q1

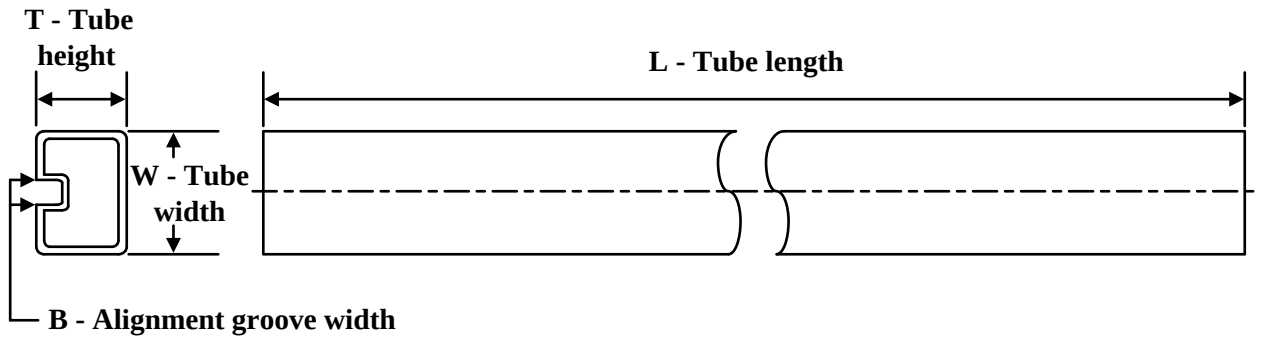
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM21212MHE-2/NOPB	HTSSOP	PWP	20	250	210.0	185.0	35.0
LM21212MHX-2/NOPB	HTSSOP	PWP	20	2500	367.0	367.0	35.0

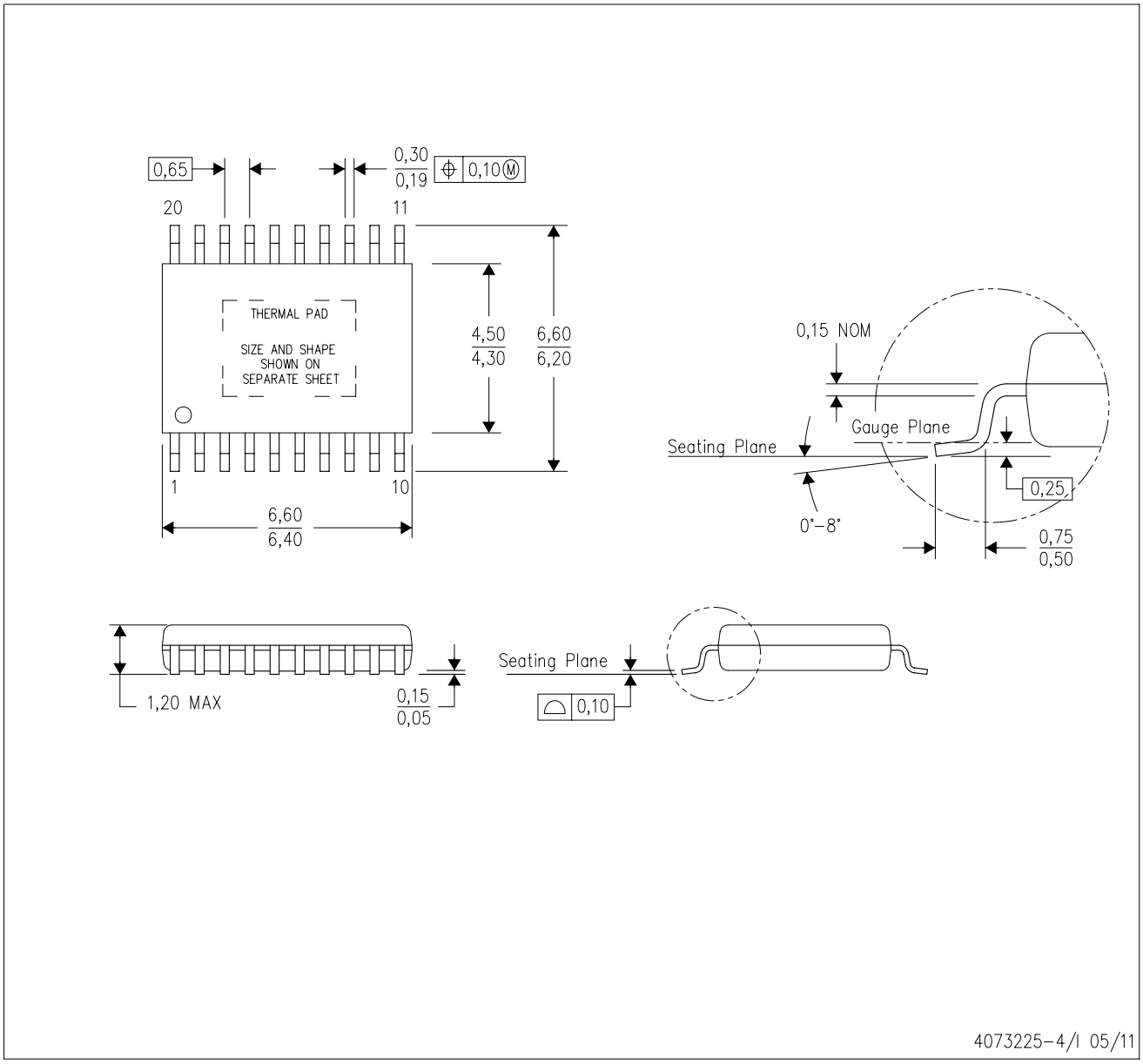
TUBE



*All dimensions are nominal

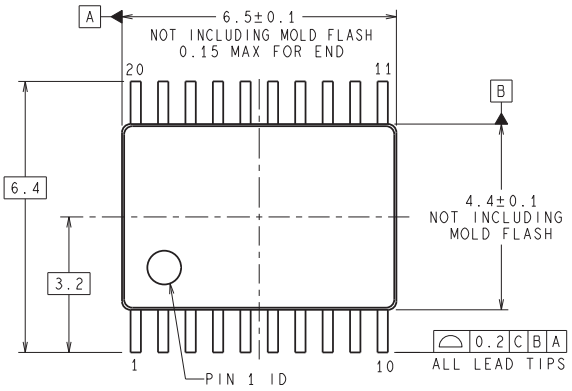
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
LM21212MH-2/NOPB	PWP	HTSSOP	20	73	495	8	2514.6	4.06
LM21212MH-2/NOPB.A	PWP	HTSSOP	20	73	495	8	2514.6	4.06

PWP (R–PDSO–G20) PowerPAD™ PLASTIC SMALL OUTLINE

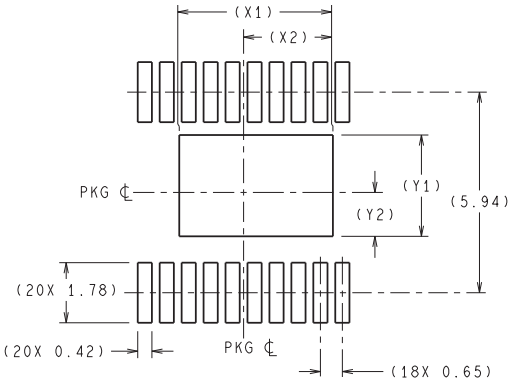


NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusions. Mold flash and protrusion shall not exceed 0.15 per side.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
E. Falls within JEDEC MO–153

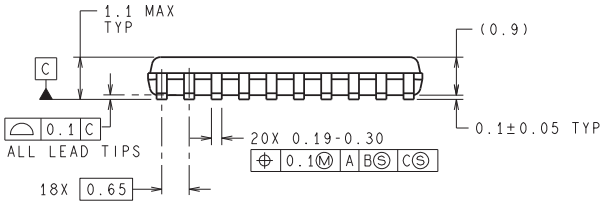
PWP0020AA

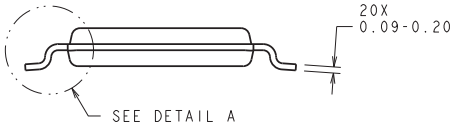


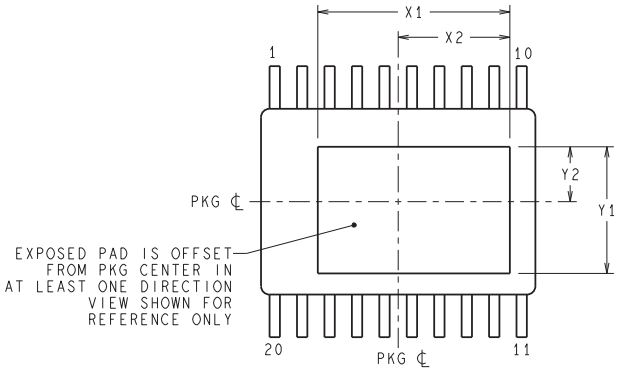
TOP VIEW



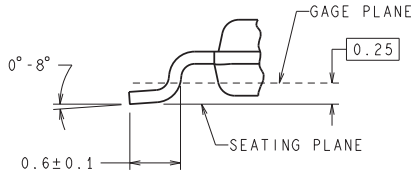
LAND PATTERN RECOMENDATION







BOTTOM VIEW



DETAIL A
TYPICAL

PAD SIZE CODE IN DWG No. (XX)	PAD SIZE		X2	Y2
	X1	Y1		
AA	4.55	3.32	2.645±0.1	1.66±0.1

DIMENSIONS ARE IN MILLIMETERS
DIMENSIONS IN ( ) FOR REFERENCE ONLY

MYB20XX (REV E)

4214875/A 02/2013

NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
B. This drawing is subject to change without notice.
C. Reference JEDEC Registration MO-153, Variation ACT.

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最終更新日：2025 年 10 月