

LM21215 2.95~5.5V、12A、電圧モード同期整流降圧レギュレータ

1 特長

- 7mΩ ハイサイドおよび 4.3mΩ ローサイドの FET スイッチを内蔵
- 調整可能な電流制限
- 出力電圧を 0.6V~V_{IN} の範囲で変更可能 (100% デューティ・サイクルが可能)、±1% の基準電圧
- 入力電圧範囲: 2.95V~5.5V
- 固定スイッチング周波数: 500kHz
- 負荷をプリバイアスして起動可能
- 出力電圧トラッキング機能
- 広い帯域幅の電圧ループ誤差アンプ
- 外付けコンデンサによりソフトスタートを設定可能
- ヒステリシス機能付きの高精度イネーブル・ピン
- OVP、OTP、UVLO、パワー・グッドを内蔵
- 熱的に強化された 20 ピン HTSSOP 露出パッド・パッケージ
- WEBENCH® Power Designer により、LM21215 を使用するカスタム設計を作成

2 アプリケーション

- ブロードバンド、ネットワーク、ワイヤレス通信
- 高性能 FPGA、ASIC、マイクロプロセッサ
- 設計が簡単な、5V または 3.3V バスからの高効率ポイント・オブ・ロード・レギュレーション

3 概要

LM21215 は、非常に優れた効率で最低 0.6V の出力電圧を生成すると同時に、最大 15A の連続出力電流を供給できるモノリシック・ポイント・オブ・ロード同期整流降圧レ

ギュレータです。このデバイスは 2.95V~5.5V の入力電圧範囲で動作するよう最適化されており、広範な低電圧システムに適しています。電圧モード制御ループにより、ノイズ耐性が高く、狭いデューティ・サイクルに対応でき、どんな種類の出力容量を使っても安定に補償できるため、柔軟性が非常に高く、簡単に使用できます。

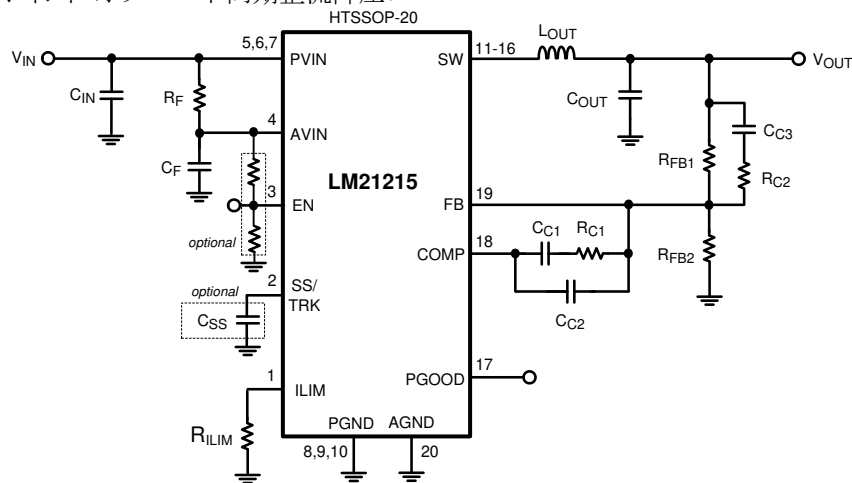
LM21215 は、過電圧保護 (OVP) 機能と抵抗で設定可能な過電流保護 (OCP) 機能を内蔵し、システムの信頼性を高めています。高精度のイネーブル・ピンと内蔵の UVLO により、デバイスの電源オンを厳格に制御し、シーケンシングできます。スタートアップ時の突入電流は、内部で固定、または外部から設定可能なソフトスタート回路により制限されます。内蔵のパワー・グッド回路により、フォルト検出と電源シーケンシングが可能です。

LM21215 は、マルチレールの電源アーキテクチャで適切に動作するよう設計されています。デバイスの出力電圧は、SS/TRK ピンを使用して、外部電圧レールに追従するよう構成可能です。起動時に出力がプリバイアスされている場合、本レギュレータは電流をシンクしないため、出力はプリバイアス電圧を超えてスムーズに上昇できます。このレギュレータは 20 ピンの HTSSOP パッケージで供給され、付属の露出パッドを PCB にハンダ付け可能なため、大きなヒートシンクが必要ありません。

製品情報

部品番号	パッケージ ⁽¹⁾	本体サイズ (公称)
LM21215	HTSSOP (20)	6.50mm × 4.40mm

- (1) 利用可能なパッケージについては、このデータシートの末尾にある注文情報を参照してください。



アプリケーションの簡略回路図



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4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision F (June 2019) to Revision G (March 2022)	Page
• 文書全体にわたって表、図、相互参照の採番方法を更新.....	1
• Removed reference to adjustable frequency.....	10
• Removed reference to adjustable frequency.....	15

Changes from Revision E (March 2013) to Revision F (June 2019)	Page
• 編集上の変更のみ、技術上の修正なし、WEBENCH のリンクを追加.....	1

5 Pin Configuration and Functions

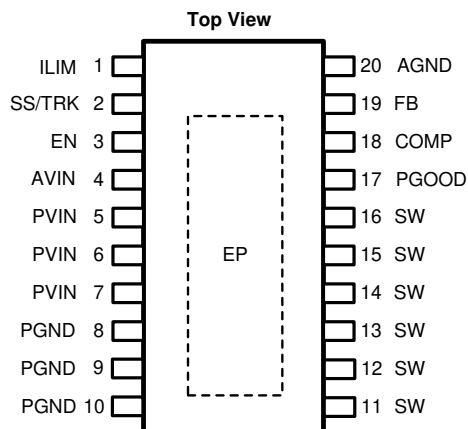


图 5-1. 20-Pin HTSSOP Package PWP Package (Top View)

表 5-1. Pin Functions

PIN		
NO.	NAME	DESCRIPTION
1	ILIM	Resistor-programmable current limit pin. A resistor connected to this pin and ground sets the value of the rising current limit, I_{CLR} . Shorting this pin to AGND programs the device to the maximum possible current limit.
2	SS/TRK	Soft-start control pin. An internal 2- μ A current source charges an external capacitor connected between this pin and AGND to set the output voltage ramp rate during start-up. This pin can also be used to configure the tracking feature.
3	EN	Active high enable input for the device. If not used, the EN pin can be left open, which goes high due to an internal current source.
4	AVIN	Analog input voltage supply that generates the internal bias. It is recommended to connect PVIN to AVIN through a low pass RC filter to minimize the influence of input rail ripple and noise on the analog control circuitry.
5,6,7	PVIN	Input voltage to the power switches inside the device. These pins should be connected together at the device. A low-ESR input capacitance should be located as close as possible to these pins.
8,9,10	PGND	Power ground pins for the internal power switches
11-16	SW	Switch node pins. These pins should be tied together locally and connected to the filter inductor.
17	PGOOD	Open-drain power good indicator
18	COMP	Compensation pin is connected to the output of the voltage loop error amplifier
19	FB	Feedback pin is connected to the inverting input of the voltage loop error amplifier
20	AGND	Quiet analog ground for the internal reference and bias circuitry
EP	Exposed Pad	Exposed metal pad on the underside of the package with an electrical and thermal connection to PGND. TI recommends connecting this pad to the PC board ground plane in order to improve thermal dissipation.

6 Specifications

6.1 Absolute Maximum Ratings

See

PVIN ⁽¹⁾ , AVIN to GND	–0.3 V to +6 V
SW ⁽²⁾ , EN, FB, COMP, PGOOD, SS/TRK to GND	–0.3 V to PVIN + 0.3 V
Storage temperature	–65°C to 150°C
Lead temperature (soldering, 10 s)	260°C

- (1) The PVIN pin can tolerate transient voltages up to 6.5 V for a period of up to 6 ns. These transients can occur during the normal operation of the device.
- (2) The SW pin can tolerate transient voltages up to 9.0 V for a period of up to 6 ns, and –1 V for a duration of 4 ns. These transients can occur during the normal operation of the device.

6.2 ESD Ratings

			VALUE	UNIT
V _(ESD)	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	±2000	V

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Ratings

See ⁽¹⁾

PVIN, AVIN to GND	+2.95 V to +5.5 V
Junction temperature	–40°C to +125°C
θ _{JA} ⁽²⁾	24°C/W

- (1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Recommended operating ratings indicate conditions for which the device is intended to be functional, but do not ensure specific performance limits. For ensured specifications and test conditions, see the *Electrical Characteristics*.
- (2) Thermal measurements were performed on a 2-inch × 2-inch, 4-layer, 2-oz. copper outer layer, 1-oz. copper inner layer board with twelve 8-mil. vias under the EP of the device and an additional sixteen 8-mil. vias under the unexposed package.

6.4 Electrical Characteristics

Unless otherwise stated, the following conditions apply: V_{PVIN, AVIN} = 5 V. Limits in standard type are for T_J = 25°C only, limits in **boldface type** apply over the junction temperature (T_J) range of –40°C to +125°C. Minimum and maximum limits are specified through test, design, or statistical correlation. Typical values represent the most likely parametric norm at T_J = 25°C, and are provided for reference purposes only.

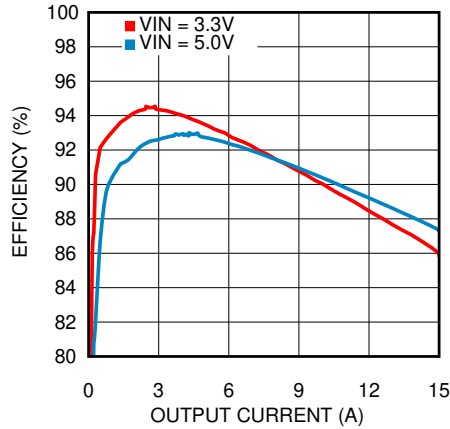
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SYSTEM						
V _{FB}	Feedback pin voltage	V _{IN} = 2.95V to 5.5V	–1%	0.6	1%	V
ΔV _{OUT} /ΔI _{OUT}	Load Regulation			0.02		%V _{OUT} /A
ΔV _{OUT} /ΔV _{IN}	Line Regulation			0.1		%V _{OUT} /V
R _{DS(on) HS}	High Side Switch On Resistance	I _{SW} = 12A		7	9.0	mΩ
R _{DS(on) LS}	Low Side Switch On Resistance	I _{SW} = 12A		4.3	6.0	mΩ
I _{CLR}	HS Rising Switch Current Limit	R _{ILIM} = 16.5 kΩ	16.5	20	23.5	A
		R _{ILIM} = 41.3 kΩ	8.5	10	11.5	
		R _{ILIM} = 130 kΩ		3.8		
I _{CLF}	LS Falling Switch Current Limit	R _{ILIM} = 16.5 kΩ		14.5		A
		R _{ILIM} = 41.3 kΩ		7.5		
		R _{ILIM} = 130 kΩ		3		
V _{ZX}	Zero Cross Voltage		–8	3	12	mV
I _Q	Operating Quiescent Current			1.5	3	mA
I _{SD}	Shutdown Quiescent Current	V _{EN} = 0V		50	70	μA

Unless otherwise stated, the following conditions apply: $V_{PVIN, AVIN} = 5\text{ V}$. Limits in standard type are for $T_J = 25^\circ\text{C}$ only, limits in **boldface type** apply over the junction temperature (T_J) range of -40°C to $+125^\circ\text{C}$. Minimum and maximum limits are specified through test, design, or statistical correlation. Typical values represent the most likely parametric norm at $T_J = 25^\circ\text{C}$, and are provided for reference purposes only.

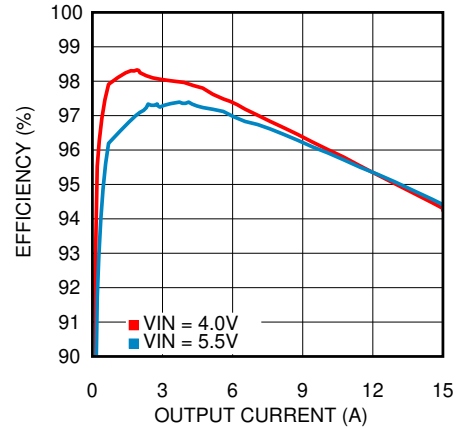
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SYSTEM						
V_{UVLO}	AVIN Under Voltage Lockout	AVIN Rising	2.45	2.7	2.95	V
$V_{UVLOHYS}$	AVIN Under Voltage Lockout Hysteresis		140	200	280	mV
$V_{TRACKOS}$	SS/TRACK PIN accuracy ($V_{SS} - V_{FB}$)	$0 < V_{TRACK} < 0.55\text{V}$	-10	6	20	mV
I_{SS}	Soft-Start Pin Source Current		1.3	1.9	2.5	μA
t_{INTSS}	Internal Soft-Start Ramp to Vref	$C_{SS} = 0$	350	500	675	μs
$t_{RESETSS}$	Device reset to soft-start ramp		50	110	200	μs
OSCILLATOR						
f_{OSC}	Switching Frequency		475	500	525	kHz
$t_{HSBLANK}$	HS OCP blanking time	Rising edge of SW to I_{CLR} comparison		55		ns
$t_{LSBLANK}$	LS OCP blanking time	Falling edge of SW to I_{CLF} comparison		400		ns
$t_{ZXBLANK}$	Zero Cross blanking time	Falling edge of SW to V_{ZX} comparison		120		ns
t_{MINON}	Minimum HS on-time			140		ns
ΔV_{RAMP}	PWM Ramp p-p Voltage			0.8		V
ERROR AMPLIFIER						
V_{OL}	Error Amplifier Open Loop Voltage Gain	$I_{COMP} = -65\mu\text{A}$ to 1mA		95		dBV/V
GBW	Error Amplifier Gain-Bandwidth Product			11		MHz
I_{FB}	Feedback Pin Bias Current	$V_{FB} = 0.6\text{V}$		1		nA
$I_{COMPSRC}$	COMP Output Source Current			1		mA
$I_{COMPSINK}$	COMP Output Sink Current			65		μA
POWERGOOD						
V_{OVP}	Overvoltage Protection Rising Threshold	V_{FB} Rising	105	112.5	120	$\%V_{FB}$
V_{OVPHYS}	Overvoltage Protection Hysteresis	V_{FB} Falling		2		$\%V_{FB}$
V_{UVP}	Undervoltage Protection Rising Threshold	V_{FB} Rising	82	90	97	$\%V_{FB}$
V_{UVPHYS}	Undervoltage Protection Hysteresis	V_{FB} Falling		2.5		$\%V_{FB}$
t_{PGDGL}	PGOOD Deglitch Low (OVP/UVP Condition Duration to PGOOD Falling)			15		μs
t_{PGDGH}	PGOOD Deglitch High (minimum low pulse)			12		μs
R_{PD}	PGOOD Pulldown Resistance		10	20	40	Ω
$I_{PGOODLEAK}$	PGOOD Leakage Current	$V_{PGOOD} = 5\text{V}$		1		nA
LOGIC						
V_{IHENR}	EN Pin Rising Threshold	V_{EN} Rising	1.20	1.35	1.45	V
V_{ENHYS}	EN Pin Hysteresis		50	110	180	mV
I_{EN}	EN Pin Pullup Current	$V_{EN} = 0\text{V}$		2		μA
THERMAL SHUTDOWN						
$T_{THERMSD}$	Thermal Shutdown			165		$^\circ\text{C}$
$T_{THERMSDHYS}$	Thermal Shutdown Hysteresis			10		$^\circ\text{C}$

6.5 Typical Characteristics

Unless otherwise specified: $V_{IN} = 5\text{ V}$, $V_{OUT} = 1.2\text{ V}$, $L = 0.56\text{ }\mu\text{H}$ ($1.8\text{-m}\Omega\text{ }R_{DCR}$), $C_{SS} = 33\text{ nF}$, $T_A = 25^\circ\text{C}$ for efficiency curves, loop gain plots and waveforms, and $T_J = 25^\circ\text{C}$ for all others.



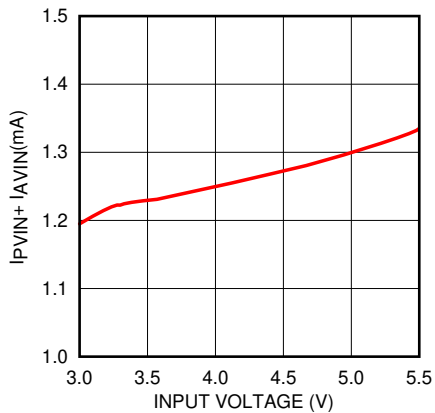
6-1. Efficiency



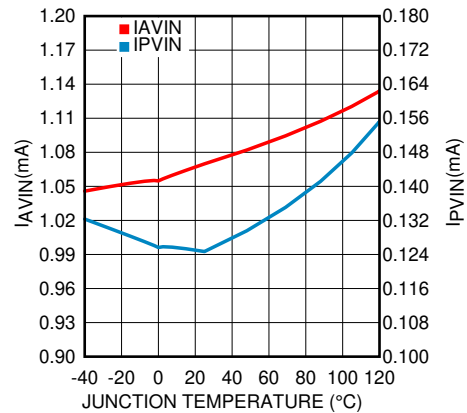
$V_{OUT} = 3.3\text{ V}$

Inductor P/N SER2010-02MLD

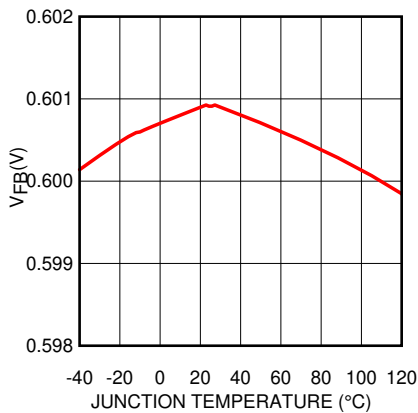
6-2. Efficiency



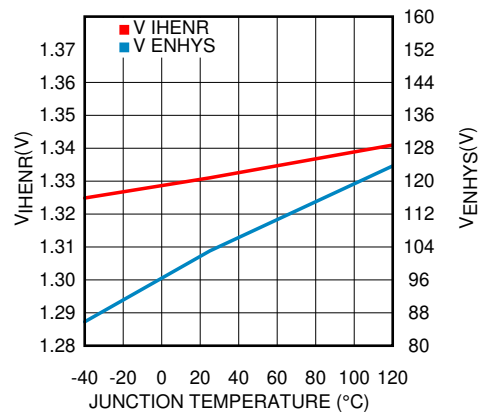
6-3. Non-Switching I_{QTOTAL} vs V_{IN}



6-4. Non-Switching I_{AVIN} and I_{PVIN} vs Temperature



6-5. V_{FB} vs Temperature



6-6. Enable Threshold and Hysteresis vs Temperature

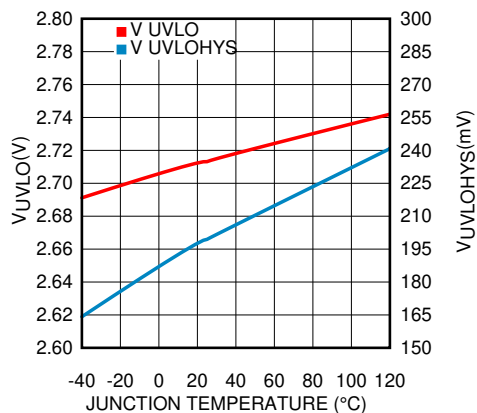


Figure 6-7. UVLO Threshold and Hysteresis vs Temperature

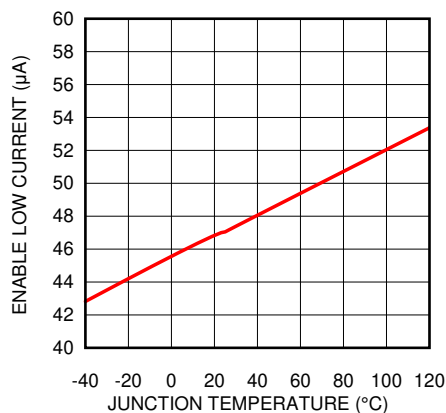


Figure 6-8. Enable Low Current vs Temperature

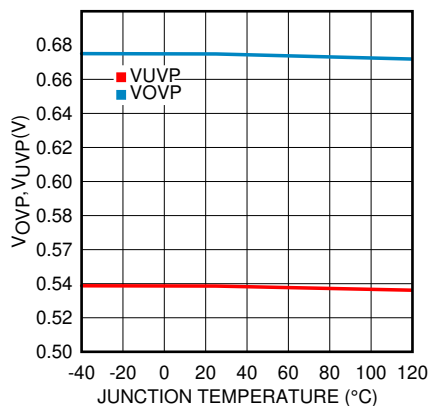


Figure 6-9. OVP/UVP Threshold vs Temperature

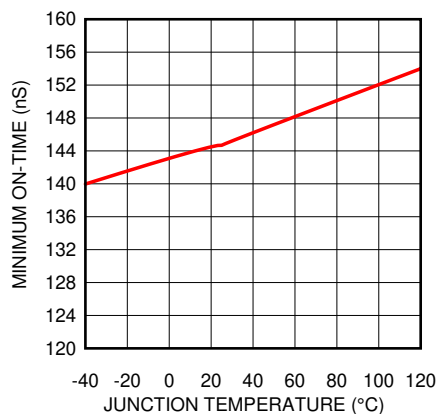


Figure 6-10. Minimum On-Time vs Temperature

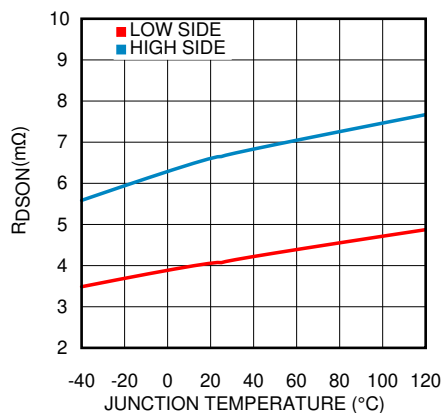


Figure 6-11. FET Resistance vs Temperature

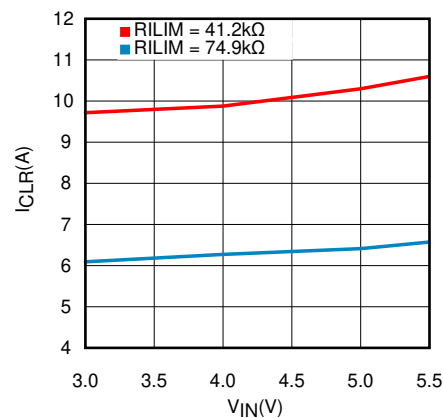


Figure 6-12. Peak Current Limit (ICLR) vs VIN

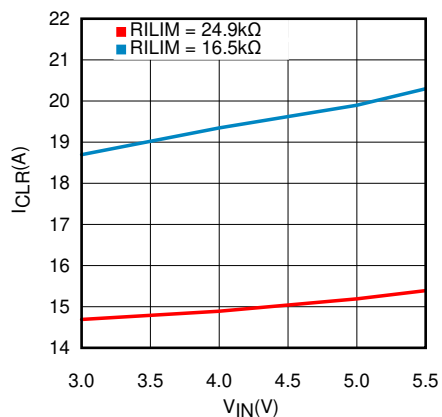
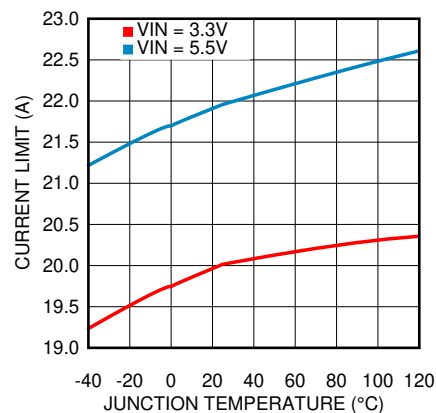
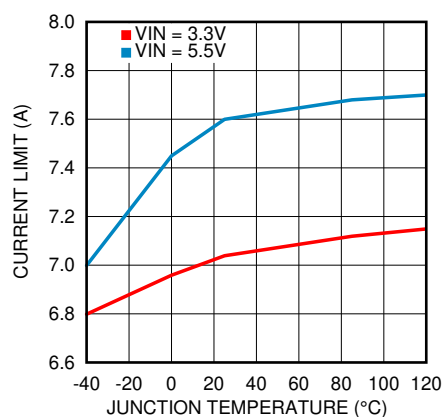


FIG 6-13. Peak Current Limit (I_{CLR}) vs V_{IN}



$R_{ILIM} = 10 k\Omega$

FIG 6-14. Peak Current Limit (I_{CLR}) vs Temperature



$R_{ILIM} = 61.9 k\Omega$

FIG 6-15. Peak Current Limit (I_{CLR}) vs Temperature

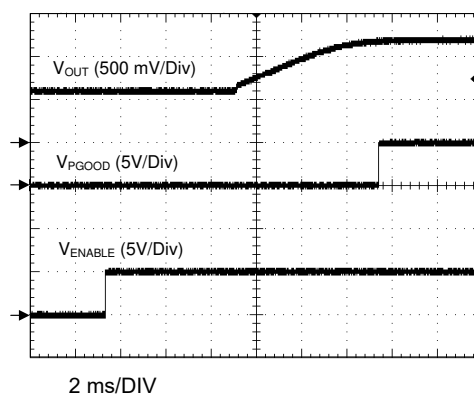


FIG 6-16. Start-up With Prebiased Output

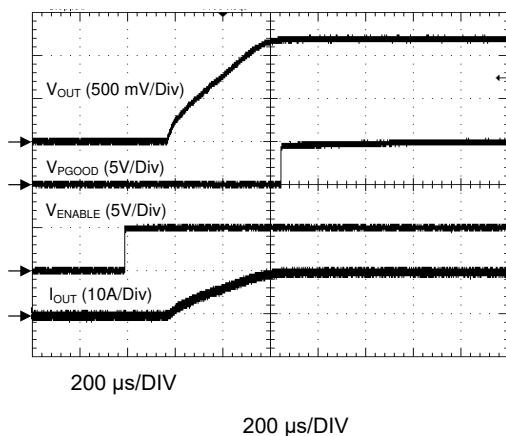


FIG 6-17. Start-up With SS/TRK Open Circuit

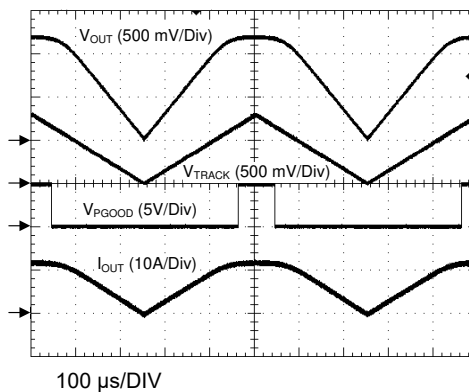
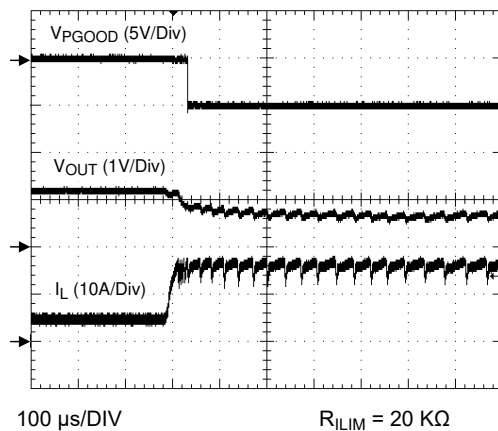


FIG 6-18. Start-up With Applied Track Signal



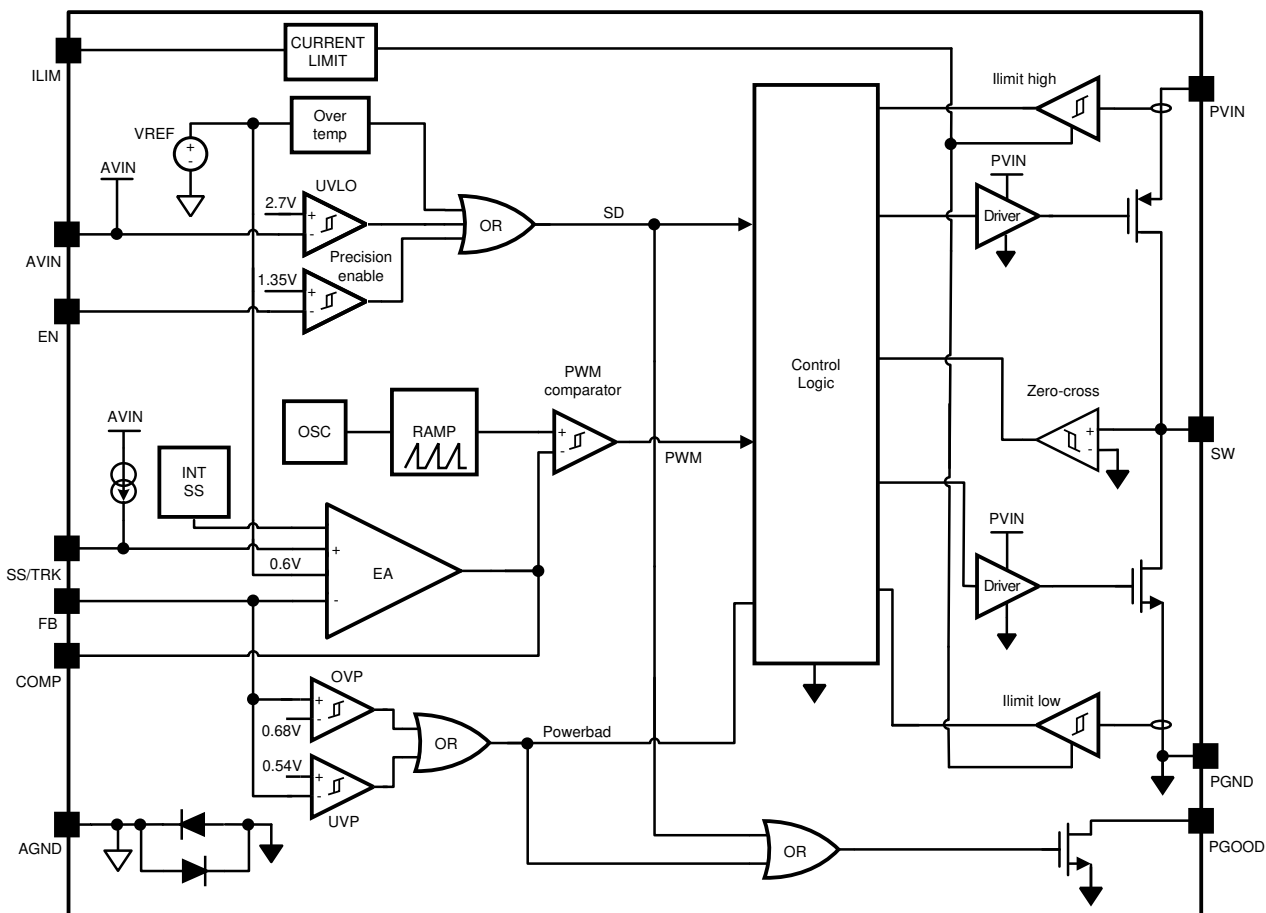

6-19. Output Overcurrent Condition

7 Detailed Description

7.1 Overview

The LM21215 switching regulator features all of the functions necessary to implement an efficient low voltage buck regulator using a minimum number of external components. This easy-to-use regulator features two integrated switches and is capable of supplying up to 15 A of continuous output current. The regulator utilizes voltage mode control with trailing edge modulation to optimize stability and transient response over the entire output voltage range. The precision internal voltage reference allows the output to be set as low as 0.6 V. Fault protection features include: current limiting, thermal shutdown, overvoltage protection, and shutdown capability. The device is available in the 20-pin HTSSOP package featuring an exposed pad to aid thermal dissipation. The LM21215 can be used in numerous applications to efficiently step-down from a 5-V or 3.3-V bus.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Precision Enable

The enable (EN) pin allows the output of the device to be enabled or disabled with an external control signal. This pin is a precision analog input that enables the device when the voltage exceeds 1.35 V (typical). The EN pin has 110 mV of hysteresis and disables the output when the enable voltage falls below 1.24 V (typical). If the EN pin is not used, it can be left open, and will be pulled high by an internal 2- μ A current source. Since the enable pin has a precise turn-on threshold, it can be used along with an external resistor divider network from VIN to configure the device to turn on at a precise input voltage.

7.3.2 UVLO

The LM21215 has a built-in undervoltage lockout protection circuit that keeps the device from switching until the input voltage reaches 2.7 V (typical). The UVLO threshold has 200 mV of hysteresis that keeps the device from responding to power-on glitches during start-up. If desired, the turn-on point of the supply can be changed by using the precision enable pin and a resistor divider network connected to VIN as shown in [Figure 8-3](#) in the design guide.

7.3.3 Current Limit

The LM21215 has programmable current limit protection to avoid dangerous current levels through the power FETs and inductor. A current limit condition is met when the current through the high side FET exceeds the rising current limit level (I_{CLR}). The control circuitry will respond to this event by turning off the high-side FET and turning on the low-side FET. This forces a negative voltage on the inductor, thereby causing the inductor current to decrease. The high-side FET will not conduct again until the lower current limit level (I_{CLF}) is sensed on the low-side FET. At this point, the device will resume normal switching.

A current limit condition will cause the internal soft-start voltage to ramp downward. After the internal soft-start ramps below the feedback (FB) pin voltage (nominally 0.6 V), FB will begin to ramp downward, as well. This voltage foldback will limit the power consumption in the device, thereby protecting the device from continuously supplying power to the load under a condition that does not fall within the device SOA. After the current limit condition is cleared, the internal soft-start voltage will ramp up again. [Figure 7-1](#) shows current limit behavior with V_{SS} , V_{FB} , V_{OUT} , and V_{SW} .

7.3.4 Short-Circuit Protection

In the unfortunate event that the output is shorted with a low impedance to ground, the LM21215 limits the current into the short by resetting the device. A short-circuit condition is sensed by a current-limit condition coinciding with a voltage on the FB pin that is lower than 100 mV. When this condition occurs, the device begins its reset sequence, turning off both power FETs and discharging the soft-start capacitor after $t_{RESETSS}$ (nominally 110 μ s). The device will then attempt to restart. If the short-circuit condition still exists, it will reset again, and repeat until the short-circuit is cleared. The reset prevents excess current flowing through the FETs in a highly inefficient manner, potentially causing thermal damage to the device or the bus supply.

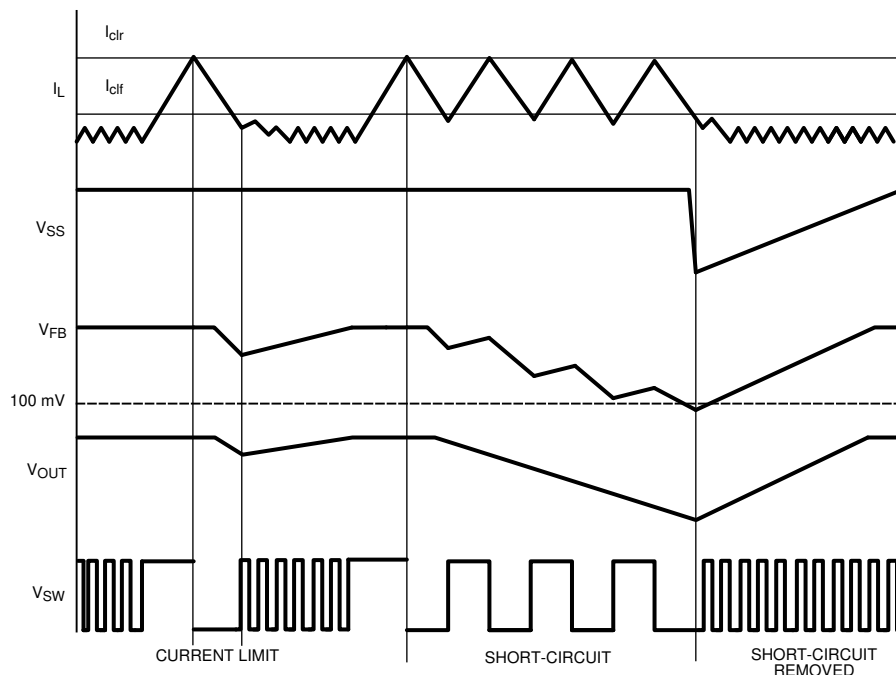


Figure 7-1. Current Limit Conditions

7.3.5 Thermal Protection

Internal thermal shutdown circuitry is provided to protect the integrated circuit in the event that the maximum junction temperature is exceeded. When activated, typically at 165°C, the LM21215 tri-states the power FETs and resets soft start. After the junction cools to approximately 155°C, the device starts up using the normal start-up routine. This feature is provided to prevent catastrophic failures from accidental device overheating. Note that thermal limit will not stop the die from operating above the specified maximum operating temperature, 125°C. The die should be kept under 125°C to ensure correct operation.

7.3.6 Light Load Operation

The LM21215 offers increased efficiency when operating at light loads. Whenever the load current is reduced to a point where the peak to peak inductor ripple current is greater than two times the load current, the device will enter the diode emulation mode, preventing significant negative inductor current. The point at which this occurs is the critical conduction boundary and can be calculated with 式 1:

$$I_{\text{BOUNDARY}} = \frac{(V_{\text{IN}} - V_{\text{OUT}}) \times D}{2 \times L \times f_{\text{SW}}} \quad (1)$$

It can be seen that in diode emulation mode, whenever the inductor current reaches zero, the SW node becomes high impedance. Ringing will occur on this pin as a result of the LC tank circuit formed by the inductor and the parasitic capacitance at the node. If this ringing is of concern, an additional RC snubber circuit can be added from the switch node to ground.

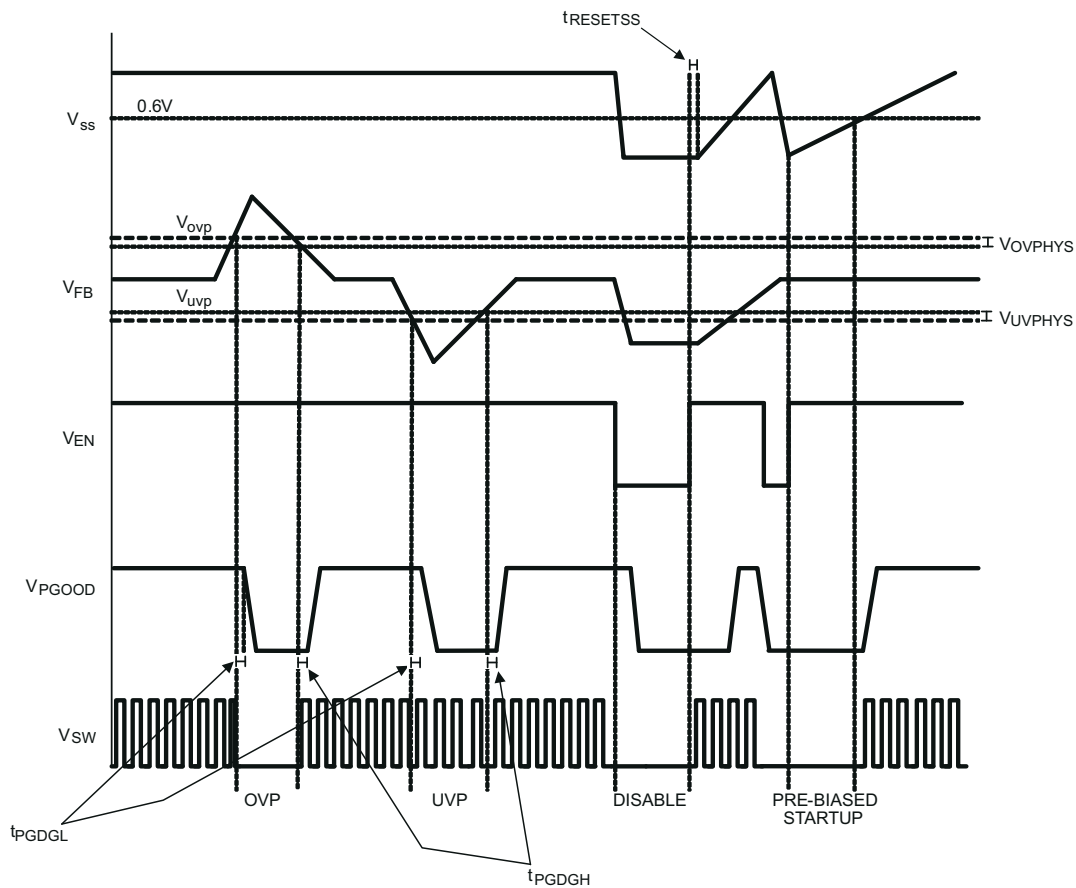
At very light loads, usually below 100 mA, several pulses can be skipped in between switching cycles, effectively reducing the switching frequency and further improving light-load efficiency.

7.3.7 Power Good Flag

The PGOOD pin provides the user with a way to monitor the status of the LM21215. In order to use the PGOOD pin, the application must provide a pullup resistor to a desired DC voltage (in other words, V_{IN}). PGOOD will respond to a fault condition by pulling the PGOOD pin low with the open-drain output. PGOOD pulls low on the following conditions:

- V_{FB} moves above or below the V_{OVP} or V_{UVP} , respectively.
- The enable pin (EN) is brought below the enable threshold.
- The device enters a prebiased output condition ($V_{\text{FB}} > V_{\text{SS}}$).

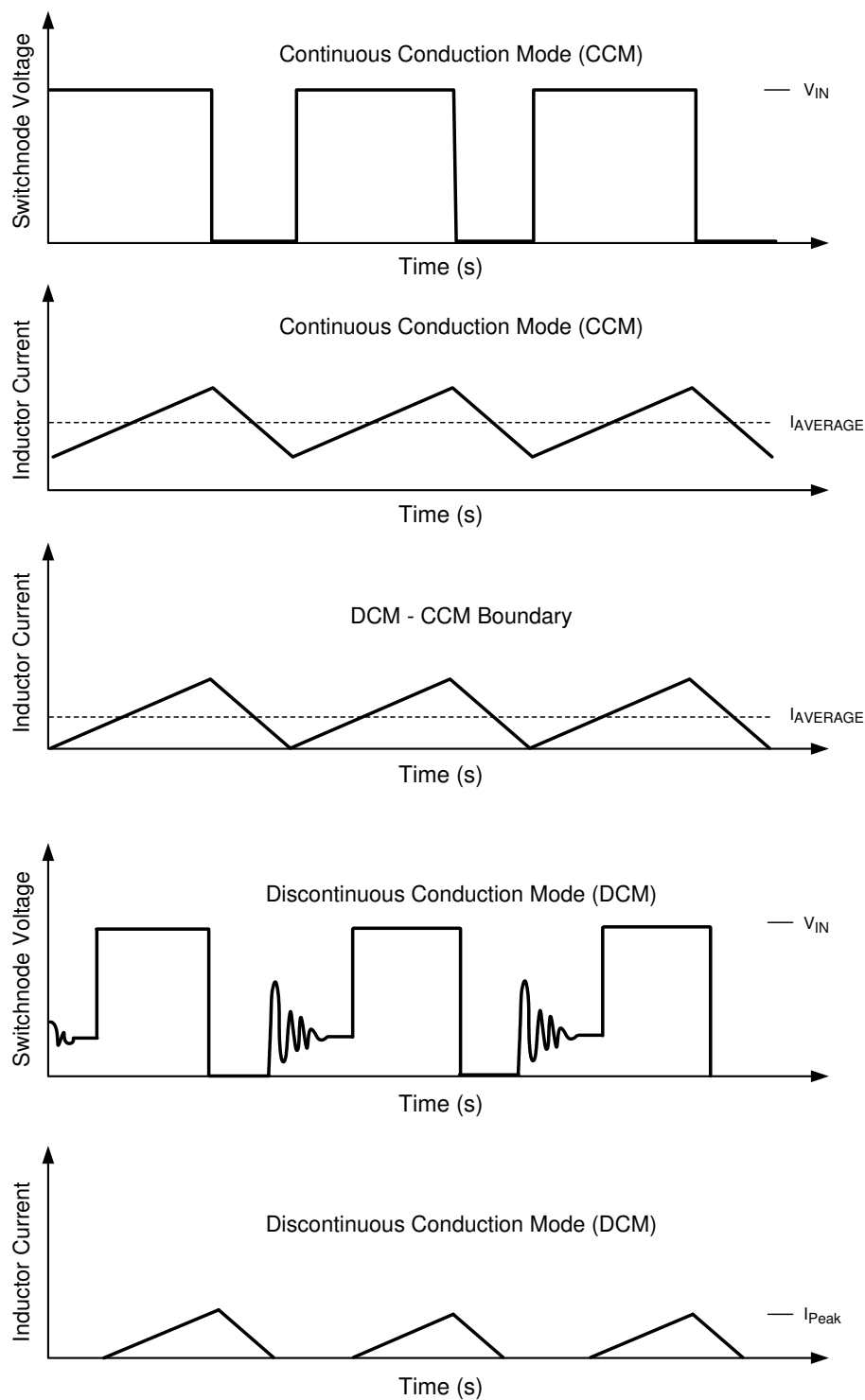
Figure 7-2 shows the conditions that will cause PGOOD to fall.




7-2. PGOOD Conditions

7.4 Device Functional Modes

Several diagrams are shown in illustrating continuous conduction mode (CCM), discontinuous conduction mode (DCM), and the boundary condition.



7-3. Modes Of Operation for LM21215

8 Application and Implementation

Note

以下のアプリケーション情報は、TI の製品仕様に含まれるものではなく、TI ではその正確性または完全性を保証いたしません。個々の目的に対する製品の適合性については、お客様の責任で判断していただくことになります。お客様は自身の設計実装を検証テストすることで、システムの機能を確認する必要があります。

8.1 Application Information

The LM21212-2 switching regulator features all of the functions necessary to implement an efficient low voltage buck regulator using a minimum number of external components. This easy-to-use regulator features two integrated switches and is capable of supplying up to 12 A of continuous output current. The regulator utilizes voltage mode control with trailing edge modulation to optimize stability and transient response over the entire output voltage range.

8.2 Typical Application

8.2.1 Typical Application 1

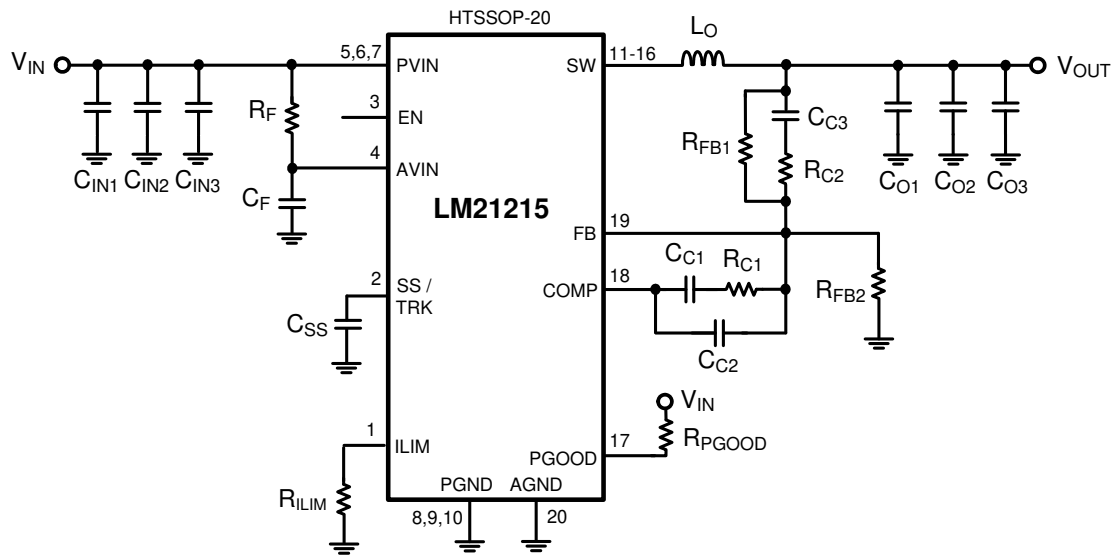


図 8-1. Typical Application Schematic 1

8.2.1.1 Design Requirements

表 8-1. Bill Of Materials ($V_{IN} = 3.3\text{ V}$ – 5.5 V , $V_{OUT} = 1.2\text{ V}$, $I_{OUT} = 15\text{ A}$)

ID	DESCRIPTION	VENDOR	PART NUMBER	QUANTITY
C_F	CAP, CERM, 1 μF , 10 V, $\pm 10\%$, X7R, 0603	MuRata	GRM188R71A105KA61D	1
C_{IN1} , C_{IN2} , C_{IN3} , C_{O1} , C_{O2} , C_{O3}	CAP, CERM, 100 μF , 6.3 V, $\pm 20\%$, X5R, 1206	MuRata	GRM31CR60J107ME39L	6
C_{C1}	CAP, CERM, 1800 pF, 50 V, $\pm 5\%$, C0G/NP0, 0603	TDK	C1608C0G1H182J	1
C_{C2}	CAP, CERM, 68 pF, 50 V, $\pm 5\%$, C0G/NP0, 0603	TDK	C1608C0G1H680J	1
C_{C3}	CAP, CERM, 820 pF, 50 V, $\pm 5\%$, C0G/NP0, 0603	TDK	C1608C0G1H821J	1
C_{SS}	CAP, CERM, 0.033 μF , 16 V, $\pm 10\%$, X7R, 0603	MuRata	GRM188R71C333KA01D	1
L_O	Inductor, Shielded Drum Core, Powdered Iron, 560 nH, 27.5 A, 0.0018 Ω , SMD	Vishay-Dale	IHLP4040DZERR56M01	1
R_F	RES, 1.0 Ω , 5%, 0.1 W, 0603	Vishay-Dale	CRCW06031R00JNEA	1
R_{C1}	RES, 9.31 k Ω , 1%, 0.1 W, 0603	Vishay-Dale	CRCW06039K31FKEA	1
R_{C2}	RES, 165 Ω , 1%, 0.1 W, 0603	Vishay-Dale	CRCW0603165RFKEA	1
R_{FB1} , R_{FB2} , R_{PGOOD}	RES, 10 k Ω , 1%, 0.1 W, 0603	Vishay-Dale	CRCW060310K0FKEA	3
R_{ILIM}	RES, 7.15 k Ω , 1%, 0.1 W, 0603	Vishay-Dale	CRCW06037K15FKEA	1

8.2.1.2 Detailed Design Procedure

8.2.1.2.1 Custom Design With WEBENCH® Tools

[Click here](#) to create a custom design using the LM21215 device with the WEBENCH® Power Designer.

1. Start by entering the input voltage (V_{IN}), output voltage (V_{OUT}), and output current (I_{OUT}) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance
- Run thermal simulations to understand board thermal performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

8.2.1.2.2 Output Voltage

The first step in designing the LM21215 application is setting the output voltage. This is done by using a voltage divider between V_{OUT} and AGND, with the middle node connected to V_{FB} . When operating under steady-state conditions, the LM21215 forces V_{OUT} so that V_{FB} is driven to 0.6 V.

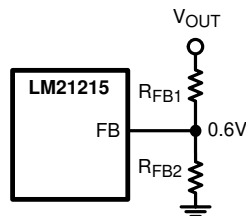


图 8-2. Setting V_{OUT}

A good starting point for the lower feedback resistor, R_{FB2} , is 10 k Ω . R_{FB1} can then be calculated with 式 2:

$$V_{OUT} = \frac{R_{FB1} + R_{FB2}}{R_{FB2}} 0.6V \quad (2)$$

8.2.1.2.3 Precision Enable

The enable (EN) pin of the LM21215 allows the output to be toggled on and off. This pin is a precision analog input. When the voltage exceeds 1.35 V, the controller will try to regulate the output voltage as long as the input voltage has exceeded the UVLO voltage of 2.7 V. There is an internal current source connected to EN so if enable is not used, the device will turn on automatically. If EN is not toggled directly, the device can be pre-programmed to turn on at a certain input voltage higher than the UVLO voltage. This can be done with an external resistor divider from AVIN to EN and EN to AGND as shown in 图 8-3.

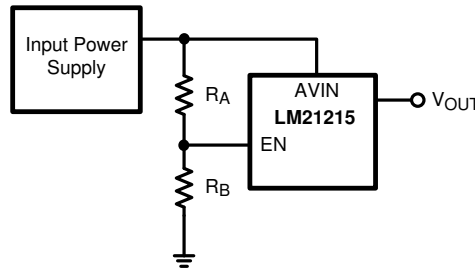


图 8-3. Enable Start-Up Through V_{IN}

The resistor values of R_A and R_B can be relatively sized to allow EN to reach the enable threshold voltage depending on the input supply voltage. With the enable current source accounted for, the equation solving for R_A is the following:

$$R_A = \frac{R_B(V_{PVIN} - 1.35V)}{1.35V - I_{EN}R_B} \quad (3)$$

where

- R_A is the resistor from V_{IN} to enable.
- R_B is the resistor from enable to ground.
- I_{EN} is the internal enable pullup current (2 μA).
- 1.35 V is the fixed precision enable threshold voltage.

Typical values for R_B range from 10 k Ω to 100 k Ω .

8.2.1.2.4 Soft Start

When EN has exceeded 1.35 V, and both PVIN and AVIN have exceeded the UVLO threshold, the LM21215 begins charging the output linearly to the voltage level dictated by the feedback resistor network. The LM21215 employs a user-adjustable soft-start circuit to lengthen the charging time of the output set by a capacitor from the soft-start pin to ground. After enable exceeds 1.35 V, an internal 2- μA current source begins to charge the soft-start capacitor. This allows the user to limit inrush currents due to a high output capacitance and not cause an overcurrent condition. Adding a soft-start capacitor can also reduce the stress on the input rail. Larger capacitor values will result in longer start-up times. Use 式 4 to approximate the size of the soft-start capacitor:

$$\frac{t_{SS} \times I_{SS}}{0.6V} = C_{SS} \quad (4)$$

where

- I_{SS} is nominally 2 μA .

- t_{SS} is the desired start-up time.

If V_{IN} is higher than the UVLO level and enable is toggled high the soft start sequence begins. There is a small delay between enable transitioning high and the beginning of the soft start sequence. This delay allows the LM21215 to initialize its internal circuitry. Once the output has charged to 90% of the nominal output voltage the power-good flag transitions high. This behavior is illustrated in [Figure 8-4](#).

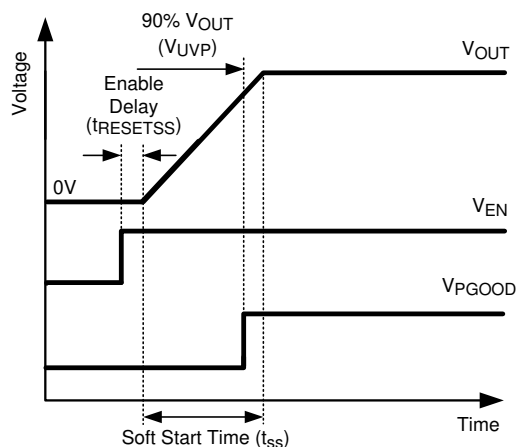


Figure 8-4. Soft-Start Timing

As shown above, the size of the capacitor is influenced by the nominal feedback voltage level 0.6 V, the soft-start charging current, I_{SS} (2 μ A), and the desired soft-start time. If no soft-start capacitor is used, then the LM21215 defaults to a minimum start-up time of 500 μ s. The LM21215 does not start up faster than 500 μ s. When enable is cycled or the device enters UVLO, the charge developed on the soft-start capacitor is discharged to reset the start-up process. This also happens when the device enters short circuit mode from an overcurrent event.

8.2.1.2.5 Inductor Selection

The inductor (L) used in the application influences the ripple current and the efficiency of the system. The first selection criteria is to define a ripple current, ΔI_L . In a buck converter, it is typically selected to run between 20% to 30% of the maximum output current. [Figure 8-5](#) shows the ripple current in a standard buck converter operating in continuous conduction mode. Larger ripple current results in a smaller inductance value, which will lead to a lower series resistance in the inductor and improved efficiency. However, larger ripple current will also cause the device to operate in discontinuous conduction mode at a higher average output current.

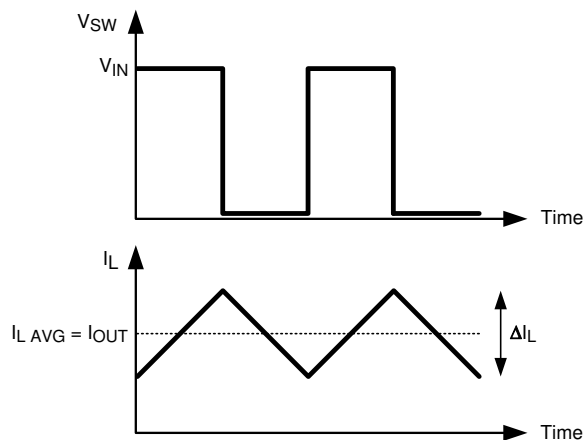


Figure 8-5. Switch And Inductor Current Waveforms

Once the ripple current has been determined, the appropriate inductor size can be calculated using 式 5:

$$L = \frac{(V_{IN} - V_{OUT}) \cdot D}{\Delta I_L \cdot f_{SW}} \quad (5)$$

8.2.1.2.6 Output Capacitor Selection

The output capacitor, C_{OUT} , filters the inductor ripple current and provides a source of charge for transient load conditions. A wide range of output capacitors can be used with the LM21215 that provide various advantages. The best performance is typically obtained using ceramic, SP, or OSCON type chemistries. Typical trade-offs are that the ceramic capacitor provides extremely low ESR to reduce the output ripple voltage and noise spikes, while the SP and OSCON capacitors provide a large bulk capacitance in a small volume for transient loading conditions.

When selecting the value for the output capacitor, the two performance characteristics to consider are the output voltage ripple and transient response. The output voltage ripple can be approximated by using 式 6:

$$\Delta V_{OUT} \approx \Delta I_L \times \left[R_{ESR} + \frac{1}{8 \times f_{SW} \times C_{OUT}} \right] \quad (6)$$

where

- ΔV_{OUT} (V) is the amount of peak-to-peak voltage ripple at the power supply output.
- R_{ESR} (Ω) is the series resistance of the output capacitor.
- f_{SW} (Hz) is the switching frequency.
- C_{OUT} (F) is the output capacitance used in the design.

The amount of output ripple that can be tolerated is application specific, however, a general recommendation is to keep the output ripple less than 1% of the rated output voltage. Keep in mind ceramic capacitors are sometimes preferred because they have very low ESR, however, depending on package and voltage rating of the capacitor, the value of the capacitance can drop significantly with applied voltage. The output capacitor selection will also affect the output voltage droop during a load transient. The peak droop on the output voltage during a load transient is dependent on many factors, however, an approximation of the transient droop ignoring loop bandwidth can be obtained using 式 7:

$$V_{DROOP} = \Delta I_{OUTSTEP} \times R_{ESR} + \frac{L \times \Delta I_{OUTSTEP}^2}{C_{OUT} \times (V_{IN} - V_{OUT})} \quad (7)$$

where

- C_{OUT} (F) is the minimum required output capacitance.
- L (H) is the value of the inductor.
- V_{DROOP} (V) is the output voltage drop ignoring loop bandwidth considerations.
- $\Delta I_{OUTSTEP}$ (A) is the load step change.
- R_{ESR} (Ω) is the output capacitor ESR.
- V_{IN} (V) is the input voltage.
- V_{OUT} (V) is the set regulator output voltage.

Examine both the tolerance and voltage coefficient of the capacitor when designing for a specific output ripple or transient droop target.

8.2.1.2.7 Input Capacitor Selection

Quality input capacitors are necessary to limit the ripple voltage at the V_{IN} pin while supplying most of the switch current during the on time. Additionally, they help minimize input voltage droop in an output current transient condition. In general, it is recommended to use a ceramic capacitor for the input as it provides both a low impedance and small footprint. Use of a high grade dielectric for the ceramic capacitor, such as X5R or X7R, will

provide improved overtemperature performance and also minimize the DC voltage derating that occurs with Y5V capacitors. The input capacitors C_{IN1} and C_{IN2} must be placed as close as possible to the PVIN and PGND pins.

Select non-ceramic input capacitors for RMS current rating and minimum ripple voltage. A good approximation for the required ripple current rating is given by the relationship:

$$I_{IN-RMS} = I_{OUT} \sqrt{D(1-D)} \quad (8)$$

As indicated by the RMS ripple current equation, the highest requirement for RMS current rating occurs at 50% duty cycle. For this case, the RMS ripple current rating of the input capacitor should be greater than half the output current. For best performance, low-ESR ceramic capacitors should be placed in parallel with higher capacitance capacitors to provide the best input filtering for the device.

When operating at low input voltages (3.3 V or lower), additional capacitance can be necessary to protect from triggering an undervoltage condition on an output current transient. This will depend on the impedance between the input voltage supply and the LM21215, as well as the magnitude and slew rate of the output transient.

The AVIN pin requires a 1- μ F ceramic capacitor to AGND and a 1- Ω resistor to PVIN. This RC network filters inherent noise on PVIN from the sensitive analog circuitry connected to AVIN.

8.2.1.2.8 Programmable Current Limit

A resistor from the ILIM pin to GND sets the internal current limit on the LM21215. Program the current limit so that the peak inductor current (I_L) does not trigger the current limit in normal operation. This requires setting the resistor from the ILIM pin to GND (R_{ILIM}) to the appropriate value to allow the maximum ripple current, ΔI_{LMAX} plus the DC output current through the high-side FET during normal operation. The maximum ripple current can be described as:

$$\begin{aligned} &\text{For } D > 0.5 \\ \Delta I_{LMAX} &= \frac{(V_{INMAX} - V_{OUTMIN}) \cdot V_{OUTMIN}}{L_{MIN} \cdot f_{SWMIN} \cdot V_{INMAX}} \\ &\text{For } D < 0.5 \\ \Delta I_{LMAX} &= \frac{(V_{INMIN} - V_{OUTMAX}) \cdot V_{OUTMAX}}{L_{MIN} \cdot f_{SWMIN} \cdot V_{INMIN}} \end{aligned} \quad (9)$$

where

- V_{INMAX} , V_{INMIN} , V_{OUTMAX} , V_{OUTMIN} , L_{MIN} , and F_{SWMIN} are the respective maximum and minimum conditions of the system as defined by the component tolerance and device variation.

From this, the maximum allowable current through the high-side FET (I_{HSMAX}) of device can be described as:

$$I_{HSMAX} = \frac{\Delta I_{LMAX}}{2} + I_{DCMAX} \quad (10)$$

where

- I_{OUTMAX} is the maximum defined DC output current, up to 15 A.

Once the I_{HSMAX} value has been determined, a nominal value of the R_{ILIM} resistor can be calculated as follows:

$$R_{ILIM} (k\Omega) = \frac{582.4}{I_{HSMAX}} - 14.2 \quad (11)$$

where

- R_{ILIM} value is the nominal resistance necessary for the given I_{HSMAX} value.

A conservative design should also take into account the device variation over V_{IN} and temperature, as seen in the [Electrical Characteristics](#) for the I_{CLR} parameter and the typical performance characteristics. These variations can cause the I_{HSMAX} value to increase, depending on the range of the input voltage and junction temperature.

8.2.1.2.9 Control Loop Compensation

The LM21215 incorporates a high bandwidth amplifier between the FB and COMP pins to allow the user to design a compensation network that matches the application. This section will walk through the various steps in obtaining the open loop transfer function.

There are three main blocks of a voltage mode buck switcher that the power supply designer must consider when designing the control system: the power train, modulator, and the compensated error amplifier. A closed loop diagram is shown in [Figure 8-6](#).

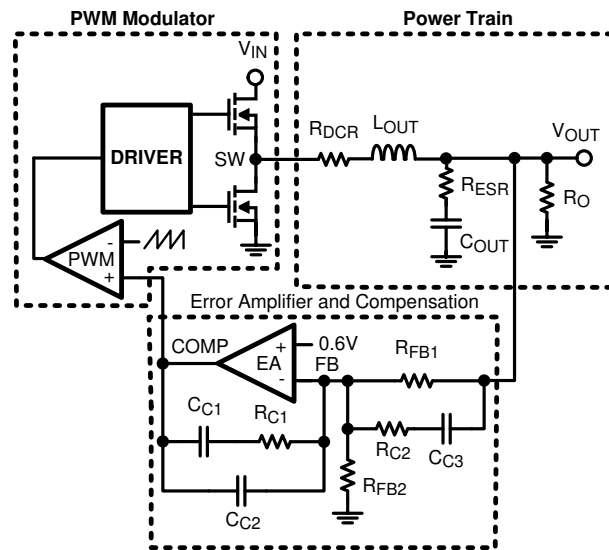


Figure 8-6. Loop Diagram

The power train consists of the output inductor (L) with DCR (DC resistance R_{DCR}), output capacitor (C_O) with ESR (effective series resistance R_{ESR}), and load resistance (R_O). The error amplifier (EA) constantly forces FB to 0.6 V. The passive compensation components around the error amplifier help maintain system stability. The modulator creates the duty cycle by comparing the error amplifier signal with an internally generated ramp set at the switching frequency.

There are three transfer functions that must be taken into consideration when obtaining the total open loop transfer function: COMP to SW (modulator), SW to V_{OUT} (power train), and V_{OUT} to COMP (error amplifier). The COMP to SW transfer function is simply the gain of the PWM modulator.

$$G_{PWM} = \frac{V_{in}}{\Delta V_{ramp}} \quad (12)$$

where

- ΔV_{RAMP} is the oscillator peak-to-peak ramp voltage (nominally 0.8 V).

The SW to COMP transfer function includes the output inductor, output capacitor, and output load resistance. The inductor and capacitor create two complex poles at a frequency described by:

$$f_{LC} = \frac{1}{2\pi} \sqrt{\frac{R_O + R_{DCR}}{L_{OUT}C_{OUT}(R_O + R_{ESR})}} \quad (13)$$

In addition to two complex poles, a left half plane zero is created by the output capacitor ESR located at a frequency described by:

$$f_{\text{esr}} = \frac{1}{2\pi C_o R_{\text{esr}}} \quad (14)$$

A Bode plot showing the power train response can be seen in [Figure 8-7](#).

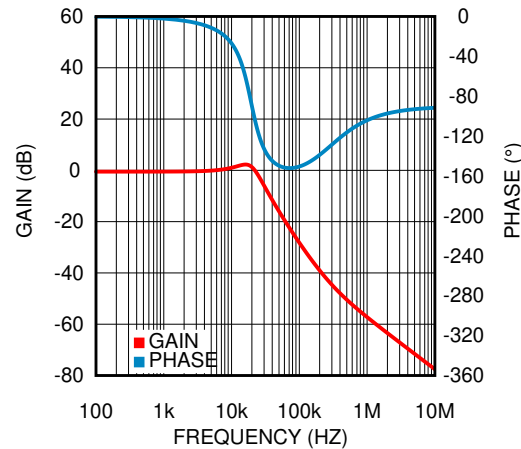


Figure 8-7. Power Train Bode Plot

The complex poles created by the output inductor and capacitor cause a 180° phase shift at the resonant frequency as seen in [Figure 8-7](#). The phase is boosted back up to -90° due to the output capacitor ESR zero. The 180° phase shift must be compensated out and phase boosted through the error amplifier to stabilize the closed loop response. The compensation network shown around the error amplifier in [Figure 8-6](#) creates two poles, two zeros, and a pole at the origin. Placing these poles and zeros at the correct frequencies stabilizes the closed loop response. The Compensated Error Amplifier transfer function is:

$$G_{\text{EA}} = K_m \frac{\left(\frac{s}{2\pi f_{Z1}} + 1\right)\left(\frac{s}{2\pi f_{Z2}} + 1\right)}{s\left(\frac{s}{2\pi f_{P1}} + 1\right)\left(\frac{s}{2\pi f_{P2}} + 1\right)} \quad (15)$$

The pole located at the origin gives high open loop gain at DC, translating into improved load regulation accuracy. This pole occurs at a very low frequency due to the limited gain of the error amplifier, however, it can be approximated at DC for the purposes of compensation. The other two poles and two zeros can be located accordingly to stabilize the voltage mode loop depending on the power stage complex poles and Q. [Figure 8-8](#) is an illustration of what the Error Amplifier Compensation transfer function will look like.

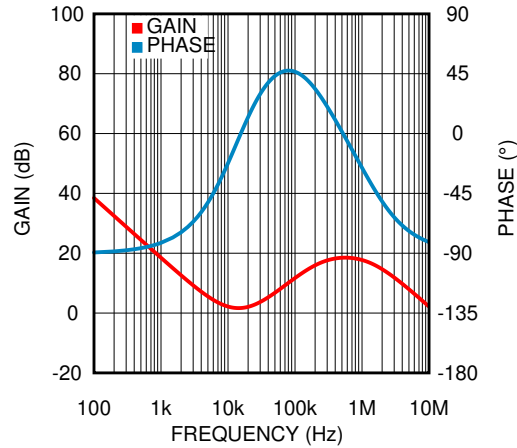


图 8-8. Type 3 Compensation Network Bode Plot

As seen in 图 8-8, the two zeros ($f_{LC}/2$, f_{LC}) in the compensation network give a phase boost. This will cancel out the effects of the phase loss from the output filter. The compensation network also adds two poles to the system. One pole should be located at the zero caused by the output capacitor ESR (f_{ESR}), and the other pole must be at half the switching frequency ($f_{SW}/2$) to roll off the high frequency response. The dependency of the pole and zero locations on the compensation components is described in 式 16.

$$\begin{aligned} f_{Z1} &= \frac{f_{LC}}{2} = \frac{1}{2\pi R_{C1} C_{C1}} \\ f_{Z2} &= f_{LC} = \frac{1}{2\pi (R_{C1} + R_{FB1}) C_{C3}} \\ f_{P1} &= f_{ESR} = \frac{1}{2\pi R_{C2} C_{C3}} \\ f_{P2} &= \frac{f_{SW}}{2} = \frac{C_{C1} + C_{C2}}{2\pi R_{C1} C_{C1} C_{C2}} \end{aligned} \quad (16)$$

An example of the step-by-step procedure to generate compensation component values using the typical application setup, is given. The parameters needed for the compensation values are given in 表 8-2.

表 8-2. Required Parameters for Compensation Values

PARAMETER	VALUE
V_{IN}	5 V
V_{OUT}	1.2 V
I_{OUT}	15 A
$f_{CROSSOVER}$	100 kHz
L	0.56 μ H
R_{DCR}	1.8 m Ω
C_O	150 μ F
R_{ESR}	1.0 m Ω
ΔV_{RAMP}	0.8 V
f_{SW}	500 kHz

where ΔV_{RAMP} is the oscillator peak-to-peak ramp voltage (nominally 0.8 V), and $f_{CROSSOVER}$ is the frequency at which the open-loop gain is a magnitude of 1. It is recommended that the $f_{CROSSOVER}$ not exceed one-fifth of the switching frequency. The output capacitance, C_O , depends on capacitor chemistry and bias voltage. For multi-

layer ceramic capacitors (MLCC), the total capacitance will degrade as the DC bias voltage is increased. Measuring the actual capacitance value for the output capacitors at the output voltage is recommended to accurately calculate the compensation network. The example given here is the total output capacitance using the three MLCC output capacitors biased at 1.2 V, as seen in [Figure 8-1](#). Note that it is more conservative, from a stability standpoint, to err on the side of a smaller output capacitance value in the compensation calculations rather than a larger, as this will result in a lower bandwidth but increased phase margin.

First, the value of R_{FB1} should be chosen. A typical value is 10 k Ω . From this, the value of R_{C1} can be calculated to set the mid-band gain so that the desired crossover frequency is achieved:

$$\begin{aligned}
 R_{C1} &= \frac{f_{\text{crossover}}}{f_{LC}} \cdot \frac{\Delta V_{\text{RAMP}}}{V_{IN}} \cdot R_{FB1} \\
 &= \frac{100 \text{ kHz}}{17.4 \text{ kHz}} \cdot \frac{0.8 \text{ V}}{5.0 \text{ V}} \cdot 10 \text{ k}\Omega \\
 &= 9.2 \text{ k}\Omega
 \end{aligned}
 \tag{17}$$

Next, the value of C_{C1} can be calculated by placing a zero at half of the LC double pole frequency (f_{LC}):

$$\begin{aligned}
 C_{C1} &= \frac{1}{\pi f_{LC} R_{C1}} \\
 &= 1.99 \text{ nF}
 \end{aligned}
 \tag{18}$$

Now the value of C_{C2} can be calculated to place a pole at half of the switching frequency (f_{SW}):

$$\begin{aligned}
 C_{C2} &= \frac{C_{C1}}{\pi f_{SW} R_{C1} C_{C1} - 1} \\
 &= 71 \text{ pF}
 \end{aligned}
 \tag{19}$$

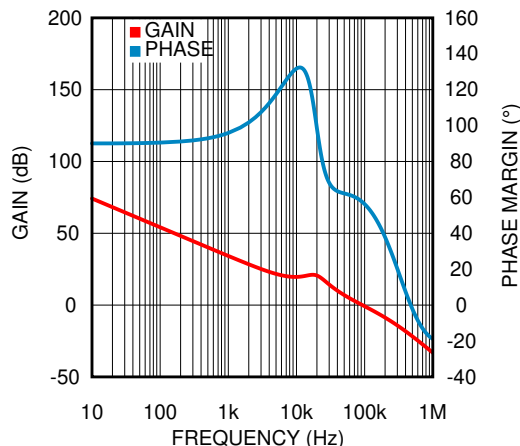
R_{C2} can then be calculated to set the second zero at the LC double pole frequency:

$$\begin{aligned}
 R_{C2} &= \frac{R_{FB1} f_{LC}}{f_{ESR} - f_{LC}} \\
 &= 166 \Omega
 \end{aligned}
 \tag{20}$$

Last, C_{C3} can be calculated to place a pole at the same frequency as the zero created by the output capacitor ESR:

$$\begin{aligned}
 C_{C3} &= \frac{1}{2\pi f_{ESR} R_{C2}} \\
 &= 898 \text{ pF}
 \end{aligned}
 \tag{21}$$

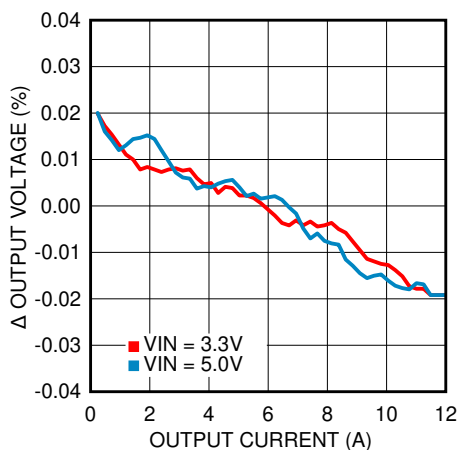
An illustration of the total loop response can be seen in [Figure 8-9](#).



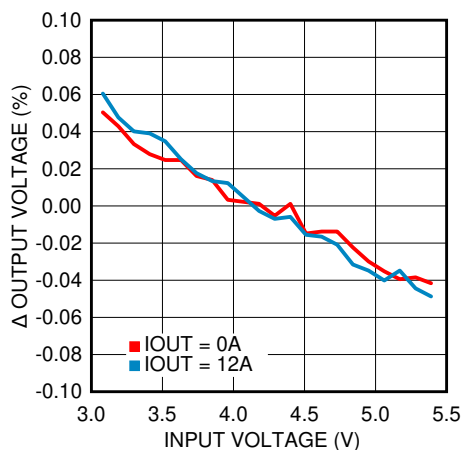
8-9. Loop Response

It is important to verify the stability by either observing the load transient response or by using a network analyzer. A phase margin between 45° and 70° is usually desired for voltage mode systems. Excessive phase margin can cause slow system response to load transients and low phase margin can cause an oscillatory load transient response. If the load step response peak deviation is larger than desired, increasing $f_{\text{CROSSOVER}}$ and recalculating the compensation components can help, but usually at the expense of phase margin.

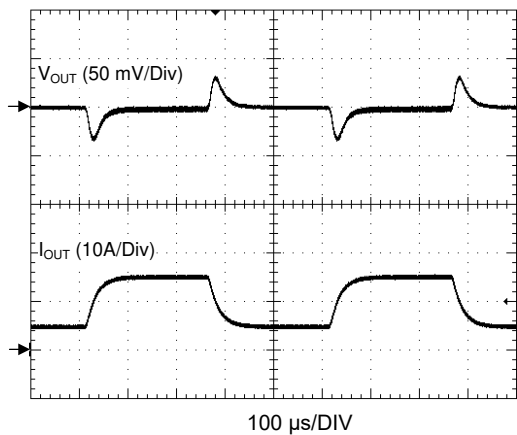
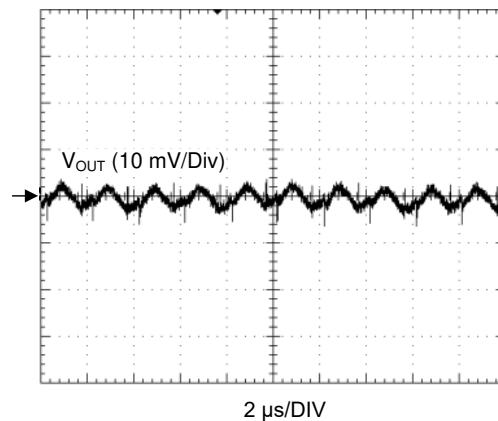
8.2.1.3 Application Curves



8-10. Load Regulation



8-11. Line Regulation

**图 8-12. Load Transient Response****图 8-13. Output Voltage Ripple ($I_{OUT} = 15$ A)**

8.2.2 Typical Application Schematic 2

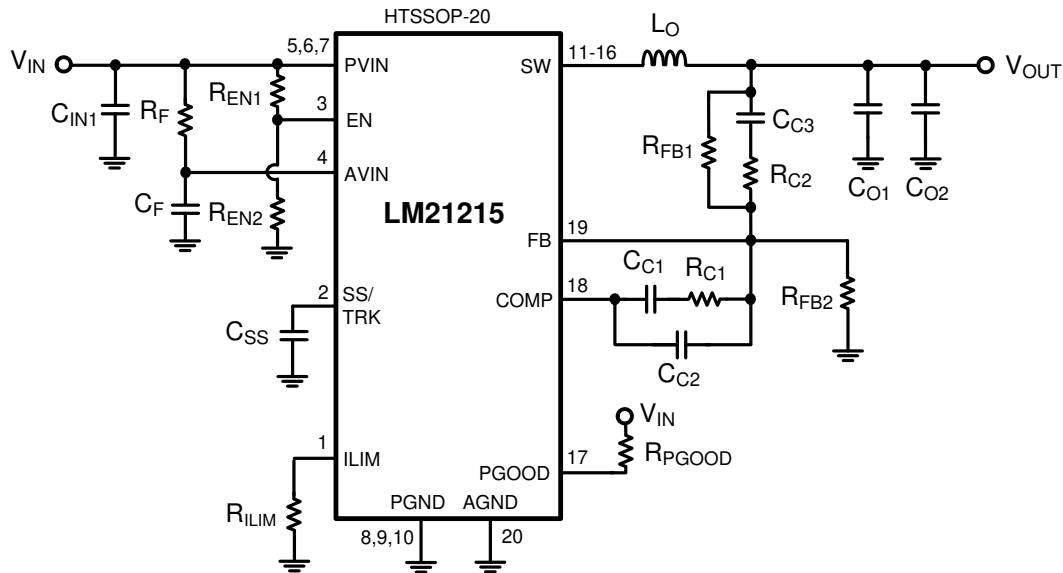


図 8-14. Typical Application Schematic 2

8.2.2.1 Design Requirements

表 8-3. Bill Of Materials ($V_{IN} = 4\text{ V}$ – 5.5 V , $V_{OUT} = 0.9\text{ V}$, $I_{OUT} = 8\text{ A}$)

ID	DESCRIPTION	VENDOR	PART NUMBER	QUANTITY
C_F	CAP, CERM, 1 μF , 10 V, $\pm 10\%$, X7R, 0603	MuRata	GRM188R71A105KA61D	1
C_{IN1} , C_{O1} , C_{O2}	CAP, CERM, 100 μF , 6.3 V, $\pm 20\%$, X5R, 1206	MuRata	GRM31CR60J107ME39L	3
C_{C1}	CAP, CERM, 1800 pF, 50 V, $\pm 5\%$, C0G/NP0, 0603	MuRata	GRM1885C1H182JA01D	1
C_{C2}	CAP, CERM, 82 pF, 50 V, $\pm 5\%$, C0G/NP0, 0603	TDK	C1608C0G1H820J	1
C_{C3}	CAP, CERM, 820 pF, 50 V, $\pm 5\%$, C0G/NP0, 0603	TDK	C1608C0G1H821J	1
C_{SS}	CAP, CERM, 0.033 μF , 16 V, $\pm 10\%$, X7R, 0603	MuRata	GRM188R71C333KA01D	1
L_O	Inductor, Shielded Drum Core, 680 nH, 22 A, 0.0014 Ω , SMD	Coilcraft	XAL1060-681ME	1
R_F	RES, 1.0 Ω , 5%, 0.1 W, 0603	Vishay-Dale	CRCW06031R00JNEA	1
R_{C1}	RES, 8.25 k Ω , 1%, 0.1 W, 0603	Vishay-Dale	CRCW06038K25FKEA	1
R_{C2}	RES, 124 Ω , 1%, 0.1 W, 0603	Vishay-Dale	CRCW0603124RFKEA	1
R_{EN1} , R_{FB1} , R_{PGOOD}	RES, 10 k Ω , 1%, 0.1 W, 0603	Vishay-Dale	CRCW060310K0FKEA	3
R_{EN2}	RES, 19.6 k Ω , 1%, 0.1 W, 0603	Vishay-Dale	CRCW060319K6FKEA	1
R_{FB2}	RES, 20.0 k Ω , 1%, 0.1 W, 0603	Vishay-Dale	CRCW060320K0FKEA	1
R_{ILIM}	RES, 39.2 k Ω , 1%, 0.1 W, 0603	Vishay-Dale	CRCW060339K2FKEA	1

8.2.2.2 Detailed Design Procedure

See [セクション 8.2.1.2](#)

9 Layout

9.1 Layout Considerations

PC board layout is an important part of DC/DC converter design. Poor board layout can disrupt the performance of a DC/DC converter and surrounding circuitry by contributing to EMI, ground bounce, and resistive voltage loss in the traces. These can send erroneous signals to the DC/DC converter resulting in poor regulation or instability.

Good layout can be implemented by following a few simple design rules.

- Minimize area of switched current loops. In a buck regulator, there are two loops where currents are switched at high slew rates. The first loop starts from the input capacitor, to the regulator PVIN pin, to the regulator SW pin, to the inductor then out to the output capacitor and load. The second loop starts from the output capacitor ground, to the regulator GND pins, to the inductor and then out to the load (see [Figure 9-1](#)). To minimize both loop areas, place the input capacitor as close as possible to the VIN pin. Grounding for both the input and output capacitor must be close. Ideally, a ground plane should be placed on the top layer that connects the PGND pins, the exposed pad (EP) of the device, and the ground connections of the input and output capacitors in a small area near pin 10 and 11 of the device. The inductor should be placed as close as possible to the SW pin and output capacitor.
- Minimize the copper area of the switch node. Route the six SW pins on a single top plane to the pad of the inductor. Place the inductor should be placed to the switch pins of the device with a wide trace to minimize conductive losses. The inductor can be placed on the bottom side of the PCB relative to the LM21215, but care must be taken to not allow any coupling of the magnetic field of the inductor into the sensitive feedback or compensation traces.
- Have a solid ground plane between PGND, the EP, and the input and output capacitor ground connections. The ground connections for the AGND, compensation, feedback, and soft-start components should be physically isolated (located near pin 1 and 20) from the power ground plane but a separate ground connection is not necessary. If not properly handled, poor grounding can result in degraded load regulation or erratic switching behavior.
- Carefully route the connection from the VOUT signal to the compensation network. This node is high impedance and can be susceptible to noise coupling. The trace should be routed away from the SW pin and inductor to avoid contaminating the feedback signal with switch noise.
- Make input and output bus connections as wide as possible. This reduces any voltage drops on the input or output of the converter and can improve efficiency. Voltage accuracy at the load is important so make sure feedback voltage sense is made at the load. Doing so corrects for voltage drops at the load and provide the best output accuracy.
- Provide adequate device heat sinking. For most 15-A, designs a four layer board is recommended. Use as many vias as is possible to connect the EP to the power plane heatsink. The vias located underneath the EP wicks solder into them if they are not filled. Complete solder coverage of the EP to the board is required to achieve the θ_{JA} values described in the previous section. Either an adequate amount of solder must be applied to the EP pad to fill the vias, or the vias must be filled during manufacturing. See [Section 9.2.1](#) to ensure enough copper heatsinking area is used to keep the junction temperature below 125°C.

9.2 Layout Example

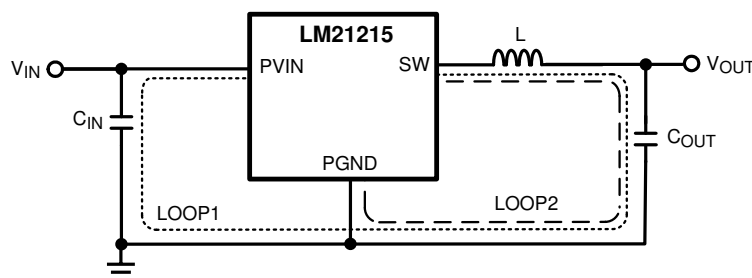


Figure 9-1. Schematic of LM21215 Highlighting Layout Sensitive Nodes

9.2.1 Thermal Considerations

The thermal characteristics of the LM21215 are specified using the parameter θ_{JA} , which relates the junction temperature to the ambient temperature. Although the value of θ_{JA} is dependent on many variables, it still can be used to approximate the operating junction temperature of the device.

To obtain an estimate of the device junction temperature, one can use the following relationship:

$$T_J = P_D \cdot \theta_{JA} + T_A \quad (22)$$

and

$$P_D = P_{IN} \cdot (1 - \text{Efficiency}) - I_{OUT}^2 \cdot R_{DCR} \quad (23)$$

where

- T_J is the junction temperature in °C.
- P_{IN} is the input power in Watts ($P_{IN} = V_{IN} \times I_{IN}$).
- θ_{JA} is the junction to ambient thermal resistance for the LM21215.
- T_A is the ambient temperature in °C.
- I_{OUT} is the output load current in A.

It is important to always keep the operating junction temperature (T_J) below 125°C for reliable operation. If the junction temperature exceeds 165°C, the device cycles in and out of thermal shutdown. If thermal shutdown occurs, it is a sign of inadequate heat sinking or excessive power dissipation in the device.

Figure 9-2 provides a better approximation of the θ_{JA} for a given PCB copper area. The PCB used in this test consisted of four layers: 1-oz. copper was used for the internal layers while the external layers were plated to 2-oz. copper weight. To provide an optimal thermal connection, a 3 × 5 array of 8-mil. vias under the thermal pad were used, and an additional twelve 8-mil. vias under the rest of the device were used to connect the four layers.

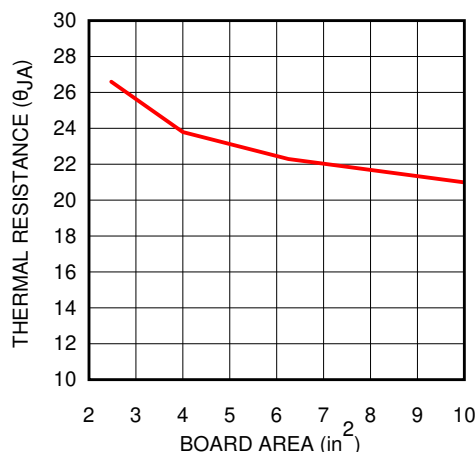


Figure 9-2. Thermal Resistance vs PCB Area (4-Layer Board)

Figure 9-3 shows a plot of the maximum ambient temperature vs output current for the typical application circuit shown in Figure 8-1, assuming a θ_{JA} value of 24°C/W.

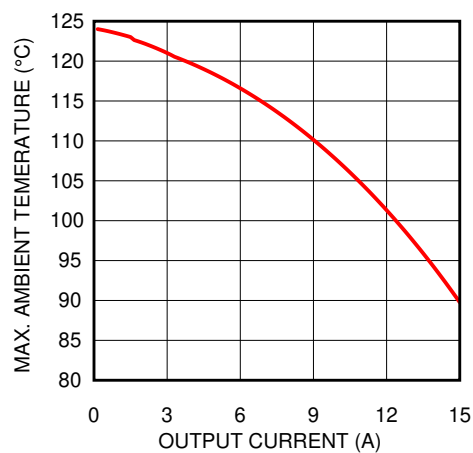


Figure 9-3. Maximum Ambient Temperature vs Output Current (0 LFM)

10 Device and Documentation Support

10.1 Device Support

10.1.1 Third-Party Products Disclaimer

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10.1.2 Development Support

10.1.2.1 Custom Design With WEBENCH® Tools

[Click here](#) to create a custom design using the LM21215 device with the WEBENCH® Power Designer.

1. Start by entering the input voltage (V_{IN}), output voltage (V_{OUT}), and output current (I_{OUT}) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance
- Run thermal simulations to understand board thermal performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

10.6 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LM21215MH/NOPB	Active	Production	HTSSOP (PWP) 20	73 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LM21215 MH
LM21215MH/NOPB.A	Active	Production	HTSSOP (PWP) 20	73 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LM21215 MH
LM21215MHE/NOPB	Active	Production	HTSSOP (PWP) 20	250 SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LM21215 MH
LM21215MHE/NOPB.A	Active	Production	HTSSOP (PWP) 20	250 SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LM21215 MH
LM21215MHE/NOPBG4.A	Active	Production	HTSSOP (PWP) 20	250 SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LM21215 MH
LM21215MHX/NOPB	Active	Production	HTSSOP (PWP) 20	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LM21215 MH
LM21215MHX/NOPB.A	Active	Production	HTSSOP (PWP) 20	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LM21215 MH

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

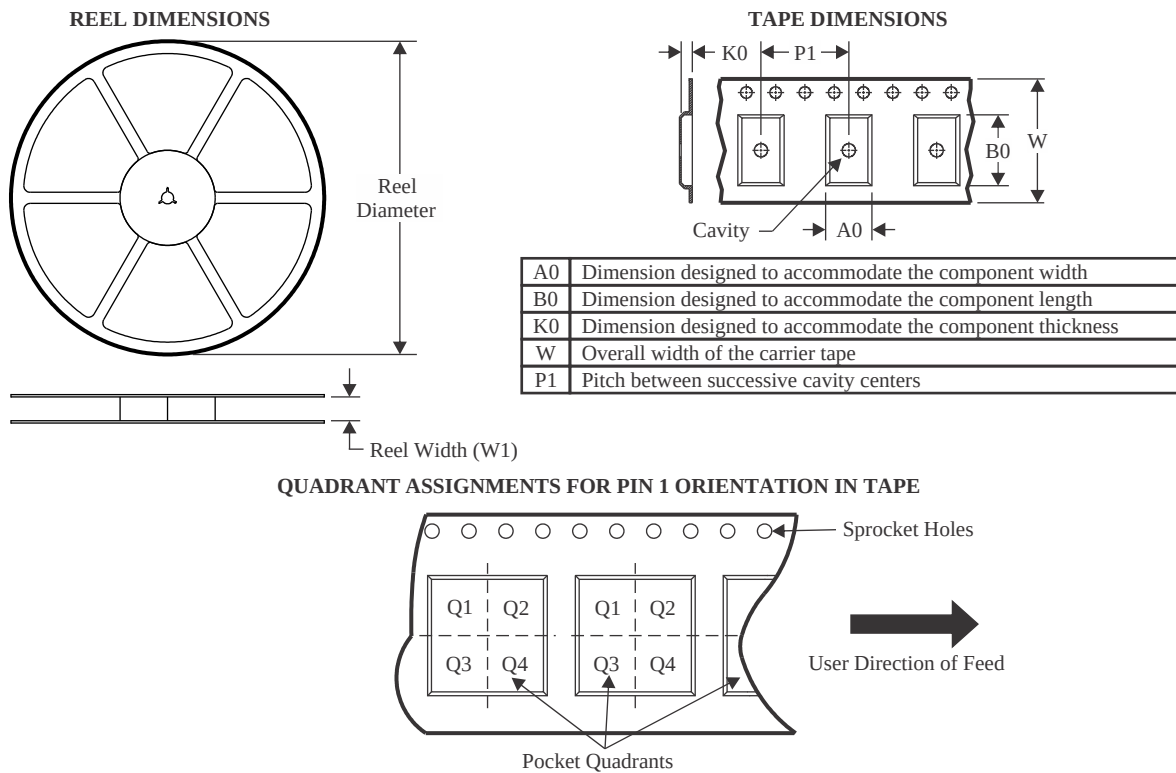
⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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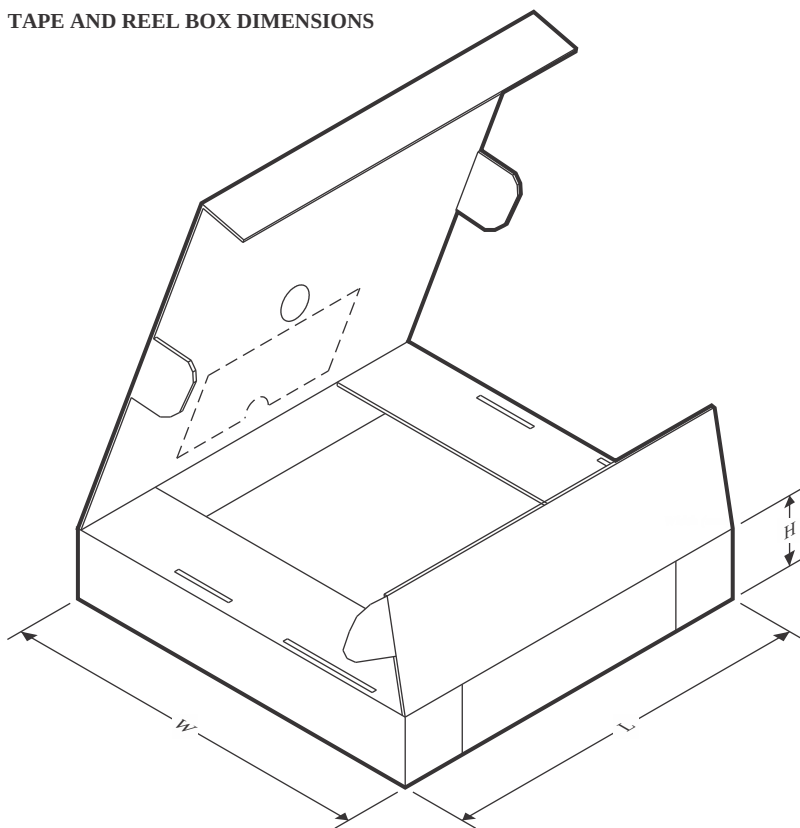
TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM21215MHE/NOPB	HTSSOP	PWP	20	250	178.0	16.4	6.95	7.0	1.4	8.0	16.0	Q1
LM21215MHX/NOPB	HTSSOP	PWP	20	2500	330.0	16.4	6.95	7.0	1.4	8.0	16.0	Q1

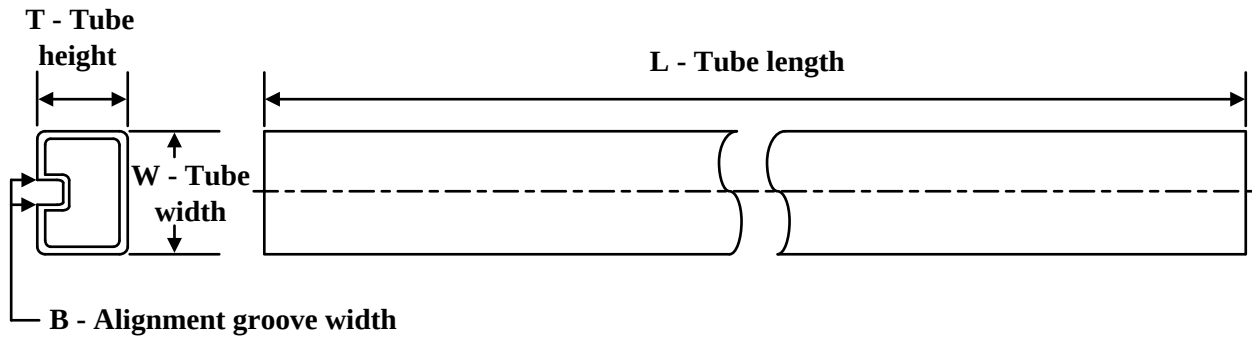
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM21215MHE/NOPB	HTSSOP	PWP	20	250	210.0	185.0	35.0
LM21215MHX/NOPB	HTSSOP	PWP	20	2500	367.0	367.0	35.0

TUBE

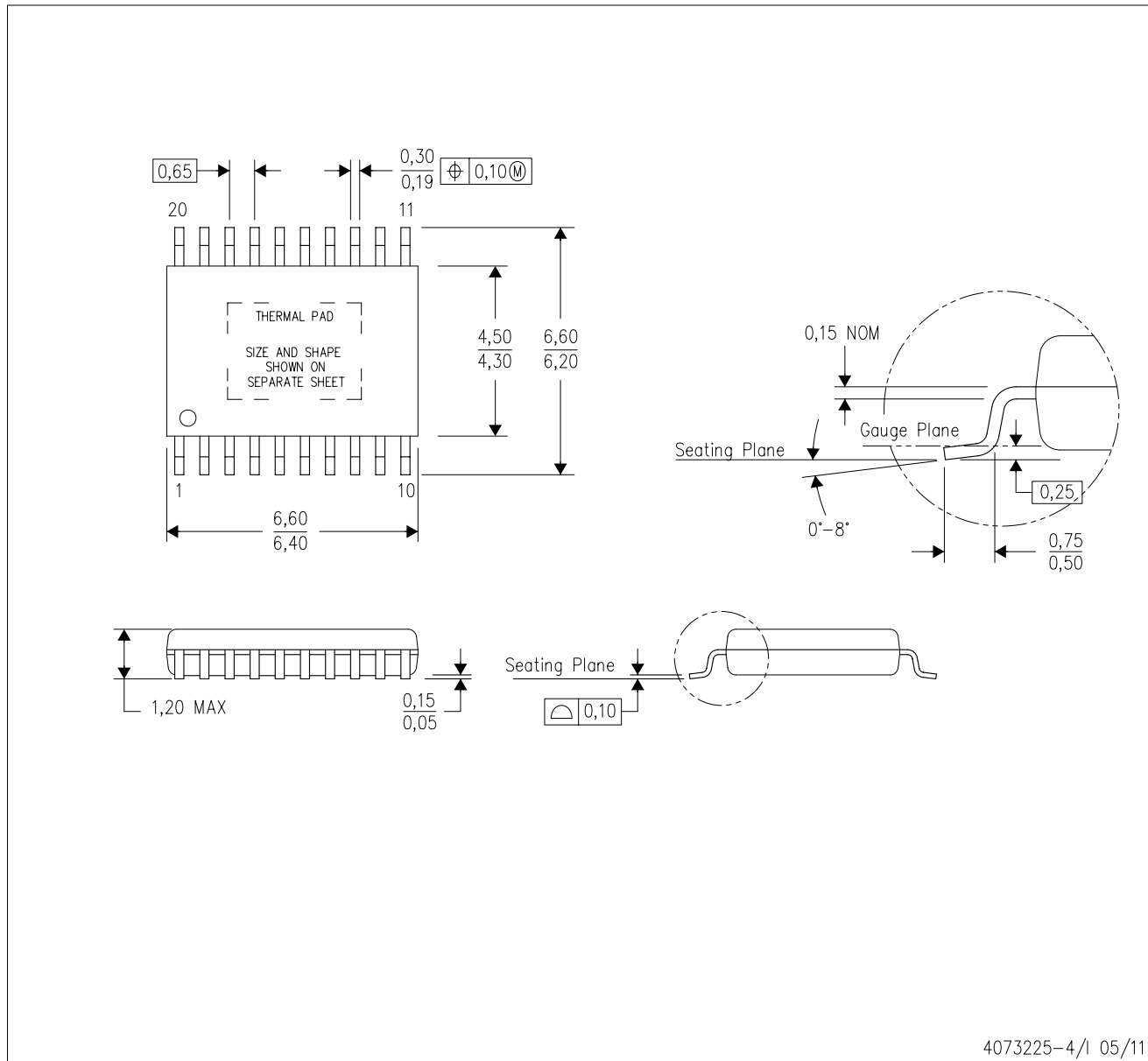


*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
LM21215MH/NOPB	PWP	HTSSOP	20	73	495	8	2514.6	4.06
LM21215MH/NOPB.A	PWP	HTSSOP	20	73	495	8	2514.6	4.06

PWP (R-PDSO-G20)

PowerPAD™ PLASTIC SMALL OUTLINE

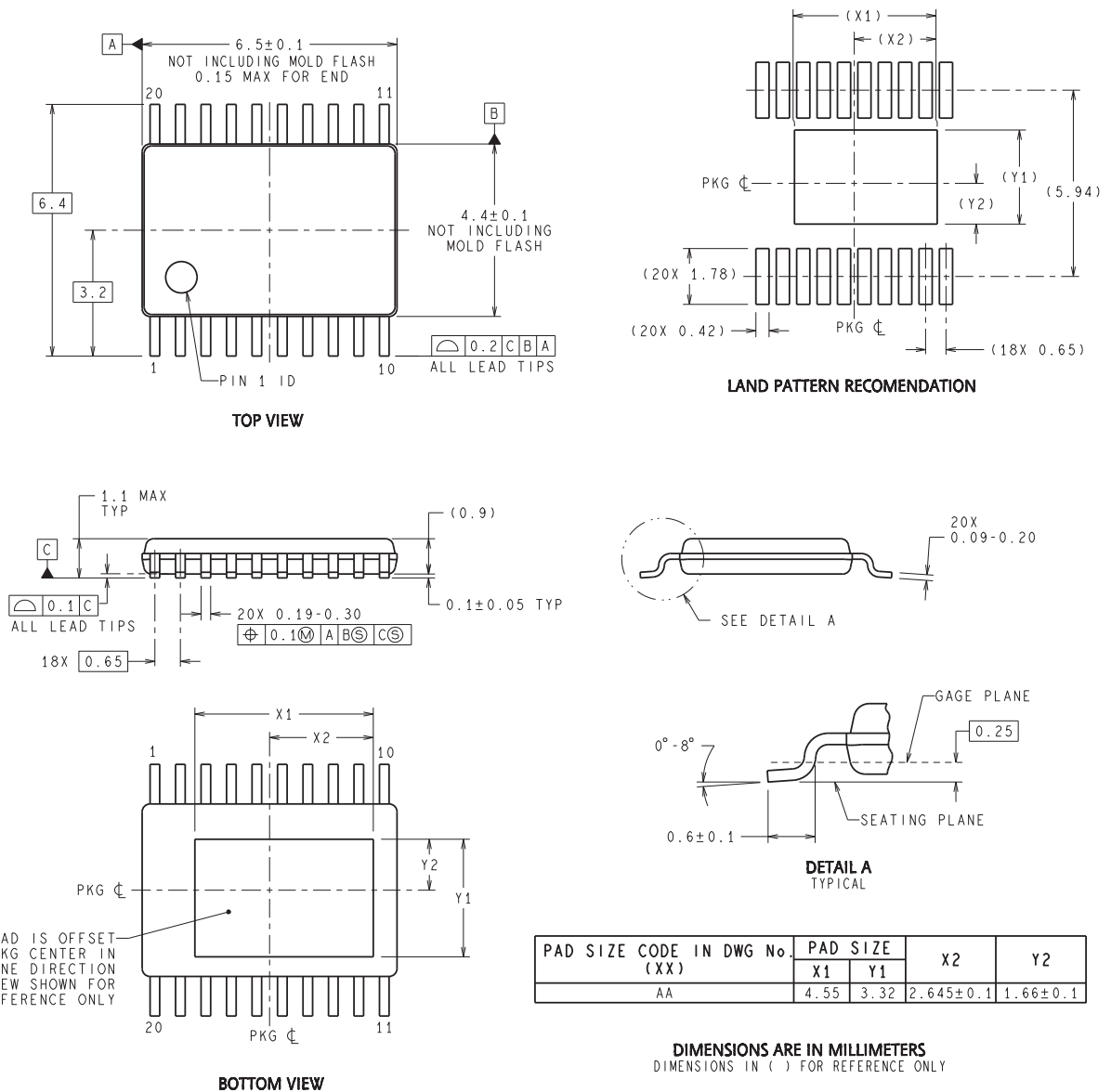


NOTES:

- All linear dimensions are in millimeters.
- This drawing is subject to change without notice.
- Body dimensions do not include mold flash or protrusions. Mold flash and protrusion shall not exceed 0.15 per side.
- This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <<http://www.ti.com>>.
- See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
- Falls within JEDEC MO-153

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PWP0020AA



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- NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
B. This drawing is subject to change without notice.
C. Reference JEDEC Registration MO-153, Variation ACT.

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