

LM290xLV 業界標準、低電圧オペアンプ

1 特長

- コストの制約が厳しいシステムのための業界標準アンプ
- 低入力オフセット電圧: $\pm 1\text{mV}$
- グラウンドを含む同相電圧範囲
- ユニティ・ゲイン帯域幅: 1MHz
- 低い広帯域ノイズ: $40\text{nV}/\sqrt{\text{Hz}}$
- 低い静止電流: $90\mu\text{A}/\text{Ch}$
- ユニティ・ゲイン安定
- 2.7V ～ 5.5V の電源電圧で動作
- デュアル・チャンネルとクワッド・チャンネルのバリエーションを提供
- 堅牢性の高い ESD 仕様: 2kV HBM
- 拡張温度範囲: -40°C ～ 125°C

2 アプリケーション

- コードレス家電
- 無停電電源
- バッテリ・パック、チャージャ、テスト機器
- 電源モジュール
- 環境センサの信号コンディショニング
- フィールド・トランスミッタ: 温度センサ
- オシロスコープ、デジタル・マルチメータ、信号アナライザ
- ラック・マウントのサーバー
- HVAC: 暖房、換気、空調
- DC モーター制御
- ローサイド電流センシング

3 概要

LM290xLV ファミリーには、デュアルの LM2904LV およびクワッドの LM2902LV オペアンプがあります。これらのオペアンプは、 2.7V ～ 5.5V の低電圧で動作します。

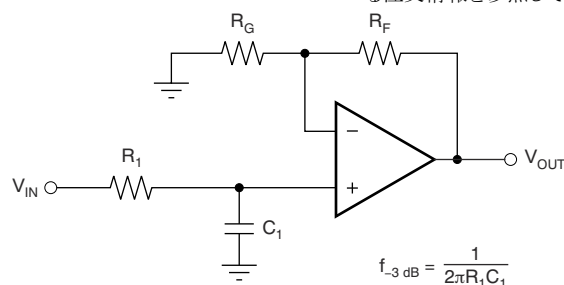
これらのオペアンプは、コストの制約が厳しい低電圧アプリケーションにおいて、LM2904 および LM2902 の代替品として使用できます。アプリケーションの例として、大型家電、煙感知器、個人用電子機器などがあります。LM290xLV デバイスは、低電圧で LM290x デバイスよりも優れた性能を備えており、低消費電力です。これらのオペアンプはユニティ・ゲインで安定であり、オーバードライブ条件で位相反転が発生しません。LM290xLV ファミリーの ESD 耐量は 2kV 以上 (HBM 仕様) です。

LM290xLV ファミリーは、業界標準のパッケージで供給されます。パッケージには SOIC、VSSOP、TSSOP があります。

デバイス情報

部品番号 ⁽¹⁾	パッケージ	本体サイズ (公称)
LM2902LV	SOIC (14)	$8.65\text{mm} \times 3.91\text{mm}$
	TSSOP (14)	$4.40\text{mm} \times 5.00\text{mm}$
	SOT-23 (14)	$4.20\text{mm} \times 2.00\text{mm}$
LM2904LV	SOIC (8)	$3.91\text{mm} \times 4.90\text{mm}$
	TSSOP (8)	$3.00\text{mm} \times 4.40\text{mm}$
	SOT-23 (8)	$1.60\text{mm} \times 2.90\text{mm}$
	VSSOP (8)	$3.00\text{mm} \times 3.00\text{mm}$

(1) 利用可能なパッケージについては、このデータシートの末尾にある注文情報を参照してください。



$$\frac{V_{\text{OUT}}}{V_{\text{IN}}} = \left(1 + \frac{R_F}{R_G}\right) \left(\frac{1}{1 + sR_1 C_1}\right)$$

単極ローパス・フィルタ



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4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision B (October 2019) to Revision C (February 2022)	Page
• 文書全体にわたって表、図、相互参照の採番方法を更新.....	1
• 「製品情報」表に SOT-23 (DYY) パッケージを追加.....	1
• Added DYY (SOT-23) package to <i>Pin Configuration and Functions</i> section.....	3
• Added DYY (SOT-23) package to <i>Thermal Information: LM2902LV</i> section.....	6
Changes from Revision A (May 2019) to Revision B (October 2019)	Page
• SOT-23 (DDF) プレビュー注記をすべて削除.....	1
Changes from Revision * (September 2018) to Revision A (May 2019)	Page
• 「製品情報」表に SOT-23 (DDF) パッケージを追加.....	1
• Added DDF (SOT-23) package to <i>Pin Configuration and Functions</i> section.....	3
• Added DDF (SOT-23) <i>Thermal Information: LM2904LV</i> section.....	5

5 Pin Configuration and Functions

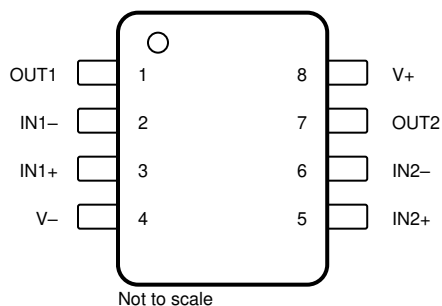


图 5-1. LM2904LV D, DGK, PW, and DDF Package
8-Pin SOIC, VSSOP, TSSOP, and SOT-23
(Top View)

表 5-1. Pin Functions: LM2904LV

PIN		I/O	DESCRIPTION
NAME	NO.		
IN1–	2	I	Inverting input, channel 1
IN1+	3	I	Noninverting input, channel 1
IN2–	6	I	Inverting input, channel 2
IN2+	5	I	Noninverting input, channel 2
OUT1	1	O	Output, channel 1
OUT2	7	O	Output, channel 2
V–	4	I or —	Negative (low) supply or ground (for single-supply operation)
V+	8	I	Positive (high) supply

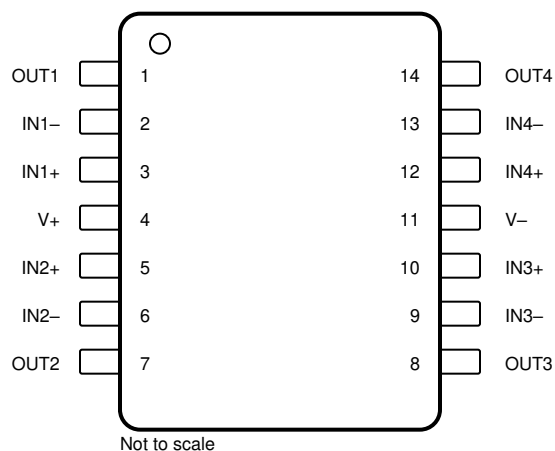


**图 5-2. LM2902LV D, PW, DYY and Package
14-Pin SOIC, TSSOP, and SOT-23
(Top View)**

表 5-2. Pin Functions: LM2902LV

PIN		I/O	DESCRIPTION
NAME	NO.		
IN1–	2	I	Inverting input, channel 1
IN1+	3	I	Noninverting input, channel 1
IN2–	6	I	Inverting input, channel 2
IN2+	5	I	Noninverting input, channel 2
IN3–	9	I	Inverting input, channel 3
IN3+	10	I	Noninverting input, channel 3
IN4–	13	I	Inverting input, channel 4
IN4+	12	I	Noninverting input, channel 4
OUT1	1	O	Output, channel 1
OUT2	7	O	Output, channel 2
OUT3	8	O	Output, channel 3
OUT4	14	O	Output, channel 4
V–	11	I or —	Negative (low) supply or ground (for single-supply operation)
V+	4	I	Positive (high) supply

6 Specifications

6.1 Absolute Maximum Ratings

over operating junction temperature range (unless otherwise noted)⁽¹⁾

			MIN	MAX	UNIT
Supply voltage, ([V+] – [V–])			0	6	V
Signal input pins	Voltage ⁽²⁾	Common-mode	(V–) – 0.5	(V+) + 0.5	V
		Differential	(V+) – (V–) + 0.2		V
	Current ⁽²⁾		–10	10	mA
Output short-circuit ⁽³⁾			Continuous		
Operating, T _A			–55	125	°C
Operating junction temperature, T _J				150	°C
Storage temperature, T _{stg}			–65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) Input pins are diode-clamped to the power-supply rails. Input signals that may swing more than 0.5 V beyond the supply rails must be current limited to 10 mA or less.
- (3) Short-circuit to ground, one amplifier per package.

6.2 ESD Ratings

			VALUE	UNIT
V _(ESD)	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾	±1000	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating junction temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V _S	Supply voltage [(V+) – (V–)]		2.7	5.5	V
V _{IN}	Input-pin voltage range		(V–) – 0.1	(V+) – 1	V
T _A	Specified temperature		–40	125	°C

6.4 Thermal Information: LM2904LV

THERMAL METRIC ⁽¹⁾		LM2904LV				UNIT
		D (SOIC)	DGK (VSSOP)	PW (TSSOP)	DDF (SOT-23)	
		8 PINS	8 PINS	8 PINS	8 PINS	
R _{θJA}	Junction-to-ambient thermal resistance	207.9	201.2	200.7	183.7	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	92.8	85.7	95.4	112.5	°C/W
R _{θJB}	Junction-to-board thermal resistance	129.7	122.9	128.6	98.2	°C/W
ψ _{JT}	Junction-to-top characterization parameter	26	21.2	27.2	18.8	°C/W
ψ _{JB}	Junction-to-board characterization parameter	127.9	121.4	127.2	97.6	°C/W

- (1) For more information about traditional and new thermal metrics, see [Semiconductor and IC Package Thermal Metrics](#).

6.5 Thermal Information: LM2902LV

THERMAL METRIC ⁽¹⁾		LM2902LV			UNIT
		D (SOIC)	PW (TSSOP)	DYY (SOT-23)	
		14 PINS	14 PINS	14 PINS	
R _{θJA}	Junction-to-ambient thermal resistance	102.1	148.3	154.6	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	56.8	68.1	86.3	°C/W
R _{θJB}	Junction-to-board thermal resistance	58.5	92.7	67.3	°C/W
ψ _{JT}	Junction-to-top characterization parameter	20.5	16.9	9.8	°C/W
ψ _{JB}	Junction-to-board characterization parameter	58.1	91.8	67.1	°C/W

(1) For more information about traditional and new thermal metrics, see [Semiconductor and IC Package Thermal Metrics](#).

6.6 Electrical Characteristics

For $V_S = (V+) - (V-) = 2.7\text{ V to }5.5\text{ V}$ ($\pm 1.35\text{ V to } \pm 2.75\text{ V}$), $T_A = 25^\circ\text{C}$, $R_L = 10\text{ k}\Omega$ connected to $V_S / 2$, and $V_{CM} = V_{OUT} = V_S / 2$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFFSET VOLTAGE						
V _{OS}	Input offset voltage	V _S = 5 V		±1	±3	mV
		V _S = 5 V, T _A = −40°C to 125°C			±5	
dV _{OS} /dT	V _{OS} vs temperature	T _A = −40°C to 125°C		±4		μV/°C
PSRR	Power-supply rejection ratio	V _S = 2.7 V to 5.5 V, V _{CM} = (V−)	80	100		dB
INPUT VOLTAGE RANGE						
V _{CM}	Common-mode voltage range	No phase reversal	(V−) − 0.1		(V+) − 1	V
CMRR	Common-mode rejection ratio	V _S = 2.7 V, (V−) − 0.1 V < V _{CM} < (V+) − 1 V T _A = −40°C to 125°C		84		dB
		V _S = 5.5 V, (V−) − 0.1 V < V _{CM} < (V+) − 1 V T _A = −40°C to 125°C	63	92		
INPUT BIAS CURRENT						
I _B	Input bias current	V _S = 5 V		±15		pA
I _{OS}	Input offset current			±5		pA
NOISE						
E _n	Input voltage noise (peak-to-peak)	f = 0.1 Hz to 10 Hz, V _S = 5 V		5.1		μV _{PP}
e _n	Input voltage noise density	f = 1 kHz, V _S = 5 V		40		nV/√ Hz
INPUT CAPACITANCE						
C _{ID}	Differential			2		pF
C _{IC}	Common-mode			5.5		pF
OPEN-LOOP GAIN						
A _{OL}	Open-loop voltage gain	V _S = 2.7 V, (V−) + 0.15 V < V _O < (V+) − 0.15 V, R _L = 2 kΩ		110		dB
		V _S = 5.5 V, (V−) + 0.15 V < V _O < (V+) − 0.15 V, R _L = 2 kΩ		125		
FREQUENCY RESPONSE						
GBW	Gain-bandwidth product	V _S = 5 V		1		MHz
Φ _m	Phase margin	V _S = 5.5 V, G = 1		75		°
SR	Slew rate	V _S = 5 V		1.5		V/μs
t _S	Settling time	To 0.1%, V _S = 5 V, 2-V step, G = 1, C _L = 100 pF		4		μs
		To 0.01%, V _S = 5 V, 2-V step, G = 1, C _L = 100 pF		5		
t _{OR}	Overload recovery time	V _S = 5 V, V _{IN} × gain > V _S		1		μs
THD+N	Total harmonic distortion + noise	V _S = 5.5 V, V _{CM} = 2.5 V, V _O = 1 V _{RMS} , G = 1, f = 1 kHz, 80-kHz measurement BW		0.005%		
OUTPUT						
V _{OH}	Voltage output swing from positive supply	R _L ≥ 2 kΩ, T _A = −40°C to 125°C		1		V
V _{OL}	Voltage output swing from negative supply	R _L ≤ 10 kΩ, T _A = −40°C to 125°C		40	75	mV
I _{SC}	Short-circuit current	V _S = 5.5 V		±40		mA
Z _O	Open-loop output impedance	V _S = 5 V, f = 1 MHz		1200		Ω

6.6 Electrical Characteristics (continued)

For $V_S = (V+) - (V-) = 2.7\text{ V to } 5.5\text{ V}$ ($\pm 1.35\text{ V to } \pm 2.75\text{ V}$), $T_A = 25^\circ\text{C}$, $R_L = 10\text{ k}\Omega$ connected to $V_S / 2$, and $V_{CM} = V_{OUT} = V_S / 2$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLY						
V_S	Specified voltage range		2.7 (± 1.35)		5.5 (± 2.75)	V
I_Q	Quiescent current per amplifier	$I_O = 0\text{ mA}$, $V_S = 5.5\text{ V}$		90	150	μA
		$I_O = 0\text{ mA}$, $V_S = 5.5\text{ V}$, $T_A = -40^\circ\text{C to } 125^\circ\text{C}$			160	

6.7 Typical Characteristics

at $T_A = 25^\circ\text{C}$, $V_+ = 2.75\text{ V}$, $V_- = -2.75\text{ V}$, $R_L = 10\text{ k}\Omega$ connected to $V_S / 2$, $V_{CM} = V_S / 2$, and $V_{OUT} = V_S / 2$ (unless otherwise noted)

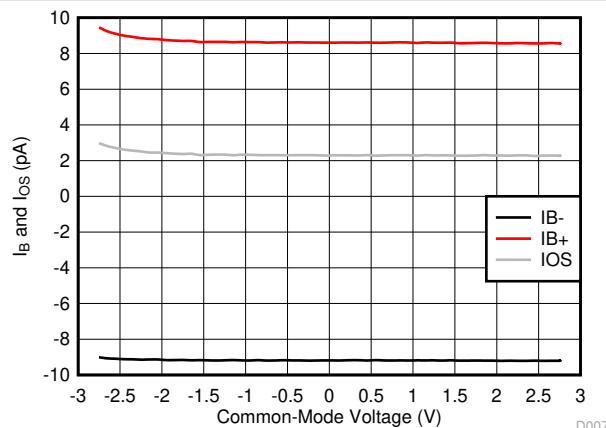


Figure 6-1. I_B and I_{OS} vs Common-Mode Voltage

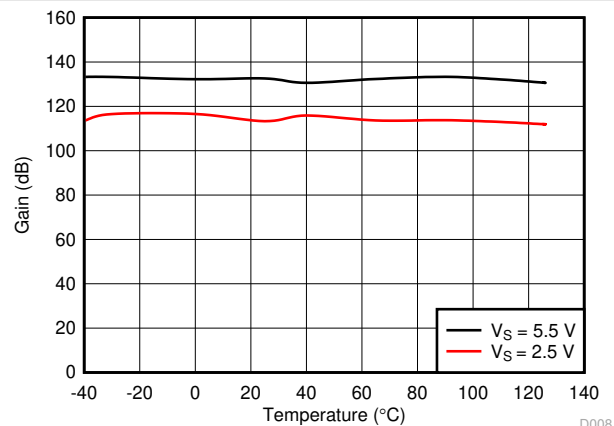


Figure 6-2. Open-Loop Gain vs Temperature

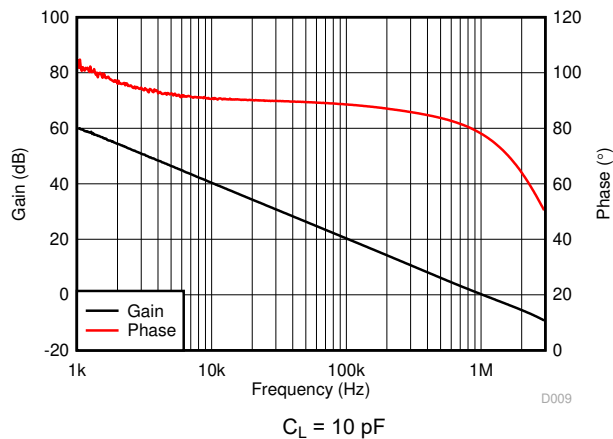


Figure 6-3. Open-Loop Gain and Phase vs Frequency

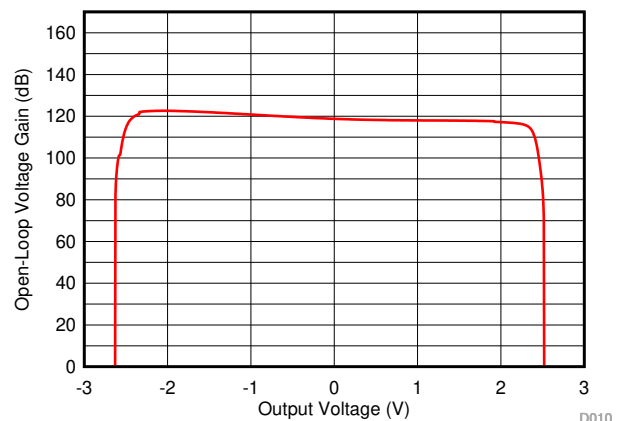


Figure 6-4. Open-Loop Gain vs Output Voltage

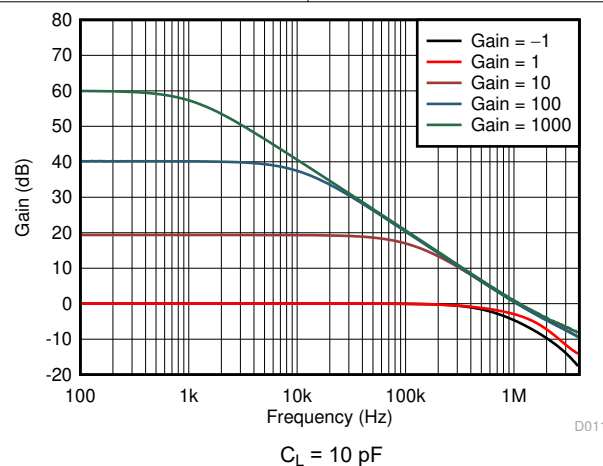
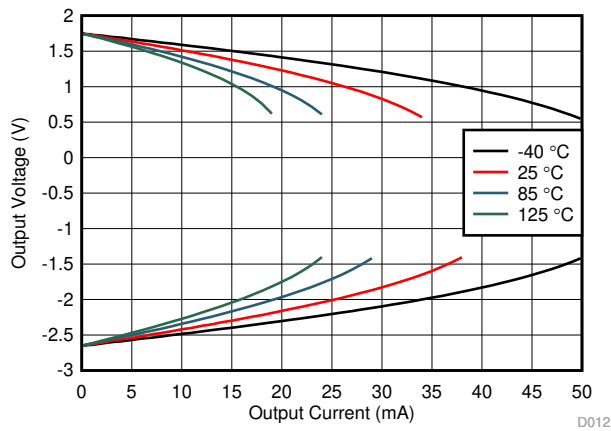


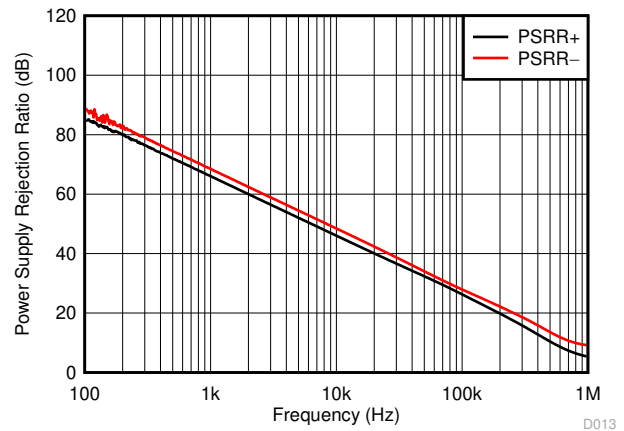
Figure 6-5. Closed-Loop Gain vs Frequency

6.7 Typical Characteristics

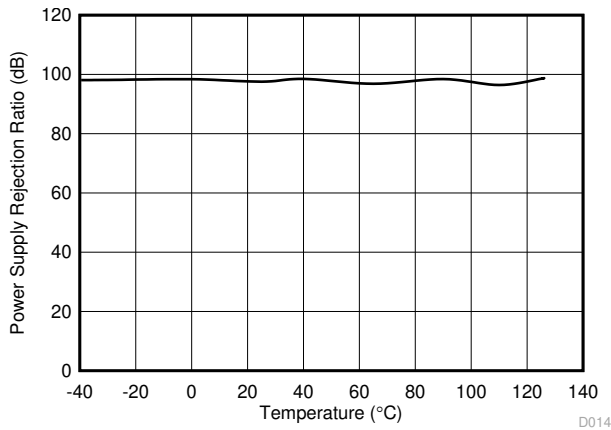
at $T_A = 25^\circ\text{C}$, $V_+ = 2.75\text{ V}$, $V_- = -2.75\text{ V}$, $R_L = 10\text{ k}\Omega$ connected to $V_S / 2$, $V_{CM} = V_S / 2$, and $V_{OUT} = V_S / 2$ (unless otherwise noted)



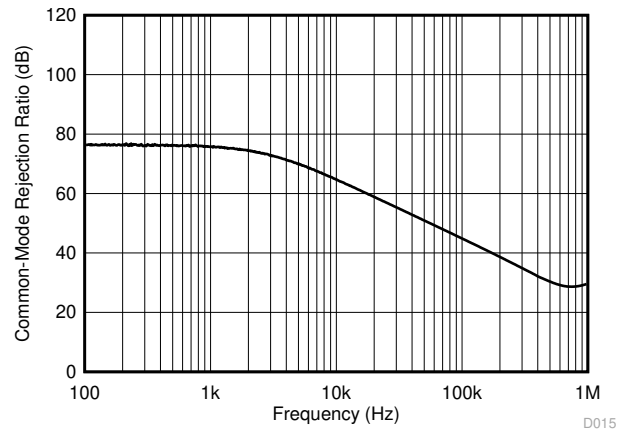
6-6. Output Voltage vs Output Current (Claw)



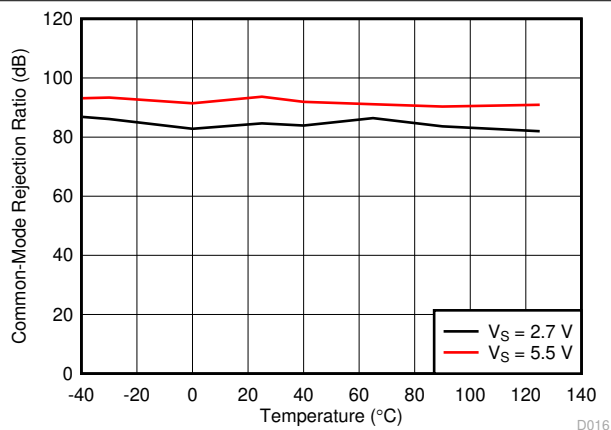
6-7. PSRR vs Frequency



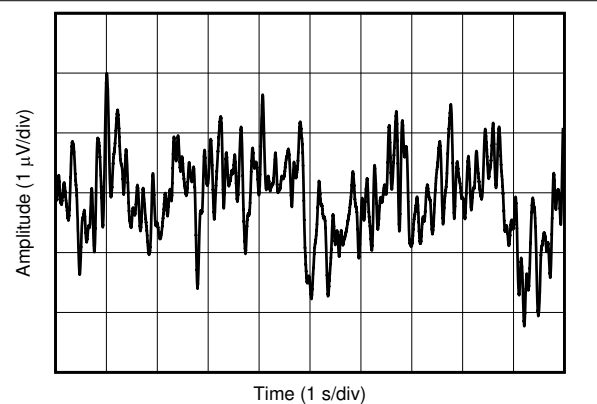
6-8. DC PSRR vs Temperature



6-9. CMRR vs Frequency



6-10. DC CMRR vs Temperature



6-11. 0.1-Hz to 10-Hz Integrated Voltage Noise

6.7 Typical Characteristics

at $T_A = 25^\circ\text{C}$, $V_+ = 2.75\text{ V}$, $V_- = -2.75\text{ V}$, $R_L = 10\text{ k}\Omega$ connected to $V_S / 2$, $V_{CM} = V_S / 2$, and $V_{OUT} = V_S / 2$ (unless otherwise noted)

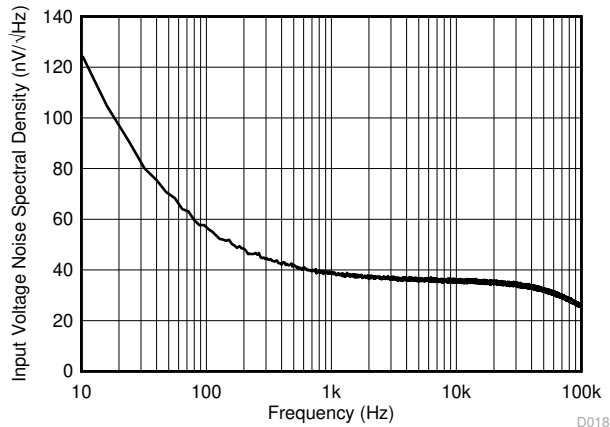
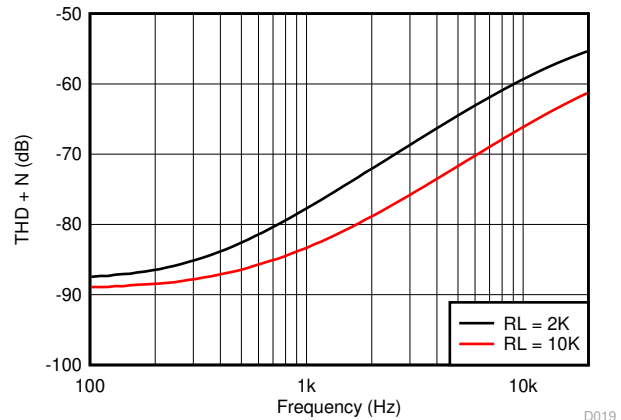
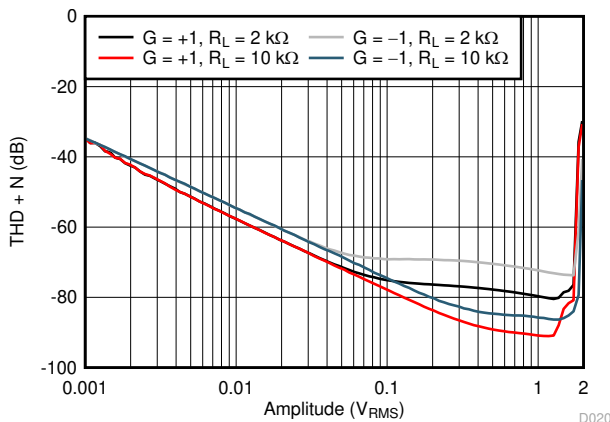


FIG 6-12. Input Voltage Noise Spectral Density



$V_S = 5.5\text{ V}$ $V_{CM} = 2.5\text{ V}$ $G = 1$
 $BW = 80\text{ kHz}$ $V_{OUT} = 0.5\text{ V}_{RMS}$

FIG 6-13. THD + N vs Frequency



$V_S = 5.5\text{ V}$ $V_{CM} = 2.5\text{ V}$ $f = 1\text{ kHz}$
 $G = 1$ $BW = 80\text{ kHz}$

FIG 6-14. THD + N vs Amplitude

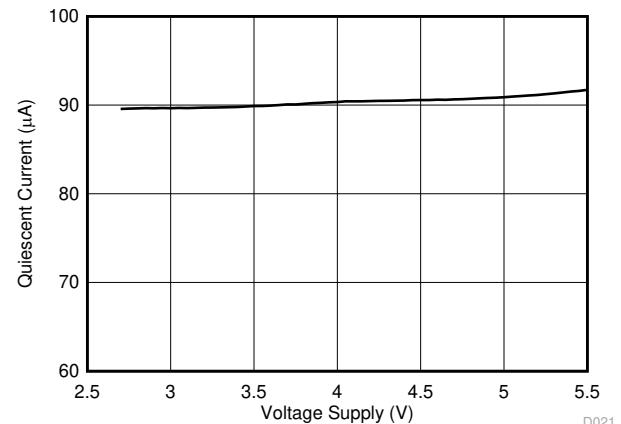


FIG 6-15. Quiescent Current vs Supply Voltage

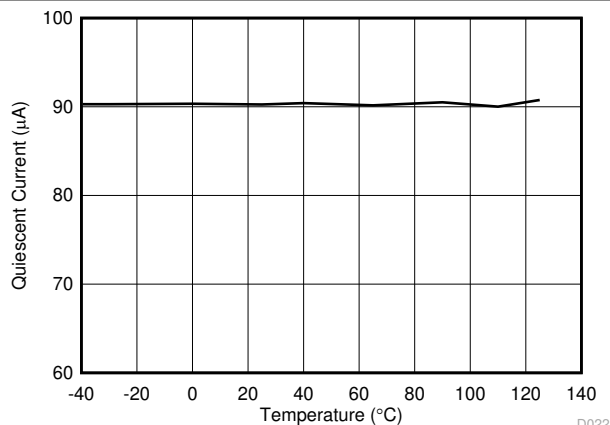


FIG 6-16. Quiescent Current vs Temperature

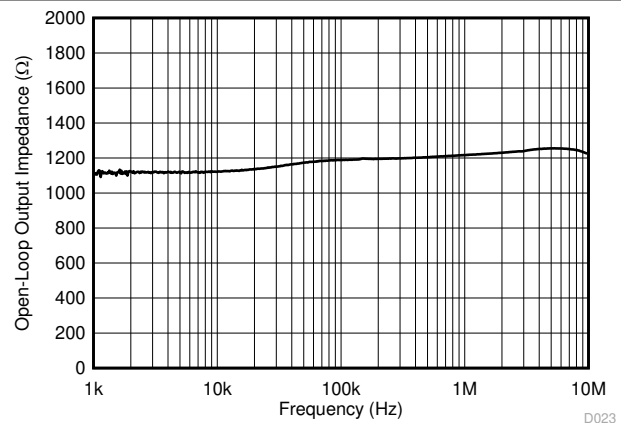


FIG 6-17. Open-Loop Output Impedance vs Frequency

6.7 Typical Characteristics

at $T_A = 25^\circ\text{C}$, $V_+ = 2.75\text{ V}$, $V_- = -2.75\text{ V}$, $R_L = 10\text{ k}\Omega$ connected to $V_S / 2$, $V_{CM} = V_S / 2$, and $V_{OUT} = V_S / 2$ (unless otherwise noted)

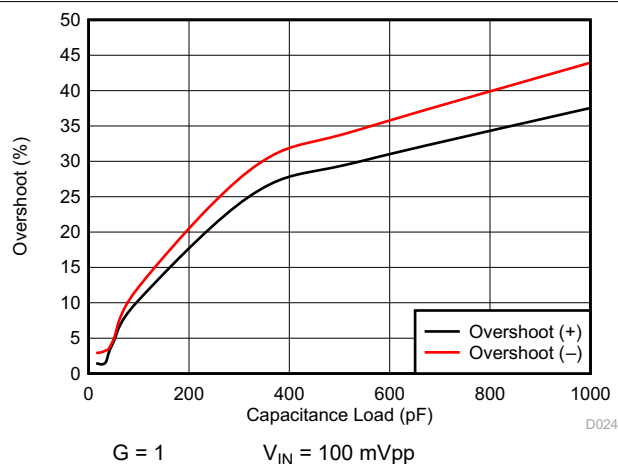


Figure 6-18. Small Signal Overshoot vs Capacitive Load

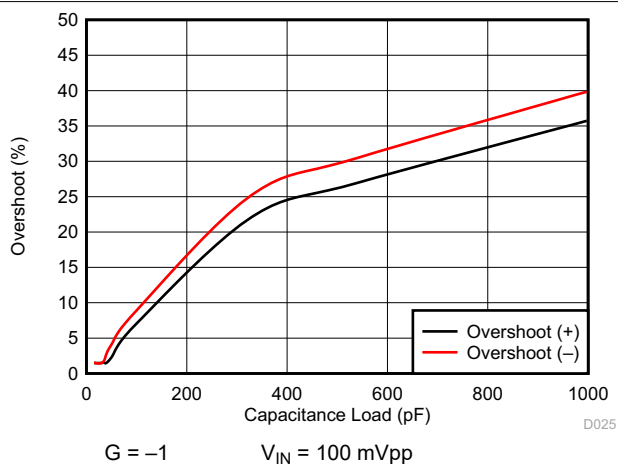


Figure 6-19. Small Signal Overshoot vs Capacitive Load

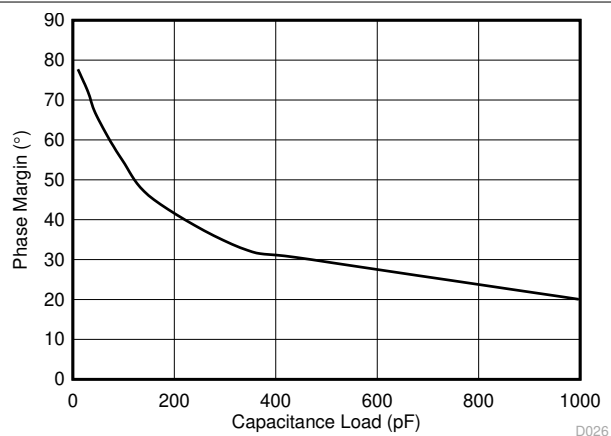


Figure 6-20. Phase Margin vs Capacitive Load

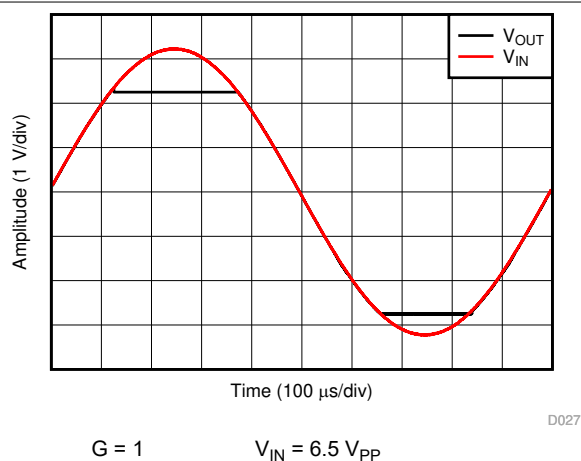


Figure 6-21. No Phase Reversal

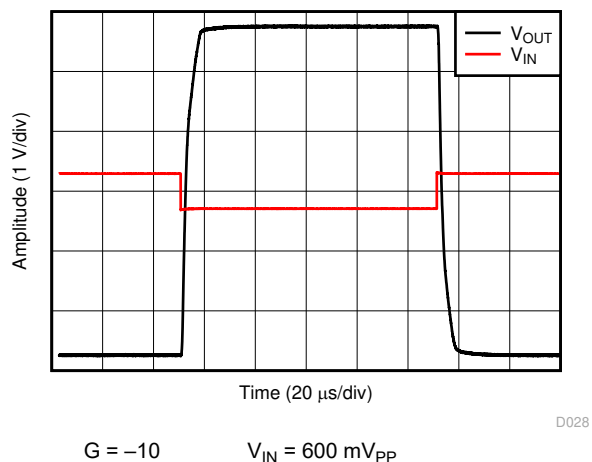


Figure 6-22. Overload Recovery

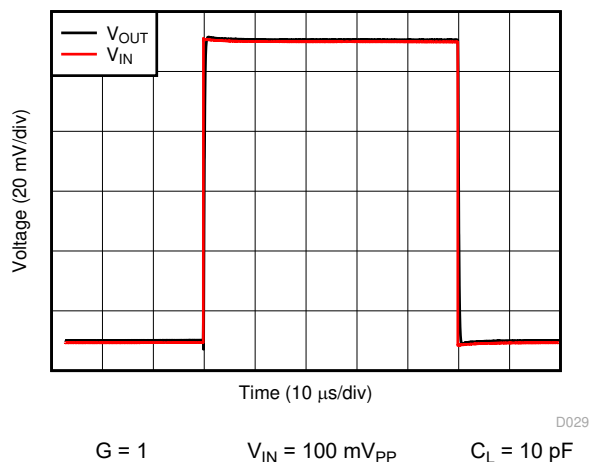


Figure 6-23. Small-Signal Step Response

6.7 Typical Characteristics (continued)

at $T_A = 25^\circ\text{C}$, $V_+ = 2.75\text{ V}$, $V_- = -2.75\text{ V}$, $R_L = 10\text{ k}\Omega$ connected to $V_S / 2$, $V_{CM} = V_S / 2$, and $V_{OUT} = V_S / 2$ (unless otherwise noted)

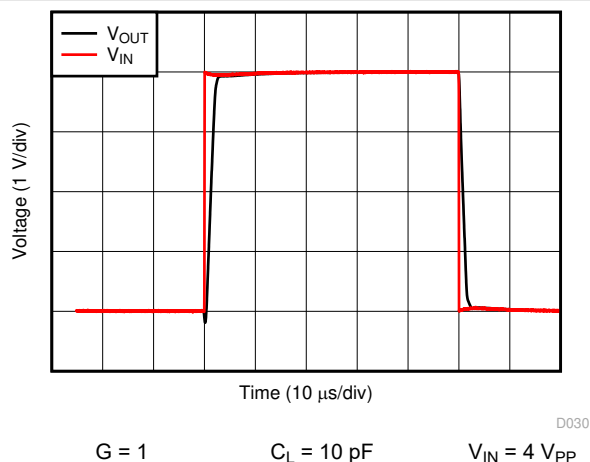


Figure 6-24. Large-Signal Step Response

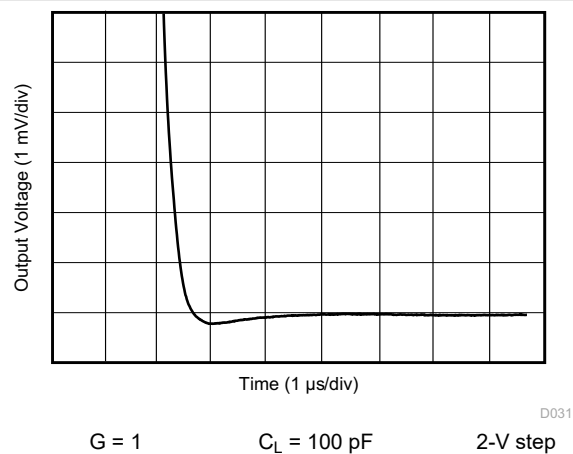


Figure 6-25. Large-Signal Settling Time (Negative)

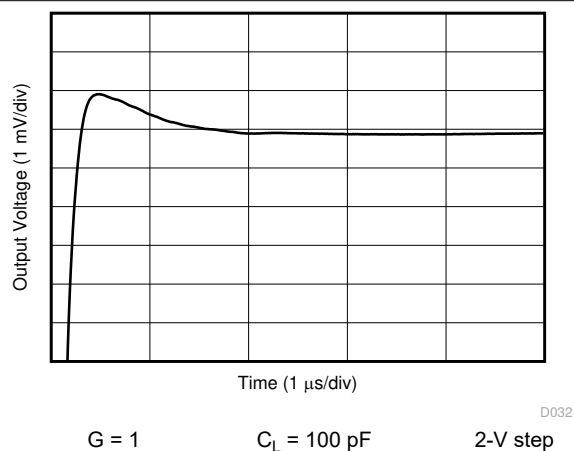


Figure 6-26. Large-Signal Settling Time (Positive)

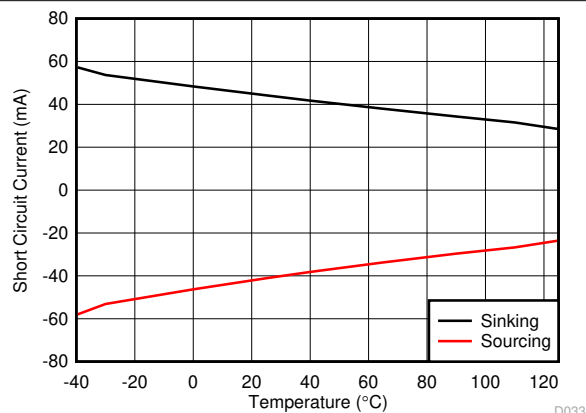


Figure 6-27. Short-Circuit Current vs Temperature

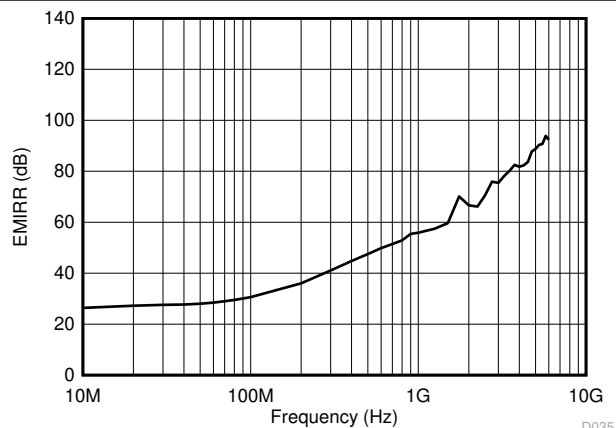


Figure 6-28. Electromagnetic Interference Rejection Ratio Referred to Noninverting Input (EMIRR+) vs Frequency

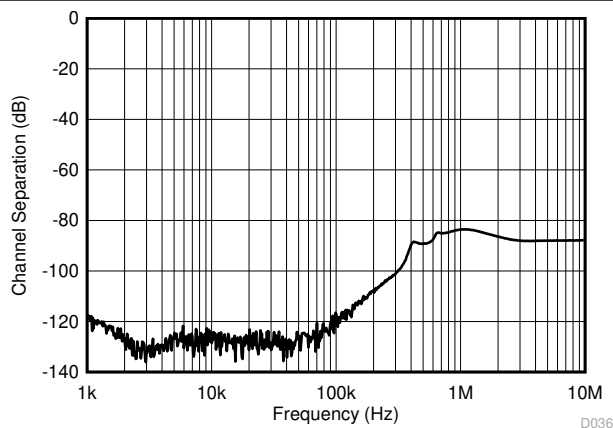


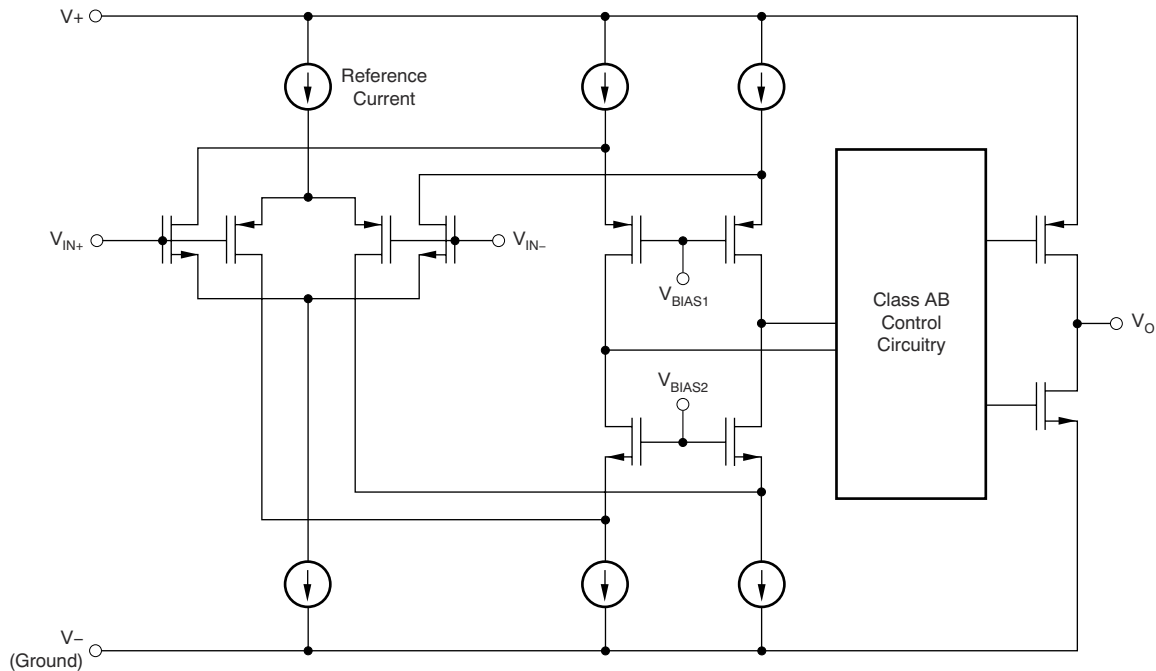
Figure 6-29. Channel Separation

7 Detailed Description

7.1 Overview

The LM290xLV family of low-power op amps is intended for cost-optimized systems. These devices operate from 2.7 V to 5.5 V, are unity-gain stable, and are designed for a wide range of general-purpose applications. The input common-mode voltage range includes the negative rail and allows the LM290xLV family to be used in many single-supply applications.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Operating Voltage

The LM290xLV family of op amps is specified for operation from 2.7 V to 5.5 V. In addition, many specifications apply from -40°C to 125°C . Parameters that vary significantly with operating voltages or temperature are shown in the section.

7.3.2 Common-Mode Input Range Includes Ground

The input common-mode voltage range of the LM290xLV family extends to the negative supply rail and within 1 V below the positive rail for the full supply voltage range of 2.7 V to 5.5 V. This performance is achieved with a P-channel differential pair, as shown in the [Functional Block Diagram](#). Additionally, a complementary N-channel differential pair has been included in parallel to eliminate issues with phase reversal that are common with previous generations of op amps. However, the N-channel pair is not optimized for operation, and significant performance degradation occurs while this pair is operational. TI recommends limiting any voltage applied at the inputs to at least 1 V below the positive supply rail (V_{+}) to ensure that the op amp conforms to the specifications detailed in the section.

7.3.3 Overload Recovery

Overload recovery is defined as the time required for the operational amplifier output to recover from a saturated state to a linear state. The output devices of the operational amplifier enter a saturation region when the output voltage exceeds the specified output voltage swing, because of the high input voltage or the high gain. After the device enters the saturation region, the charge carriers in the output devices require time to return to the linear state. After the charge carriers return to the linear state, the device begins to slew at the specified slew rate.

Therefore, the propagation delay (in case of an overload condition) is the sum of the overload recovery time and the slew time. The overload recovery time for the LM290xLV family is typically 1 μ s.

7.3.4 Electrical Overstress

Designers often ask questions about the capability of an operational amplifier to withstand electrical overstress. These questions tend to focus on the device inputs, but can also involve the supply voltage pins. Each of these different pin functions has electrical stress limits determined by the voltage breakdown characteristics of the particular semiconductor fabrication process and specific circuits connected to the pin. Additionally, internal electrostatic discharge (ESD) protection is built into these circuits to protect them from accidental ESD events both before and during product assembly.

Having a good understanding of this basic ESD circuitry and its relevance to an electrical overstress event is helpful. [Figure 7-1](#) shows the ESD circuits contained in the LM290xLV. The ESD protection circuitry involves several current-steering diodes connected from the input and output pins and routed back to the internal power supply lines, where they meet at an absorption device internal to the operational amplifier. This protection circuitry is intended to remain inactive during normal circuit operation.

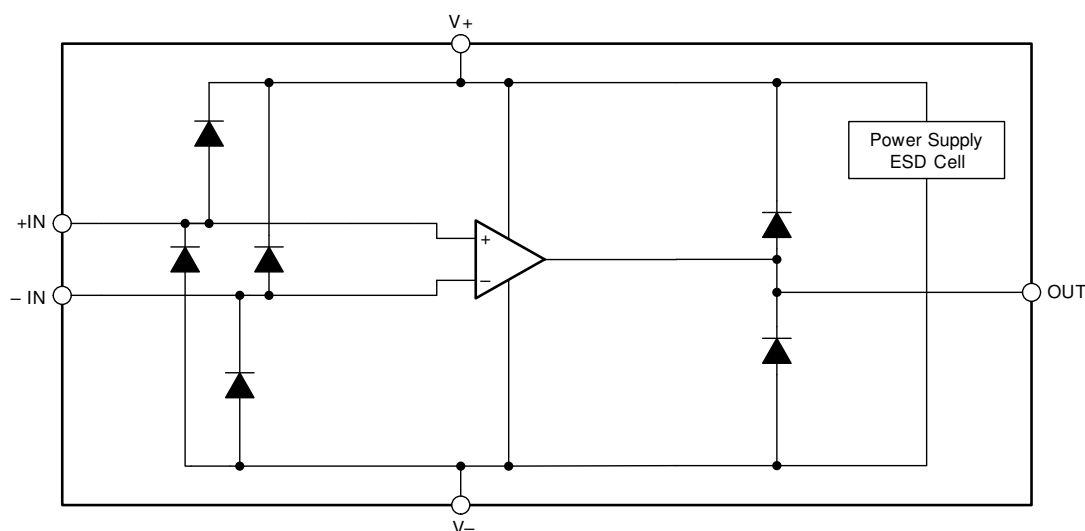


Figure 7-1. Equivalent Internal ESD Circuitry

7.3.5 EMI Susceptibility and Input Filtering

Texas Instruments has developed the ability to accurately measure and quantify the immunity of an operational amplifier over a broad frequency spectrum extending from 10 MHz to 6 GHz. The [Figure 6-28](#) plot illustrates the performance of the LM290xLV family's EMI filters across a wide range of frequencies. For more detailed information, see *EMI Rejection Ratio of Operational Amplifiers* available for download from www.ti.com.

7.4 Device Functional Modes

The LM290xLV family has a single functional mode. The devices are powered on as long as the power-supply voltage is between 2.7 V (± 1.35 V) and 5.5 V (± 2.75 V).

8 Application and Implementation

Note

以下のアプリケーション情報は、TI の製品仕様に含まれるものではなく、TI ではその正確性または完全性を保証いたしません。個々の目的に対する製品の適合性については、お客様の責任で判断していただくことになります。お客様は自身の設計実装を検証しテストすることで、システムの機能を確認する必要があります。

8.1 Application Information

The LM290xLV devices are a family of low-power, cost-optimized operational amplifiers. The devices operate from 2.7 V to 5.5 V, are unity-gain stable, and are suitable for a wide range of general-purpose applications. The input common-mode voltage range includes the negative rail, and allows the LM290xLV to be used in any single-supply applications.

8.2 Typical Application

図 8-1 shows the LM290xLV device configured in a low-side current sensing application.

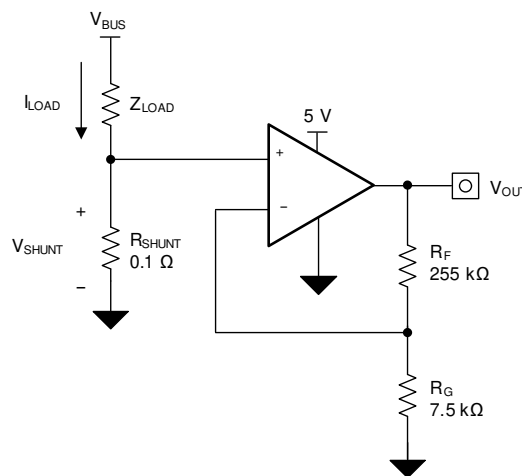


図 8-1. LM290xLV Device in a Low-Side, Current-Sensing Application

8.2.1 Design Requirements

The design requirements for this design are:

- Load current: 0 A to 1 A
- Output voltage: 3.5 V
- Maximum shunt voltage: 100 mV

8.2.2 Detailed Design Procedure

The transfer function of the circuit in 図 8-1 is given in 式 1:

$$V_{OUT} = I_{LOAD} \times R_{SHUNT} \times \text{Gain} \quad (1)$$

The load current (I_{LOAD}) produces a voltage drop across the shunt resistor (R_{SHUNT}). The load current is set from 0 A to 1 A. To keep the shunt voltage below 100 mV at maximum load current, the largest allowable shunt resistor is shown using 式 2:

$$R_{SHUNT} = \frac{V_{SHUNT_MAX}}{I_{LOAD_MAX}} = \frac{100\text{mV}}{1\text{A}} = 100\text{m}\Omega \quad (2)$$

Using 式 2, R_{SHUNT} is calculated to be 100 mΩ. The voltage drop produced by I_{LOAD} and R_{SHUNT} is amplified by the LM290xLV device to produce an output voltage of approximately 0 V to 3.5 V. The gain needed by the LM290xLV to produce the necessary output voltage is calculated using 式 3:

$$\text{Gain} = \frac{(V_{OUT_MAX} - V_{OUT_MIN})}{(V_{IN_MAX} - V_{IN_MIN})} \quad (3)$$

Using 式 3, the required gain is calculated to be 35 V/V, which is set with resistors R_F and R_G . 式 4 sizes the resistors R_F and R_G , to set the gain of the LM290xLV device to 35 V/V.

$$\text{Gain} = 1 + \frac{(R_F)}{(R_G)} \quad (4)$$

8.2.3 Application Curve

Selecting R_F as 255 kΩ and R_G as 7.5 kΩ provides a combination that equals 35 V/V. 图 8-2 shows the measured transfer function of the circuit shown in 图 8-1. Notice that the gain is only a function of the feedback and gain resistors. This gain is adjusted by varying the ratio of the resistors and the actual resistors values are determined by the impedance levels that the designer wants to establish. The impedance level determines the current drain, the effect that stray capacitance has, and a few other behaviors. There is no optimal impedance selection that works for every system, you must choose an impedance that is ideal for your system parameters.

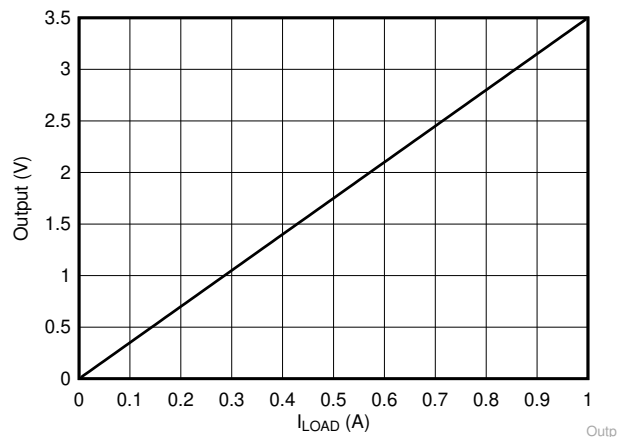


图 8-2. Low-Side, Current-Sense Transfer Function

9 Power Supply Recommendations

The LM290xLV family is specified for operation from 2.7 V to 5.5 V (± 1.35 V to ± 2.75 V); many specifications apply from -40°C to 125°C . [セクション 6.6](#) presents parameters that may exhibit significant variance with regard to operating voltage or temperature.

CAUTION

Supply voltages larger than 6 V may permanently damage the device; see the [セクション 6.1](#).

Place 0.1- μF bypass capacitors close to the power-supply pins to reduce coupling errors from noisy or high-impedance power supplies. For more detailed information on bypass capacitor placement, see [セクション 10.1](#).

9.1 Input and ESD Protection

The LM290xLV family incorporates internal ESD protection circuits on all pins. For input and output pins, this protection primarily consists of current-steering diodes connected between the input and power-supply pins. These ESD protection diodes provide in-circuit, input overdrive protection, as long as the current is limited to 10 mA, as stated in the section. [図 9-1](#) shows how a series input resistor can be added to the driven input to limit the input current. The added resistor contributes thermal noise at the amplifier input and the value must be kept to a minimum in noise-sensitive applications.

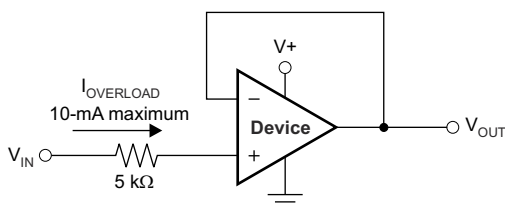


図 9-1. Input Current Protection

10 Layout

10.1 Layout Guidelines

For best operational performance of the device, use good printed circuit board (PCB) layout practices, including:

- Noise can propagate into analog circuitry through the power pins of the circuit as a whole and of the op amp itself. Bypass capacitors are used to reduce the coupled noise by providing low-impedance power sources local to the analog circuitry.
 - Connect low-ESR, 0.1- μ F ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from V+ to ground is applicable for single-supply applications.
- Separate grounding for analog and digital portions of circuitry is one of the simplest and most effective methods of noise suppression. One or more layers on multilayer PCBs are usually devoted to ground planes. A ground plane helps distribute heat and reduces electromagnetic interference (EMI) noise pickup. Take care to physically separate digital and analog grounds. Use thermal signatures or EMI measurement techniques to determine where the majority of the ground current is flowing and be sure to route this path away from sensitive analog circuitry. For more detailed information, see [Circuit Board Layout Techniques](#).
- To reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If these traces cannot be kept separate, crossing the sensitive trace at a 90° angle is much better as opposed to running the traces in parallel with the noisy trace.
- Place the external components as close to the device as possible, as shown in [Figure 10-2](#). Keeping R_F and R_G close to the inverting input minimizes parasitic capacitance.
- Keep the length of input traces as short as possible. Remember that the input traces are the most sensitive part of the circuit.
- Consider a driven, low-impedance guard ring around the critical traces. A guard ring may significantly reduce leakage currents from nearby traces that are at different potentials.
- Cleaning the PCB following board assembly is recommended for best performance.
- Any precision integrated circuit can experience performance shifts resulting from moisture ingress into the plastic package. Following any aqueous PCB cleaning process, baking the PCB assembly is recommended to remove moisture introduced into the device packaging during the cleaning process. A low-temperature, post-cleaning bake at 85°C for 30 minutes is sufficient for most circumstances.

10.2 Layout Example

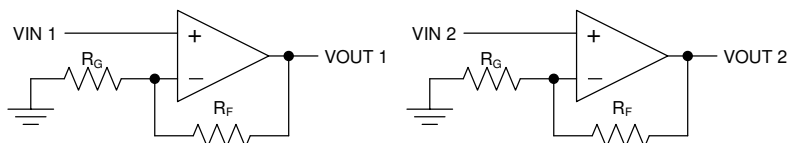


Figure 10-1. Schematic Representation for

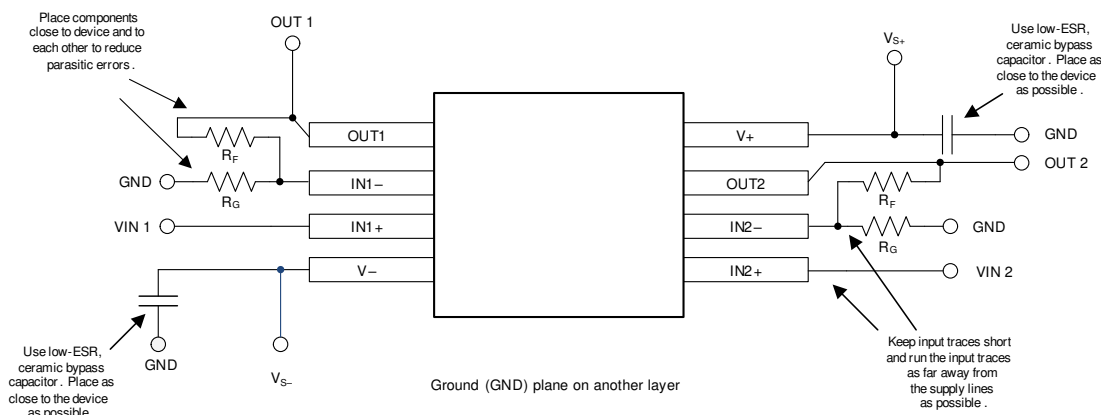


Figure 10-2. Layout Example

11 Device and Documentation Support

11.1 Documentation Support

11.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, [EMI Rejection Ratio of Operational Amplifiers](#)

11.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](#). Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.3 サポート・リソース

TI E2E™ サポート・フォーラムは、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計に必要な支援を迅速に得ることができます。

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11.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.

すべての商標は、それぞれの所有者に帰属します。

11.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.6 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most-current data available for the designated devices. This data is subject to change without notice and without revision of this document. For browser-based versions of this data sheet, see the left-hand navigation pane.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LM2902LVIDR	Active	Production	SOIC (D) 14	2500 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	LM2902LV
LM2902LVIDR.A	Active	Production	SOIC (D) 14	2500 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	LM2902LV
LM2902LVIDYYR	Active	Production	SOT-23-THIN (DYY) 14	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LM2902I
LM2902LVIDYYR.A	Active	Production	SOT-23-THIN (DYY) 14	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LM2902I
LM2902LVIPWR	Active	Production	TSSOP (PW) 14	2000 LARGE T&R	Yes	NIPDAU SN	Level-2-260C-1 YEAR	-40 to 125	(LM2902LV, M2902LV)
LM2902LVIPWR.A	Active	Production	TSSOP (PW) 14	2000 LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	(LM2902LV, M2902LV)
LM2904LVIDDFR	Active	Production	SOT-23-THIN (DDF) 8	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	L904
LM2904LVIDDFR.A	Active	Production	SOT-23-THIN (DDF) 8	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	L904
LM2904LVIDGKR	Active	Production	VSSOP (DGK) 8	2500 LARGE T&R	Yes	NIPDAU SN NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	1SQX
LM2904LVIDGKR.A	Active	Production	VSSOP (DGK) 8	2500 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	1SQX
LM2904LVIDR	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU SN	Level-2-260C-1 YEAR	-40 to 125	2904LV
LM2904LVIDR.A	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	2904LV
LM2904LVIPWR	Active	Production	TSSOP (PW) 8	2000 LARGE T&R	Yes	NIPDAU SN	Level-2-260C-1 YEAR	-40 to 125	2904
LM2904LVIPWR.A	Active	Production	TSSOP (PW) 8	2000 LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	2904

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

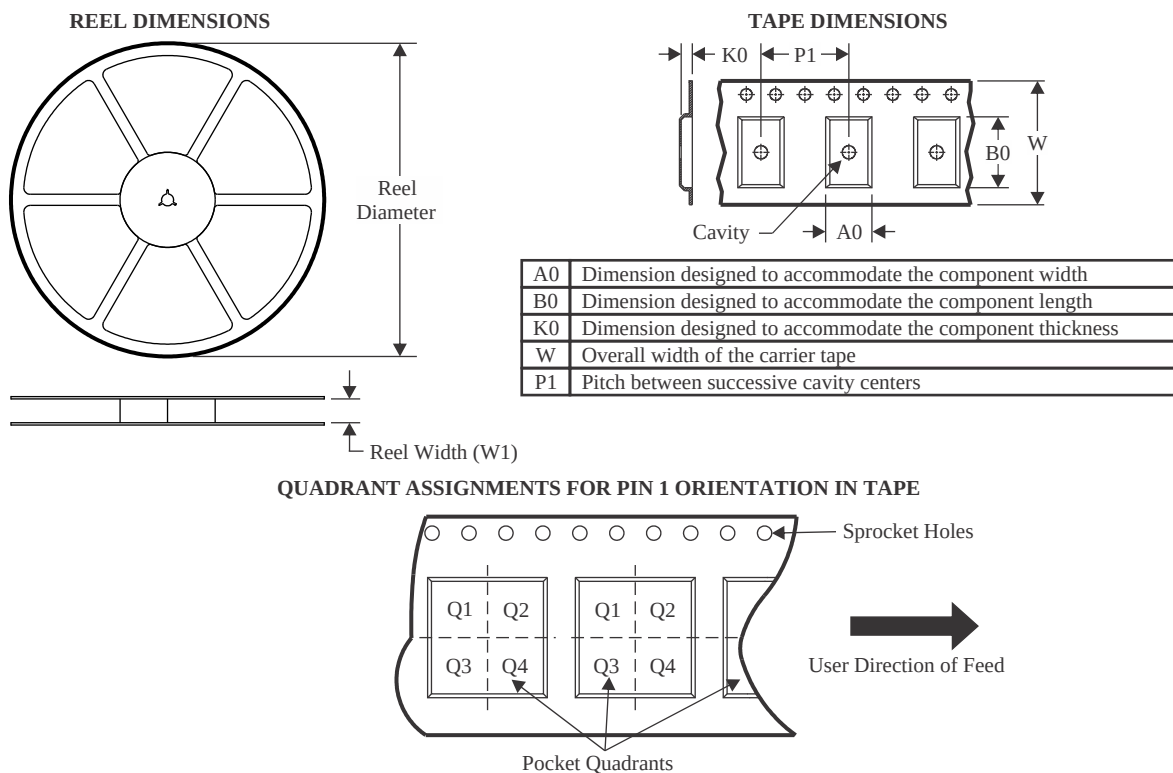
OTHER QUALIFIED VERSIONS OF LM2902LV, LM2904LV :

- Automotive : [LM2902LV-Q1](#), [LM2904LV-Q1](#)

NOTE: Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

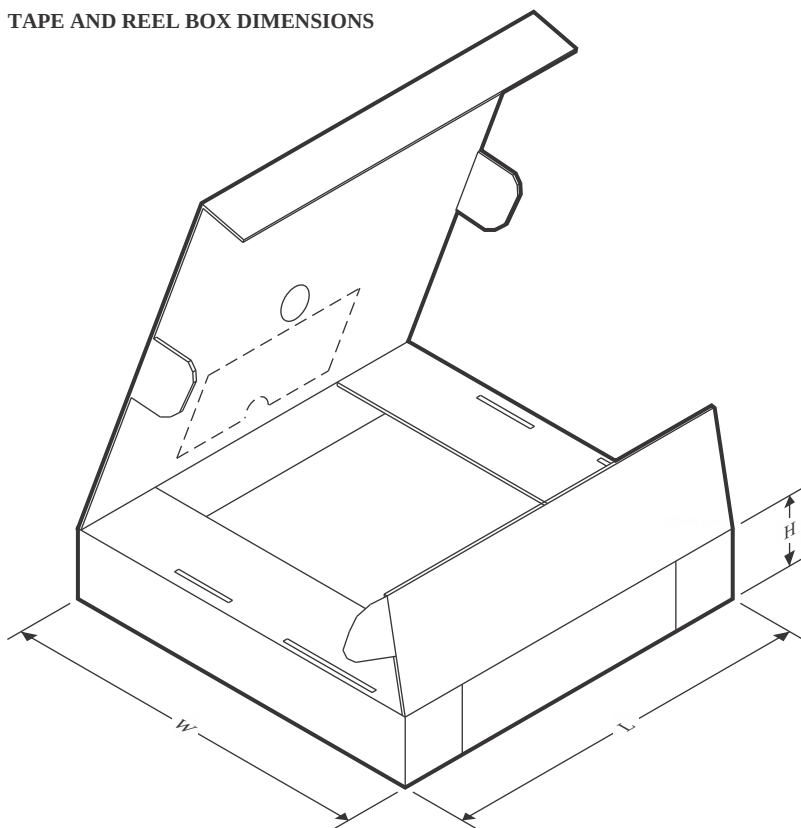
TAPE AND REEL INFORMATION



*All dimensions are nominal

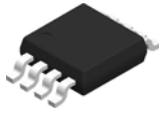
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM2902LVIDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
LM2902LVIDYYR	SOT-23-THIN	DYY	14	3000	330.0	12.4	4.8	3.6	1.6	8.0	12.0	Q3
LM2902LVIPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
LM2904LVDDFR	SOT-23-THIN	DDF	8	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LM2904LVIDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM2904LVIDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM2904LVIPWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS

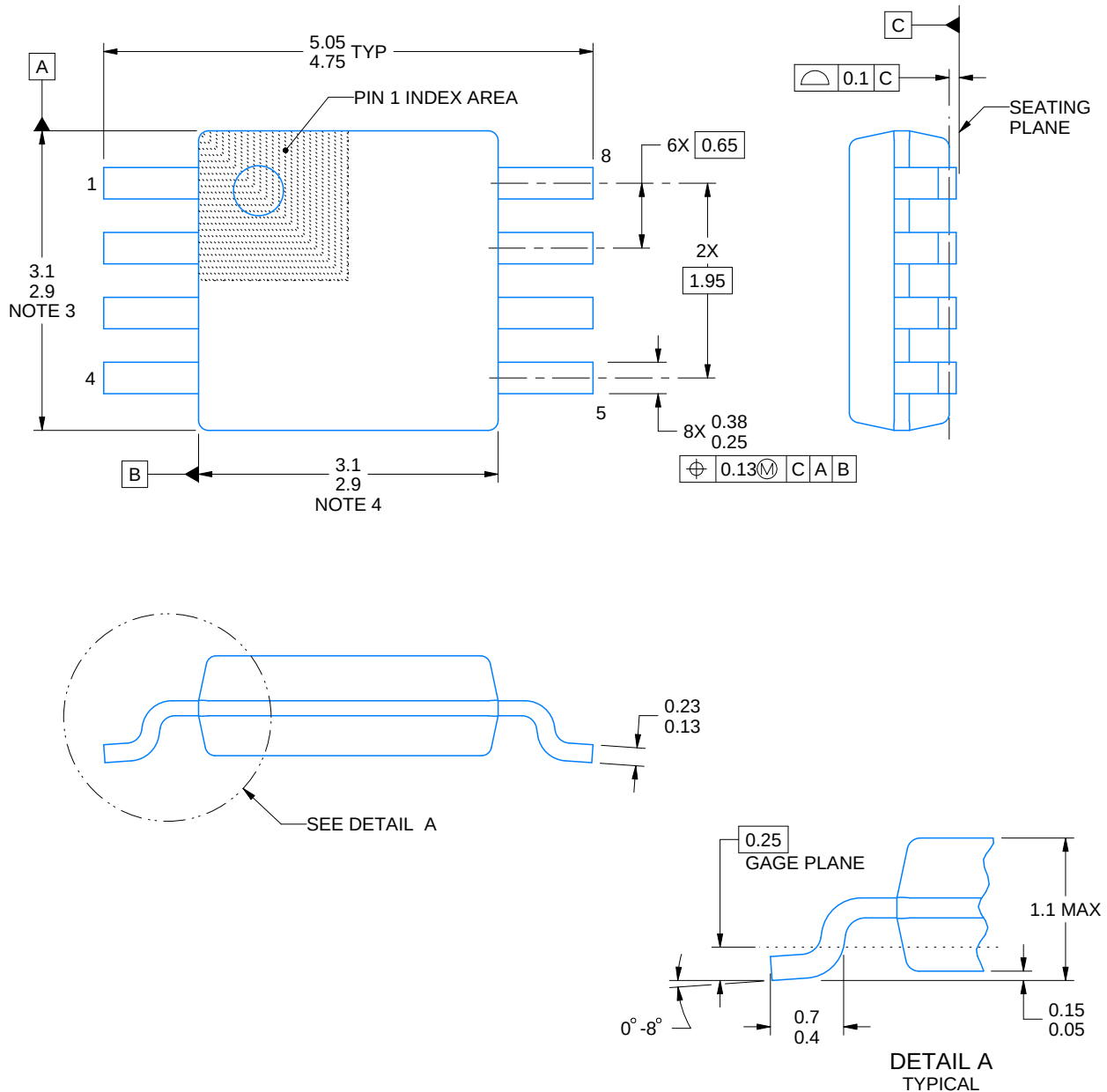


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM2902LVIDR	SOIC	D	14	2500	353.0	353.0	32.0
LM2902LVIDYYR	SOT-23-THIN	DYY	14	3000	336.6	336.6	31.8
LM2902LVIPWR	TSSOP	PW	14	2000	353.0	353.0	32.0
LM2904LVIDDFR	SOT-23-THIN	DDF	8	3000	210.0	185.0	35.0
LM2904LVIDGKR	VSSOP	DGK	8	2500	356.0	356.0	36.0
LM2904LVIDR	SOIC	D	8	2500	353.0	353.0	32.0
LM2904LVIPWR	TSSOP	PW	8	2000	353.0	353.0	32.0

DGK0008A**PACKAGE OUTLINE****VSSOP - 1.1 mm max height**

SMALL OUTLINE PACKAGE



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NOTES:

PowerPAD is a trademark of Texas Instruments.

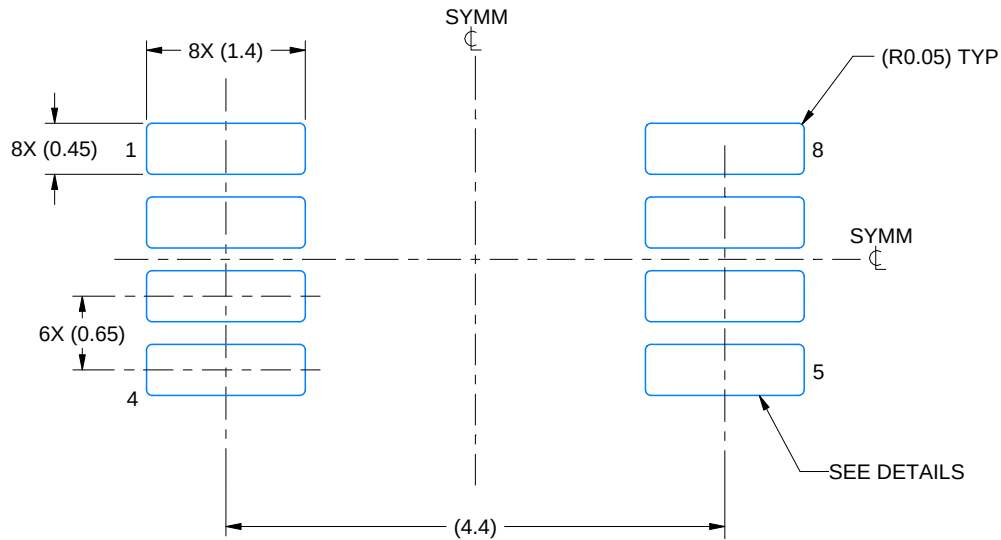
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.

EXAMPLE BOARD LAYOUT

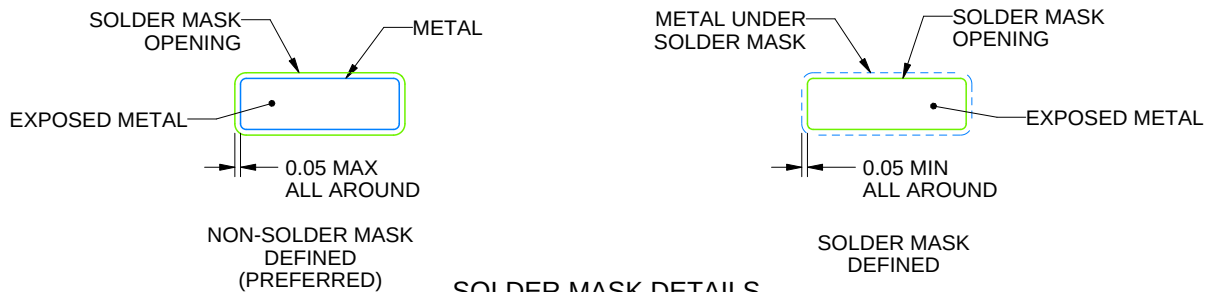
DGK0008A

TM VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X



SOLDER MASK DETAILS

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NOTES: (continued)

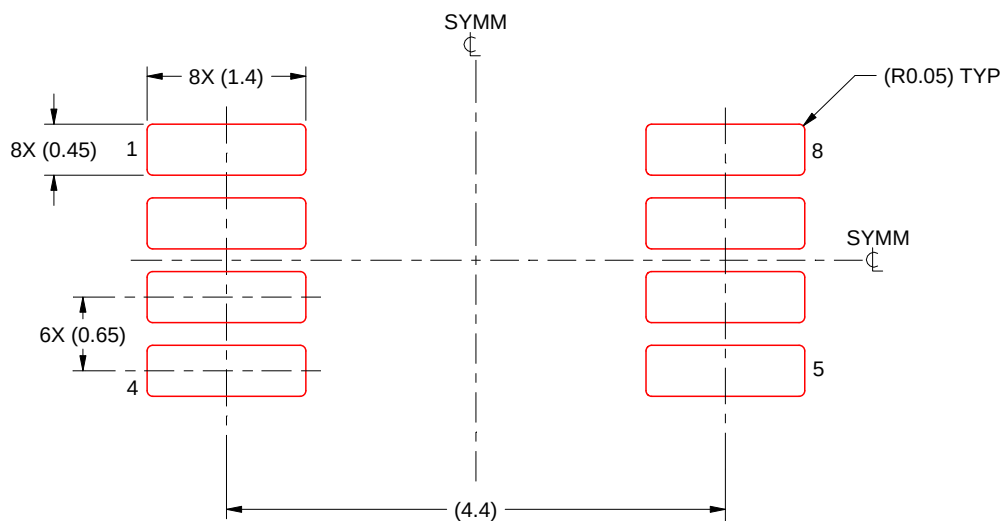
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.

EXAMPLE STENCIL DESIGN

DGK0008A

TM VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE

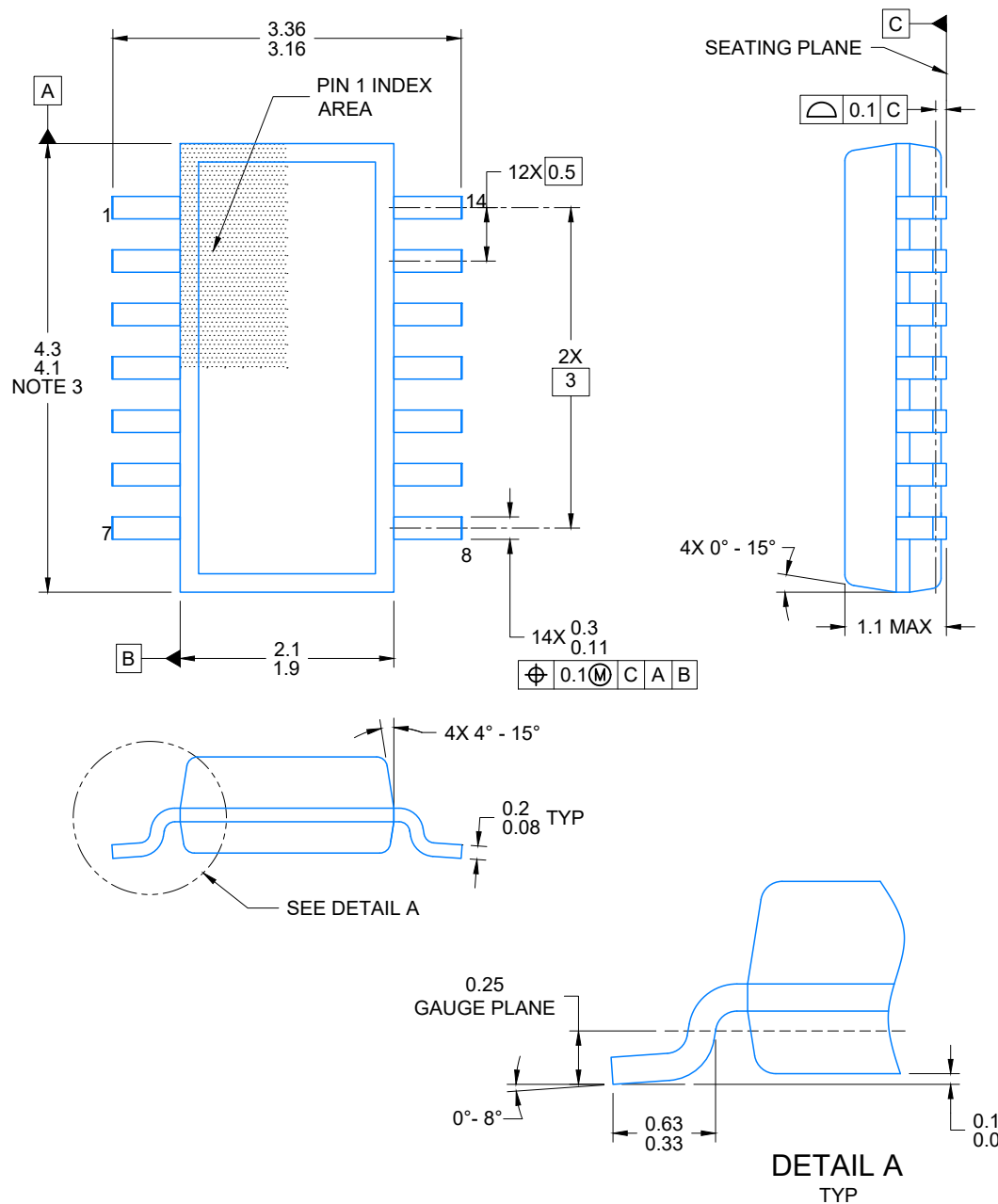


SOLDER PASTE EXAMPLE
SCALE: 15X

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NOTES: (continued)

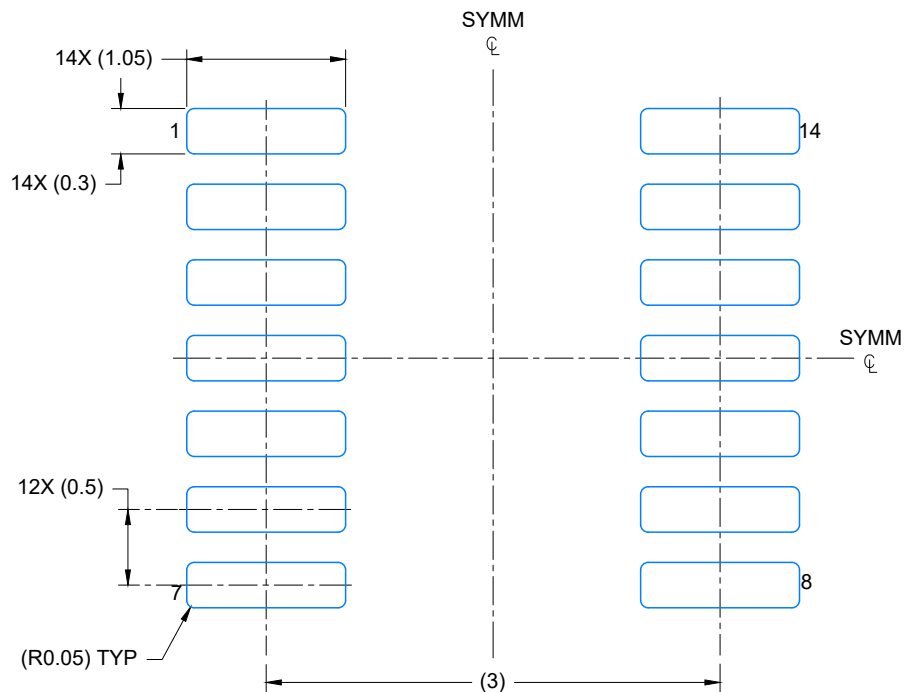
11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.



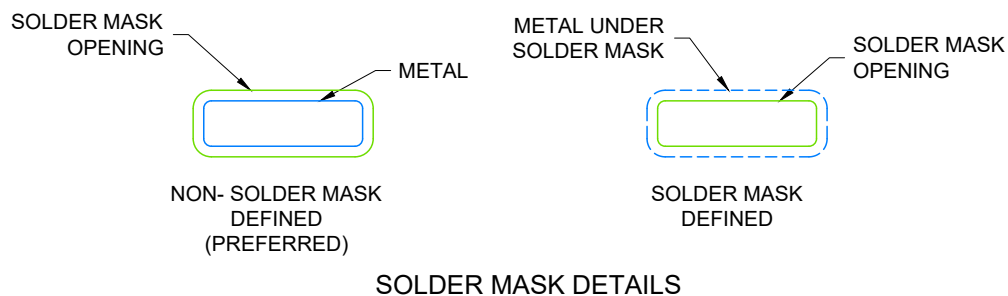
4224643/D 07/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
5. Reference JEDEC Registration MO-345, Variation AB



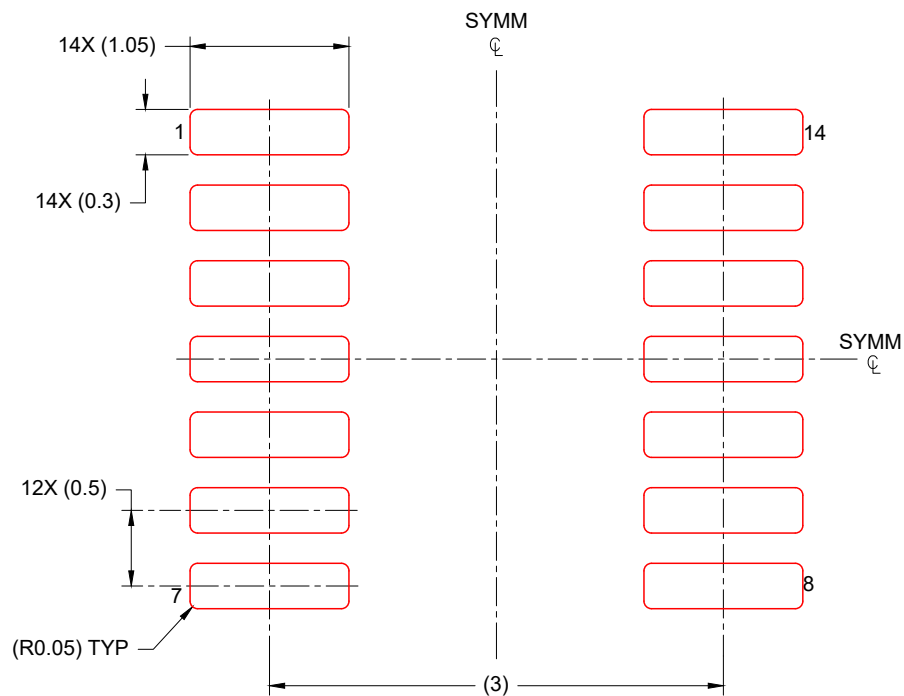
LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X



4224643/D 07/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

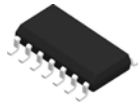


SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 20X

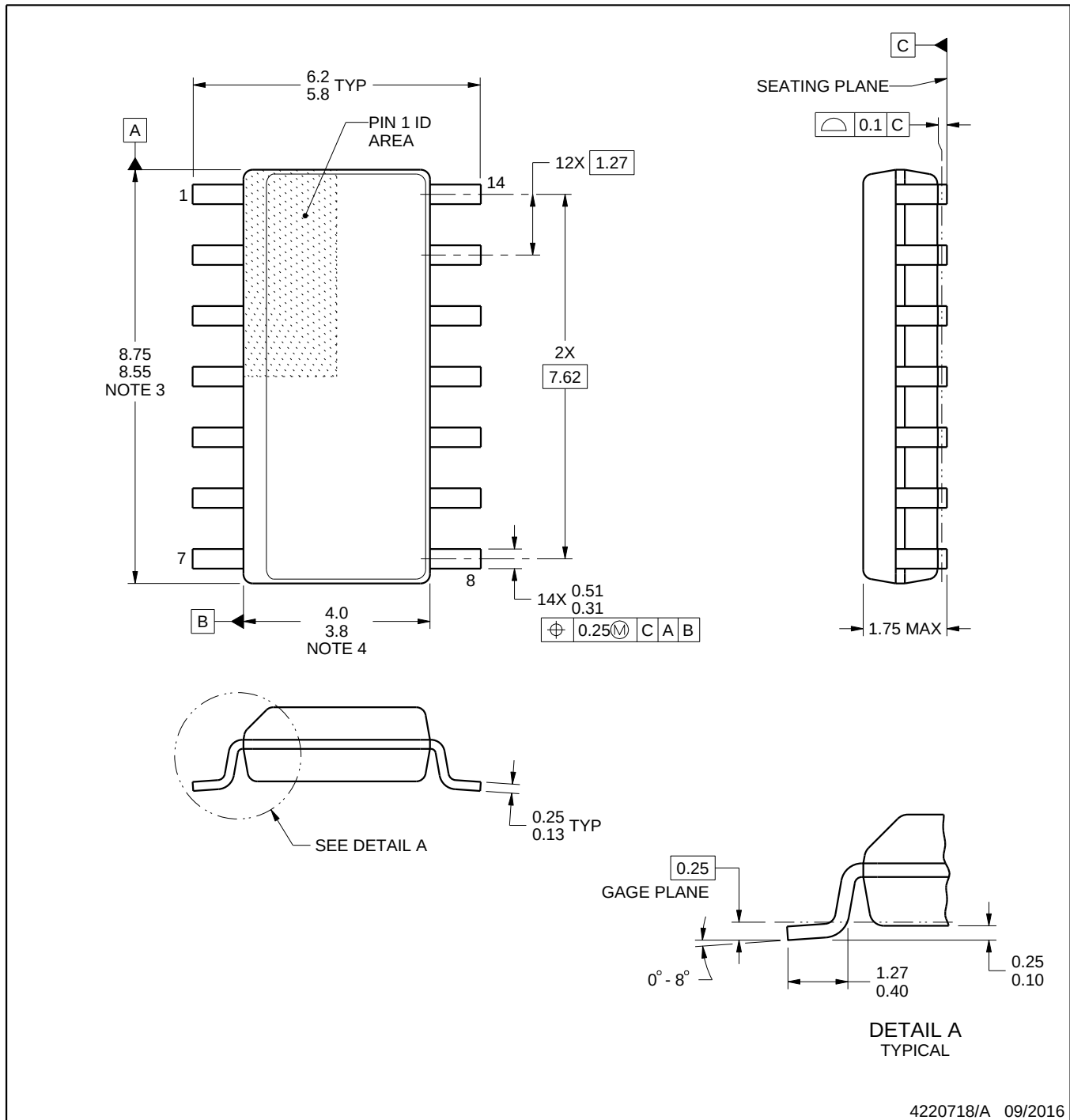
4224643/D 07/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

D0014A**PACKAGE OUTLINE****SOIC - 1.75 mm max height**

SMALL OUTLINE INTEGRATED CIRCUIT

**NOTES:**

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.



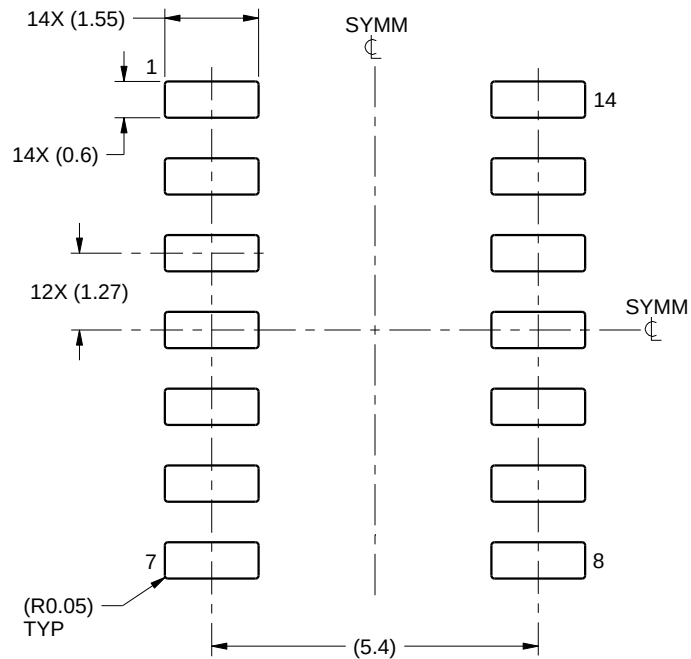
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EXAMPLE BOARD LAYOUT

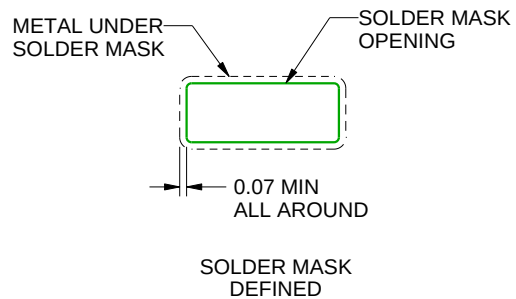
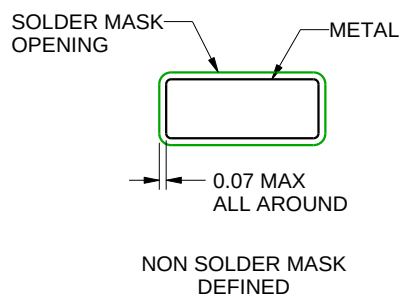
D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE
SCALE:8X



SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

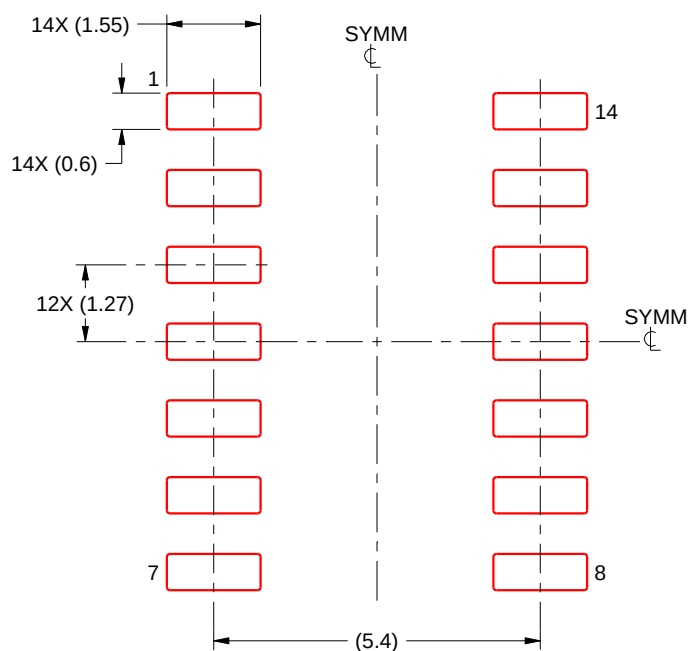
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

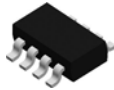


SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

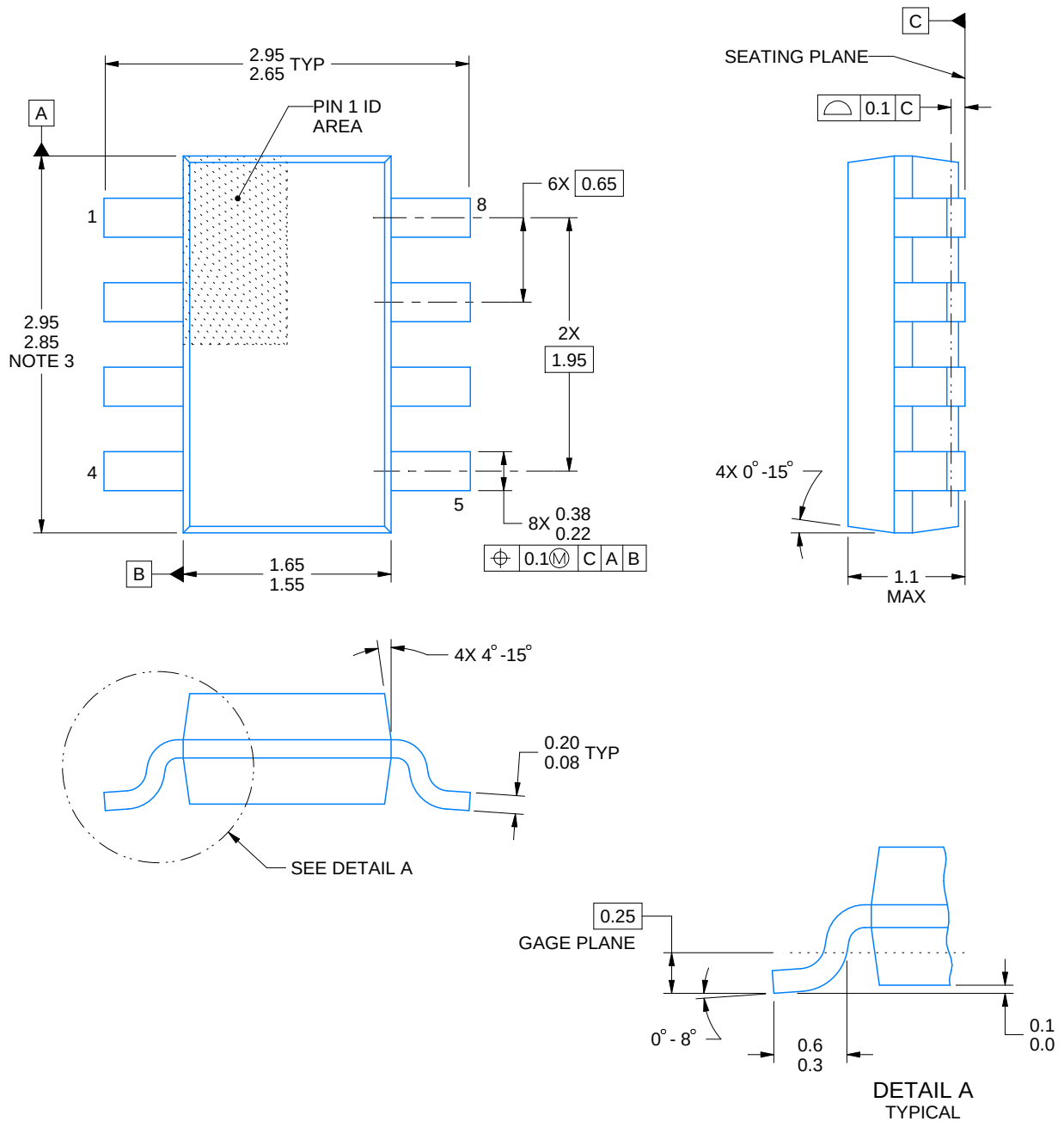
4220718/A 09/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

DDF0008A**PACKAGE OUTLINE****SOT-23-THIN - 1.1 mm max height**

PLASTIC SMALL OUTLINE



4222047/E 07/2024

NOTES:

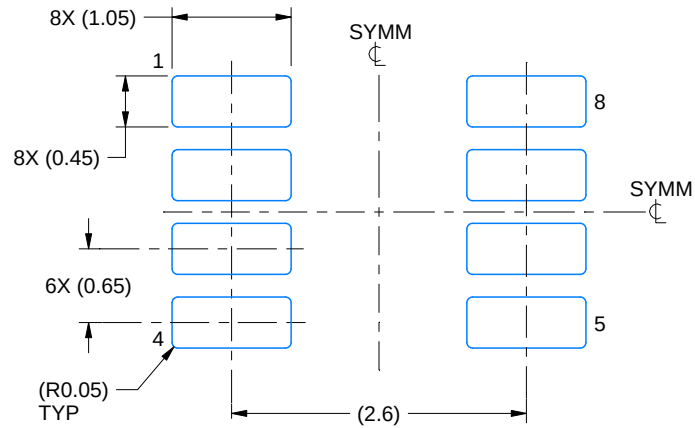
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.

EXAMPLE BOARD LAYOUT

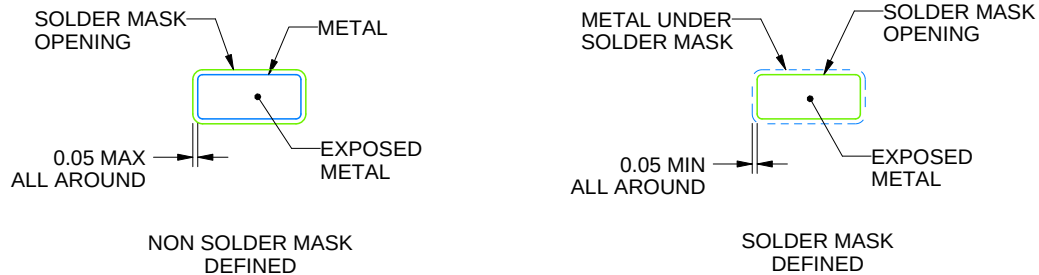
DDF0008A

SOT-23-THIN - 1.1 mm max height

PLASTIC SMALL OUTLINE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

4222047/E 07/2024

NOTES: (continued)

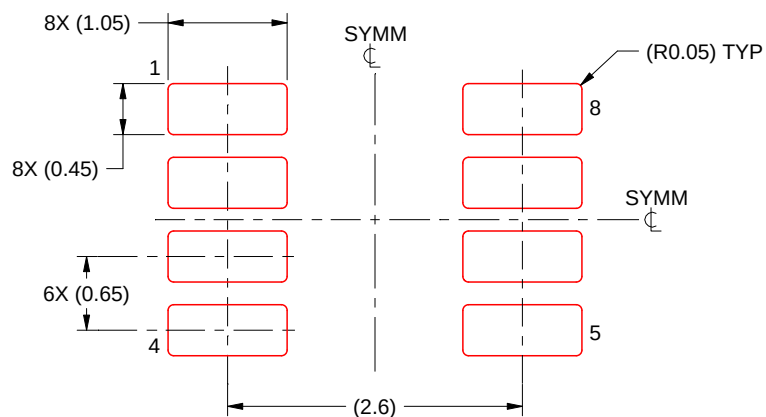
4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DDF0008A

SOT-23-THIN - 1.1 mm max height

PLASTIC SMALL OUTLINE

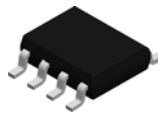


SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4222047/E 07/2024

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.

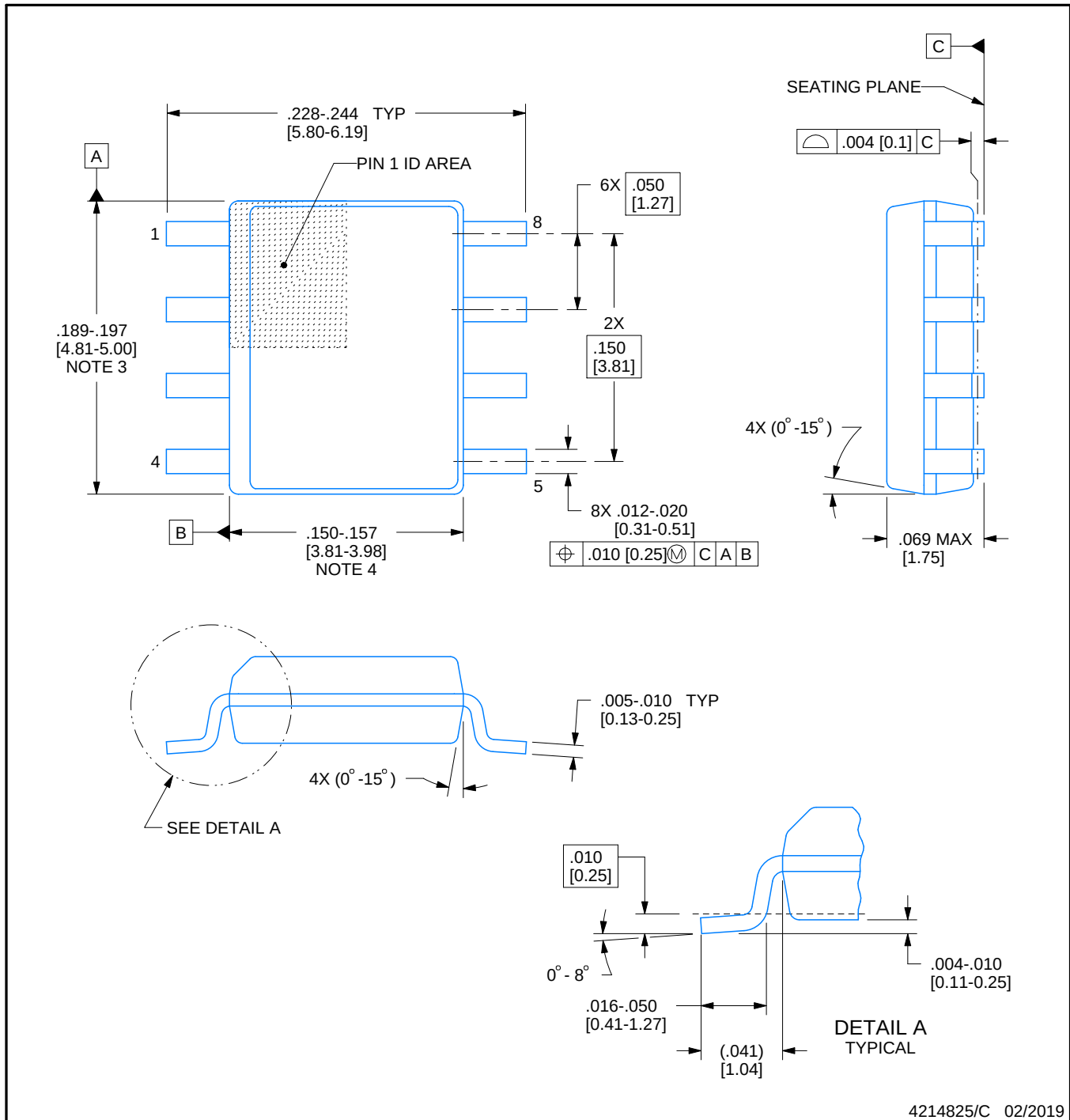


D0008A

PACKAGE OUTLINE

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



4214825/C 02/2019

NOTES:

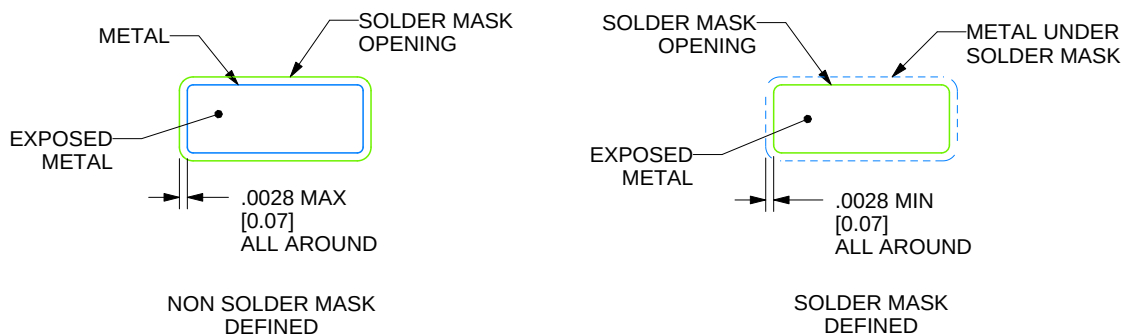
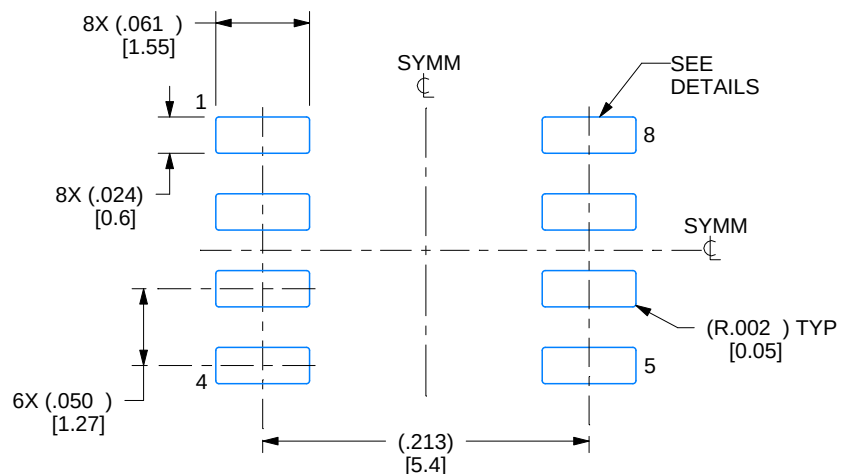
1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.

EXAMPLE BOARD LAYOUT

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



4214825/C 02/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

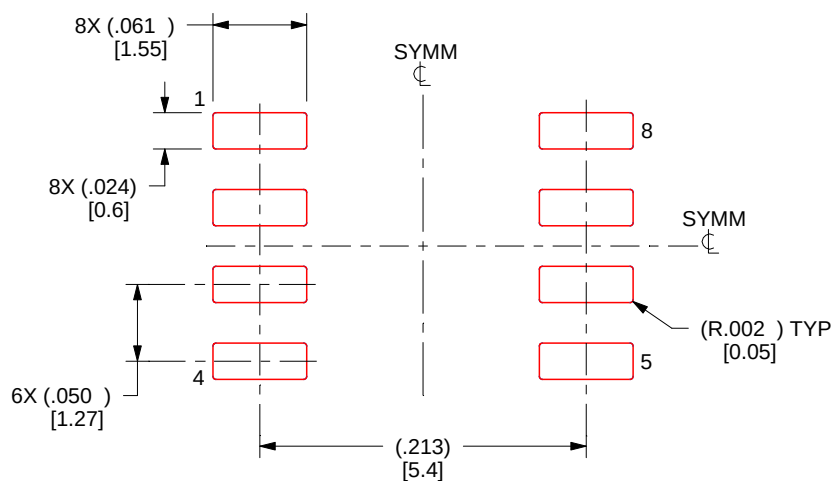
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

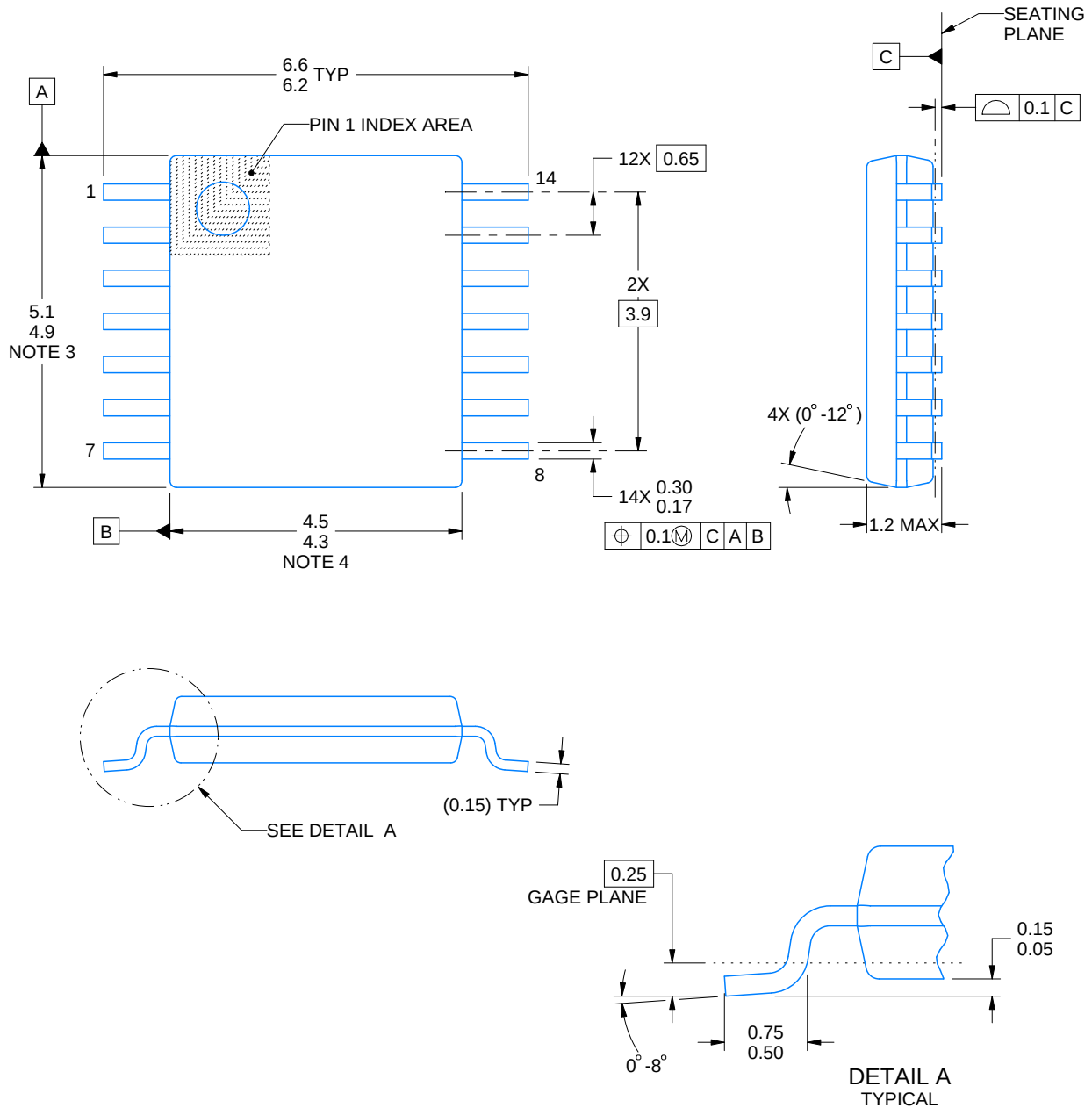
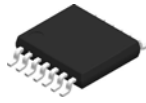


SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.



4220202/B 12/2023

NOTES:

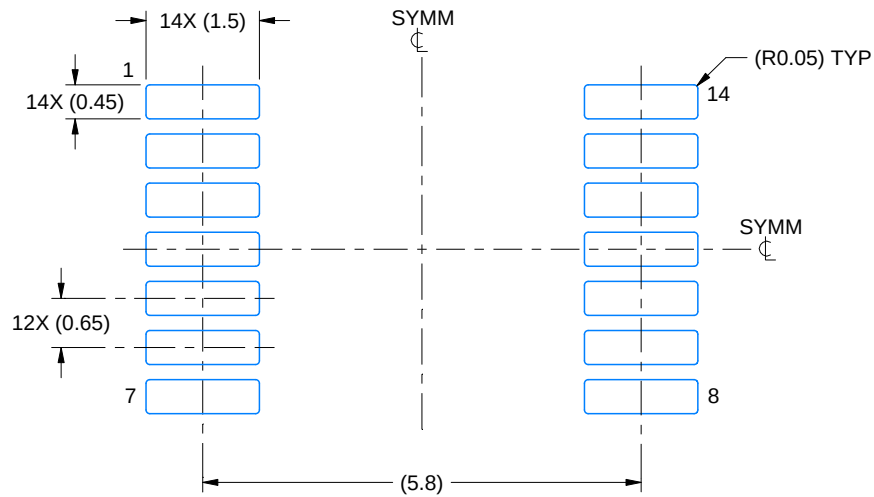
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

EXAMPLE BOARD LAYOUT

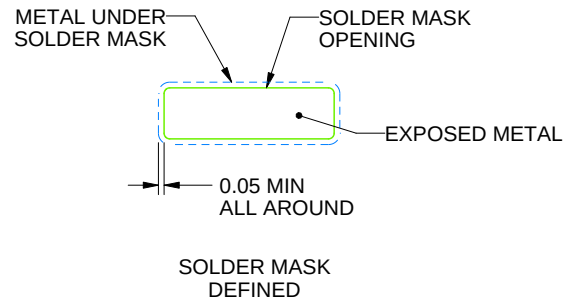
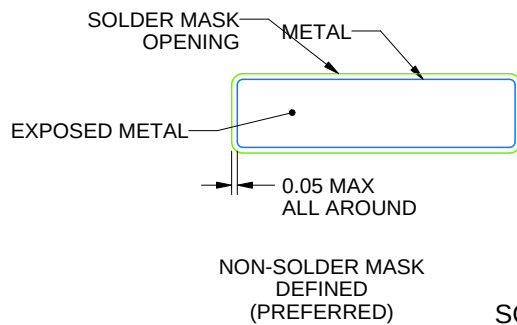
PW0014A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



SOLDER MASK DETAILS

4220202/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

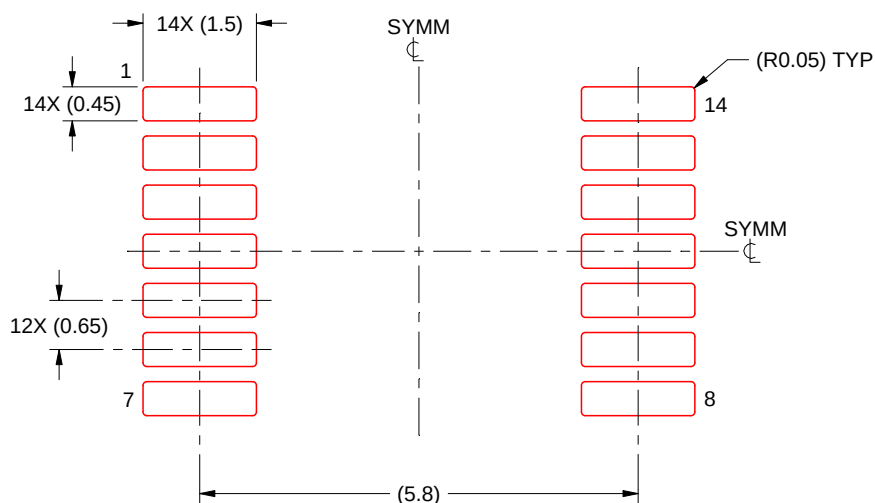
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0014A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220202/B 12/2023

NOTES: (continued)

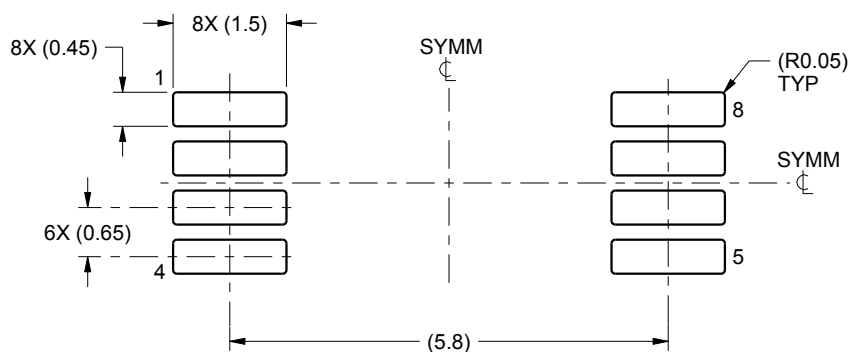
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

EXAMPLE BOARD LAYOUT

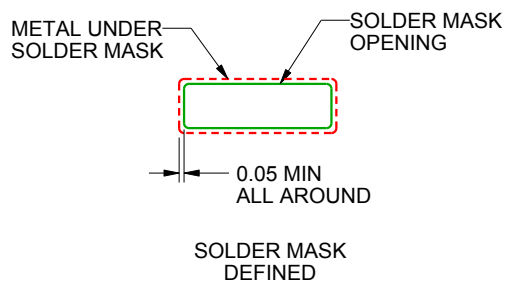
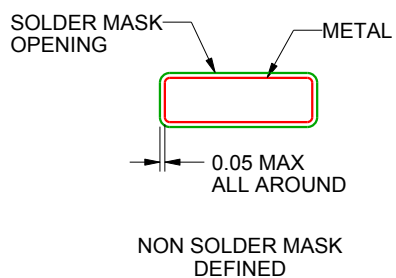
PW0008A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
SCALE:10X



SOLDER MASK DETAILS
NOT TO SCALE

4221848/A 02/2015

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

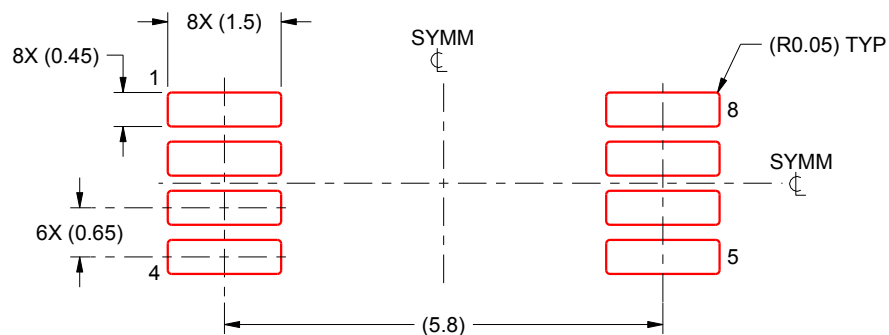
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0008A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:10X

4221848/A 02/2015

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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最終更新日：2025 年 10 月