LM2903-Q1 および LM2903B-Q1 車載用デュアル コンパレータ

特長

- 車載アプリケーション認定済み
- 以下の結果で AEC-Q100 認定済み:
  - デバイス温度グレード 0:-40℃～150℃の動作時周囲温度範囲 (LM2903E-Q1)
  - デバイス温度グレード 1:動作時周囲温度範囲 -40℃～125℃
  - デバイス HBM ESD 分類レベル H1C
  - デバイス CDM ESD 分類レベル C4B
- 「B」デバイスの HBM ESD を 2kV に改善
- 「B」デバイスでは 3 温度テストが利用可能
- シングル電源またはデュアル電源
- 電源電圧に依存しない低い消費電流、コンパレータあたり 200µA (代表値) (「B」バージョン)
- 低い入力バイアス電流、3.5nA (代表値) (「B」デバイス)
- 低い入力オフセット電流、0.5nA (代表値) (「B」デバイス)
- 低い入力オフセット電圧、±0.37mV (代表値) (「B」デバイス)
- 同相入力電圧範囲にグランドを含む
- 差動入力電圧範囲は最大定格電源電圧と同じ ±36V
- TTL、MOS、CMOS 互換出力
- 機能安全対応
  - 機能安全システムの設計に役立つ資料を利用可能

アプリケーション

- 車載用
  - HEV/EV およびパワートレイン
  - インフォテインメントおよびクラスタ
  - ボディ コントロール モジュール
- 産業用
- 電化製品

概要

LM2903B-Q1 デバイスは、業界標準の LM2903-Q1 コンパレータ ファミリの次世代バージョンです。この次世代ファミリは、小さいオフセット電圧、高い電源電圧への対応、小さい消費電流、小さい入力バイアス電流、短い伝搬遅延時間、優れた 2kV の ESD 性能などの特長と、ドロップイン互換で置換可能という利便性を兼ね備えており、コスト制約が厳しい用途で大きな価値を提供します。

すべてのデバイスは、広い電圧範囲にわたって動作するように設計された 2 つの独立した電圧コンパレータで構成されています。デュアル電源でも、2 つの電源間の差分が 2V～36V の範囲内であり、VCC が入力同相電圧より 1.5V 以上高ければ、動作可能です。出力は、他のオープン コレクタ出力に接続できます。

LM2903-Q1 と LM2903B-Q1 は、AEC-Q100 グレード 1 の温度範囲 (-40℃～+125℃) で認定済みです。LM2903E-Q1 はグレード 0 の拡張温度範囲 (-40℃～+150℃) で認定済みです。

製品情報

部品番号	パッケージ (1)	本体サイズ (公称)
LM2903B-Q1	SOIC (8)	4.90mm × 3.91mm
	TSSOP (8)	3.00mm × 4.40mm
	VSSOP(8)	3.00 mm × 3.00mm
	WSON (8)	2.00 mm × 2.00mm
	SOT-23 (8)	1.60mm × 2.90mm
LM2903-Q1	SOIC (8)	4.90mm × 3.91mm
	TSSOP (8)	3.00mm × 4.40mm
	VSSOP(8)	3.00 mm × 3.00mm
LM2903E-Q1	TSSOP (8)	3.00mm × 4.40mm

(1) 利用可能なすべてのパッケージについては、データシートの末尾にある注文情報を参照してください。

ファミリ比較表

仕様	LM2903B-Q1	LM2903-Q1	LM2903-Q1 「A」デバイス	LM2903-Q1 「AV」デバイス	LM2903E-Q1	単位
電源電圧仕様	2～36	2～30	2～30	2～32	2～30	V
総電源電流 (5V～V_S (最大値))	0.6～0.8	1～2.5	1～2.5	1～2.5	1～2.5	mA
温度範囲	-40～125	-40～125	-40～125	-40～125	-40～150	℃
ESD (HBM / CDM)	2k / 1k	1k / 750	1k / 750	1k / 750	1k / 750	V
オフセット電圧 (全温度範囲での最大値)	±4	±15	±4	±4	±15	mV
入力バイアス電流 (標準値 / 最大値)	3.5 / 25	25 / 250	25 / 250	25 / 250	25 / 250	nA
応答時間 (標準値)	1	1.3	1.3	1.3	1.3	µsec

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1 Pin Configuration and Functions

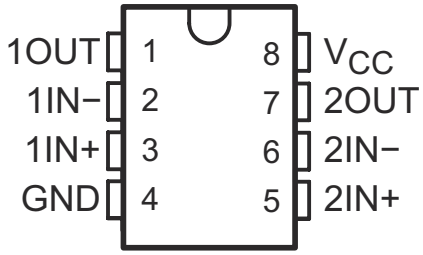
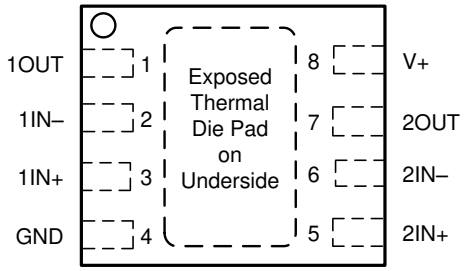


図 1-1. D, DGK, DDF OR PW PACKAGE
Top View



Connect thermal pad directly to GND pin.

図 1-2. DSG Package
8-Pin WSON With Exposed Pad
Top View

1.1 Pin Functions

PIN			I/O	DESCRIPTION
NAME	SOIC, VSSOP, PDIP, SO, DDF and TSSOP	DSG		
1OUT	1	1	Output	Output pin of comparator 1
1IN–	2	2	Input	Negative input pin of comparator 1
1IN+	3	3	Input	Positive input pin of comparator 1
GND	4	4	—	Ground
2IN+	5	5	Input	Positive input pin of comparator 2
2IN-	6	6	Input	Negative input pin of comparator 2
2OUT	7	7	Output	Output pin of comparator 2
V_{CC}	8	8	—	Positive Supply
Thermal Pad	—	PAD	—	Connect directly to GND pin

2 Specifications

2.1 Absolute Maximum Ratings, LM2903-Q1 and LM2903E-Q1

over operating free-air temperature range (unless otherwise noted) (1)

		MIN	MAX	UNIT
V_{CC}	Supply voltage(2)		36	V
V_{CC}	Supply voltage, LM2903E-Q1 Only(2)		32	V
V_{ID}	Differential input voltage(3)	–36	36	V
V_I	Input voltage range (either input)	−0.3	36	V
V_O	Output voltage		36	V
I_O	Output current		20	mA
T_J	Operating virtual-junction temperature		150	°C
T_{SCG}	Duration of output short-circuit to ground		Unlimited	s

(1) Stresses beyond those listed under *Absolute Maximum Ratings* can cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods can affect device reliability.
(2) All voltage values, except differential voltages, are with respect to GND.
(3) Differential voltages are at IN+ with respect to IN−.

2.2 Absolute Maximum Ratings, LM2903B-Q1

over operating free-air temperature range (unless otherwise noted)(1)

	MIN	MAX	UNIT
Supply voltage: V_S = (V+) – (V–)	-0.3	38	V
Differential input voltage : V_{ID} (2)		±38	V
Input pins (IN+, IN–)	-0.3	38	V
Current into input pins (IN+, IN–)		-50	mA
Output pin (OUT)	-0.3	38	V
Output sink current		25	mA
Operating virtual-junction temperature		150	°C
Output short-circuit duration(3)		Unlimited	s

(1) Stresses beyond those listed under *Absolute Maximum Ratings* can cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods can affect device reliability.
(2) Differential voltages are at IN+ with respect to IN-
(3) Short circuits from outputs to V+ can cause excessive heating and eventual destruction.

2.3 ESD Ratings, LM2903-Q1 and LM2903E-Q1

				MIN	MAX	UNIT
T_{stg}	Storage temperature range		LM2903-Q1 Only	–65	150	°C
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002(1)		-1000	1000	V
		Charged device model (CDM), per AEC Q100-011	All pins	-750	750	

(1) AEC Q100-002 indicates HBM stressing is done in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

2.4 ESD Ratings, LM2903B-Q1

				MIN	MAX	UNIT
T_{stg}	Storage temperature range			–65	150	°C
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002(1)		-2000	2000	V
		Charged device model (CDM), per AEC Q100-011	All pins	-1000	1000	

(1) AEC Q100-002 indicates HBM stressing is done in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

2.5 Recommended Operating Conditions, LM2903B-Q1

over operating free-air temperature range (unless otherwise noted)

	MIN	MAX	UNIT
Supply voltage: V_S = (V+) – (V–)	2	36	V
Ambient temperature, T_A, LM2903B	–40	125	°C
Input voltage range, V_{IVR}	–0.1	(V+) – 2	V

2.6 Recommended Operating Conditions, LM2903-Q1

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{CC} (non-V devices)		2	30	V
V_{CC} (V devices)		2	32	V
T_J	Junction Temperature	-40	125	°C

2.7 Recommended Operating Conditions, LM2903E-Q1

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{CC}		2	30	V
T_J	Junction Temperature	-40	150	°C

2.8 Thermal Information

THERMAL METRIC[1]		LM2903x-Q1					UNIT
		D (SOIC)	DGK (VSSOP)	PW (TSSOP)	DSG (WSON)	DDF (SOT-23)	
		8 PINS	8 PINS	8 PINS	8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	154.1	176.5	182.9	102.1	197.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	96.5	85.5	87.1	126.0	119.2	
$R_{\theta JB}$	Junction-to-board thermal resistance	97.7	112.4	123.2	68.6	115.4	
Ψ_{JT}	Junction-to-top characterization parameter	45.7	17.3	16.7	15.9	19.4	
Ψ_{JB}	Junction-to-board characterization parameter	96.9	110.1	120.4	68.4	113.7	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	-	-	-	43.9	-	

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

2.9 Electrical Characteristics LM2903B - Q1

V_S = 5V, V_{CM} = (V–) ; T_A = 25°C (unless otherwise noted).

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage, DGK package only	Input offset voltage, DGK package only	V_S = 5 to 36V	–3.5	±0.37	3.5	mV
V_{IO}	Input offset voltage, DGK package only	Input offset voltage, DGK package only	V_S = 5 to 36V, T_A = –40°C to +125°C	–5		5	mV
V_{IO}	Input offset voltage		V_S = 5 to 36V	–2.5	±0.37	2.5	mV
			V_S = 5 to 36V, T_A = –40°C to +125°C	–4		4	mV
I_B	Input bias current			-25	–3.5		nA
			T_A = –40°C to +125°C	-50			nA
I_{OS}	Input offset current			–10	±0.5	10	nA
			T_A = –40°C to +125°C	–25		25	nA
V_{CM}	Common mode range(1)		V_S = 3 to 36V	(V–)		(V+) – 1.5	V
			V_S = 3 to 36V, T_A = –40°C to +125°C	(V–)		(V+) – 2.0	V
A_{VD}	Large signal differential voltage amplification		V_S = 15V, V_O = 1.4V to 11.4V; R_L ≥ 15k to (V+)	50	200		V/mV
V_{OL}	Low level output Voltage {swing from (V–)}		I_{SINK} ≤ 4mA, V_{ID} = -1V		110	400	mV
			I_{SINK} ≤ 4mA, V_{ID} = -1V T_A = –40°C to +125°C			550	mV
I_{OH-LKG}	High-level output leakage current		(V+) = V_O = 5V; V_{ID} = 1V		0.1	20	nA
			(V+) = V_O = 36V; V_{ID} = 1V		0.3	50	nA
I_{OL}	Low level output current		V_{OL} = 1.5V; V_{ID} = -1V; V_S = 5V	6	21		mA
I_Q	Quiescent current (all comparators)		V_S = 5V, no load		400	600	µA
			V_S = 36V, no load, T_A = –40°C to +125°C		550	800	µA

(1) The voltage at any input should not be allowed to go negative by more than 0.3V. The upper end of the input voltage range is V_{CC} − 1.5V for one input, and the other input can exceed the V_{CC} level; the comparator provides a proper output state. Either or both inputs can go to 36V without damage.

2.10 Switching Characteristics LM2903B - Q1

V_S = 5V, V_{O_PULLUP} = 5V, V_{CM} = V_S/2, C_L = 15pF, R_L = 5.1kOhm, T_A = 25°C (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{response}$	Propagation delay time, high-to-low; TTL input signal (1)	TTL input with V_{ref} = 1.4V		300		ns
$t_{response}$	Propagation delay time, high-to-low; Small scale input signal (1)	Input overdrive = 5mV, Input step = 100mV		1000		ns

(1) High-to-low and low-to-high refers to the transition at the input.

2.11 LM2903B-Q1 "T", "R" and "H" Temperature Test Options

The following table describes the production temperature testing for the LM2903B-Q1 "H", "R" and "T" options. Specifications are the same as the LM2903B-Q1 above.

Test	LM2903B-Q1	LM2903BR-Q1	LM2903BH-Q1	LM2903BT-Q1
Probe (Wafer)	-	25°C	125°C	-40°C and 125°C
Final (Packaged)	25°C	25°C	25°C	25°C

2.12 Electrical Characteristics, LM2903-Q1 and LM2903E-Q1

at specified free-air temperature, V_{CC} = 5V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A (1)	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	V_O = 1.4V, V_{IC} = $V_{IC(min)}$, V_{CC} = 5V to MAX(2)	Non-A devices	25°C		2	7	mV
				Full range			15	
			A-suffix devices	25°C		1	2	
				Full range			4	
I_{IO}	Input offset current	V_O = 1.4V		25°C		5	50	nA
				Full range			200	
I_{IB}	Input bias current	V_O = 1.4V		25°C		−25	−250	nA
				Full range			−500	
V_{ICR}	Common-mode input voltage range(3)			25°C	0 to V_{CC}−1.5			V
				Full range	0 to V_{CC}−2			
A_{VD}	Large-signal differential-voltage amplification	V_{CC} = 15V, V_O = 1.4V to 11.4V, R_L ≥ 15kΩ to V_{CC}		25°C	25	100		V/mV
I_{OH}	High-level output current	V_{OH} = 5V	V_{ID} = 1V	25°C		0.1	50	nA
		V_{OH} = V_{CC} MAX(2)		Full range			1	µA
V_{OL}	Low-level output voltage	I_{OL} = 4mA,	V_{ID} = −1V	25°C		150	400	mV
				Full range			700	
I_{OL}	Low-level output current	V_{OL} = 1.5V,	V_{ID} = −1V	25°C	6			mA
I_{CC}	Supply current	R_L = ∞	V_{CC} = 5V	25°C		0.8	1	mA
			V_{CC} = MAX(2)	Full range			2.5	

(1) Full range (MIN or MAX) for LM2903-Q1 is −40°C to 125°C and −40°C to 150°C for the LM2903E-Q1 . All characteristics are measured with zero common-mode input voltage, unless otherwise specified.
(2) V_{CC} MAX = 30V for non-V devices and 32V for V-suffix devices.
(3) The voltage at either input or common-mode can not be allowed to go negative by more than 0.3V. The upper end of the common-mode voltage range is VCC+ − 1.5V for the inverting input (−), and the non-inverting input (+) can exceed the VCC level; the comparator provides a proper output state. Either or both inputs can go to 30V (32V for V-suffix devices) without damage.

2.13 Switching Characteristics, LM2903-Q1 and LM2903E-Q1

V_{CC} = 5V, T_A = 25°C

PARAMETER	TEST CONDITIONS		TYP	UNIT
Response time	R_L connected to 5V through 5.1kΩ,	100m input step with 5mV overdrive	1.3	µs
	C_L = 15pF(1) (2)	TTL-level input step	0.3	

(1) C_L includes probe and jig capacitance.
(2) The response time specified is the interval between the input step function and the instant when the output crosses 1.4V.

2.14 Typical Characteristics

T_A = 25°C, V_S = 5V, R_{PULLUP} = 5.1k, C_L = 15pF, V_{CM} = 0V, $V_{UNDERDRIVE}$ = 100mV, $V_{OVERDRIVE}$ = 100mV unless otherwise noted.

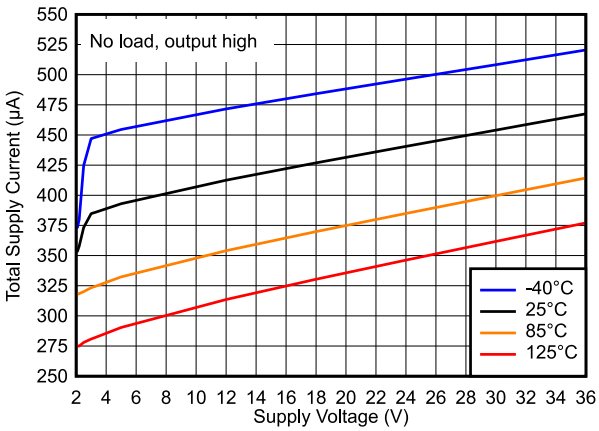


図 2-1. Total Supply Current vs. Supply Voltage

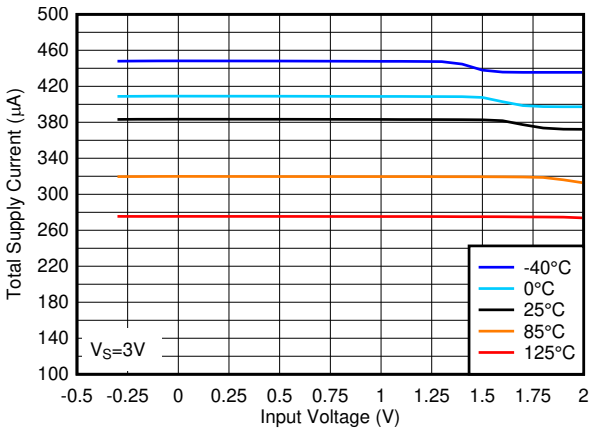


図 2-2. Total Supply Current vs. Input Voltage at 3V

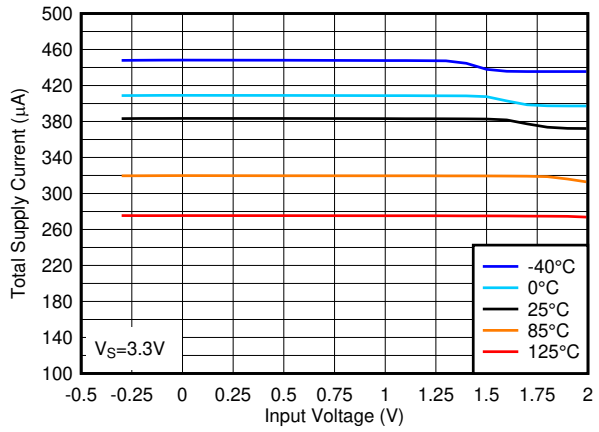


図 2-3. Total Supply Current vs. Input Voltage at 3.3V

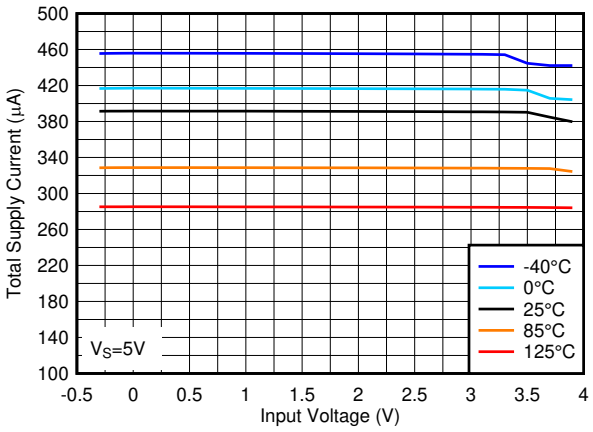


図 2-4. Total Supply Current vs. Input Voltage at 5V

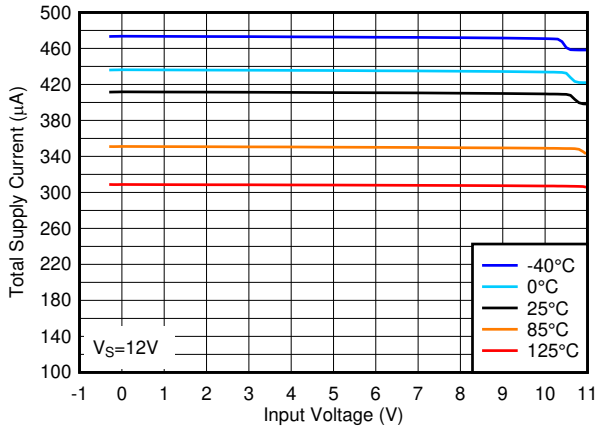


図 2-5. Total Supply Current vs. Input Voltage at 12V

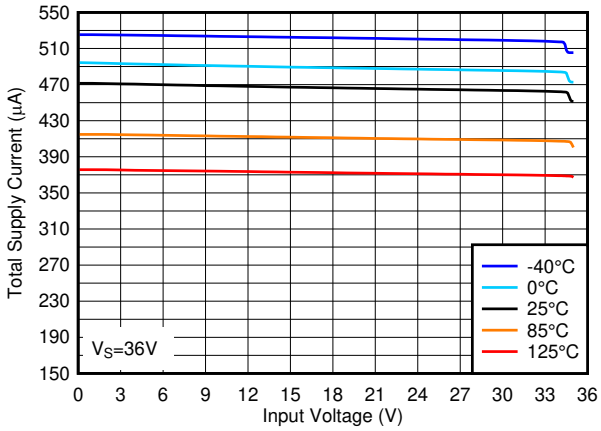


図 2-6. Total Supply Current vs. Input Voltage at 36V

2.14 Typical Characteristics (continued)

T_A = 25°C, V_S = 5V, R_{PULLUP} = 5.1k, C_L = 15pF, V_{CM} = 0V, $V_{UNDERDRIVE}$ = 100mV, $V_{OVERDRIVE}$ = 100mV unless otherwise noted.

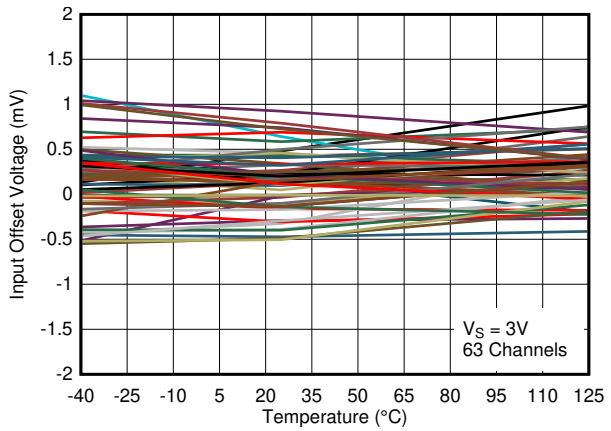


図 2-7. Input Offset Voltage vs. Temperature at 3V

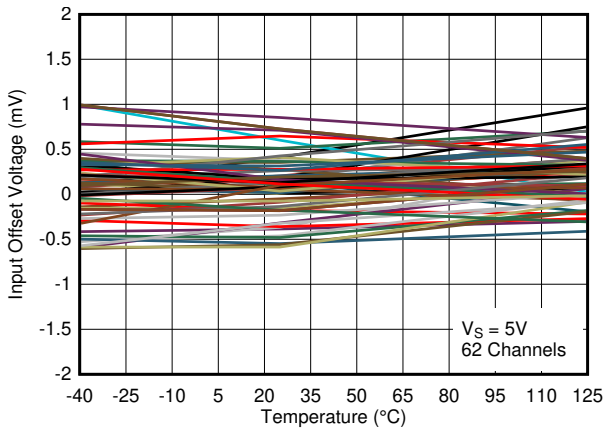


図 2-8. Input Offset Voltage vs. Temperature at 5V

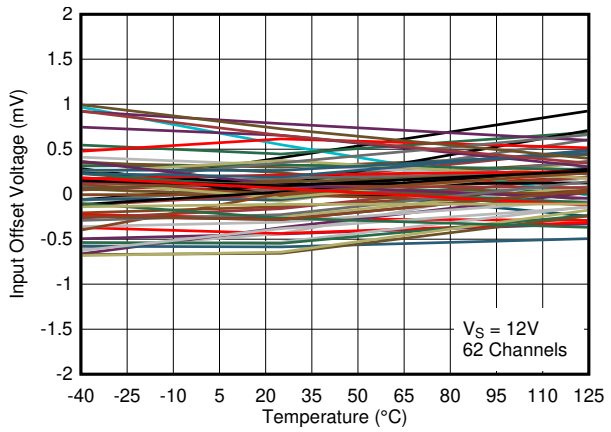


図 2-9. Input Offset Voltage vs. Temperature at 12V

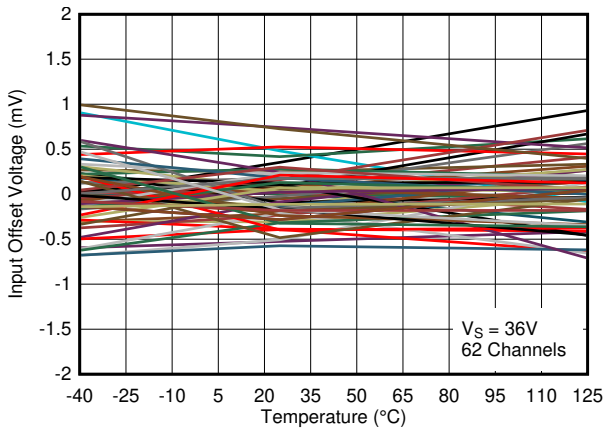


図 2-10. Input Offset Voltage vs. Temperature at 36

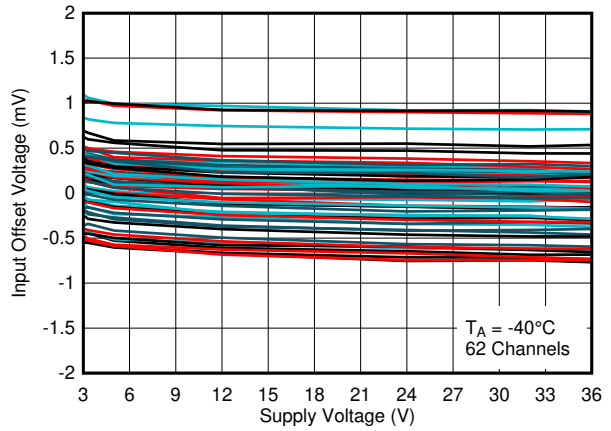


図 2-11. Input Offset Voltage vs. Supply Voltage at -40°C

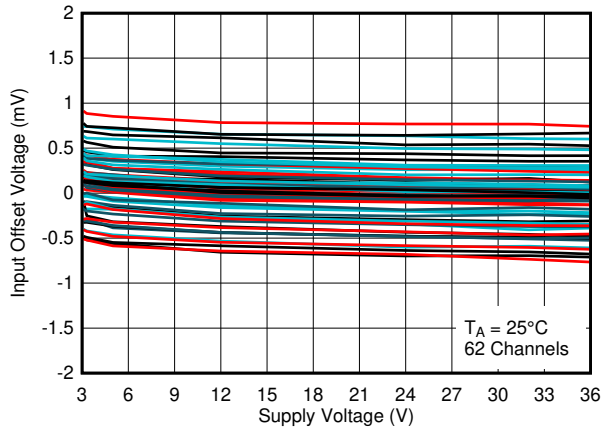


図 2-12. Input Offset Voltage vs. Supply Voltage at 25°C

2.14 Typical Characteristics (continued)

T_A = 25°C, V_S = 5V, R_{PULLUP} = 5.1k, C_L = 15pF, V_{CM} = 0V, $V_{UNDERDRIVE}$ = 100mV, $V_{OVERDRIVE}$ = 100mV unless otherwise noted.

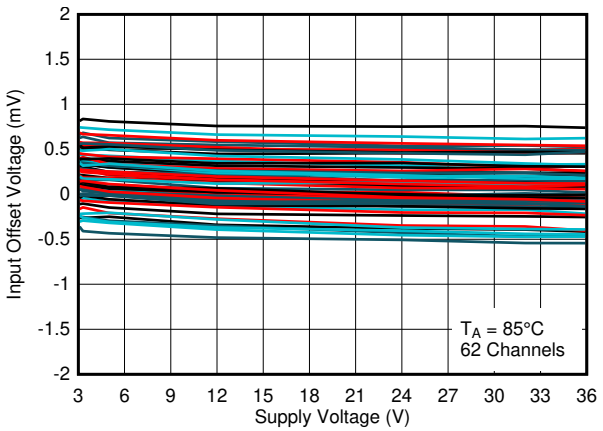


図 2-13. Input Offset Voltage vs. Supply Voltage at 85°C

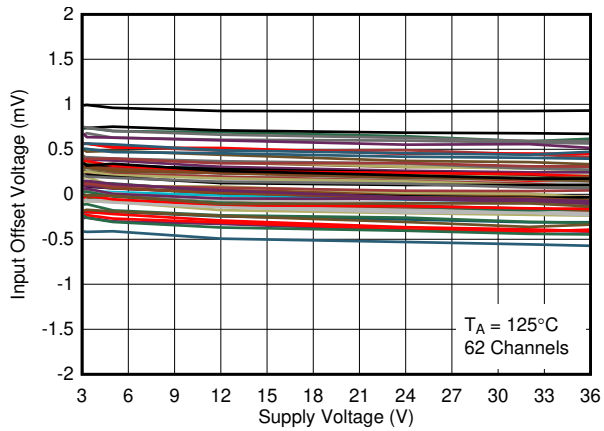


図 2-14. Input Offset Voltage vs. Supply Voltage at 125°C

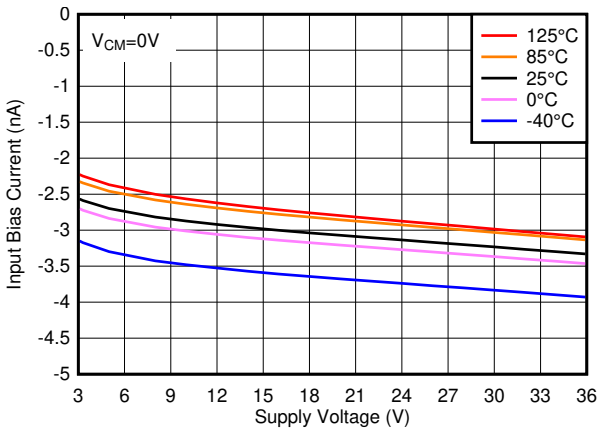


図 2-15. Input Bias Current vs. Supply Voltage

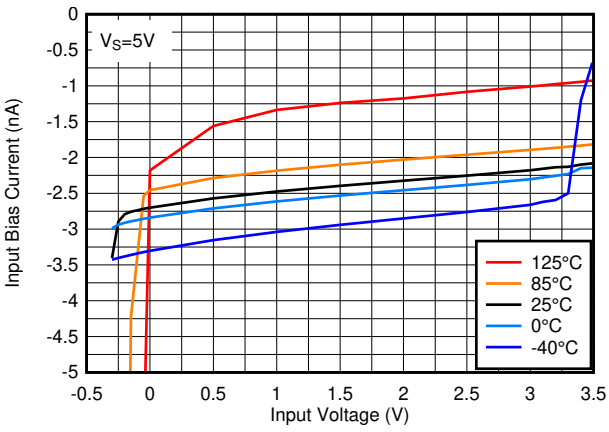


図 2-16. Input Bias Current vs. Input Voltage at 5V

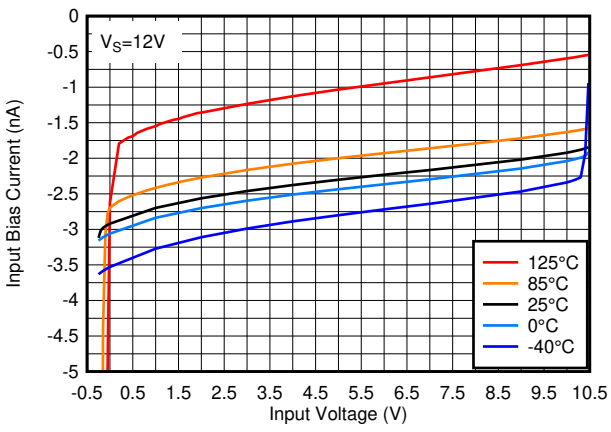


図 2-17. Input Bias Current vs. Input Voltage at 12V

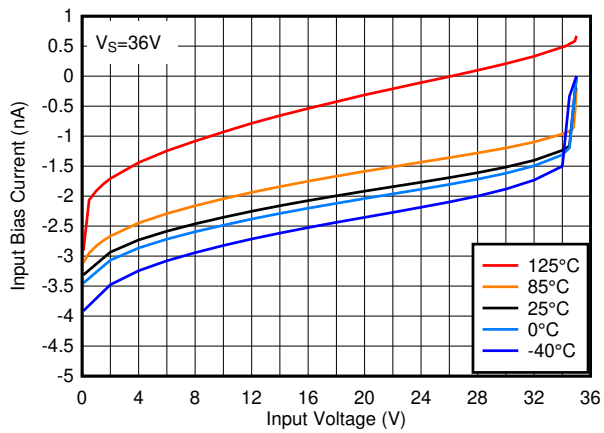


図 2-18. Input Bias Current vs. Input Voltage at 36V

2.14 Typical Characteristics (continued)

T_A = 25°C, V_S = 5V, R_{PULLUP} = 5.1k, C_L = 15pF, V_{CM} = 0V, $V_{UNDERDRIVE}$ = 100mV, $V_{OVERDRIVE}$ = 100mV unless otherwise noted.

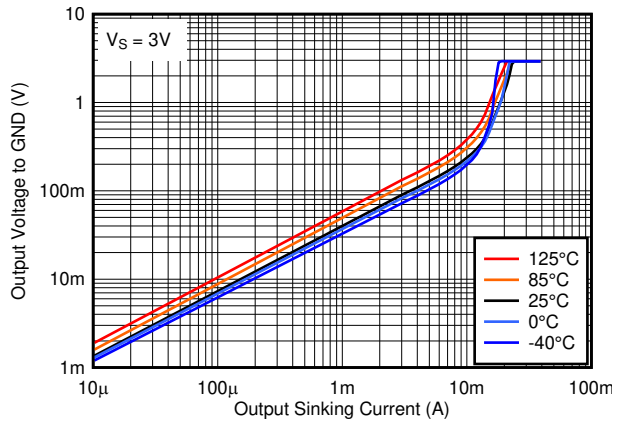


図 2-19. Output Low Voltage vs. Output Sinking Current at 3V

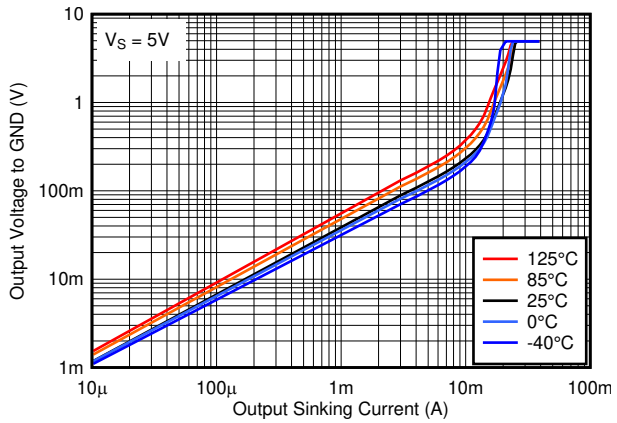


図 2-20. Output Low Voltage vs. Output Sinking Current at 5V

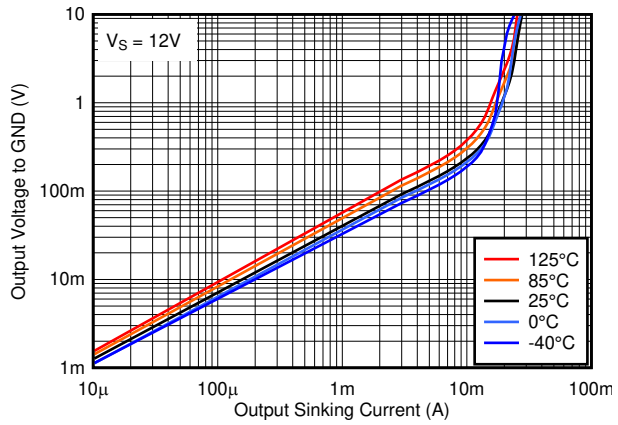


図 2-21. Output Low Voltage vs. Output Sinking Current at 12V

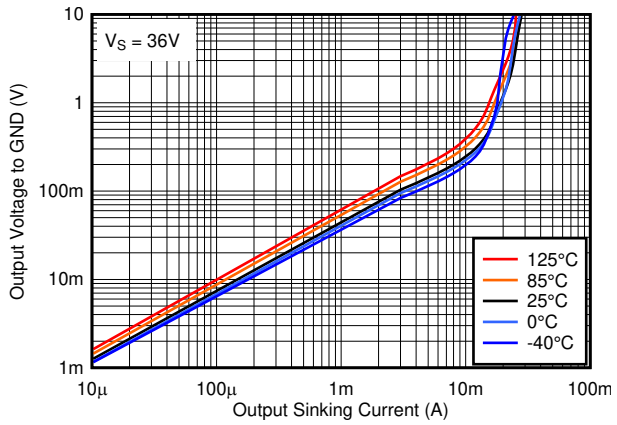


図 2-22. Output Low Voltage vs. Output Sinking Current at 36V

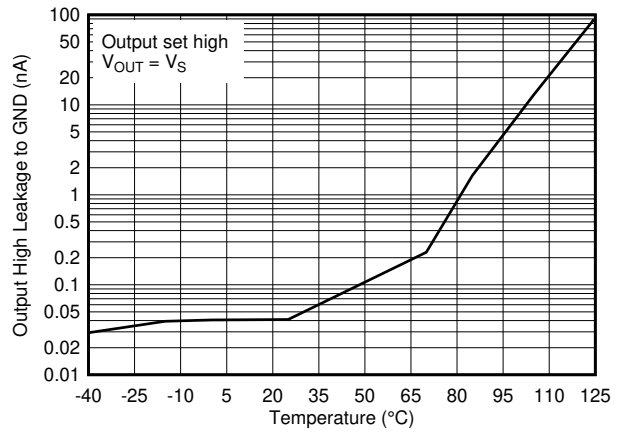


図 2-23. Output High Leakage Current vs.Temperature at 5V

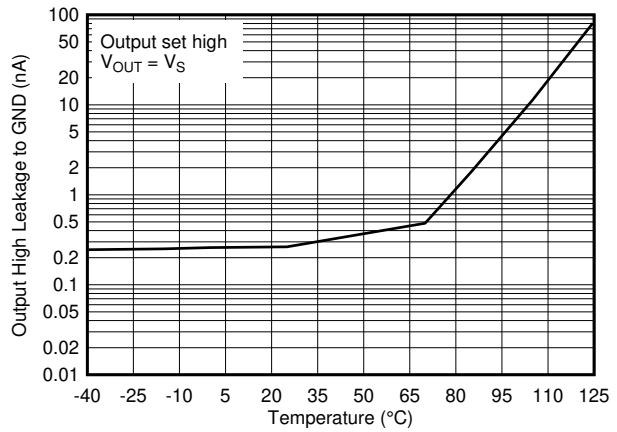


図 2-24. Output High Leakage Current vs. Temperature at 36V

2.14 Typical Characteristics (continued)

T_A = 25°C, V_S = 5V, R_{PULLUP} = 5.1k, C_L = 15pF, V_{CM} = 0V, $V_{UNDERDRIVE}$ = 100mV, $V_{OVERDRIVE}$ = 100mV unless otherwise noted.

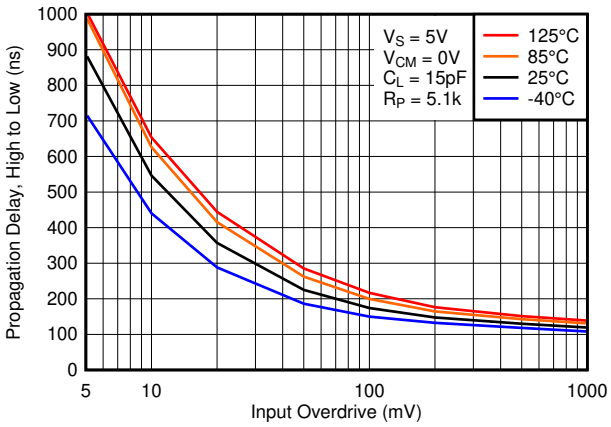


図 2-25. High to Low Propagation Delay vs. Input Overdrive Voltage, 5V

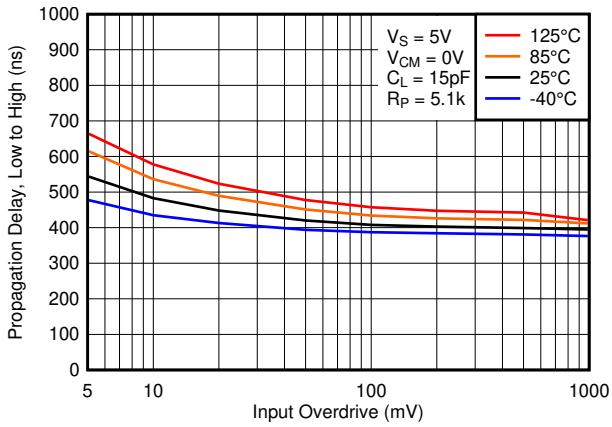


図 2-26. Low to High Propagation Delay vs. Input Overdrive Voltage, 5V

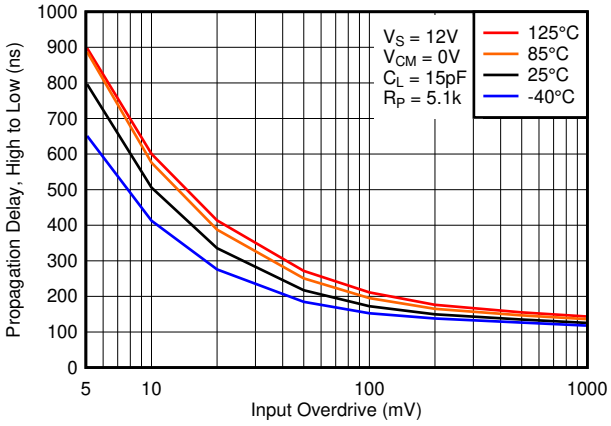


図 2-27. High to Low Propagation Delay vs. Input Overdrive Voltage, 12V

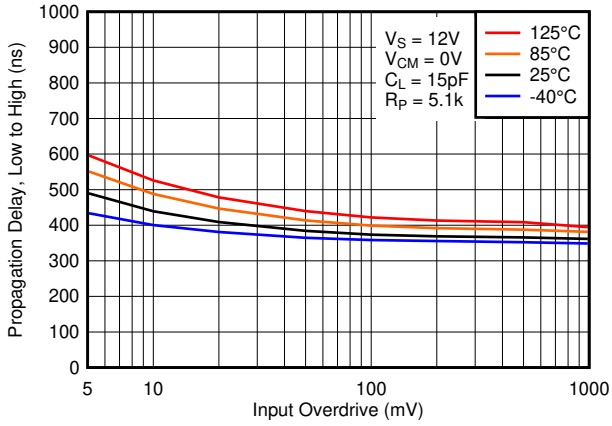


図 2-28. Low to High Propagation Delay vs. Input Overdrive Voltage, 12V

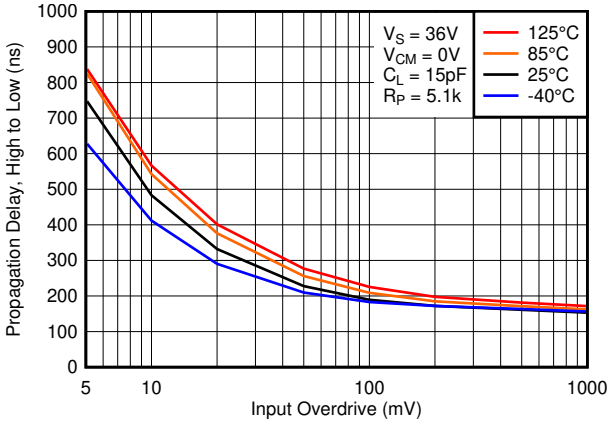


図 2-29. High to Low Propagation Delay vs. Input Overdrive Voltage, 36V

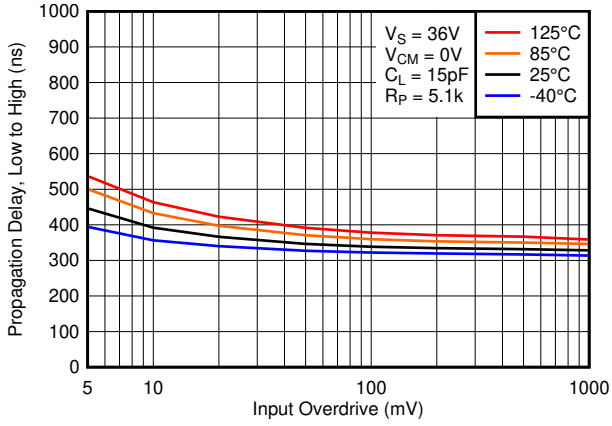


図 2-30. Low to High Propagation Delay vs. Input Overdrive Voltage, 36V

2.14 Typical Characteristics (continued)

T_A = 25°C, V_S = 5V, R_{PULLUP} = 5.1k, C_L = 15pF, V_{CM} = 0V, $V_{UNDERDRIVE}$ = 100mV, $V_{OVERDRIVE}$ = 100mV unless otherwise noted.

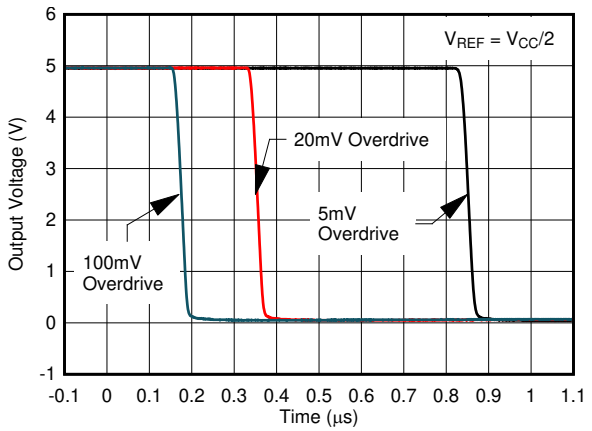


図 2-31. Response Time for Various Overdrives, High-to-Low Transition

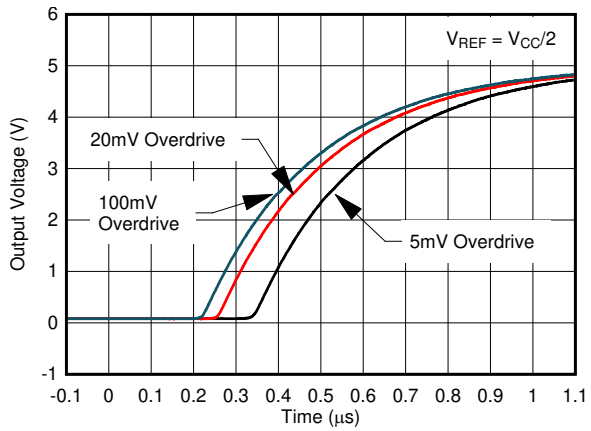


図 2-32. Response Time for Various Overdrives, Low-to-High Transition

3 Detailed Description

3.1 Overview

The LM2903-Q1 family is a dual comparator with the ability to operate up to 36V on the supply pin. This standard device has proven ubiquity and versatility across a wide range of applications. This is due to it's very wide supply voltages range (2V to 36V), low Iq and fast response.

This device is AEC-Q100 qualified and can operate over a wide temperature range of –40°C to 125°C (LM2903-Q1 and LM2903B-Q1) or –40°C to 150°C (LM2903E-Q1).

The open-drain output allows the user to configure the output's logic low voltage (V_{OL}) and can be utilized to enable the comparator to be used in AND functionality.

The "B" versions add dedicated ESD protections on all the pins for improved ESD performance as well as improved negative input voltage handling. Please see Application Note SNOAA35 for more information

3.2 Functional Block Diagram

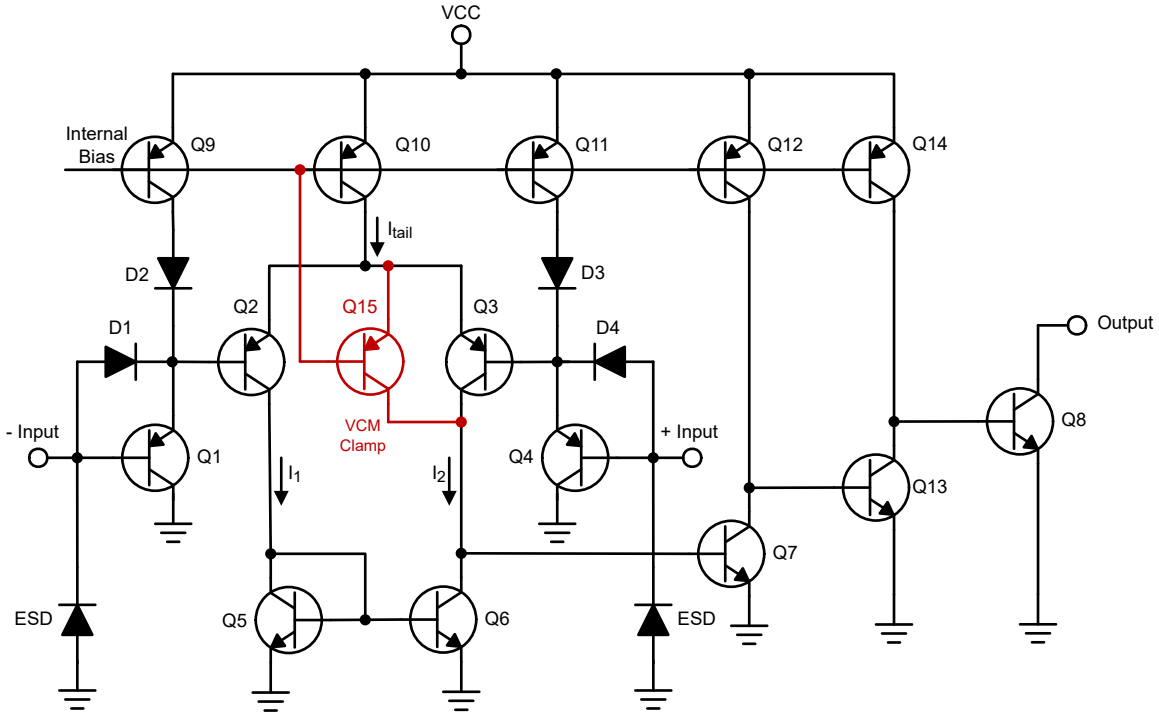


図 3-1. Schematic (Each Comparator)

3.3 Feature Description

LM2903-Q1 family consists of a PNP darlington pair input, allowing the device to operate with very high gain and fast response with minimal input bias current. The input Darlington pair creates a limit on the input common mode voltage capability, allowing LM2903-Q1 to accurately function from ground to V_{CC}–1.5V differential input. This is enables much head room for modern day supplies of 3.3V and 5.0V. A clamp (Q15) was added around Q3 to force the output low when both inputs are taken above the VCM range.

The output consists of an open drain NPN (pull-down or low side) transistor. The output NPN sinks current when the negative input voltage is higher than the positive input voltage and the offset voltage. The VOL is resistive and scales with the output current. Please see Output Low Voltage vs. Output Sinking Current at 5V in the *Typical Characteristics* section for V_{OL} values with respect to the output current.

3.4 Device Functional Modes

3.4.1 Voltage Comparison

The LM2903-Q1 family operates solely as a voltage comparator, comparing the differential voltage between the positive and negative pins and outputting a logic low or high impedance (logic high with pull-up) based on the input differential polarity.

4 Application and Implementation

注

以下のアプリケーション情報は、TI の製品仕様に含まれるものではなく、TI ではその正確性または完全性を保証いたしません。個々の目的に対する製品の適合性については、お客様の責任で判断していただくことになります。お客様は自身の設計実装を検証しテストすることで、システムの機能を確認する必要があります。

4.1 Application Information

LM2903-Q1 will typically be used to compare a single signal to a reference or two signals against each other. Many users take advantage of the open drain output to drive the comparison logic output to a logic voltage level to an MCU or logic device. The wide supply range and high voltage capability makes LM2903Q1 optimal for level shifting to a higher or lower voltage.

4.2 Typical Application

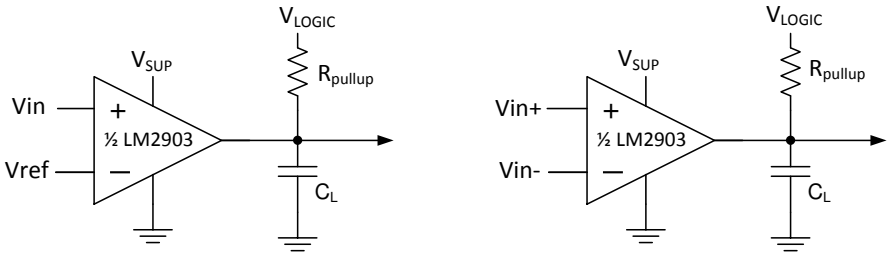


図 4-1. Single-ended and Differential Comparator Configurations

4.2.1 Design Requirements

For this design example, use the parameters listed in 表 4-1 as the input parameters.

表 4-1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input Voltage Range	0V to Vsup-1.5V
Supply Voltage	2V to 36V
Logic Supply Voltage	2V to 36V
Output Current (R_{PULLUP})	1µA to 20mA
Input Overdrive Voltage	100mV
Reference Voltage	2.5V
Load Capacitance (C_L)	15pF

4.2.2 Detailed Design Procedure

When using LM2903-Q1 family in a general comparator application, determine the following:

- Input Voltage Range
- Minimum Overdrive Voltage
- Output and Drive Current
- Response Time

4.2.2.1 Input Voltage Range

When choosing the input voltage range, the input common mode voltage range (V_{ICR}) must be taken in to account. If temperature operation is above or below 25°C the V_{ICR} can range from 0V to V_{CC}– 2V. This limits the input voltage range to as high as V_{CC}– 2.0V and as low as 0V. Operation outside of this range can yield incorrect comparisons.

Below is a list of input voltage situation and the outcomes:

1. When both IN- and IN+ are both within the common mode range:
   a. If IN- is higher than IN+ and the offset voltage, the output is low and the output transistor is sinking current
   b. If IN- is lower than IN+ and the offset voltage, the output is high impedance and the output transistor is not conducting
2. When IN- is higher than common mode and IN+ is within common mode, the output is low and the output transistor is sinking current
3. When IN+ is higher than common mode and IN- is within common mode, the output is high impedance and the output transistor is not conducting
4. When IN- and IN+ are both higher than common mode, see Section 2 of Application Design Guidelines for LM339, LM393, TL331 Family Comparators Including the New B-versions

4.2.2.2 Minimum Overdrive Voltage

Overdrive Voltage is the differential voltage produced between the positive and negative inputs of the comparator over the offset voltage (V_{IO}). To make an accurate comparison the Overdrive Voltage (V_{OD}) must be higher than the input offset voltage (V_{IO}). Overdrive voltage can also determine the response time of the comparator, with the response time decreasing with increasing overdrive. 図 4-2 and 図 4-3 show positive and negative response times with respect to overdrive voltage.

4.2.2.3 Output and Drive Current

Output current is determined by the load/pull-up resistance and logic/pull-up voltage. The output current produces a output low voltage (V_{OL}) from the comparator. In which V_{OL} is proportional to the output current. Use 図 2-21 to determine V_{OL} based on the output current.

The output current can also effect the transient response. More explanation is in the next section.

4.2.2.4 Response Time

The transient response can be determined by the load capacitance (C_L), load/pull-up resistance (R_{PULLUP}) and equivalent collector-emitter resistance (R_{CE}).

- The positive response time (τ_p) is approximately $\tau_P = R_{PULLUP} \times C_L$
- The negative response time (τ_N) is approximately $\tau_N = R_{CE} \times C_L$
  – R_{CE} can be determine by taking the slope of 図 2-21 in it's linear region at the desired temperature, or by dividing the V_{OL} by I_{out}

4.2.3 Application Curves

The following curves were generated with 5V on V_{CC} and V_{Logic}, R_{PULLUP} = 5.1kΩ, and 50pF scope probe.

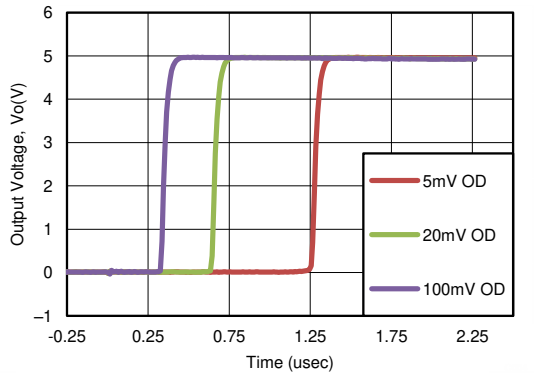


図 4-2. Response Time for Various Overdrives (Positive Transition)

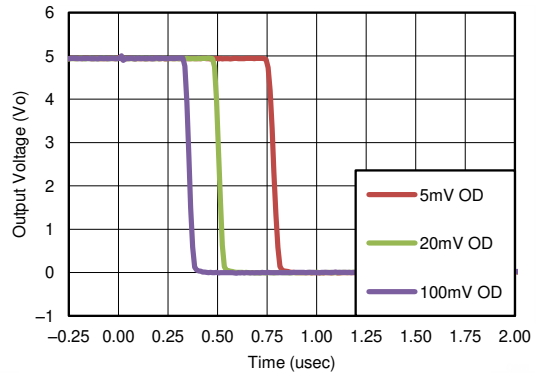


図 4-3. Response Time for Various Overdrives (Negative Transition)

4.3 Power Supply Recommendations

A bypass capacitor is recommended on the supply pin to reject any variation on the supply voltage. This variation can eat into the comparator's input common mode range and create an inaccurate comparison.

4.4 Layout

4.4.1 Layout Guidelines

For accurate comparator applications without hysteresis, a stable power supply with minimimal noise must be maintained. To achieve this, the best practice is to add a bypass capacitor between the supply voltage and ground. This can be implemented on the positive power supply and negative supply (if available). If a negative supply is not being used, do not put a capacitor between the IC's GND pin and system ground.

4.4.2 Layout Example

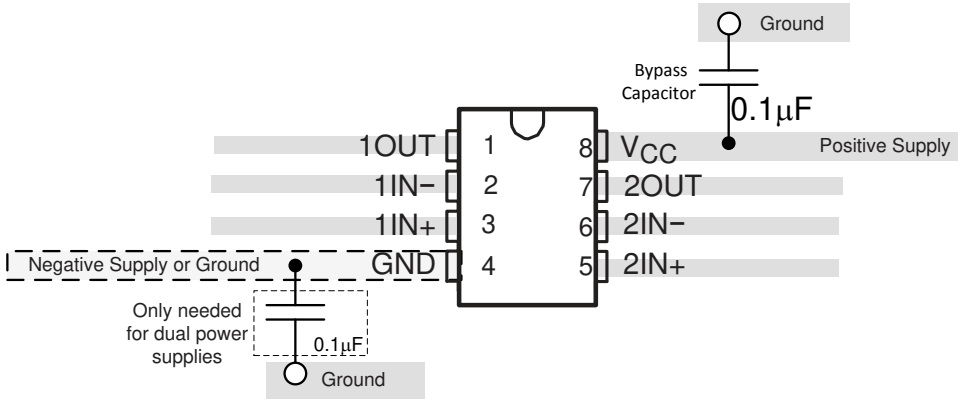


図 4-4. LM2903Q1 Layout Example

5 Device and Documentation Support

5.1 Documentation Support

5.1.1 Related Documentation

LM2903B-Q1 Functional Safety FIT Rate, FMD and Pin FMA - SLCA005

Application Design Guidelines for LM339, LM393, TL331 Family Comparators - SNOAA35

Analog Engineers Circuit Cookbook: Amplifiers (See Comparators section) - SLYY137

5.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

5.3 サポート・リソース

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5.4 Trademarks

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5.5 静電気放電に関する注意事項

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ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

5.6 用語集

テキサス・インスツルメンツ用語集　　この用語集には、用語や略語の一覧および定義が記載されています。

6 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision L (August 2023) to Revision M (December 2024) **Page**

- Updated thermal table 5
- Updated Typical Characteristics..... 8
- Updated Functional Block Diagram..... 14

Changes from Revision K (August 2022) to Revision L (August 2023) **Page**

- Added reference to Application Note..... 16

Changes from Revision J (November 2020) to Revision K (August 2022) **Page**

- Added T, R and H Temp Test Options table..... 6

Changes from Revision I (June 2020) to Revision J (November 2020) **Page**

- データシート全体を通して、LM2903B-Q1 の最小推奨電源電圧を 2V に変更..... 1
- Added Operating Virtual Temp to Abs Max Table for both versions..... 4
- Updated Supply Voltage vs Supply Current graph for 2V..... 4

Changes from Revision G (November 2018) to Revision H (January 2020) **Page**

- データシートに LM2903B-Q1 を追加..... 1
- 「製品情報」表を追加。..... 1
- Added "B" device graphs 8
- Changed incorrect input text in Feature Description in Apps Section..... 14

Changes from Revision F (May 2018) to Revision G (November 2018) **Page**

Changes from Revision H (January 2020) to Revision I (June 2020) **Page**

- 機能安全のテキストとリンクを追加..... 1
- 「B」の「製品情報」の一覧に VSSOP パッケージを追加..... 1
- Added DGK to "B" Thermal Table..... 5
- Added text to Apps Overview section for ESD..... 14

7 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LM2903AVQDRG4Q1	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2903AVQ
LM2903AVQDRG4Q1.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2903AVQ
LM2903AVQDRG4Q1.B	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2903AVQ
LM2903AVQDRQ1	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(2903AVQ, 903AVQ)
LM2903AVQDRQ1.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(2903AVQ, 903AVQ)
LM2903AVQDRQ1.B	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(2903AVQ, 903AVQ)
LM2903AVQPWRG4Q1	Active	Production	TSSOP (PW) | 8	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2903AVQ
LM2903AVQPWRG4Q1.A	Active	Production	TSSOP (PW) | 8	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2903AVQ
LM2903AVQPWRQ1	Active	Production	TSSOP (PW) | 8	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2903AVQ
LM2903AVQPWRQ1.A	Active	Production	TSSOP (PW) | 8	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2903AVQ
LM2903BHQDGKRQ1	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	3BHQ
LM2903BHQDGKRQ1.A	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	3BHQ
LM2903BHQDGKRQ1.B	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	3BHQ
LM2903BHQDRQ1	Active	Production	SOIC (D) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	903BHQ
LM2903BHQDRQ1.A	Active	Production	SOIC (D) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	903BHQ
LM2903BHQDRQ1.B	Active	Production	SOIC (D) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	903BHQ
LM2903BHQPWRQ1	Active	Production	TSSOP (PW) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2903BH
LM2903BHQPWRQ1.A	Active	Production	TSSOP (PW) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2903BH
LM2903BHQPWRQ1.B	Active	Production	TSSOP (PW) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2903BH
LM2903BQDDFRQ1	Active	Production	SOT-23-THIN (DDF) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	903BQ
LM2903BQDDFRQ1.B	Active	Production	SOT-23-THIN (DDF) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	903BQ
LM2903BQDGKRQ1	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	Call TI | Nipdau	Level-1-260C-UNLIM	-40 to 125	03BQ
LM2903BQDGKRQ1.A	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	03BQ
LM2903BQDGKRQ1.B	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	03BQ
LM2903BQDRQ1	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2903BQ
LM2903BQDRQ1.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2903BQ
LM2903BQDRQ1.B	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2903BQ
LM2903BQPWRQ1	Active	Production	TSSOP (PW) | 8	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2903BQ
LM2903BQPWRQ1.A	Active	Production	TSSOP (PW) | 8	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2903BQ

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LM2903BQPWRQ1.B	Active	Production	TSSOP (PW) | 8	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2903BQ
LM2903BRQDGKRQ1	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	3BRQ
LM2903BRQDGKRQ1.A	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	3BRQ
LM2903BRQDGKRQ1.B	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	3BRQ
LM2903BRQDRQ1	Active	Production	SOIC (D) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	903BRQ
LM2903BRQDRQ1.A	Active	Production	SOIC (D) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	903BRQ
LM2903BRQDRQ1.B	Active	Production	SOIC (D) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	903BRQ
LM2903BRQPWRQ1	Active	Production	TSSOP (PW) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2903BR
LM2903BRQPWRQ1.A	Active	Production	TSSOP (PW) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2903BR
LM2903BRQPWRQ1.B	Active	Production	TSSOP (PW) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2903BR
LM2903BTQDGKRQ1	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	3BTQ
LM2903BTQDGKRQ1.A	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	3BTQ
LM2903BTQDGKRQ1.B	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	3BTQ
LM2903BTQDRQ1	Active	Production	SOIC (D) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	903BTQ
LM2903BTQDRQ1.A	Active	Production	SOIC (D) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	903BTQ
LM2903BTQDRQ1.B	Active	Production	SOIC (D) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	903BTQ
LM2903BTQPWRQ1	Active	Production	TSSOP (PW) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2903BT
LM2903BTQPWRQ1.A	Active	Production	TSSOP (PW) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2903BT
LM2903BTQPWRQ1.B	Active	Production	TSSOP (PW) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2903BT
LM2903BWDSGRQ1	Active	Production	WSON (DSG) | 8	3000 | LARGE T&R	Yes	Call TI | Sn	Level-2-260C-1 YEAR	-40 to 125	3BWQ
LM2903BWDSGRQ1.A	Active	Production	WSON (DSG) | 8	3000 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	3BWQ
LM2903BWDSGRQ1.B	Active	Production	WSON (DSG) | 8	3000 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	3BWQ
LM2903EPWRQ1	Active	Production	TSSOP (PW) | 8	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 150	2903Q0
LM2903EPWRQ1.A	Active	Production	TSSOP (PW) | 8	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 150	2903Q0
LM2903QDGKRQ1	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	KACQ
LM2903QDGKRQ1.A	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	KACQ
LM2903QDRG4Q1	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2903Q1
LM2903QDRG4Q1.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2903Q1
LM2903QDRQ1	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2903Q1
LM2903QDRQ1.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2903Q1
LM2903QDRQ1.B	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2903Q1

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LM2903QPWRG4Q1	Active	Production	TSSOP (PW) | 8	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2903Q1
LM2903QPWRG4Q1.A	Active	Production	TSSOP (PW) | 8	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2903Q1
LM2903QPWRQ1	Active	Production	TSSOP (PW) | 8	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2903Q1
LM2903QPWRQ1.A	Active	Production	TSSOP (PW) | 8	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2903Q1
LM2903VQDRG4Q1	Obsolete	Production	SOIC (D) | 8	-	-	Call TI	Call TI	-40 to 125	2903VQ1
LM2903VQDRQ1	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2903VQ1
LM2903VQDRQ1.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2903VQ1
LM2903VQDRQ1.B	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2903VQ1
LM2903VQPWRG4Q1	Active	Production	TSSOP (PW) | 8	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2903VQ
LM2903VQPWRG4Q1.A	Active	Production	TSSOP (PW) | 8	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2903VQ
LM2903VQPWRG4Q1.B	Active	Production	TSSOP (PW) | 8	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2903VQ
LM2903VQPWRQ1	Active	Production	TSSOP (PW) | 8	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2903VQ
LM2903VQPWRQ1.A	Active	Production	TSSOP (PW) | 8	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2903VQ
LM2903VQPWRQ1.B	Active	Production	TSSOP (PW) | 8	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2903VQ

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

OTHER QUALIFIED VERSIONS OF LM2903-Q1, LM2903B-Q1 :

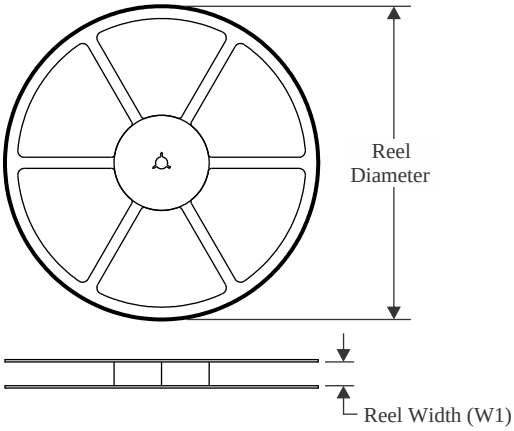
- Catalog : LM2903, LM2903B

NOTE: Qualified Version Definitions:

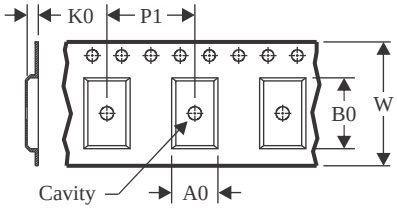
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

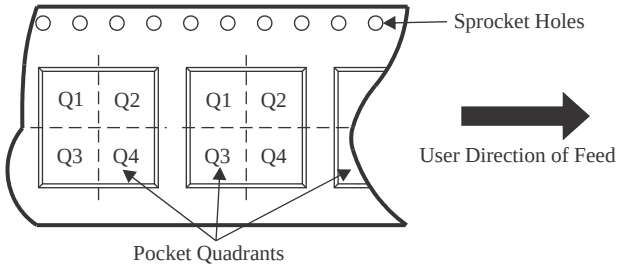


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

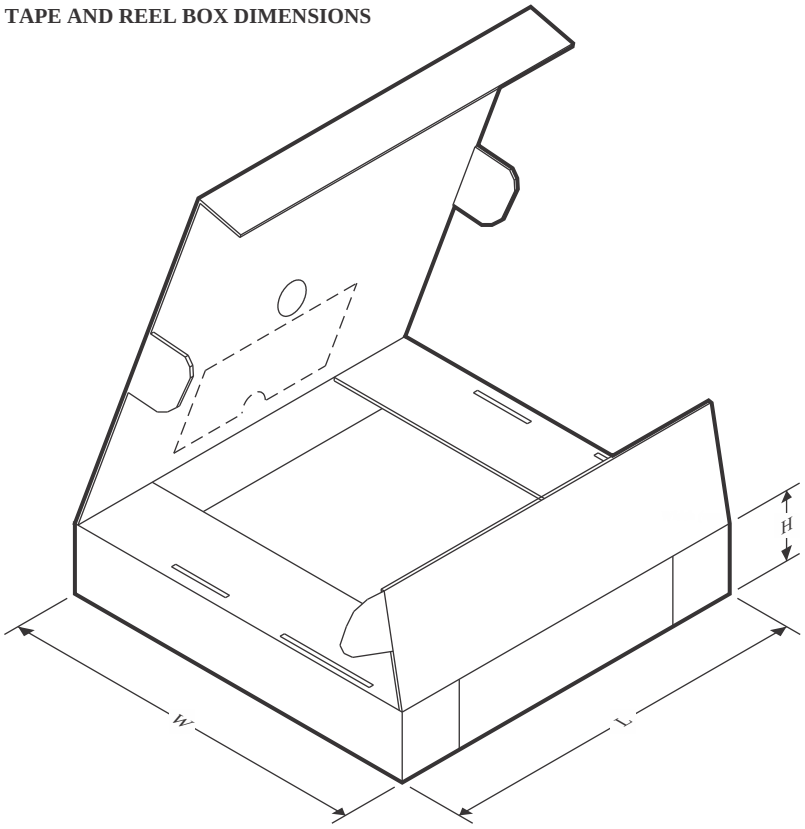


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM2903AVQDRG4Q1	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM2903AVQDRG4Q1	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM2903AVQDRQ1	SOIC	D	8	2500	330.0	12.5	6.4	5.2	2.1	8.0	12.0	Q1
LM2903AVQDRQ1	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM2903AVQPWRG4Q1	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
LM2903AVQPWRQ1	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
LM2903BHQDGKRQ1	VSSOP	DGK	8	2500	330.0	12.4	5.25	3.35	1.25	8.0	12.0	Q1
LM2903BHQDRQ1	SOIC	D	8	3000	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM2903BHQPWRQ1	TSSOP	PW	8	3000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
LM2903BQDDFRQ1	SOT-23-THIN	DDF	8	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LM2903BQDGKRQ1	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM2903BQDRQ1	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM2903BQPWRQ1	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
LM2903BRQDGKRQ1	VSSOP	DGK	8	2500	330.0	12.4	5.25	3.35	1.25	8.0	12.0	Q1
LM2903BRQDRQ1	SOIC	D	8	3000	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM2903BRQPWRQ1	TSSOP	PW	8	3000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
LM2903BTQDGKRQ1	VSSOP	DGK	8	2500	330.0	12.4	5.25	3.35	1.25	8.0	12.0	Q1
LM2903BTQDRQ1	SOIC	D	8	3000	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM2903BTQPWRQ1	TSSOP	PW	8	3000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
LM2903BWDSGRQ1	WSON	DSG	8	3000	180.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
LM2903EPWRQ1	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
LM2903QDGKRQ1	VSSOP	DGK	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM2903QDRG4Q1	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM2903QDRQ1	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM2903QPWRG4Q1	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
LM2903QPWRQ1	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
LM2903VQDRQ1	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM2903VQPWRG4Q1	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
LM2903VQPWRQ1	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS

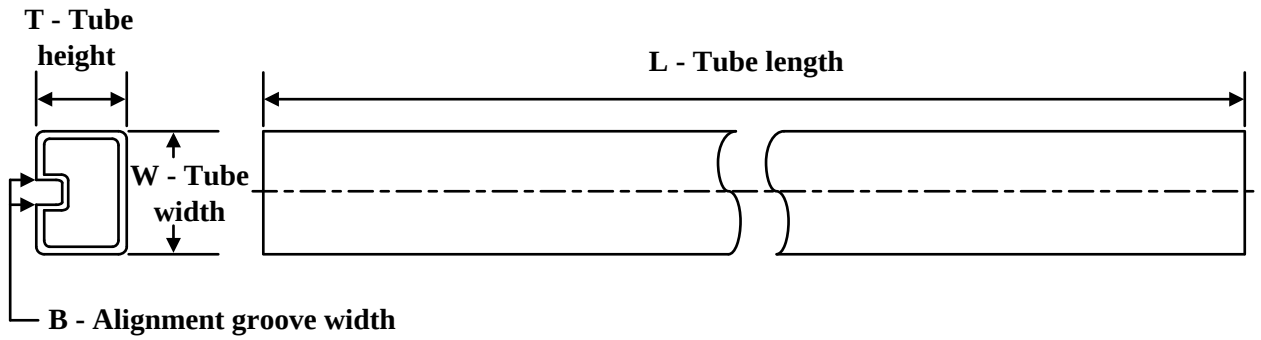


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM2903AVQDRG4Q1	SOIC	D	8	2500	340.5	338.1	20.6
LM2903AVQDRG4Q1	SOIC	D	8	2500	353.0	353.0	32.0
LM2903AVQDRQ1	SOIC	D	8	2500	353.0	353.0	32.0
LM2903AVQDRQ1	SOIC	D	8	2500	340.5	338.1	20.6
LM2903AVQPWRG4Q1	TSSOP	PW	8	2000	353.0	353.0	32.0
LM2903AVQPWRQ1	TSSOP	PW	8	2000	353.0	353.0	32.0
LM2903BHQDGKRQ1	VSSOP	DGK	8	2500	366.0	364.0	50.0
LM2903BHQDRQ1	SOIC	D	8	3000	340.5	338.1	20.6
LM2903BHQPWRQ1	TSSOP	PW	8	3000	353.0	353.0	32.0
LM2903BQDDFRQ1	SOT-23-THIN	DDF	8	3000	210.0	185.0	35.0
LM2903BQDGKRQ1	VSSOP	DGK	8	2500	353.0	353.0	32.0
LM2903BQDRQ1	SOIC	D	8	2500	353.0	353.0	32.0
LM2903BQPWRQ1	TSSOP	PW	8	2000	353.0	353.0	32.0
LM2903BRQDGKRQ1	VSSOP	DGK	8	2500	366.0	364.0	50.0
LM2903BRQDRQ1	SOIC	D	8	3000	340.5	338.1	20.6
LM2903BRQPWRQ1	TSSOP	PW	8	3000	353.0	353.0	32.0
LM2903BTQDGKRQ1	VSSOP	DGK	8	2500	366.0	364.0	50.0
LM2903BTQDRQ1	SOIC	D	8	3000	340.5	338.1	20.6

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM2903BTQPWRQ1	TSSOP	PW	8	3000	353.0	353.0	32.0
LM2903BWDSGRQ1	WSON	DSG	8	3000	213.0	191.0	35.0
LM2903EPWRQ1	TSSOP	PW	8	2000	353.0	353.0	32.0
LM2903QDGKRQ1	VSSOP	DGK	8	2500	353.0	353.0	32.0
LM2903QDRG4Q1	SOIC	D	8	2500	353.0	353.0	32.0
LM2903QDRQ1	SOIC	D	8	2500	353.0	353.0	32.0
LM2903QPWRG4Q1	TSSOP	PW	8	2000	353.0	353.0	32.0
LM2903QPWRQ1	TSSOP	PW	8	2000	353.0	353.0	32.0
LM2903VQDRQ1	SOIC	D	8	2500	353.0	353.0	32.0
LM2903VQPWRG4Q1	TSSOP	PW	8	2000	353.0	353.0	32.0
LM2903VQPWRQ1	TSSOP	PW	8	2000	353.0	353.0	32.0

TUBE



*All dimensions are nominal

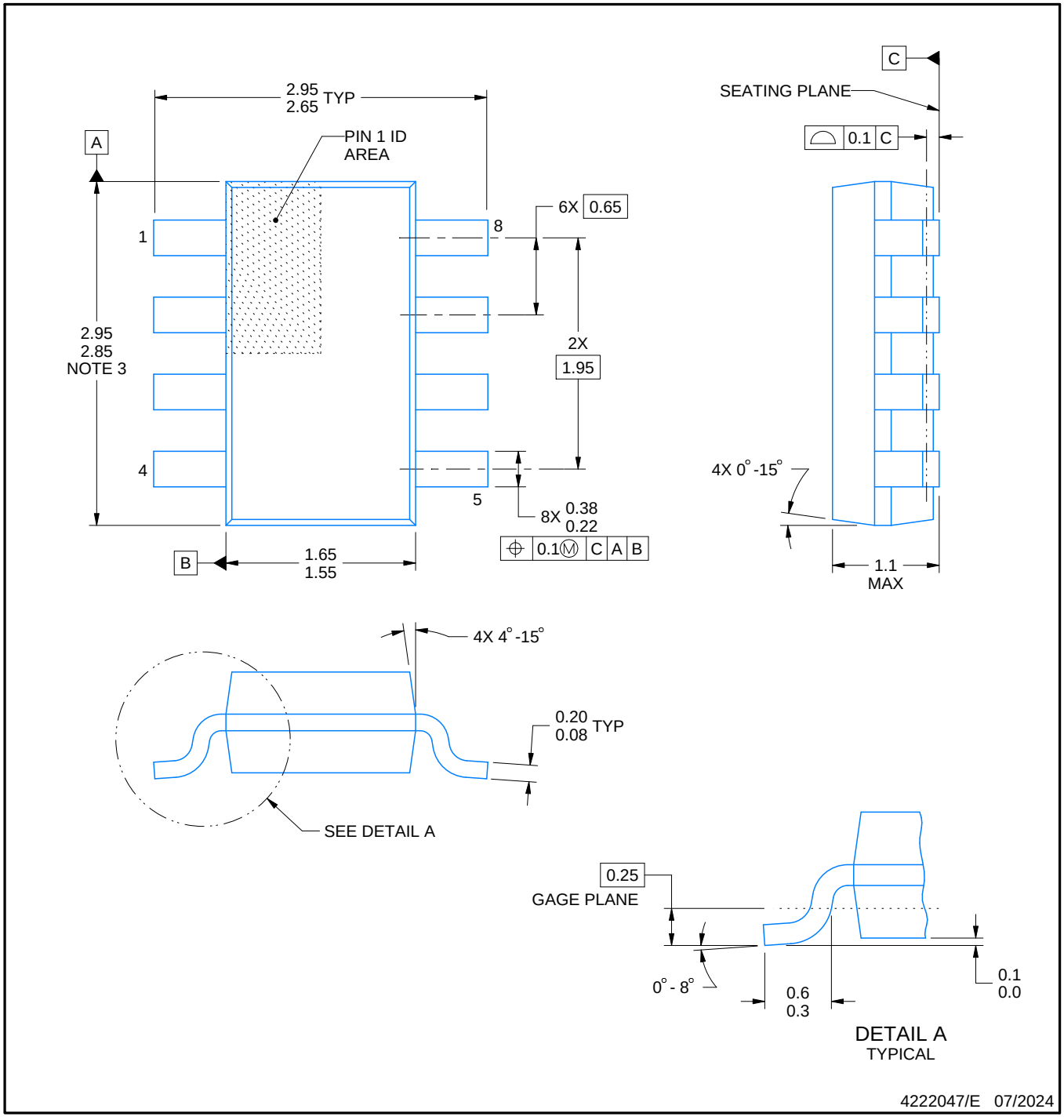
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
LM2903BQDGKRQ1	DGK	VSSOP	8	2500	328	7.98	550	NA
LM2903BQDGKRQ1.A	DGK	VSSOP	8	2500	328	7.98	550	NA
LM2903BQDGKRQ1.B	DGK	VSSOP	8	2500	328	7.98	550	NA

PACKAGE OUTLINE

DDF0008A

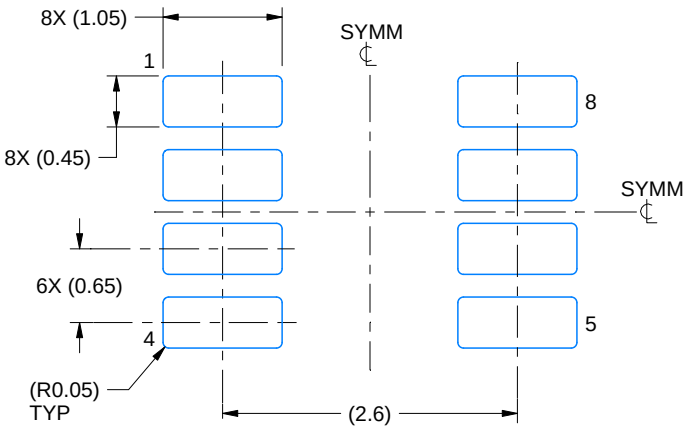
SOT-23-THIN - 1.1 mm max height

PLASTIC SMALL OUTLINE

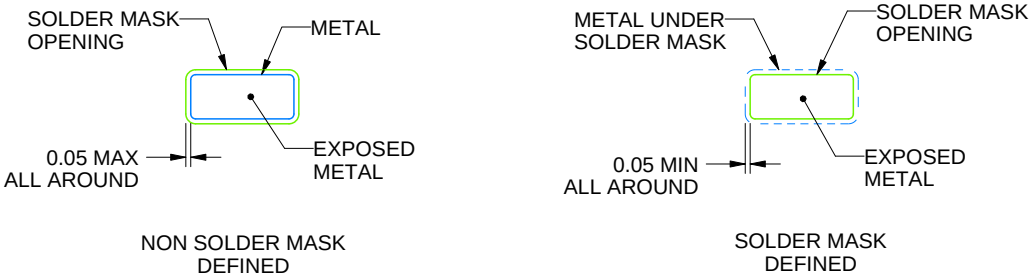


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

4222047/E 07/2024

NOTES: (continued)

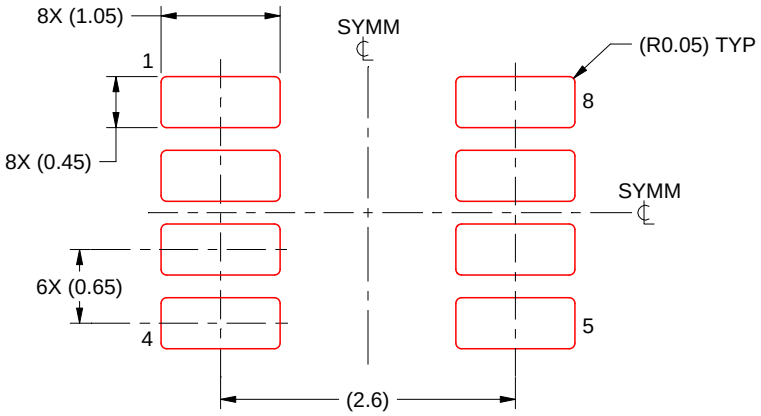
4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DDF0008A

SOT-23-THIN - 1.1 mm max height

PLASTIC SMALL OUTLINE

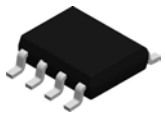


SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4222047/E 07/2024

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.

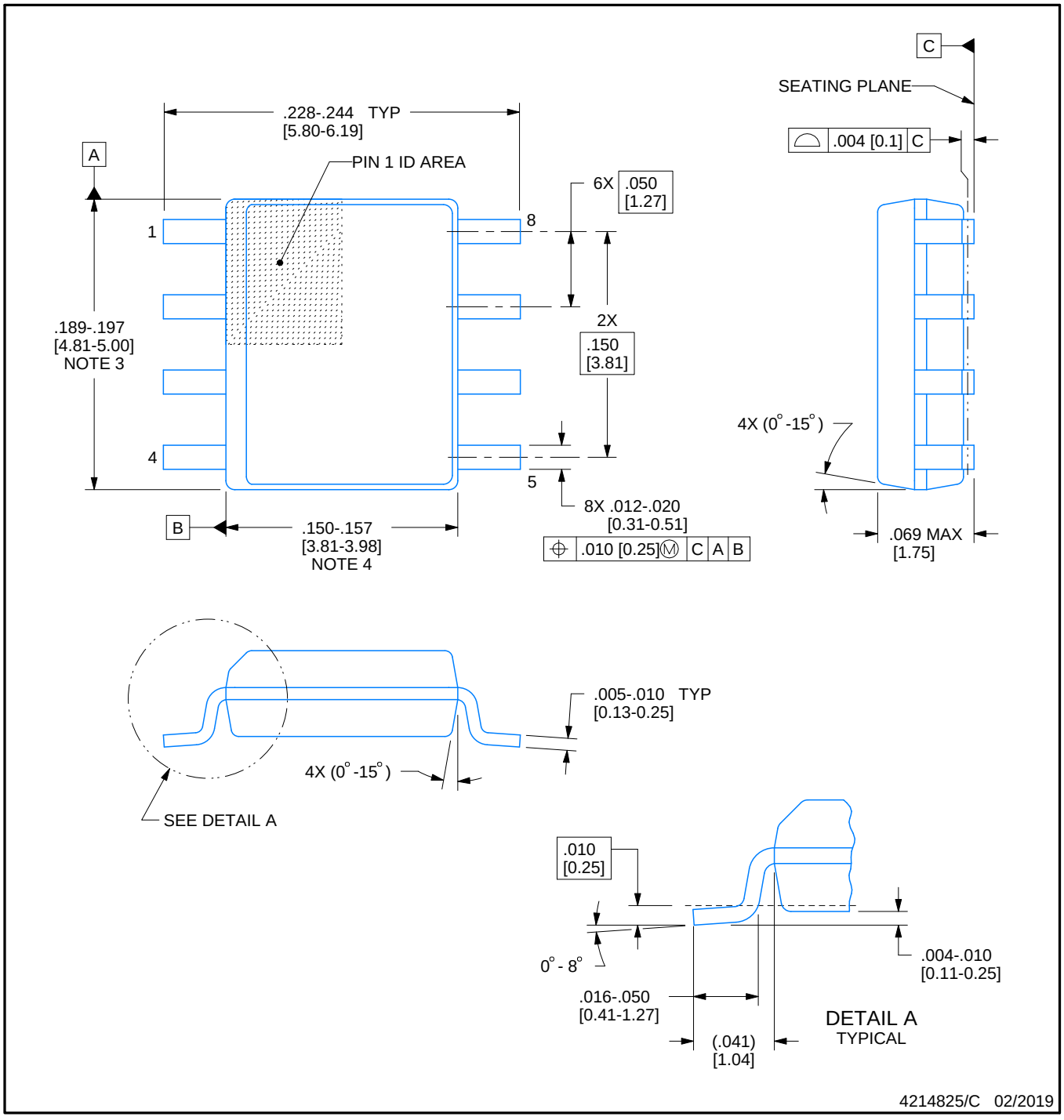


PACKAGE OUTLINE

D0008A

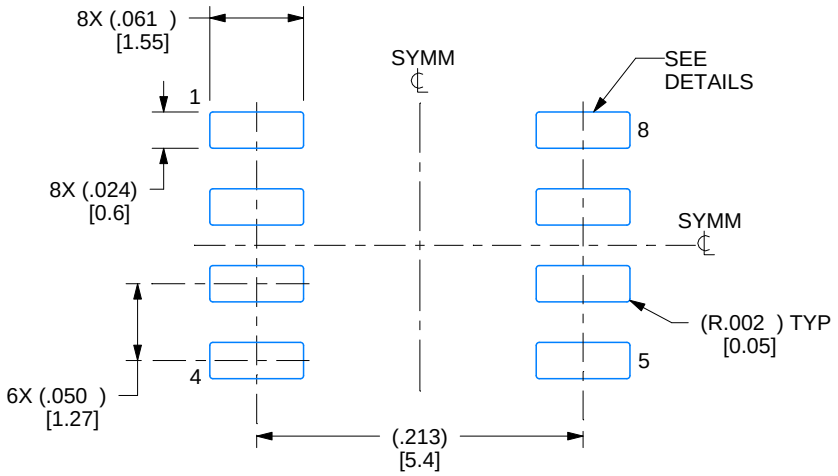
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

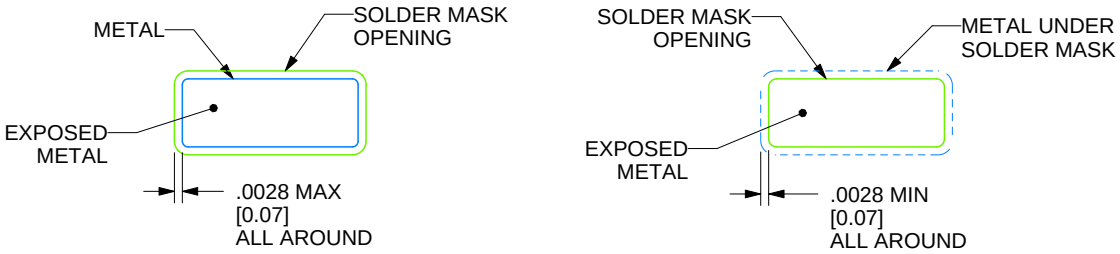


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

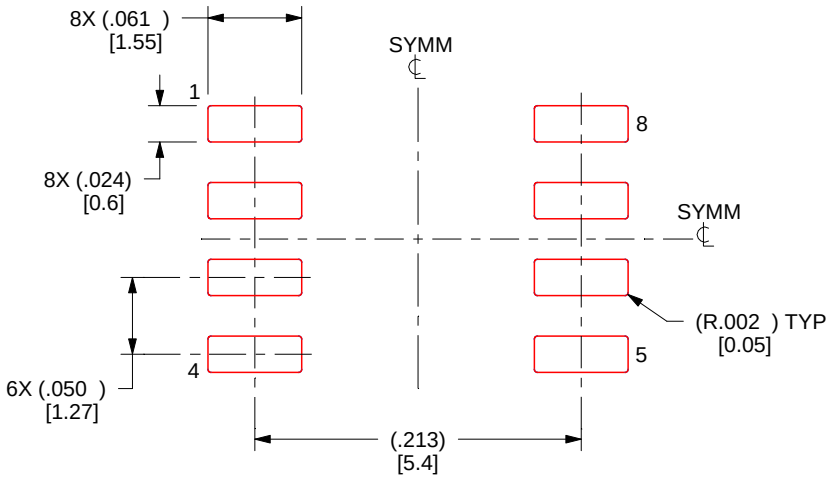
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

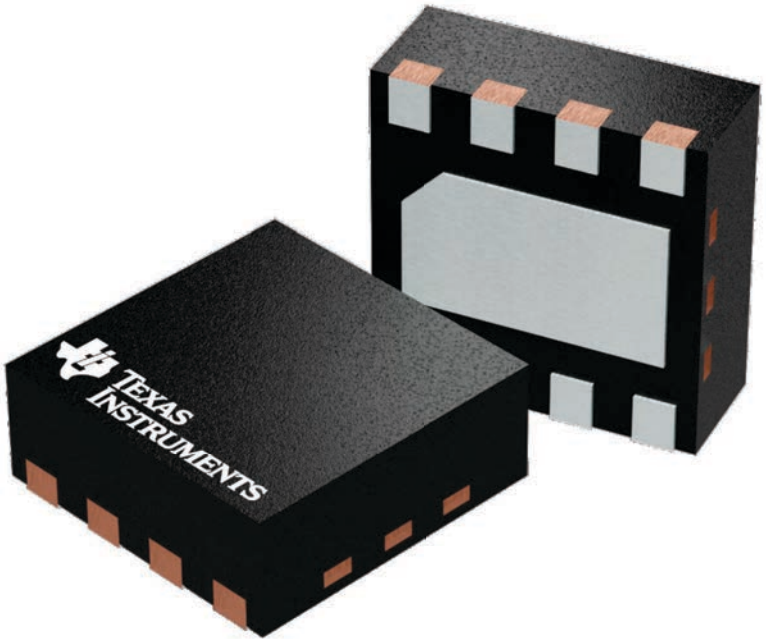
DSG 8

WSON - 0.8 mm max height

2 x 2, 0.5 mm pitch

PLASTIC SMALL OUTLINE - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



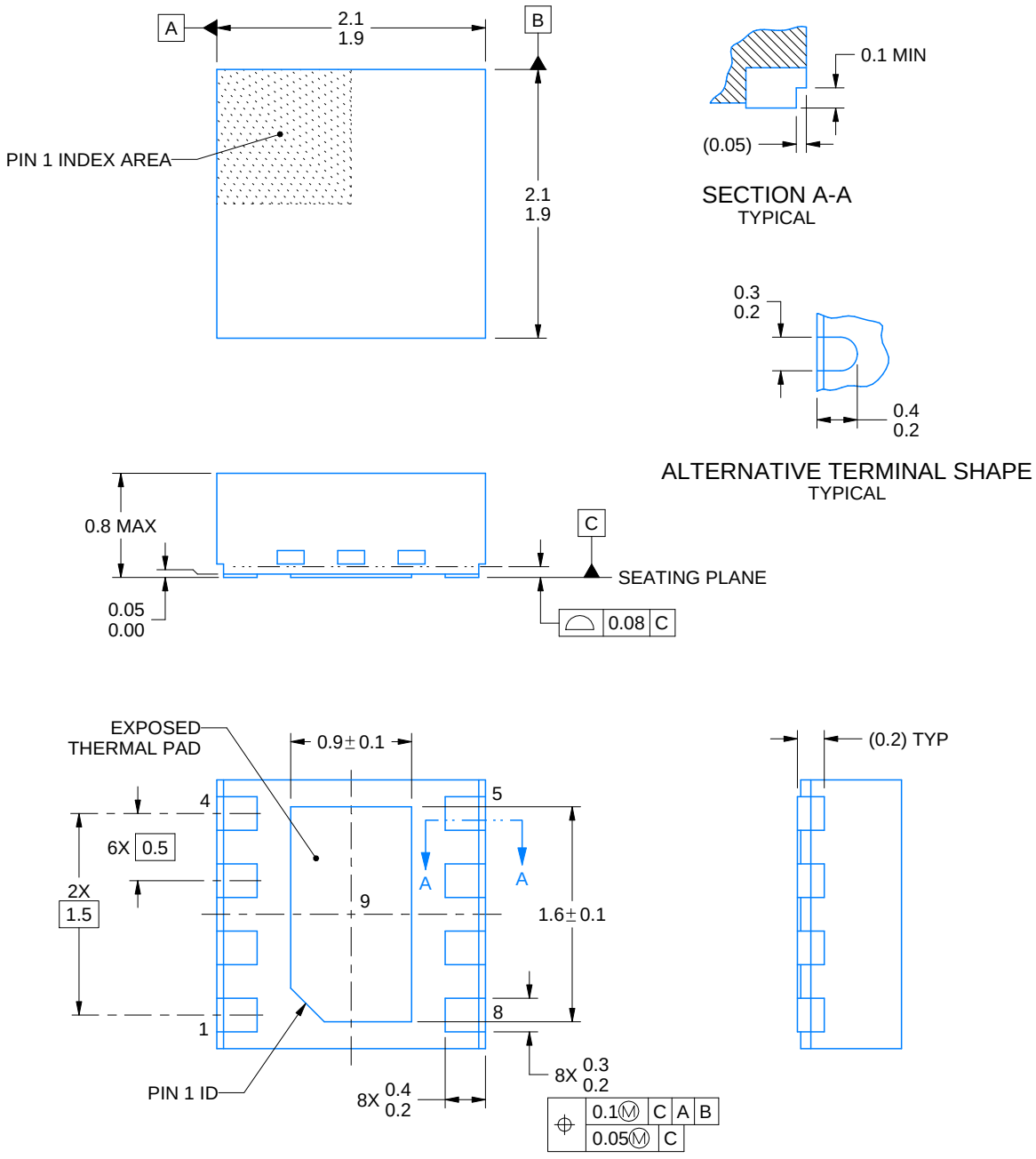
4224783/A

PACKAGE OUTLINE

DSG0008B

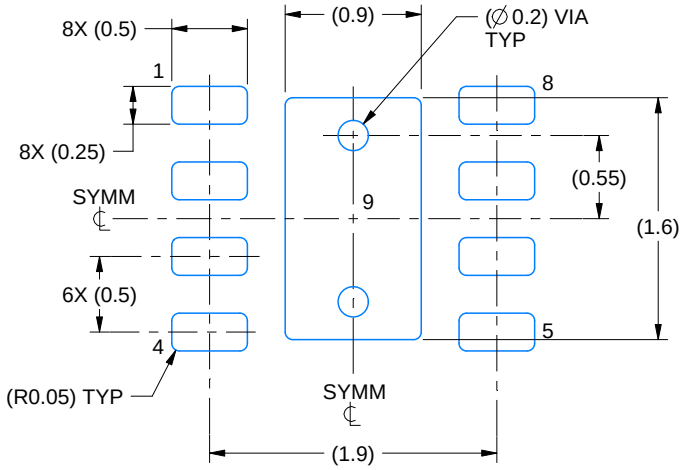
WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

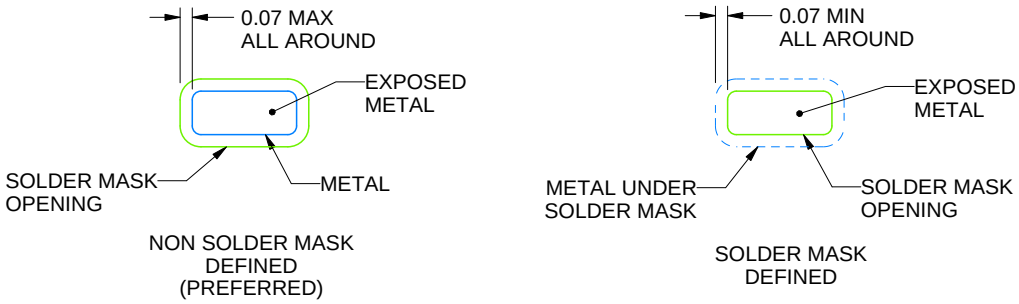


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X



SOLDER MASK DETAILS

4222124/E 05/2020

NOTES: (continued)

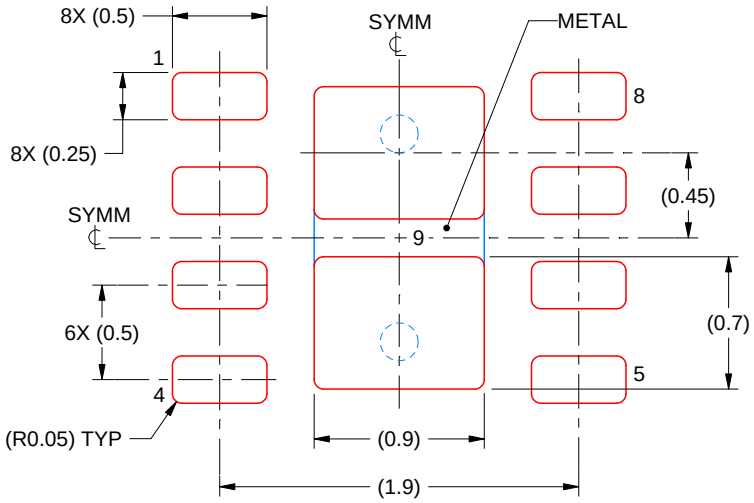
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

DSG0008B

WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 9:
87% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:25X

4222124/E 05/2020

NOTES: (continued)

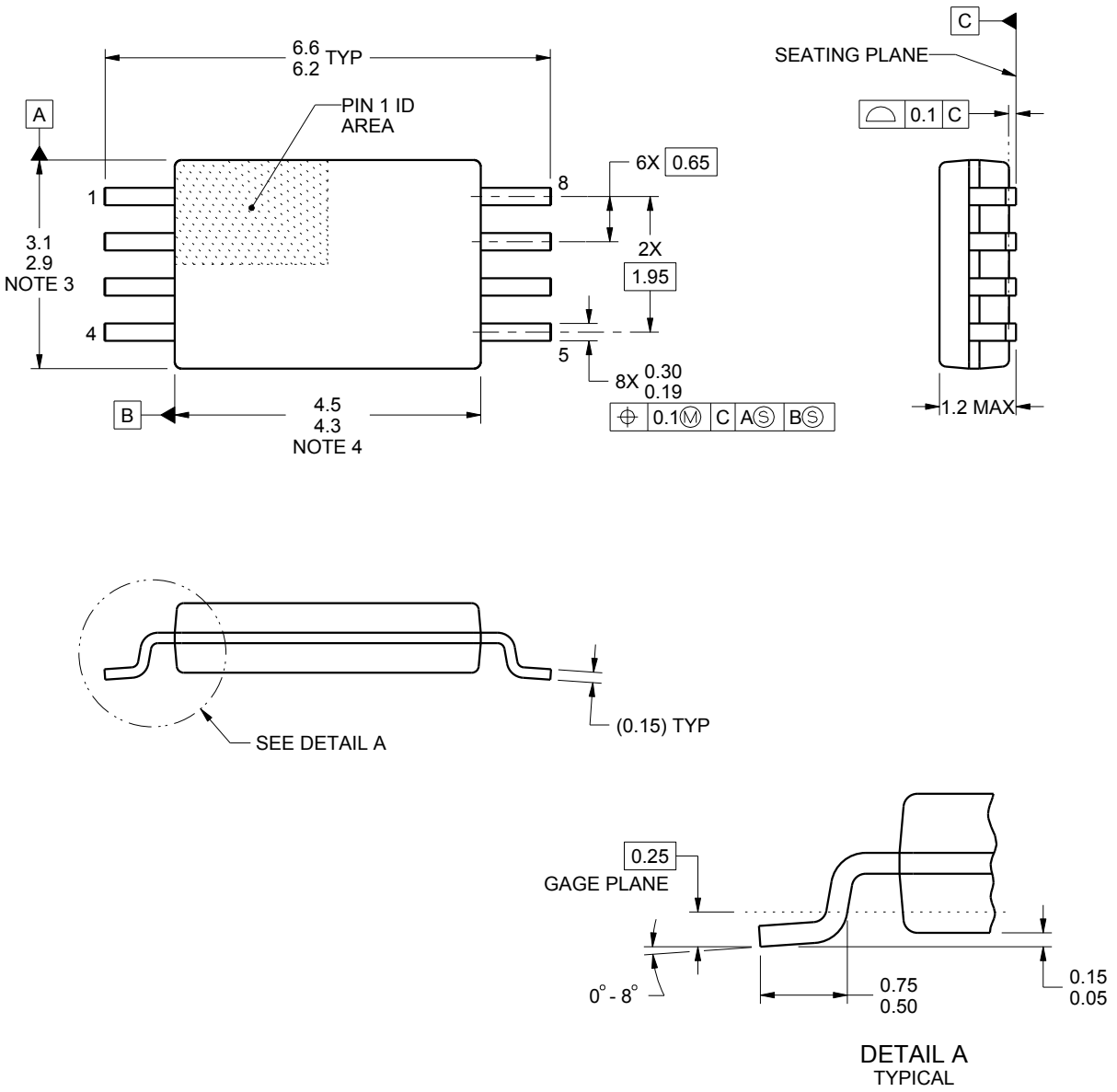
6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGE OUTLINE

PW0008A

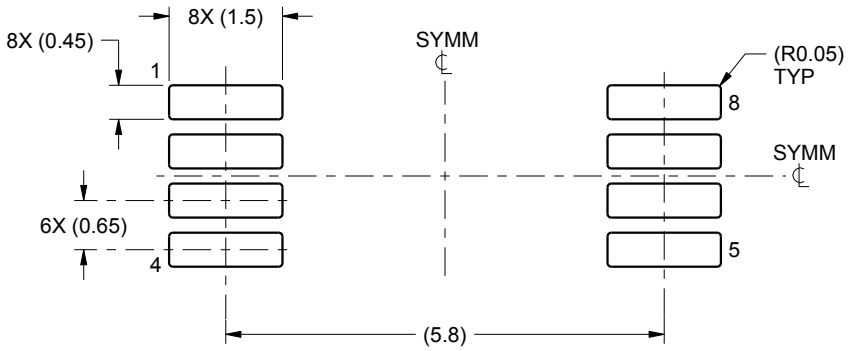
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

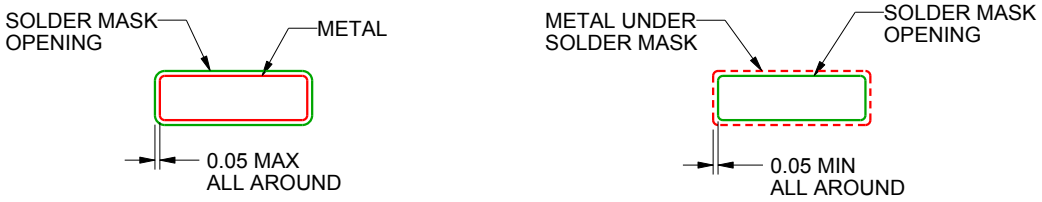


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153, variation AA.



LAND PATTERN EXAMPLE
SCALE:10X

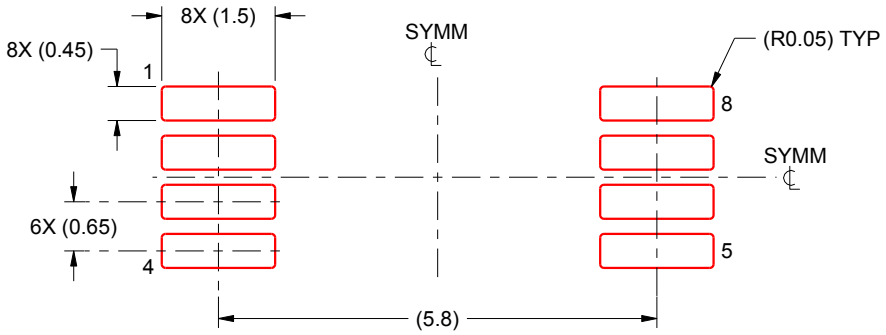


SOLDER MASK DETAILS
NOT TO SCALE

4221848/A 02/2015

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:10X

4221848/A 02/2015

NOTES: (continued)

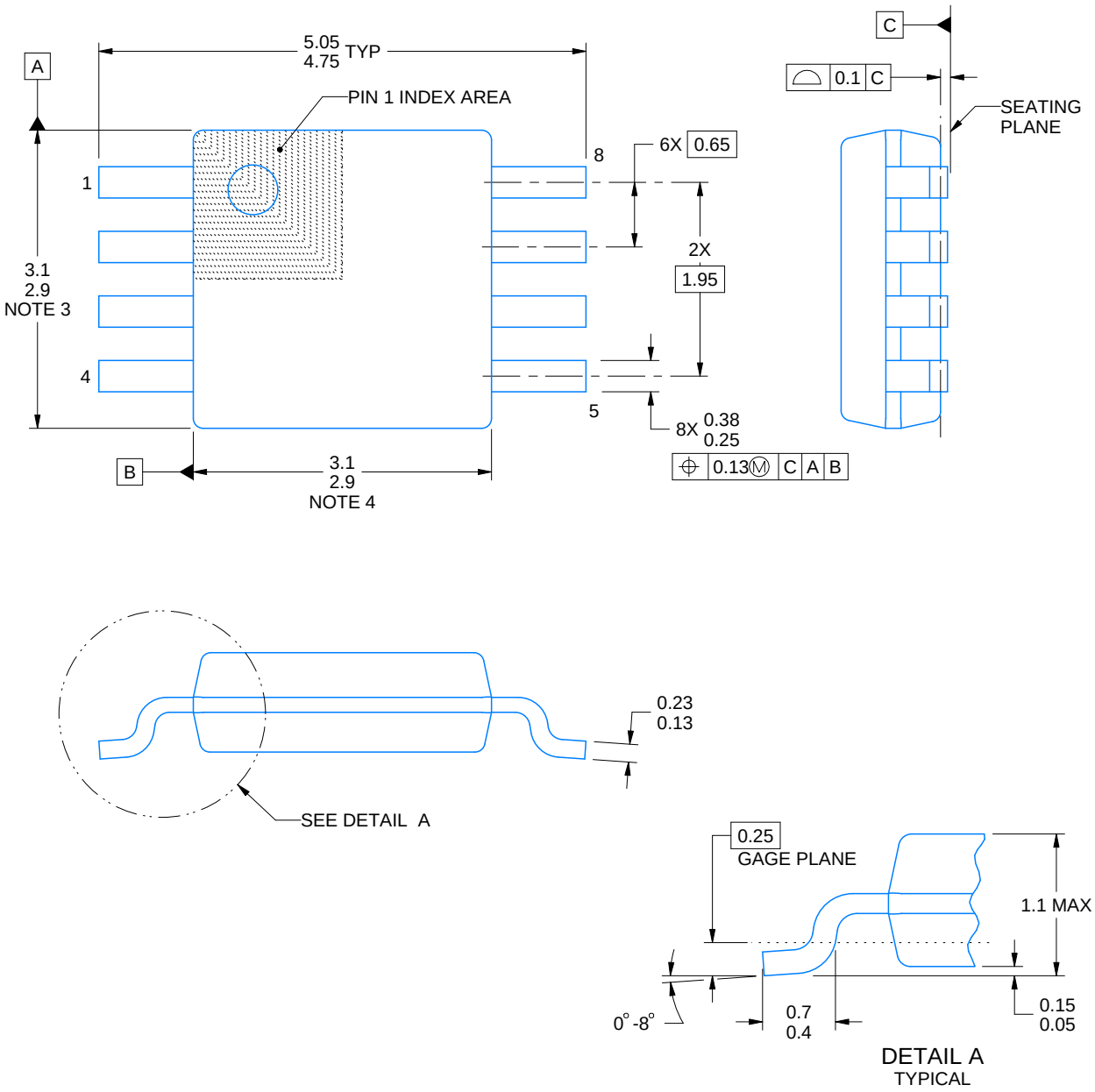
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DGK0008A

VSSOP - 1.1 mm max height

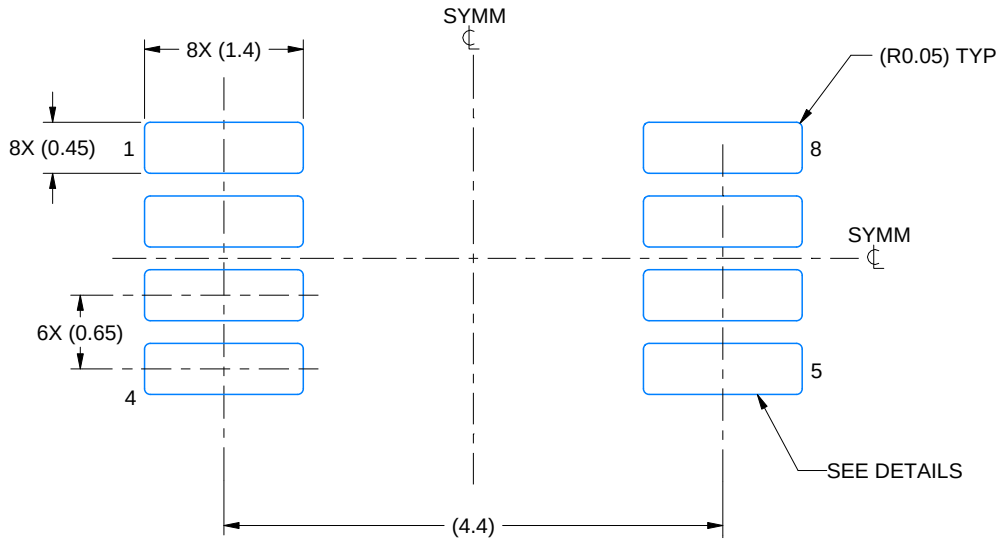
SMALL OUTLINE PACKAGE



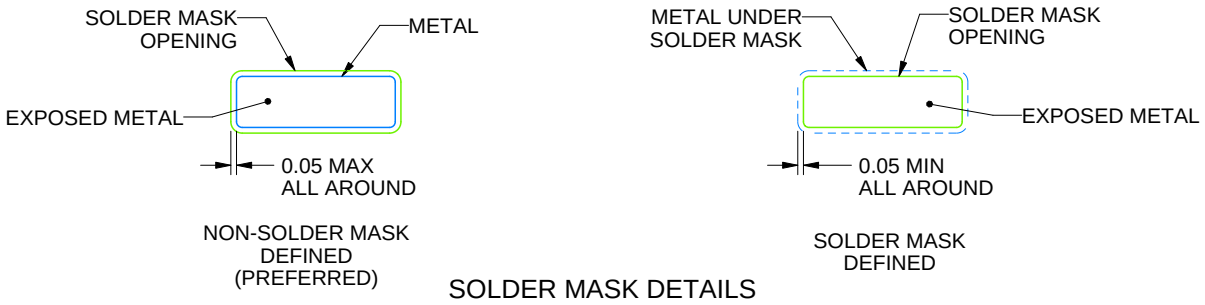
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X

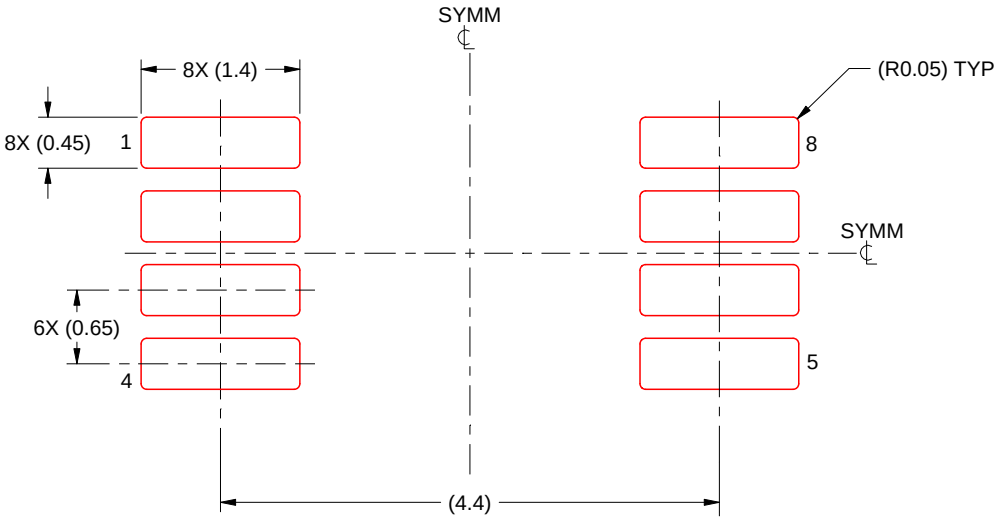


SOLDER MASK DETAILS

4214862/A 04/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
SCALE: 15X

4214862/A 04/2023

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

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最終更新日：2025 年 10 月