TEXAS INSTRUMENTS
LM3103
JAJSAV1G – SEPTEMBER 2007 – REVISED JANUARY 2018

# LM3103 1MHz 0.75A同期整流降圧型レギュレータ

## 1 特長

- 入力電圧範囲: 4.5V～42V
- 出力電流: 0.75A
- 0.6V、±2%の基準電圧
- デュアルNチャネル・メイン/同期整流MOSFET内蔵
- 外付け部品点数が少なく、小型
- セラミック・コンデンサなどの低ESRコンデンサにより安定動作
- ループ補償が不要
- DCM動作による軽負荷時の高効率
- プリバイアス・スタートアップ
- 超高速の過渡応答
- プログラム可能なソフト・スタート
- スイッチング周波数を最高1MHzまでプログラム可能
- バレー電流制限
- サーマル・シャットダウン
- 出力過電圧保護
- 高精度の内部基準電圧により、出力電圧を最低0.6Vまで調整可能
- 放熱特性の優れたHTSSOP-16パッケージ

## 2 アプリケーション

- 5VDC、12VDC、24VDC、12VAC、24VACの各システム
- 組み込みシステム
- 産業用制御
- 車載用テレマティクス/ボディ・エレクトロニクス
- POL (Point of Load)型レギュレータ
- ストレージ・システム
- ブロードバンド・インフラストラクチャ
- 2、3、4セルのリチウム電池システムからの直接変換

## 3 概要

LM3103同期整流降圧コンバータには、高効率でコスト効果の高い降圧レギュレータを実装するため必要な、すべての機能が搭載されています。最小0.6Vの出力電圧で0.75Aの負荷電流を供給できます。Nチャネル同期整流型デュアルMOSFETスイッチにより、外付け部品点数を削減できるため、設計を簡素化し、基板スペースを最小限に抑えられます。

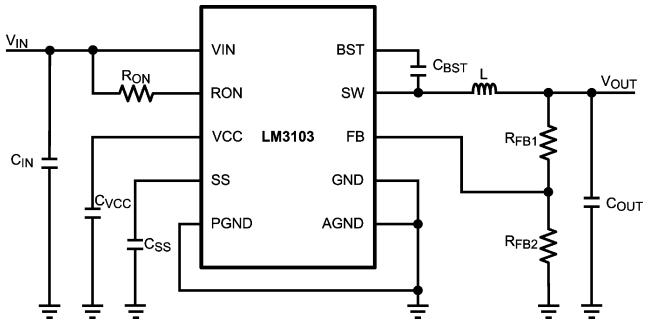
LM3103は、COT制御方式のその他のレギュレータとは異なり、出力コンデンサのESRに依存せずに安定性を確保することが可能で、セラミック・コンデンサなど、ESRの非常に小さい出力コンデンサを接続した場合に極めて良好に動作するように設計されています。ループ補償が必要ないため、高速な負荷過渡応答が得られ、回路の実装が簡単になります。入力電圧とオン時間は反比例の関係にあるため、入力電圧の変動に対して動作周波数はほぼ一定に維持されます。動作周波数は外付け部品による設定が可能で、最大1MHzです。保護機能として、$V_{CC}$の低電圧誤動作防止、出力過電圧保護、サーマル・シャットダウン、ゲート・ドライブの低電圧誤動作防止が搭載されています。LM3103は、放熱特性の優れたHTSSOP-16パッケージで供給されます。

**製品情報(1)**

| 型番 | パッケージ | 本体サイズ(公称) |
|---|---|---|
| LM3103 | HTSSOP-16 | 5.00mm×4.40mm |

(1) 提供されているすべてのパッケージについては、データシートの末尾にある注文情報を参照してください。

**代表的なアプリケーションの回路図**




英語版のTI製品についての情報を翻訳したこの資料は、製品の概要を確認する目的で便宜的に提供しているものです。該当する正式な英語版の最新情報は、www.ti.comで閲覧でき、その内容が常に優先されます。TIでは翻訳の正確性および妥当性につきましては一切保証いたしません。実際の設計などの前には、必ず最新版の英語版をご参照くださいますようお願いいたします。

# 目次

**1** 特長 ... 1
**2** アプリケーション ... 1
**3** 概要 ... 1
**4** 改訂履歴 ... 2
**5** **Pin Configuration and Functions** ... 3
**6** **Specifications** ... 4
6.1 Absolute Maximum Ratings ... 4
6.2 ESD Ratings ... 4
6.3 Recommended Operating Conditions ... 4
6.4 Thermal Information ... 4
6.5 Electrical Characteristics ... 5
6.6 Typical Characteristics ... 7
**7** **Detailed Description** ... 10
7.1 Functional Block Diagram ... 10
7.2 Feature Description ... 10
**8** **Applications and Implementation** ... 14
8.1 Application Information ... 14
**9** デバイスおよびドキュメントのサポート ... 17
9.1 ドキュメントの更新通知を受け取る方法 ... 17
9.2 コミュニティ・リソース ... 17
9.3 商標 ... 17
9.4 静電気放電に関する注意事項 ... 17
9.5 Glossary ... 17
**10** メカニカル、パッケージ、および注文情報 ... 17

## 4 改訂履歴

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

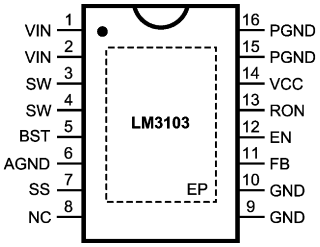
**Revision F (April 2013) から Revision G に変更** **Page**

- データシートのレイアウトをナショナル・セミコンダクター形式からTI形式に変更 ... 1


Copyright © 2007–2018, Texas Instruments Incorporated

# 5 Pin Configuration and Functions

**PWP Package**
**16-Pin HTSSOP**
**Top View**




**Pin Functions**

| Pin | Name | Description | Application Information |
|---|---|---|---|
| 1, 2 | VIN | Input supply voltage | Supply pin to the device. Nominal input range is 4.5 V to 42 V. |
| 3, 4 | SW | Switch Node | Internally connected to the source of the main MOSFET and the drain of the synchronous MOSFET. Connect to the output inductor. |
| 5 | BST | Connection for bootstrap capacitor | Connect a 33 nF capacitor from the SW pin to this pin. This capacitor is charged through an internal diode during the main MOSFET off-time. |
| 6 | AGND | Analog Ground | Ground for all internal circuitry other than the PGND pin. |
| 7 | SS | Soft-start | A 70 µA internal current source charges an external capacitor of larger than 22 nF to provide the soft-start function. |
| 8 | NC | No Connection | This pin should be left unconnected. |
| 9, 10 | GND | Ground | Must be connected to the AGND pin for normal operation. The GND and AGND pins are not internally connected. |
| 11 | FB | Feedback | Internally connected to the regulation and over-voltage comparators. The regulation setting is 0.6 V at this pin. Connect to feedback resistors. |
| 12 | EN | Enable pin | Internal pull-up. Connect to a voltage higher than 1.6 V to enable the device. |
| 13 | RON | On-time Control | An external resistor from the VIN pin to this pin sets the main MOSFET on-time. |
| 14 | VCC | Startup regulator Output | Nominally regulated to 6 V. Connect a capacitor of larger than 1 µF between the VCC and AGND pins for stable operation. |
| 15, 16 | PGND | Power Ground | Synchronous MOSFET source connection. Tie to a ground plane. |
| DAP | EP | Exposed Pad | Thermal connection pad. Connect to the ground plane. |

Copyright © 2007–2018, Texas Instruments Incorporated

# 6 Specifications

## 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

| | MIN | MAX | UNIT |
|---|---|---|---|
| VIN, RON to AGND | –0.3 | 43.5 | V |
| SW to AGND | –0.3 | 43.5 | V |
| SW to AGND (Transient) | | –2 (< 100 ns) | V |
| VIN to SW | –0.3 | 43.5 | V |
| BST to SW | –0.3 | 7 | V |
| VCC to AGND | –0.3 | 7 | V |
| FB to AGND | –0.3 | 5 | V |
| All Other Inputs to AGND | –0.3 | 7 | V |
| Junction Temperature, $T_J$ | | 150 | °C |
| Storage Temperature, $T_{stg}$ | –65 | 150 | °C |

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

## 6.2 ESD Ratings

| | | VALUE | UNIT |
|---|---|---|---|
| $V_{(ESD)}$ Electrostatic discharge | Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1) | ±2 | kV |

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

## 6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)(1)

| | MIN | MAX | UNIT |
|---|---|---|---|
| Supply Voltage Range (VIN) | 4.5 | 42 | V |
| Junction Temperature Range ($T_J$) | −40 | 125 | °C |

(1) *Absolute Maximum Ratings* are limits beyond which damage to the device may occur. *Recommended Operating Ratings* are conditions under which operation of the device is intended to be functional. For ensured specifications and test conditions, see the *Electrical Characteristics*.

## 6.4 Thermal Information

| THERMAL METRIC(1) | | LM3103 PWP (HTSSOP) 16 PINS | UNIT |
|---|---|---|---|
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 35 | °C/W |

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.


Copyright © 2007–2018, Texas Instruments Incorporated

## 6.5 Electrical Characteristics

Specifications with standard type are for $T_J$ = 25°C unless otherwise specified. Minimum and Maximum limits are specified through test, design, or statistical correlation. Typical values represent the most likely parametric norm at $T_J$ = 25°C, and are provided for reference purposes only. Unless otherwise stated the following conditions apply: $V_{IN}$ = 18 V, $V_{OUT}$ = 3.3 V.

| PARAMETER | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| **START-UP REGULATOR, $V_{CC}$** | | | | | | | |
| $V_{CC}$ | $V_{CC}$ output voltage | $C_{VCC}$ = 1 µF, no load | $T_J$ = –40°C to +125°C | 5.6 | 6.0 | 6.2 | V |
| $V_{IN} – V_{CC}$ | $V_{IN} – V_{CC}$ dropout voltage | $I_{CC}$ = 2 mA | $T_J$ = –40°C to +125°C | | 55 | 150 | mV |
| | | $I_{CC}$ = 10 mA | $T_J$ = –40°C to +125°C | | 235 | 500 | |
| $V_{CC-UVLO}$ | $V_{CC}$ undervoltage lockout threshold (UVLO) | $V_{IN}$ increasing | $T_J$ = –40°C to +125°C | 3.5 | 3.7 | 4.1 | V |
| $V_{CC-UVLO-HYS}$ | $V_{CC}$ UVLO hysteresis | $V_{IN}$ decreasing | | | 275 | | mV |
| $I_{IN}$ | $I_{IN}$ operating current | No switching, $V_{FB}$ = 1 V | $T_J$ = –40°C to +125°C | | 1.0 | 1.25 | mA |
| $I_{IN-SD}$ | $I_{IN}$ operating current, device shutdown | $V_{EN}$ = 0 V | $T_J$ = –40°C to +125°C | | 20 | 40 | µA |
| $I_{VCC}$ | $V_{CC}$ current limit | $V_{CC}$ = 0 V | $T_J$ = –40°C to +125°C | 20 | 33 | 42 | mA |
| **SWITCHING CHARACTERISTICS** | | | | | | | |
| $R_{DS-UP-ON}$ | Main MOSFET $R_{DS(on)}$ | $T_J$ = –40°C to +125°C | | | 0.370 | 0.7 | Ω |
| $R_{DS-DN-ON}$ | Syn. MOSFET $R_{DS(on)}$ | $T_J$ = –40°C to +125°C | | | 0.220 | 0.4 | Ω |
| **SOFT-START** | | | | | | | |
| $I_{SS}$ | SS pin source current | $V_{SS}$ = 0 V | $T_J$ = –40°C to +125°C | 45 | 70 | 95 | µA |

Copyright © 2007–2018, Texas Instruments Incorporated

## Electrical Characteristics (continued)

Specifications with standard type are for $T_J$ = 25°C unless otherwise specified. Minimum and Maximum limits are specified through test, design, or statistical correlation. Typical values represent the most likely parametric norm at $T_J$ = 25°C, and are provided for reference purposes only. Unless otherwise stated the following conditions apply: $V_{IN}$ = 18 V, $V_{OUT}$ = 3.3 V.

| PARAMETER | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| **CURRENT LIMIT** | | | | | | | |
| $I_{CL}$ | Syn. MOSFET current limit threshold | | | | 0.9 | | A |
| **ON/OFF TIMER** | | | | | | | |
| $t_{on}$ | ON timer pulse width | $V_{IN}$ = 10 V, $R_{ON}$ = 33 kΩ | | | 0.350 | | µs |
| | | $V_{IN}$ = 18 V, $R_{ON}$ = 33 kΩ | | | 0.170 | | |
| $t_{on-MIN}$ | ON timer minimum pulse width | | | | 100 | | ns |
| $t_{off}$ | OFF timer pulse width | | | | 240 | | ns |
| **ENABLE INPUT** | | | | | | | |
| $V_{EN}$ | EN Pin input threshold | $V_{EN}$ rising | $T_J$ = –40°C to +125°C | | 1.6 | 1.85 | V |
| $V_{EN-HYS}$ | Enable threshold hysteresis | $V_{EN}$ falling | | | 230 | | mV |
| $I_{EN}$ | Enable Pull-up Current | $V_{EN}$ = 0 V | | | 1 | | µA |
| **REGULATION AND OVERVOLTAGE COMPARATOR** | | | | | | | |
| $V_{FB}$ | In-regulation feedback voltage | $T_J$ = –40°C to +125°C | | 0.588 | 0.6 | 0.612 | V |
| $V_{FB-OV}$ | Feedback overvoltage threshold | $T_J$ = –40°C to +125°C | | 0.655 | 0.680 | 0.705 | V |
| $I_{FB}$ | | | | | 1 | | nA |
| **THERMAL SHUTDOWN** | | | | | | | |
| $T_{SD}$ | Thermal shutdown temperature | $T_J$ rising | | | 165 | | °C |
| $T_{SD-HYS}$ | Thermal shutdown temperature hysteresis | $T_J$ falling | | | 20 | | °C |


Copyright © 2007–2018, Texas Instruments Incorporated

## 6.6 Typical Characteristics

All curves are taken at $V_{IN}$ = 18 V with the configuration in the typical application circuit for $V_{OUT}$ = 3.3 V shown in this datasheet. $T_A$ = 25°C, unless otherwise specified.

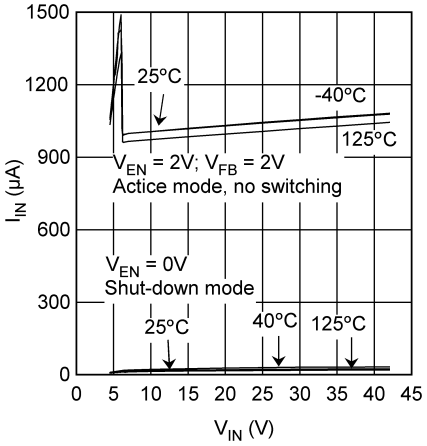



**Figure 1. Quiescent Current, $I_{IN}$ vs $V_{IN}$**

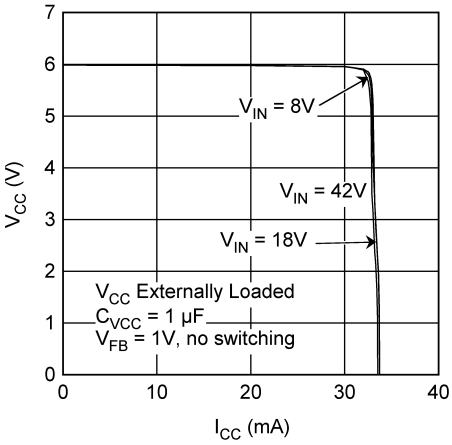



**Figure 2. $V_{CC}$ vs $I_{CC}$**

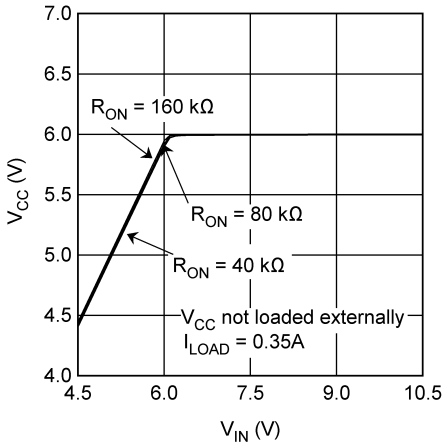



**Figure 3. $V_{CC}$ vs $V_{IN}$**

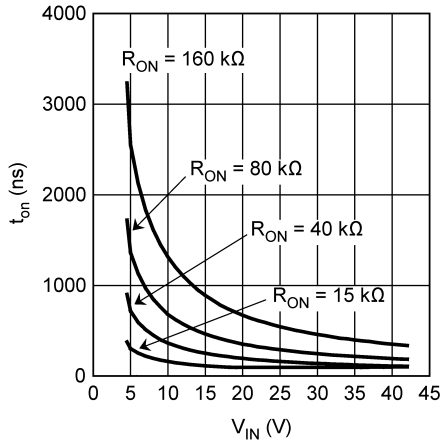



**Figure 4. $t_{on}$ vs $V_{IN}$**

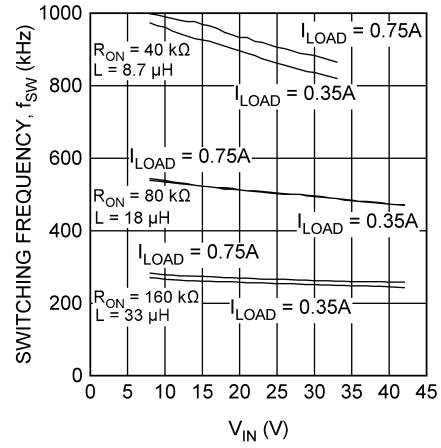



**Figure 5. Switching Frequency, $f_{SW}$ vs $V_{IN}$**

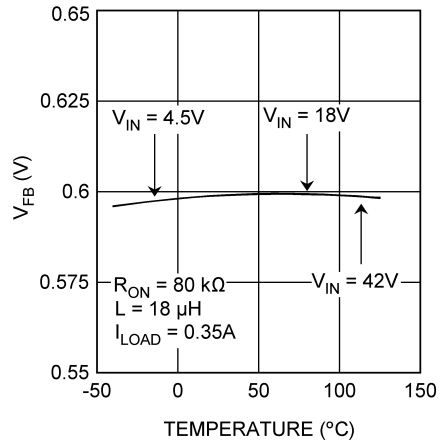



**Figure 6. $V_{FB}$ vs Temperature**

## Typical Characteristics (continued)

All curves are taken at $V_{IN}$ = 18 V with the configuration in the typical application circuit for $V_{OUT}$ = 3.3 V shown in this datasheet. $T_A$ = 25°C, unless otherwise specified.

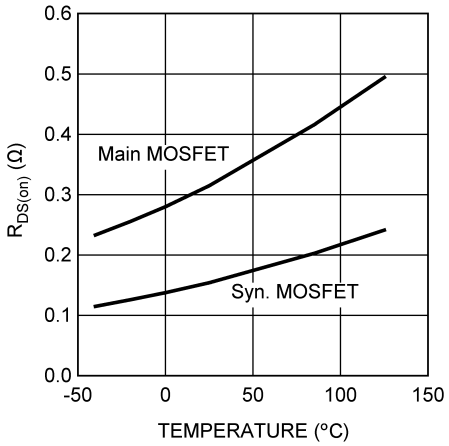



**Figure 7. $R_{DS(on)}$ vs Temperature**

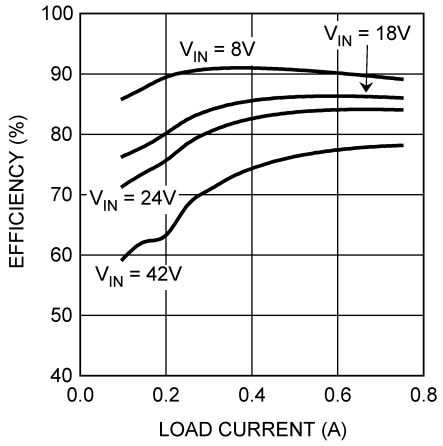



**Figure 8. Efficiency vs Load Current ($V_{OUT}$ = 3.3 V)**

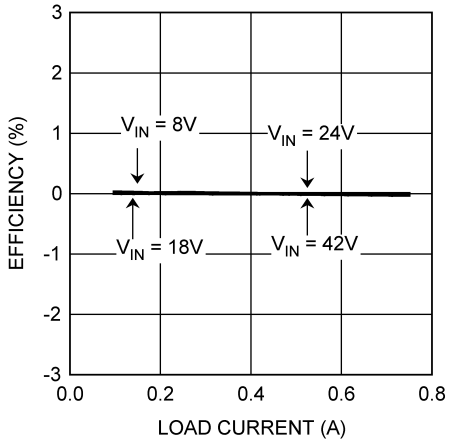



**Figure 9. $V_{OUT}$ Regulation vs Load Current ($V_{OUT}$ = 3.3 V)**

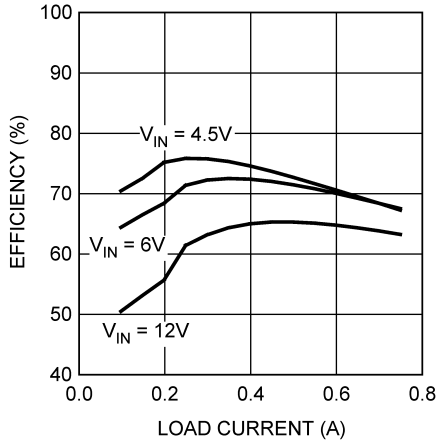



**Figure 10. Efficiency vs Load Current ($V_{OUT}$ = 0.6 V)**

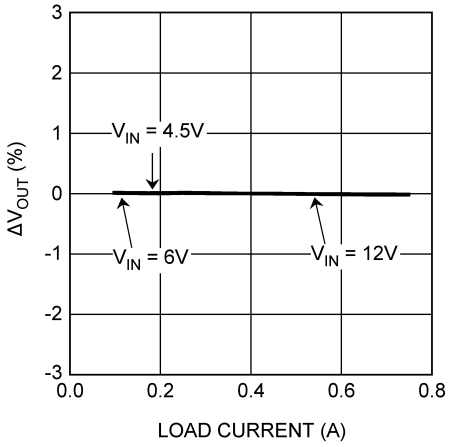



**Figure 11. $V_{OUT}$ Regulation vs Load Current ($V_{OUT}$ = 0.6 V)**

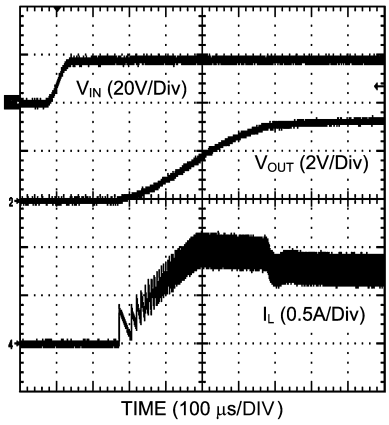



**Figure 12. Power Up ($V_{OUT}$ = 3.3 V, 0.75 A Loaded)**


Copyright © 2007–2018, Texas Instruments Incorporated

## Typical Characteristics (continued)

All curves are taken at $V_{IN}$ = 18 V with the configuration in the typical application circuit for $V_{OUT}$ = 3.3 V shown in this datasheet. $T_A$ = 25°C, unless otherwise specified.

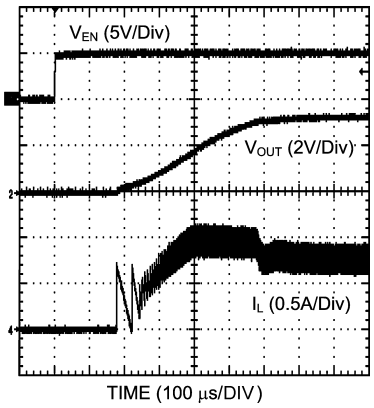



**Figure 13. Enable Transient ($V_{OUT}$ = 3.3 V, 0.75 A Loaded)**

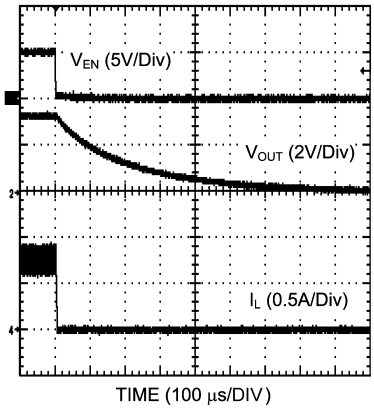



**Figure 14. Shutdown Transient ($V_{OUT}$ = 3.3 V, 0.75 A Loaded)**

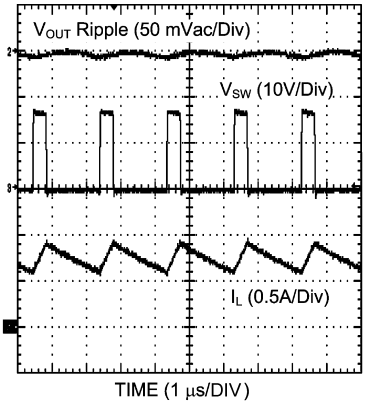



**Figure 15. Continuous Mode Operation ($V_{OUT}$ = 3.3 V, 2.5 A Loaded)**

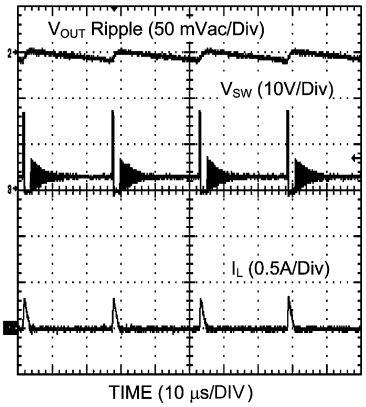



**Figure 16. Discontinuous Mode Operation ($V_{OUT}$ = 3.3 V, 0.02 A Loaded)**

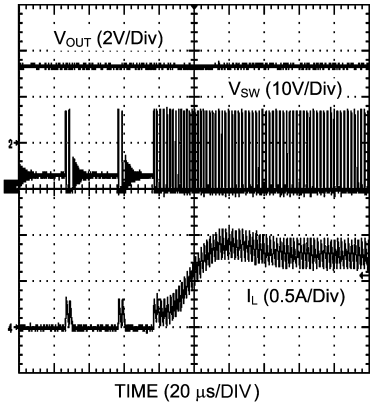



**Figure 17. DCM to CCM Transition ($V_{OUT}$ = 3.3 V, 0.01 A - 0.75 A Load)**

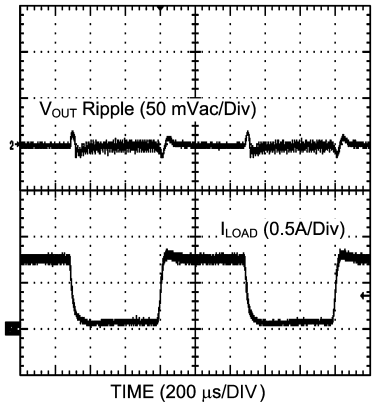
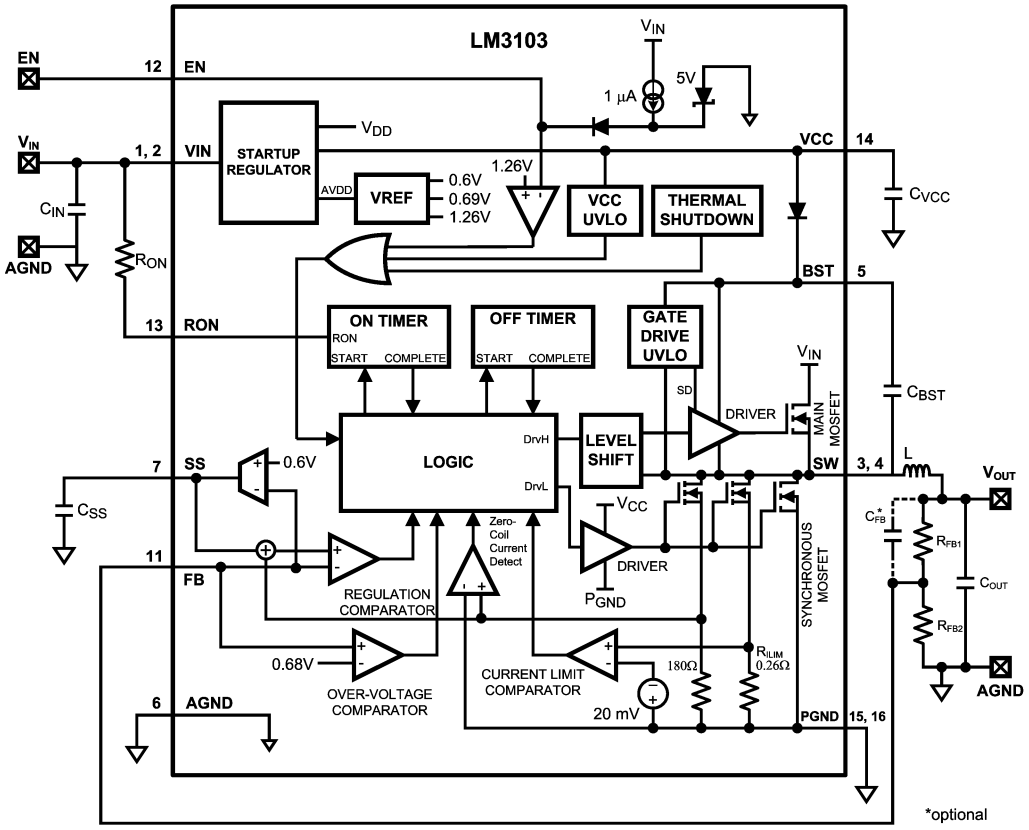



**Figure 18. Load Transient ($V_{OUT}$ = 3.3 V, 0.075 A - 0.75 A Load, Current slew-rate: 2.5 A/µs)**

Copyright © 2007–2018, Texas Instruments Incorporated

# 7 Detailed Description

## 7.1 Functional Block Diagram




## 7.2 Feature Description

The LM3103 Step Down Switching Regulator features all required functions to implement a cost effective, efficient buck power converter which is capable of supplying 0.75 A to loads. It contains dual N-Channel main and synchronous MOSFETs. The Constant ON-Time (COT) regulation scheme requires no loop compensation, results in a fast load transient response and simple circuit implementation. The regulator can function properly even with an all ceramic output capacitor network, and does not rely on the output capacitor's ESR for stability. The operating frequency remains constant with line variations due to the inverse relationship between the input voltage and the on-time. The valley current limit detection circuit, with a limit set internally at 0.9 A, inhibits the main MOSFET until the inductor current level subsides.

The LM3103 can be applied in numerous applications and can operate efficiently for inputs as high as 42 V. Protection features include $V_{CC}$ under-voltage lockout, output over-voltage protection, thermal shutdown, gate drive under-voltage lock-out. The LM3103 is available in the thermally enhanced HTSSOP-16 package.

### 7.2.1 COT Control Circuit Overview

COT control is based on a comparator and a one-shot on-timer, with the output voltage feedback (feeding to the FB pin) compared with a 0.6 V internal reference. If the voltage of the FB pin is below the reference, the main MOSFET is turned on for a fixed on-time determined by a programming resistor RON and the input voltage $V_{IN}$, upon which the on-time varies inversely. Following the on-time, the main MOSFET remains off for a minimum of 240 ns. Then, if the voltage of the FB pin is below the reference, the main MOSFET is turned on again for another on-time period. The switching will continue to achieve regulation.


Copyright © 2007–2018, Texas Instruments Incorporated

## Feature Description (continued)

The regulator will operate in the discontinuous conduction mode (DCM) at a light load, and the continuous conduction mode (CCM) with a heavy load. In the DCM, the current through the inductor starts at zero and ramps up to a peak during the on-time, and then ramps back to zero before the end of the off-time. It remains zero and the load current is supplied entirely by the output capacitor. The next on-time period starts when the voltage at the FB pin falls below the internal reference. The operating frequency in the DCM is lower and varies larger with the load current as compared with the CCM. Conversion efficiency is maintained since conduction loss and switching loss are reduced with the reduction in the load and the switching frequency respectively. The operating frequency in the DCM can be calculated approximately as follows:

$$f_{SW} = \frac{V_{OUT} (V_{IN} - 1) \times L \times 1.18 \times 10^{20} \times I_{OUT}}{(V_{IN} - V_{OUT}) \times R_{ON}^2} \quad (1)$$

In the continuous conduction mode (CCM), the current flows through the inductor in the entire switching cycle, and never reaches zero during the off-time. The operating frequency remains relatively constant with load and line variations. The CCM operating frequency can be calculated approximately as follows:

$$f_{SW} = \frac{V_{OUT}}{8.3 \times 10^{-11} \times R_{ON}} \quad (2)$$

The output voltage is set by two external resistors $R_{FB1}$ and $R_{FB2}$. The regulated output voltage is

$$V_{OUT} = 0.6V \times (R_{FB1} + R_{FB2})/R_{FB2} \quad (3)$$

### 7.2.2 Startup Regulator ($V_{CC}$)

A startup regulator is integrated within the LM3103. The input pin VIN can be connected directly to a line voltage up to 42 V. The $V_{CC}$ output regulates at 6 V, and is current limited to 30 mA. Upon power up, the regulator sources current into an external capacitor $C_{VCC}$, which is connected to the VCC pin. For stability, $C_{VCC}$ must be at least 1 µF. When the voltage on the VCC pin is higher than the under-voltage lock-out (UVLO) threshold of 3.7 V, the main MOSFET is enabled and the SS pin is released to allow the soft-start capacitor $C_{SS}$ to charge.

The minimum input voltage is determined by the dropout voltage of the regulator and the $V_{CC}$ UVLO falling threshold (≅3.4 V). If $V_{IN}$ is less than ≅4.0 V, the regulator shuts off and $V_{CC}$ goes to zero.

### 7.2.3 Regulation Comparator

The feedback voltage at the FB pin is compared to a 0.6 V internal reference. In normal operation (the output voltage is regulated), an on-time period is initiated when the voltage at the FB pin falls below 0.6 V. The main MOSFET stays on for the programmed on-time, causing the output voltage to rise and consequently the voltage of the FB pin to rise above 0.6 V. After the on-time period, the main MOSFET stays off until the voltage of the FB pin falls below 0.6 V again. Bias current at the FB pin is nominally 1 nA.

### 7.2.4 Zero Coil Current Detect

The current of the synchronous MOSFET is monitored by a zero coil current detection circuit which inhibits the synchronous MOSFET when its current reaches zero until the next on-time. This circuit enables the DCM operation, which improves the efficiency at a light load.

### 7.2.5 Over-Voltage Comparator

The voltage at the FB pin is compared to a 0.68 V internal reference. If it rises above 0.68 V, the on-time is immediately terminated. This condition is known as over-voltage protection (OVP). It can occur if the input voltage or the output load changes suddenly. Once the OVP is activated, the main MOSFET remains off until the voltage at the FB pin falls below 0.6 V. The synchronous MOSFET will stay on to discharge the inductor until the inductor current reduces to zero and then switch off.

### 7.2.6 ON-Time Timer, Shutdown

The on-time of the LM3103 main MOSFET is determined by the resistor $R_{ON}$ and the input voltage $V_{IN}$. It is calculated as follows:

$$t_{ON} = \frac{8.3 \times 10^{-11} \times R_{ON}}{V_{IN}} \quad (4)$$

Copyright © 2007–2018, Texas Instruments Incorporated

## Feature Description (continued)

The inverse relationship of $t_{on}$ and $V_{IN}$ gives a nearly constant frequency as $V_{IN}$ is varied. $R_{ON}$ should be selected such that the on-time at maximum $V_{IN}$ is greater than 100 ns. The on-timer has a limiter to ensure a minimum of 100 ns for $t_{on}$. This limits the maximum operating frequency, which is governed by the following equation:

$$f_{SW(MAX)} = \frac{V_{OUT}}{V_{IN(MAX)} \times 100\ ns} \quad (5)$$

The LM3103 can be remotely shut down by pulling the voltage of the EN pin below 1.6 V. In this shutdown mode, the SS pin is internally grounded, the on-timer is disabled, and bias currents are reduced. Releasing the EN pin allows normal operation to resume because the EN pin is internally pulled up.

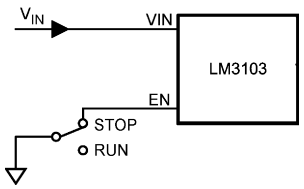



**Figure 19. Shutdown Implementation**

### 7.2.7 Current Limit

Current limit detection is carried out during the off-time by monitoring the re-circulating current through the synchronous MOSFET. Referring to the Functional Block Diagram, when the main MOSFET is turned off, the inductor current flows through the load, the PGND pin and the internal synchronous MOSFET. If this current exceeds 0.9 A, the current limit comparator toggles, and as a result the start of the next on-time period is disabled. The next switching cycle starts when the re-circulating current falls back below 0.9 A (and the voltage at the FB pin is below 0.6 V). The inductor current is monitored during the on-time of the synchronous MOSFET. As long as the inductor current exceeds 0.9 A, the main MOSFET will remain inhibited to achieve current limit. The operating frequency is lower during current limit owing to a longer off-time.

Figure 20 illustrates an inductor current waveform. On average, the output current $I_{OUT}$ is the same as the inductor current $I_L$, which is the average of the rippled inductor current. In case of current limit (the current limit portion of Figure 20), the next on-time will not initiate until that the current drops below 0.9 A (assume the voltage at the FB pin is lower than 0.6 V). During each on-time the current ramps up an amount equal to:

$$I_{LR} = \frac{(V_{IN} - V_{OUT}) \times t_{on}}{L} \quad (6)$$

During current limit, the LM3103 operates in a constant current mode with an average output current $I_{OUT(CL)}$ equal to 0.9 A + $I_{LR}$ / 2.


Copyright © 2007–2018, Texas Instruments Incorporated

## Feature Description (continued)

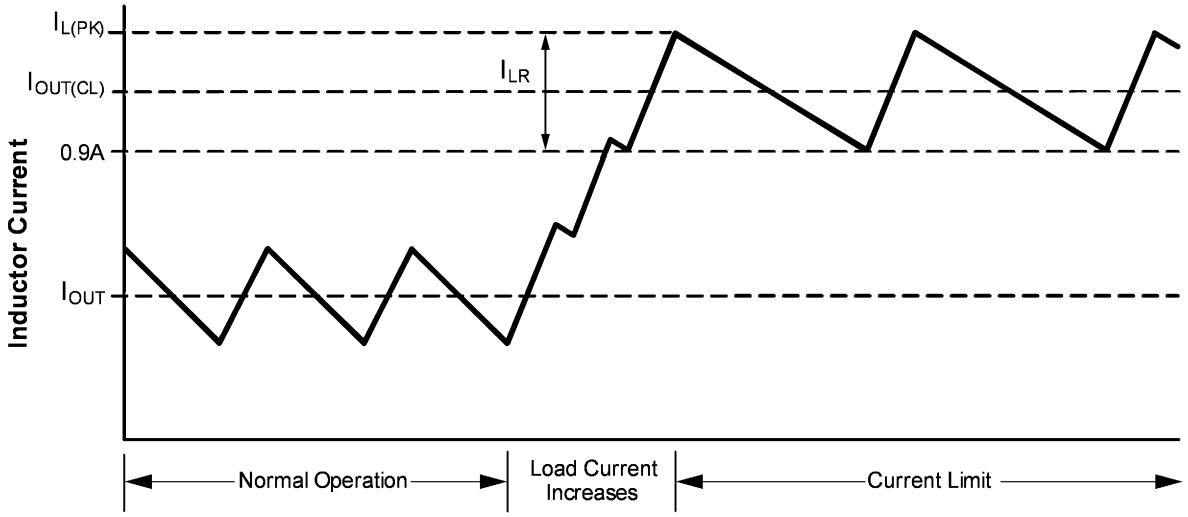



**Figure 20. Inductor Current - Current Limit Operation**

### 7.2.8 N-Channel MOSFET and Driver

The LM3103 integrates an N-Channel main MOSFET and an associated floating high voltage main MOSFET gate driver. The gate drive circuit works in conjunction with an external bootstrap capacitor $C_{BST}$ and an internal high voltage diode. $C_{BST}$ connected between the BST and SW pins powers the main MOSFET gate driver during the main MOSFET on-time. During each off-time, the voltage of the SW pin falls to approximately –1 V, and $C_{BST}$ charges from $V_{CC}$ through the internal diode. The minimum off-time of 240 ns provides enough time for charging $C_{BST}$ in each cycle.

### 7.2.9 Soft-Start

The soft-start feature allows the converter to gradually reach a steady state operating point, thereby reducing startup stresses and current surges. Upon turn-on, after $V_{CC}$ reaches the under-voltage threshold and a 180 µs fixed delay, a 70 µA internal current source charges an external capacitor $C_{SS}$ connecting to the SS pin. The ramping voltage at the SS pin (and the non-inverting input of the regulation comparator as well) ramps up the output voltage $V_{OUT}$ in a controlled manner. An internal switch grounds the SS pin if any of the following three cases happen: (i) $V_{CC}$ is below the under-voltage lockout threshold; (ii) a thermal shutdown occurs; or (iii) the EN pin is grounded. Alternatively, the output voltage can be shut off by connecting the SS pin to the ground using an external switch. Releasing the switch allows the voltage of the SS pin to ramp up and the output voltage to return to normal. The shutdown configuration is shown in Figure 21.

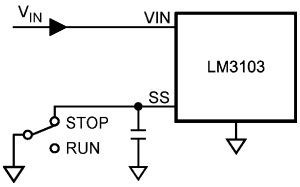



**Figure 21. Alternate Shutdown Implementation**

### 7.2.10 Thermal Protection

The junction temperature of the LM3103 should not exceed the maximum limit. Thermal protection is implemented by an internal Thermal Shutdown circuit, which activates (typically) at 165°C to make the controller enter a low power reset state by disabling the main MOSFET, disabling the on-timer, and grounding the SS pin. Thermal protection helps prevent catastrophic failures from accidental device overheating. When the junction temperature falls back below 145°C (typical hysteresis = 20°C), the SS pin is released and normal operation resumes.

Copyright © 2007–2018, Texas Instruments Incorporated

# 8 Applications and Implementation

**NOTE**

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

## 8.1 Application Information

### 8.1.1 External Components

The following guidelines can be used to select external components.

**$R_{FB1}$ and $R_{FB2}$** : These resistors should be chosen from standard values in the range of 1.0 kΩ to 10 kΩ, satisfying the following ratio:

$$R_{FB1}/R_{FB2} = (V_{OUT}/0.6\ V) - 1 \quad (7)$$

For $V_{OUT}$ = 0.6 V, the FB pin can be connected to the output directly with a pre-load resistor drawing more than 20 µA. This is because the converter operation needs a minimum inductor current ripple to maintain good regulation when no load is connected.

**$R_{ON}$:** Equation 2 can be used to select $R_{ON}$ if a desired operating frequency is selected. But the minimum value of $R_{ON}$ is determined by the minimum on-time. It can be calculated as follows:

$$R_{ON} \geq \frac{V_{IN(MAX)} \times 100\ ns}{8.3 \times 10^{-11}} \quad (8)$$

If $R_{ON}$ calculated from Equation 2 is smaller than the minimum value determined in Equation 8, a lower frequency should be selected to re-calculate $R_{ON}$ by Equation 2. Alternatively, $V_{IN(MAX)}$ can also be limited in order to keep the frequency unchanged. The relationship of $V_{IN(MAX)}$ and $R_{ON}$ is shown in Figure 22.

On the other hand, the minimum off-time of 240 ns can limit the maximum duty ratio. This may be significant at low $V_{IN}$. A larger $R_{ON}$ should be selected in any application requiring a large duty ratio.

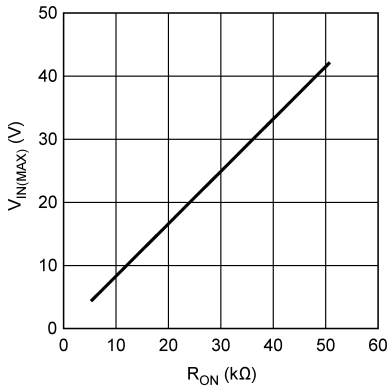



**Figure 22. Maximum $V_{IN}$ for selected $R_{ON}$**

**L:** The main parameter affected by the inductor is the amplitude of the inductor current ripple ($I_{LR}$), which is recommended to be greater than 0.3 A. Once $I_{LR}$ is selected, L can be determined by:

$$L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{I_{LR} \times f_{SW} \times V_{IN}} \quad (9)$$

where $V_{IN}$ is the input voltage and $f_{SW}$ is determined from Equation 2.


Copyright © 2007–2018, Texas Instruments Incorporated

## Application Information (continued)

If the output current $I_{OUT}$ is known, by assuming that $I_{OUT} = I_L$, the peak and valley of $I_{LR}$ can be determined. Beware that the peak of $I_{LR}$ should not be larger than the saturation current of the inductor and the current rating of the main and synchronous MOSFETs. Also, the valley of $I_{LR}$ must be positive if CCM operation is required.

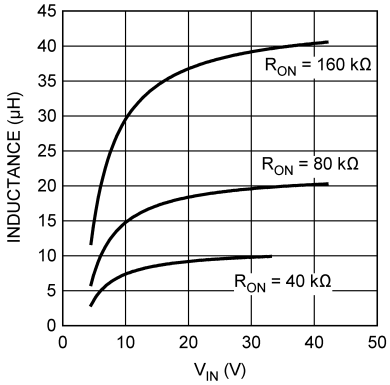



**Figure 23. Inductor selection for $V_{OUT}$ = 3.3 V**

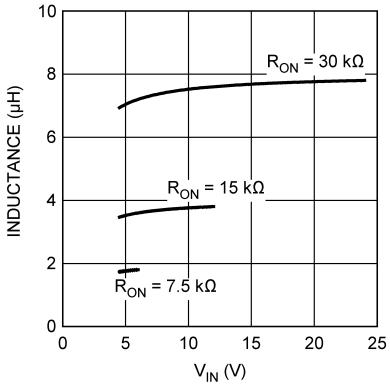



**Figure 24. Inductor selection for $V_{OUT}$ = 0.6 V**

Figure 23 and Figure 24 show curves on inductor selection for various $V_{OUT}$ and $R_{ON}$. According to Equation 8, $V_{IN}$ is limited for small $R_{ON}$. Some curves are therefore limited as shown in the figures.

**$C_{VCC}$:** The capacitor on the $V_{CC}$ output provides not only noise filtering and stability, but also prevents false triggering of the $V_{CC}$ UVLO at the main MOSFET on/off transitions. $C_{VCC}$ should be no smaller than 1 µF for stability, and should be a good quality, low ESR, ceramic capacitor.

**$C_{OUT}$ and $C_{OUT3}$:** $C_{OUT}$ should generally be no smaller than 10 µF. Experimentation is usually necessary to determine the minimum value for $C_{OUT}$, as the nature of the load may require a larger value. A load which creates significant transients requires a larger $C_{OUT}$ than a fixed load.

$C_{OUT3}$ is a small value ceramic capacitor located close to the LM3103 to further suppress high frequency noise at $V_{OUT}$. A 47 nF capacitor is recommended.

**$C_{IN}$ and $C_{IN3}$:** The function of $C_{IN}$ is to supply most of the main MOSFET current during the on-time, and limit the voltage ripple at the VIN pin, assuming that the voltage source connecting to the VIN pin has finite output impedance. If the voltage source's dynamic impedance is high (effectively a current source), $C_{IN}$ supplies the difference between the instantaneous input current and the average input current.

At the maximum load current, when the main MOSFET turns on, the current to the VIN pin suddenly increases from zero to the valley of the inductor's ripple current and ramps up to the peak value. It then drops to zero at turn-off. The average current during the on-time is the load current. For a worst case calculation, $C_{IN}$ must be capable of supplying this average load current during the maximum on-time. $C_{IN}$ is calculated from:

Copyright © 2007–2018, Texas Instruments Incorporated

## Application Information (continued)

$$C_{IN} = \frac{I_{OUT} \times t_{ON}}{\Delta V_{IN}} \quad (10)$$

where $I_{OUT}$ is the load current, $t_{on}$ is the maximum on-time, and $\Delta V_{IN}$ is the allowable ripple voltage at $V_{IN}$.

$C_{IN3}$'s purpose is to help avoid transients and ringing due to long lead inductance at the VIN pin. A low ESR 0.1 µF ceramic chip capacitor located close to the LM3103 is recommended.

**$C_{BST}$:** A 33 nF high quality ceramic capacitor with low ESR is recommended for $C_{BST}$ since it supplies a surge current to charge the main MOSFET gate driver at each turn-on. Low ESR also helps ensure a complete recharge during each off-time.

**$C_{SS}$:** The capacitor at the SS pin determines the soft-start time, i.e. the time for the reference voltage at the regulation comparator and therefore, the output voltage to reach their final value. The time is determined from the following equation:

$$t_{SS} = 180\ \mu s + \frac{C_{SS} \times 0.6V}{70\ \mu A} \quad (11)$$

**$C_{FB}$:** If the output voltage is higher than 1.6 V, $C_{FB}$ is needed in the Discontinuous Conduction Mode to reduce the output ripple. The recommended value for $C_{FB}$ is 10 nF.


Copyright © 2007–2018, Texas Instruments Incorporated

# 9 デバイスおよびドキュメントのサポート

## 9.1 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、ti.comのデバイス製品フォルダを開いてください。右上の隅にある「*通知を受け取る*」をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

## 9.2 コミュニティ・リソース

**以下のリンクから、TIのコミュニティ・リソースにアクセスできます。リンクされているコンテンツは、該当する貢献者により、現状のまま提供されるものです。これらはTIの仕様を構成するものではなく、必ずしもTIの見解を反映したものではありません。TIの使用条件を参照してください。**

**TI E2E™オンライン・コミュニティ** ***TIのE2E（Engineer-to-Engineer）コミュニティ。*****エンジニア間の共同作業を促進するために開設されたものです。e2e.ti.comでは、他のエンジニアに質問し、知識を共有し、アイディアを検討して、問題解決に役立てることができます。**

**設計サポート** ***TIの設計サポート*** **役に立つE2Eフォーラムや、設計サポート・ツールをすばやく見つけることができます。技術サポート用の連絡先情報も参照できます。**

## 9.3 商標

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

## 9.4 静電気放電に関する注意事項



すべての集積回路は、適切なESD保護方法を用いて、取扱いと保存を行うようにして下さい。

静電気放電はわずかな性能の低下から完全なデバイスの故障に至るまで、様々な損傷を与えます。高精度の集積回路は、損傷に対して敏感であり、極めてわずかなパラメータの変化により、デバイスに規定された仕様に適合しなくなる場合があります。

## 9.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

# 10 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。この情報は、そのデバイスについて利用可能な最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

Copyright © 2007–2018, Texas Instruments Incorporated

## PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package \| Pins | Package qty \| Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|---|---|---|---|---|---|---|---|---|---|
| LM3103MH/NOPB | Active | Production | HTSSOP (PWP) \| 16 | 92 \| TUBE | Yes | SN | Level-1-260C-UNLIM | -40 to 125 | LM3103 MH |
| LM3103MH/NOPB.A | Active | Production | HTSSOP (PWP) \| 16 | 92 \| TUBE | Yes | SN | Level-1-260C-UNLIM | -40 to 125 | LM3103 MH |
| LM3103MH/NOPB.B | Active | Production | HTSSOP (PWP) \| 16 | 92 \| TUBE | Yes | SN | Level-1-260C-UNLIM | -40 to 125 | LM3103 MH |
| LM3103MHX/NOPB | Active | Production | HTSSOP (PWP) \| 16 | 2500 \| LARGE T&R | Yes | SN | Level-1-260C-UNLIM | -40 to 125 | LM3103 MH |
| LM3103MHX/NOPB.A | Active | Production | HTSSOP (PWP) \| 16 | 2500 \| LARGE T&R | Yes | SN | Level-1-260C-UNLIM | -40 to 125 | LM3103 MH |
| LM3103MHX/NOPB.B | Active | Production | HTSSOP (PWP) \| 16 | 2500 \| LARGE T&R | Yes | SN | Level-1-260C-UNLIM | -40 to 125 | LM3103 MH |

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

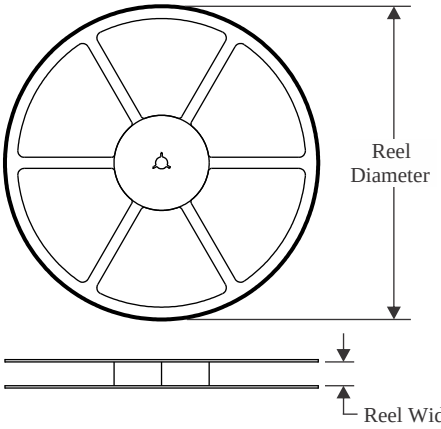
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

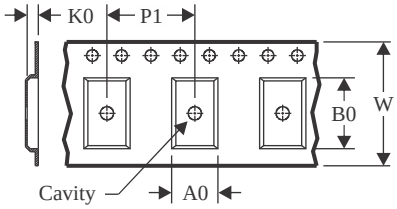
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

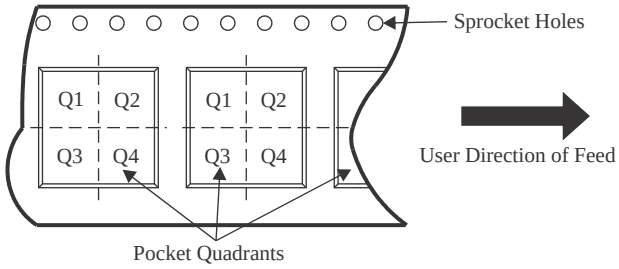



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

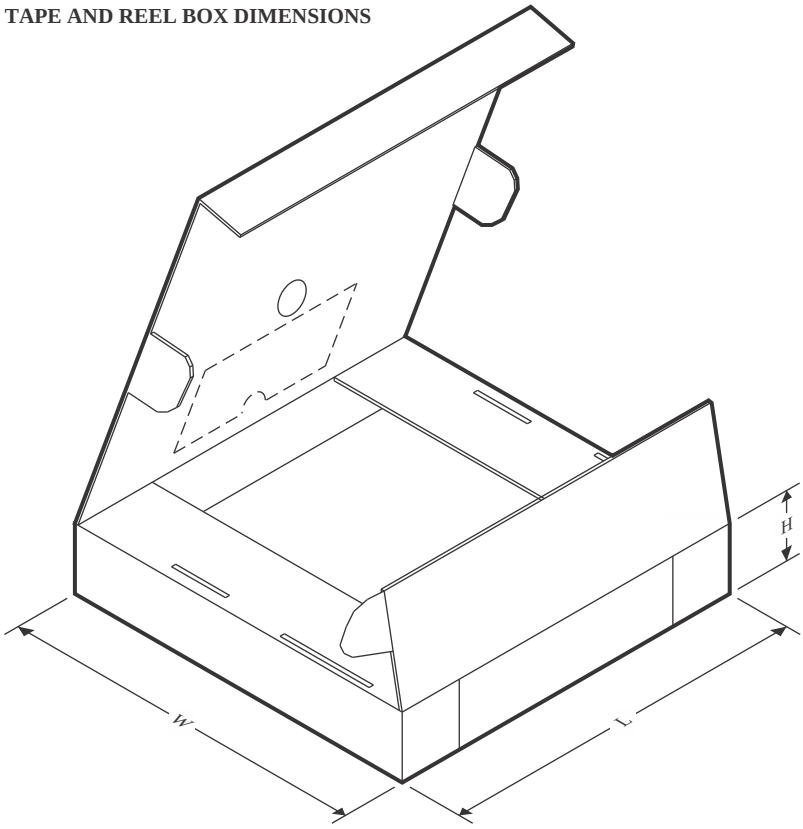
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| LM3103MHX/NOPB | HTSSOP | PWP | 16 | 2500 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |

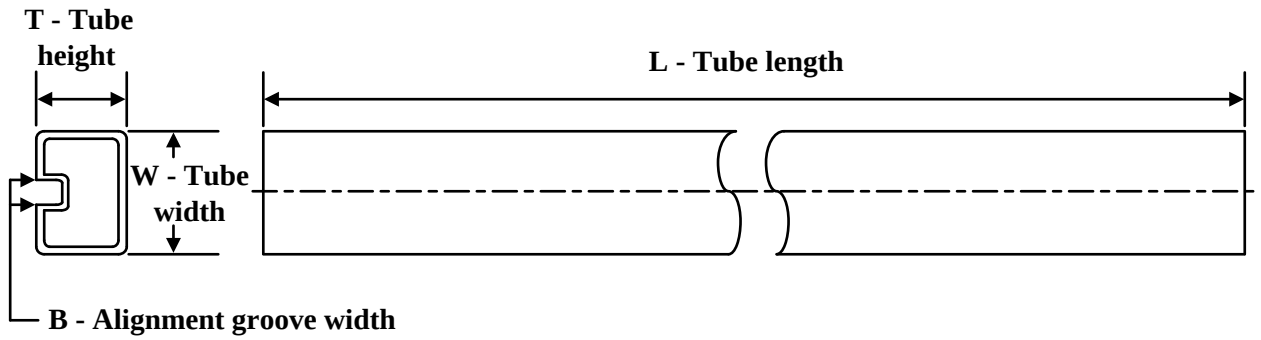
TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

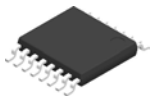
| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| LM3103MHX/NOPB | HTSSOP | PWP | 16 | 2500 | 367.0 | 367.0 | 35.0 |

## TUBE




*All dimensions are nominal

| Device | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (µm) | B (mm) |
|---|---|---|---|---|---|---|---|---|
| LM3103MH/NOPB | PWP | HTSSOP | 16 | 92 | 495 | 8 | 2514.6 | 4.06 |
| LM3103MH/NOPB.A | PWP | HTSSOP | 16 | 92 | 495 | 8 | 2514.6 | 4.06 |
| LM3103MH/NOPB.B | PWP | HTSSOP | 16 | 92 | 495 | 8 | 2514.6 | 4.06 |

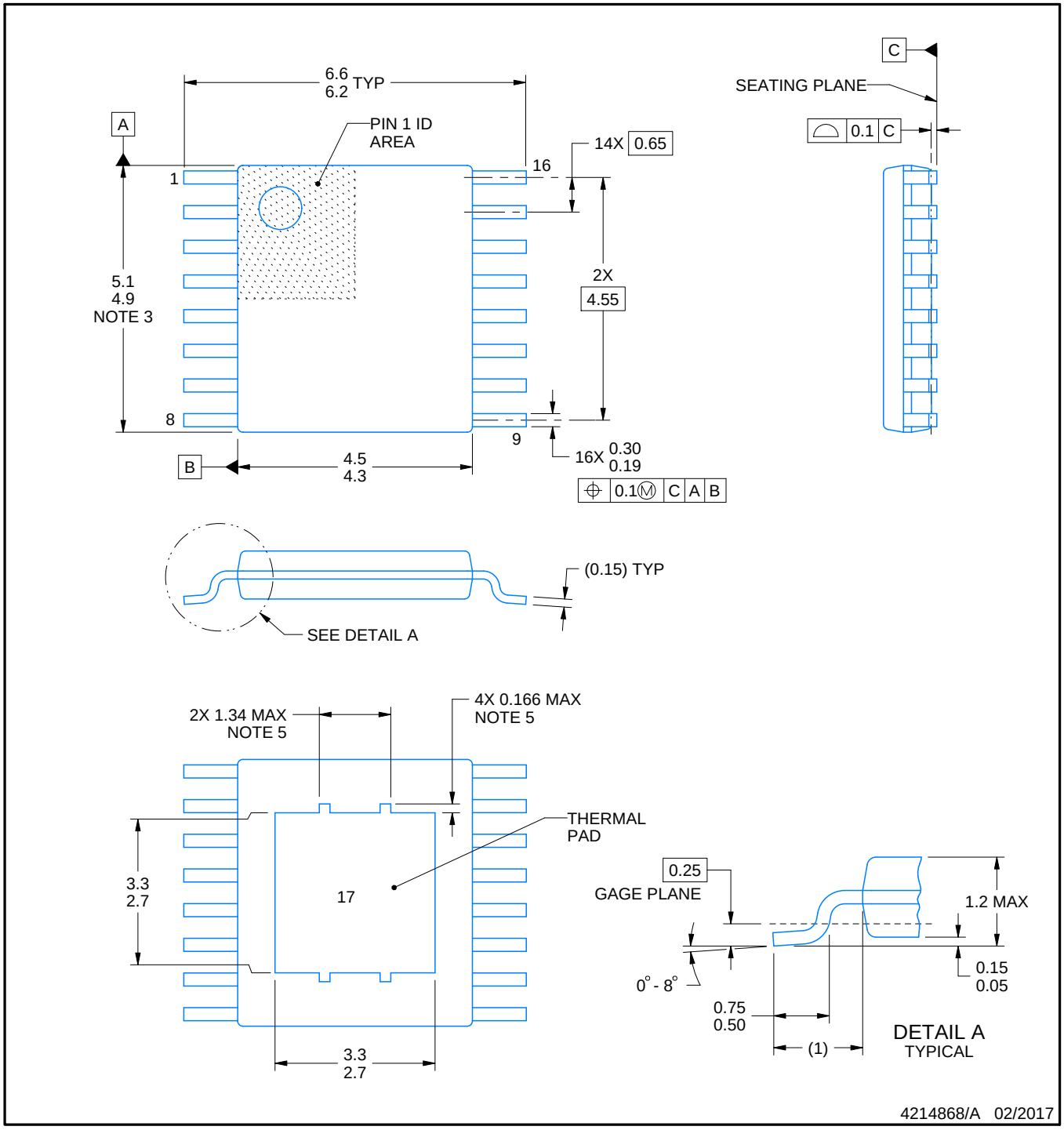


# PACKAGE OUTLINE

## PWP0016A

## PowerPAD ™ HTSSOP - 1.2 mm max height

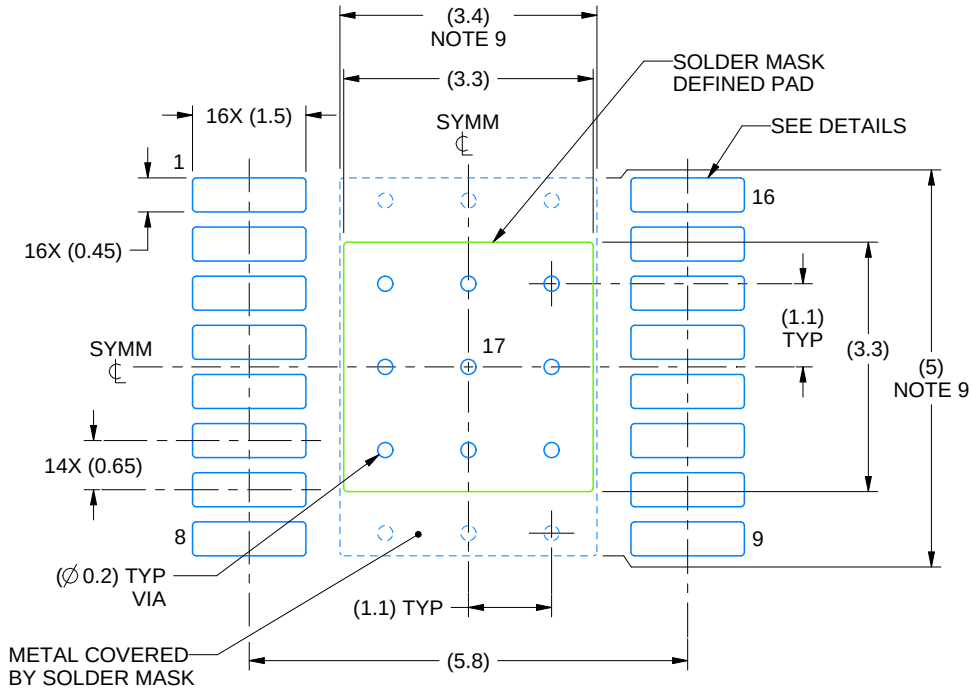
PLASTIC SMALL OUTLINE



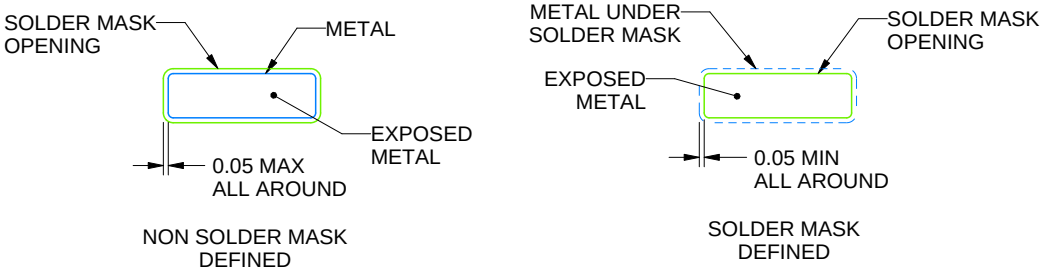

PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.
5. Features may not be present.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:10X

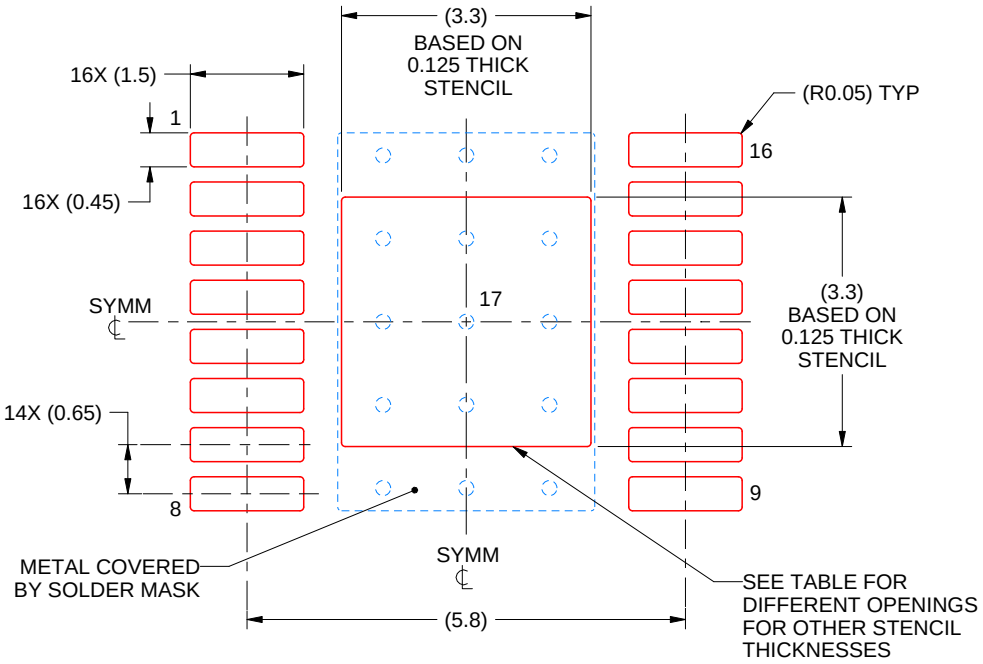



SOLDER MASK DETAILS
PADS 1-16

4214868/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.




SOLDER PASTE EXAMPLE
EXPOSED PAD
100% PRINTED SOLDER COVERAGE BY AREA
SCALE:10X

| STENCIL THICKNESS | SOLDER STENCIL OPENING |
|---|---|
| 0.1 | 3.69 X 3.69 |
| 0.125 | 3.3 X 3.3 (SHOWN) |
| 0.15 | 3.01 X 3.01 |
| 0.175 | 2.79 X 2.79 |

4214868/A 02/2017

NOTES: (continued)

10. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
11. Board assembly site may have different recommendations for stencil design.

# 重要なお知らせと免責事項

TI は、技術データと信頼性データ (データシートを含みます)、設計リソース (リファレンス デザインを含みます)、アプリケーションや設計に関する各種アドバイス、Web ツール、安全性情報、その他のリソースを、欠陥が存在する可能性のある「現状のまま」提供しており、商品性および特定目的に対する適合性の黙示保証、第三者の知的財産権の非侵害保証を含むいかなる保証も、明示的または黙示的にかかわらず拒否します。

これらのリソースは、TI 製品を使用する設計の経験を積んだ開発者への提供を意図したものです。(1) お客様のアプリケーションに適した TI 製品の選定、(2) お客様のアプリケーションの設計、検証、試験、(3) お客様のアプリケーションに該当する各種規格や、その他のあらゆる安全性、セキュリティ、規制、または他の要件への確実な適合に関する責任を、お客様のみが単独で負うものとします。

上記の各種リソースは、予告なく変更される可能性があります。これらのリソースは、リソースで説明されている TI 製品を使用するアプリケーションの開発の目的でのみ、TI はその使用をお客様に許諾します。これらのリソースに関して、他の目的で複製することや掲載することは禁止されています。TI や第三者の知的財産権のライセンスが付与されている訳ではありません。お客様は、これらのリソースを自身で使用した結果発生するあらゆる申し立て、損害、費用、損失、責任について、TI およびその代理人を完全に補償するものとし、TI は一切の責任を拒否します。

TI の製品は、 TI の販売条件 、 TI の総合的な品質ガイドライン 、 ti.com または TI 製品などに関連して提供される他の適用条件に従い提供されます。TI がこれらのリソースを提供することは、適用される TI の保証または他の保証の放棄の拡大や変更を意味するものではありません。 TI がカスタム、またはカスタマー仕様として明示的に指定していない限り、TI の製品は標準的なカタログに掲載される汎用機器です。

お客様がいかなる追加条項または代替条項を提案する場合も、TI はそれらに異議を唱え、拒否します。

Copyright © 2026, Texas Instruments Incorporated

最終更新日：2025 年 10 月