LM324-N-MIL 低消費電力クワッド・オペアンプ

1 特長

- ユニティ・ゲインのため内部的に周波数を補償
- 大きなDC電圧ゲイン: 100dB
- 広い帯域幅(ユニティ・ゲイン): 1MHz (温度補償後)
- 広い電源電圧範囲:
  - 単一電源3V～32V
  - またはデュアル電源±1.5V～±16V
- 非常に低い電源消費電流: 700µA - 本質的に電源電圧の値には無関係
- 低い入力バイアス電流: 45nA (温度補償後)
- 低い入力オフセット電圧: 2mV およびオフセット電流: 5nA
- 入力同相電圧範囲にグランドを含む
- 差動入力電圧範囲は電源電圧に等しい
- 大きな出力電圧スイング: 0V～V^+ – 1.5V
- 利点
  - デュアル電源が不要
  - 4つの内部補償オペアンプを単一のパッケージに搭載
  - 直接GNDレベル近くまでセンシング可能、V_{OUT}もGNDレベルまで遷移可能
  - すべての形式のロジックと互換
  - バッテリ動作に適した消費電力
  - リニア・モードでは、入力同相電圧範囲にグランドおよび出力電圧を含む
  - 単一の電源電圧で動作しながら、グランドまでスイング可能
  - ユニティ・ゲインのクロス周波数を温度補償
  - 入力バイアス電流も温度補償

2 アプリケーション

- トランスデューサ・アンプ
- DCゲイン・ブロック
- 従来型のオペアンプ回路

3 概要

LM324-N-MILデバイスは4つの独立した高ゲインの内部周波数補償付きオペアンプで構成され、単一の電源から、広い電圧範囲で動作するよう設計されています。分割電源からも動作でき、低消費電力で、電源からの消費電流は電源電圧の大きさに依存しません。

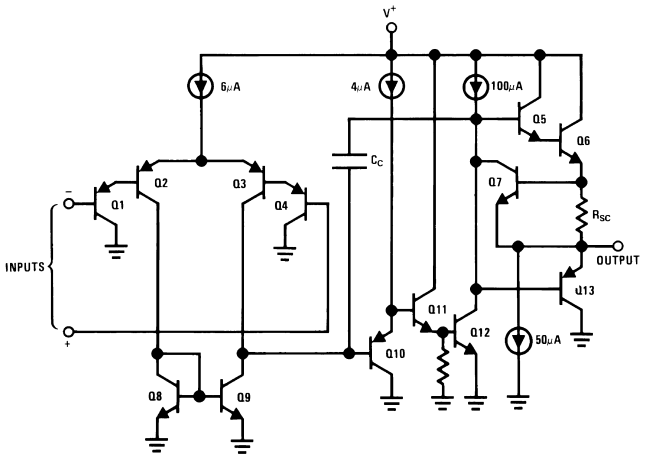
応用分野として、トランスデューサ・アンプ、DCゲイン・ブロック、各種の従来型オペアンプ回路があり、これらを単一の電源システムで、より簡単に実装できます。たとえば、LM324-N-MILデバイスは、デジタル・システムで使用される標準の5V電源電圧で直接動作し、追加の±15V電源の必要なしに、必要なインターフェイス電子回路を簡単に提供できます。

製品情報(1)

型番	パッケージ	本体サイズ(公称)
LM324-N-MIL	CDIP (14)	19.56mm×6.67mm
	PDIP (14)	19.177mm×6.35mm
	SOIC (14)	8.65mm×3.91mm
	TSSOP (14)	5.00mm×4.40mm

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。

回路図



英語版のTI製品についての情報を翻訳したこの資料は、製品の概要を確認する目的で便宜的に提供しているものです。該当する正式な英語版の最新情報は、www.ti.comで閲覧でき、その内容が常に優先されます。TIでは翻訳の正確性および妥当性につきましては一切保証いたしません。実際の設計などの前には、必ず最新版の英語版をご参照くださいますようお願いいたします。

目次

1 特長 ... 1
2 アプリケーション ... 1
3 概要 ... 1
4 改訂履歴 ... 2
5 **Pin Configuration and Functions** ... 3
6 **Specifications** ... 4
6.1 Absolute Maximum Ratings ... 4
6.2 ESD Ratings ... 4
6.3 Recommended Operating Conditions ... 4
6.4 Thermal Information ... 4
6.5 Electrical Characteristics ... 5
6.6 Typical Characteristics ... 6
7 **Detailed Description** ... 8
7.1 Overview ... 8
7.2 Functional Block Diagram ... 8
7.3 Feature Description ... 8
7.4 Device Functional Modes ... 8
8 **Application and Implementation** ... 10
8.1 Application Information ... 10
8.2 Typical Applications ... 10
9 **Power Supply Recommendations** ... 20
10 **Layout** ... 20
10.1 Layout Guidelines ... 20
10.2 Layout Example ... 20
11 デバイスおよびドキュメントのサポート ... 21
11.1 ドキュメントの更新通知を受け取る方法 ... 21
11.2 コミュニティ・リソース ... 21
11.3 商標 ... 21
11.4 静電気放電に関する注意事項 ... 21
11.5 Glossary ... 21
12 メカニカル、パッケージ、および注文情報 ... 21

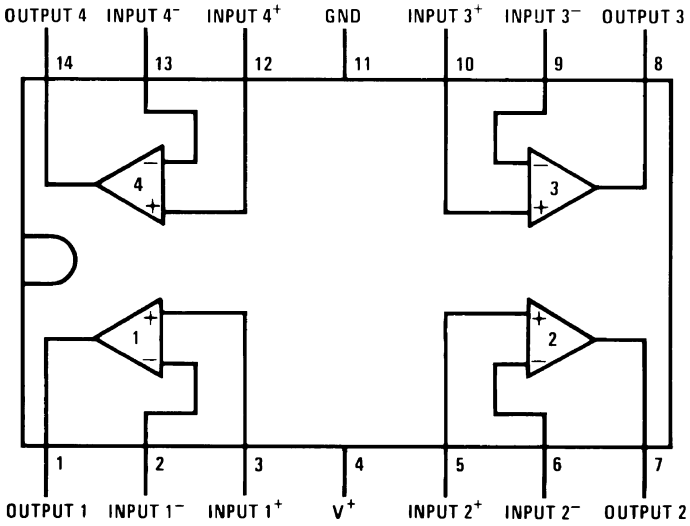
4 改訂履歴

日付	改訂内容	注
2017年6月	*	初版

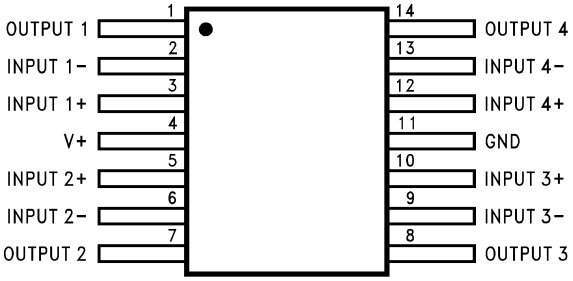
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5 Pin Configuration and Functions

J Package
14-Pin CDIP
Top View



D Package
14-Pin SOIC
Top View



Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
OUTPUT1	1	O	Output, Channel 1
INPUT1-	2	I	Inverting Input, Channel 1
INPUT1+	3	I	Noninverting Input, Channel 1
V+	4	P	Positive Supply Voltage
INPUT2+	5	I	Nonnverting Input, Channel 2
INPUT2-	6	I	Inverting Input, Channel 2
OUTPUT2	7	O	Output, Channel 2
OUTPUT3	8	O	Output, Channel 3
INPUT3-	9	I	Inverting Input, Channel 3
INPUT3+	10	I	Noninverting Input, Channel 3
GND	11	P	Ground or Negative Supply Voltage
INPUT4+	12	I	Noninverting Input, Channel 4
INPUT4-	13	I	Inverting Input, Channel 4
OUTPUT4	14	O	Output, Channel 4

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6 Specifications

6.1 Absolute Maximum Ratings

See (1).

			MIN	MAX	UNIT
Supply Voltage, V^+				32	V
Differential Input Voltage				32	V
Input Voltage			−0.3	32	V
Input Current (V_{IN} < −0.3 V) (2)				50	mA
Power Dissipation (3)	PDIP			1130	mW
	CDIP			1260	mW
	SOIC Package			800	mW
Output Short-Circuit to GND (One Amplifier) (4)		V^+ ≤ 15 V and T_A = 25°C	Continuous		
Soldering Information	Dual-In-Line Package	Soldering (10 seconds)		260	°C
	Small Outline Package	Vapor Phase (60 seconds)		215	°C
		Infrared (15 seconds)		220	°C
Storage temperature, T_{stg}			–65	150	°C

(1) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.
(2) This input current will only exist when the voltage at any of the input leads is driven negative. It is due to the collector-base junction of the input PNP transistors becoming forward biased and thereby acting as input diode clamps. In addition to this diode action, there is also lateral NPN parasitic transistor action on the IC chip. This transistor action can cause the output voltages of the op amps to go to the V^+voltage level (or to ground for a large overdrive) for the time duration that an input is driven negative. This is not destructive and normal output states will re-establish when the input voltage, which was negative, again returns to a value greater than −0.3 V (at 25°C).
(3) For operating at high temperatures, the LM324-N-MIL must be derated based on a 125°C maximum junction temperature and a thermal resistance of 88°C/W which applies for the device soldered in a printed circuit board, operating in a still air ambient. The dissipation is the total of all four amplifiers—use external resistors, where possible, to allow the amplifier to saturate of to reduce the power which is dissipated in the integrated circuit.
(4) Short circuits from the output to V^+ can cause excessive heating and eventual destruction. When considering short circuits to ground, the maximum output current is approximately 40 mA independent of the magnitude of V^+. At values of supply voltage in excess of 15 V, continuous short-circuits can exceed the power dissipation ratings and cause eventual destruction. Destructive dissipation can result from simultaneous shorts on all amplifiers.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±250	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	MAX	UNIT
Supply Voltage (V^+ - V^-)	3	32	V
Operating Input Voltage on Input pins	0	V+	V
Operating junction temperature, T_J	0	70	°C

6.4 Thermal Information

THERMAL METRIC (1)		LM324-N-MIL D/SOIC 14 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	88	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

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6.5 Electrical Characteristics

V^+ = +5.0V, (1), unless otherwise stated

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
Input Offset Voltage		T_A = 25°C (2)			2	7	mV
Input Bias Current (3)		$I_{IN(+)}$ or $I_{IN(-)}$, V_{CM} = 0 V, T_A = 25°C			45	250	nA
Input Offset Current		$I_{IN(+)}$ or $I_{IN(-)}$, V_{CM} = 0 V, T_A = 25°C			5	50	nA
Input Common-Mode Voltage Range (4)		V^+ = 30 V, T_A = 25°C		0		V^+−1.5	V
Supply Current		Over Full Temperature Range R_L = ∞ On All Op Amps, V^+ = 30 V			1.5	3	mA
		V^+ = 5 V			0.7	1.2	
Large Signal Voltage Gain		V^+ = 15V, R_L≥ 2 kΩ, (V_O = 1 V to 11 V), T_A = 25°C		25	100		V/mV
Common-Mode Rejection Ratio		DC, V_{CM} = 0 V to V^+ − 1.5 V, T_A = 25°C		65	85		dB
Power Supply Rejection Ratio		V^+ = 5 V to 30 V, T_A = 25°C		65	100		dB
Amplifier-to-Amplifier Coupling (5)		f = 1 kHz to 20 kHz, T_A = 25°C (Input Referred)			−120		dB
Output Current	Source	V_{IN}^+ = 1 V, V_{IN}^- = 0 V, V^+ = 15 V, V_O = 2 V, T_A = 25°C		20	40		mA
	Sink	V_{IN}^- = 1 V, V_{IN}^+ = 0 V, V^+ = 15 V, V_O = 2 V, T_A = 25°C		10	20		mA
		V_{IN}^- = 1 V, V_{IN}^+ = 0 V, V^+ = 15 V, V_O = 200 mV, T_A = 25°C		12	50		µA
Short Circuit to Ground		V^+ = 15 V, T_A = 25°C (6)			40	60	mA
Input Offset Voltage		See (2)				9	mV
V_{OS} Drift		R_S = 0 Ω			7		µV/°C
Input Offset Current		$I_{IN(+)}$ − $I_{IN(-)}$, V_{CM} = 0 V				150	nA
I_{OS} Drift		R_S = 0 Ω			10		pA/°C
Input Bias Current		$I_{IN(+)}$ or $I_{IN(-)}$			40	500	nA
Input Common-Mode Voltage Range (4)		V^+ = 30 V		0		V^+−2	V
Large Signal Voltage Gain		V^+ = 15 V (V_OSwing = 1V to 11V), R_L ≥ 2 kΩ		15			V/mV
Output Voltage Swing	V_{OH}	V^+ = 30 V	R_L = 2 kΩ	26			V
			R_L = 10 kΩ	27	28		
	V_{OL}	V^+ = 5 V, R_L = 10 kΩ			5	20	mV
Output Current	Source	V_O = 2 V	V_{IN}^+ = 1 V, V_{IN}^- = 0 V, V^+ = 15 V	10	20		mA
	Sink		V_{IN}^- = 1 V, V_{IN}^+ = 0 V, V^+ = 15 V	5	8		mA

(1) The LM324-N-MIL temperature specifications are limited to 0°C ≤ T_A ≤ +70°C.
(2) V_O ≅ 1.4V, R_S = 0 Ω with V^+ from 5 V to 30 V.
(3) The direction of the input current is out of the IC due to the PNP input stage. This current is essentially constant, independent of the state of the output so no loading change exists on the input lines.
(4) The input common-mode voltage of either input signal voltage should not be allowed to go negative by more than 0.3 V (at 25°C). The upper end of the common-mode voltage range is V^+ − 1.5 V (at 25°C), but either or both inputs can go to 32 V without damage, independent of the magnitude of V^+.
(5) Due to proximity of external components, insure that coupling is not originating via stray capacitance between these external parts. This typically can be detected as this type of capacitance increases at higher frequencies.
(6) Short circuits from the output to V^+ can cause excessive heating and eventual destruction. When considering short circuits to ground, the maximum output current is approximately 40 mA independent of the magnitude of V^+. At values of supply voltage in excess of 15 V, continuous short-circuits can exceed the power dissipation ratings and cause eventual destruction. Destructive dissipation can result from simultaneous shorts on all amplifiers.

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6.6 Typical Characteristics

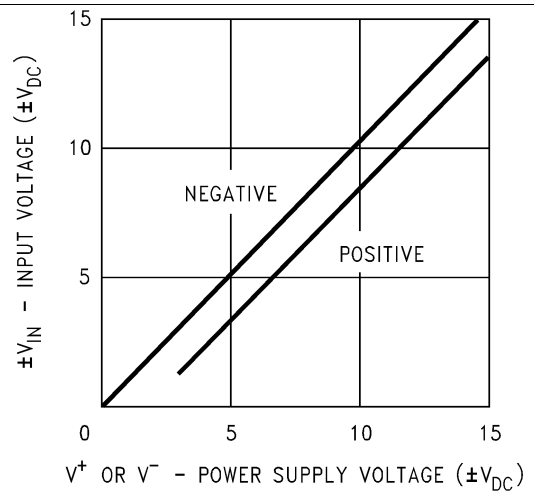


Figure 1. Input Voltage Range

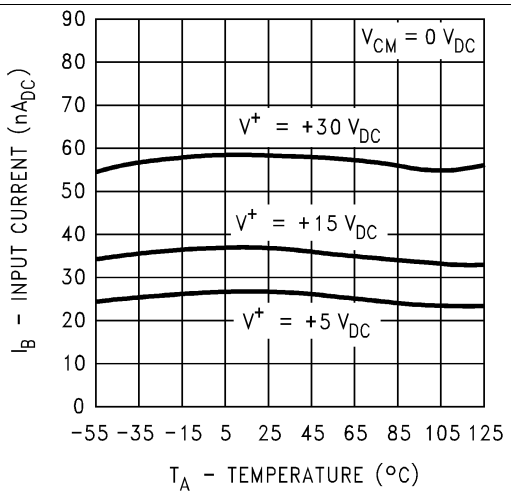


Figure 2. Input Current

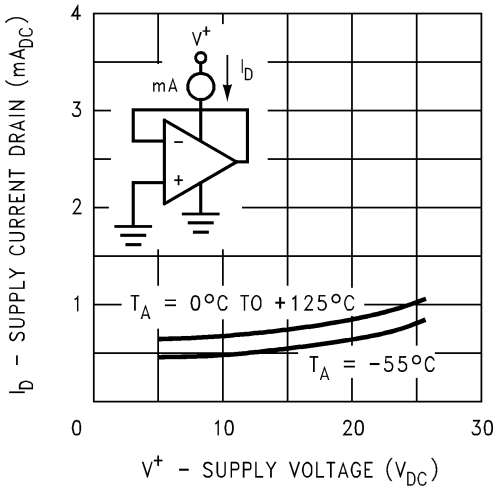


Figure 3. Supply Current

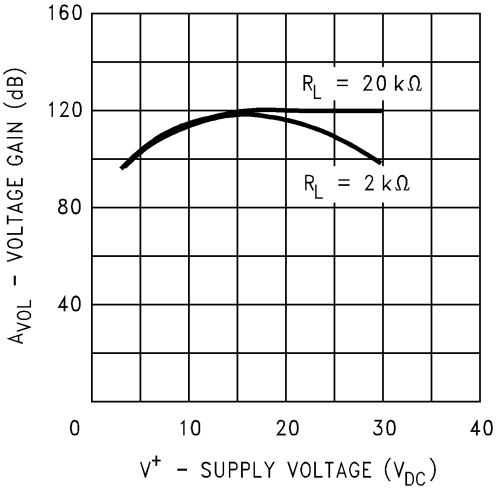


Figure 4. Voltage Gain

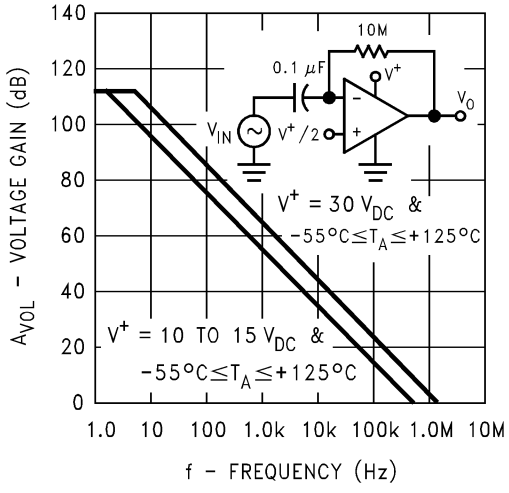


Figure 5. Open-Loop Frequency Response

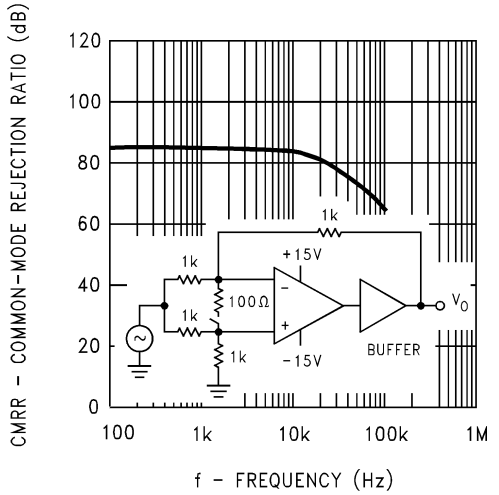


Figure 6. Common Mode Rejection Ratio

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Typical Characteristics (continued)

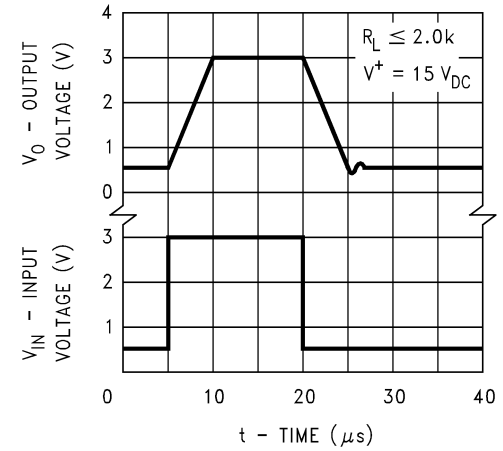


Figure 7. Voltage Follower Pulse Response

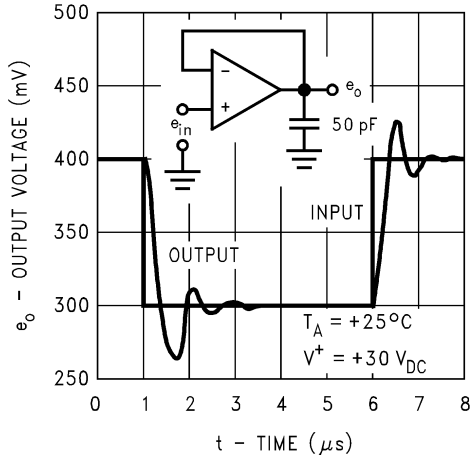


Figure 8. Voltage Follower Pulse Response (Small Signal)

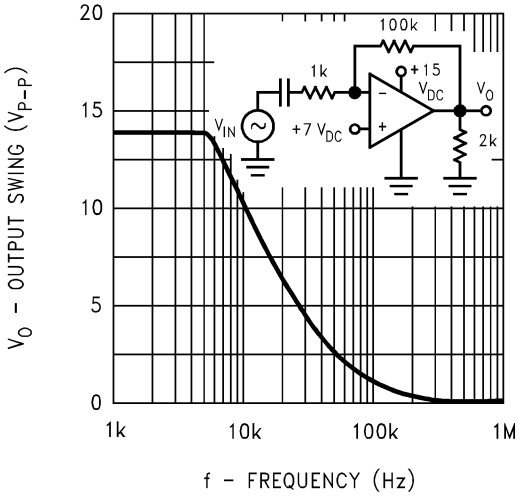


Figure 9. Large Signal Frequency Response

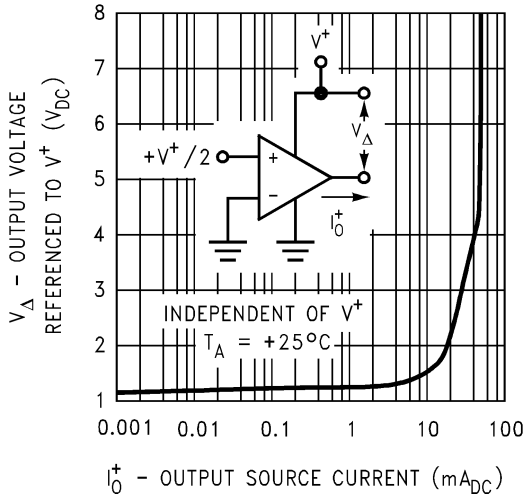


Figure 10. Output Characteristics Current Sourcing

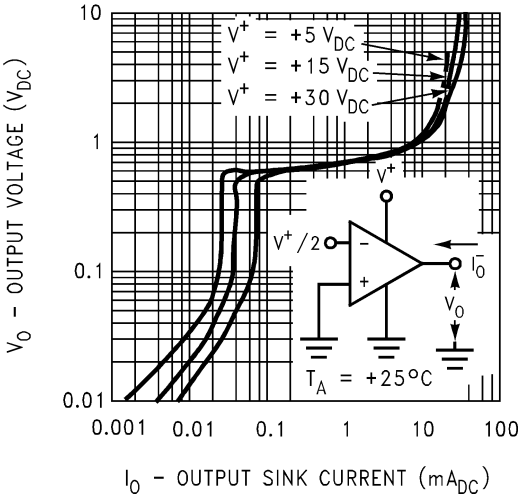


Figure 11. Output Characteristics Current Sinking

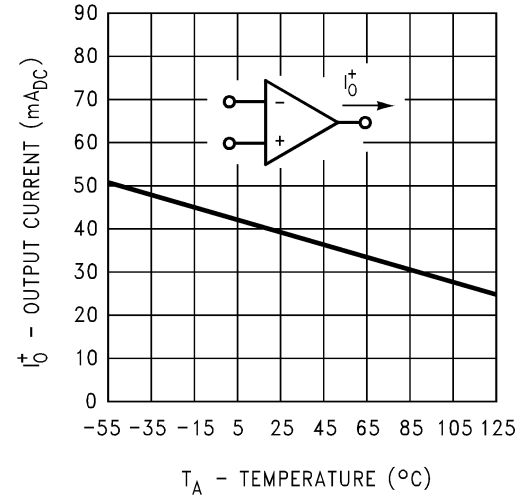


Figure 12. Current Limiting

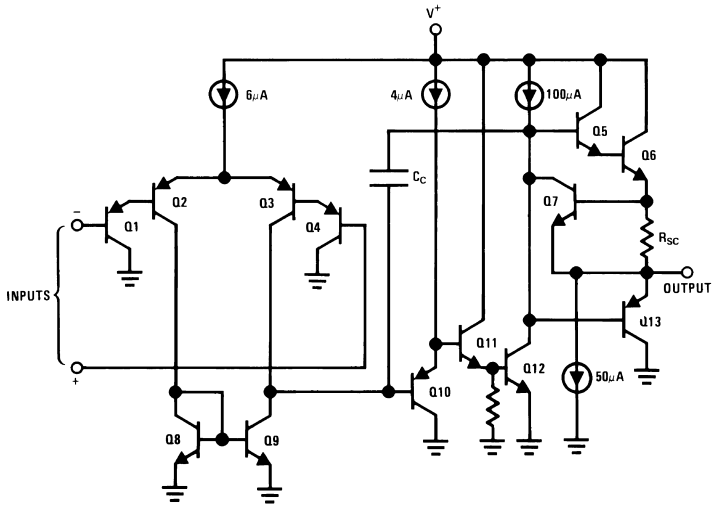
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7 Detailed Description

7.1 Overview

The LM324-N-MIL device is an op amp which operates with only a single power supply voltage, has true-differential inputs, and remains in the linear mode with an input common-mode voltage of 0 V_{DC}. This amplifier operates over a wide range of power supply voltage with little change in performance characteristics. At 25°C amplifier operation is possible down to a minimum supply voltage of 2.3 V_{DC}.

7.2 Functional Block Diagram



7.3 Feature Description

The LM324-N-MIL provides a compelling balance of performance versus current consumption. The 700 μA of supply current draw over the wide operating conditions with a 1-MHz gain-bandwidth and temperature compensated bias currents makes the LM324-N-MIL an effective solution for large variety of applications. The input offset voltage of 2 mV and offset current of 5 nA, along with the 45n-A bias current across a wide supply voltage means a single design can be used in a large number of different implementations.

7.4 Device Functional Modes

Large differential input voltages can be easily accommodated and, as input differential voltage protection diodes are not needed, no large input currents result from large differential input voltages. The differential input voltage may be larger than V^+ without damaging the device. Protection should be provided to prevent the input voltages from going negative more than −0.3 V_{DC} (at 25°C). An input clamp diode with a resistor to the IC input terminal can be used.

To reduce the power supply drain, the amplifiers have a class A output stage for small signal levels which converts to class B in a large signal mode. This allows the amplifiers to both source and sink large output currents. Therefore both NPN and PNP external current boost transistors can be used to extend the power capability of the basic amplifiers. The output voltage needs to raise approximately 1 diode drop above ground to bias the on-chip vertical PNP transistor for output current sinking applications.

For ac applications, where the load is capacitively coupled to the output of the amplifier, a resistor should be used, from the output of the amplifier to ground to increase the class A bias current and prevent crossover distortion.

Where the load is directly coupled, as in dc applications, there is no crossover distortion.

Capacitive loads which are applied directly to the output of the amplifier reduce the loop stability margin. Values of 50 pF can be accommodated using the worst-case non-inverting unity gain connection. Large closed loop gains or resistive isolation should be used if larger load capacitance must be driven by the amplifier.

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Device Functional Modes (continued)

The bias network of the LM324-N-MIL establishes a drain current which is independent of the magnitude of the power supply voltage over the range of from 3 V_{DC} to 30 V_{DC}.

Output short circuits either to ground or to the positive power supply should be of short time duration. Units can be destroyed, not as a result of the short circuit current causing metal fusing, but rather due to the large increase in IC chip dissipation which will cause eventual failure due to excessive junction temperatures. Putting direct short-circuits on more than one amplifier at a time will increase the total IC power dissipation to destructive levels, if not properly protected with external dissipation limiting resistors in series with the output leads of the amplifiers. The larger value of output source current which is available at 25°C provides a larger output current capability at elevated temperatures (see *Typical Characteristics*) than a standard IC op amp.

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8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

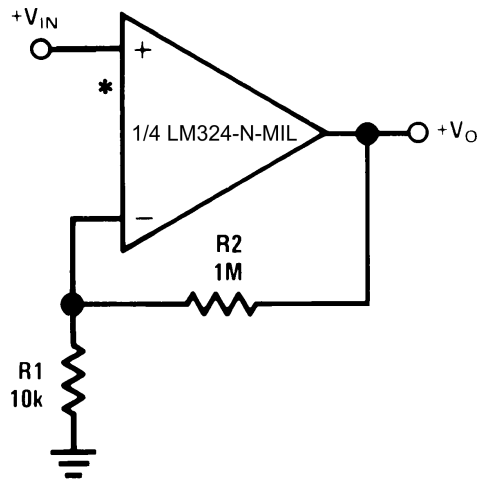
8.1 Application Information

The LM324-N-MIL amplifier is specified for operation from 3 V to 32 V (±1.5 V to ±16 V). Many of the specifications apply from –40°C to 125°C. Parameters that can exhibit significant variance with regards to operating voltage or temperature are presented in *Typical Characteristics*.

8.2 Typical Applications

Figure 13 emphasizes operation on only a single power supply voltage. If complementary power supplies are available, all of the standard op amp circuits can be used. In general, introducing a pseudo-ground (a bias voltage reference of $V^+/2$) will allow operation above and below this value in single power supply systems. Many application circuits are shown which take advantage of the wide input common-mode voltage range which includes ground. In most cases, input biasing is not required and input voltages which range to ground can easily be accommodated.

8.2.1 Non-Inverting DC Gain (0 V Input = 0 V Output)



*R not needed due to temperature independent I_{IN}

Figure 13. Non-Inverting Amplifier with G = 100

8.2.1.1 Design Requirements

For this example application, the required signal gain is a non-inverting 100x±5% with a supply voltage of 5 V.

8.2.1.2 Detailed Design Procedure

Using the equation for a non-inverting gain configuration, Av = 1+R2/R1. Setting the R1 to 10 kΩ, R2 is 99 times larger than R1, which is 990 kΩ. A 1MΩ is more readily available, and provides a gain of 101, which is within the desired specification.

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Typical Applications (continued)

The gain-frequency characteristic of the amplifier and its feedback network must be such that oscillation does not occur. To meet this condition, the phase shift through amplifier and feedback network must never exceed 180° for any frequency where the gain of the amplifier and its feedback network is greater than unity. In practical applications, the phase shift should not approach 180° since this is the situation of conditional stability. Obviously the most critical case occurs when the attenuation of the feedback network is zero.

8.2.1.3 Application Curve

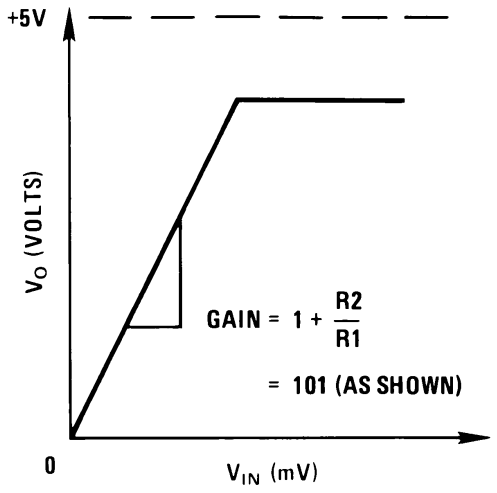
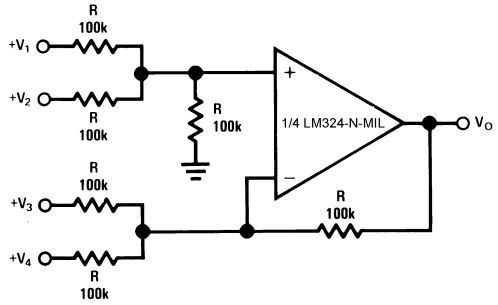


Figure 14. Non-Inverting Amplified Response Curve

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Typical Applications (continued)

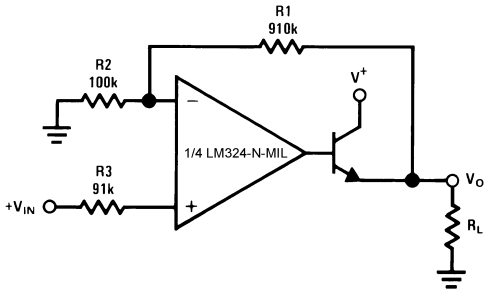
8.2.2 Other Application Circuits at $V^+ = 5.0\ V_{DC}$



Where: $V_0 = V_1 + V_2 - V_3 - V_4$

$(V_1 + V_2) \geq (V_3 + V_4)$ to keep $V_O > 0\ V_{DC}$

Figure 15. DC Summing Amplifier ($V_{IN'S} \geq 0\ V_{DC}$ And $V_O \geq V_{DC}$)



Where: $V_0 = 0\ V_{DC}$ for $V_{IN} = 0\ V_{DC}$

$A_V = 10$

Figure 16. Power Amplifier

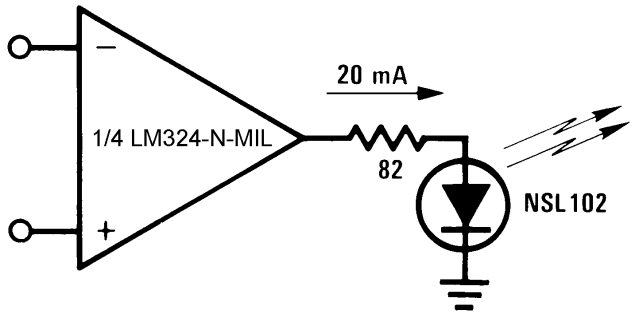
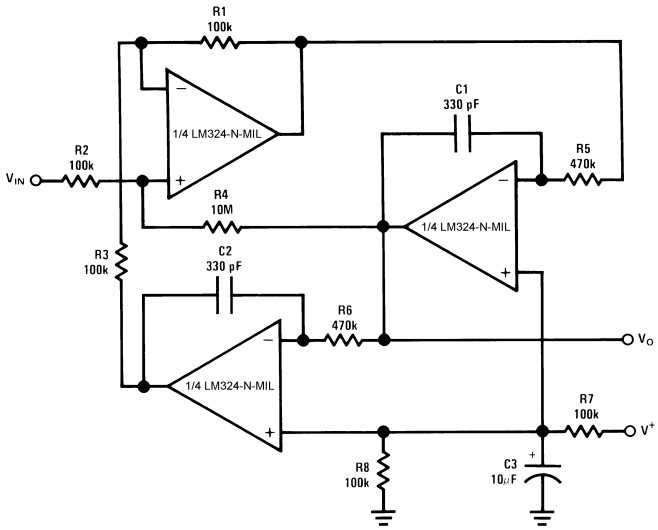


Figure 17. LED Driver

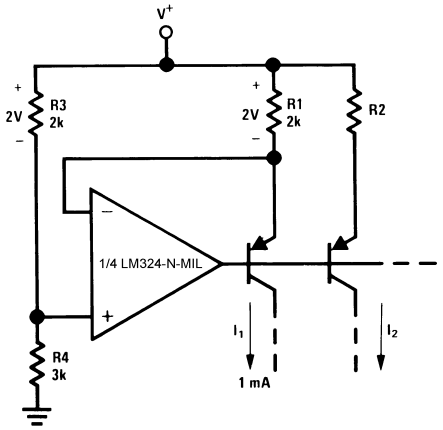


$f_0 = 1$ kHz Q = 50 $A_V = 100$ (40 dB)

Figure 18. "BI-QUAD" RC Active Bandpass Filter

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Typical Applications (continued)



$$I_2 = \left(\frac{R1}{R2}\right) I_1$$

Figure 19. Fixed Current Sources

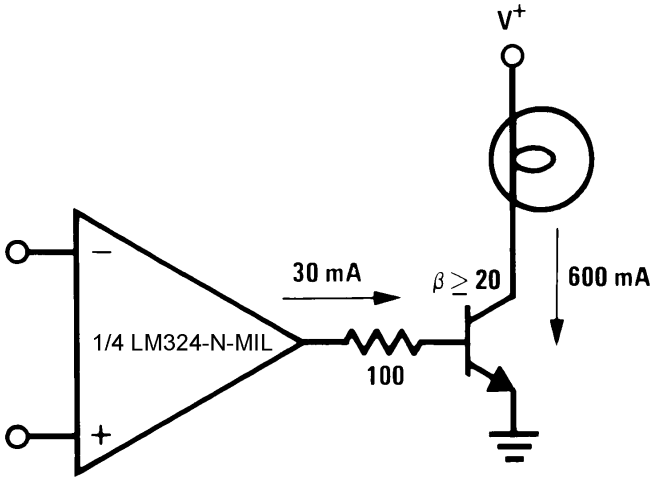
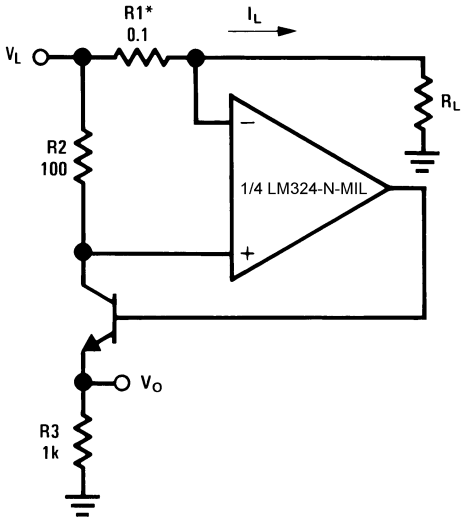


Figure 20. Lamp Driver



*(Increase R1 for I_L small)

Figure 21. Current Monitor

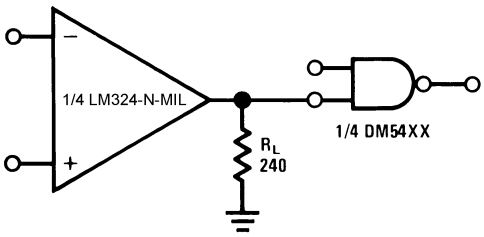


Figure 22. Driving TTL

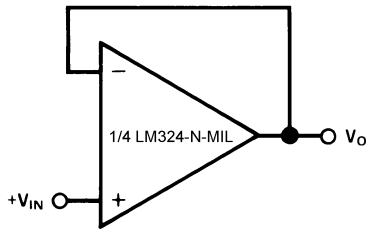


Figure 23. Voltage Follower

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Typical Applications (continued)

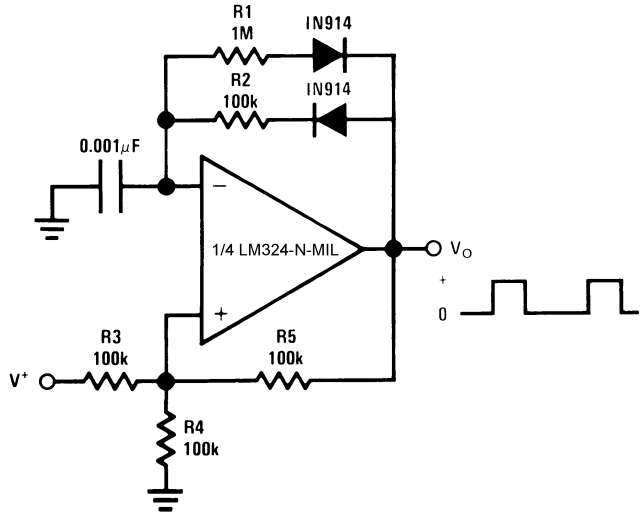


Figure 24. Pulse Generator

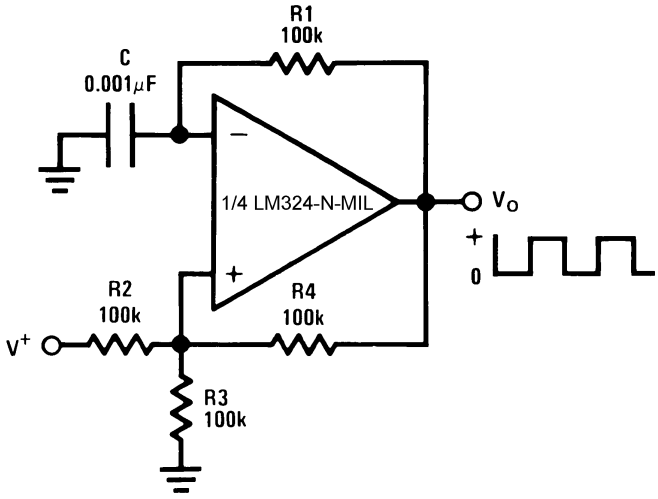


Figure 25. Squarewave Oscillator

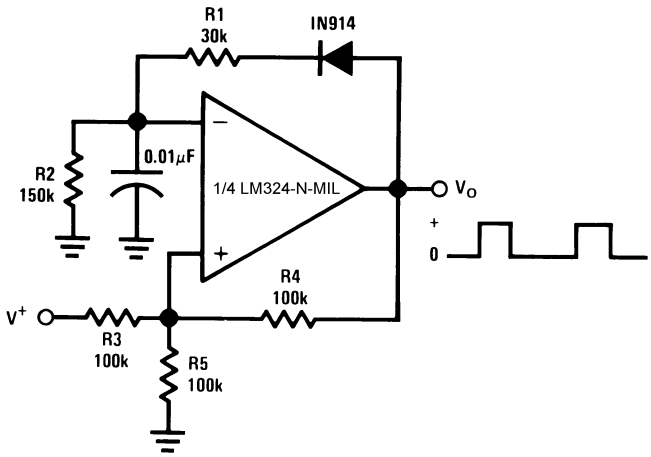
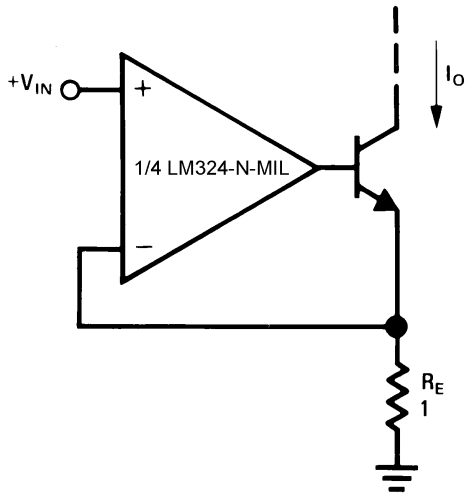


Figure 26. Pulse Generator



I_O = 1 amp/volt V_{IN} (Increase R_E for I_o small)

Figure 27. High Compliance Current Sink

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Typical Applications (continued)

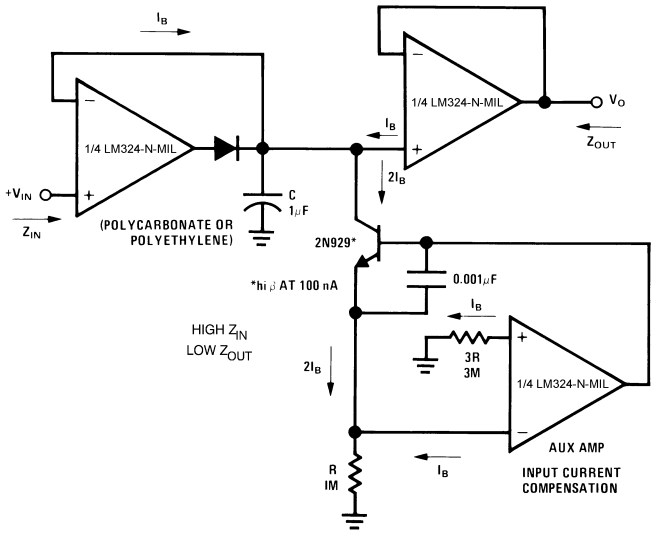


Figure 28. Low Drift Peak Detector

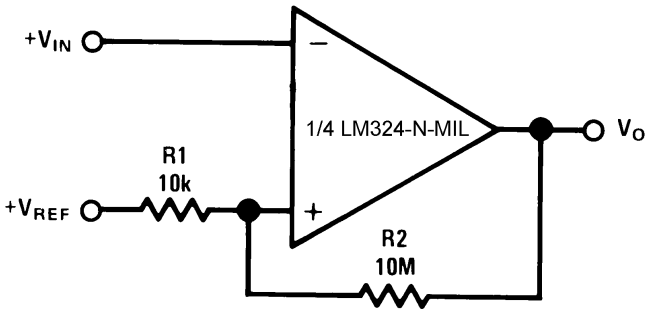
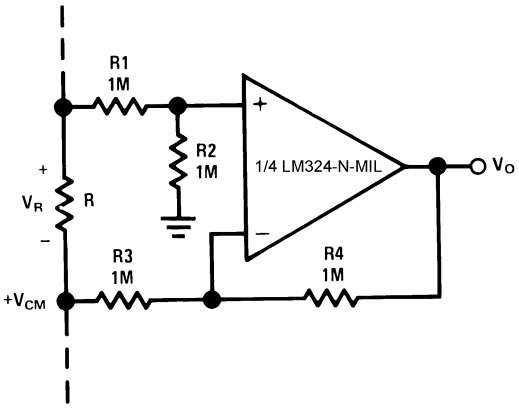
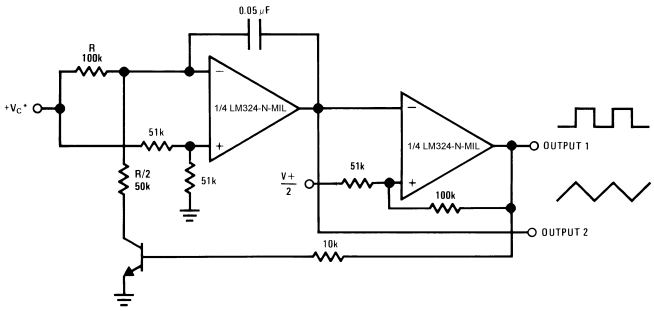


Figure 29. Comparator With Hysteresis



$V_O = V_R$

Figure 30. Ground Referencing a Differential Input Signal



*Wide control voltage range:
$0\ V_{DC} \le V_C \le 2\ (V^+ - 1.5\ V_{DC})$

Figure 31. Voltage Controlled Oscillator Circuit

Typical Applications (continued)

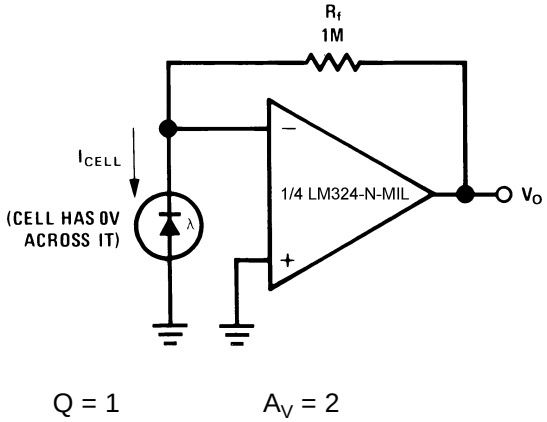


Figure 32. Photo Voltaic-Cell Amplifier

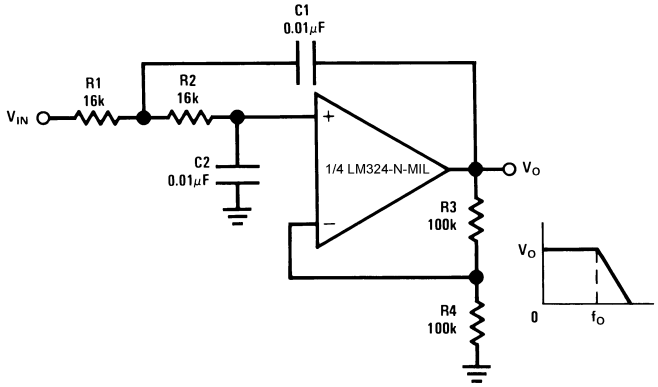
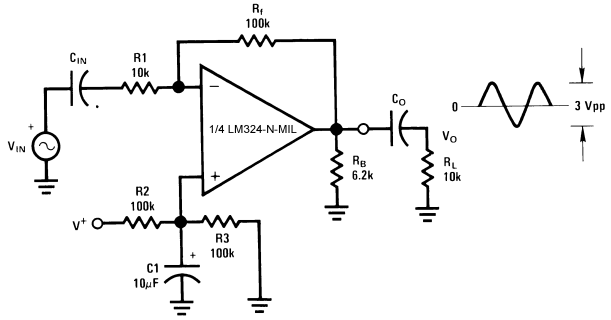
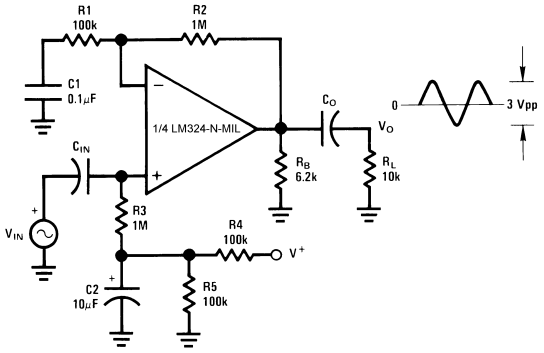


Figure 33. DC Coupled Low-Pass RC Active Filter



$$A_V = \frac{R_f}{R1} \text{ (As shown, } A_V = 10)$$

Figure 34. AC Coupled Inverting Amplifier



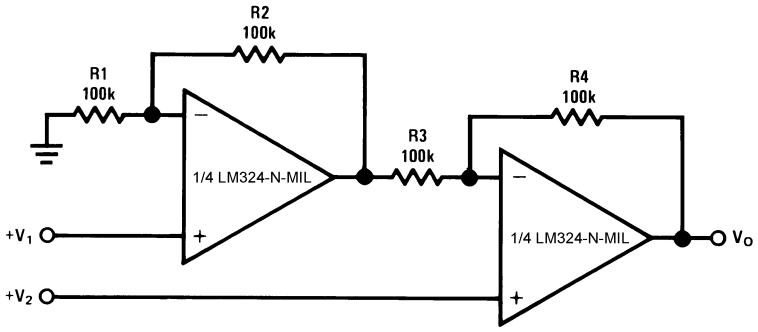
$$A_V = 1 + \frac{R2}{R1}$$

A_V = 11 (As shown)

Figure 35. AC Coupled Non-Inverting Amplifier

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Typical Applications (continued)

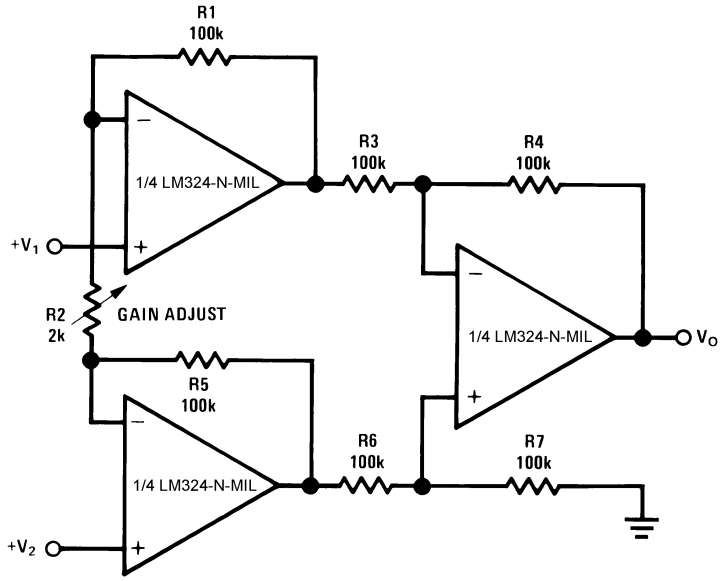


For $\frac{R1}{R2} = \frac{R4}{R3}$ (CMRR depends on this resistor ratio match)

$V_O = 1 + \frac{R4}{R3}(V_2 - V_1)$

As shown: $V_O = 2(V_2 - V_1)$

Figure 36. High Input Z, DC Differential Amplifier



If R1 = R5 & R3 = R4 = R6 = R7 (CMRR depends on match)

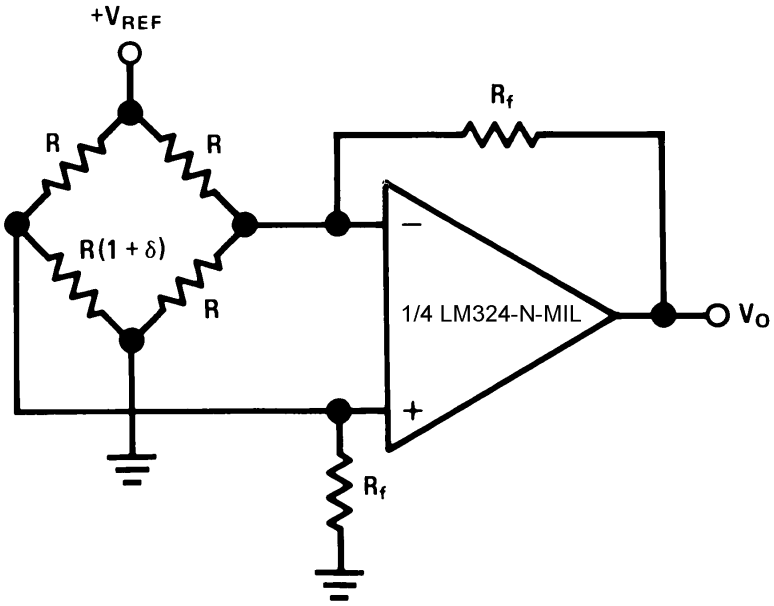
$V_O = 1 + \frac{2R1}{R2}(V_2 - V_1)$

As shown $V_O = 101\,(V_2 - V_1)$

Figure 37. High Input Z Adjustable-Gain DC Instrumentation Amplifier

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Typical Applications (continued)



For $\delta << 1$ and $R_f >> R$

$$V_O \cong V_{REF} \left(\frac{\delta}{2}\right) \frac{R_f}{R}$$

Figure 38. Bridge Current Amplifier

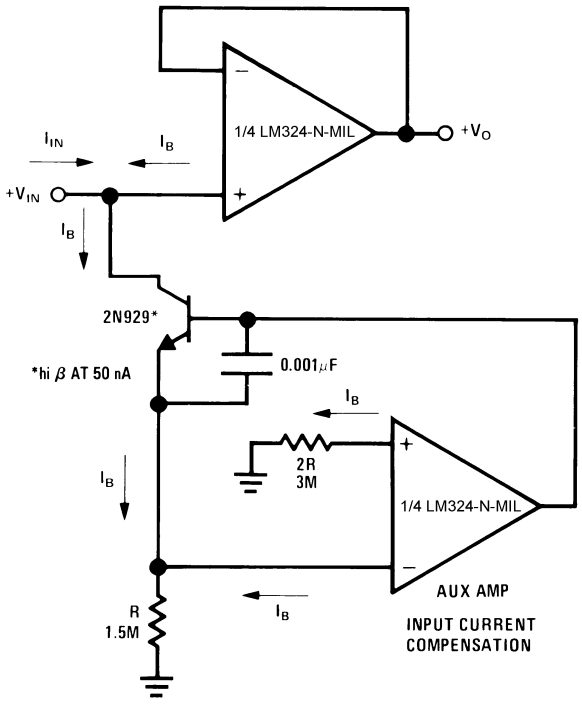
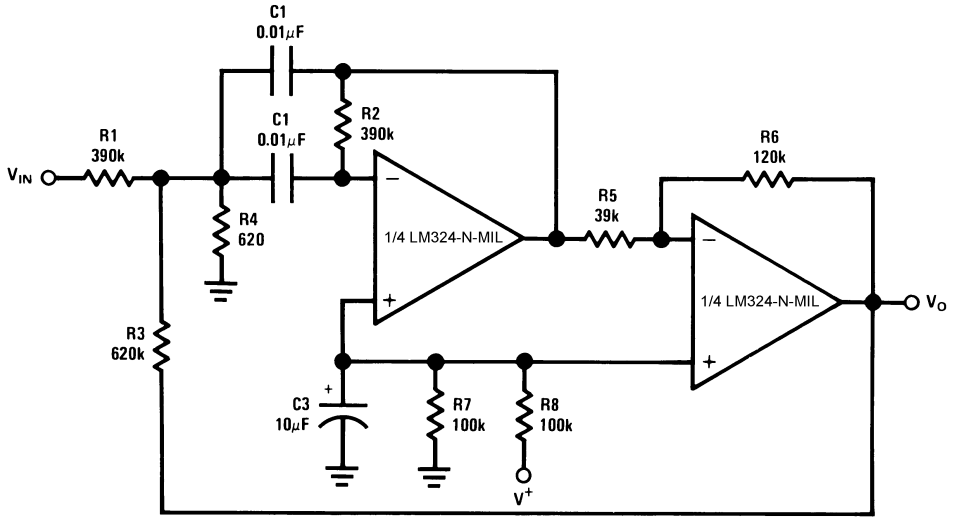


Figure 39. Using Symmetrical Amplifiers to Reduce Input Current (General Concept)

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Typical Applications (continued)



f_O = 1 kHz Q = 25

Figure 40. Bandpass Active Filter

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9 Power Supply Recommendations

The pinouts of the package have been designed to simplify PC board layouts. Inverting inputs are adjacent to outputs for all of the amplifiers and the outputs have also been placed at the corners of the package (pins 1, 7, 8, and 14).

Precautions should be taken to insure that the power supply for the integrated circuit never becomes reversed in polarity or that the unit is not inadvertently installed backwards in a test socket as an unlimited current surge through the resulting forward diode within the IC could cause fusing of the internal conductors and result in a destroyed unit.

10 Layout

10.1 Layout Guidelines

The V + pin should be bypassed to ground with a low-ESR capacitor. The optimum placement is closest to the V + and ground pins.

Take care to minimize the loop area formed by the bypass capacitor connection between V + and ground.

The ground pin should be connected to the PCB ground plane at the pin of the device.

The feedback components should be placed as close to the device as possible minimizing strays.

10.2 Layout Example

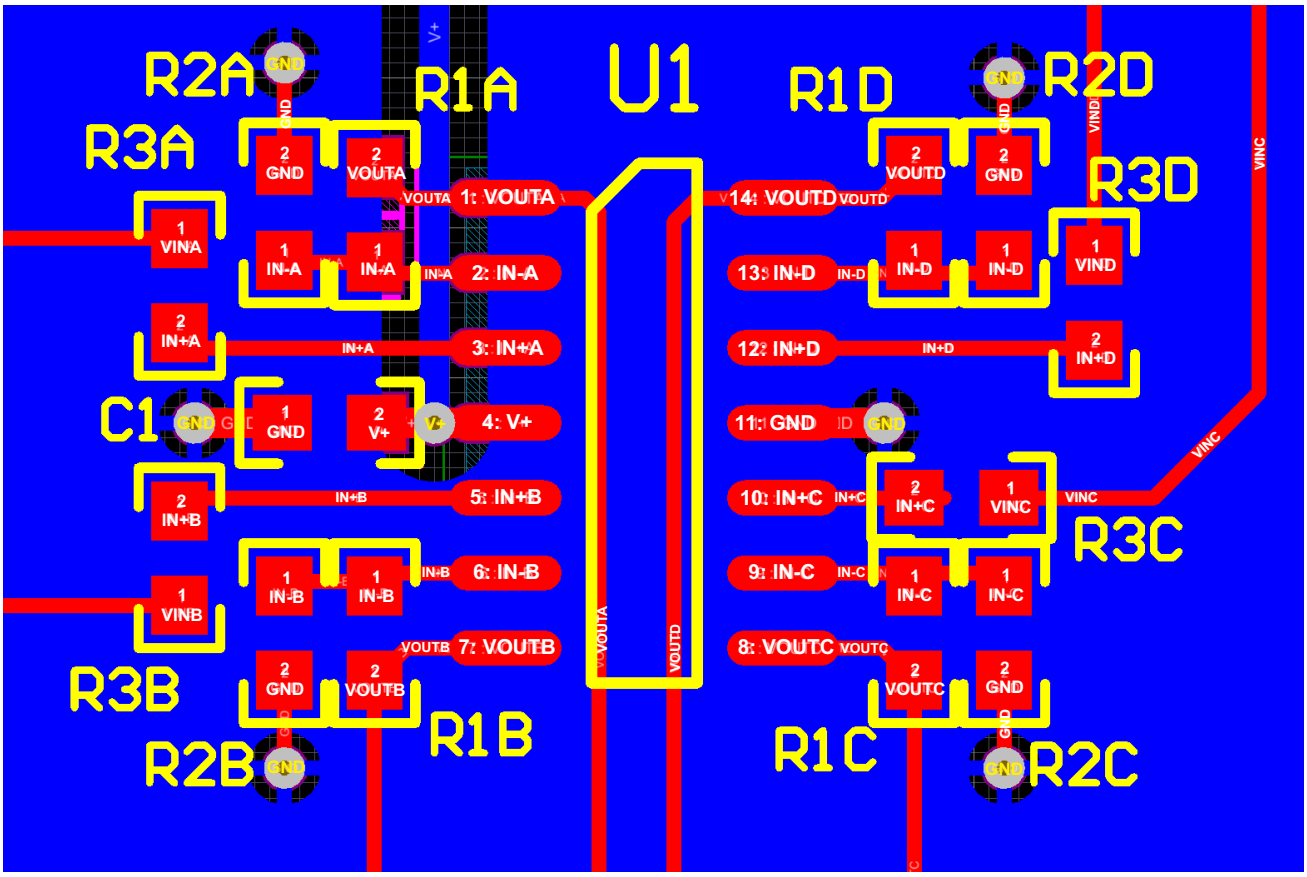


Figure 41. Layout Example

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11 デバイスおよびドキュメントのサポート

11.1 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、ti.comのデバイス製品フォルダを開いてください。右上の隅にある「*通知を受け取る*」をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

11.2 コミュニティ・リソース

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静電気放電はわずかな性能の低下から完全なデバイスの故障に至るまで、様々な損傷を与えます。高精度の集積回路は、損傷に対して敏感であり、極めてわずかなパラメータの変化により、デバイスに規定された仕様に適合しなくなる場合があります。

11.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。この情報は、そのデバイスについて利用可能な最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LM324J	Active	Production	CDIP (J) | 14	25 | TUBE	No	SNPB	Level-1-NA-UNLIM	0 to 70	LM324J

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

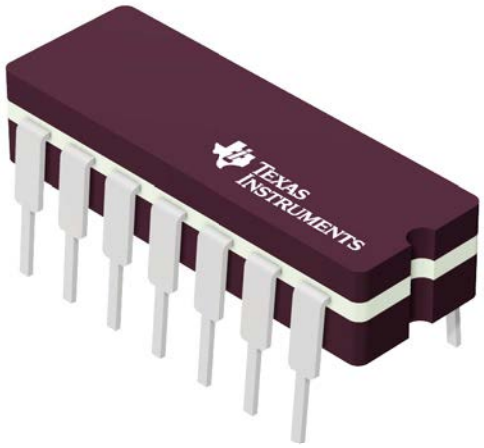
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GENERIC PACKAGE VIEW

J 14 CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4040083-5/G

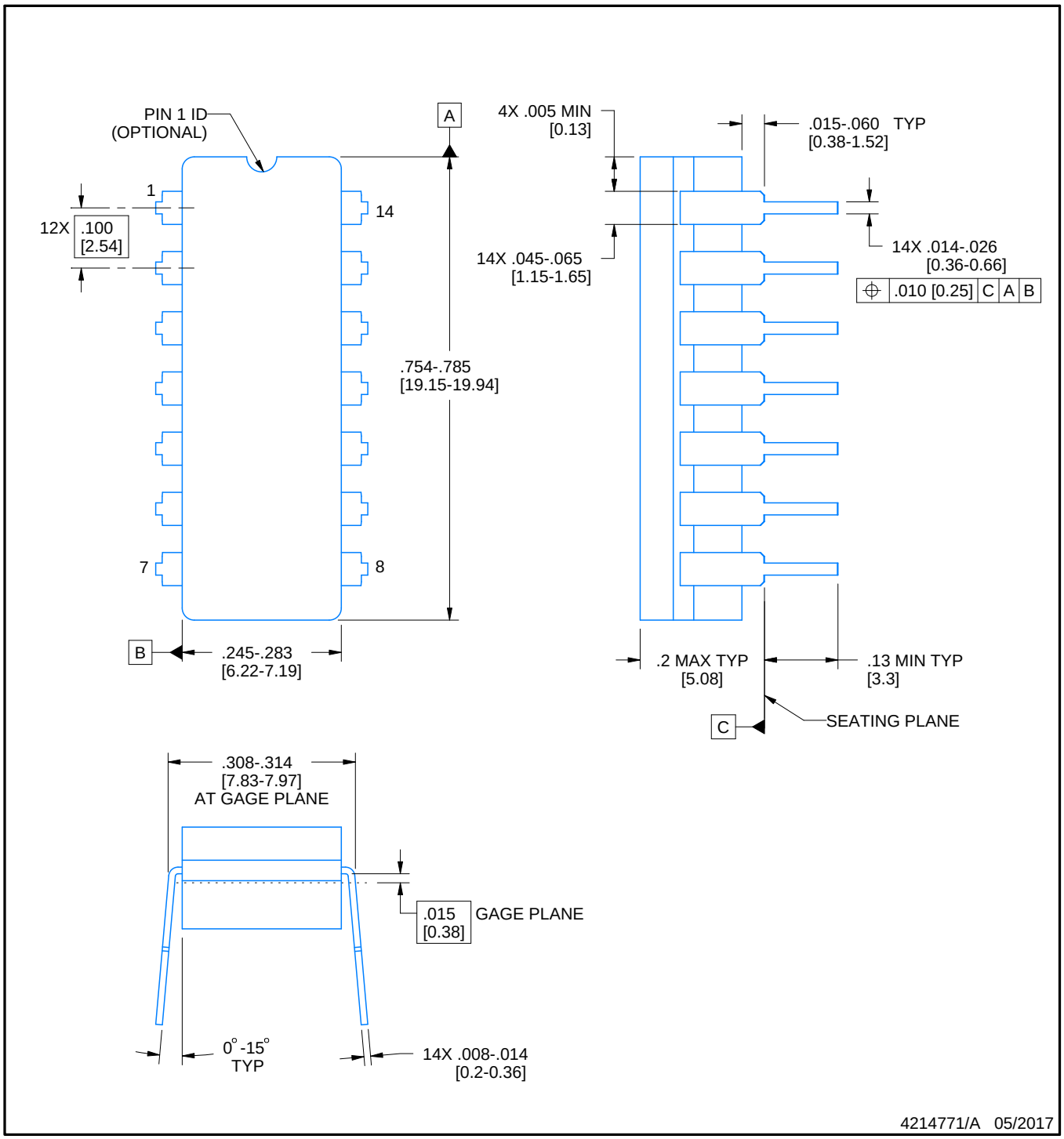


PACKAGE OUTLINE

J0014A

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



NOTES:

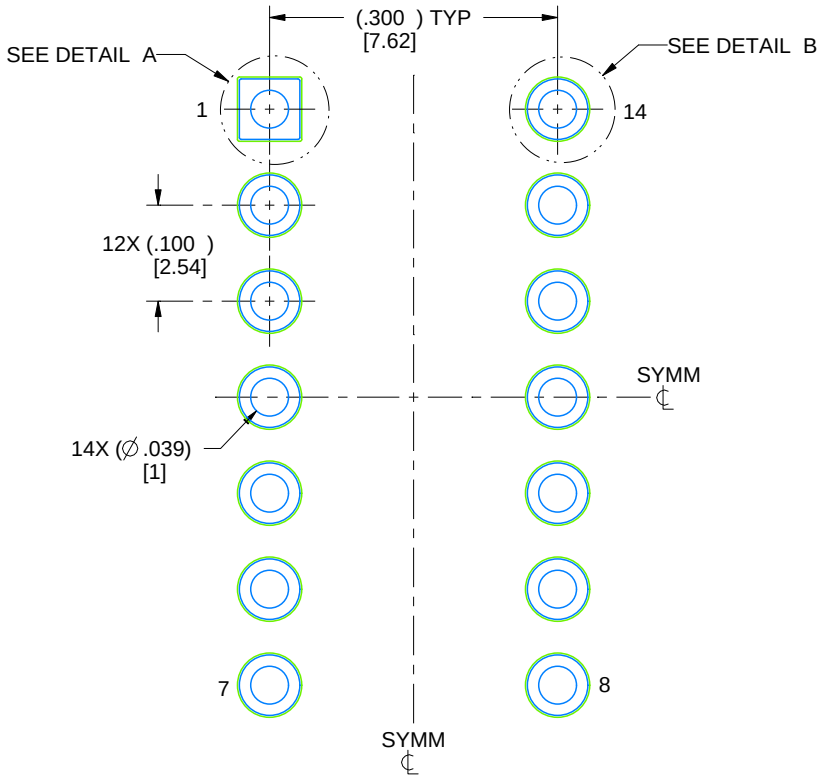
1. All controlling linear dimensions are in inches. Dimensions in brackets are in millimeters. Any dimension in brackets or parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package is hermitically sealed with a ceramic lid using glass frit.
4. Index point is provided on cap for terminal identification only and on press ceramic glass frit seal only.
5. Falls within MIL-STD-1835 and GDIP1-T14.

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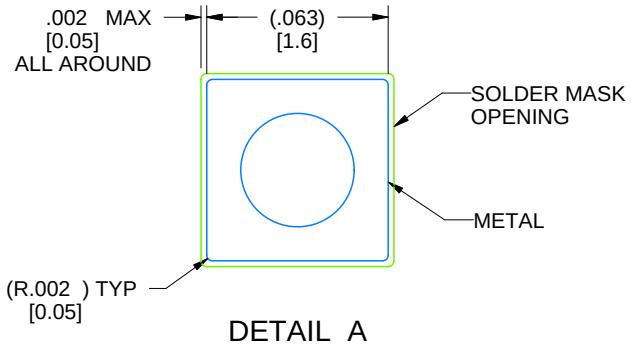
J0014A

CDIP - 5.08 mm max height

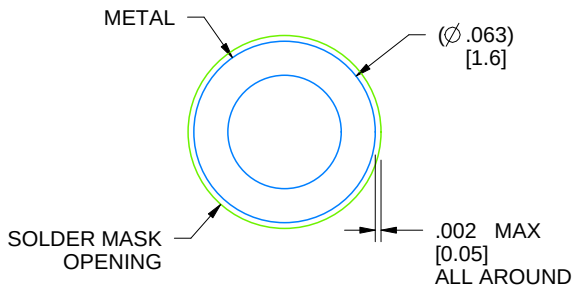
CERAMIC DUAL IN LINE PACKAGE



LAND PATTERN EXAMPLE
NON-SOLDER MASK DEFINED
SCALE: 5X



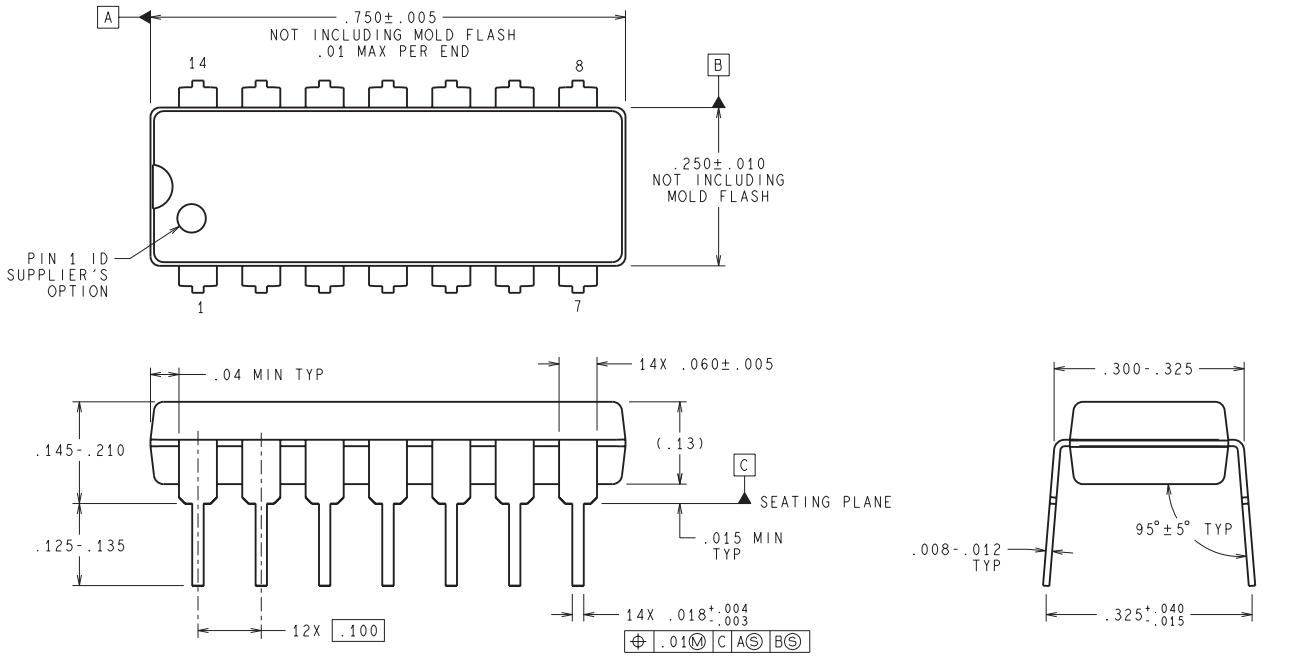
DETAIL A
SCALE: 15X



DETAIL B
13X, SCALE: 15X

4214771/A 05/2017

NFF0014A



DIMENSIONS ARE IN INCHES
DIMENSIONS IN ( ) FOR REFERENCE ONLY

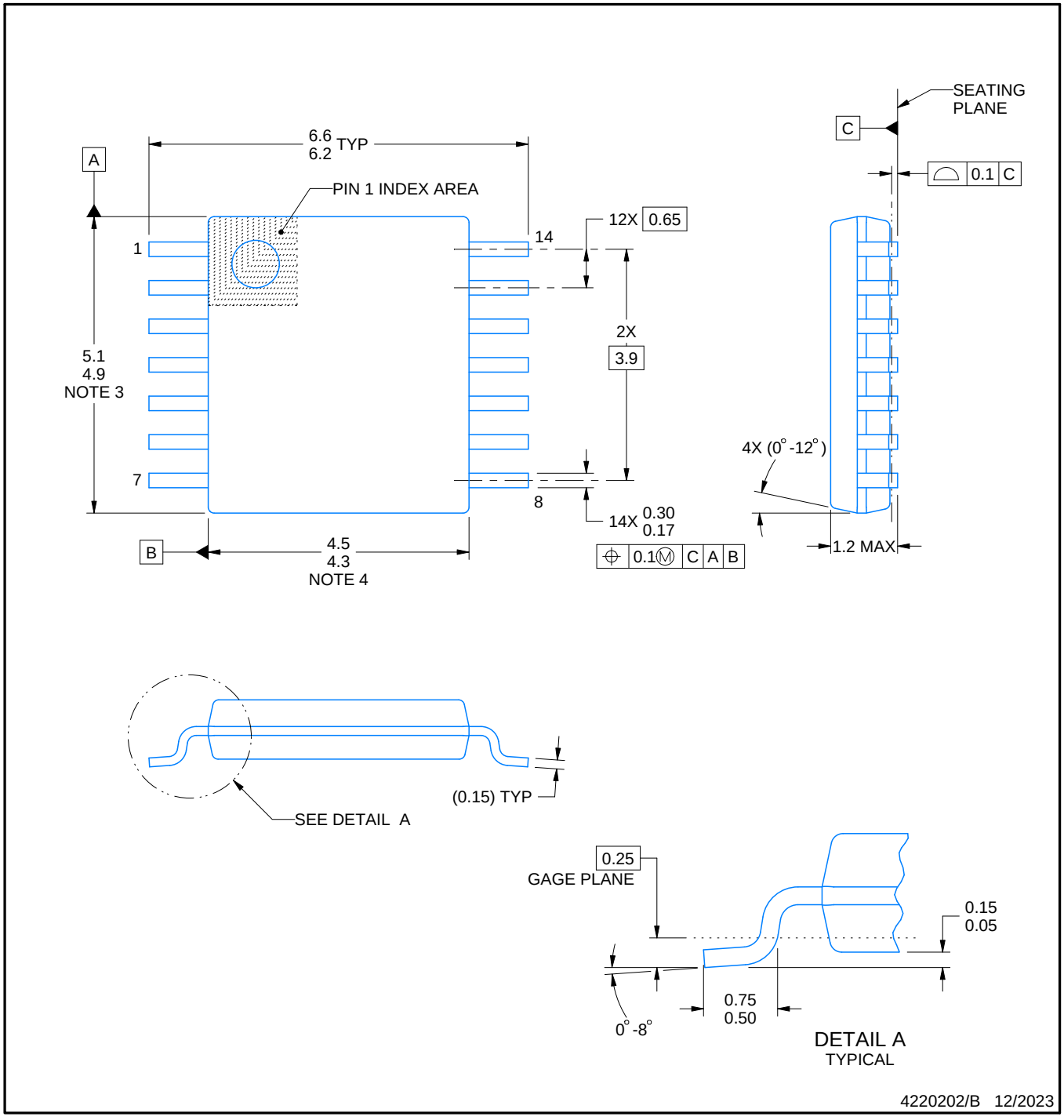
N14A (Rev G)

PACKAGE OUTLINE

PW0014A

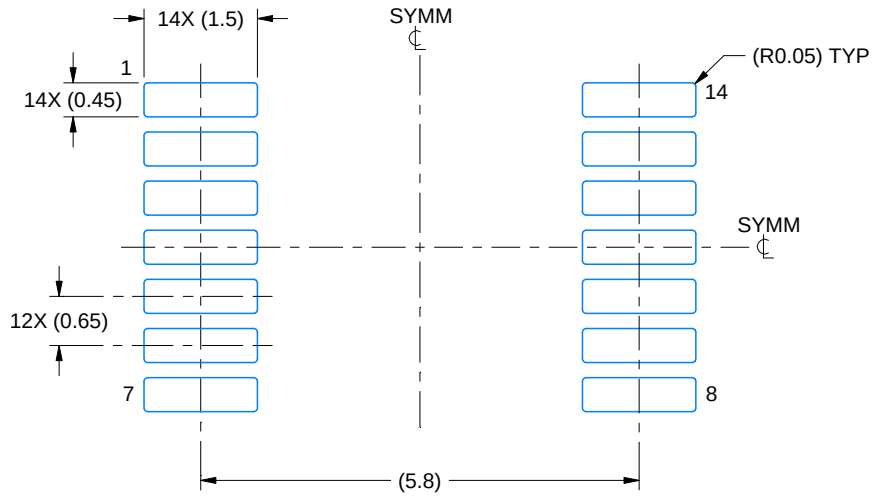
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

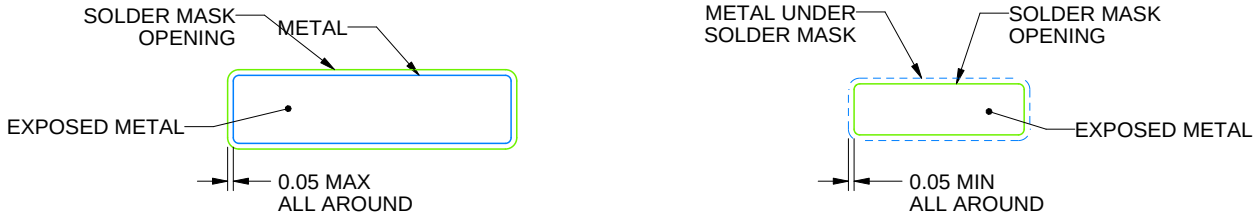


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

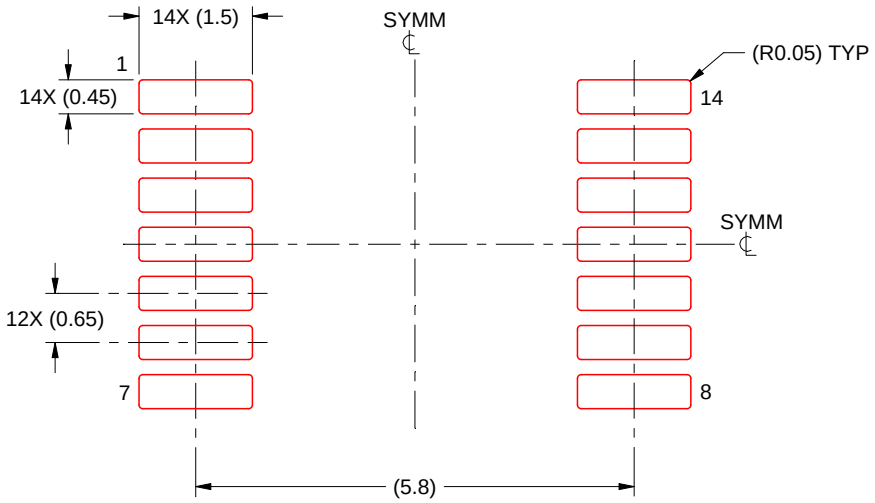


SOLDER MASK DETAILS

4220202/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

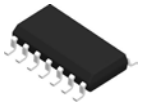


SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220202/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

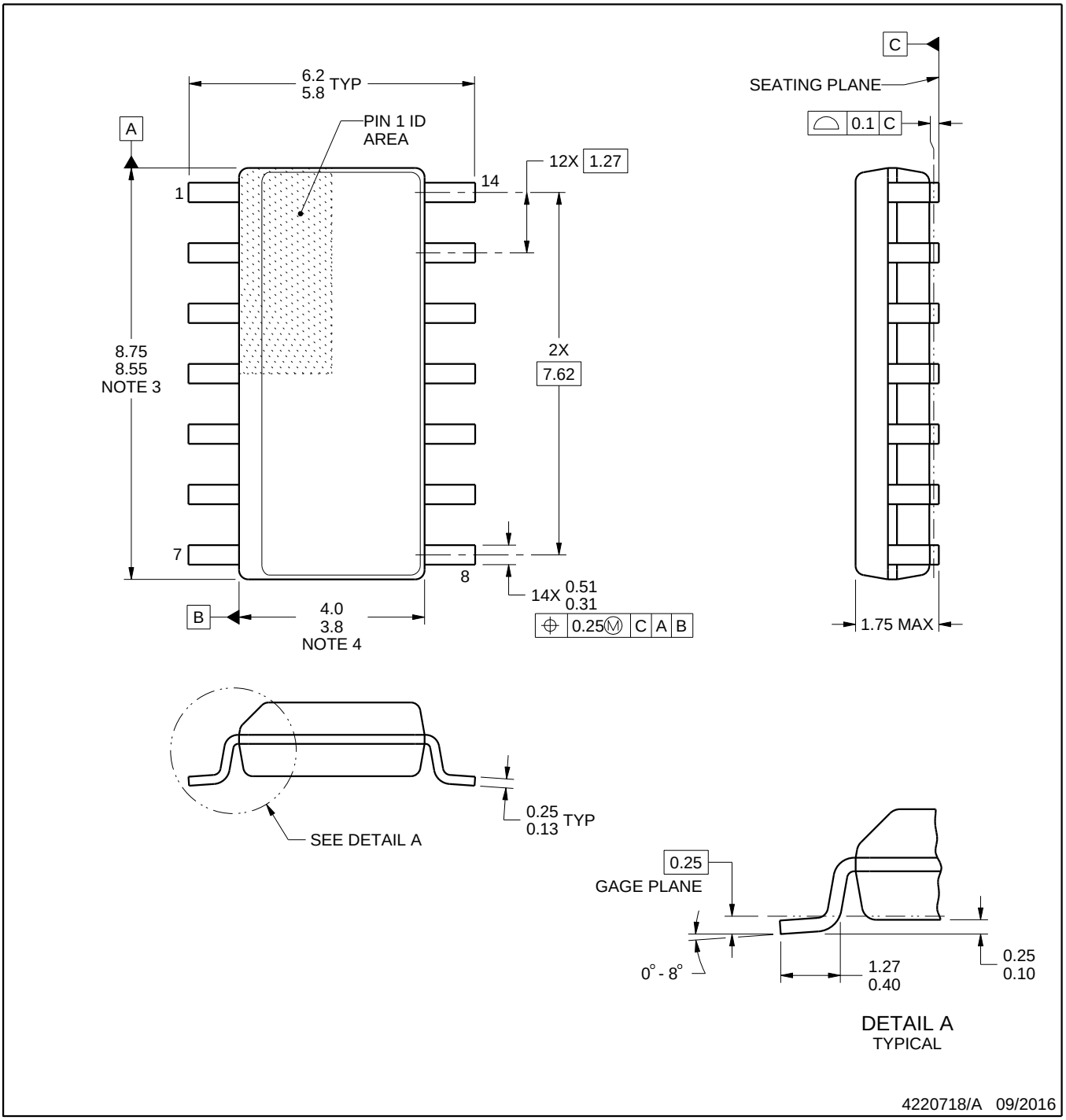


PACKAGE OUTLINE

D0014A

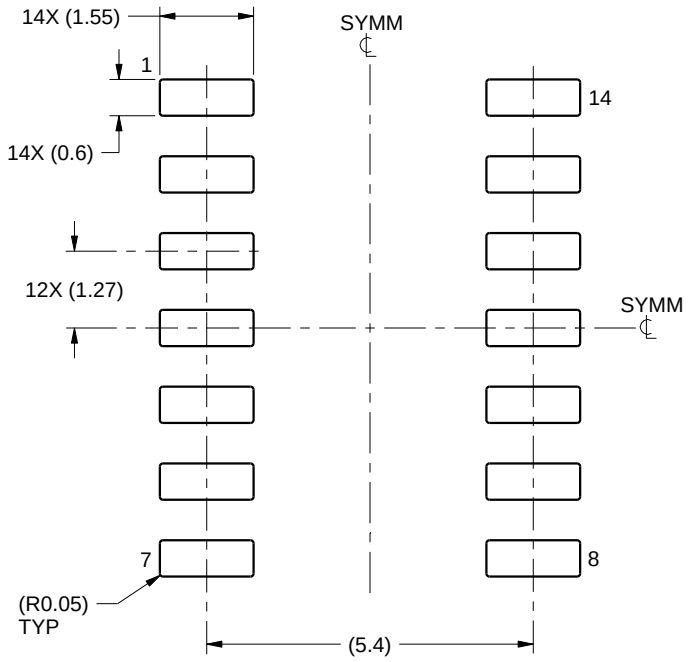
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

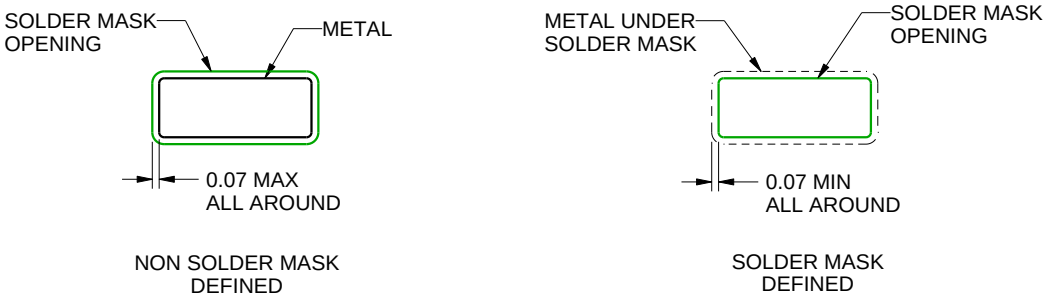


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.



LAND PATTERN EXAMPLE
SCALE:8X



SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

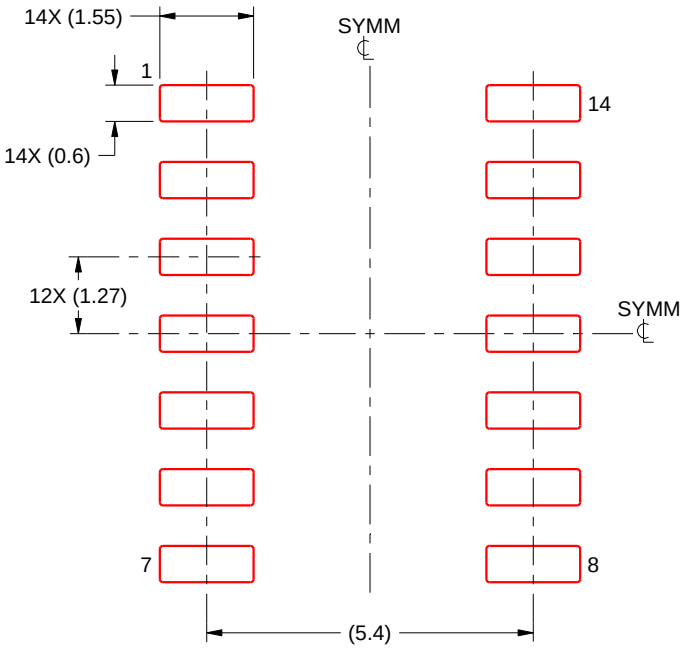
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

4220718/A 09/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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