TEXAS INSTRUMENTS
LM158-N, LM258-N, LM2904-N, LM358-N
JAJSB93J – JANUARY 2000 – REVISED MARCH 2022

LMx58-N 低消費電力、デュアル・オペアンプ

1 特長

- 8 バンプの DSBGA チップ・サイズ・パッケージで供給 (AN-1112、SNVA009 を参照)
- ユニティ・ゲインのため内部的に周波数を補償
- 大きい DC 電圧ゲイン：100dB
- 広い帯域幅 (ユニティ・ゲイン)：1MHz (温度補償済み)
- 広い電源電圧範囲：
  - 単一電源：3V～32V
  - またはデュアル電源：±1.5V～±16V
- 非常に低い電源消費電流 (500μA) - 本質的に電源電圧の値には無関係
- 低い入力オフセット電圧：2mV
- グランドを含む入力同相電圧範囲
- 差動入力電圧範囲が電源電圧と同じ
- 大きな出力電圧振幅
- 独自の特性：
  - リニア・モードでは、単一電源電圧のみで動作していても、入力同相電圧範囲はグランドを含み、出力電圧もグランドまでスイングできます。
  - ユニティ・ゲインのクロス周波数を温度補償
  - 入力バイアス電流も温度補償
- 利点：
  - 2 つの内部補償付きオペアンプ
  - デュアル電源が不要
  - 直接 GND レベル近くまでセンシング可能、V_{OUT} も GND レベルまで遷移可能
  - すべての形式のロジックと互換
  - バッテリ動作に適した消費電力

2 アプリケーション

- アクティブ・フィルタ
- 汎用のシグナル・コンディショニングと増幅
- 4mA～20mA の電流ループ・トランスミッタ

3 概要

LM158 シリーズは、2 つの独立した高ゲインの内部周波数補償付きオペアンプで構成され、広い電圧範囲にわたって単一電源で動作するように特に設計されています。分割電源からも動作でき、低消費電力で、電源からの消費電流は電源電圧の大きさに依存しません。

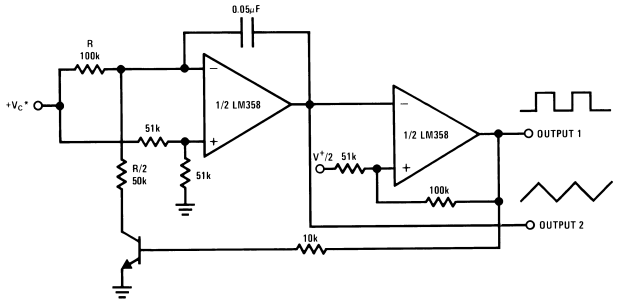
応用分野として、トランスデューサ・アンプ、DC ゲイン・ブロック、各種の従来型オペアンプ回路があり、これらを単一電源システムで、より簡単に実装できます。たとえば、LM158 シリーズは、デジタル・システムで使用される標準の 3.3V 電源電圧で直接動作し、追加の ±15V 電源の必要なしに、必要なインターフェイス電子回路を簡単に提供できます。

LM358 と LM2904 は TI の DSBGA パッケージ技術を使用したチップ・サイズ・パッケージ (8 バンプ DSBGA) で供給されます。

製品情報

部品番号(1)	パッケージ	本体サイズ (公称)
LM158-N	TO-CAN (8)	9.08mm × 9.09mm
	CDIP (8)	10.16mm × 6.502mm
LM258-N	TO-CAN (8)	9.08mm × 9.09mm
LM2904-N	DSBGA (8)	1.31mm × 1.31mm
	SOIC (8)	4.90mm × 3.91mm
	PDIP (8)	9.81mm × 6.35mm
LM358-N	TO-CAN (8)	9.08mm × 9.09mm
	DSBGA (8)	1.31mm × 1.31mm
	SOIC (8)	4.90mm × 3.91mm
	PDIP (8)	9.81mm × 6.35mm

(1) 利用可能なパッケージについては、このデータシートの末尾にある注文情報を参照してください。



電圧制御発振器 (VCO)

英語版の TI 製品についての情報を翻訳したこの資料は、製品の概要を確認する目的で便宜的に提供しているものです。該当する正式な英語版の最新情報は、www.ti.com で閲覧でき、その内容が常に優先されます。TI では翻訳の正確性および妥当性につきましては一切保証いたしません。実際の設計などの前には、必ず最新版の英語版をご参照くださいますようお願いいたします。

Table of Contents

1 特長 ... 1
2 アプリケーション ... 1
3 概要 ... 1
4 Revision History ... 2
5 Pin Configuration and Functions ... 3
6 Specifications ... 4
6.1 Absolute Maximum Ratings ... 4
6.2 ESD Ratings ... 4
6.3 Recommended Operating Conditions ... 5
6.4 Thermal Information ... 5
6.5 Electrical Characteristics: LM158A, LM358A, LM158, LM258 ... 5
6.6 Electrical Characteristics: LM358, LM2904 ... 7
6.7 Typical Characteristics ... 9
7 Detailed Description ... 12
7.1 Overview ... 12
7.2 Functional Block Diagram ... 12
7.3 Feature Description ... 12
7.4 Device Functional Modes ... 13
8 Application and Implementation ... 14
8.1 Application Information ... 14
8.2 Typical Applications ... 14
9 Power Supply Recommendations ... 22
10 Layout ... 22
10.1 Layout Guidelines ... 22
10.2 Layout Example ... 22
11 Device and Documentation Support ... 23
11.1 Receiving Notification of Documentation Updates ... 23
11.2 サポート・リソース ... 23
11.3 Trademarks ... 23
11.4 Electrostatic Discharge Caution ... 23
11.5 Glossary ... 23
12 Mechanical, Packaging, and Orderable Information ... 23

4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision I (December 2014) to Revision J (March 2022)	Page
• 文書全体にわたって表、図、相互参照の採番方法を更新	1
• Corrected pin 5 (+INB) and pin 7 (OUTB) description information in the *Pin Configuration and Functions* section	3
• Deleted *Related Links* from the *Device and Documentation Support* section	23

Changes from Revision H (March 2013) to Revision I (December 2014)	Page
• 「*ピン構成および機能*」セクション、「*ESD 定格*」表、「*機能説明*」セクション、「*デバイスの機能モード*」セクション、「*アプリケーションと実装*」セクション、「*電源に関する推奨事項*」セクション、「*レイアウト*」セクション、「*デバイスおよびドキュメントのサポート*」セクション、「*メカニカル、パッケージ、および注文情報*」セクションを追加	1

Changes from Revision G (March 2013) to Revision H (March 2013)	Page
• ナショナル セミコンダクターのデータシートのレイアウトを TI 形式に変更	1

Copyright © 2022 Texas Instruments Incorporated

5 Pin Configuration and Functions

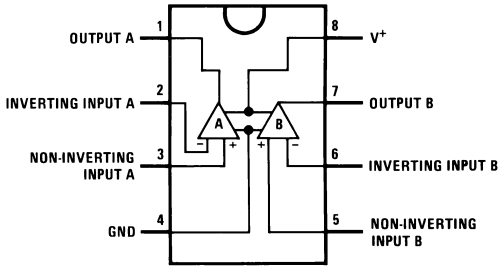


図 5-1. D, P, and NAB Package 8-Pin SOIC, PDIP, and CDIP (Top View)

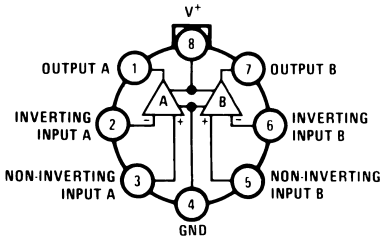


図 5-2. LMC Package 8-Pin TO-99 Top View

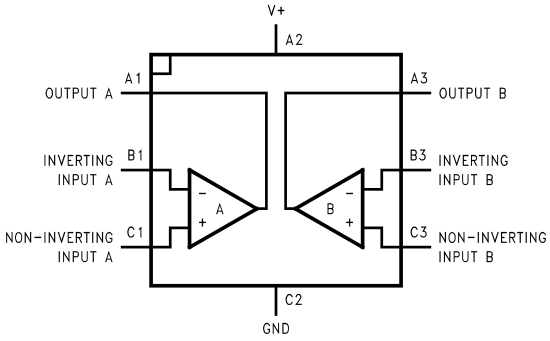


図 5-3. YPB Package 8-Pin DSBGA Top View

表 5-1. Pin Functions

PIN			TYPE(1)	DESCRIPTION
NAME	D/P/LMC	YPB		
OUTA	1	A1	O	Output, channel A
–INA	2	B1	I	Inverting input, channel A
+INA	3	C1	I	Non-inverting input, channel A
GND / V–	4	C2	P	Ground for single-supply configurations. Negative supply for dual-supply configurations.
+INB	5	C3	I	Non-inverting input, channel B
–INB	6	B3	I	Inverting input, channel B
OUTB	7	A3	O	Output, channel B
V+	8	A2	P	Positive supply

(1) Signal Types: I = Input, O = Output, I/O = Input or Output, P = Power

Copyright © 2022 Texas Instruments Incorporated

6 Specifications

6.1 Absolute Maximum Ratings

See (1) (2) (3).

			LM158, LM258, LM358, LM158A, LM258A, LM358A		LM2904		UNIT
			MIN	MAX	MIN	MAX	
Supply Voltage, V^+				32		26	V
Differential Input Voltage				32		26	V
Input Voltage			−0.3	32	−0.3	26	V
Power Dissipation(4)	PDIP (P)			830		830	mW
	TO-99 (LMC)			550			mW
	SOIC (D)			530		530	mW
	DSBGA (YPB)			435			mW
Output Short-Circuit to GND (One Amplifier)(5)	$V^+ \le 15$ V and $T_A = 25°C$			Continuous		Continuous	
Input Current ($V_{IN} < -0.3V$)(6)				50		50	mA
Temperature			−55	125			°C
	PDIP Package (P): Soldering (10 seconds)			260		260	°C
	SOIC Package (D)	Vapor Phase (60 seconds)		215		215	°C
		Infrared (15 seconds)		220		220	°C
Lead Temperature	PDIP (P): (Soldering, 10 seconds)			260		260	°C
	TO-99 (LMC): (Soldering, 10 seconds)			300		300	°C
Storage temperature, T_{stg}			−65	150	−65	150	°C

(1) *Absolute Maximum Ratings* indicate limits beyond which damage to the device may occur. *Recommended Operating Conditions* indicate conditions for which the device is intended to be functional, but specific performance is not ensured. For ensured specifications and the test conditions, see the Electrical Characteristics.
(2) Refer to RETS158AX for LM158A military specifications and to RETS158X for LM158 military specifications.
(3) If Military/Aerospace specified devices are required, please contact the TI Sales Office/Distributors for availability and specifications.
(4) For operating at high temperatures, the LM358/LM358A, LM2904 must be derated based on a 125°C maximum junction temperature and a thermal resistance of 120°C/W for PDIP, 182°C/W for TO-99, 189°C/W for SOIC package, and 230°C/W for DSBGA, which applies for the device soldered in a printed circuit board, operating in a still air ambient. The LM258/LM258A and LM158/LM158A can be derated based on a +150°C maximum junction temperature. The dissipation is the total of both amplifiers—use external resistors, where possible, to allow the amplifier to saturate or to reduce the power which is dissipated in the integrated circuit.
(5) Short circuits from the output to V^+ can cause excessive heating and eventual destruction. When considering short circuits to ground, the maximum output current is approximately 40 mA independent of the magnitude of V^+. At values of supply voltage in excess of +15 V, continuous short-circuits can exceed the power dissipation ratings and cause eventual destruction. Destructive dissipation can result from simultaneous shorts on all amplifiers.
(6) This input current will only exist when the voltage at any of the input leads is driven negative. It is due to the collector-base junction of the input PNP transistors becoming forward biased and thereby acting as input diode clamps. In addition to this diode action, there is also lateral NPN parasitic transistor action on the IC chip. This transistor action can cause the output voltages of the op amps to go to the V^+voltage level (or to ground for a large overdrive) for the time duration that an input is driven negative. This is not destructive and normal output states will re-establish when the input voltage, which was negative, again returns to a value greater than −0.3 V (at 25°C).

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±250	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

Copyright © 2022 Texas Instruments Incorporated

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	MAX	UNIT
Supply Voltage (V+ - V-):LM158. LM258, LM358	3 (±1.5)	32 (±16)	V
Supply Voltage (V+ - V-):LM2904	3 (±1.5)	26 (±13)	V
Operating Temperature: LM158	-55	125	°C
Operating Temperature: LM258	-25	85	°C
Operating Temperature: LM358	0	70	°C
Operating Temperature: LM2904	-40	85	°C

6.4 Thermal Information

THERMAL METRIC(1)		LM158-N, LM258-N, LM358-N	LM158-N	LM2904-N, LM358-N			UNIT
		LMC	NAB	YPB	D	P	
		8 PINS					
$R_{\theta JA}$	Junction-to-ambient thermal resistance	155	132	230	189	120	°C/W

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics: LM158A, LM358A, LM158, LM258

V^+ = +5.0 V, See(2), unless otherwise stated

PARAMETER	TEST CONDITIONS	LM158A			LM358A			LM158, LM258			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	See(3), T_A = 25°C		1	2		2	3		2	5	mV
Input Bias Current	$I_{IN(+)}$ or $I_{IN(-)}$, T_A = 25°C,		20	50		45	100		45	150	nA
	V_{CM} = 0 V,(4)										
Input Offset Current	$I_{IN(+)} - I_{IN(-)}$, V_{CM} = 0V, T_A = 25°C		2	10		5	30		3	30	nA
Input Common-Mode Voltage Range	V^+ = 30 V,(5) (LM2904, V^+ = 26V), T_A = 25°C	0		V^+−1.5	0		V^+−1.5	0		V^+−1.5	V
Supply Current	Over Full Temperature Range R_L = ∞ on All Op Amps										
	V^+ = 30V (LM2904 V^+ = 26V)		1	2		1	2		1	2	mA
	V^+ = 5V		0.5	1.2		0.5	1.2		0.5	1.2	mA
Large Signal Voltage Gain	V^+ = 15 V, T_A = 25°C, R_L ≥ 2 kΩ, (For V_O = 1 V to 11 V)	50	100		25	100		50	100		V/mV
Common-Mode Rejection Ratio	T_A = 25°C, V_{CM} = 0 V to V^+−1.5 V	70	85		65	85		70	85		dB
Power Supply Rejection Ratio	V^+ = 5 V to 30 V (LM2904, V^+ = 5 V to 26 V), T_A = 25°C	65	100		65	100		65	100		dB
Power Supply Rejection Ratio	V^+ = 5 V to 30 V (LM2904, V^+ = 5 V to 26 V), T_A = 25°C	65	100		65	100		65	100		dB
Amplifier-to-Amplifier Coupling	f = 1 kHz to 20 kHz, T_A = 25°C (Input Referred), See(6)		−120			−120			−120		dB

Copyright © 2022 Texas Instruments Incorporated

6.5 Electrical Characteristics: LM158A, LM358A, LM158, LM258 (continued)

V^+ = +5.0 V, See(2), unless otherwise stated

PARAMETER		TEST CONDITIONS		LM158A			LM358A			LM158, LM258			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Output Current	Source	V_{IN}^+ = 1 V,		20	40		20	40		20	40		mA
		V_{IN}^- = 0 V,											
		V^+ = 15 V,											
		V_O = 2 V, T_A = 25°C											
	Sink	V_{IN}^- = 1 V, V_{IN}^+ = 0 V		10	20		10	20		10	20		mA
		V^+ = 15 V, T_A = 25°C,											
		V_O = 2 V											
		V_{IN}^- = 1 V,		12	50		12	50		12	50		µA
		V_{IN}^+ = 0 V											
		T_A = 25°C, V_O = 200 mV,											
		V^+ = 15 V											
Short Circuit to Ground		T_A = 25°C, See(1), V^+ = 15 V			40	60		40	60		40	60	mA
Input Offset Voltage		See(3)				4			5			7	mV
Input Offset Voltage Drift		R_S = 0Ω			7	15		7	20		7		µV/°C
Input Offset Current		$I_{IN(+)} - I_{IN(-)}$				30			75			100	nA
Input Offset Current Drift		R_S = 0Ω			10	200		10	300		10		pA/°C
Input Bias Current		$I_{IN(+)}$ or $I_{IN(-)}$			40	100		40	200		40	300	nA
Input Common-Mode Voltage Range		V^+ = 30 V, See(5) (LM2904, V^+ = 26 V)		0		V^+–2	0		V^+–2	0		V^+–2	V
Large Signal Voltage Gain		V^+ = +15 V		25			15			25			V/mV
		(V_O = 1 V to 11 V)											
		R_L ≥ 2 kΩ											
Output Voltage	V_{OH}	V^+ = +30 V	R_L = 2 kΩ	26			26			26			V
		(LM2904, V^+ = 26 V)	R_L = 10 kΩ	27	28		27	28		27	28		V
Swing	V_{OL}	V^+ = 5V, R_L = 10 kΩ			5	20		5	20		5	20	mV
Output Current	Source	V_{IN}^+ = +1 V, V_{IN}^- = 0 V,		10	20		10	20		10	20		mA
		V^+ = 15 V, V_O = 2 V											
	Sink	V_{IN}^- = +1 V, V_{IN}^+ = 0 V,		10	15		5	8		5	8		mA
		V^+ = 15 V, V_O = 2 V											

(1) Short circuits from the output to V^+ can cause excessive heating and eventual destruction. When considering short circuits to ground, the maximum output current is approximately 40 mA independent of the magnitude of V^+. At values of supply voltage in excess of +15 V, continuous short-circuits can exceed the power dissipation ratings and cause eventual destruction. Destructive dissipation can result from simultaneous shorts on all amplifiers.

(2) These specifications are limited to –55°C ≤ T_A ≤ +125°C for the LM158/LM158A. With the LM258/LM258A, all temperature specifications are limited to −25°C ≤ T_A ≤ 85°C, the LM358/LM358A temperature specifications are limited to 0°C ≤ T_A ≤ 70°C, and the LM2904 specifications are limited to –40°C ≤ T_A ≤ 85°C.

(3) V_O ≈ 1.4 V, R_S = 0 Ω with V^+ from 5 V to 30 V; and over the full input common-mode range (0 V to V^+ −1.5 V) at 25°C. For LM2904, V^+ from 5 V to 26 V.

(4) The direction of the input current is out of the IC due to the PNP input stage. This current is essentially constant, independent of the state of the output so no loading change exists on the input lines.

(5) The input common-mode voltage of either input signal voltage should not be allowed to go negative by more than 0.3 V (at 25°C). The upper end of the common-mode voltage range is V^+ −1.5 V (at 25°C), but either or both inputs can go to 32 V without damage (26 V for LM2904), independent of the magnitude of V^+.

(6) Due to proximity of external components, insure that coupling is not originating via stray capacitance between these external parts. This typically can be detected as this type of capacitance increases at higher frequencies.

Copyright © 2022 Texas Instruments Incorporated

6.6 Electrical Characteristics: LM358, LM2904

V^+ = +5.0 V, See(2), unless otherwise stated

PARAMETER		TEST CONDITIONS		LM358			LM2904			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage		See(3) , T_A = 25°C			2	7		2	7	mV
Input Bias Current		$I_{IN(+)}$ or $I_{IN(-)}$, T_A = 25°C, V_{CM} = 0 V, See(4)			45	250		45	250	nA
Input Offset Current		$I_{IN(+)}$ − $I_{IN(-)}$, V_{CM} = 0 V, T_A = 25°C			5	50		5	50	nA
Input Common-Mode Voltage Range		V^+ = 30 V, See(5) (LM2904, V^+ = 26 V), T_A = 25°C		0		V^+−1.5	0		V^+−1.5	V
Supply Current		Over Full Temperature Range								
		R_L = ∞ on All Op Amps								
		V^+ = 30 V (LM2904 V^+ = 26 V)			1	2		1	2	mA
		V^+ = 5 V			0.5	1.2		0.5	1.2	mA
Large Signal Voltage		V^+ = 15V, T_A = 25°C,								
Gain		R_L ≥ 2 kΩ, (For V_O = 1 V to 11 V)		25	100		25	100		V/mV
Common-Mode Rejection Ratio		T_A = 25°C,		65	85		50	70		dB
		V_{CM} = 0 V to V^+−1.5 V								
Power Supply Rejection Ratio		V^+ = 5 V to 30 V		65	100		50	100		dB
		(LM2904, V^+ = 5 V to 26 V), T_A = 25°C								
Amplifier-to-Amplifier Coupling		f = 1 kHz to 20 kHz, T_A = 25°C (Input Referred), See(6)			−120			−120		dB
Output Current	Source	V_{IN}^+ = 1 V,		20	40		20	40		mA
		V_{IN}^- = 0 V,								
		V^+ = 15 V,								
		V_O = 2 V, T_A = 25°C								
	Sink	V_{IN}^- = 1 V, V_{IN}^+ = 0 V		10	20		10	20		mA
		V^+ = 15V, T_A = 25°C,								
		V_O = 2 V								
		V_{IN}^- = 1 V,		12	50		12	50		µA
		V_{IN}^+ = 0 V								
		T_A = 25°C, V_O = 200 mV,								
		V^+ = 15 V								
Short Circuit to Ground		T_A = 25°C, See(1), V^+ = 15 V			40	60		40	60	mA
Input Offset Voltage		See(3)				9			10	mV
Input Offset Voltage Drift		R_S = 0 Ω			7			7		µV/°C
Input Offset Current		$I_{IN(+)}$ − $I_{IN(-)}$				150		45	200	nA
Input Offset Current Drift		R_S = 0 Ω			10			10		pA/°C
Input Bias Current		$I_{IN(+)}$ or $I_{IN(-)}$			40	500		40	500	nA
Input Common-Mode Voltage Range		V^+ = 30 V, See(5) (LM2904, V^+ = 26 V)		0		V^+−2	0		V^+ −2	V
Large Signal Voltage Gain		V^+ = +15 V		15			15			V/mV
		(V_O = 1 V to 11 V)								
		R_L ≥ 2 kΩ								
Output	V_{OH}	V^+ = 30 V	R_L = 2 kΩ	26			22			V
Voltage		(LM2904, V^+ = 26 V)	R_L = 10 kΩ	27	28		23	24		V
Swing	V_{OL}	V^+ = 5 V, R_L = 10 kΩ			5	20		5	100	mV

Copyright © 2022 Texas Instruments Incorporated

6.6 Electrical Characteristics: LM358, LM2904 (continued)

V^+ = +5.0 V, See(2), unless otherwise stated

PARAMETER		TEST CONDITIONS	LM358			LM2904			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
Output Current	Source	V_{IN}^+ = 1 V, V_{IN}^- = 0 V, V^+ = 15 V, V_O = 2 V	10	20		10	20		mA
	Sink	V_{IN}^- = 1 V, V_{IN}^+ = 0 V, V^+ = 15 V, V_O = 2 V	5	8		5	8		mA

(1) Short circuits from the output to V^+ can cause excessive heating and eventual destruction. When considering short circuits to ground, the maximum output current is approximately 40 mA independent of the magnitude of V^+. At values of supply voltage in excess of +15 V, continuous short-circuits can exceed the power dissipation ratings and cause eventual destruction. Destructive dissipation can result from simultaneous shorts on all amplifiers.

(2) These specifications are limited to –55°C ≤ T_A ≤ +125°C for the LM158/LM158A. With the LM258/LM258A, all temperature specifications are limited to −25°C ≤ T_A ≤ 85°C, the LM358/LM358A temperature specifications are limited to 0°C ≤ T_A ≤ 70°C, and the LM2904 specifications are limited to –40°C ≤ T_A ≤ 85°C.

(3) V_O ≅ 1.4 V, R_S = 0 Ω with V^+ from 5 V to 30 V; and over the full input common-mode range (0 V to V^+ −1.5 V) at 25°C. For LM2904, V^+ from 5 V to 26 V.

(4) The direction of the input current is out of the IC due to the PNP input stage. This current is essentially constant, independent of the state of the output so no loading change exists on the input lines.

(5) The input common-mode voltage of either input signal voltage should not be allowed to go negative by more than 0.3 V (at 25°C). The upper end of the common-mode voltage range is V^+ −1.5 V (at 25°C), but either or both inputs can go to 32 V without damage (26 V for LM2904), independent of the magnitude of V^+.

(6) Due to proximity of external components, insure that coupling is not originating via stray capacitance between these external parts. This typically can be detected as this type of capacitance increases at higher frequencies.

Copyright © 2022 Texas Instruments Incorporated

6.7 Typical Characteristics

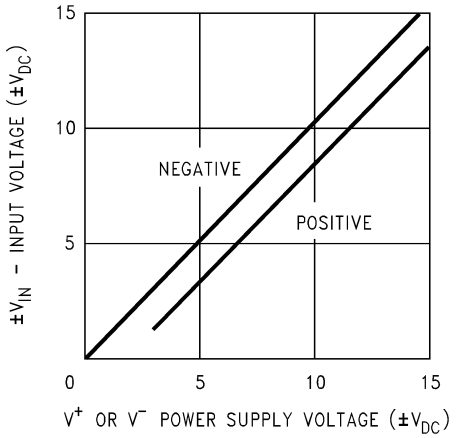


図 6-1. Input Voltage Range

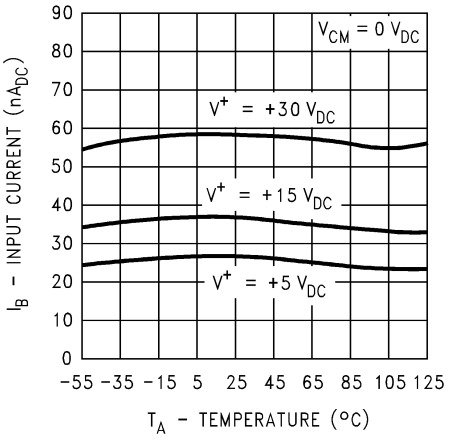


図 6-2. Input Current

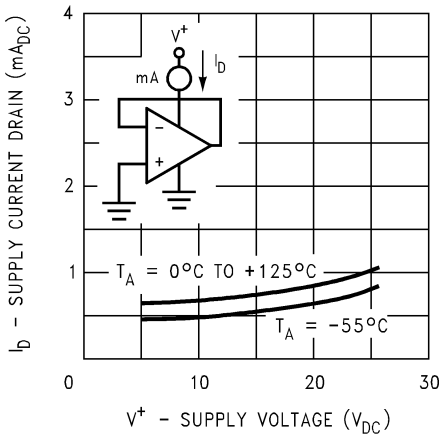


図 6-3. Supply Current

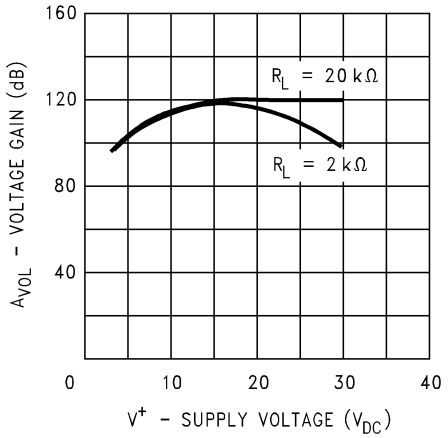


図 6-4. Voltage Gain

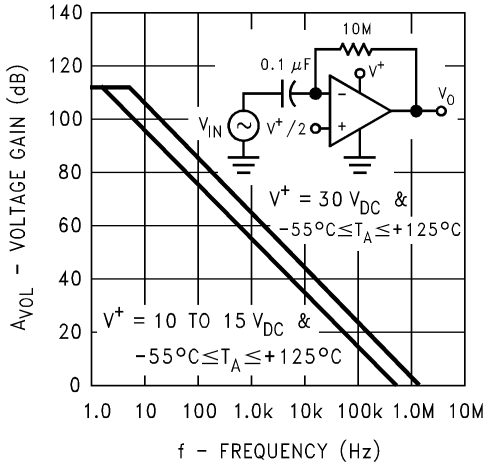


図 6-5. Open Loop Frequency Response

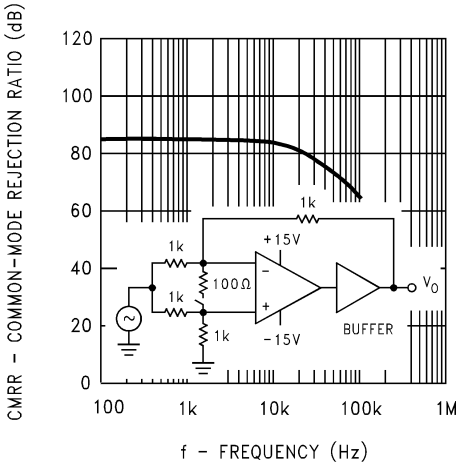


図 6-6. Common-Mode Rejection Ratio

Copyright © 2022 Texas Instruments Incorporated

6.7 Typical Characteristics (continued)

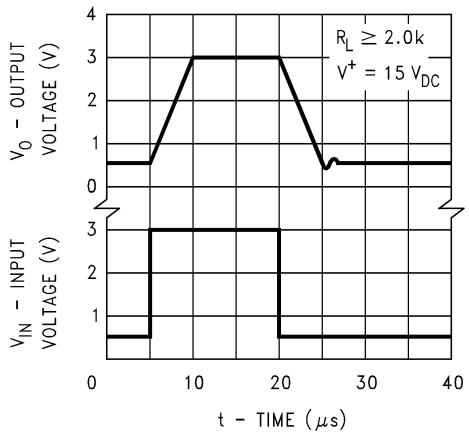


図 6-7. Voltage Follower Pulse Response

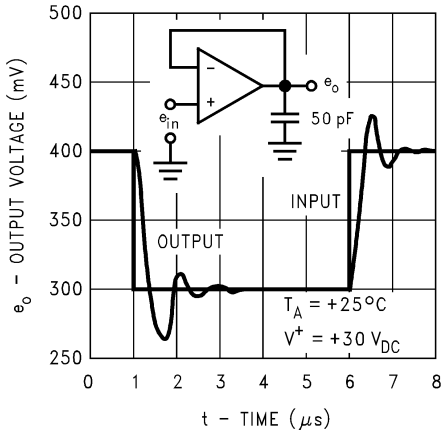


図 6-8. Voltage Follower Pulse Response (Small Signal)

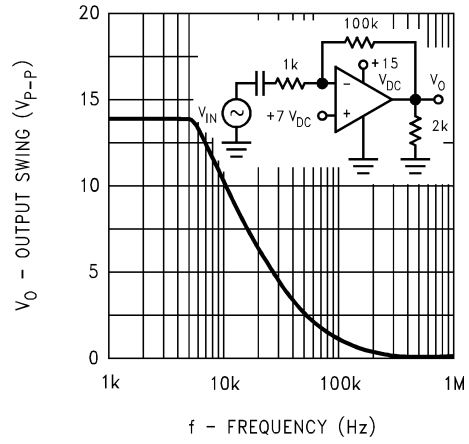


図 6-9. Large Signal Frequency Response

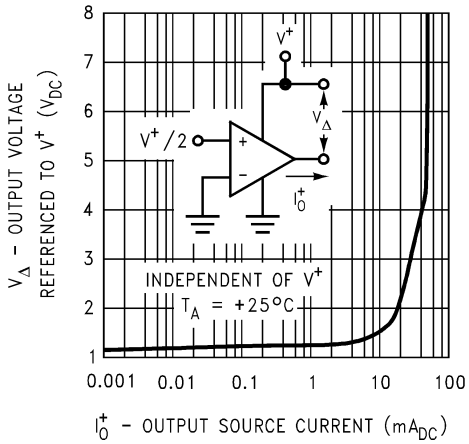


図 6-10. Output Characteristics Current Sourcing

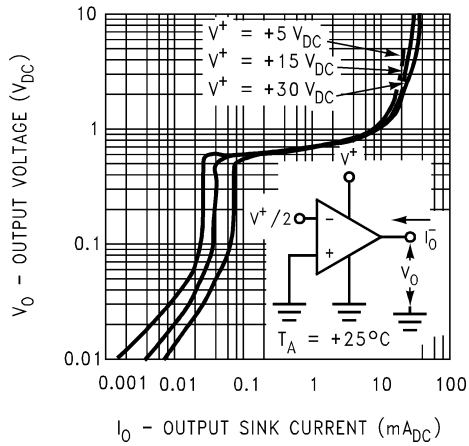


図 6-11. Output Characteristics Current Sinking

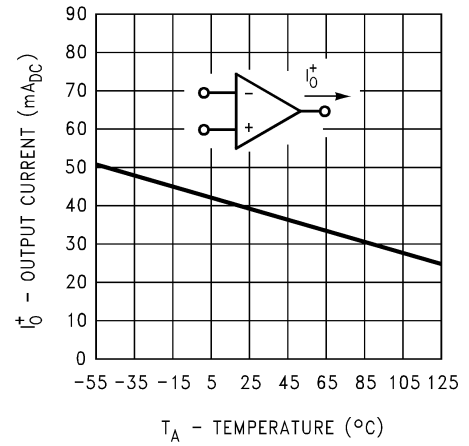


図 6-12. Current Limiting

Copyright © 2022 Texas Instruments Incorporated

6.7 Typical Characteristics (continued)

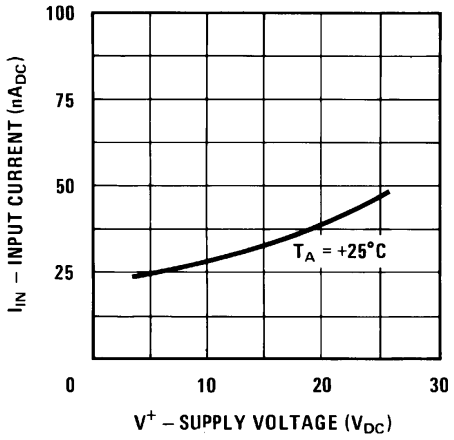


図 6-13. Input Current (LM2902 Only)

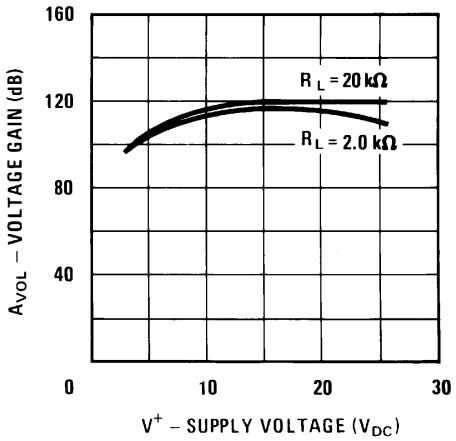


図 6-14. Voltage Gain (LM2902 Only)

Copyright © 2022 Texas Instruments Incorporated

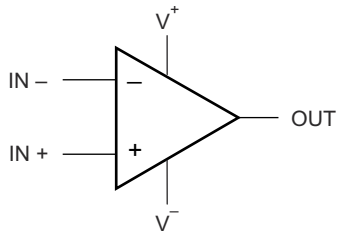
7 Detailed Description

7.1 Overview

The LM158 series are operational amplifiers which can operate with only a single power supply voltage, have true-differential inputs, and remain in the linear mode with an input common-mode voltage of 0 V_{DC}. These amplifiers operate over a wide range of power supply voltage with little change in performance characteristics. At 25°C amplifier operation is possible down to a minimum supply voltage of 2.3 V_{DC}.

Large differential input voltages can be easily accommodated and, as input differential voltage protection diodes are not needed, no large input currents result from large differential input voltages. The differential input voltage may be larger than V^+ without damaging the device. Protection should be provided to prevent the input voltages from going negative more than −0.3 V_{DC} (at 25°C). An input clamp diode with a resistor to the IC input terminal can be used.

7.2 Functional Block Diagram



Copyright © 2016,
Texas Instruments Incorporated

図 7-1. (Each Amplifier)

7.3 Feature Description

The amplifier's differential inputs consist of a non-inverting input (+IN) and an inverting input (–IN). The amplifer amplifies only the difference in voltage between the two inpus, which is called the differential input voltage. The output voltage of the op-amp Vout is given by Equation 1:

$$VOUT = AOL (IN+ - IN-) \quad (1)$$

where

- AOL is the open-loop gain of the amplifier, typically around 100dB (100,000x, or 10uV per Volt).

To reduce the power supply current drain, the amplifiers have a class A output stage for small signal levels which converts to class B in a large signal mode. This allows the amplifiers to both source and sink large output currents. Therefore both NPN and PNP external current boost transistors can be used to extend the power capability of the basic amplifiers. The output voltage needs to raise approximately 1 diode drop above ground to bias the on-chip vertical PNP transistor for output current sinking applications.

For ac applications, where the load is capacitively coupled to the output of the amplifier, a resistor should be used, from the output of the amplifier to ground to increase the class A bias current and prevent crossover distortion. Where the load is directly coupled, as in dc applications, there is no crossover distortion.

Capacitive loads which are applied directly to the output of the amplifier reduce the loop stability margin. Values of 50 pF can be accommodated using the worst-case non-inverting unity gain connection. Large closed loop gains or resistive isolation should be used if larger load capacitance must be driven by the amplifier.

The bias network of the LM158 establishes a drain current which is independent of the magnitude of the power supply voltage over the range of 3 V_{DC} to 30 V_{DC}.

Output short circuits either to ground or to the positive power supply should be of short time duration. Units can be destroyed, not as a result of the short circuit current causing metal fusing, but rather due to the large increase in IC chip power dissipation which will cause eventual failure due to excessive junction temperatures. Putting

Copyright © 2022 Texas Instruments Incorporated

direct short-circuits on more than one amplifier at a time will increase the total IC power dissipation to destructive levels, if not properly protected with external dissipation limiting resistors in series with the output leads of the amplifiers. The larger value of output source current which is available at 25°C provides a larger output current capability at elevated temperatures (see *Typical Characteristics*) than a standard IC op amp.

7.4 Device Functional Modes

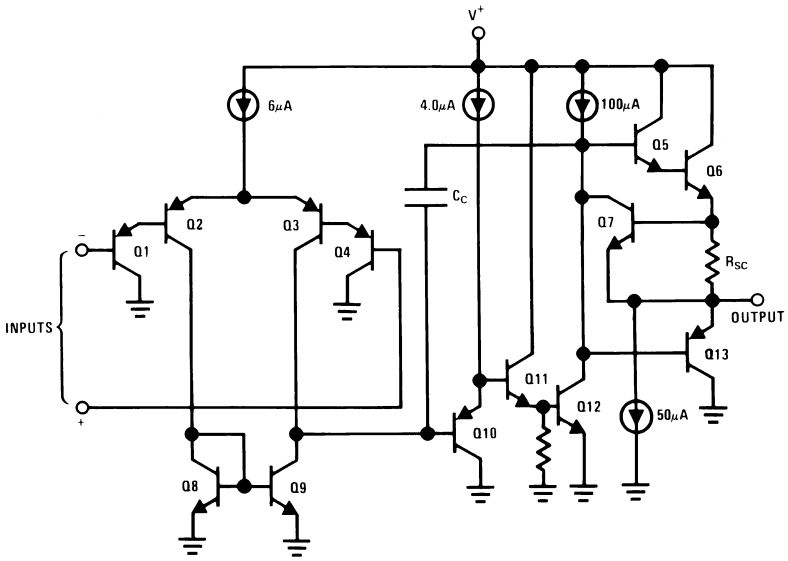


図 7-2. Schematic Diagram

The circuits presented in the *Typical Single-Supply Applications* emphasize operation on only a single power supply voltage. If complementary power supplies are available, all of the standard op-amp circuits can be used. In general, introducing a pseudo-ground (a bias voltage reference of $V^+/2$) will allow operation above and below this value in single power supply systems. Many application circuits are shown which take advantage of the wide input common-mode voltage range which includes ground. In most cases, input biasing is not required and input voltages which range to ground can easily be accommodated.

Copyright © 2022 Texas Instruments Incorporated

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

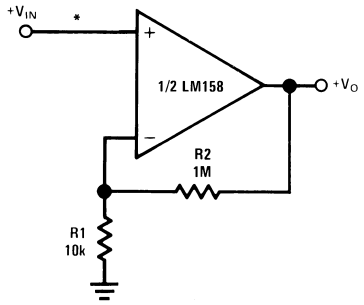
8.1 Application Information

The LM158 family bring performance, economy, and ease-of-use to a wide variety of op-amp applications.

8.2 Typical Applications

8.2.1 Noninverting DC Gain

図 8-1 shows a high input impedance non-inverting circuit. This circuit gives a closed-loop gain equal to the ratio of the sum of R1 and R2 to R1 and a closed-loop 3 dB bandwidth equal to the amplifier unity-gain frequency divided by the closed-loop gain. This design has the benefit of a very high input impedance, which is equal to the differential input impedance multiplied by loop gain. (Open loop gain/Closed loop gain.) In DC coupled applications, input impedance is not as important as input current and its voltage drop across the source resistance. Note that the amplifier output will go into saturation if the input is allowed to float. This may be important if the amplifier must be switched from source to source.



*R not needed due to temperature independent I_{IN}

図 8-1. Non-Inverting DC Gain (0-V Output)

8.2.1.1 Design Requirements

For this example application, the supply voltage is +5V, and 100x±5% of noninverting gain is necessary. Signal input impedance is approx 10kΩ.

8.2.1.2 Detailed Design Procedure

Using the equation for a non-inverting amplifier configuration ; G = 1+ R2/R1, set R1 to 10kΩ, and R2 to 99x the value of R1, which would be 990kΩ. Replacing the 990kΩ with a 1MΩ will result in a gain of 101, which is within the desired gain tolerance.

The gain-frequency characteristic of the amplifier and its feedback network must be such that oscillation does not occur. To meet this condition, the phase shift through amplifier and feedback network must never exceed 180° for any frequency where the gain of the amplifier and its feedback network is greater than unity. In practical applications, the phase shift should not approach 180° since this is the situation of conditional stability. Obviously the most critical case occurs when the attenuation of the feedback network is zero.

Copyright © 2022 Texas Instruments Incorporated

8.2.1.3 Application Curve

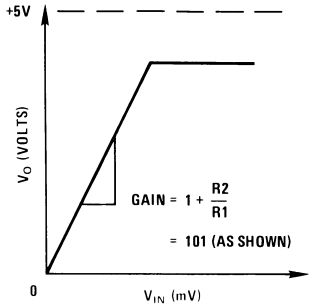
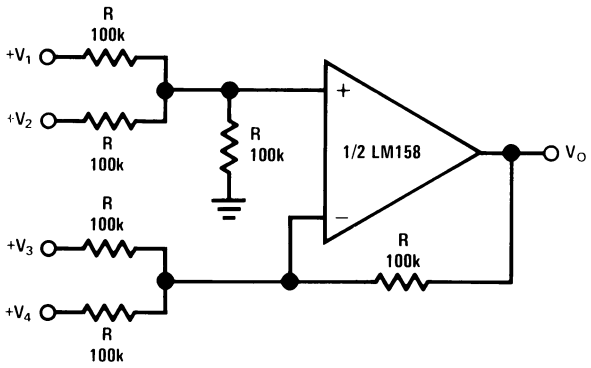


図 8-2. Transfer Curve for Non-Inverting Configuration

8.2.2 System Examples

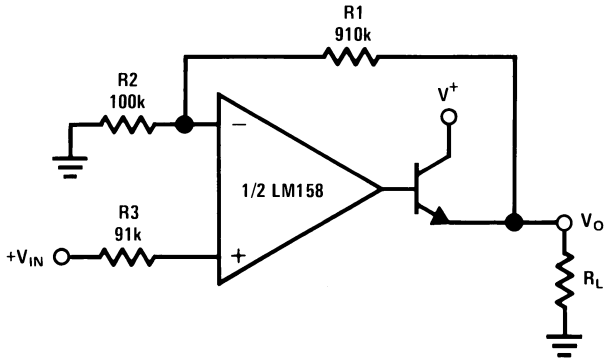
8.2.2.1 Typical Single-Supply Applications

(V^+ = 5.0 V_{DC})



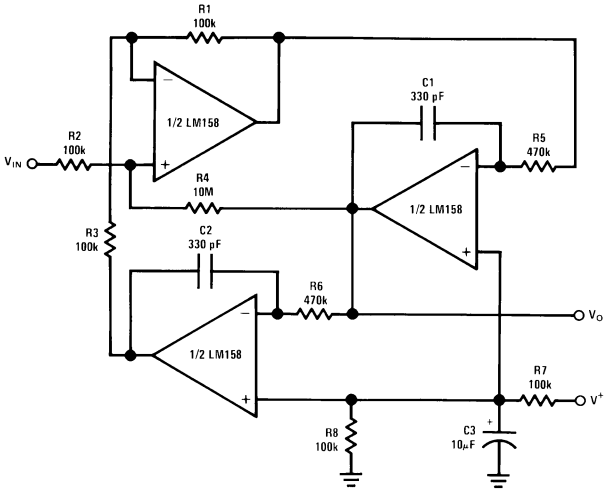
Where: $V_O = V_1 + V_2 - V_3 - V_4$
$(V_1 + V_2) \geq (V_3 + V_4)$ to keep $V_O > 0$ V_{DC}

図 8-3. DC Summing Amplifier ($V_{IN'S} \geq 0$ V_{DC} and $V_O \geq 0$ V_{DC})



$V_O = 0$ V_{DC} for $V_{IN} = 0$ V_{DC}
$A_V = 10$

図 8-4. Power Amplifier



f_o = 1 kHz
Q = 50
A_V = 100 (40 dB)

図 8-5. “BI-QUAD” RC Active Bandpass Filter

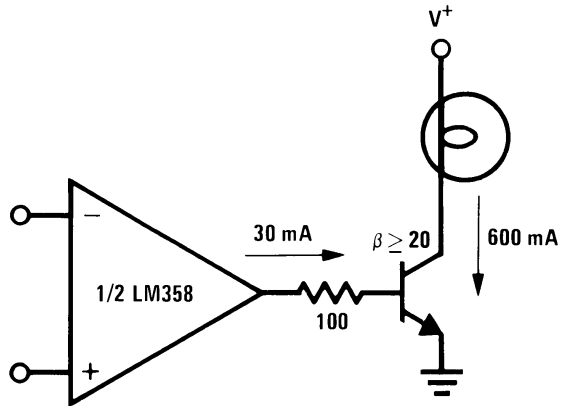


図 8-6. Lamp Driver

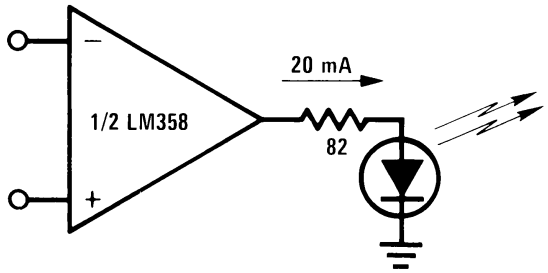


図 8-7. LED Driver

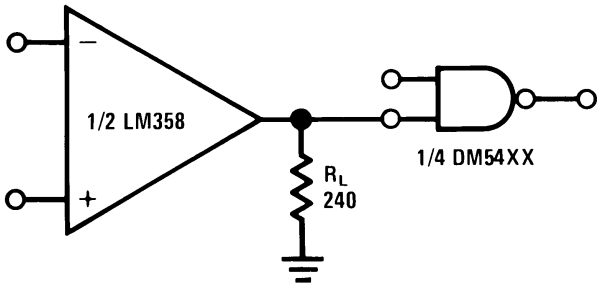
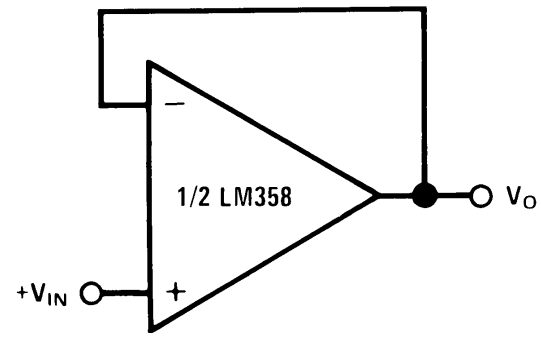


図 8-8. Driving TTL



$V_O = V_{IN}$

図 8-9. Voltage Follower

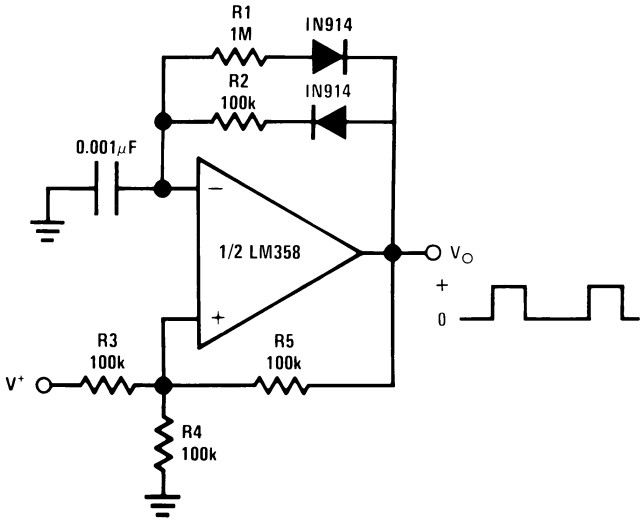


図 8-10. Pulse Generator

Copyright © 2022 Texas Instruments Incorporated

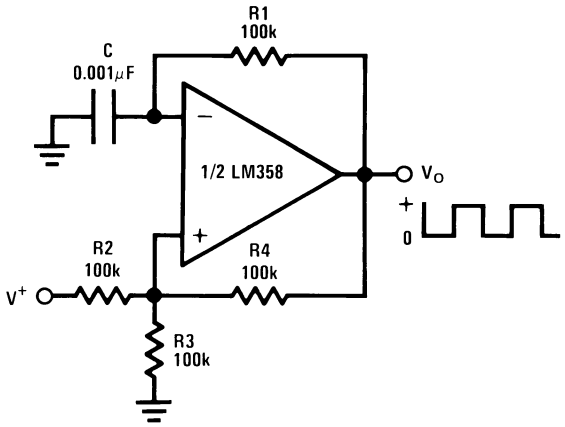


図 8-11. Squarewave Oscillator

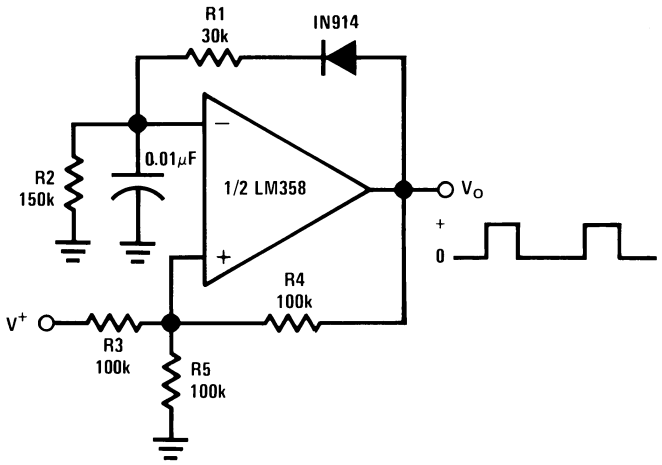
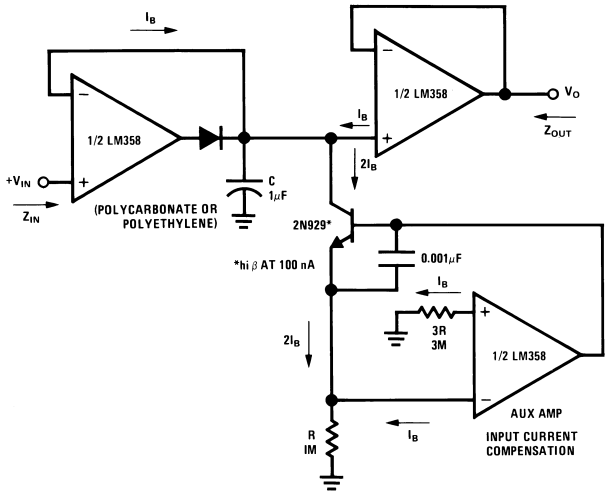
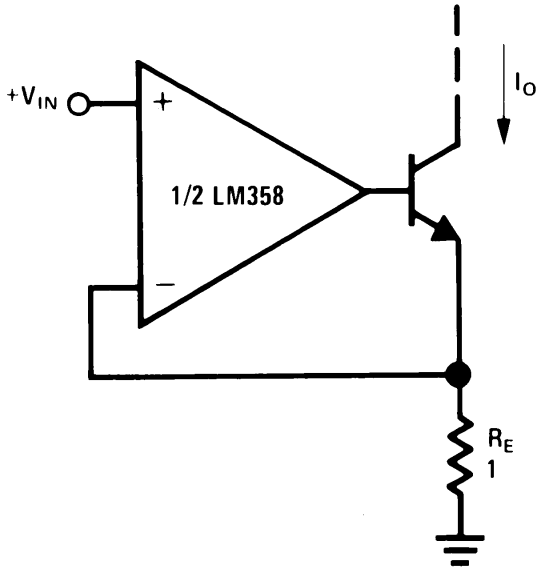


図 8-12. Pulse Generator



HIGH Z_{IN}
LOW Z_{OUT}

図 8-13. Low Drift Peak Detector



I_O = 1 amp/volt V_{IN}
(Increase R_E for I_O small)

図 8-14. High Compliance Current Sink

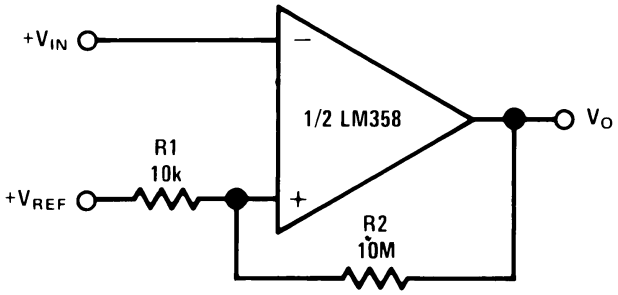
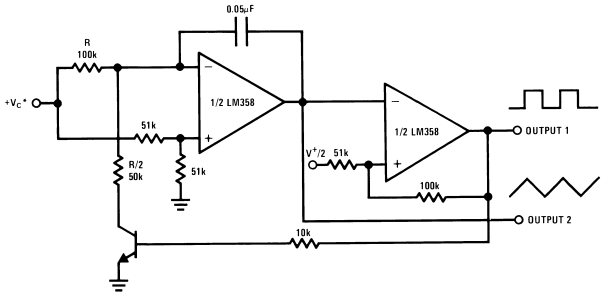


図 8-15. Comparator with Hysteresis



*WIDE CONTROL VOLTAGE RANGE: 0 $V_{DC} \le V_C \le 2$ ($V^+ - 1.5V_{DC}$)

図 8-16. Voltage Controlled Oscillator (VCO)

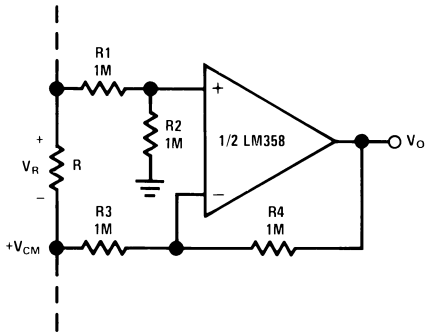
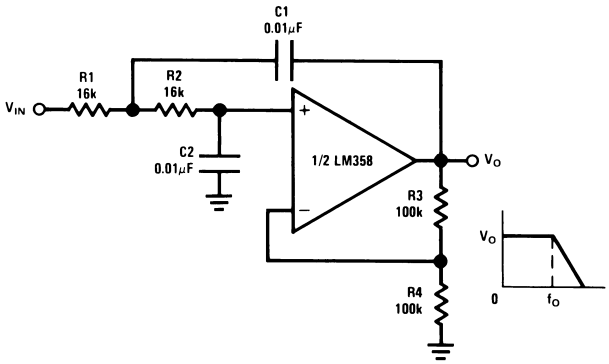
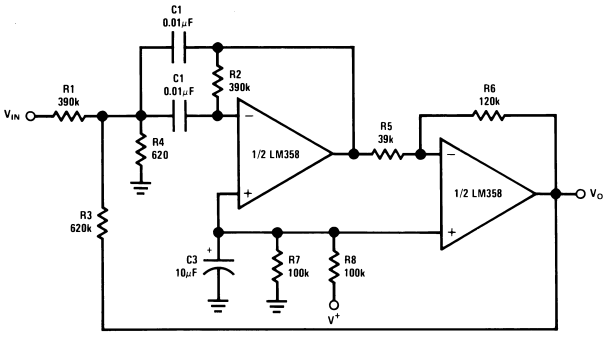


図 8-17. Ground Referencing a Differential Input Signal



f_o = 1 kHz
Q = 1
A_V = 2

図 8-18. DC Coupled Low-Pass RC Active Filter



f_o = 1 kHz
Q = 25

図 8-19. Bandpass Active Filter

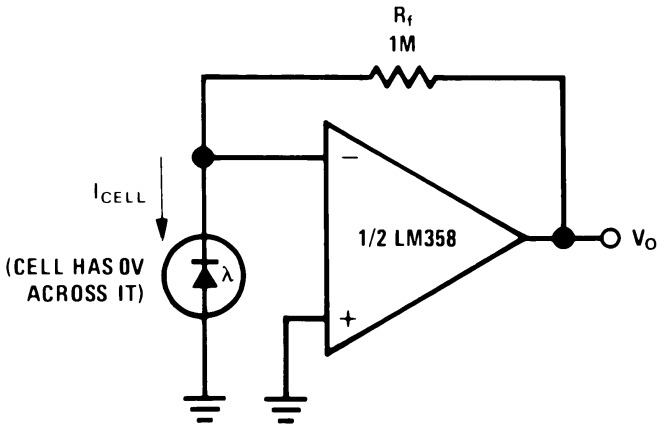


図 8-20. Photo Voltaic-Cell Amplifier

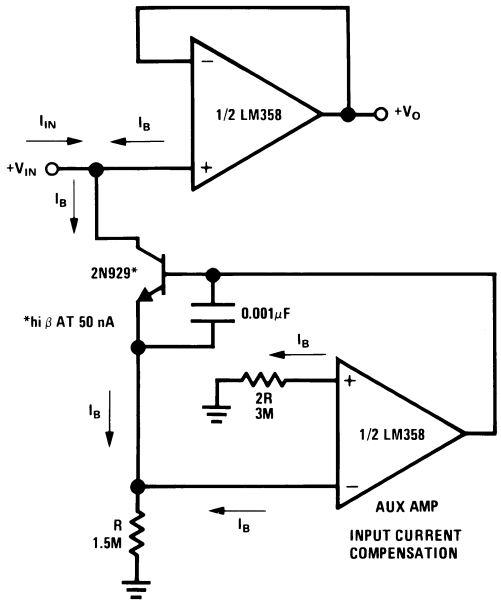
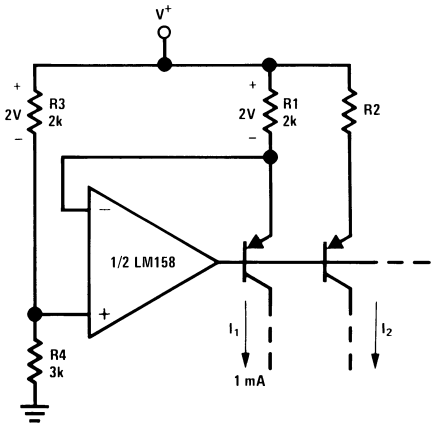


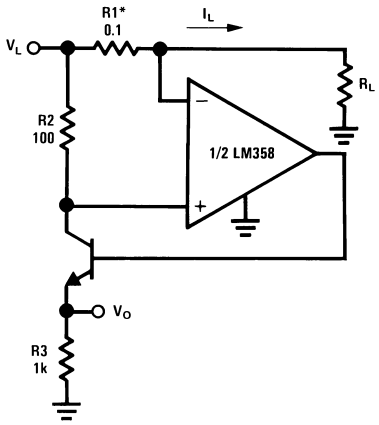
図 8-21. Using Symmetrical Amplifiers to Reduce Input Current (General Concept)

Copyright © 2022 Texas Instruments Incorporated



$$I_2 = \left(\frac{R1}{R2}\right) I_1$$

図 8-22. Fixed Current Sources

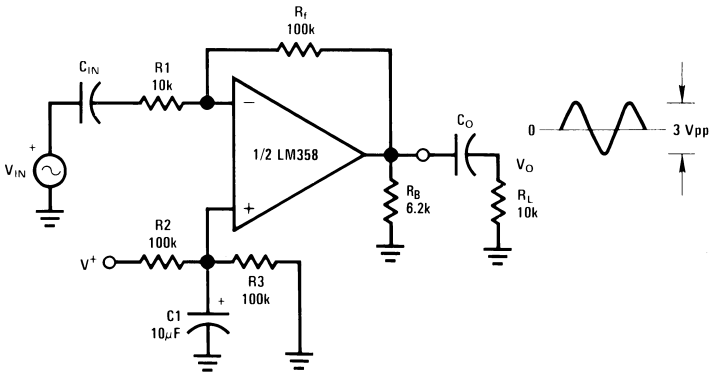


$$V_O = \frac{1V\ (I_L)}{1A}$$

*(Increase R1 for I_L small)

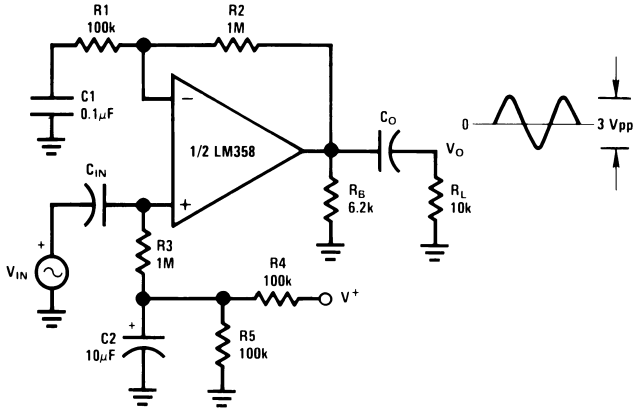
$V_L \leq V^+ - 2V$

図 8-23. Current Monitor



$$A_V = \frac{R_f}{R1} \text{ (As shown, } A_V = 10)$$

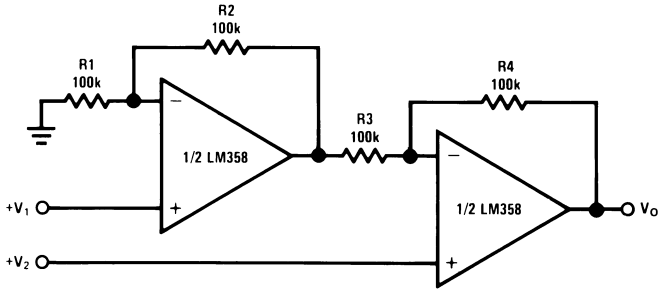
図 8-24. AC Coupled Inverting Amplifier



$$A_V = 1 + \frac{R2}{R1}$$

A_v = 11 (As Shown)

図 8-25. AC Coupled Non-Inverting Amplifier

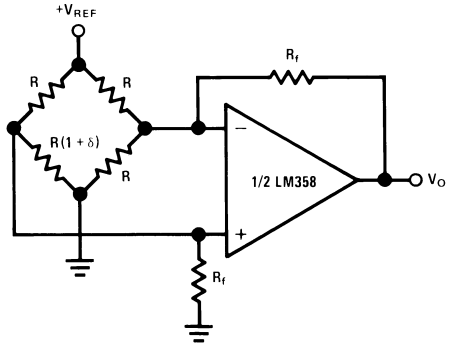


For $\frac{R1}{R2} = \frac{R4}{R3}$ (CMRR depends on this resistor ratio match)

$$V_O = 1 + \frac{R4}{R3}(V_2 - V_1)$$

As Shown: $V_O = 2(V_2 - V_1)$

図 8-26. High Input Z, DC Differential Amplifier

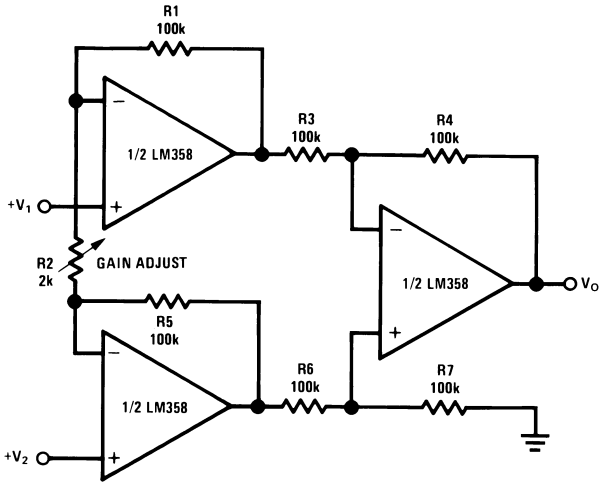


For $\delta << 1$ and $R_f >> R$

$$V_O \cong V_{REF}\left(\frac{\delta}{2}\right)\frac{R_f}{R}$$

図 8-27. Bridge Current Amplifier

Copyright © 2022 Texas Instruments Incorporated



If R1 = R5 & R3 = R4 = R6 = R7 (CMRR depends on match)

$$V_O = 1 + \frac{2R1}{R2}(V_2 - V_1)$$

As shown $V_O = 101 (V_2 - V_1)$

図 8-28. High Input Z Adjustable-Gain DC Instrumentation Amplifier

Copyright © 2022 Texas Instruments Incorporated

9 Power Supply Recommendations

For proper operation, the power supplies must be properly decoupled. For decoupling the supply pins it is suggested that 10-nF capacitors be placed as close as possible to the op-amp power supply pins. For single supply, place a capacitor between V+ and V– supply leads. For dual supplies, place one capacitor between V+ and ground, and one capacitor between V– and ground.

Precautions should be taken to insure that the power supply for the integrated circuit never becomes reversed in polarity or that the unit is not inadvertently installed backwards in a test socket as an unlimited current surge through the resulting forward diode within the IC could cause fusing of the internal conductors and result in a destroyed unit.

10 Layout

10.1 Layout Guidelines

For single-ended supply configurations, the V+ pin should be bypassed to ground with a low ESR capacitor. The optimum placement is closest to the V+ pin. Care should be taken to minimize the loop area formed by the bypass capacitor connection between V+ and ground. The ground pin should be connected to the PCB ground plane at the pin of the device. The feedback components should be placed as close to the device as possible to minimize stray parasitics.

For dual supply configurations, both the V+ pin and V- pin should be bypassed to ground with a low ESR capacitor. The optimum placement is closest to the corresponding supply pin. Care should be taken to minimize the loop area formed by the bypass capacitor connection between V+ or V- and ground. The feedback components should be placed as close to the device as possible to minimize stray parasitics.

For both configurations, as ground plane underneath the device is recommended.

10.2 Layout Example

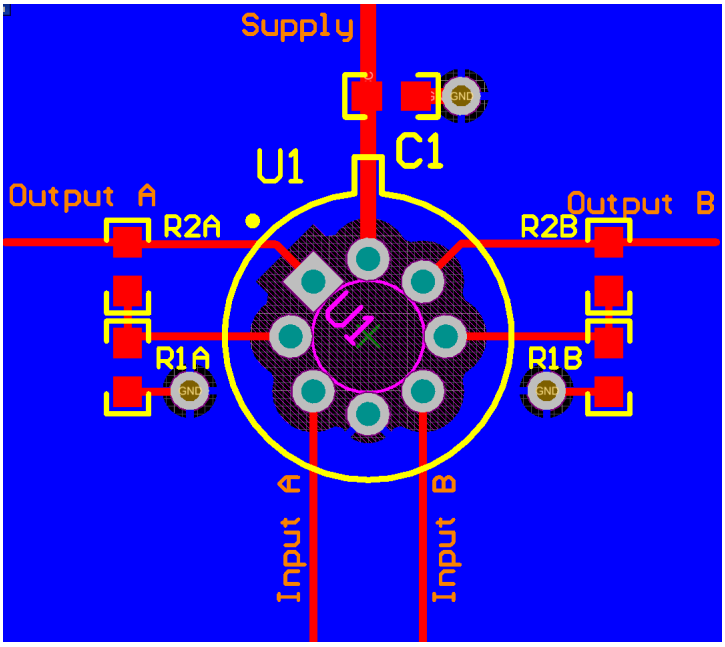


図 10-1. Layout Example

Copyright © 2022 Texas Instruments Incorporated

11 Device and Documentation Support

11.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.2 サポート・リソース

TI E2E™ サポート・フォーラムは、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計で必要な支援を迅速に得ることができます。

リンクされているコンテンツは、該当する貢献者により、現状のまま提供されるものです。これらは TI の仕様を構成するものではなく、必ずしも TI の見解を反映したものではありません。TI の使用条件を参照してください。

11.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.
すべての商標は、それぞれの所有者に帰属します。

11.4 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.5 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

Copyright © 2022 Texas Instruments Incorporated

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LM158AH	Active	Production	TO-99 (LMC) | 8	500 | OTHER	No	Call TI	Level-1-NA-UNLIM	-55 to 125	(LM158AH, LM158AH)
LM158AH/NOPB	Active	Production	TO-99 (LMC) | 8	500 | OTHER	Yes	Call TI	Level-1-NA-UNLIM	-55 to 125	(LM158AH, LM158AH)
LM158H	Active	Production	TO-99 (LMC) | 8	500 | OTHER	No	Call TI	Level-1-NA-UNLIM	-55 to 125	(LM158H, LM158H)
LM158H/NOPB	Active	Production	TO-99 (LMC) | 8	500 | OTHER	Yes	Call TI	Level-1-NA-UNLIM	-55 to 125	(LM158H, LM158H)
LM158J	Active	Production	CDIP (NAB) | 8	40 | TUBE	No	SNPB	Level-1-NA-UNLIM	-55 to 125	LM158J
LM258H	Active	Production	TO-99 (LMC) | 8	500 | OTHER	No	Call TI	Level-1-NA-UNLIM	-25 to 85	(LM258H, LM258H)
LM258H/NOPB	Active	Production	TO-99 (LMC) | 8	500 | TRAY NON-STD	Yes	Call TI	Level-1-NA-UNLIM	-25 to 85	(LM258H, LM258H)
LM2904ITP/NOPB	Active	Production	DSBGA (YPB) | 8	250 | SMALL T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	A 09
LM2904ITP/NOPB.B	Active	Production	DSBGA (YPB) | 8	250 | SMALL T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	A 09
LM2904ITPX/NOPB	Active	Production	DSBGA (YPB) | 8	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	A 09
LM2904ITPX/NOPB.B	Active	Production	DSBGA (YPB) | 8	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	A 09
LM2904M/NOPB	Active	Production	SOIC (D) | 8	95 | TUBE	Yes	SN	Level-1-260C-UNLIM	-40 to 85	LM 2904M
LM2904M/NOPB.B	Active	Production	SOIC (D) | 8	95 | TUBE	Yes	SN	Level-1-260C-UNLIM	-40 to 85	LM 2904M
LM2904MX/NOPB	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	LM 2904M
LM2904MX/NOPB.B	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	LM 2904M
LM2904N/NOPB	Active	Production	PDIP (P) | 8	40 | TUBE	Yes	NIPDAU	Level-1-NA-UNLIM	-40 to 85	LM 2904N
LM2904N/NOPB.B	Active	Production	PDIP (P) | 8	40 | TUBE	Yes	NIPDAU	Level-1-NA-UNLIM	-40 to 85	LM 2904N
LM358AM/NOPB	Active	Production	SOIC (D) | 8	95 | TUBE	Yes	SN	Level-1-260C-UNLIM	0 to 70	LM 358AM
LM358AM/NOPB.B	Active	Production	SOIC (D) | 8	95 | TUBE	Yes	SN	Level-1-260C-UNLIM	0 to 70	LM 358AM

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LM358AMX/NOPB	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	0 to 70	LM 358AM
LM358AMX/NOPB.B	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	0 to 70	LM 358AM
LM358AN/NOPB	Active	Production	PDIP (P) | 8	40 | TUBE	Yes	NIPDAU	Level-1-NA-UNLIM	0 to 70	LM 358AN
LM358AN/NOPB.B	Active	Production	PDIP (P) | 8	40 | TUBE	Yes	NIPDAU	Level-1-NA-UNLIM	0 to 70	LM 358AN
LM358H/NOPB	Active	Production	TO-99 (LMC) | 8	500 | TUBE	Yes	Call TI	Level-1-NA-UNLIM	0 to 70	(LM358H, LM358H)
LM358H/NOPB.B	Active	Production	TO-99 (LMC) | 8	500 | TUBE	Yes	Call TI	Level-1-NA-UNLIM	0 to 70	(LM358H, LM358H)
LM358M/NOPB	Active	Production	SOIC (D) | 8	95 | TUBE	Yes	SN	Level-1-260C-UNLIM	0 to 70	LM 358M
LM358M/NOPB.B	Active	Production	SOIC (D) | 8	95 | TUBE	Yes	SN	Level-1-260C-UNLIM	0 to 70	LM 358M
LM358MX/NOPB	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	0 to 70	LM 358M
LM358MX/NOPB.B	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	0 to 70	LM 358M
LM358N/NOPB	Active	Production	PDIP (P) | 8	40 | TUBE	Yes	NIPDAU	Level-1-NA-UNLIM	0 to 70	LM 358N
LM358N/NOPB.B	Active	Production	PDIP (P) | 8	40 | TUBE	Yes	NIPDAU	Level-1-NA-UNLIM	0 to 70	LM 358N
LM358TP/NOPB	Active	Production	DSBGA (YPB) | 8	250 | SMALL T&R	Yes	SNAGCU	Level-1-260C-UNLIM	0 to 70	A 07
LM358TP/NOPB.B	Active	Production	DSBGA (YPB) | 8	250 | SMALL T&R	Yes	SNAGCU	Level-1-260C-UNLIM	0 to 70	A 07
LM358TPX/NOPB	Active	Production	DSBGA (YPB) | 8	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	0 to 70	A 07
LM358TPX/NOPB.B	Active	Production	DSBGA (YPB) | 8	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	0 to 70	A 07

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF LM2904-N :

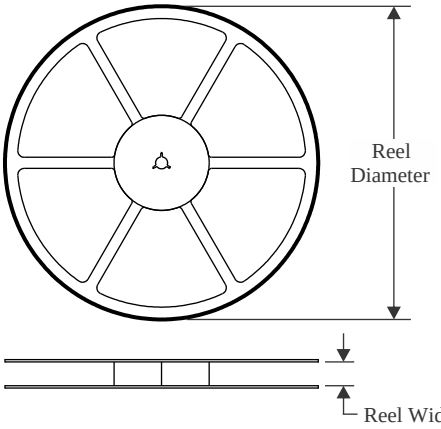
- Automotive : LM2904-Q1
- Enhanced Product : LM2904-EP

NOTE: Qualified Version Definitions:

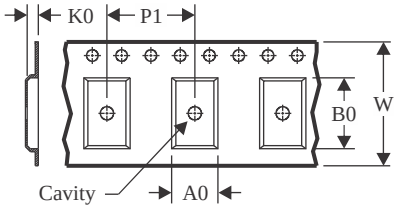
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

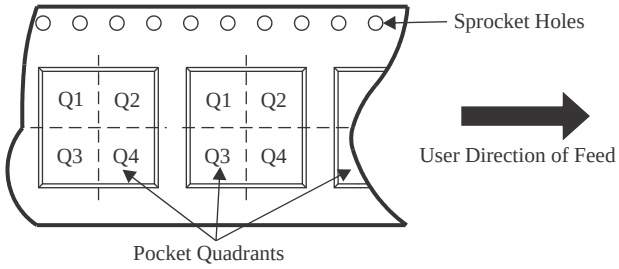


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

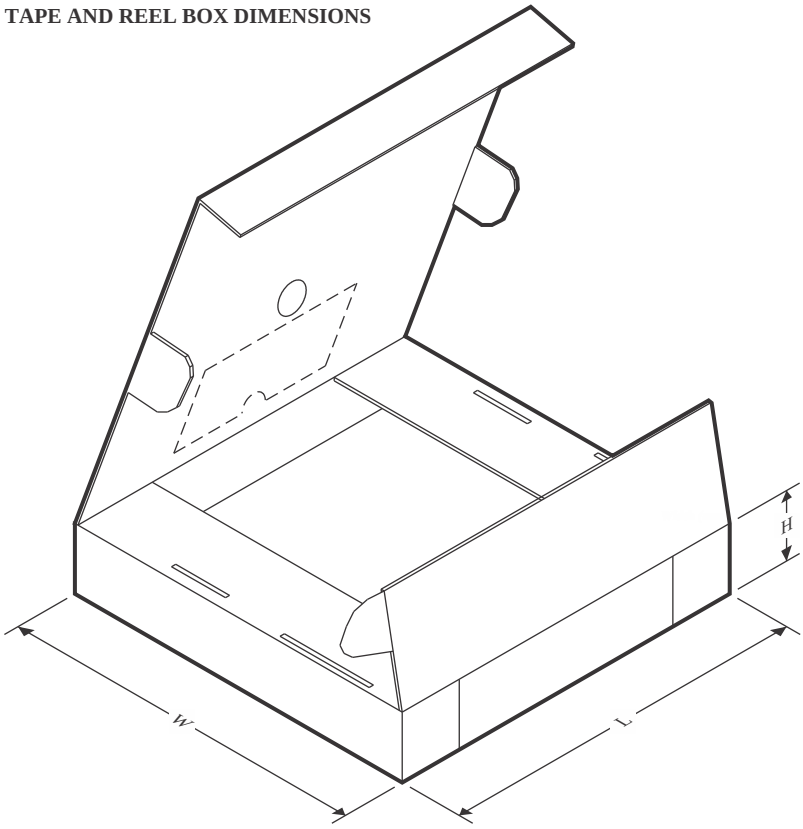
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM2904ITP/NOPB	DSBGA	YPB	8	250	178.0	8.4	1.5	1.5	0.66	4.0	8.0	Q1
LM2904ITPX/NOPB	DSBGA	YPB	8	3000	178.0	8.4	1.5	1.5	0.66	4.0	8.0	Q1
LM2904MX/NOPB	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM358AMX/NOPB	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM358MX/NOPB	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM358TP/NOPB	DSBGA	YPB	8	250	178.0	8.4	1.5	1.5	0.66	4.0	8.0	Q1
LM358TPX/NOPB	DSBGA	YPB	8	3000	178.0	8.4	1.5	1.5	0.66	4.0	8.0	Q1

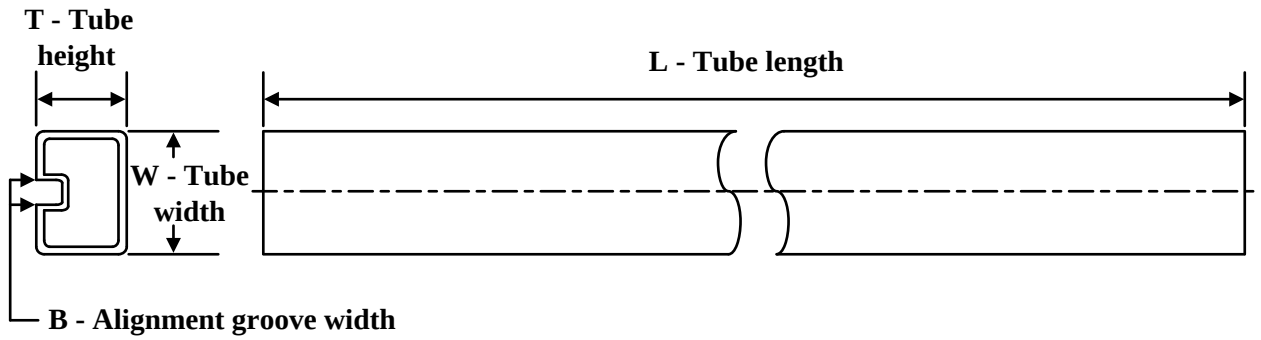
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM2904ITP/NOPB	DSBGA	YPB	8	250	208.0	191.0	35.0
LM2904ITPX/NOPB	DSBGA	YPB	8	3000	208.0	191.0	35.0
LM2904MX/NOPB	SOIC	D	8	2500	367.0	367.0	35.0
LM358AMX/NOPB	SOIC	D	8	2500	367.0	367.0	35.0
LM358MX/NOPB	SOIC	D	8	2500	367.0	367.0	35.0
LM358TP/NOPB	DSBGA	YPB	8	250	208.0	191.0	35.0
LM358TPX/NOPB	DSBGA	YPB	8	3000	208.0	191.0	35.0

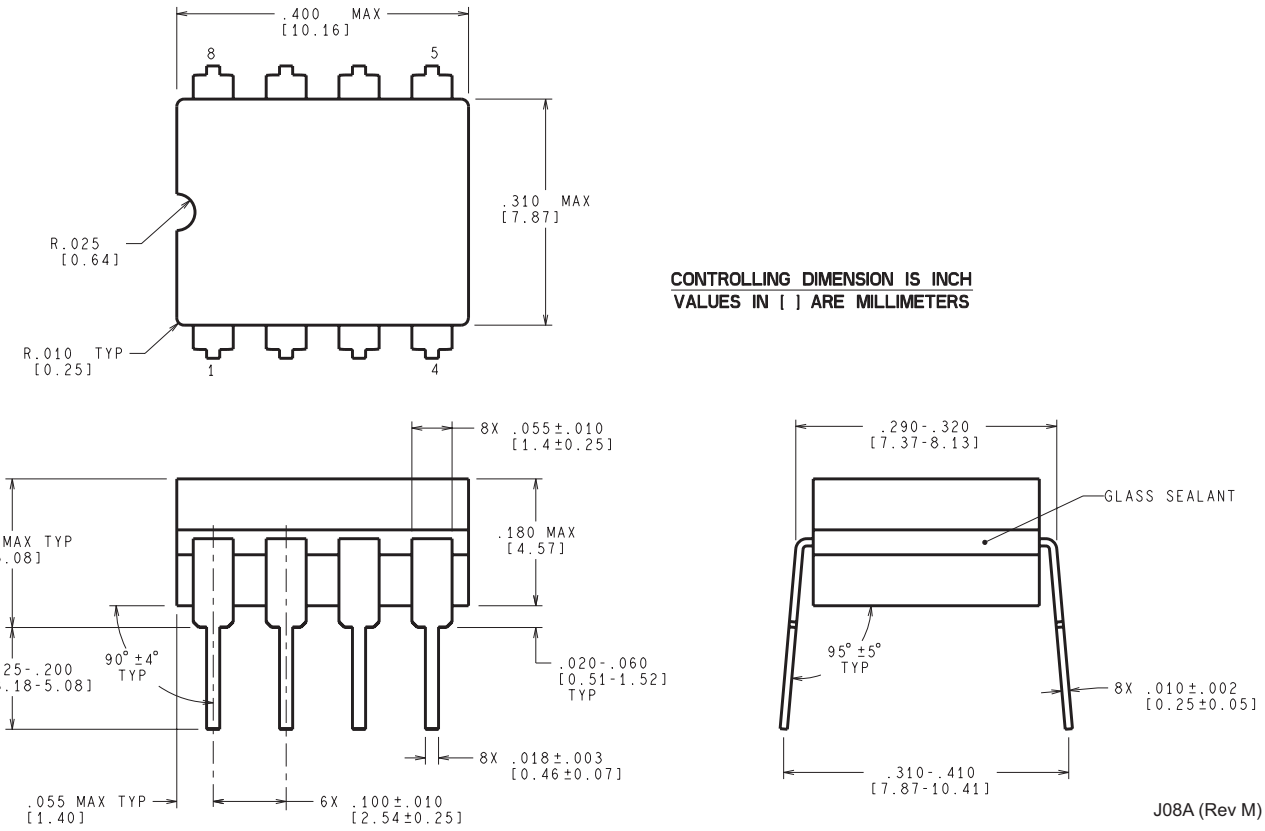
TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
LM158J	NAB	CDIP	8	40	502	14	11938	4.32
LM2904M/NOPB	D	SOIC	8	95	495	8	4064	3.05
LM2904M/NOPB.B	D	SOIC	8	95	495	8	4064	3.05
LM2904N/NOPB	P	PDIP	8	40	502	14	11938	4.32
LM2904N/NOPB.B	P	PDIP	8	40	502	14	11938	4.32
LM358AM/NOPB	D	SOIC	8	95	495	8	4064	3.05
LM358AM/NOPB.B	D	SOIC	8	95	495	8	4064	3.05
LM358AN/NOPB	P	PDIP	8	40	502	14	11938	4.32
LM358AN/NOPB.B	P	PDIP	8	40	502	14	11938	4.32
LM358M/NOPB	D	SOIC	8	95	495	8	4064	3.05
LM358M/NOPB.B	D	SOIC	8	95	495	8	4064	3.05
LM358N/NOPB	P	PDIP	8	40	502	14	11938	4.32
LM358N/NOPB.B	P	PDIP	8	40	502	14	11938	4.32

NAB0008A

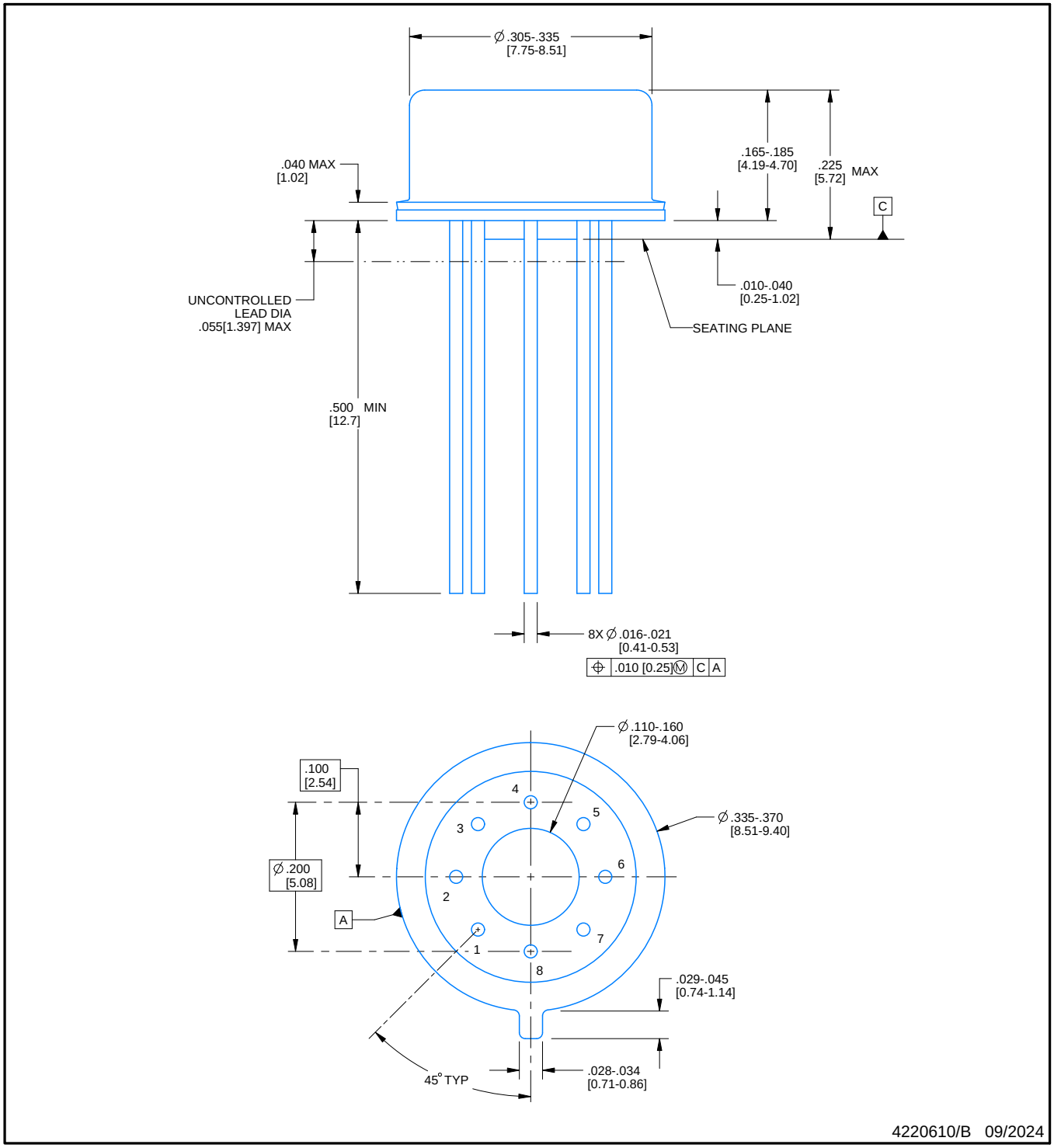

.400 MAX
[10.16]
8
5
.310 MAX
[7.87]
R.025
[0.64]
R.010 TYP
[0.25]
1
4
CONTROLLING DIMENSION IS INCH
VALUES IN [ ] ARE MILLIMETERS
8X .055±.010
[1.4±0.25]
.200 MAX TYP
[5.08]
.180 MAX
[4.57]
8X .125-.200
[3.18-5.08]
90° ±4°
TYP
.020-.060
[0.51-1.52]
TYP
8X .018±.003
[0.46±0.07]
.055 MAX TYP
[1.40]
6X .100±.010
[2.54±0.25]
.290-.320
[7.37-8.13]
GLASS SEALANT
95° ±5°
TYP
8X .010±.002
[0.25±0.05]
.310-.410
[7.87-10.41]
J08A (Rev M)

PACKAGE OUTLINE

LMC0008A

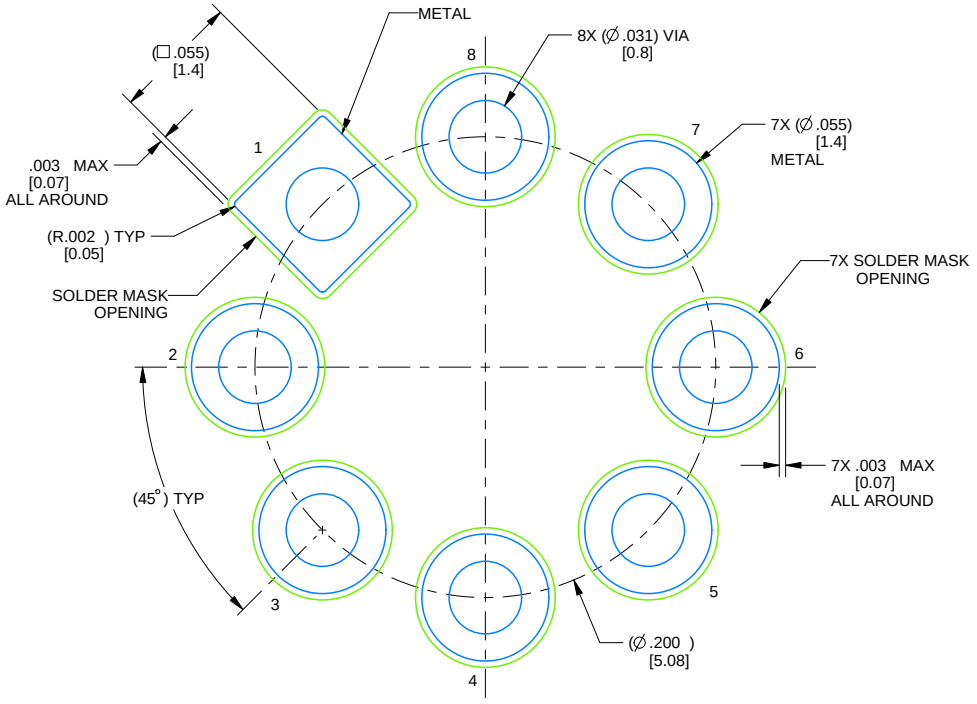
TO-CAN - 5.72 mm max height

TRANSISTOR OUTLINE



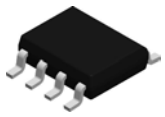
NOTES:

1. All linear dimensions are in inches [millimeters]. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Pin numbers shown for reference only. Numbers may not be marked on package.
4. Reference JEDEC registration MO-002/TO-99.



LAND PATTERN EXAMPLE
NON-SOLDER MASK DEFINED
SCALE: 12X

4220610/B 09/2024

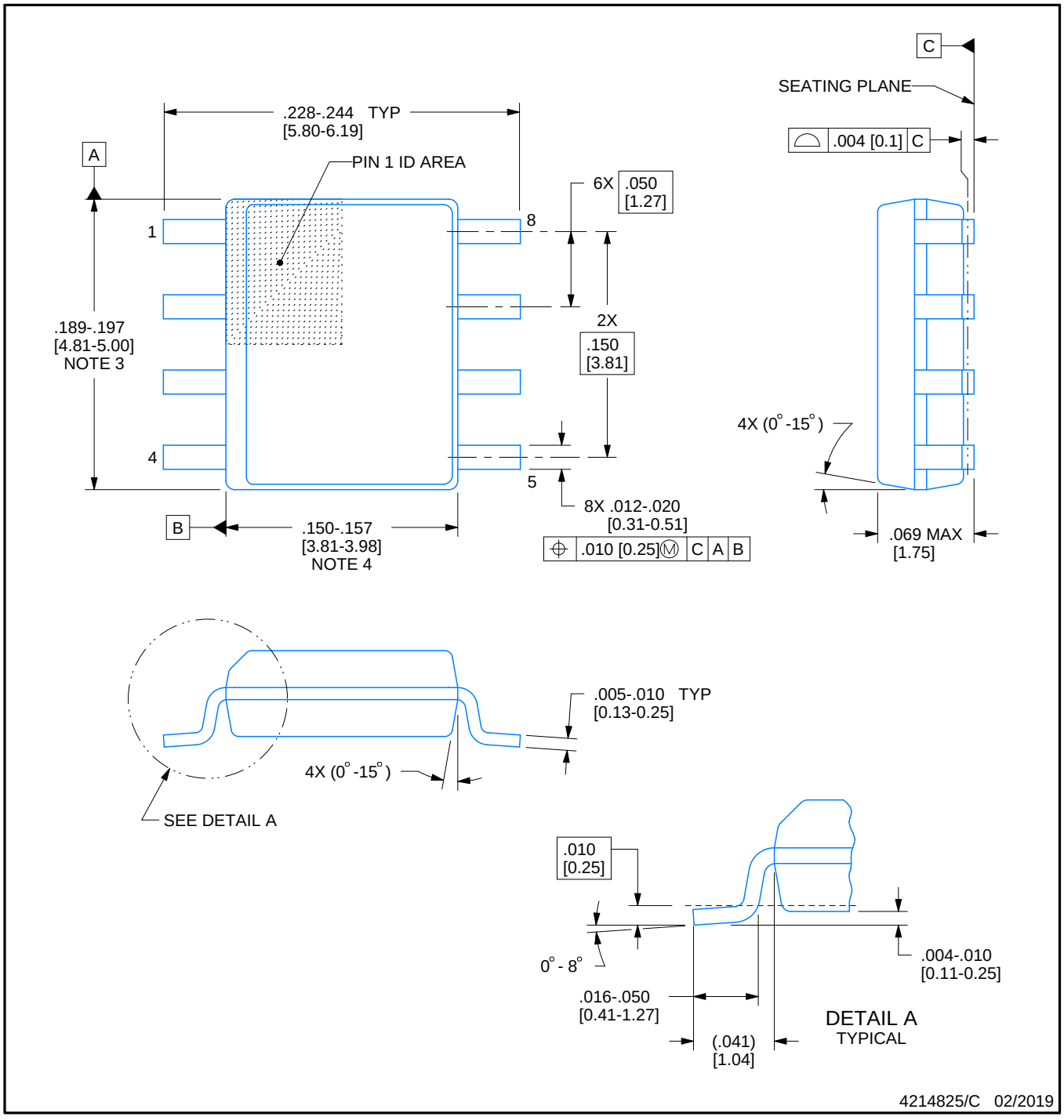


PACKAGE OUTLINE

D0008A

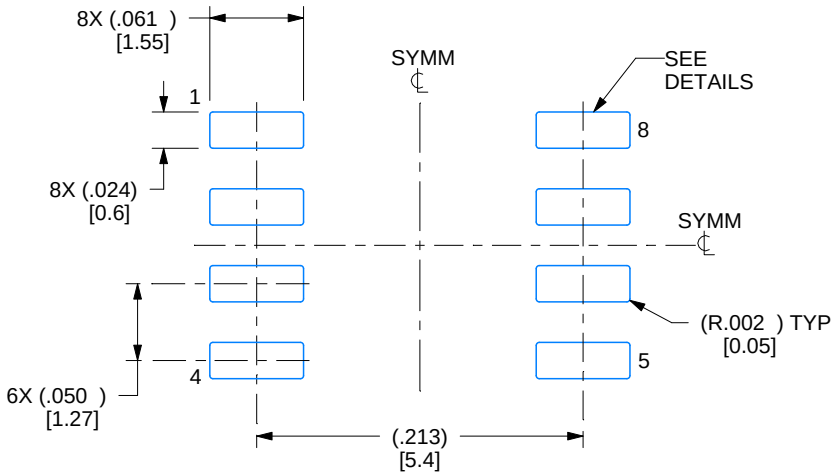
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

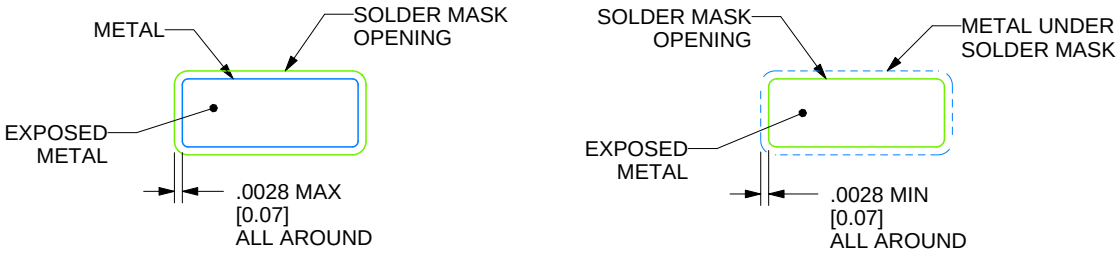


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

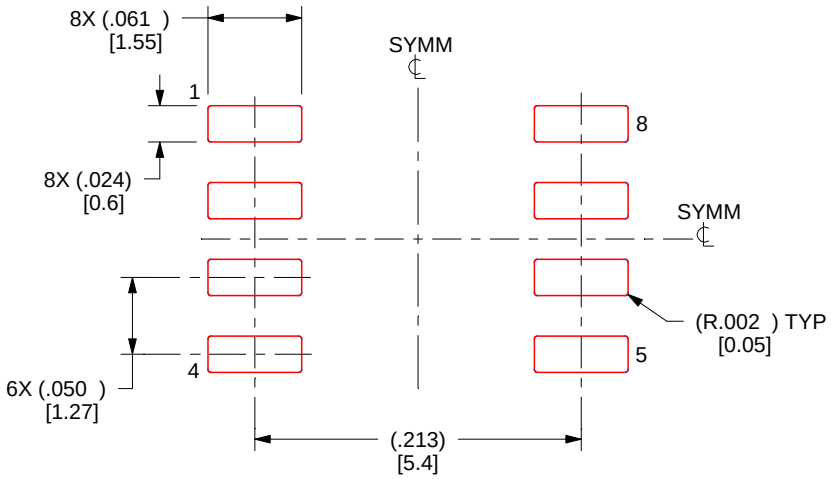
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



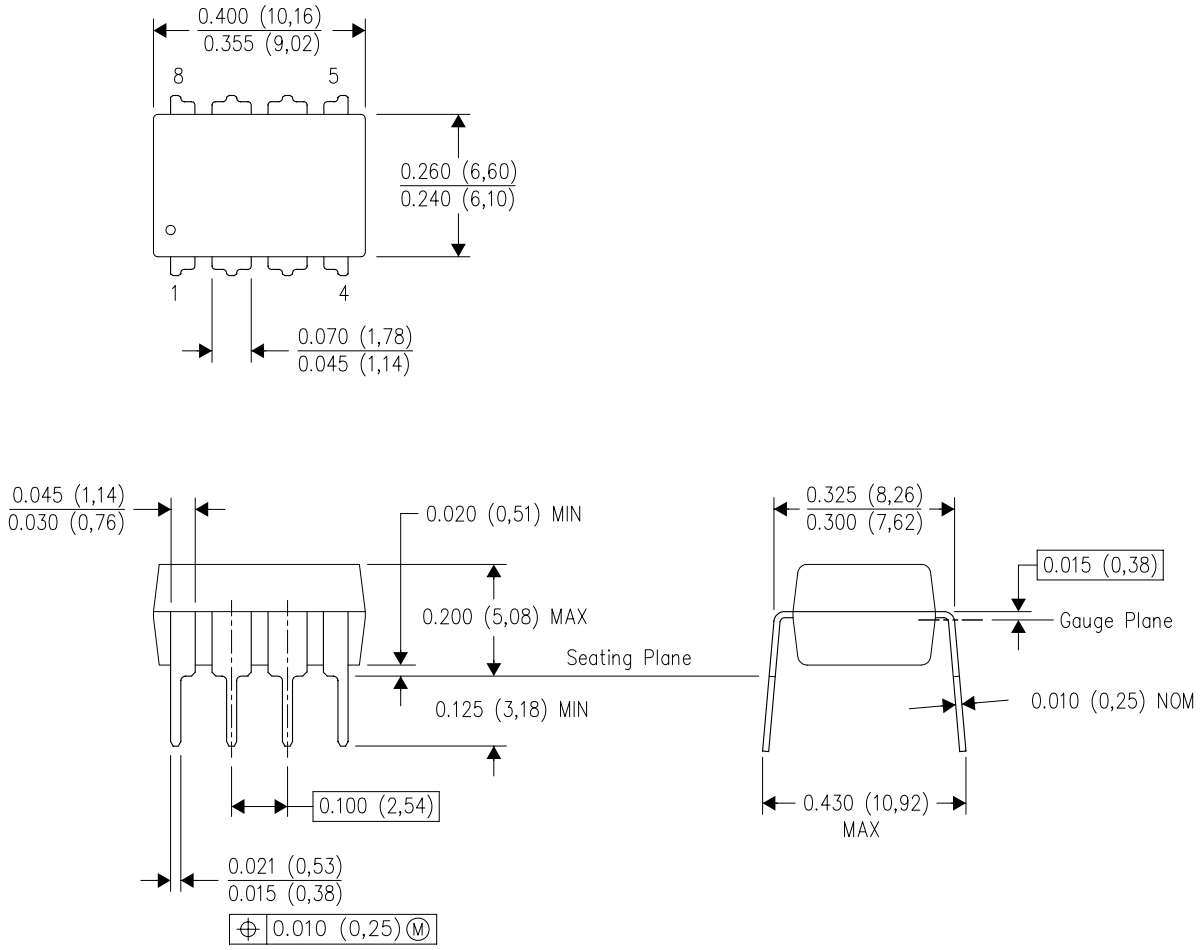
SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

P (R–PDIP–T8) PLASTIC DUAL–IN–LINE PACKAGE



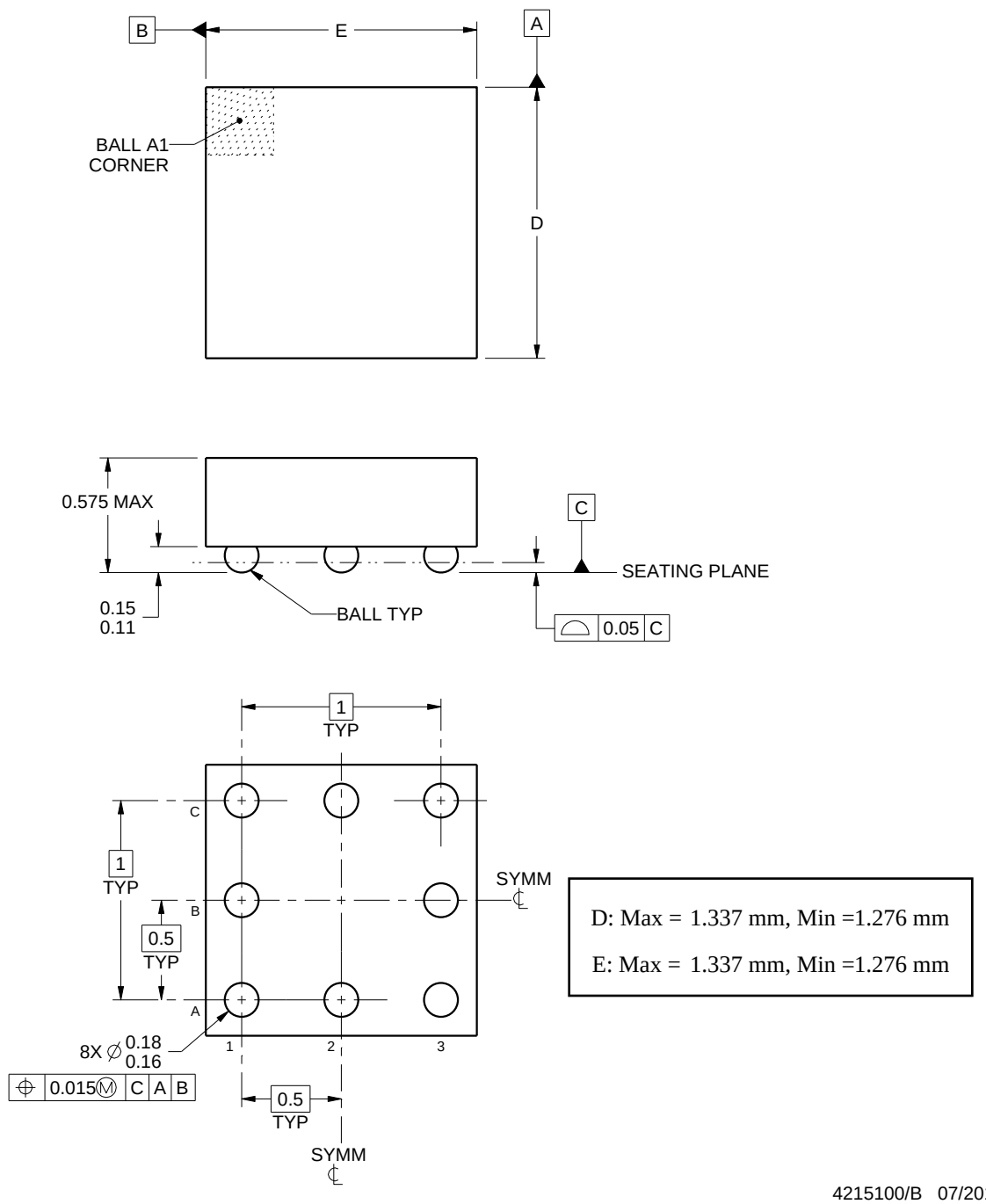
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001 variation BA.

PACKAGE OUTLINE

YPB0008

DSBGA - 0.575 mm max height

DIE SIZE BALL GRID ARRAY



NOTES:

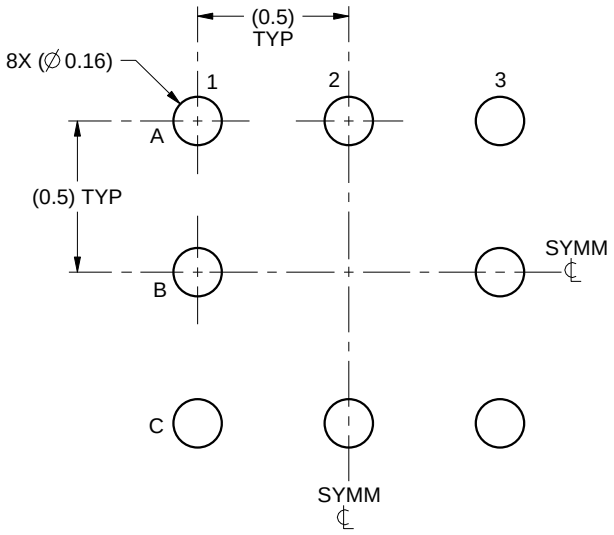
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

EXAMPLE BOARD LAYOUT

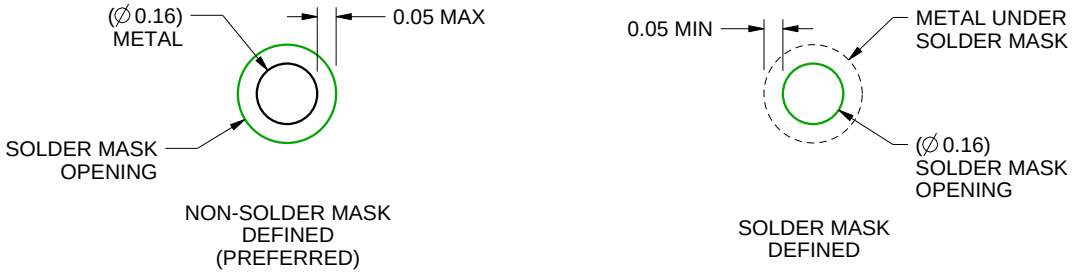
YPB0008

DSBGA - 0.575 mm max height

DIE SIZE BALL GRID ARRAY



LAND PATTERN EXAMPLE
SCALE:40X

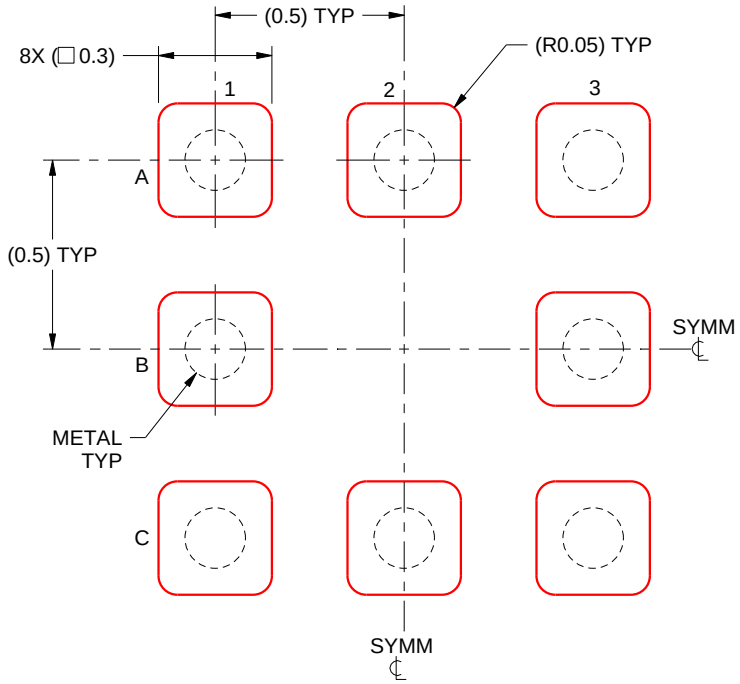


SOLDER MASK DETAILS
NOT TO SCALE

4215100/B 07/2016

NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints.
   See Texas Instruments Literature No. SNVA009 (www.ti.com/lit/snva009).



SOLDER PASTE EXAMPLE
BASED ON 0.125mm THICK STENCIL
SCALE:50X

4215100/B 07/2016

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

重要なお知らせと免責事項

TI は、技術データと信頼性データ (データシートを含みます)、設計リソース (リファレンス デザインを含みます)、アプリケーションや設計に関する各種アドバイス、Web ツール、安全性情報、その他のリソースを、欠陥が存在する可能性のある「現状のまま」提供しており、商品性および特定目的に対する適合性の黙示保証、第三者の知的財産権の非侵害保証を含むいかなる保証も、明示的または黙示的にかかわらず拒否します。

これらのリソースは、TI 製品を使用する設計の経験を積んだ開発者への提供を意図したものです。(1) お客様のアプリケーションに適した TI 製品の選定、(2) お客様のアプリケーションの設計、検証、試験、(3) お客様のアプリケーションに該当する各種規格や、その他のあらゆる安全性、セキュリティ、規制、または他の要件への確実な適合に関する責任を、お客様のみが単独で負うものとします。

上記の各種リソースは、予告なく変更される可能性があります。これらのリソースは、リソースで説明されている TI 製品を使用するアプリケーションの開発の目的でのみ、TI はその使用をお客様に許諾します。これらのリソースに関して、他の目的で複製することや掲載することは禁止されています。TI や第三者の知的財産権のライセンスが付与されている訳ではありません。お客様は、これらのリソースを自身で使用した結果発生するあらゆる申し立て、損害、費用、損失、責任について、TI およびその代理人を完全に補償するものとし、TI は一切の責任を拒否します。

TI の製品は、 TI の販売条件 、 TI の総合的な品質ガイドライン 、 ti.com または TI 製品などに関連して提供される他の適用条件に従い提供されます。TI がこれらのリソースを提供することは、適用される TI の保証または他の保証の放棄の拡大や変更を意味するものではありません。 TI がカスタム、またはカスタマー仕様として明示的に指定していない限り、TI の製品は標準的なカタログに掲載される汎用機器です。

お客様がいかなる追加条項または代替条項を提案する場合も、TI はそれらに異議を唱え、拒否します。

Copyright © 2026, Texas Instruments Incorporated

最終更新日：2025 年 10 月