LM46002 3.5V～60V、2A の同期整流降圧型電圧コンバータ

1 特長

- レギュレーション時の静止電流：27μA
- 軽負荷時の高効率 (DCM および PFM)
- EN55022/CISPR 22 EMI 標準に準拠
- 同期整流回路を内蔵
- 可変周波数範囲：200kHz～2.2MHz (デフォルト：500kHz)
- 外部クロックへの周波数同期
- 内部補償
- 各種コンデンサ (セラミック、ポリマー、タンタル、アルミ) のほとんどの組み合わせで安定動作
- パワー・グッド・フラグ
- プリバイアスされた負荷へのソフトスタート
- 内部ソフト・スタート：4.1ms
- 外付けコンデンサによってソフト・スタート時間を延長可能
- 出力電圧トラッキング制御機能
- 高精度のイネーブルによりシステム UVLO をプログラム
- ヒカップ・モードによる出力短絡保護
- 過熱時のサーマル・シャットダウン保護
- WEBENCH® Power Designer により、LM46002 を使用するカスタム設計を作成

2 アプリケーション

- 産業用電源
- 通信システム
- Sub-AM 帯域の車載機器
- 民生用車載電源
- 汎用の広い V_{IN} のレギュレーション
- 高効率のポイント・オブ・ロード・レギュレーション

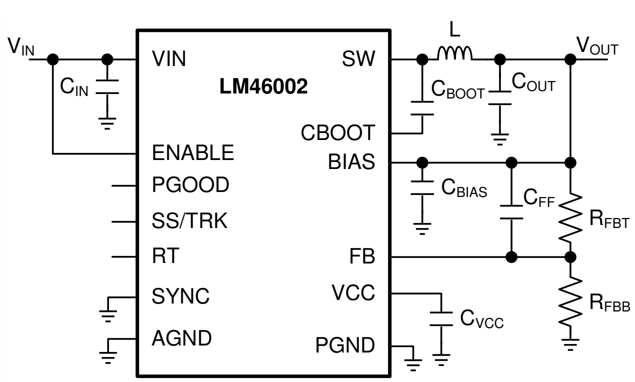
3 概要

LM46002 レギュレータは、3.5V～60V の範囲の入力電圧から最大 2A の負荷電流を駆動できる、使いやすい同期整流降圧型 DC/DC コンバータです。LM46002 はごく小さなソリューション・サイズで、非常に高い効率、出力精度、低いドロップアウト電圧を実現します。36V の最大入力電圧に対応し各種負荷電流の選択肢を取りそろえた広範なファミリ (例：LM46001、LM46000、LM43603、LM43602、LM43601、LM43600) をピン互換パッケージで提供しています。ピーク電流モード制御の採用により、単純な制御ループ補償と、サイクル単位の電流制限が実現されています。オプション機能として、プログラム可能なスイッチング周波数、同期、パワー・グッド・フラグ、高精度のイネーブル、内部ソフト・スタート、延長可能なソフト・スタート、トラッキングなどの機能があり、広範なアプリケーション向けの柔軟で使いやすいプラットフォームとなります。不連続導通と周波数自動低減によって、軽負荷時の効率を向上させています。このファミリは、わずかな外付け部品のみで動作します。単純で最適な PCB レイアウトが可能になるよう、ピン配置が設計されています。保護機能として、サーマル・シャットダウン、V_{CC} 低電圧誤動作防止、サイクル単位の電流制限、出力短絡保護が搭載されています。LM46002 デバイスは、リード・ピッチ 0.65mm の16 リード HTSSOP/PWP パッケージ (6.6mm × 5.1mm × 1.2mm) で供給されます。

製品情報

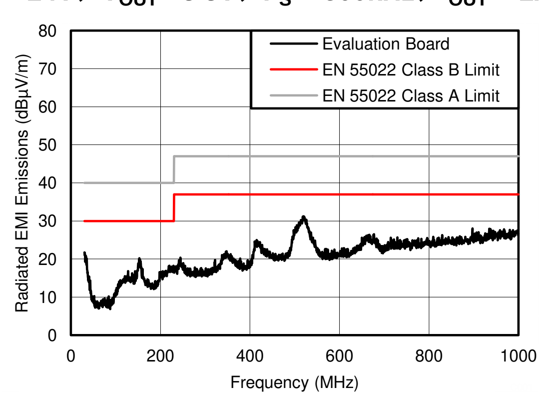
型番	パッケージ	本体サイズ
LM46002	HTSSOP (16)	6.60mm×5.10mm

概略回路図



放射エミッションのグラフ

V_{IN} = 24V、V_{OUT} =3.3V、F_S = 500kHz、I_{OUT} = 2A



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4 改訂履歴

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Revision B (September 2014) から **Revision C** に変更 **Page**

- 最新のドキュメント標準に合わせて編集上の変更、WEBENCH へのリンクと TI Design の上部ナビゲーション・アイコンを 追加 1
- Changed *Handling Ratings* to *ESD Ratings* ; move Storage temperature to *Abs Max* table ... 4
- Deleted "T_J = –40°C to 85°C" row from V_{FB} ... 6
- Changed I_{SSC} min from 1.45 µA to 1.17 µA and typ from 2.2 µA to 2 µA ... 6
- Changed R_{PGOOD}, V_{EN} = 3.3 V: typ from 40 Ω to 69 Ω and max from 125 Ω to 150 Ω ... 6
- Changed R_{PGOOD}, V_{EN} = 0: typ from 60 Ω to 150 Ω and max from 150 Ω to 350 Ω ... 6
- Changed Equation 16 to add "/ 2" ... 28
- 追加 「*ドキュメントの更新通知を受け取る方法*」および「*コミュニティ・リソース*」 ... 44

Revision A (April 2014) から **Revision B** に変更 **Page**

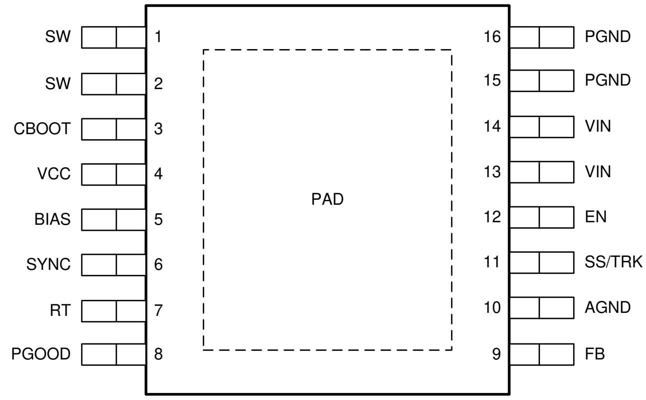
- Changed this graph ... 12
- Added this equation ... 30
- Added this equation ... 30
- Changed this graph ... 31
- Changed this graph ... 35
- Changed this graph ... 35
- Changed this graph ... 36
- Changed this graph ... 43

2014年4月発行のものから更新 **Page**

- デバイスを「製品プレビュー」から「量産データ」に 変更 ... 1

5 Pin Configuration and Functions

PWP Package
16-Pin HTSSOP With PowerPAD™
Top View



Pin Functions

PIN		TYPE (1)	DESCRIPTION
NO.	NAME		
1,2	SW	P	Switching output of the regulator. Internally connected to both power MOSFETs. Connect to power inductor.
3	CBOOT	P	Boot-strap capacitor connection for high-side driver. Connect a high-quality 470-nF capacitor from CBOOT to SW.
4	VCC	P	Internal bias supply output for bypassing. Connect bypass capacitor from this pin to AGND. Do not connect external load to this pin. Never short this pin to ground during operation.
5	BIAS	P	Optional internal LDO supply input. To improve efficiency, TI recommends tying to V_{OUT} when 3.3 V ≤ V_{OUT} ≤ 28 V or tie to an external 3.3-V or 5-V rail if available. When used, place a bypass capacitor (1 to 10 µF) from this pin to ground. Tie to ground when not in use.
6	SYNC	A	Clock input to synchronize switching action to an external clock. Use proper high-speed termination to prevent ringing. Connect to ground if not used.
7	RT	A	Connect a resistor R_T from this pin to AGND to program switching frequency. Leave floating for 500-kHz default switching frequency.
8	PGOOD	A	Open drain output for power-good flag. Use a 10-kΩ to 100-kΩ pullup resistor to logic rail or other DC voltage no higher than 12 V.
9	FB	A	Feedback sense input pin. Connect to the midpoint of feedback divider to set V_{OUT}. Do not short this pin to ground during operation.
10	AGND	G	Analog ground pin. Ground reference for internal references and logic. Connect to system ground.
11	SS/TRK	A	Soft-start control pin. Leave floating for internal soft-start slew rate. Connect to a capacitor to extend soft start time. Connect to external voltage ramp for tracking.
12	EN	A	Enable input to the LM46002: High = ON and Low = OFF. Connect to VIN, or to VIN through resistor divider, or to an external voltage or logic source. Do not float.
13,14	VIN	P	Supply input pins to internal LDO and high side power FET. Connect to power supply and bypass capacitors C_{IN}. Path from VIN pin to high frequency bypass C_{IN} and PGND must be as short as possible.
15,16	PGND	G	Power ground pins, connected internally to the low side power FET. Connect to system ground, PAD, AGND, ground pins of C_{IN} and C_{OUT}. Path to C_{IN} must be as short as possible.
—	PAD	—	Low impedance connection to AGND. Connect to PGND on PCB. Major heat dissipation path of the die. Must be used for heat sinking to ground plane on PCB.

(1) P = Power, G = Ground, A = Analog

6 Specifications

6.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Input voltages	VIN to PGND	–0.3	65	V
	EN to PGND	–0.3	V_{IN} + 0.3	
	FB, RT, SS/TRK to AGND	–0.3	3.6	
	PGOOD to AGND	–0.3	15	
	SYNC to AGND	–0.3	5.5	
	BIAS to AGND	–0.3	30	
	AGND to PGND	–0.3	0.3	
Output voltages	SW to PGND	–0.3	V_{IN} + 0.3	V
	SW to PGND less than 10-ns transients	–3.5	65	
	CBOOT to SW	–0.3	5.5	
	VCC to AGND	–0.3	3.6	
Storage temperature range, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

see(1)

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(2)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(3)	±500	

(1) ESD testing is performed according to the respective JESD22 JEDEC standard.
(2) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(3) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. .

6.3 Recommended Operating Conditions

Over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Input voltages	VIN to PGND	3.5	60	V
	EN	–0.3	V_{IN}	
	FB	–0.3	1.1	
	PGOOD	–0.3	12	
	BIAS input not used	–0.3	0.3	
	BIAS input used	3.3	28	
	AGND to PGND	–0.1	0.1	
Output voltage	V_{OUT}	1	28	V
Output current	I_{OUT}	0	2	A
Temperature	Operating junction temperature range, T_J	–40	125	°C

(1) Recommended Operating Ratings indicate conditions for which the device is intended to be functional, but do not ensure specific performance limits. For specified specifications, see *Electrical Characteristics*.

6.4 Thermal Information

THERMAL METRIC(1)(2)		LM46002 PWP (HTSSOP) 16 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	38.9(3)	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	24.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	19.9	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.7	°C/W
ψ_{JB}	Junction-to-board characterization parameter	19.7	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	1.7	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.
(2) The package thermal impedance is calculated in accordance with JESD 51-7 standard with a 4-layer board and 2 W power dissipation.
(3) $R_{\theta JA}$ is highly related to PCB layout and heat sinking. See Figure 101 for measured $R_{\theta JA}$ vs PCB area from a 2-layer board and a 4-layer board.

6.5 Electrical Characteristics

Limits apply over the recommended operating junction temperature (T_J) range of –40°C to +125°C, unless otherwise stated. Minimum and Maximum limits are specified through test, design or statistical correlation. Typical values represent the most likely parametric norm at T_J = 25°C, and are provided for reference purposes only. Unless otherwise stated, the following conditions apply: V_{IN} = 24 V, V_{OUT} = 3.3 V, F_S = 500 kHz.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY VOLTAGE (VIN PINS)						
$I_{SHDN}V_{IN-MIN-ST}$	Minimum input voltage for start-up				3.8	V
	Shutdown quiescent current	V_{EN} = 0 V		2.3	5	µA
$I_{Q-NONSW}$	Operating quiescent current (non-switching) from V_{IN}	V_{EN} = 3.3 V V_{FB} = 1.5 V V_{BIAS} = 3.4 V external		7	12	µA
$I_{BIAS-NONSW}$	Operating quiescent current (non-switching) from external V_{BIAS}	V_{EN} = 3.3 V V_{FB} = 1.5 V V_{BIAS} = 3.4 V external		87	135	µA
I_{Q-SW}	Operating quiescent current (switching)	V_{EN} = V_{IN} I_{OUT} = 0 A R_T = open V_{BIAS} = V_{OUT} = 3.3 V R_{FBT} = 1 Meg		27		µA
ENABLE (EN PIN)						
$V_{EN-VCC-H}$	Voltage level to enable the internal LDO output V_{CC}	V_{ENABLE} high level	1.2			V
$V_{EN-VCC-L}$	Voltage level to disable the internal LDO output V_{CC}	V_{ENABLE} low level			0.4	V
$V_{EN-VOUT-H}$	Precision enable level for switching and regulator output: V_{OUT}	V_{ENABLE} high level	2	2.1	2.42	V
$V_{EN-VOUT-HYS}$	Hysteresis voltage between V_{OUT} precision enable and disable thresholds	V_{ENABLE} hysteresis		–294		mV
I_{LKG-EN}	Enable input leakage current	V_{EN} = 3.3 V		0.8	1.7	µA
INTERNAL LDO (VCC PIN AND BIAS PIN)						
V_{CC}	Internal LDO output voltage V_{CC}	V_{IN} ≥ 3.8 V		3.2		V
$V_{CC-UVLO}$	Undervoltage lockout (UVLO) thresholds for V_{CC}	V_{CC} rising threshold		3.15		V
		Hysteresis voltage between rising and falling thresholds		–575		mV
$V_{BIAS-ON}$	Internal LDO input change over threshold to BIAS	V_{BIAS} rising threshold		2.94	3.15	V
		Hysteresis voltage between rising and falling thresholds		–67		mV

Electrical Characteristics (continued)

Limits apply over the recommended operating junction temperature (T_J) range of –40°C to +125°C, unless otherwise stated. Minimum and Maximum limits are specified through test, design or statistical correlation. Typical values represent the most likely parametric norm at T_J = 25°C, and are provided for reference purposes only. Unless otherwise stated, the following conditions apply: V_{IN} = 24 V, V_{OUT} = 3.3 V, F_S = 500 kHz.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
VOLTAGE REFERENCE (FB PIN)						
V_{FB}	Feedback voltage	T_J = 25°C	1.004	1.011	1.018	V
		T_J = –40°C to 125°C	0.994	1.011	1.030	
$I_{LKG\text{-}FB}$	Input leakage current at FB pin	FB = 1.011 V		0.2	65	nA
THERMAL SHUTDOWN						
T_{SD} (1)	Thermal shutdown	Shutdown threshold		160		°C
		Recovery threshold		150		
CURRENT LIMIT AND HICCUP						
$I_{HS\text{-}LIMIT}$	Peak inductor current limit		3.6	4.5	5	A
$I_{LS\text{-}LIMIT}$	Valley inductor current limit		1.8	2.05	2.3	A
SOFT START (SS/TRK PIN)						
I_{SSC}	Soft-start charge current		1.17	2	2.75	µA
R_{SSD}	Soft-start discharge resistance	UVLO, TSD, OCP, or EN = 0 V		16		kΩ
POWER GOOD (PGOOD PIN)						
$V_{PGOOD\text{-}HIGH}$	Power-good flag overvoltage tripping threshold	% of FB voltage		110%	113%	
$V_{PGOOD\text{-}LOW}$	Power-good flag undervoltage tripping threshold	% of FB voltage	80%	88%		
$V_{PGOOD\text{-}HYS}$	Power-good flag recovery hysteresis	% of FB voltage		6%		
R_{PGOOD}	PGOOD pin pulldown resistance when power bad	V_{EN} = 3.3 V		69	150	Ω
		V_{EN} = 0 V		150	350	
MOSFETS (2)						
$R_{DS\text{-}ON\text{-}HS}$	High-side MOSFET ON-resistance	I_{OUT} = 1 A V_{BIAS} = V_{OUT} = 3.3 V		210		mΩ
$R_{DS\text{-}ON\text{-}LS}$	Low-side MOSFET ON-resistance	I_{OUT} = 1 A V_{BIAS} = V_{OUT} = 3.3 V		110		mΩ

(1) Ensured by design. Not production tested.
(2) Measured at package pins.

6.6 Timing Requirements

		MIN	NOM	MAX	UNIT
CURRENT LIMIT AND HICCUP					
N_{OC}	Hiccup wait cycles when LS current limit tripped		32		Cycles
T_{OC}	Hiccup retry delay time		5.5		ms
SOFT START (SS/TRK PIN)					
T_{SS}	Internal soft-start time when SS pin open circuit		4.1		ms
POWER GOOD (PGOOD PIN)					
$T_{PGOOD\text{-}RISE}$	Power-good flag rising transition deglitch delay		220		µs
$T_{PGOOD\text{-}FALL}$	Power-good flag falling transition deglitch delay		220		µs

6.7 Switching Characteristics

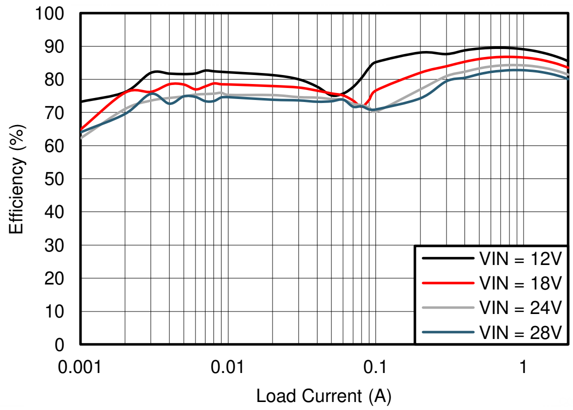
Limits apply over the recommended operating junction temperature (T_J) range of –40°C to +125°C, unless otherwise stated. Minimum and Maximum limits are specified through test, design or statistical correlation. Typical values represent the most likely parametric norm at T_J = 25°C, and are provided for reference purposes only. Unless otherwise stated, the following conditions apply: V_{IN} = 24 V, V_{OUT} = 3.3 V, F_S = 500 kHz.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SW (SW PIN)						
t_{ON-MIN} (1)	Minimum high side MOSFET ON-time			125	165	ns
$t_{OFF-MIN}$ (1)	Minimum high side MOSFET OFF-time			200	250	ns
OSCILLATOR (SW PINS AND SYNC PIN)						
$F_{OSC-DEFAULT}$	Oscillator default frequency	RT pin open circuit	410	500	590	kHz
F_{ADJ}	Minimum adjustable frequency	With 1% resistors at RT pin		200		kHz
	Maximum adjustable frequency			2200		kHz
	Frequency adjust accuracy			10%		
$V_{SYNC-HIGH}$	Sync clock high level threshold		2			V
$V_{SYNC-LOW}$	Sync clock low level threshold				0.4	V
$D_{SYNC-MAX}$	Sync clock maximum duty cycle			90%		
$D_{SYNC-MIN}$	Sync clock minimum duty cycle			10%		
$T_{SYNC-MIN}$	Mininum sync clock ON and OFF time			80		ns

(1) Ensured by design. Not production tested.

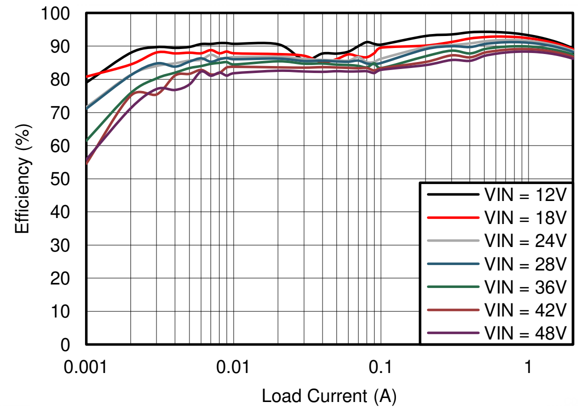
6.8 Typical Characteristics

Unless otherwise specified, V_{IN} = 24 V, V_{OUT} = 3.3 V, F_S = 500 kHz, L = 10 µH, C_{OUT} = 150 µF, C_{FF} = 47 pF. Please refer to Application Performance Curves for Bill of Materials (BOM) for other V_{OUT} and F_S combinations.



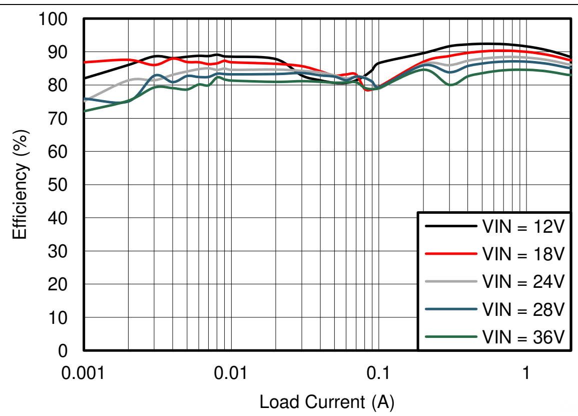
V_{OUT} = 3.3 V F_S = 500 kHz

Figure 1. Efficiency



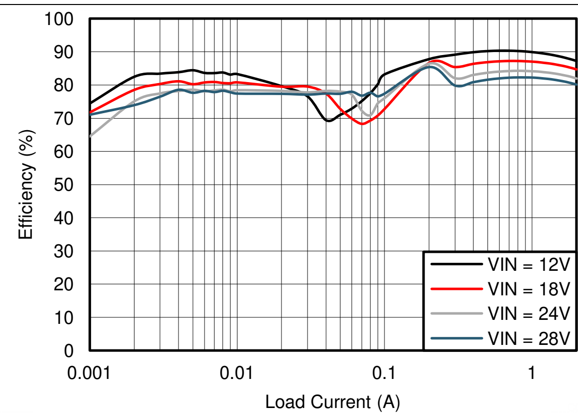
V_{OUT} = 5 V F_S = 200 kHz

Figure 2. Efficiency



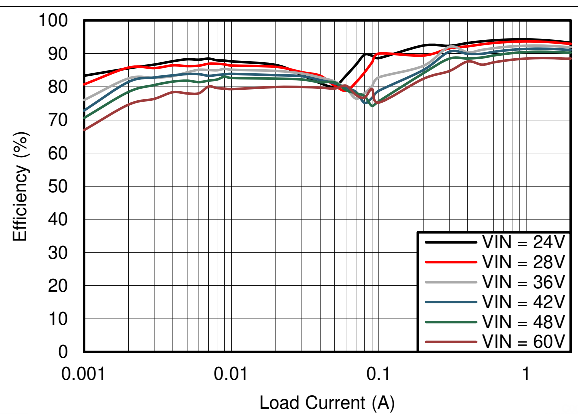
V_{OUT} = 5 V F_S = 500 kHz

Figure 3. Efficiency



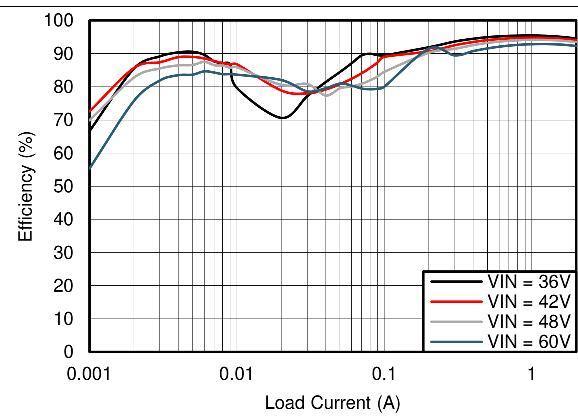
V_{OUT} = 5 V F_S = 1 MHz

Figure 4. Efficiency



V_{OUT} = 12 V F_S = 500 kHz

Figure 5. Efficiency

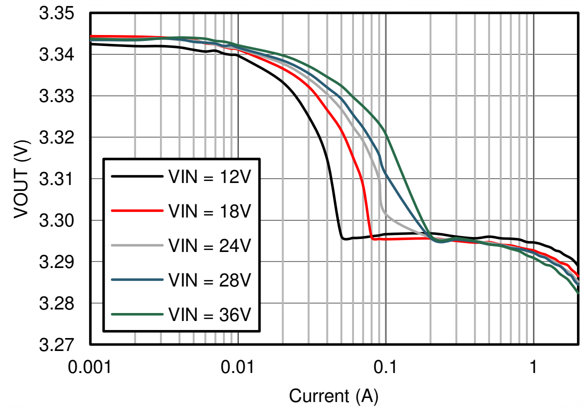


V_{OUT} = 24 V F_S = 500 kHz

Figure 6. Efficiency

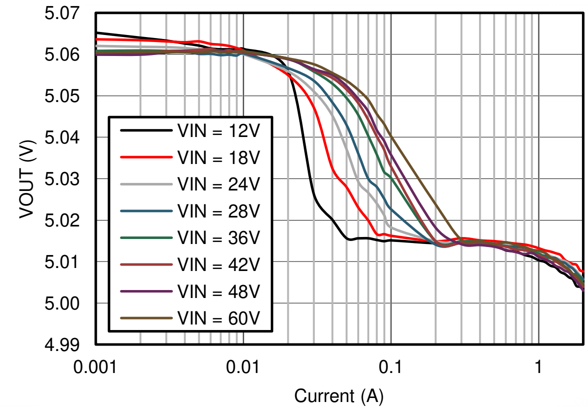
Typical Characteristics (continued)

Unless otherwise specified, V_{IN} = 24 V, V_{OUT} = 3.3 V, F_S = 500 kHz, L = 10 µH, C_{OUT} = 150 µF, C_{FF} = 47 pF. Please refer to Application Performance Curves for Bill of Materials (BOM) for other V_{OUT} and F_S combinations.



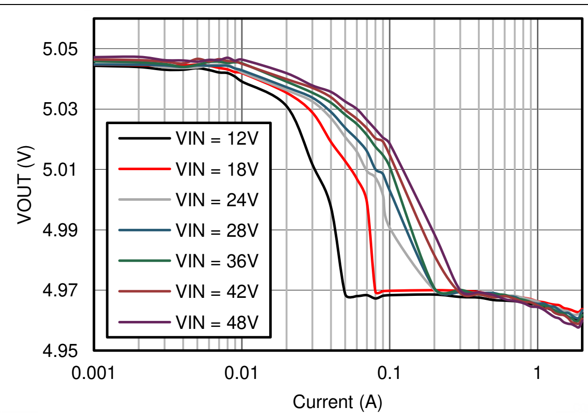
V_{OUT} = 3.3 V F_S = 500 kHz

Figure 7. V_{OUT} Regulation



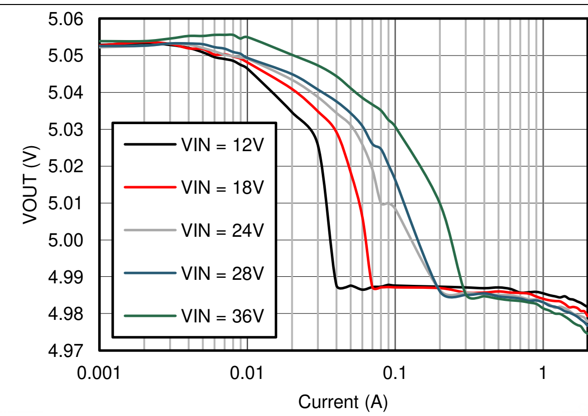
V_{OUT} = 5 V F_S = 200 kHz

Figure 8. V_{OUT} Regulation



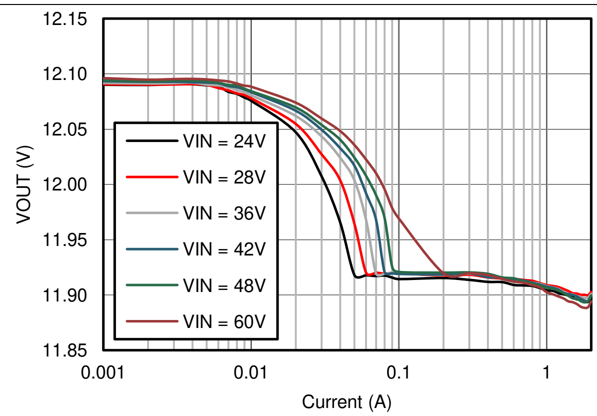
V_{OUT} = 5 V F_S = 500 kHz

Figure 9. V_{OUT} Regulation



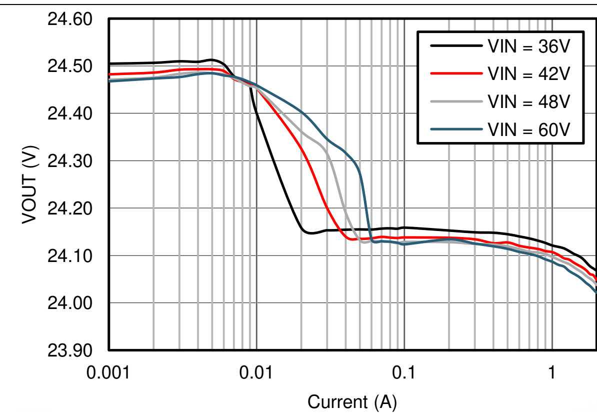
V_{OUT} = 5 V F_S = 1 MHz

Figure 10. V_{OUT} Regulation



V_{OUT} = 12 V F_S = 500 kHz

Figure 11. V_{OUT} Regulation

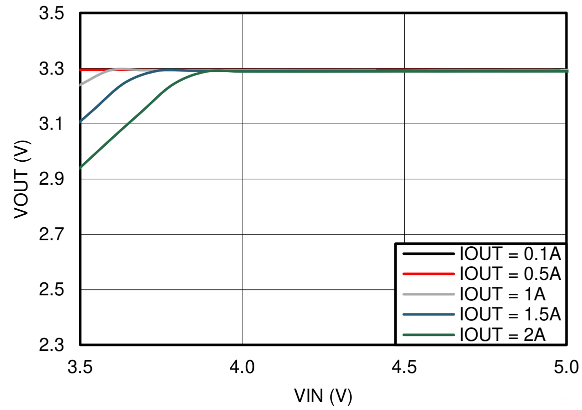


V_{OUT} = 24 V F_S = 500 kHz

Figure 12. V_{OUT} Regulation

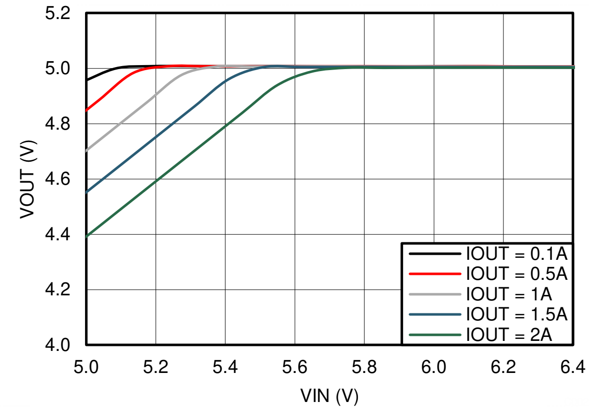
Typical Characteristics (continued)

Unless otherwise specified, V_{IN} = 24 V, V_{OUT} = 3.3 V, F_S = 500 kHz, L = 10 µH, C_{OUT} = 150 µF, C_{FF} = 47 pF. Please refer to Application Performance Curves for Bill of Materials (BOM) for other V_{OUT} and F_S combinations.



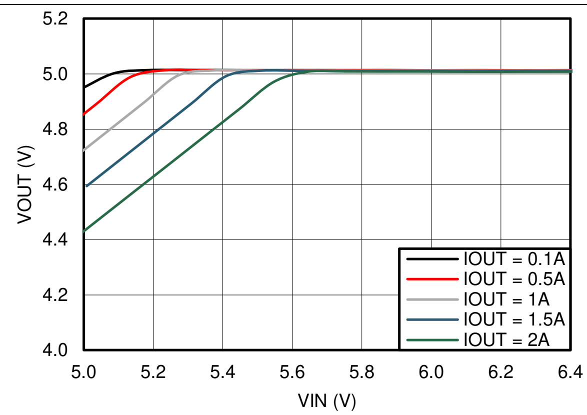
V_{OUT} = 3.3 V F_S = 500 kHz

Figure 13. Dropout Curve



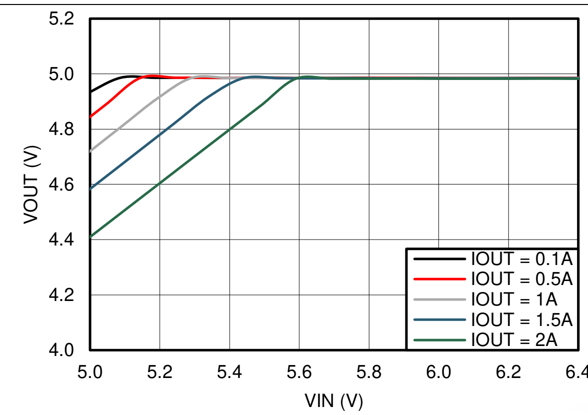
V_{OUT} = 5 V F_S = 200 kHz

Figure 14. Dropout Curve



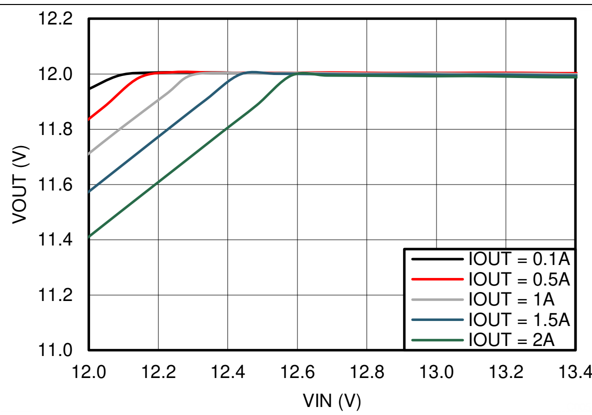
V_{OUT} = 5 V F_S = 500 kHz

Figure 15. Dropout Curve



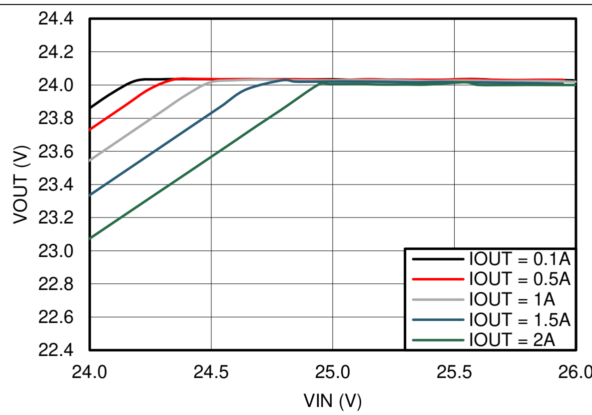
V_{OUT} = 5 V F_S = 1 MHz

Figure 16. Dropout Curve



V_{OUT} = 12 V F_S = 500 kHz

Figure 17. Dropout Curve

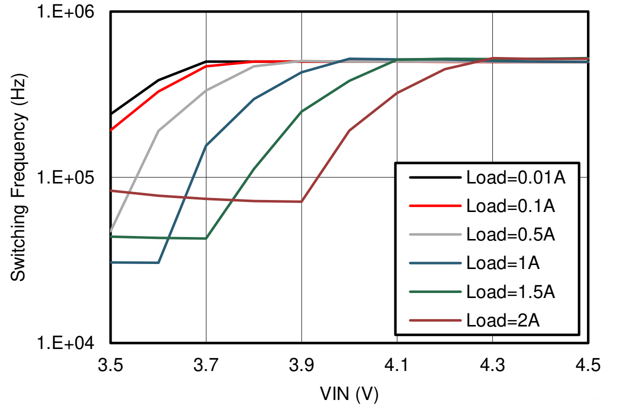


V_{OUT} = 24 V F_S = 500 kHz

Figure 18. Dropout Curve

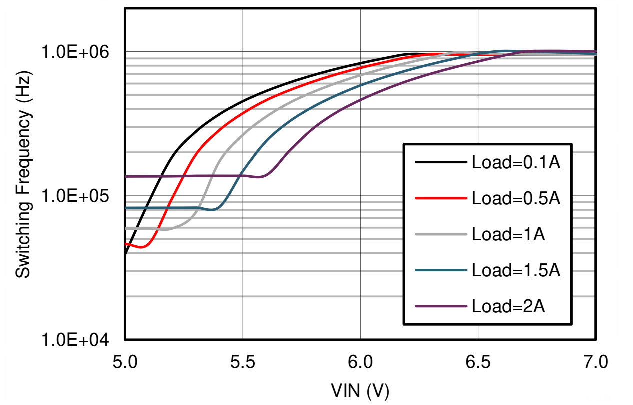
Typical Characteristics (continued)

Unless otherwise specified, V_{IN} = 24 V, V_{OUT} = 3.3 V, F_S = 500 kHz, L = 10 µH, C_{OUT} = 150 µF, C_{FF} = 47 pF. Please refer to Application Performance Curves for Bill of Materials (BOM) for other V_{OUT} and F_S combinations.



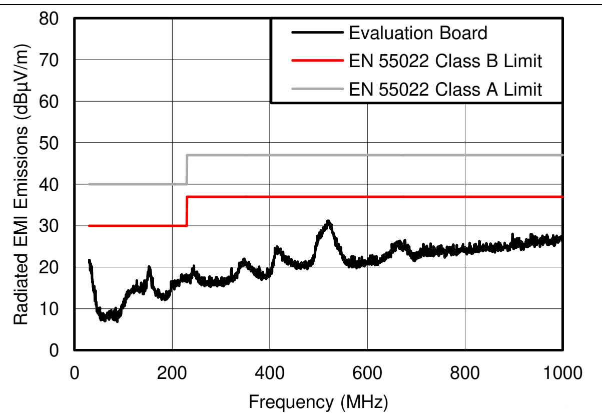
V_{OUT} = 3.3 V F_S = 500 kHz

Figure 19. Switching Frequency vs V_{IN} in Dropout Operation



V_{OUT} = 5 V F_S = 1 MHz

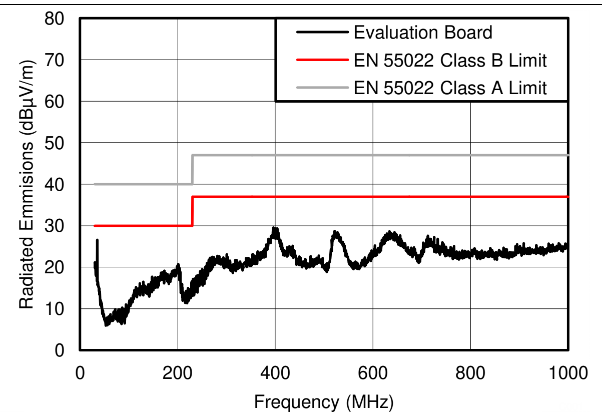
Figure 20. Switching Frequency vs V_{IN} in Dropout Operation



V_{OUT} = 3.3 V F_S = 500 kHz I_{OUT} = 2 A

Measured on the LM46002PWPEVM with default BOM. No input filter used.

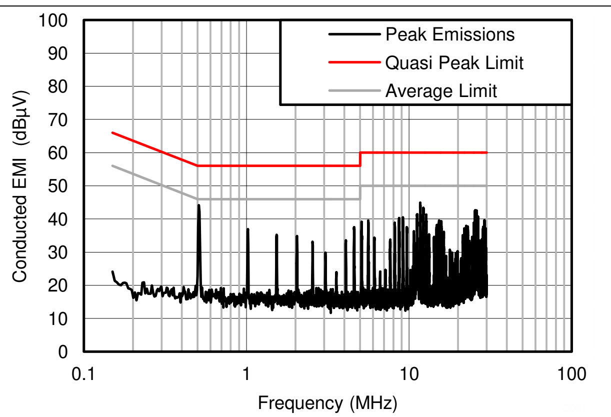
Figure 21. Radiated EMI Curve



V_{OUT} = 5 V F_S = 1 MHz I_{OUT} = 2 A

Measured on the LM46002PWPEVM with L = 6.8 µH, C_{OUT} = 47 µF, C_{FF} = 47 pF. No input filter used.

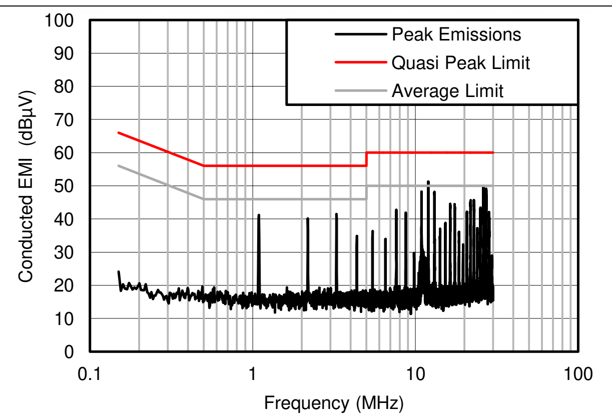
Figure 22. Radiated EMI Curve



V_{OUT} = 3.3 V F_S = 500 kHz I_{OUT} = 2 A

Measured on the LM46002PWPEVM with default BOM. Input filter: L_{in} = 1 µH C_d = 47 µF C_{IN4} = 68 µF

Figure 23. Conducted EMI Curve



V_{OUT} = 5 V F_S = 1 MHz I_{OUT} = 2 A

Measured on the LM46002PWPEVM with L = 6.8 µH, C_{OUT} = 47 µF, C_{FF} = 47 pF. Input filter L_{in} = 1 µH C_d = 47 µF C_{IN4} = 68 µF

Figure 24. Conducted EMI Curve

Typical Characteristics (continued)

Unless otherwise specified, V_{IN} = 24 V, V_{OUT} = 3.3 V, F_S = 500 kHz, L = 10 µH, C_{OUT} = 150 µF, C_{FF} = 47 pF. Please refer to Application Performance Curves for Bill of Materials (BOM) for other V_{OUT} and F_S combinations.

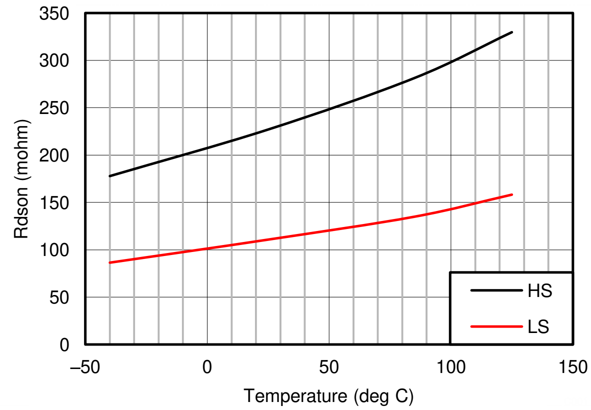


Figure 25. High-Side and Low-side On Resistance vs Junction Temperature

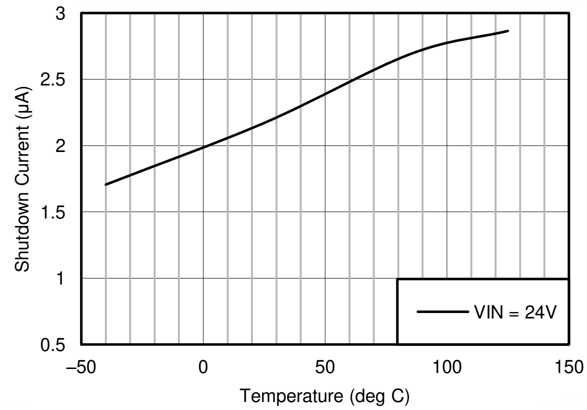


Figure 26. Shutdown Current vs Junction Temperature

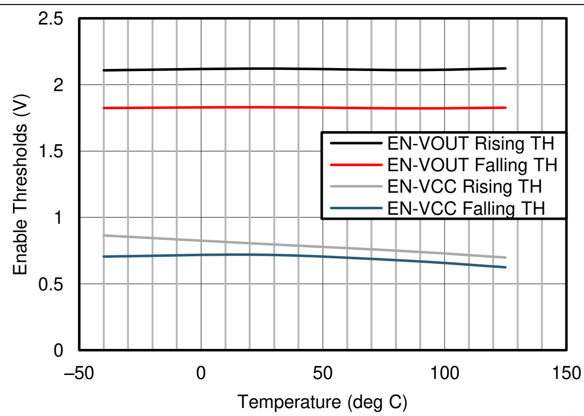


Figure 27. Enable Threshold vs Junction Temperature

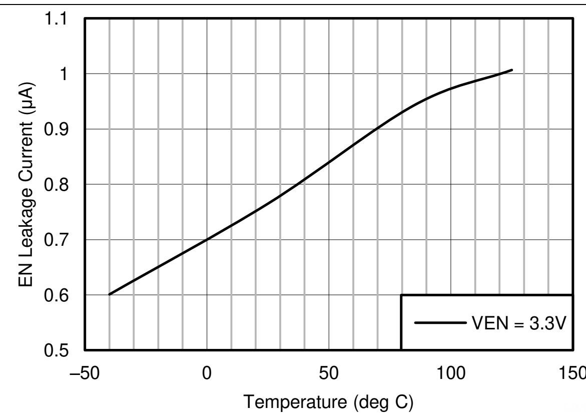


Figure 28. Enable Leakage Current vs Junction Temperature

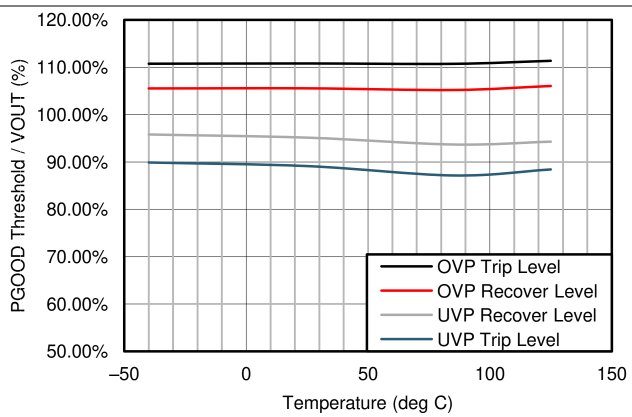


Figure 29. PGOOD Threshold vs Junction Temperature

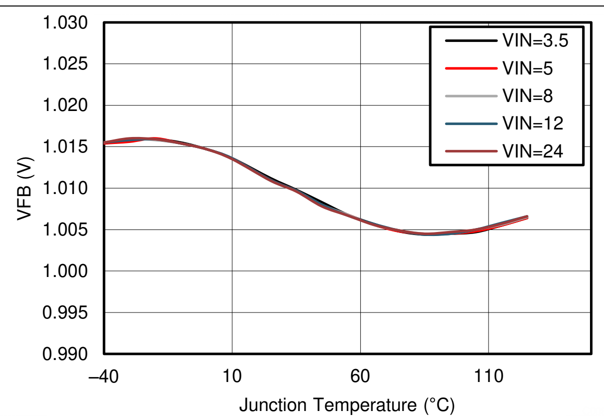
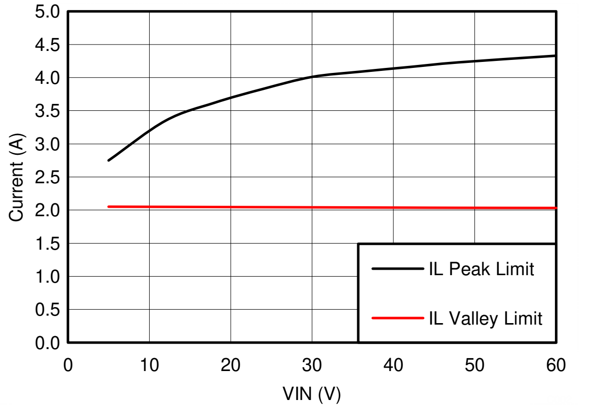


Figure 30. Feedback Voltage vs Junction Temperature

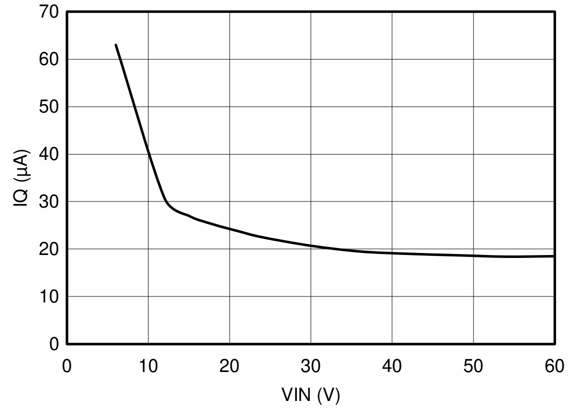
Typical Characteristics (continued)

Unless otherwise specified, V_{IN} = 24 V, V_{OUT} = 3.3 V, F_S = 500 kHz, L = 10 µH, C_{OUT} = 150 µF, C_{FF} = 47 pF. Please refer to Application Performance Curves for Bill of Materials (BOM) for other V_{OUT} and F_S combinations.



V_{OUT} = 3.3 V F_S = 500 kHz

Figure 31. Peak and Valley Current Limits vs V_{IN}



V_{OUT} = 3.3 V F_S = 500 kHz I_{OUT} = 0 A
EN pin is connected to external 5 V rail

Figure 32. Operation I_Q vs V_{IN} with BIAS Connected to V_{OUT}

7 Detailed Description

7.1 Overview

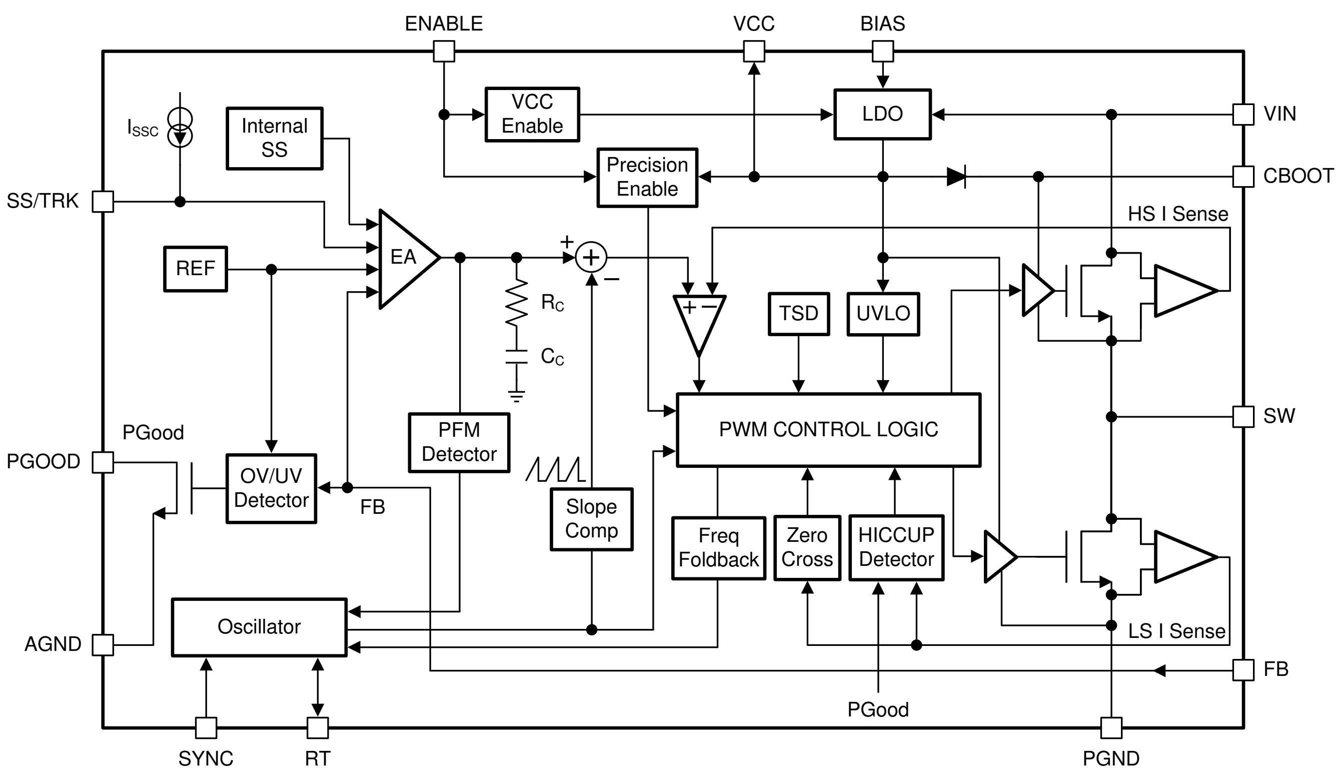
The LM46002 regulator is an easy to use synchronous step-down DC-DC converter that operates from 3.5-V to 60-V supply voltage. It is capable of delivering up to 2-A DC load current with exceptional efficiency and thermal performance in a very small solution size. An extended family is available in 0.5-A and 1-A load options in pin-to-pin compatible packages.

The LM46002 employs fixed-frequency, peak-current-mode control with discontinuous conduction mode (DCM) and pulse frequency modulation (PFM) mode at light load to achieve high efficiency across the load range. The device is internally compensated, which reduces design time, and requires fewer external components. The switching frequency is programmable from 200 kHz to 2.2 MHz by an external resistor, R_T. It defaults at 500 kHz without R_T. The LM46002 is also capable of synchronization to an external clock within the 200-kHz to 2.2-MHz frequency range. The wide switching frequency range allows the device to be optimized to fit small board space at higher frequency, or high efficient power conversion at lower frequency.

Optional features are included for more comprehensive system requirements, including power-good (PGOOD) flag, precision enable, synchronization to external clock, extendable soft-start time, and output-voltage tracking. These features provide a flexible and easy-to-use platform for a wide range of applications. Protection features include overtemperature shutdown, V_{CC} undervoltage lockout (UVLO), cycle-by-cycle current limit, and short-circuit protection with hiccup mode.

The family requires few external components and the pin arrangement was designed for simple, optimum PCB layout. The LM46002 device is available in the 16-pin HTSSOP (PWP) leaded package (6.6 mm × 5.1 mm × 1.2 mm) with 0.65-mm lead pitch.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Fixed-Frequency, Peak-Current-Mode-Controlled, Step-Down Regulator

The following operating description of the LM46002 refer to the *Functional Block Diagram* and to the waveforms in Figure 33. The LM46002 is a step-down buck regulator with both high-side (HS) switch and low-side (LS) switch (synchronous rectifier) integrated. The LM46002 supplies a regulated output voltage by turning on the HS and LS NMOS switches with controlled ON-time. During the HS switch ON-time, the SW pin voltage V_{SW} swings up to approximately V_{IN}, and the inductor current I_L increases with a linear slope (V_{IN} – V_{OUT}) / L. When the HS switch is turned off by the control logic, the LS switch is turned on after a anti-shoot-through dead time. Inductor current discharges through the LS switch with a slope of $–V_{OUT}$ / L. The control parameter of buck converters are defined as duty cycle D = t_{ON} / T_{SW}, where t_{ON} is the HS switch ON-time and T_{SW} is the switching period. The regulator control loop maintains a constant output voltage by adjusting the duty cycle D. In an ideal buck converter, where losses are ignored, D is proportional to the output voltage and inversely proportional to the input voltage: D = V_{OUT} / V_{IN}.

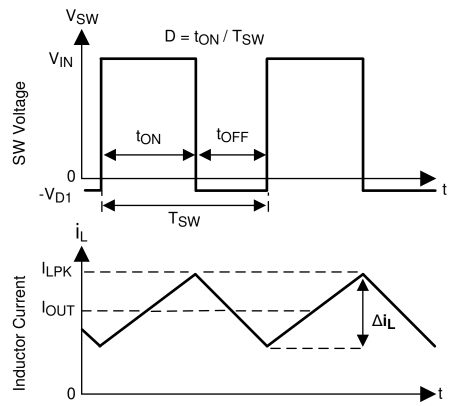


Figure 33. SW Node and Inductor Current Waveforms in Continuous Conduction Mode (CCM)

The LM46002 synchronous buck converter employs peak current mode control topology. A voltage feedback loop is used to get accurate DC voltage regulation by adjusting the peak current command based on voltage offset. The peak inductor current is sensed from the HS switch and compared to the peak current to control the ON-time of the HS switch. The voltage feedback loop is internally compensated, which allows for fewer external components, makes it easy to design, and provides stable operation with almost any combination of output capacitors. The regulator operates with fixed switching frequency in CCM and DCM. At very light load, the LM46002 operates in PFM to maintain high efficiency, and the switching frequency decreases with reduced load current.

7.3.2 Light Load Operation

DCM operation is employed in the LM46002 when the inductor current valley reaches zero. The LM46002 is in DCM when load current is less than half of the peak-to-peak inductor current ripple in CCM. In DCM, the LS switch is turned off when the inductor current reaches zero. Switching loss is reduced by turning off the LS FET at zero current, and the conduction loss is lowered by not allowing negative current conduction. Power conversion efficiency is higher in DCM than CCM under the same conditions.

In DCM, the HS switch ON-time reduces with lower load current. When either the minimum HS switch ON-time (T_{ON-MIN}) or the minimum peak inductor current ($I_{PEAK-MIN}$) is reached, the switching frequency decreasse to maintain regulation. At this point, the LM46002 operates in PFM. In PFM, switching frequency is decreased by the control loop when load current reduces to maintain output voltage regulation. Switching loss is further reduced in PFM operation due to less frequent switching actions. Figure 34 shows an example of switching frequency decreases with decreased load current.

Feature Description (continued)

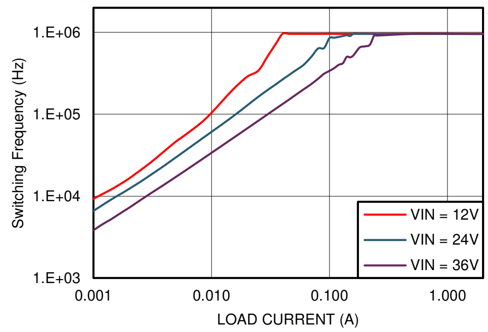


Figure 34. Switching Frequency Decreases With Lower Load Current in PFM Operation V_{OUT} = 5 V F_S = 1 MHz

In PFM operation, a small positive DC offset is required at the output voltage to activate the PFM detector. The lower the frequency in PFM, the more DC offset is needed at V_{OUT}. See *Typical Characteristics* for typical DC offset at very light load. If the DC offset on V_{OUT} is not acceptable for a given application, a static load at output is recommended to reduce or eliminate the offset. Lowering values of the feedback divider R_{FBT} and R_{FBB} can also serve as a static load. In conditions with low V_{IN} and/or high frequency, the LM46002 may not enter PFM mode if the output voltage cannot be charged up to provide the trigger to activate the PFM detector. Once the LM46002 is operating in PFM mode at higher V_{IN}, it remains in PFM operation when V_{IN} is reduced.

7.3.3 Adjustable Output Voltage

The voltage regulation loop in the LM46002 regulates output voltage by maintaining the voltage on FB pin (V_{FB}) to be the same as the internal REF voltage (V_{REF}). Use a resistor divider pair to program the ratio from output voltage V_{OUT} to V_{FB}. The resistor divider is connected from the V_{OUT} of the LM46002 to ground with the mid-point connecting to the FB pin.

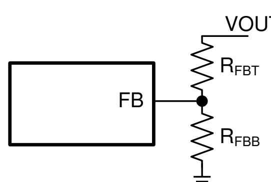


Figure 35. Output Voltage Setting

The voltage reference system produces a precise voltage reference over temperature. The internal REF voltage is 1.011 V typically. To program the output voltage of the LM46002 to be a certain value V_{OUT}, R_{FBB} can be calculated with a selected R_{FBT} by Equation 1:

$$R_{FBB} = \frac{V_{FB}}{V_{OUT} - V_{FB}} R_{FBT} \quad (1)$$

The choice of the R_{FBT} depends on the application. TI recommends R_{FBT} in the range from 10 kΩ to 100 kΩ for most applications. A lower R_{FBT} value can be used if static loading is desired to reduce V_{OUT} offset in PFM operation. Lower R_{FBT} reduces efficiency at very light load. Less static current goes through a larger R_{FBT} and might be more desirable when light load efficiency is critical. But R_{FBT} larger than 1 MΩ is not recommended because it makes the feedback path more susceptible to noise. Larger R_{FBT} value requires more carefully designed feedback path on the PCB. The tolerance and temperature variation of the resistor dividers affect the output voltage regulation. TI recommends using divider resistors with 1% tolerance or better and temperature coefficient of 100 ppm or lower.

Feature Description (continued)

If the resistor divider is not connected properly, output voltage cannot be regulated because the feedback loop is broken. If the FB pin is shorted to ground, the output voltage is driven close to V_{IN} because the regulator detects very low voltage on the FB pin and tries to regulate it up. The load connected to the output could be damaged under such a condition. Do not short FB pin to ground when the LM46002 is enabled. It is important to route the feedback trace away from the noisy area of the PCB. For more layout recommendations, see *Layout* section.

7.3.4 Enable (ENABLE)

Voltage on the EN pin (V_{EN}) controls the ON or OFF functionality of the LM46002. Applying a voltage less than 0.4 V to the EN input shuts down the operation of the LM46002. In shutdown mode the quiescent current drops to typically 2.3 µA at V_{IN} = 24 V.

The internal LDO output voltage V_{CC} is turned on when V_{EN} is higher than 1.2 V. The LM46002 switching action and output regulation are enabled when V_{EN} is greater than 2.1 V (typical). The LM46002 supplies regulated output voltage when enabled and output current up to 2 A.

The ENABLE pin is an input and cannot be open circuit or floating. The simplest way to enable the operation of the LM46002 is to connect the ENABLE pin to VIN pins directly. This allows self-start-up of the LM46002 when V_{IN} is within the operation range.

Many applications will benefit from the employment of an enable divider R_{ENT} and R_{ENB} in Figure 36 to establish a precision system UVLO level for the stage. System UVLO can be used for supplies operating from utility power as well as battery power. It can be used for sequencing, ensuring reliable operation, or supply protection, such as a battery. An external logic signal can also be used to drive EN input for system sequencing and protection.

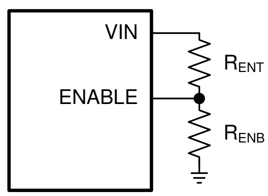


Figure 36. System UVLO by Enable Dividers

7.3.5 VCC, UVLO, and BIAS

The LM46002 integrates an internal LDO to generate V_{CC} for control circuitry and MOSFET drivers. The nominal voltage for V_{CC} is 3.2 V. The VCC pin is the output of the LDO and must be properly bypassed. Place a high-quality ceramic capacitor with 2.2 µF to 10 µF capacitance and 6.3 V or higher rated voltage as close as possible to VCC and grounded to the exposed PAD and ground pins. Do not load the VCC output pin or leave floating or shorted to ground during operation. Shorting VCC to ground during operation may cause damage to the LM46002.

Undervoltage lockout (UVLO) prevents the LM46002 from operating until the V_{CC} voltage exceeds 3.15 V (typical). The V_{CC} UVLO threshold has 575 mV of hysteresis (typically) to prevent undesired shutting down due to temporary V_{IN} droops.

The internal LDO has two inputs: primary from VIN and secondary from BIAS input. The BIAS input powers the LDO when V_{BIAS} is higher than the changeover threshold. Power loss of an LDO is calculated by $I_{LDO} \times (V_{IN\text{-}LDO} - V_{OUT\text{-}LDO})$. The higher the difference between the input and output voltages of the LDO, the more power loss occur to supply the same output current. The BIAS input is designed to reduce the difference of the input and output voltages of the LDO to reduce power loss and improve LM46002 efficiency, especially at light load. TI recommends tying the BIAS pin to V_{OUT} when V_{OUT} ≥ 3.3V. The BIAS pin must be grounded in applications with V_{OUT} less than 3.3 V. BIAS input can also come from an external voltage source, if available, to reduce power loss. When used, TI recommends a 1-µF to 10-µF high-quality ceramic capacitor to bypass the BIAS pin to ground.

Feature Description (continued)

7.3.6 Soft Start and Voltage Tracking (SS/TRK)

The LM46002 has a flexible and easy-to-use start-up rate control pin: SS/TRK. Soft-start feature is to prevent inrush current impacting the LM46002 and its supply when power is first applied. Soft start is achieved by slowly ramping up the target regulation voltage when the device is first enabled or powered up.

The simplest way to use the device is to leave the SS/TRK pin open circuit or floating. The LM46002 employs the internal soft-start control ramp and start up to the regulated output voltage in 4.1 ms typically.

In applications with a large amount of output capacitors, higher V_{OUT}, or other special requirements, the soft-start time can be extended by connecting an external capacitor C_{SS} from SS/TRK pin to AGND. Extended soft-start time further reduces the supply current required to charge up output capacitors and supply any output loading. An internal current source (I_{SSC} = 2.2 µA) charges C_{SS} and generates a ramp from 0 V to V_{FB} to control the ramp-up rate of the output voltage. For a desired soft start time t_{SS}, the capacitance for C_{SS} can be found by

$$C_{SS} = I_{SSC} \times t_{SS} \quad (2)$$

The soft-start capacitor C_{SS} is discharged by an internal FET when V_{OUT} is shutdown by hiccup protection or ENABLE = logic low. When a large C_{SS} is applied and ENABLE is toggled low only for a short period of time, it could happen that C_{SS} is not fully discharged and the next soft start ramp will follow internal soft start ramp before reaching the left-over voltage on C_{SS} and then follow the ramp programmed by C_{SS}. If this is not acceptable by a certain application, a R-C low-pass filter can be added to ENABLE to slow down the shutting down of VCC, which allows more time to discharge C_{SS}.

The LM46002 is capable of start-up into prebiased output conditions. When the inductor current reaches zero, the LS switch is turned off to avoid negative current conduction. This operation mode is also called diode emulation mode. It is built-in by the DCM operation in light loads. With a prebiased output voltage, the LM46002 waits until the soft-start ramp allows regulation above the prebiased voltage and then follows the soft-start ramp to the regulation level.

When an external voltage ramp is applied to the SS/TRK pin, the LM46002 FB voltage follows the ramp if the ramp magnitude is lower than the internal soft-start ramp. A resistor divider pair can be used on the external control ramp to the SS/TRK pin to program the tracking rate of the output voltage. The final voltage seen by the SS/TRK pin must not fall below 1.2 V to avoid abnormal operation.

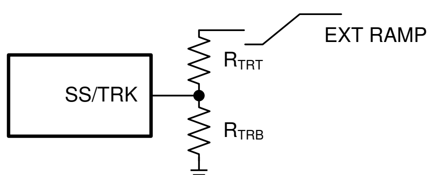


Figure 37. Soft Start Tracking External Ramp

V_{OUT} tracked to an external voltage ramp has the option of ramping up slower or faster than the internal voltage ramp. V_{FB} always follows the lower potential of the internal voltage ramp and the voltage on the SS/TRK pin. Figure 38 shows the case when V_{OUT} ramps slower than the internal ramp, while Figure 39 shows when V_{OUT} ramps faster than the internal ramp. Faster start up time may result in inductor current-tripping current protection during start-up. Use with special care.

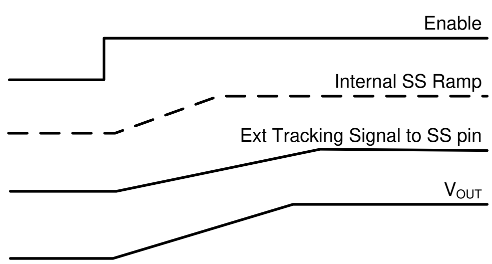


Figure 38. Tracking With Longer Start-up Time Than The Internal Ramp

Feature Description (continued)

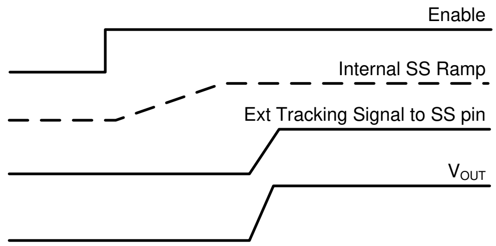


Figure 39. Tracking With Shorter Start-up Time Than The Internal Ramp

7.3.7 Switching Frequency (RT) and Synchronization (SYNC)

The switching frequency of the LM46002 can be programmed by the impedance R_T from the RT pin to ground. The frequency is inversely proportional to the R_T resistance. The RT pin can be left floating, and the LM46002 operates at 500 kHz default switching frequency. The RT pin is not designed to be shorted to ground.

For a desired frequency, typical R_T resistance can be found by Equation 3.

$$R_T(k\Omega) = 40200 / Freq\ (kHz) - 0.6 \quad (3)$$

Figure 40 shows R_T resistance vs switching frequency F_S curve.

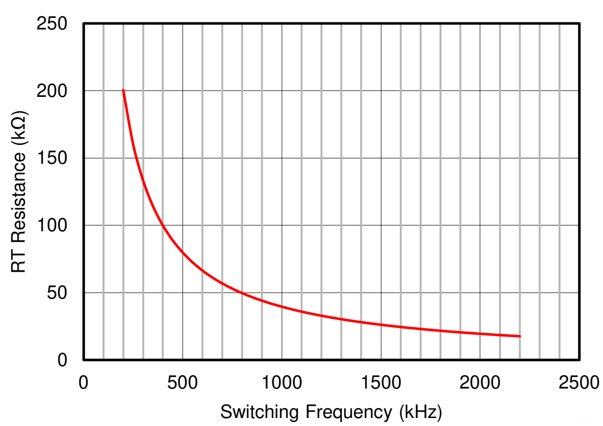


Figure 40. R_T Resistance vs Switching Frequency

Table 1 provides typical R_T values for a given F_S.

Table 1. Typical Frequency Setting R_T Resistance

F_S (kHz)	R_T (kΩ)
200	200
350	115
500	80.6
750	53.6
1000	39.2
1500	26.1
2000	19.6
2200	17.8

Feature Description (continued)

The LM46002 switching action can also be synchronized to an external clock from 200 kHz to 2.2 MHz. Connect an external clock to the SYNC pin, with proper high speed termination, to avoid ringing. Ground the SYNC pin if not used.

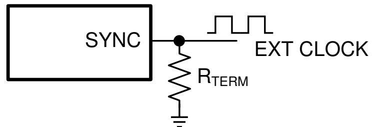


Figure 41. Frequency Synchronization

The recommendations for the external clock include high level no lower than 2 V, low level no higher than 0.4 V, duty cycle between 10% and 90%, and both positive and negative pulse width no shorter than 80 ns. When the external clock fails at logic high or low, the LM46002 switches at the frequency programmed by the R_T resistor after a time-out period. TI recommends connecting a resistor R_T to the RT pin so that the internal oscillator frequency is the same as the target clock frequency when the LM46002 is synchronized to an external clock. This allows the regulator to continue operating at approximately the same switching frequency if the external clock fails.

The choice of switching frequency is usually a compromise between conversion efficiency and the size of the circuit. Lower switching frequency implies reduced switching losses (including gate charge losses, switch transition losses, etc.) and usually results in higher overall efficiency. However, higher switching frequency allows use of smaller LC output filters and hence a more compact design. Lower inductance also helps transient response (higher large signal slew rate of inductor current) and reduces the DCR loss. The optimal switching frequency is usually a trade-off in a given application and thus needs to be determined on a case-by-case basis. It is related to the input voltage, output voltage, most frequent load current level(s), external component choices, and circuit size requirement. The choice of switching frequency may also be limited if an operating condition triggers T_{ON-MIN} or $T_{OFF-MIN}$.

7.3.8 Minimum ON-Time, Minimum OFF-Time, and Frequency Foldback at Dropout Conditions

Minimum ON-time, T_{ON-MIN}, is the least duration of time that the HS switch can be on. T_{ON-MIN} is typically 125 ns in the LM46002. Minimum OFF-time, $T_{OFF-MIN}$, is the least duration that the HS switch can be off. $T_{OFF-MIN}$ is typically 200 ns in the LM46002.

In CCM operation, T_{ON-MIN} and $T_{OFF-MIN}$ limits the voltage conversion range given a selected switching frequency. The minimum duty cycle allowed is

$$D_{MIN} = T_{ON-MIN} \times F_S \quad (4)$$

And the maximum duty cycle allowed is

$$D_{MAX} = 1 - T_{OFF-MIN} \times F_S \quad (5)$$

Given fixed T_{ON-MIN} and $T_{OFF-MIN}$, the higher the switching frequency the narrower the range of the allowed duty cycle. In the LM46002, frequency foldback scheme is employed to extend the maximum duty cycle when $T_{OFF-MIN}$ is reached. The switching frequency decreases once longer duty cycle is needed under low V_{IN} conditions. The switching frequency can be decreased to approximately 1/10 of the programmed frequency by R_T or the synchronization clock. Such wide range of frequency foldback allows the LM46002 output voltage to stay in regulation with a much lower supply voltage V_{IN}. This leads to a lower effective dropout voltage. See *Typical Characteristics* for more details.

Given an output voltage, the choice of the switching frequency affects the allowed input voltage range, solution size, and efficiency. The maximum operatable supply voltage can be found by

$$V_{IN-MAX} = V_{OUT} / (F_S \times T_{ON-MIN}) \quad (6)$$

At lower supply voltage, the switching frequency decreases once $T_{OFF-MIN}$ is tripped. The minimum V_{IN} without frequency foldback can be approximated by

$$V_{IN-MIN} = V_{OUT} / (1 - F_S \times T_{OFF-MIN}) \quad (7)$$

Taking considerations of power losses in the system with heavy load operation, V_{IN-MIN} is higher than the result calculated in Equation 7 . With frequency foldback, V_{IN-MIN} is lowered by decreased F_S. Figure 42 gives an example of how F_S decreases with decreasing supply voltage V_{IN} at dropout operation.

Feature Description (continued)

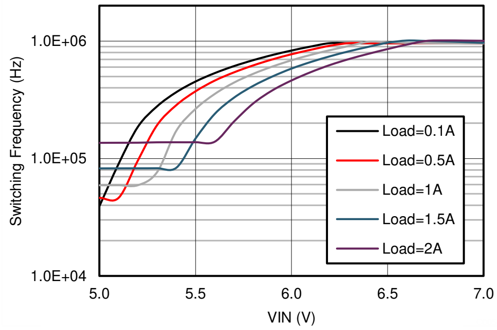


Figure 42. Switching Frequency Decreases in Dropout Operation
V_{OUT} = 5 V F_S = 1 MHz

7.3.9 Internal Compensation and C_{FF}

The LM46002 is internally compensated with R_C = 400 kΩ and C_C = 50 pF as shown in Functional Block Diagram. The internal compensation is designed such that the loop response is stable over the entire operating frequency and output voltage range. Depending on the output voltage, the compensation loop phase margin can be low with all ceramic capacitors. An external feed-forward cap C_{FF} is recommended to be placed in parallel with the top resistor divider R_{FBT} for optimum transient performance.

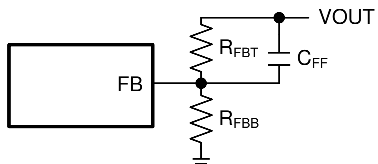


Figure 43. Feed-Forward Capacitor for Loop Compensation

The feedforward capacitor C_{FF} in parallel with R_{FBT} places an additional zero before the crossover frequency of the control loop to boost phase margin. The zero frequency can be found by

$$f_{Z\text{-}CFF} = 1 / (2\pi \times R_{FBT} \times C_{FF}). \tag{8}$$

An additional pole is also introduced with C_{FF} at the frequency of

$$f_{P\text{-}CFF} = 1 / (2\pi \times C_{FF} \times (R_{FBT} // R_{FBB})). \tag{9}$$

The C_{FF} should be selected such that the bandwidth of the control loop without the C_{FF} is centered between $f_{Z\text{-}CFF}$ and $f_{P\text{-}CFF}$. The zero $f_{Z\text{-}CFF}$ adds phase boost at the crossover frequency and improves transient response. The pole $f_{P\text{-}CFF}$ helps maintaining proper gain margin at frequency beyond the crossover.

Designs with different combinations of output capacitors need different C_{FF}. Different types of capacitors have different Equivalent Series Resistance (ESR). Ceramic capacitors have the smallest ESR and need the most C_{FF}. Electrolytic capacitors have much larger ESR, and the ESR zero frequency would be low enough to boost the phase up around the crossover frequency. Designs using mostly electrolytic capacitors at the output may not need any C_{FF} (see Equation 10):

$$f_{Z\text{-}ESR} = 1 / (2\pi \times ESR \times C_{OUT}) \tag{10}$$

The C_{FF} creates a time constant with R_{FBT} that couples in the attenuated output voltage ripple to the FB node. If the C_{FF} value is too large, it can couple too much ripple to the FB and affect V_{OUT} regulation. It could also couple too much transient voltage deviation and falsely trip PGOOD thresholds. Therefore, calculate C_{FF} based on output capacitors used in the system. At cold temperatures, the value of C_{FF} might change based on the tolerance of the chosen component. This may reduce its impedance and ease noise coupling on the FB node. To avoid this, more capacitance can be added to the output or the value of C_{FF} can be reduced. See the *Detailed Design Procedure* for the calculation of C_{FF}.

Feature Description (continued)

7.3.10 Bootstrap Voltage (BOOT)

The driver of the HS switch requires a bias voltage higher than V_{IN} when the HS switch is ON. The capacitor connected between CBOOT and SW pins works as a charge pump to boost voltage on the CBOOT pin to (V_{SW} + V_{CC}). The boot diode is integrated on the LM46002 die to minimize the bill-of-material (BOM). A synchronous switch is also integrated in parallel with the boot diode to reduce voltage drop on CBOOT. TI recommends a high-quality ceramic, 0.47-µF, 6.3-V or higher capacitor for C_{CBOOT}.

7.3.11 Power Good (PGOOD)

The LM46002 has a built-in power-good flag shown on PGOOD pin to indicate whether the output voltage is within its regulation level. The PGOOD signal can be used for start-up sequencing of multiple rails or fault protection. The PGOOD pin is an open-drain output that requires a pullup resistor to an appropriate DC voltage. Voltage detected by the PGOOD pin must never exceed 12 V. A resistor divider pair can be used to divide the voltage down from a higher potential. A typical range of pullup resistor value is 10 kΩ to 100 kΩ.

When the FB voltage is within the power-good band, +4% above and –7% below the internal reference V_{REF} typically, the PGOOD switch is turned off, and the PGOOD voltage is pulled up to the voltage level defined by the pullup resistor or divider. When the FB voltage is outside of the tolerance band, +10 % above or –13 % below V_{REF} typically, the PGOOD switch is turned on, and the PGOOD pin voltage is pulled low to indicate power bad. Both rising and falling edges of the power-good flag have a built-in 220 µs (typical) deglitch delay.

7.3.12 Overcurrent and Short-Circuit Protection

The LM46002 is protected from overcurrent conditions by cycle-by-cycle current limiting on both peak and valley of the inductor current. Hiccup mode is activated if a fault condition persists to prevent overheating.

High-side MOSFET overcurrent protection is implemented by the nature of the peak-current-mode control. The HS switch current is sensed when the HS is turned on after a set blanking time. The HS switch current is compared to the output of the error amplifier (EA) minus slope compensation every switching cycle. See the *Functional Block Diagram* for more details. The peak current of the HS switch is limited by the maximum EA output voltage minus the slope compensation at every switching cycle. The slope compensation magnitude at the peak current is proportional to the duty cycle.

When the LS switch is turned on, the current going through it is also sensed and monitored. The LS switch is be turned OFF at the end of a switching cycle if its current is above the LS current limit $I_{LS-LIMIT}$. The LS switch is kept ON so that inductor current keeps ramping down, until the inductor current ramps below $I_{LS-LIMIT}$. The LS switch is then turned OFF, and the HS switch is turned on, after a dead time. If the current of the LS switch is higher than the LS current limit for 32 consecutive cycles, and the power-good flag is low, hiccup-current protection mode is activated. In hiccup mode, the regulator is shut down and kept off for 5.5 ms, typically, before the LM46002 tries to start again. If overcurrent or short-circuit fault condition still exists, hiccup repeats until the fault condition is removed. Hiccup mode reduces power dissipation under severe overcurrent conditions, preventing overheating and potential damage to the device.

Hiccup is only activated when power-good flag is low. Under non-severe overcurrent conditions when V_{OUT} has not fallen outside of the PGOOD tolerance band, the LM46002 reduces the switching frequency and keeps the inductor current valley clamped at the LS current limit level. This operation mode allows slight overcurrent operation during load transients without tripping hiccup. If the power-good flag becomes low, hiccup operation starts after LS current limit is tripped 32 consecutive cycles.

7.3.13 Thermal Shutdown

Thermal shutdown is a built-in self protection to limit junction temperature and prevent damages due to overheating. Thermal shutdown turns off the device when the junction temperature exceeds 160°C typically to prevent further power dissipation and temperature rise. Junction temperature reduces after thermal shutdown. The LM46002 attempts to restart when the junction temperature drops to 150°C.

7.4 Device Functional Modes

7.4.1 Shutdown Mode

The EN pin provides electrical ON and OFF control for the LM46002. When V_{EN} is below 0.4 V, the device is in shutdown mode. Both the internal LDO and the switching regulator are off. In shutdown mode the quiescent current drops to 2.3 µA typically with V_{IN} = 24 V. The LM46002 also employs UVLO protection. If V_{CC} voltage is below the UVLO level, the output of the regulator is turned off.

7.4.2 Standby Mode

The internal LDO has a lower enable threshold than the regulator. When V_{EN} is above 1.2 V and below the precision enable falling threshold (1.8 V typically), the internal LDO regulates the V_{CC} voltage at 3.2 V. The precision enable circuitry is turned on once V_{CC} is above the UVLO threshold. The switching action and voltage regulation are not enabled unless V_{EN} rises above the precision enable threshold (2.1 V typically).

7.4.3 Active Mode

The LM46002 is in active mode when V_{EN} is above the precision enable threshold and V_{CC} is above its UVLO level. The simplest way to enable the LM46002 is to connect the EN pin to V_{IN}. This allows self start-up of the LM46002 when the input voltage is in the operation range: 3.5 V to 60 V. See *Enable (ENABLE)* and *VCC, UVLO, and BIAS* for details on setting these operating levels.

In active mode, depending on the load current, the LM46002 is in one of four modes:

1. Continuous conduction mode (CCM) with fixed switching frequency when load current is above half of the peak-to-peak inductor current ripple;
2. Discontinuous conduction mode (DCM) with fixed switching frequency when load current is lower than half of the peak-to-peak inductor current ripple in CCM operation;
3. Pulse frequency modulation (PFM) when switching frequency is decreased at very light load;
4. Foldback mode when switching frequency is decreased to maintain output regulation at lower supply voltage V_{IN}.

7.4.4 CCM Mode

CCM operation is employed in the LM46002 when the load current is higher than half of the peak-to-peak inductor current. In CCM operation, the frequency of operation is fixed unless the minimum HS switch ON-time (T_{ON-MIN}), the mininum HS switch OFF-time ($T_{OFF-MIN}$) or LS current limit is exceeded. Output voltage ripple is at a minimum in this mode, and the maximum output current of 2 A can be supplied by the LM46002.

7.4.5 Light Load Operation

When the load current is lower than half of the peak-to-peak inductor current in CCM, the LM46002 operates in DCM, also known as diode emulation mode (DEM). In DCM operation, the LS FET is turned off when the inductor current drops to 0 A to improve efficiency. Both switching losses and conduction losses are reduced in DCM, comparing to forced PWM operation at light load.

At even lighter current loads, PFM is activated to maintain high efficiency operation. When the HS switch ON-time reduces to T_{ON-MIN} or peak inductor current reduces to its minimum $I_{PEAK-MIN}$, the switching frequency reduces to maintain proper regulation. Efficiency is greatly improved by reducing switching and gate drive losses.

7.4.6 Self-Bias Mode

For highest efficiency of operation, TI recommends that the BIAS pin be connected directly to V_{OUT} when 3.3 V ≤ V_{OUT} ≤ 28 V. In this self-bias mode of operation, the difference between the input and output voltages of the internal LDO are reduced and therefore the total efficiency of the LM46002 is improved. These efficiency gains are more evident during light load operation. During this mode of operation, the LM46002 operates with a minimum quiescent current of 27 µA (typical). See *VCC, UVLO, and BIAS* for more details.

8 Applications and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The LM46002 is a step down DC-to-DC regulator. It is typically used to convert a higher DC voltage to a lower DC voltage with a maximum output current of 2 A. The following design procedure can be used to select components for the LM46002. Alternately, the WEBENCH® software may be used to generate complete designs. When generating a design, the WEBENCH® software utilizes iterative design procedure and accesses comprehensive databases of components. See *Custom Design With WEBENCH® Tools* for more details.

8.2 Typical Applications

The LM46002 only requires a few external components to convert from a wide range of supply voltage to output voltage. Figure 44 shows a basic schematic when BIAS is connected to V_{OUT} . This is recommended for $V_{OUT} \geq 3.3$ V. For $V_{OUT} < 3.3$ V, connect BIAS to ground, as shown in Figure 45.

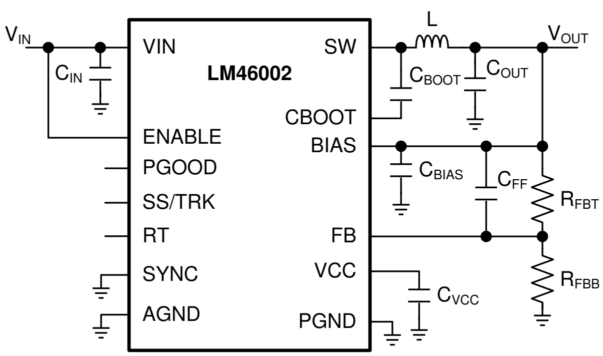


Figure 44. LM46002 Basic Schematic for $V_{OUT} \geq 3.3$ V, Tie BIAS to V_{OUT}

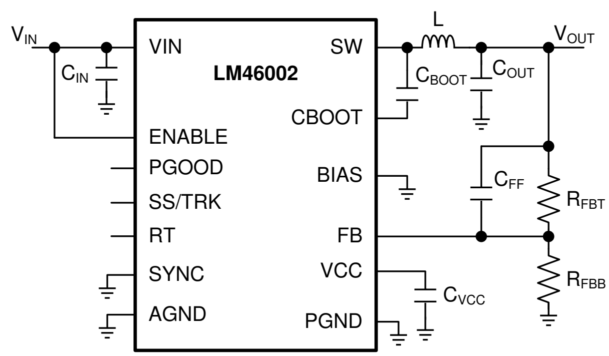


Figure 45. LM46002 Basic Schematic for $V_{OUT} < 3.3$ V, t-Tie BIAS to Ground

The LM46002 also integrates a full list of optional features to aid system design requirements, such as precision enable, V_{CC} UVLO, programmable soft start, output voltage tracking, programmable switching frequency, clock synchronization, and power-good indication. Each application can select the features for a more comprehensive design. A schematic with all features utilized is shown in Figure 46.

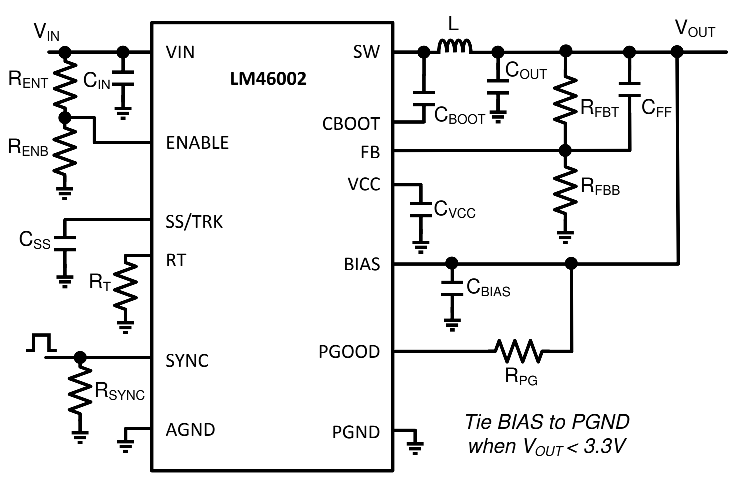


Figure 46. LM46002 Schematic with All Features

Typical Applications (continued)

The external components must fulfill the needs of the application, but also the stability criteria of the device control loop. The LM46002 is optimized to work within a range of external components. The inductance and capacitance of the LC output filter must be considered in conjunction, creating a double pole, responsible for the corner frequency of the converter. Table 2 can be used to simplify the output filter component selection.

Table 2. L, C_{OUT} and C_{FF} Typical Values

F_S (kHz)	L (µH)(1)	C_{OUT} (µF) (2)	C_{FF} (pF) (3)(4)	R_T (kΩ)	R_{FBB} (kΩ) (3)(4)
V_{OUT} = 1 V					
200	8.2	560	none	200	100
500	3.3	470	none	80.6 or open	100
1000	1.8	220	none	39.2	100
2200	0.68	150	none	17.8	100
V_{OUT} = 3.3 V					
200	27	250	56	200	432
500	10	150	47	80.6 or open	432
1000	4.7	100	33	39.2	432
2200	2.2	47	22	17.8	432
V_{OUT} = 5 V					
200	33	200	68	200	249
500	15	100	47	80.6 or open	249
1000	6.8	47	47	39.2	249
2200	3.3	33	33	17.8	249
V_{OUT} = 12 V					
200	56	68	see note (5)	200	90.9
500	22	47	68	80.6 or open	90.9
1000	10	33	47	39.2	90.9
V_{OUT} = 24 V					
200	180	68	see note (5)	200	43.2
500	47	47	see note (5)	80.6 or open	43.2
1000	22	33	see note (5)	39.2	43.2

(1) Inductor values are calculated based on typical V_{IN} = 24 V.
(2) All the C_{OUT} values are after derating. Add more when using ceramics.
(3) R_{FBT} = 0 Ω for V_{OUT} = 1 V. R_{FBT} = 1 MΩ for all other V_{OUT} settings.
(4) For designs with R_{FBT} other than 1 MΩ, adjust C_{FF} so that ($C_{FF} \times R_{FBT}$) is unchanged, and adjust R_{FBB} so that (R_{FBT} / R_{FBB}) is unchanged.
(5) High ESR C_{OUT} provides enough phase boost, and C_{FF} is not needed.

Typical Applications (continued)

8.2.1 Design Requirements

A detailed design procedure is described based on a design example. For this design example, use the parameters listed in Table 3 as the input parameters.

Table 3. Design Example Parameters

DESIGN PARAMETER	VALUE
Input voltage V_{IN}	24 V typical, range from 3.8 V to 60 V
Output voltage V_{OUT}	3.3 V
Input ripple voltage	400 mV
Output ripple voltage	30 mV
Output current rating	2 A
Operating frequency	500 kHz
Soft-start time	10 ms

8.2.2 Detailed Design Procedure

8.2.2.1 Custom Design With WEBENCH® Tools

Click here to create a custom design using the LM46002 device with the WEBENCH® Power Designer.

1. Start by entering the input voltage (V_{IN}), output voltage (V_{OUT}), and output current (I_{OUT}) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance
- Run thermal simulations to understand board thermal performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

8.2.2.2 Output Voltage Setpoint

The output voltage of the LM46002 device is externally adjustable using a resistor divider network. The divider network is comprised of top feedback resistor R_{FBT} and bottom feedback resistor R_{FBB}. Use Equation 11 to determine the output voltage of the converter:

$$R_{FBB} = \frac{V_{FB}}{V_{OUT} - V_{FB}} R_{FBT} \tag{11}$$

Choose the value of the R_{FBT} to be 1 MΩ to minimize quiescent current to improve light load efficiency in this application. With the desired output voltage set to be 3.3 V and the V_{FB} = 1.011 V, the R_{FBB} value can then be calculated using Equation 11. The formula yields a value of 434.78 kΩ. Choose the closest available value of 432 kΩ for the R_{FBB}. See *Adjustable Output Voltage* for more details.

8.2.2.3 Switching Frequency

The default switching frequency of the LM46002 device is set at 500 kHz when RT pin is open circuit. The switching frequency is selected to be 500 kHz in this application for one less passive components. If other frequency is desired, use Equation 12 to calculate the required value for R_T.

$$R_T(k\Omega) = 40200 / \text{Freq (kHz)} - 0.6 \quad (12)$$

For 500 kHz, the calculated R_T is 79.8 kΩ and standard value 80.6 kΩ can also be used to set the switching frequency at 500 kHz.

8.2.2.4 Input Capacitors

The LM46002 device requires high frequency input decoupling capacitor(s) and a bulk input capacitor, depending on the application. The typical recommended value for the high frequency decoupling capacitor is 4.7 µF to 10 µF. A high-quality ceramic type X5R or X7R with sufficiency voltage rating is recommended. The voltage rating must be greater than the maximum input voltage. To compensate the derating of ceramic capacitors, a voltage rating of twice the maximum input voltage is recommended. Additionally, some bulk capacitance can be required, especially if the LM46002 circuit is not located within approximately 5 cm from the input voltage source. This capacitor is used to provide damping to the voltage spiking due to the lead inductance of the cable or trace. The value for this capacitor is not critical but must be rated to handle the maximum input voltage including ripple.

For this design, a 10 µF, X7R dielectric capacitor rated for 100 V is used for the input decoupling capacitor. The equivalent series resistance (ESR) is approximately 3 mΩ, and the current-rating is 3 A. Include a capacitor with a value of 0.1 µF for high-frequency filtering and place it as close as possible to the device pins.

NOTE

DC bias effect: High-capacitance ceramic capacitors have a DC bias effect, which has a strong influence on the final effective capacitance. Therefore, choose the right capacitor value carefully. Package size and voltage rating in combination with dielectric material are responsible for differences between the rated capacitor value and the effective capacitance.

8.2.2.5 Inductor Selection

The first criterion for selecting an output inductor is the inductance itself. In most buck converters, this value is based on the desired peak-to-peak ripple current, Δi_L, that flows in the inductor along with the DC load current. As with switching frequency, the selection of the inductor is a tradeoff between size and cost. Higher inductance gives lower ripple current and hence lower output voltage ripple with the same output capacitors. Lower inductance could result in smaller, less expensive component. An inductance that gives a ripple current of 20% to 40% of the 2 A at the typical supply voltage is a good starting point. Δi_L = (1/5 to 2/5) × I_{OUT}. The peak-to-peak inductor current ripple can be found by Equation 13, and the range of inductance can be found by Equation 14 with the typical input voltage used as V_{IN}.

$$\Delta i_L = \frac{(V_{IN} - V_{OUT}) \times D}{L \times F_S} \quad (13)$$

$$\frac{(V_{IN} - V_{OUT}) \times D}{0.4 \times F_S \times I_{L-MAX}} \le L \le \frac{(V_{IN} - V_{OUT}) \times D}{0.2 \times F_S \times I_{L-MAX}} \quad (14)$$

D is the duty cycle of the converter which in a buck converter it can be approximated as D = V_{OUT} / V_{IN}, assuming no loss power conversion. By calculating in terms of amperes, volts, and megahertz, the inductance value comes out in micro henries. The inductor ripple current ratio is defined by:

$$r = \frac{\Delta i_L}{I_{OUT}} \tag{15}$$

The second criterion is the inductor saturation current rating. The inductor must be rated to handle the maximum load current plus the ripple current:

$$I_{L\text{-}PEAK} = I_{LOAD\text{-}MAX} + \Delta\ i_L / 2 \tag{16}$$

The LM46002 has both valley current limit and peak current limit. During an instantaneous short, the peak inductor current can be high due to a momentary increase in duty cycle. The inductor current rating must be higher than the HS current limit. It is advised to select an inductor with a larger core saturation margin and preferably a softer rolloff of the inductance value over load current.

In general, lower inductance in switching power supplies is the best choice because it usually corresponds to faster transient response, smaller DCR, and reduced size for more compact designs. But an inductance that is too low can generate an inductor current ripple that is too large so that overcurrent protection at the full load could be falsely triggered. It also generates more conduction loss, since the RMS current is slightly higher relative that with lower current ripple at the same DC current. Larger inductor current ripple also implies larger output voltage ripple with the same output capacitors. With peak-current-mode control, TI does not recommend having an inductor current ripple that is too small. Enough inductor current ripple improves signal-to-noise ratio on the current comparator and makes the control loop more immune to noise.

Once the inductance is determined, the type of inductor must be selected. Ferrite designs have very low core losses and are preferable at high switching frequencies, so design goals can concentrate on copper loss and preventing saturation. Ferrite core material saturates hard, which means that inductance collapses abruptly when the peak design current is exceeded. The 'hard' saturation results in an abrupt increase in inductor ripple current and consequent output voltage ripple. Do not allow the core to saturate!

For the design example, a standard 10-µH inductor from Wurth, Coiltronics, or Vishay can be used for the 3.3-V output with plenty of current-rating margin.

8.2.2.6 Output Capacitor Selection

The device is designed to be used with a wide variety of LC filters. Use as little output capacitance as possible to keep cost and size down. Choose the output capacitor(s), C_{OUT}, with care because C_{OUT} directly affects the steady-state output voltage ripple, loop stability, and the voltage over/undershoot during load current transients.

The output voltage ripple is essentially composed of two parts. One is caused by the inductor current ripple going through the ESR of the output capacitors:

$$\Delta V_{OUT\text{-}ESR} = \Delta i_L \times ESR \tag{17}$$

The other is caused by the inductor current ripple charging and discharging the output capacitors:

$$\Delta V_{OUT\text{-}C} = \Delta i_L / (8 \times F_S \times C_{OUT}) \tag{18}$$

The two components in the voltage ripple are not in phase, so the actual peak-to-peak ripple is smaller than the sum of the two peaks.

Output capacitance is usually limited by transient performance specifications if the system requires tight voltage regulation in the presence of large current steps and fast slew rates. When a fast large load transient happens, output capacitors provide the required charge before the inductor current can slew to the appropriate level. The initial output voltage step is equal to the load current step multiplied by the ESR. VOUT continues to droop until the control loop response increases or decreases the inductor current to supply the load. To maintain a small over- or under-shoot during a transient, small ESR and large capacitance are desired. But these also come with higher cost and size. Thus, the motivation is to seek a fast control loop response to reduce the output voltage deviation.

For a given input and output requirement, the following inequality gives an approximation for an absolute minimum output cap required:

$$C_{OUT} > \frac{1}{(F_S \times r \times \Delta V_{OUT} / I_{OUT})} \times \left[\left(\frac{r^2}{12} \times (1 + D')\right) + (D' \times (1 + r))\right] \quad (19)$$

Along with this for the same requirement, the max ESR should be calculated as per the following inequality

$$ESR < \frac{D'}{F_S \times C_{OUT}} \times (\frac{1}{r} + 0.5)$$

where
- r = Ripple ratio of the inductor ripple current (ΔI_L / I_{OUT})
- ΔV_{OUT} = target output voltage undershoot
- D' = 1 – duty cycle
- F_S = switching frequency
- I_{OUT} = load current (20)

A general guide line for C_{OUT} range is that C_{OUT} should be larger than the minimum required output capacitance calculated by Equation 19, and smaller than 10 times the minimum required output capacitance or 1 mF. In applications with V_{OUT} less than 3.3 V, it is critical that low ESR output capacitors are selected. This will limit potential output voltage overshoots as the input voltage falls below the device normal operating range. To optimize the transient behavior a feed-forward capacitor could be added in parallel with the upper feedback resistor. For this design example, three 47-µF,10-V, X7R ceramic capacitors are used in parallel.

8.2.2.7 Feed-Forward Capacitor

The LM46002 is internally compensated and the internal R-C values are 400 kΩ and 50 pF, respectively. Depending on the V_{OUT} and frequency F_S, if the output capacitor C_{OUT} is dominated by low ESR (ceramic types) capacitors, it could result in low phase margin. To improve the phase boost an external feedforward capacitor C_{FF} can be added in parallel with R_{FBT}. C_{FF} is chosen such that phase margin is boosted at the crossover frequency without C_{FF}. A simple estimation for the crossover frequency without C_{FF} (f_x) is shown in Equation 21, assuming C_{OUT} has very small ESR.

$$f_x = \frac{4.35}{V_{OUT} \times C_{OUT}} \quad (21)$$

Equation 22 was tested for C_{FF} was tested:

$$C_{FF} = \frac{1}{2\pi f_x} \times \frac{1}{\sqrt{R_{FBT} \times (R_{FBT} // R_{FBB})}} \quad (22)$$

Equation 22 indicates that the crossover frequency is geometrically centered on the zero and pole frequencies caused by the C_{FF} capacitor.

For designs with higher ESR, C_{FF} is not necessary when C_{OUT} has very high ESR and C_{FF} calculated from Equation 22 should be reduced with medium ESR. Table 2 can be used as a quick starting point.

For the application in this design example, a 47-pF COG capacitor is selected.

8.2.2.8 Bootstrap Capacitors

Every LM46002 design requires a bootstrap capacitor, C_{BOOT}. The recommended bootstrap capacitor is 0.47 µF and rated at 6.3 V or higher. The bootstrap capacitor is located between the SW pin and the CBOOT pin. The bootstrap capacitor must be a high-quality ceramic type with X7R or X5R grade dielectric for temperature stability.

8.2.2.9 VCC Capacitor

The VCC pin is the output of an internal LDO for LM46002. The input for this LDO comes from either VIN or BIAS (see *Functional Block Diagram* for LM46002). To insure stability of the part, place a minimum of 2.2-µF, 10-V capacitor from this pin to ground.

8.2.2.10 BIAS Capacitors

For an output voltage of 3.3 V and greater, the BIAS pin can be connected to the output in order to increase light load efficiency. This pin is an input for the VCC LDO. When BIAS is not connected, the input for the VCC LDO will be internally connected into VIN. Because this is an LDO, the voltage differences between the input and output will affect the efficiency of the LDO. If necessary, a capacitor with a value of 1 µF can be added close to the BIAS pin as an input capacitor for the LDO.

8.2.2.11 Soft-Start Capacitors

The user can leave the SS/TRK pin floating, and the LM46002 will implement a soft-start time of 4.1 ms typically. In order to use an external soft-start capacitor, size the capacitor such that the soft start time will be longer than 4.1 ms. Use Equation 23 to calculate the soft-start capacitor value:

$$C_{SS} = I_{SSC} \times t_{SS} \tag{23}$$

where

- C_{SS} = soft-start capacitor value (µF)
- I_{SSC} = soft-start charging current (µA)
- t_{SS} = desired soft-start time (s)

For the desired soft start time of 10 ms and soft-start charging current of 2.2 µA, Equation 23 yield a soft start capacitor value of 0.022 µF.

8.2.2.12 Undervoltage Lockout Setpoint

The undervoltage lockout (UVLO) is adjusted using the external voltage divider network of R_{ENT} and R_{ENB}. R_{ENT} is connected between the VIN pin and the EN pin of the LM46002. R_{ENB} is connected between the EN pin and the GND pin. The UVLO has two thresholds, one for power up when the input voltage is rising and one for power down or brown outs when the input voltage is falling. The following equation can be used to determine the VIN UVLO level.

$$V_{IN\text{-}UVLO\text{-}RISING} = V_{ENH} \times (R_{ENB} + R_{ENT}) / R_{ENB} \tag{24}$$

The EN rising threshold (V_{ENH}) for LM46002 is set to be 2.1 V (typical). Choose the value of R_{ENB} to be 1 MΩ to minimize input current from the supply. If the desired VIN UVLO level is at 5 V, then the value of R_{ENT} can be calculated using Equation 25:

$$R_{ENT} = (V_{IN\text{-}UVLO\text{-}RISING} / V_{ENH} - 1) \times R_{ENB} \tag{25}$$

Equation 25 yields a value of 1.38 MΩ. The resulting falling UVLO threshold, equals 4.3 V, can be calculated by below equation, where EN falling threshold (V_{ENL}) is 1.8 V (typical).

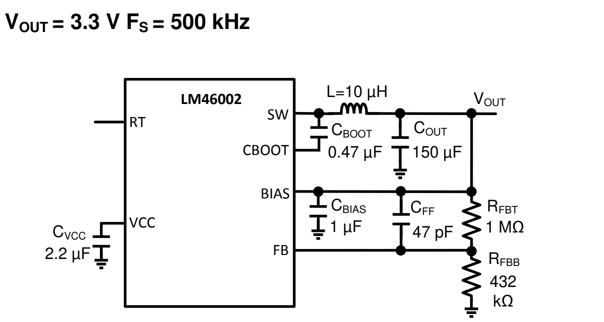
$$V_{IN\text{-}UVLO\text{-}FALLING} = V_{ENL} \times (R_{ENB} + R_{ENT}) / R_{ENB} \tag{26}$$

8.2.2.13 PGOOD

A typical pull-up resistor value is 10 kΩ to 100 kΩ from the PGOOD pin to a voltage no higher than 12 V. If it is desired to pull up the PGOOD pin to a voltage higher than 12 V, a resistor can be added from the PGOOD pin to ground to divide the voltage seen by the PGOOD pin to a value no higher than 12 V.

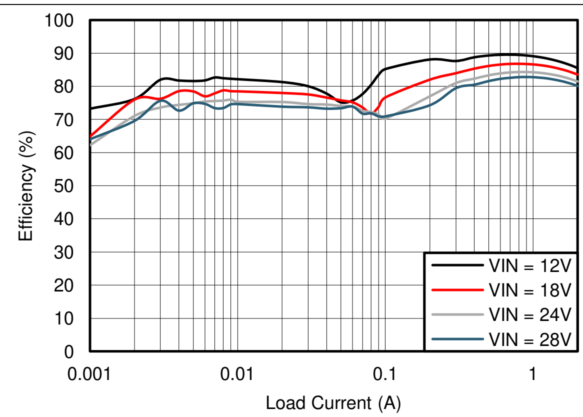
8.2.3 Application Performance Curves

Please refer to Table 2 for bill of materials for each V_{OUT} and F_S combination. Unless otherwise stated, application performance curves were taken at T_A = 25 °C.



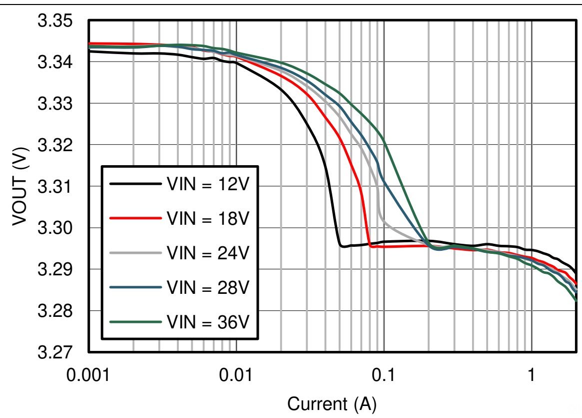
V_{OUT} = 3.3 V F_S = 500 kHz V_{IN} = 24 V

Figure 47. BOM for V_{OUT} = 3.3 V F_S = 500 kHz



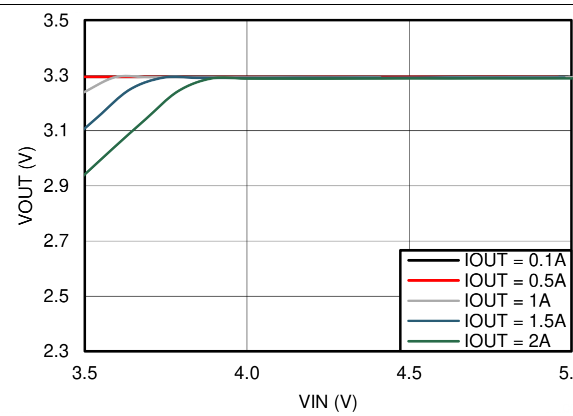
V_{OUT} = 3.3 V F_S = 500 kHz

Figure 48. Efficiency



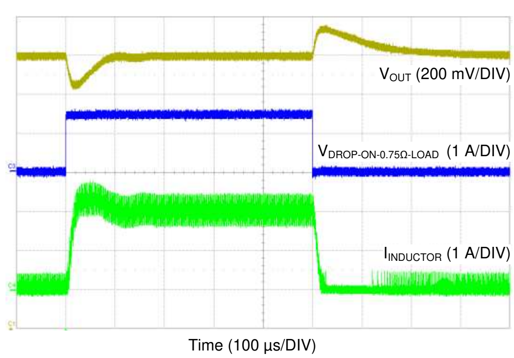
V_{OUT} = 3.3 V F_S = 500 kHz

Figure 49. Output Voltage Regulation



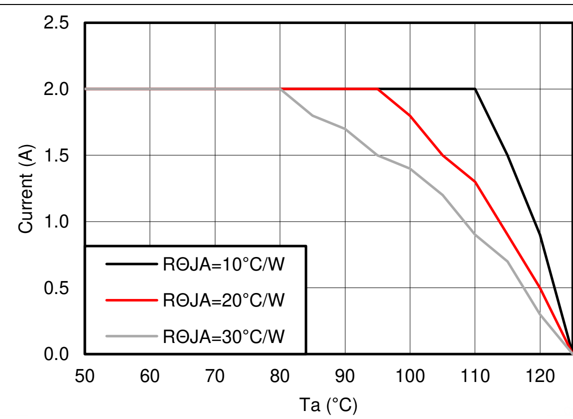
V_{OUT} = 3.3 V F_S = 500 kHz

Figure 50. Drop-Out Curve



V_{OUT} = 3.3 V F_S = 500 kHz V_{IN} = 24 V

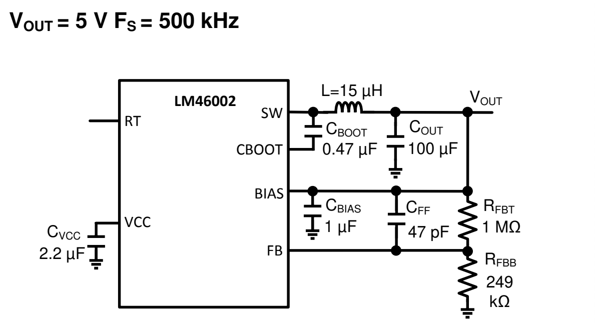
Figure 51. Load Transient Between 0.1 A and 2 A



V_{OUT} = 3.3 V F_S = 500 kHz V_{IN} = 24 V

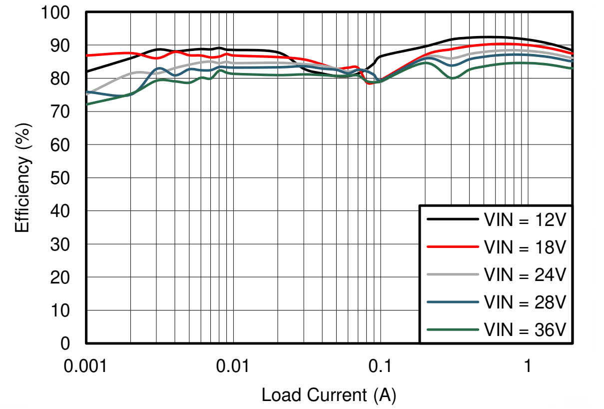
Figure 52. Derating Curve

Please refer to Table 2 for bill of materials for each V_{OUT} and F_S combination. Unless otherwise stated, application performance curves were taken at T_A = 25 °C.



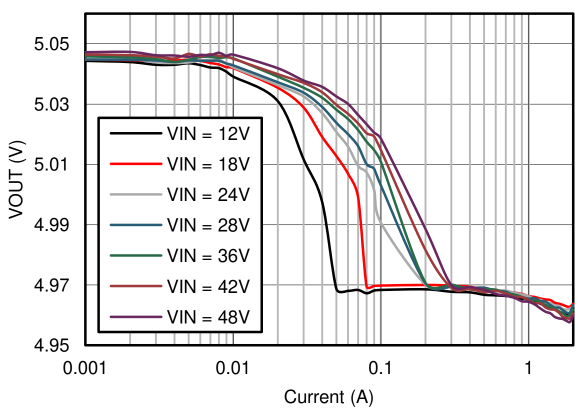
V_{OUT} = 5 V F_S = 500 kHz V_{IN} = 24 V

Figure 53. BOM for V_{OUT} = 5 V F_S = 500 kHz



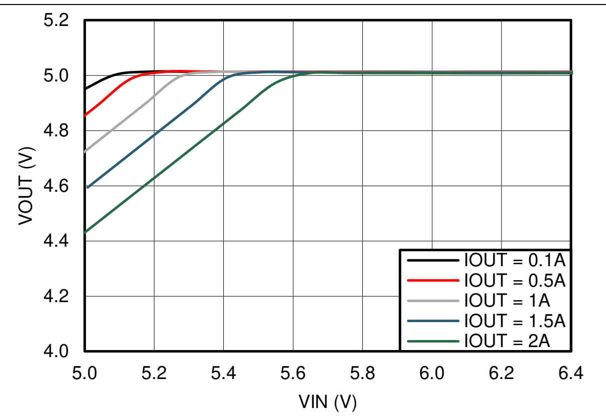
V_{OUT} = 5 V F_S = 500 kHz

Figure 54. Efficiency



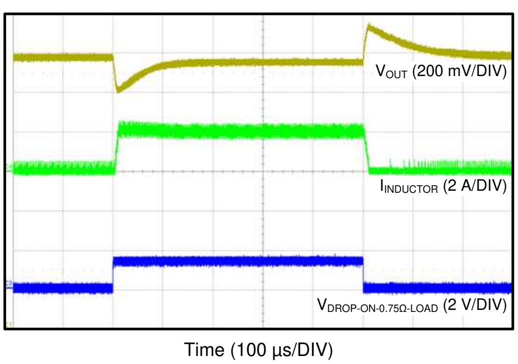
V_{OUT} = 5 V F_S = 500 kHz

Figure 55. Output Voltage Regulation



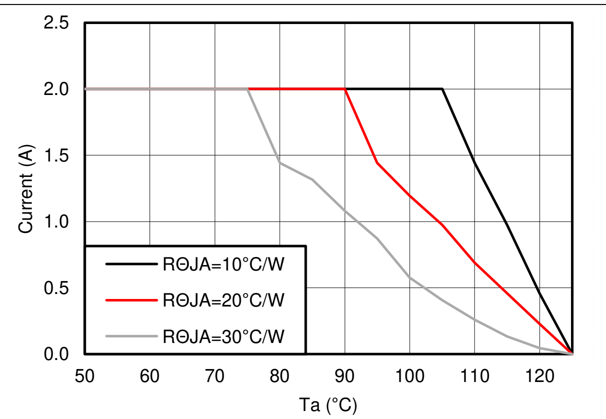
V_{OUT} = 5 V F_S = 500 kHz

Figure 56. Dropout Curve



V_{OUT} = 5 V F_S = 500 kHz V_{IN} = 24 V

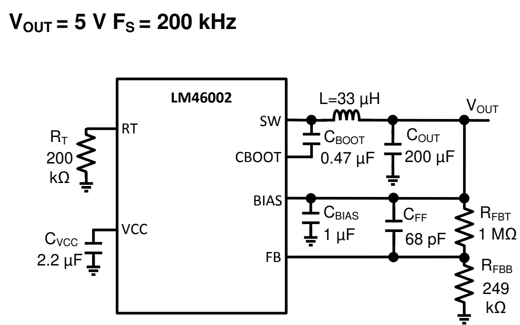
Figure 57. Load Transient Between 0.1 A and 2 A



V_{OUT} = 5 V F_S = 500 kHz V_{IN} = 24 V

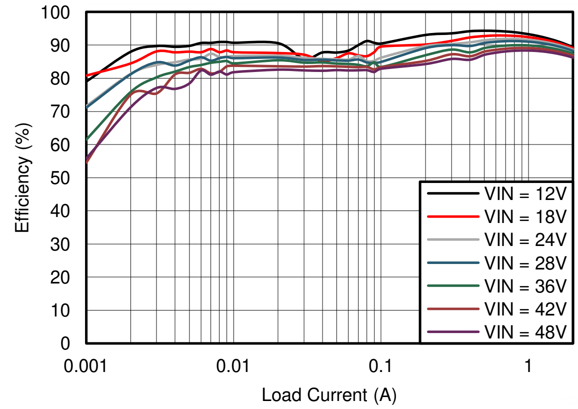
Figure 58. Derating Curve

Please refer to Table 2 for bill of materials for each V_{OUT} and F_S combination. Unless otherwise stated, application performance curves were taken at T_A = 25 °C.



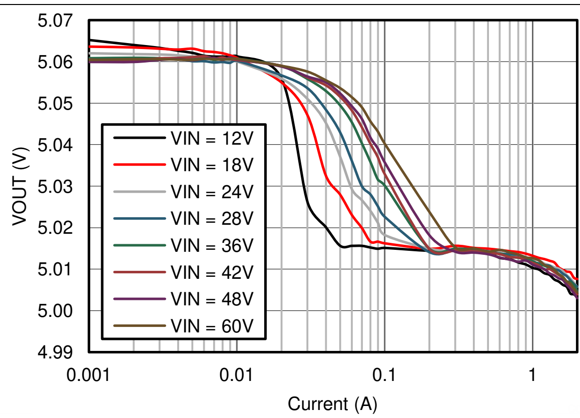
V_{OUT} = 5 V F_S = 200 kHz V_{IN} = 24 V

Figure 59. BOM for V_{OUT} = 5 V F_S = 200 kHz



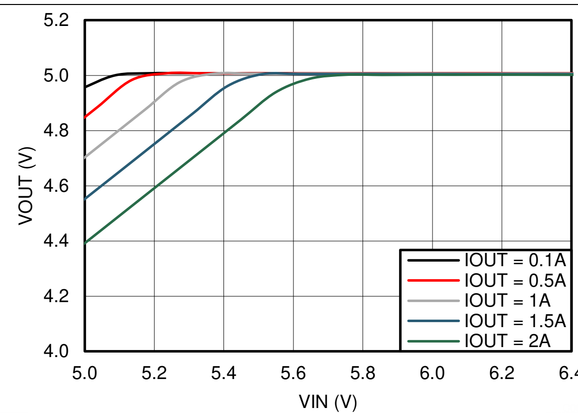
V_{OUT} = 5 V F_S = 200 kHz

Figure 60. Efficiency



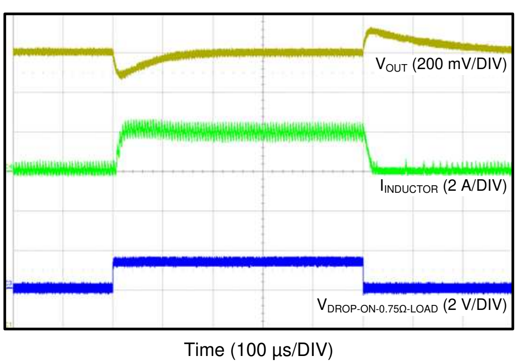
V_{OUT} = 5 V F_S = 200 kHz

Figure 61. Output Voltage Regulation



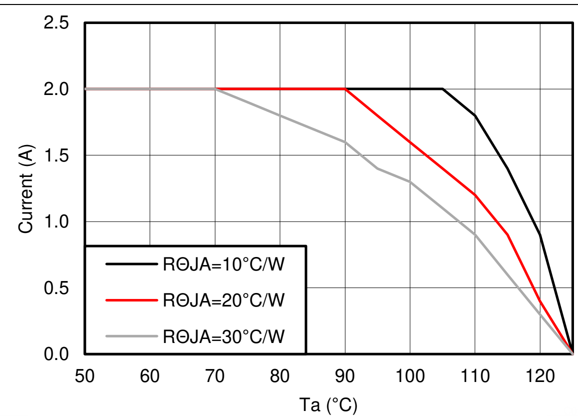
V_{OUT} = 5 V F_S = 200 kHz

Figure 62. Dropout Curve



V_{OUT} = 5 V F_S = 200 kHz V_{IN} = 24 V

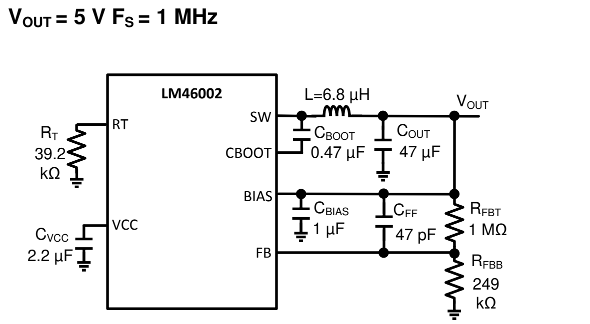
Figure 63. Load Transient Between 0.1 A and 2 A



V_{OUT} = 5 V F_S = 200 kHz

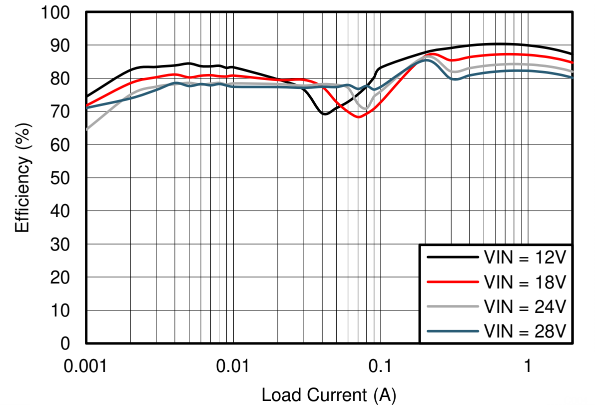
Figure 64. Derating Curve

Please refer to Table 2 for bill of materials for each V_{OUT} and F_S combination. Unless otherwise stated, application performance curves were taken at T_A = 25 °C.



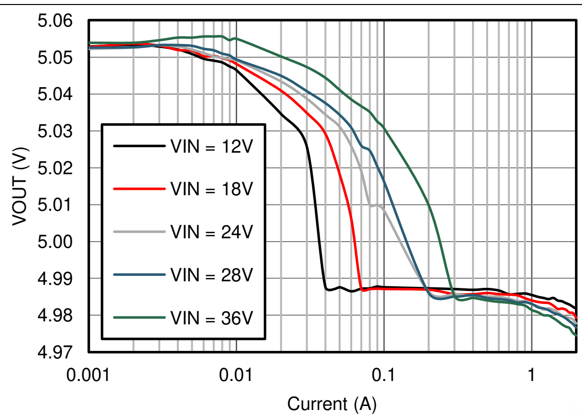
V_{OUT} = 5 V F_S = 1 MHz V_{IN} = 24 V

Figure 65. BOM for V_{OUT} = 5 V F_S = 1 MHz



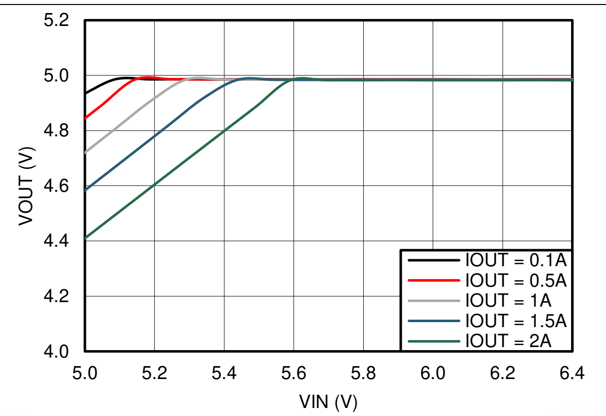
V_{OUT} = 5 V F_S = 1 MHz V_{IN} = 24 V

Figure 66. Efficiency



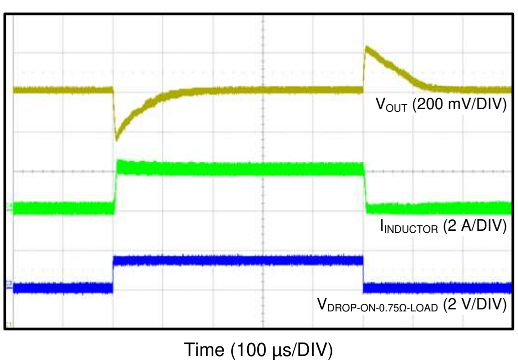
V_{OUT} = 5 V F_S = 1 MHz

Figure 67. Output Voltage Regulation



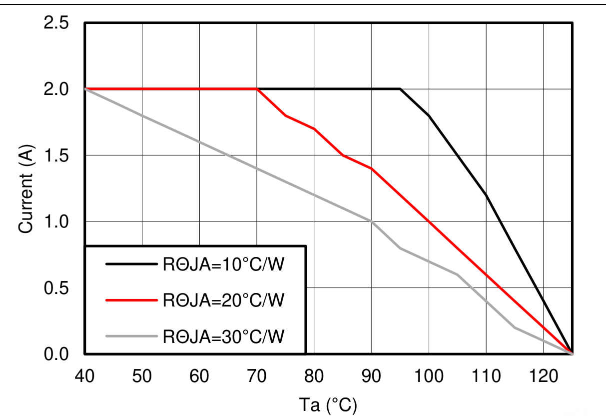
V_{OUT} = 5 V F_S = 1 MHz

Figure 68. Dropout Curve



V_{OUT} = 5 V F_S = 1 MHz V_{IN} = 24 V

Figure 69. Load Transient Between 0.1 A and 2 A

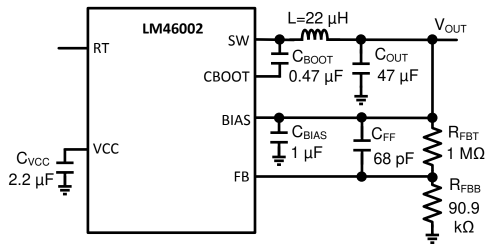


V_{OUT} = 5 V F_S = 1 MHz V_{IN} = 24 V

Figure 70. Derating Curve

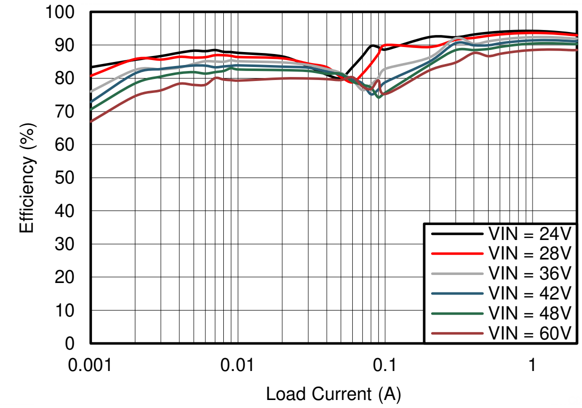
Please refer to Table 2 for bill of materials for each V_{OUT} and F_S combination. Unless otherwise stated, application performance curves were taken at T_A = 25 °C.

V_{OUT} = 12 V F_S = 500 kHz



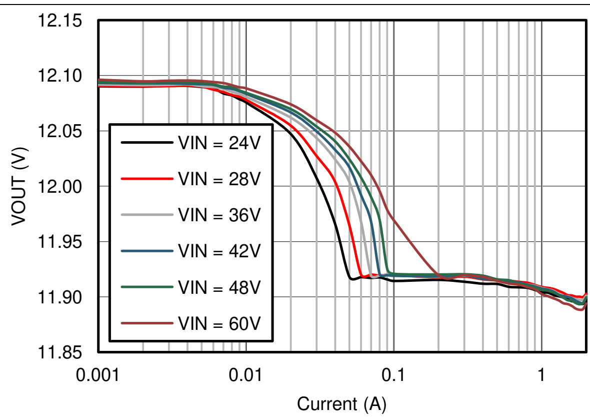
V_{OUT} = 12 V F_S = 500 kHz V_{IN} = 24 V

Figure 71. BOM for V_{OUT} = 12 V F_S = 500 kHz



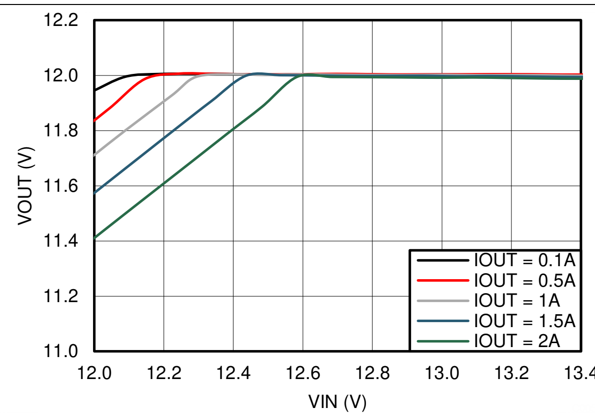
V_{OUT} = 12 V F_S = 500 kHz

Figure 72. Efficiency



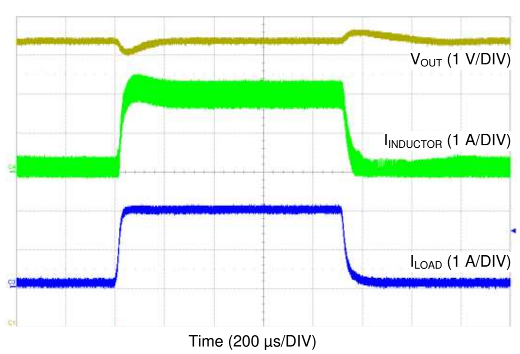
V_{OUT} = 12 V F_S = 500 kHz

Figure 73. Output Voltage Regulation



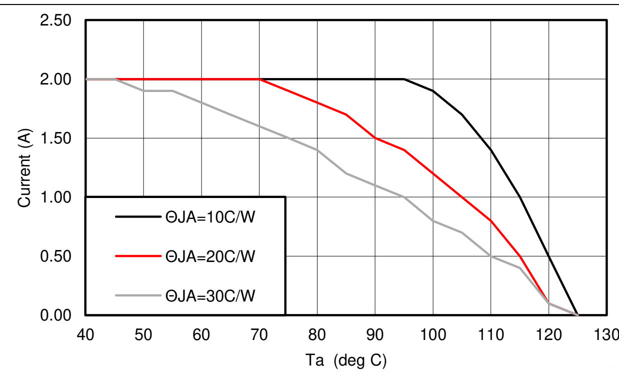
V_{OUT} = 12 V F_S = 500 kHz

Figure 74. Dropout Curve



V_{OUT} = 12 V F_S = 500 kHz V_{IN} = 24 V

Figure 75. Load Transient Between 0.1 A and 2 A

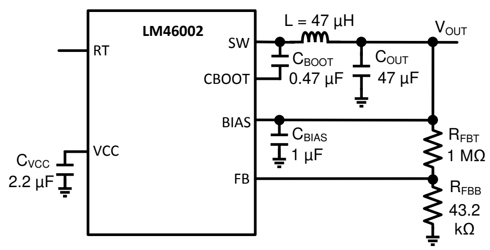


V_{OUT} = 12 V F_S = 500 kHz V_{IN} = 24 V

Figure 76. Derating Curve

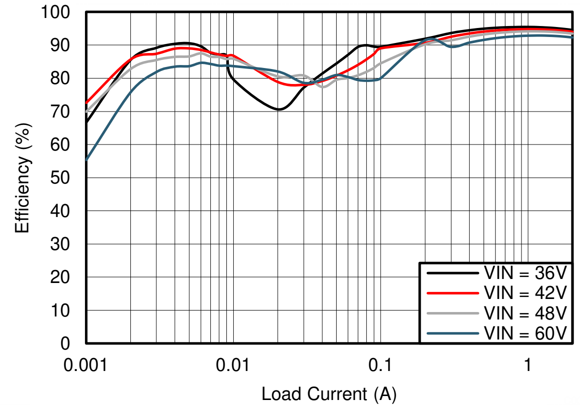
Please refer to Table 2 for bill of materials for each V_{OUT} and F_S combination. Unless otherwise stated, application performance curves were taken at T_A = 25 °C.

V_{OUT} = 24 V F_S = 500 kHz



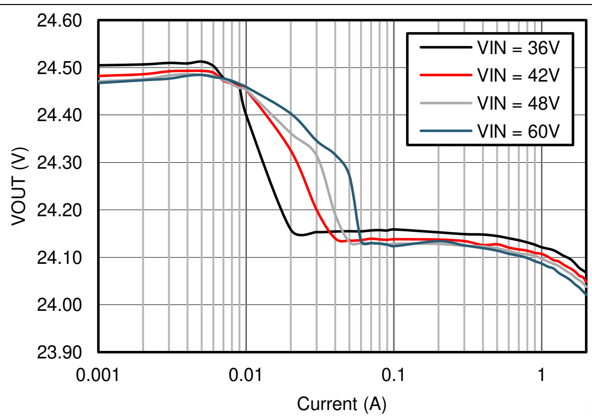
V_{OUT} = 24 V F_S = 500 kHz V_{IN} = 48 V

Figure 77. BOM for V_{OUT} = 24 V F_S = 500 kHz



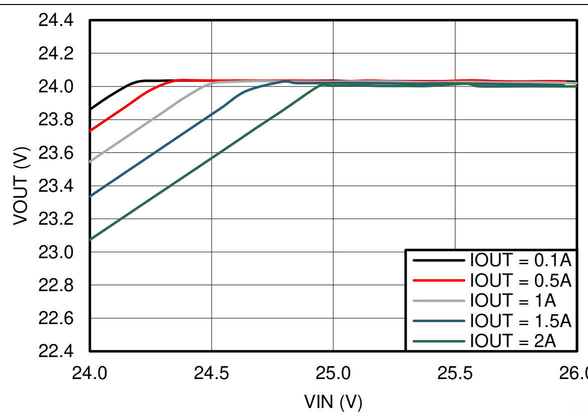
V_{OUT} = 24 V F_S = 500 kHz

Figure 78. Efficiency



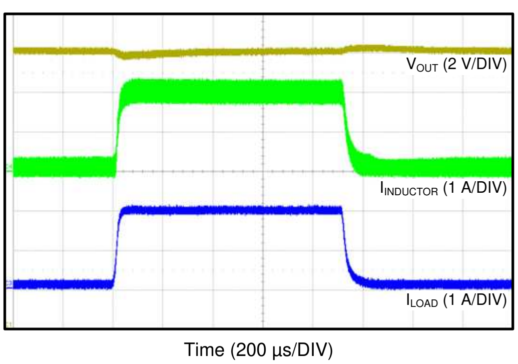
V_{OUT} = 24 V F_S = 500 kHz

Figure 79. Output Voltage Regulation



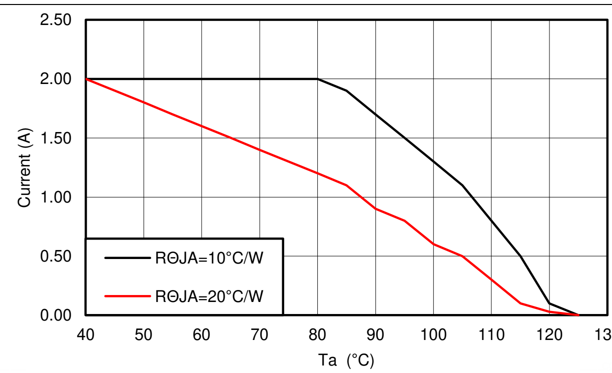
V_{OUT} = 24 V F_S = 500 kHz

Figure 80. Dropout Curve



V_{OUT} = 24 V F_S = 500 kHz V_{IN} = 48 V

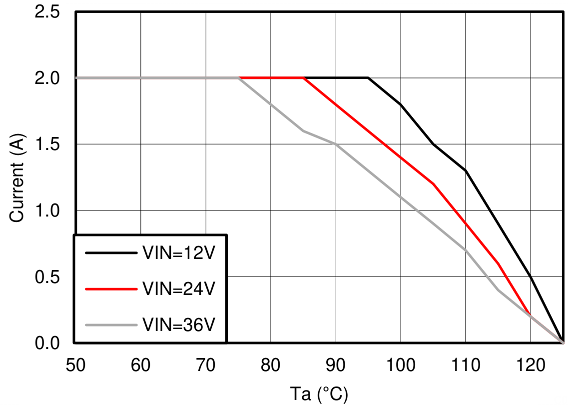
Figure 81. Load Transient Between 0.1 A and 2 A



V_{OUT} = 24 V F_S = 500 kHz V_{IN} = 48 V

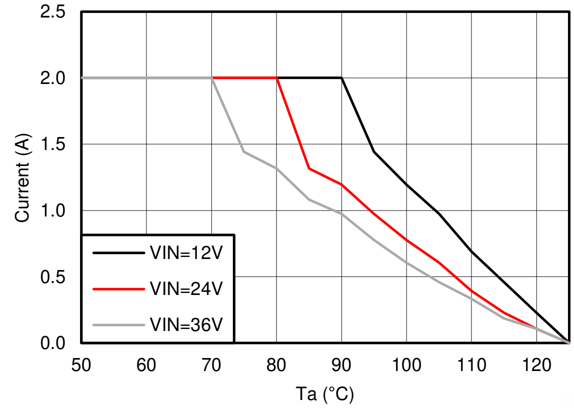
Figure 82. Derating Curve

Please refer to Table 2 for bill of materials for each V_{OUT} and F_S combination. Unless otherwise stated, application performance curves were taken at T_A = 25 °C.



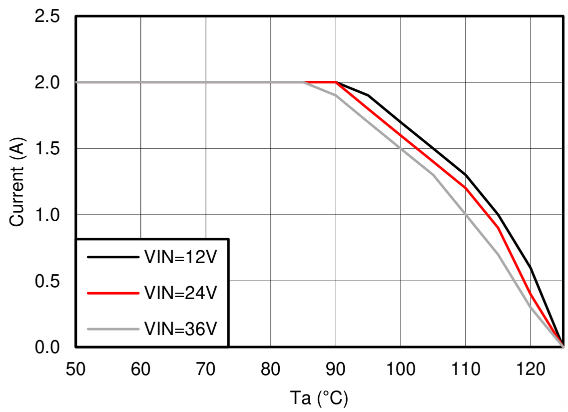
V_{OUT} = 3.3 V F_S = 500 kHz $R_{\theta JA}$ = 20°C/W

Figure 83. Derating Curve with $R_{\theta JA}$ = 20°C/W



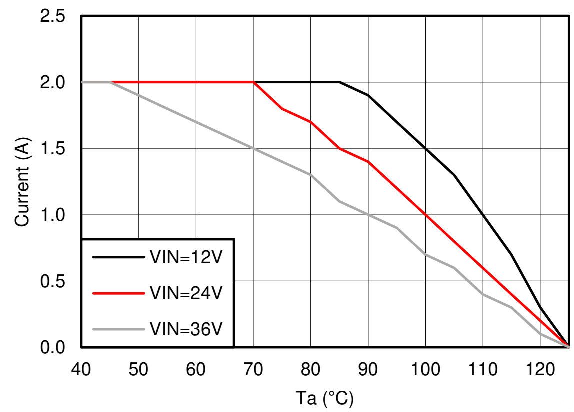
V_{OUT} = 5 V F_S = 500 kHz $R_{\theta JA}$ = 20°C/W

Figure 84. Derating Curve with $R_{\theta JA}$ = 20°C/W



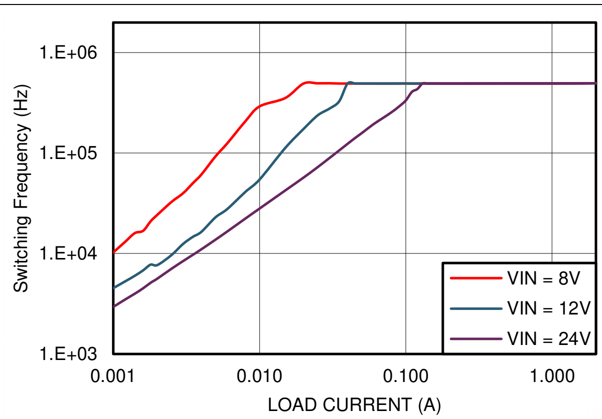
V_{OUT} = 5 V F_S = 200 kHz $R_{\theta JA}$ = 20°C/W

Figure 85. Derating Curve with $R_{\theta JA}$ = 20°C/W



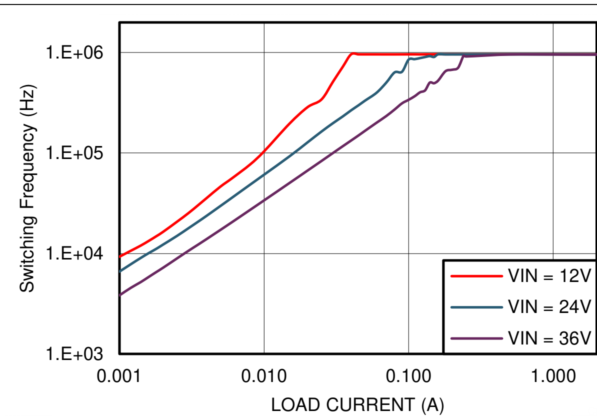
V_{OUT} = 5 V F_S = 1 MHz $R_{\theta JA}$ = 20°C/W

Figure 86. Derating Curve with $R_{\theta JA}$ = 20°C/W



V_{OUT} = 3.3 V F_S = 500 kHz

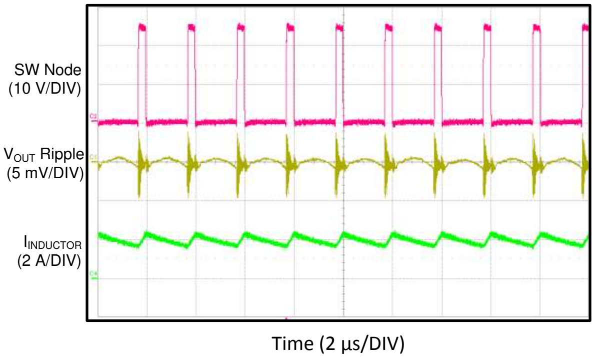
Figure 87. Switching Frequency vs I_{OUT} in PFM Operation



V_{OUT} = 5 V F_S = 1 MHz

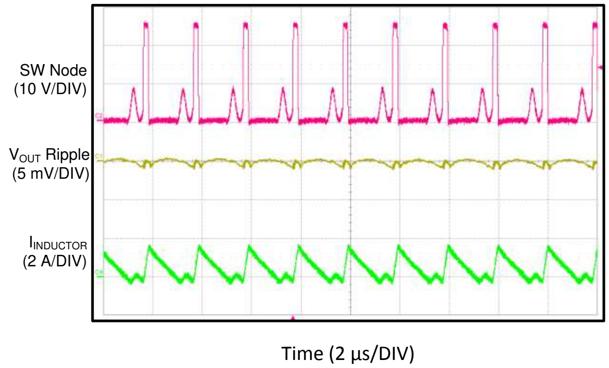
Figure 88. Switching Frequency vs I_{OUT} in PFM Operation

Please refer to Table 2 for bill of materials for each V_{OUT} and F_S combination. Unless otherwise stated, application performance curves were taken at T_A = 25 °C.



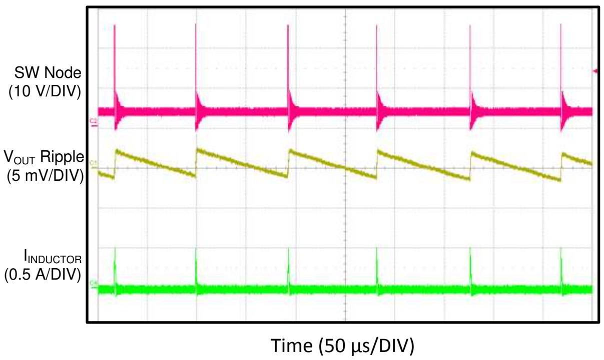
V_{OUT} = 3.3 V F_S = 500 kHz I_{OUT} = 2 A

Figure 89. Switching Waveform in CCM Operation



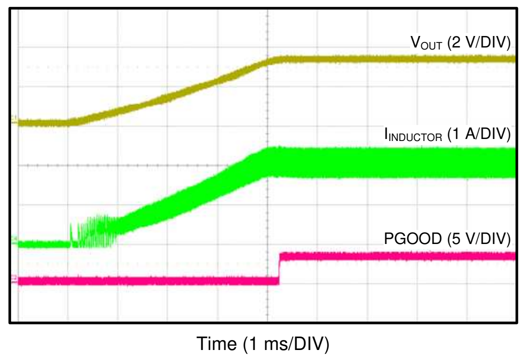
V_{OUT} = 3.3 V F_S = 500 kHz I_{OUT} = 130 mA

Figure 90. Switching Waveform in DCM Operation



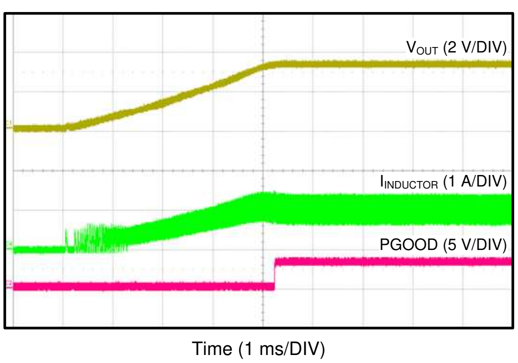
V_{OUT} = 3.3 V F_S = 500 kHz I_{OUT} = 5 mA

Figure 91. Switching Waveform in PFM Operation



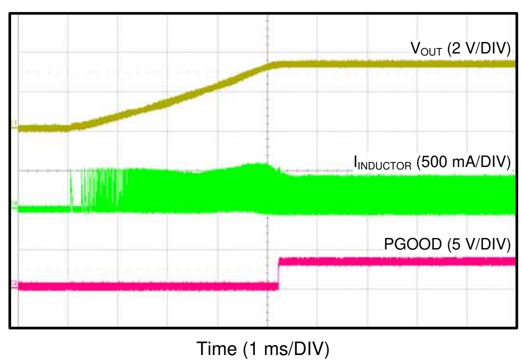
V_{IN} = 24 V V_{OUT} = 3.3 V R_{LOAD} = 1.65 Ω

Figure 92. Startup Into Full Load with Internal Soft-Start Rate



V_{IN} = 24 V V_{OUT} = 3.3 V R_{LOAD} = 3.3 Ω

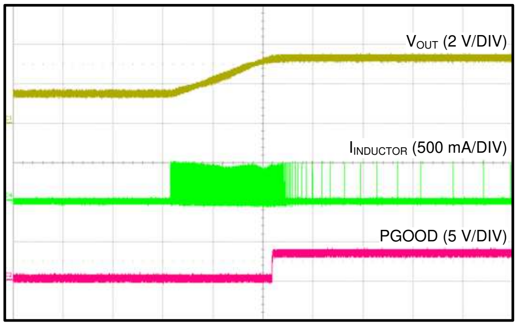
Figure 93. Startup Into Half Load with Internal Soft-Start Rate



V_{IN} = 24 V V_{OUT} = 3.3 V R_{LOAD} = 33 Ω

Figure 94. Startup Into 100 mA with Internal Soft-Start Rate

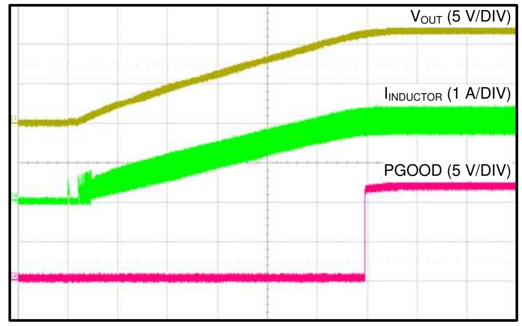
Please refer to Table 2 for bill of materials for each V_{OUT} and F_S combination. Unless otherwise stated, application performance curves were taken at T_A = 25 °C.



Time (1 ms/DIV)

V_{IN} = 24 V V_{OUT} = 3.3 V R_{LOAD} = Open

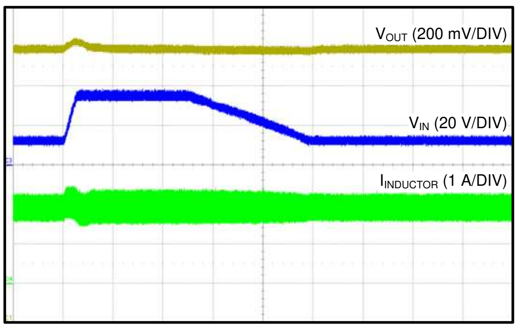
Figure 95. Startup Into 1.5 V Pre-biased Voltage



Time (2 ms/DIV)

V_{IN} = 24 V V_{OUT} = 12 V R_{LOAD} = 6 Ω

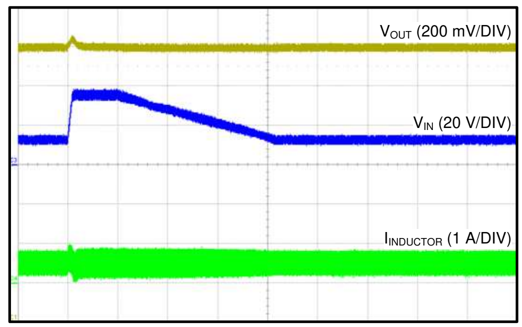
Figure 96. Startup with External Capacitor C_{SS}



Time (200 µs/DIV)

V_{OUT} = 3.3 V F_S = 500 kHz I_{OUT} = 2 A

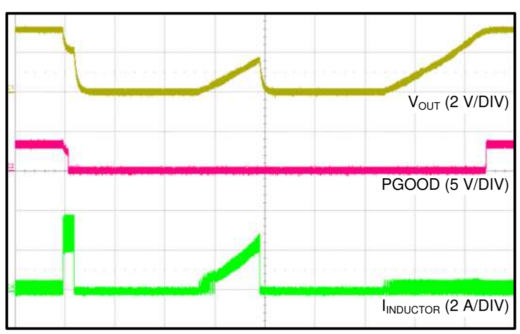
Figure 97. Line Transient: V_{IN} Transitions Between 12 V and 36 V, 1 V/µs Slew Rate



Time (500 µs/DIV)

V_{OUT} = 3.3 V F_S = 500 kHz I_{OUT} = 0.5 A

Figure 98. Line Transient: V_{IN} Transitions Between 12 V and 36 V, 1 V/µs Slew Rate



Time (2 ms/DIV)

V_{OUT} = 3.3 V F_S = 500 kHz V_{IN} = 24 V

Figure 99. Short Circuit Protection and Recover

9 Power Supply Recommendations

The LM46002 is designed to operate from an input voltage supply range between 3.5 V and 60 V. This input supply must be able to withstand the maximum input current and maintain a voltage above 3.5 V. The resistance of the input supply rail must be low enough that an input current transient does not cause a high enough drop at the LM46002 supply voltage that can cause a false UVLO fault triggering and system reset.

If the input supply is located more than a few inches from the LM46002 additional bulk capacitance may be required in addition to the ceramic bypass capacitors. The amount of bulk capacitance is not critical, but a 47-µF or 100-µF electrolytic capacitor is a typical choice.

10 Layout

The performance of any switching converter depends as much upon the layout of the PCB as the component selection. The following guidelines will help users design a PCB with the best power conversion performance, thermal performance, and minimized generation of unwanted EMI.

10.1 Layout Guidelines

1. Place ceramic high frequency bypass C_{IN} as close as possible to the LM46002 VIN and PGND pins. Grounding for both the input and output capacitors must consist of localized top side planes that connect to the PGND pins and PAD.
2. Place bypass capacitors for VCC and BIAS close to the pins and ground the bypass capacitors to device ground.
3. Minimize trace length to the FB pin. Both feedback resistors, R_{FBT} and R_{FBB} should be located close to the FB pin. Place C_{FF} directly in parallel with R_{FBT}. If V_{OUT} accuracy at the load is important, make sure V_{OUT} sense is made at the load. Route V_{OUT} sense path away from noisy nodes and preferably through a layer on the other side of a shieldig layer.
4. Use ground plane in one of the middle layers as noise shielding and heat dissipation path.
5. Have a single point ground connection to the plane. Route the ground connections for the feedback, soft start, and enable components to the ground plane. This prevents any switched or load currents from flowing in the analog ground traces. If not properly handled, poor grounding can result in degraded load regulation or erratic output voltage ripple behavior.
6. Make V_{IN}, V_{OUT} and ground bus connections as wide as possible. This reduces any voltage drops on the input or output paths of the converter and maximizes efficiency.
7. Provide adequate device heat sinking. Use an array of heat-sinking vias to connect the exposed pad to the ground plane on the bottom PCB layer. If the PCB has multiple copper layers, these thermal vias can also be connected to inner layer heat-spreading ground planes. Ensure enough copper area is used for heat sinking to keep the junction temperature below 125°C.

10.1.1 Compact Layout for EMI Reduction

Radiated EMI is generated by the high di/dt components in pulsing currents in switching converters. The larger area covered by the path of a pulsing current, the more electromagnetic emission is generated. The key to minimize radiated EMI is to identify the pulsing current path and minimize the area of the path. In Buck converters,the pulsing current path is from the V_{IN} side of the input capacitors to HS switch, to the LS switch, and then return to the ground of the input capacitors, as shown in Figure 100.

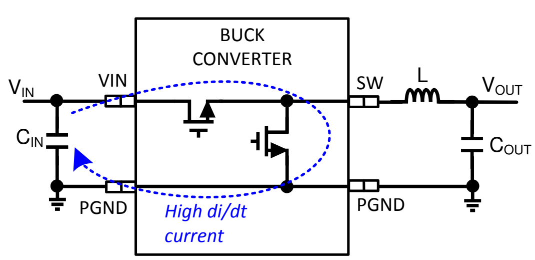


Figure 100. Buck Converter High di / dt Path

Layout Guidelines (continued)

High frequency ceramic bypass capacitors at the input side provide primary path for the high di/dt components of the pulsing current. Placing ceramic bypass capacitor(s) as close as possible to the VIN and PGND pins is the key to EMI reduction.

The SW pin connecting to the inductor must be as short as possible and just wide enough to carry the load current without excessive heating. Short, thick traces or copper pours (shapes) should be used for high current condution path to minimize parasitic resistance. The output capacitors should be place close to the V_{OUT} end of the inductor and closely grounded to PGND pin and exposed PAD.

Place the bypass capacitors on VCC and BIAS pins as close as possible to the pins respectively and closely grounded to PGND and the exposed PAD.

10.1.2 Ground Plane and Thermal Considerations

TI recommends using one of the middle layers as a solid ground plane. Ground plane provides shielding for sensitive circuits and traces. It also provides a quiet reference potential for the control circuitry. The AGND and PGND pins should be connected to the ground plane using vias right next to the bypass capacitors. PGND pins are connected to the source of the internal LS switch. They should be connected directly to the grounds of the input and output capacitors. The PGND net contains noise at the switching frequency and may bounce due to load variations. The PGND trace, as well as PVIN and SW traces, should be constrained to one side of the ground plane. The other side of the ground plane contains much less noise and should be used for sensitive routes.

It is recommended to provide adequate device heat sinking by utilizing the PAD of the IC as the primary thermal path. Use a minimum 4 by 4 array of 10 mil thermal vias to connect the PAD to the system ground plane for heat sinking. The vias should be evenly distributed under the PAD. Use as much copper as possible for system ground plane on the top and bottom layers for the best heat dissipation. It is recommended to use a four-layer board with the copper thickness, for the four layers, starting from the top one, 2 oz / 1 oz / 1 oz / 2 oz. Four layer boards with enough copper thickness and proper layout provides low current conduction impedance, proper shielding and lower thermal resistance.

The thermal characteristics of the LM46002 are specified using the parameter $R_{\theta JA}$, which characterize the junction temperature of the silicon to the ambient temperature in a specific system. Although the value of $R_{\theta JA}$ is dependant on many variables, it still can be used to approximate the operating junction temperature of the device. To obtain an estimate of the device junction temperature, one may use the following relationship:

$$T_J = P_D \times R_{\theta JA} + T_A$$

where

- T_J = junction temperature in °C
- $P_D = V_{IN} \times I_{IN} \times (1 - \text{Efficiency}) - 1.1 \times I_{OUT} \times DCR$
- DCR = inductor DC parasitic resistance in Ω
- $R_{\theta JA}$ = junction-to-ambient thermal resistance of the device in °C/W
- T_A = ambient temperature in °C.
- (27)

The maximum operating junction temperature of the LM46002 is 125°C. $R_{\theta JA}$ is highly related to PCB size and layout, as well as enviromental factors such as heat sinking and air flow. Figure 101 shows measured results of $R_{\theta JA}$ with different copper area on a 2-layer board and a 4-layer board.

Layout Guidelines (continued)

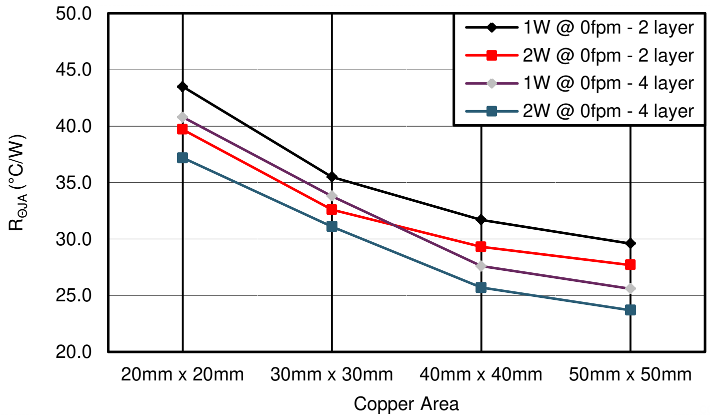


Figure 101. Measured $R_{\theta JA}$ vs PCB Copper Area on a 2-layer Board and a 4-layer Board

10.1.3 Feedback Resistors

To reduce noise sensitivity of the output voltage feedback path, it is important to place the resistor divider and C_{FF} close to the FB pin, rather than close to the load. The FB pin is the input to the error amplifier, so it is a high impedance node and very sensitive to noise. Placing the resistor divider and C_{FF} closer to the FB pin reduces the trace length of FB signal and reduces noise coupling. The output node is a low impedance node, so the trace from V_{OUT} to the resistor divider can be long if short path is not available.

If voltage accuracy at the load is important, make sure voltage sense is made at the load. Doing so will correct for voltage drops along the traces and provide the best output accuracy. The voltage sense trace from the load to the feedback resistor divider should be routed away from the SW node path, the inductor and V_{IN} path to avoid contaminating the feedback signal with switch noise, while also minimizing the trace length. This is most important when high value resistors are used to set the output voltage. TI recommends routing the voltage sense trace on a different layer than the inductor, SW node and V_{IN} path, such that there is a ground plane in between the feedback trace and inductor / SW node / V_{IN} polygon. This provides further shielding for the voltage feedback path from switching noises.

10.2 Layout Example

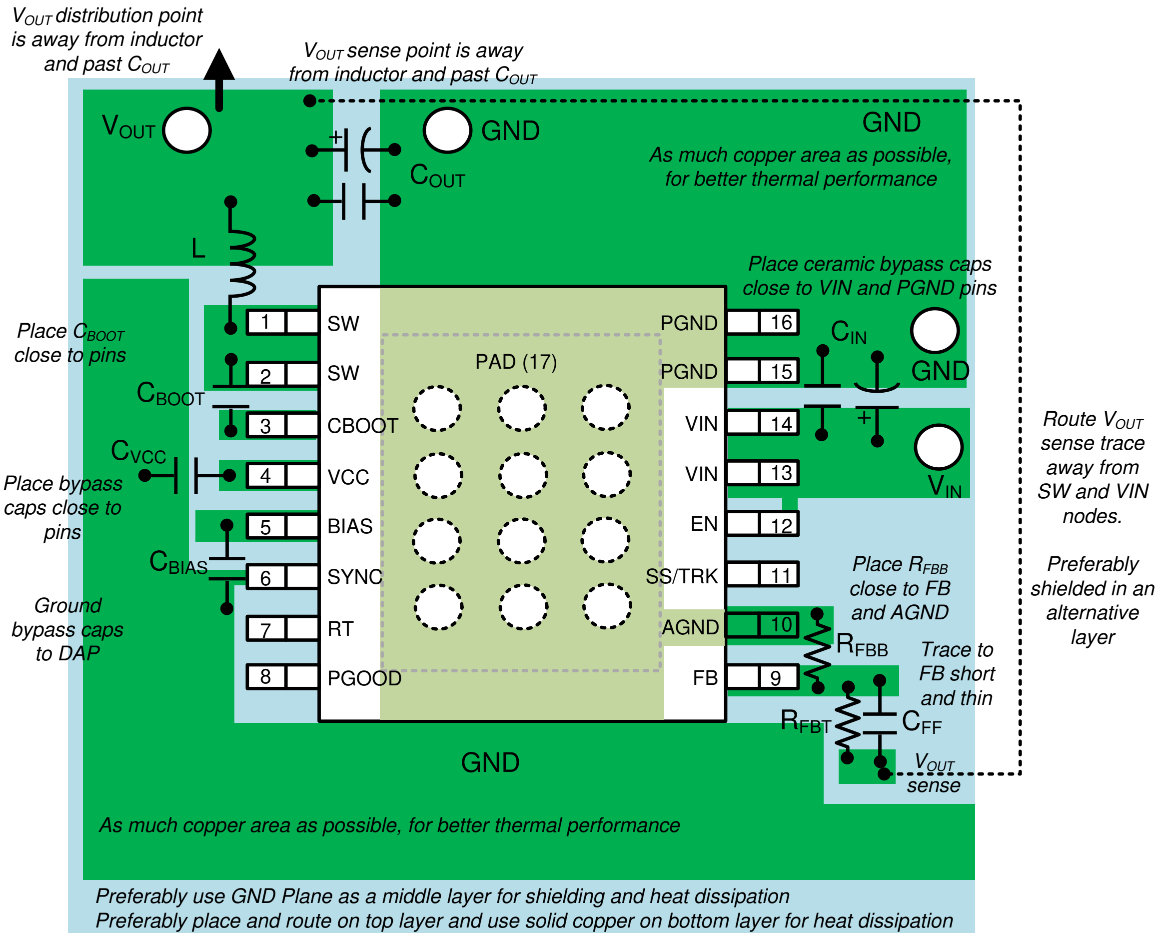


Figure 102. LM46002 PCB Layout Example and Guidelines

11 デバイスおよびドキュメントのサポート

11.1 デバイス・サポート

11.1.1 開発サポート

11.1.1.1 WEBENCH®ツールによるカスタム設計

ここをクリックすると、WEBENCH® Power Designer により、LM46002 デバイスを使用するカスタム設計を作成できます。

1. 最初に、入力電圧(V_{IN})、出力電圧(V_{OUT})、出力電流(I_{OUT})の要件を入力します。
2. オプティマイザのダイヤルを使用して、効率、占有面積、コストなどの主要なパラメータについて設計を最適化します。
3. 生成された設計を、テキサス・インスツルメンツが提供する他の方式と比較します。

WEBENCH Power Designerでは、カスタマイズされた回路図と部品リストを、リアルタイムの価格と部品の在庫情報と併せて参照できます。

通常、次の操作を実行可能です。

- 電気的なシミュレーションを実行し、重要な波形と回路の性能を確認する。
- 熱シミュレーションを実行し、基板の熱特性を把握する。
- カスタマイズされた回路図やレイアウトを、一般的なCADフォーマットで出力する。
- 設計のレポートをPDFで印刷し、設計を共有する。

WEBENCHツールの詳細は、www.ti.com/WEBENCHでご覧になれます。

11.2 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、ti.comのデバイス製品フォルダを開いてください。右上の「アラートを受け取る」をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

11.3 コミュニティ・リソース

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

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これらのデバイスは、限定的なESD(静電破壊)保護機能を内 蔵しています。保存時または取り扱い時は、MOSゲートに対す る静電破壊を防止するために、リード線同士をショートさせて おくか、デバイスを導電フォームに入れる必要があります。

11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。これらの情報は、指定のデバイスに対して提供されている最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LM46002PWP	Active	Production	HTSSOP (PWP) | 16	90 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	LM46002
LM46002PWP.B	Active	Production	HTSSOP (PWP) | 16	90 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	LM46002
LM46002PWPR	Active	Production	HTSSOP (PWP) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	LM46002
LM46002PWPR.B	Active	Production	HTSSOP (PWP) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	LM46002
LM46002PWPRG4	Active	Production	HTSSOP (PWP) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	LM46002
LM46002PWPRG4.B	Active	Production	HTSSOP (PWP) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	LM46002
LM46002PWPT	Active	Production	HTSSOP (PWP) | 16	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	LM46002
LM46002PWPT.B	Active	Production	HTSSOP (PWP) | 16	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	LM46002

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF LM46002 :

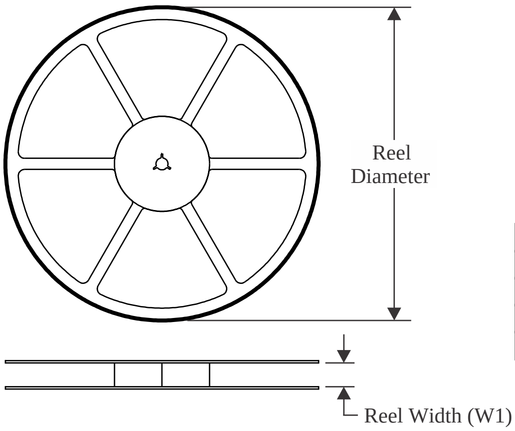
- Automotive : LM46002-Q1

NOTE: Qualified Version Definitions:

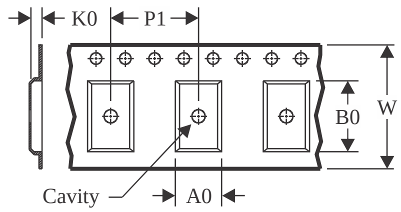
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

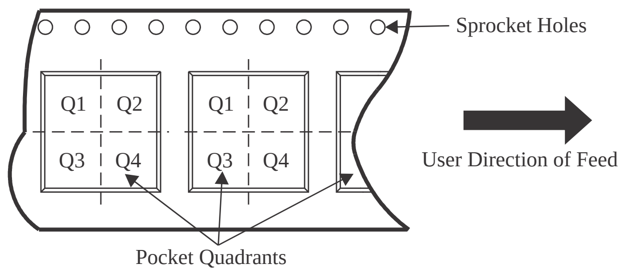


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

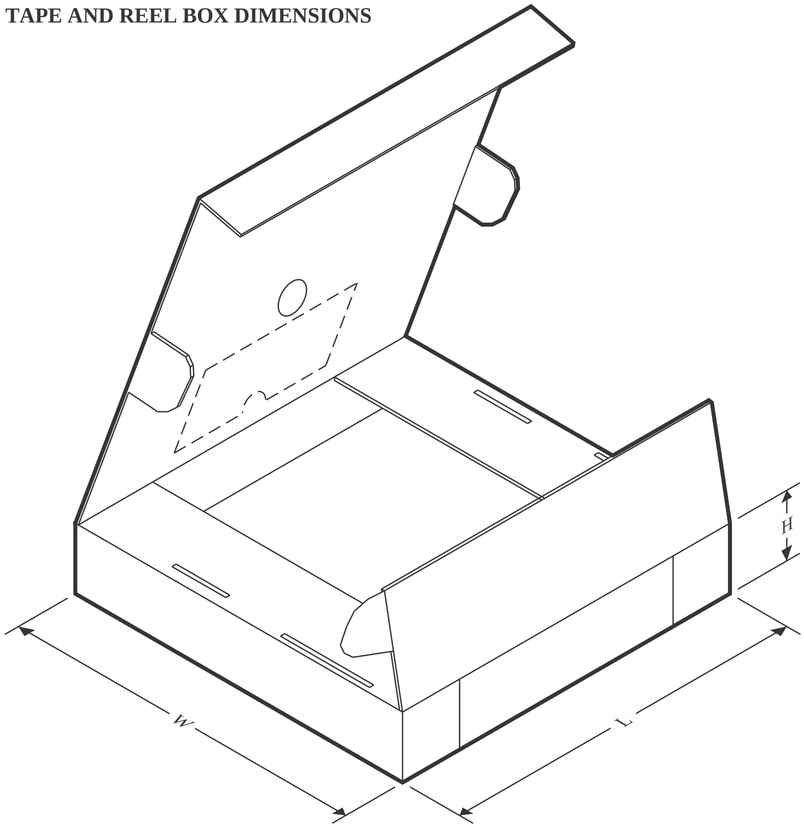
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM46002PWPR	HTSSOP	PWP	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
LM46002PWPRG4	HTSSOP	PWP	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
LM46002PWPT	HTSSOP	PWP	16	250	180.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

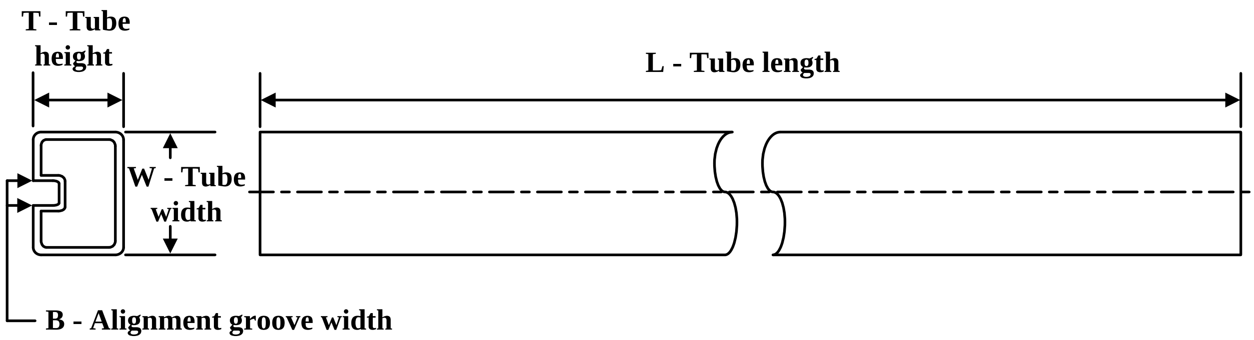
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM46002PWPR	HTSSOP	PWP	16	2000	350.0	350.0	43.0
LM46002PWPRG4	HTSSOP	PWP	16	2000	350.0	350.0	43.0
LM46002PWPT	HTSSOP	PWP	16	250	210.0	185.0	35.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
LM46002PWP	PWP	HTSSOP	16	90	530	10.2	3600	3.5
LM46002PWP.B	PWP	HTSSOP	16	90	530	10.2	3600	3.5