TEXAS INSTRUMENTS
LM5002
JAJSAQ4F – JANUARY 2007 – REVISED MAY 2021

LM5002 入力電圧範囲の広いスイッチング・モード・レギュレータ

1 特長

- 75V N チャネル MOSFET を内蔵
- 非常に広い入力電圧範囲:3.1V～75V
- 高電圧バイアス・レギュレータを内蔵
- 調整可能な出力電圧
- ±1.5% の出力電圧精度
- 電流モード制御、補償を選択可能
- 広帯域幅のエラー・アンプ
- 電流検出および制限機能を内蔵
- スロープ補償機能を内蔵
- 最大デューティ・サイクル制限:85%
- 1 個の抵抗によるオシレータ設定
- オシレータの同期機能
- イネーブルおよび低電圧誤動作防止 (UVLO) ピン
- 8 ピン SOIC パッケージ
- 8 ピン WSON パッケージ
- ヒステリシス付きサーマル・シャットダウン

2 アプリケーション

- 産業用、通信用、車載用アプリケーションの DC/DC 電源
- 昇圧、フライバック、SEPIC、およびフォワード・コンバータ・トポロジ

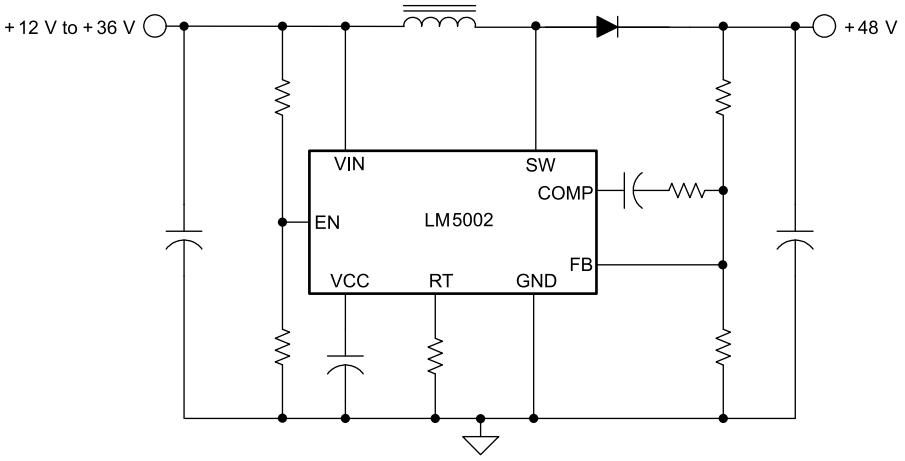
3 概要

LM5002 高耐圧スイッチ・モード・レギュレータは、外付け部品をほとんど使用せずに効率的な高耐圧昇圧、フライバック、SEPIC、およびフォワード・コンバータを実装するため必要なすべての機能を備えています。この使いやすいレギュレータは、ピーク電流制限 0.5A、耐圧 75V の N チャネル MOSFET を内蔵しています。電流モード制御が本質的に備える特性によって、ループ補償と入力電圧フィードフォワードが容易で、入力過渡除去性能が優れています。スイッチング周波数は単一の抵抗によって、最高 1.5MHz までの範囲で設定可能です。オシレータは、外部クロックと同期させることもできます。そのほかの保護機能として、電流制限、サーマル・シャットダウン、低電圧誤動作防止、リモート・シャットダウン機能が搭載されています。このデバイスは、8 ピン SOIC と 8 ピン WSON のパッケージで供給されます。カスタムのレギュレータ設計を作成するには、LM5002 を WEBENCH® Power Designer とともに使用します。

製品情報

部品番号	パッケージ(1)	本体サイズ (公称)
LM5002	SOIC (8)	4.90mm × 3.90mm
	WSON (8)	4.00mm × 4.00mm

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。



代表的なアプリケーション回路

英語版の TI 製品についての情報を翻訳したこの資料は、製品の概要を確認する目的で便宜的に提供しているものです。該当する正式な英語版の最新情報は、www.ti.com で閲覧でき、その内容が常に優先されます。TI では翻訳の正確性および妥当性につきましては一切保証いたしません。実際の設計などの前には、必ず最新版の英語版をご参照くださいますようお願いいたします。

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4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision E (December 2016) to Revision F (May 2021) — **Page**

- 文書全体にわたって表、図、相互参照の採番方法を更新.....1
- LM5005 を LM5002 に変更.....1

Changes from Revision D (March 2013) to Revision E (December 2016) — **Page**

- 「アプリケーション」セクション、「ESD 定格」表、「機能説明」セクション、「デバイスの機能モード」、「アプリケーションと実装」セクション、「電源に関する推奨事項」セクション、「レイアウト」セクション、「デバイスおよびドキュメントのサポート」セクション、「メカニカル、パッケージ、および注文情報」セクションを追加.....1
- Changed Junction to Ambient, $R_{\theta JA}$, values in *Thermal Information* table From: 140 To: 105.7 (SOIC) and From: 40 To: 37.1 (WSON).....4
- Changed Junction to Case, θ_{JC}, values in *Thermal Information* table From: 32 To: 50.8 (SOIC) and From: 4.5 To: 25.8 (WSON).....4

Changes from Revision C (March 2013) to Revision D (March 2013) — **Page**

- ナショナル セミコンダクターのデータシートのレイアウトを TI 形式に変更.....1

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5 Pin Configuration and Functions

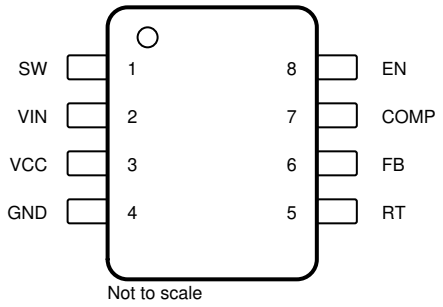


図 5-1. D Package 8-Pin SOIC Top View

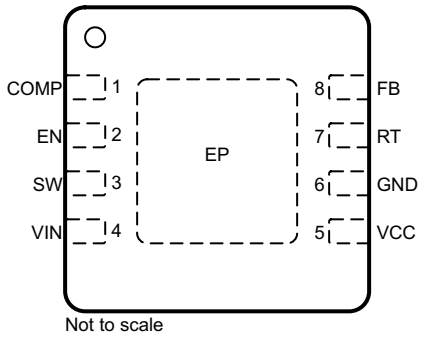


図 5-2. NGT Package 8-Pin WSON Top View

表 5-1. Pin Functions

PIN			TYPE(1)	DESCRIPTION
NAME	SOIC	WSON		
COMP	7	1	O	Open-drain output of the internal error amplifier: the loop compensation network must be connected between the COMP pin and the FB pin. COMP pullup is provided by an internal 5-kΩ resistor which can be used to bias an opto-coupler transistor (while FB is grounded) for isolated ground applications.
EN	8	2	I	Enable and undervoltage lockout or shutdown input: an external voltage divider can be used to set the line undervoltage lockout threshold. If the EN pin is left unconnected, a 6-µA pullup current source pulls the EN pin high to enable the regulator.
EP	—	EP	—	Exposed pad (WSON only): exposed metal pad on the underside of the package with a resistive connection to pin 6. It is recommended to connect this pad to the PCB ground plane to improve heat dissipation.
FB	6	8	I	Feedback input from the regulated output voltage: this pin is connected to the inverting input of the internal error amplifier. The 1.26-V reference is internally connected to the non-inverting input of the error amplifier.
GND	4	6	G	Ground: internal reference for the regulator control functions and the power MOSFET current sense resistor connection.
RT	5	7	I	Oscillator frequency programming and optional synchronization pulse input: the internal oscillator is set with a resistor, between this pin and the GND pin. The recommended frequency range is 50 KHz to 1.5 MHz. The RT pin can accept synchronization pulses from an external clock. A 100-pF capacitor is recommended for coupling the synchronizing clock to the RT pin.
SW	1	3	I	Switch pin: the drain terminal of the internal power MOSFET
VIN	2	4	P	Input supply pin: nominal operating range is 3.1 V to 75 V.
VCC	3	5	P	Bias regulator output, or input for external bias supply: VCC tracks VIN up to 6.9 V. Above VIN = 6.9 V, VCC is regulated to 6.9 V. A 0.47-µF or greater ceramic decoupling capacitor is required. An external voltage (7 V to 12 V) can be applied to this pin which disables the internal VCC regulator to reduce internal power dissipation and improve converter efficiency.

(1) G = Ground, I = Input, O = Output, P = Power

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

	MIN	MAX	UNIT
VIN to GND		76	V
SW to GND (steady state)	–0.3	76	V
VCC, EN to GND		14	V
COMP, FB, RT to GND	–0.3	7	V
Maximum junction temperature, T_{J-MAX}		150	°C
Storage temperature, T_{stg}	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±750	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	MAX	UNIT
VIN	3.1	75	V
Operating junction temperature	–40	125	°C

6.4 Thermal Information

THERMAL METRIC(1)		LM5002		UNIT
		D (SOIC)	NGT (WSON)	
		8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	105.7	37.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	50.8	25.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	46.1	14.2	°C/W
ψ_{JT}	Junction-to-top characterization parameter	8.2	0.2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	45.6	14.4	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	—	3.8	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

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6.5 Electrical Characteristics

Typical values at T_J = 25°C, minimum and maximum values at T_J = –40°C to 125°C, V_{VIN} = 10 V, and R_{RT} = 48.7 kΩ (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
STARTUP REGULATOR						
$V_{VCC-REG}$	VCC regulator output		6.55	6.85	7.15	V
	VCC current limit	V_{VCC} = 6 V	15	20		mA
	VCC UVLO threshold	V_{VCC} increasing	2.6	2.8	3	V
	VCC undervoltage hysteresis			0.1		V
I_{IN}	Bias current	V_{FB} = 1.5 V		3.1	4.5	mA
I_Q	Shutdown current (I_{IN})	V_{EN} = 0 V		95	130	µA
EN THRESHOLDS						
	EN shutdown threshold	V_{EN} increasing	0.25	0.45	0.65	V
	EN shutdown hysteresis			0.1		V
	EN standby threshold	V_{EN} increasing	1.2	1.26	1.32	V
	EN standby hysteresis			0.1		V
	EN current source			6		µA
MOSFET CHARACTERISTICS						
	MOSFET $R_{DS(ON)}$ plus current sense resistance	I_D = 0.25 A		850	1600	mΩ
	MOSFET leakage current	V_{SW} = 75 V		0.05	5	µA
	MOSFET gate charge	V_{VCC} = 6.9 V		2.4		nC
CURRENT LIMIT						
I_{LIM}	Cycle by cycle current limit		0.4	0.5	0.6	A
	Cycle by cycle current limit delay			100	200	ns
OSCILLATOR						
F_{SW1}	Frequency1	R_{RT} = 48.7 kΩ	225	260	295	KHz
F_{SW2}	Frequency2	R_{RT} = 15.8 kΩ	660	780	900	KHz
$V_{RT-SYNC}$	SYNC threshold		2.2	2.6	3.2	V
	SYNC pulse width minimum	V_{RT} > $V_{RT-SYNC}$ + 0.5 V		15		ns
PWM COMPARATOR						
	Maximum duty cycle		80%	85%	90%	
	Minimum ON-time	V_{COMP} > $V_{COMP-OS}$		25		ns
	Minimum ON-time	V_{COMP} < $V_{COMP-OS}$		0		ns
$V_{COMP-OS}$	COMP to PWM comparator offset		0.9	1.3	1.55	V
ERROR AMPLIFIER						
V_{FB-REF}	Feedback reference voltage	Internal reference and V_{FB} = V_{COMP}	1.241	1.26	1.279	V
	FB bias current			10		nA
	DC gain			72		dB
	COMP sink current	V_{COMP} = 250 mV	2.5			mA
	COMP short circuit current	V_{FB} = 0 V and V_{COMP} = 0 V	0.9	1.2	1.5	mA
	COMP open circuit voltage	V_{FB} = 0 V	4.8	5.5	6.2	V
	COMP to SW delay			42		ns
	Unity gain bandwidth			3		MHz
THERMAL SHUTDOWN						
T_{SD}	Thermal shutdown threshold			165		°C

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Typical values at T_J = 25°C, minimum and maximum values at T_J = –40°C to 125°C, V_{VIN} = 10 V, and R_{RT} = 48.7 kΩ (unless otherwise noted)(1)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Thermal shutdown hysteresis			20		°C

(1) Min and Max limits are 100% production tested at 25°C. Limits over the operating temperature range are ensured through correlation using Statistical Quality Control (SQC) methods. Limits are used to calculate TI's Average Outgoing Quality Level (AOQL).

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6.6 Typical Characteristics

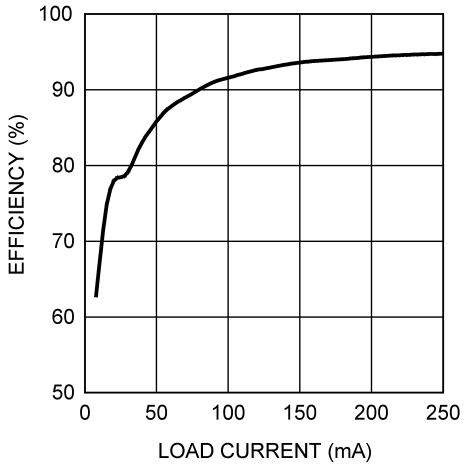


図 6-1. Efficiency, Boost Converter

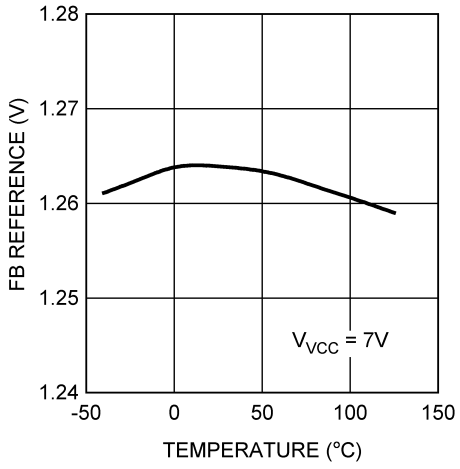


図 6-2. V_{FB} vs Temperature

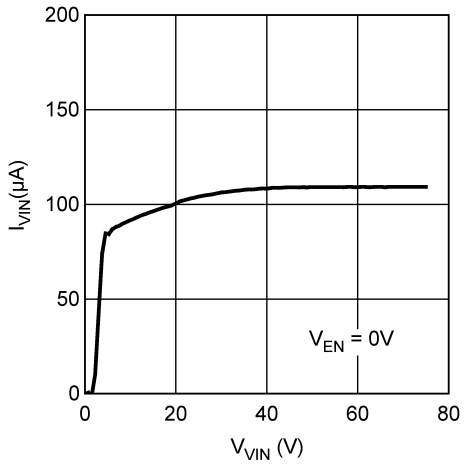


図 6-3. I_Q (Non-Switching) vs V_{IN}

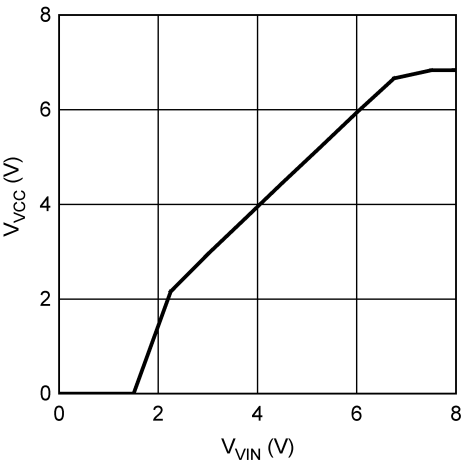


図 6-4. V_{CC} vs V_{IN}

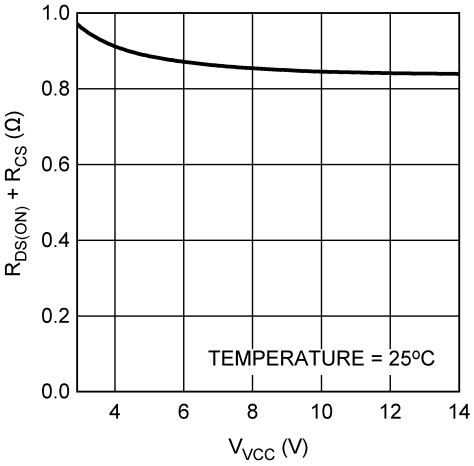


図 6-5. $R_{DS(ON)}$ vs V_{CC}

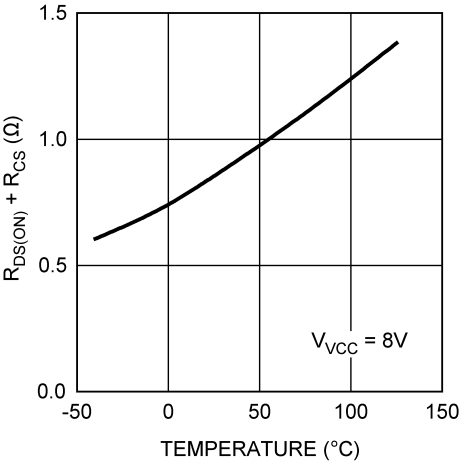


図 6-6. $R_{DS(ON)}$ vs Temperature

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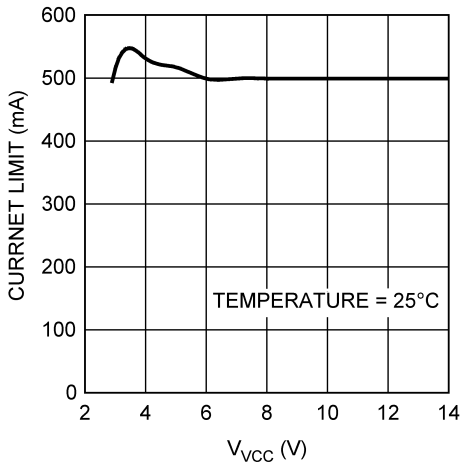


図 6-7. I_{LIM} vs V_{CC}

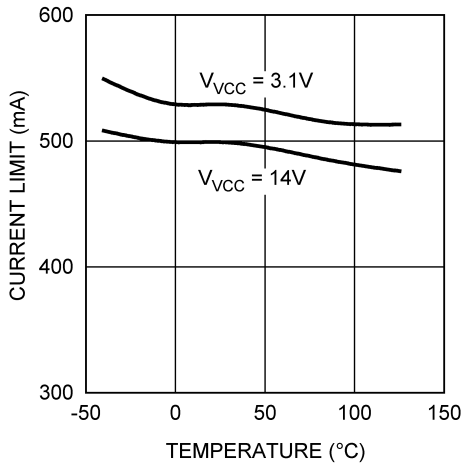


図 6-8. I_{LIM} vs V_{CC} vs Temperature

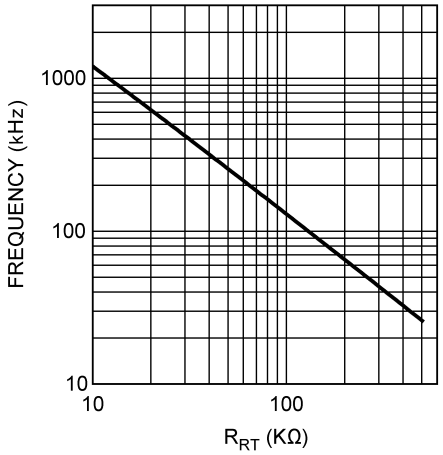


図 6-9. F_{SW} vs R_{RT}

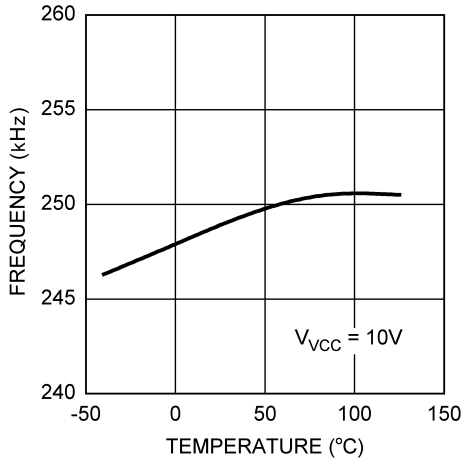


図 6-10. F_{SW} vs Temperature

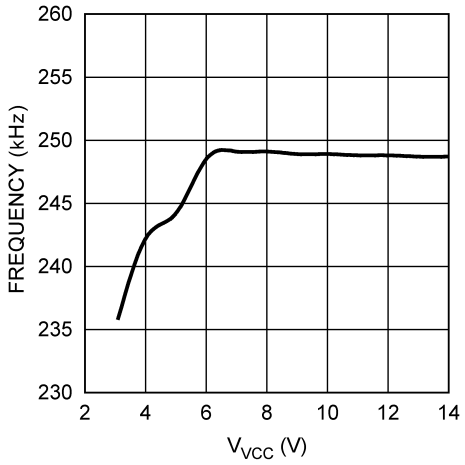


図 6-11. F_{SW} vs V_{CC}

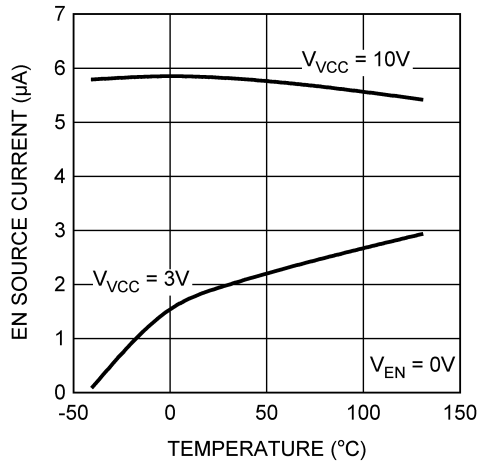


図 6-12. I_{EN} vs V_{VIN} vs Temperature

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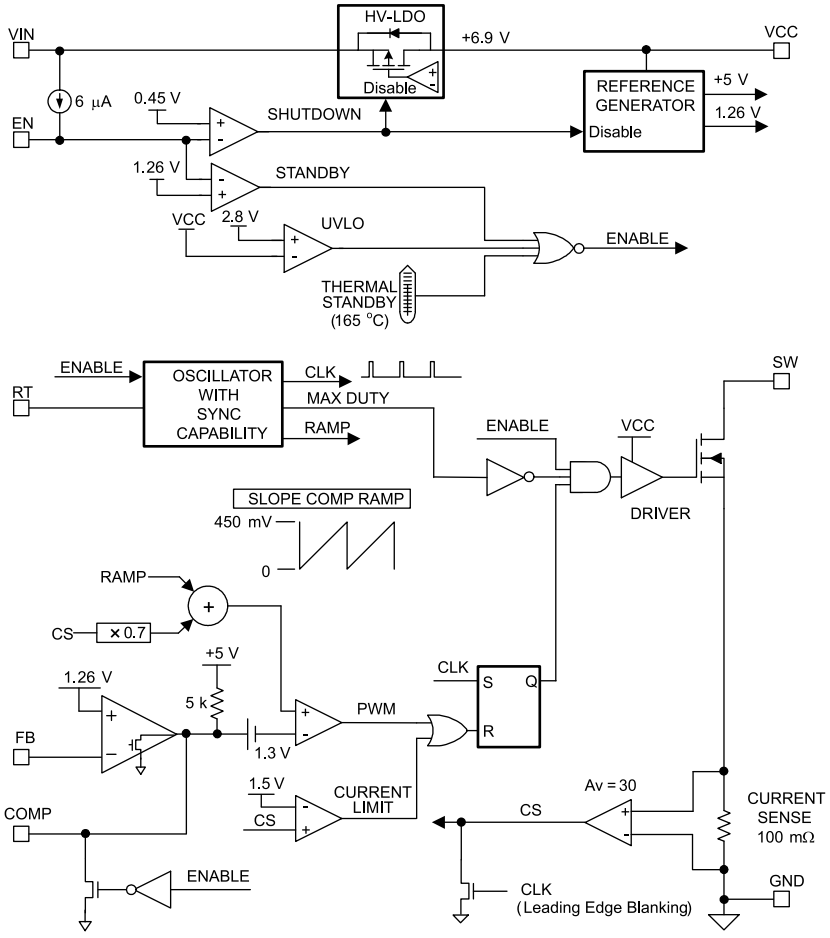
7 Detailed Description

7.1 Overview

The LM5002 high-voltage switching regulator features all the functions necessary to implement an efficient boost, flyback, SEPIC or forward current-mode power converter. The operation can be best understood by referring to the block diagram. At the start of each cycle, the oscillator sets the driver logic and turns on the power MOSFET to conduct current through the inductor or transformer. The peak current in the MOSFET is controlled by the voltage at the COMP pin. The COMP voltage increases with larger loads and decrease with smaller loads. This voltage is compared with the sum of a voltage proportional to the power MOSFET current and an internally generated slope compensation ramp. Slope compensation is used in current mode PWM architectures to eliminate subharmonic current oscillation that occurs with static duty cycles greater than 50%. When the summed signal exceeds the COMP voltage, the PWM comparator resets the driver logic, turning off the power MOSFET. The driver logic is then set by the oscillator at the end of the switching cycle to initiate the next power period.

The LM5002 has dedicated protection circuitry to protect the IC from abnormal operating conditions. Cycle-by-cycle current limiting prevents the power MOSFET current from exceeding 0.5A. This feature can also be used to soft start the regulator. Thermal shutdown circuitry holds the driver logic in reset when the die temperature reaches 165°C, and returns to normal operation when the die temperature drops by approximately 20°C. The EN pin can be used as an input voltage undervoltage lockout (UVLO) during start-up to prevent operation with less than the minimum desired input voltage.

7.2 Functional Block Diagram



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7.3 Feature Description

7.3.1 High Voltage VCC Regulator

The LM5002 VCC low dropout (LDO) regulator allows the LM5002 to operate at the lowest possible input voltage. The VCC pin voltage is very nearly equal to the input voltage from 2.8 V up to approximately 6.9 V. As the input voltage continues to increase, the VCC voltage is regulated at the 6.9 V set-point. The total input operating range of the VCC LDO regulator is 3.1 V to 75 V.

The output of the VCC regulator is current limited to 20 mA. During power-up, the VCC regulator supplies current into the required decoupling capacitor (0.47 µF or greater ceramic capacitor) at the VCC pin. When the VCC voltage exceeds the VCC UVLO threshold of 2.8 V and the EN pin is greater than 1.26 V the PWM controller is enabled and switching begins. The controller remains enabled until VCC falls below 2.7 V or the EN pin falls below 1.16 V.

An auxiliary supply voltage can be applied to the VCC pin to reduce the IC power dissipation. If the auxiliary voltage is greater than 6.9 V, the internal regulator essentially shuts-off, and internal power dissipation is decreased by the VIN voltage times the operating current. The overall converter efficiency also improves if the VIN voltage is much higher than the auxiliary voltage. Do not exceed 14 V with an externally applied VCC voltage. The VCC regulator series pass MOSFET includes a body diode (see *セクション 7.2*) between VCC and VIN that must not be forward biased in normal operation. Therefore, the auxiliary VCC voltage must never exceed the VIN voltage.

In high voltage applications take extra care to ensure the VIN pin does not exceed the absolute maximum voltage rating of 76 V. Voltage ringing on the VIN line during line transients that exceeds the Absolute Maximum Ratings can damage the IC. Both careful PCB layout and the use of quality bypass capacitors placed close to the VIN and GND pins are essential.

7.3.2 Oscillator

A single external resistor connected between RT and GND pins sets the LM5002 oscillator frequency. To set a desired oscillator frequency (F_{SW}), the necessary value for the RT resistor can be calculated with 式 1.

$$RT = 13.1 \times 10^{9} \times \left(\frac{1}{F_{SW}} - 83\ ns \right) \tag{1}$$

The tolerance of the external resistor and the frequency tolerance indicated in the *セクション 6.5* must be taken into account when determining the worst case frequency range.

7.3.3 External Synchronization

The LM5002 can be synchronized to the rising edge of an external clock. The external clock must have a higher frequency than the free running oscillator frequency set by the RT resistor. The clock signal must be coupled through a 100-pF capacitor into the RT pin. A peak voltage level greater than 2.6 V at the RT pin is required for detection of the sync pulse. The DC voltage across the RT resistor is internally regulated at 1.5 V. The negative portion of the AC voltage of the synchronizing clock is clamped to this 1.5 V by an amplifier inside the LM5002 with approximately 100-Ω output impedance. Therefore, the AC pulse superimposed on the RT resistor must have positive pulse amplitude of 1.1 V or greater to successfully synchronize the oscillator. The sync pulse width measured at the RT pin must have a duration greater than 15 ns and less than 5% of the switching period. The sync pulse rising edge initiates the internal CLK signal rising edge, which turns off the power MOSFET. The RT resistor is always required, whether the oscillator is free running or externally synchronized. Place the RT resistor very close to the device and connected directly to the RT and GND pins of the LM5002.

7.3.4 Enable and Standby

The LM5002 contains a dual level Enable circuit. When the EN pin voltage is below 450 mV, the IC is in a low current shutdown mode with the VCC LDO disabled. When the EN pin voltage is raised above the shutdown threshold but below the 1.26-V standby threshold, the VCC LDO regulator is enabled, while the remainder of the IC is disabled. When the EN pin voltage is raised above the 1.26-V standby threshold, all functions are enabled

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and normal operation begins. An internal 6-µA current source pulls up the EN pin to activate the IC when the EN pin is left disconnected.

7.3.5 Error Amplifier and PWM Comparator

An internal high-gain error amplifier generates an error signal proportional to the difference between the regulated output voltage and an internal precision reference. The output of the error amplifier is connected to the COMP pin allowing the user to add loop compensation, typically a Type-II network, as illustrated in 図 7-1. This network creates a low-frequency pole that rolls off the high DC gain of the amplifier, which is necessary to accurately regulate the output voltage. F_{DC_POLE} is the closed-loop unity gain (0 dB) frequency of this pole. A zero provides phase boost near the closed-loop unity gain frequency, and a high-frequency pole attenuates switching noise. The PWM comparator compares the current sense signal from the current sense amplifier to the error amplifier output voltage at the COMP pin.

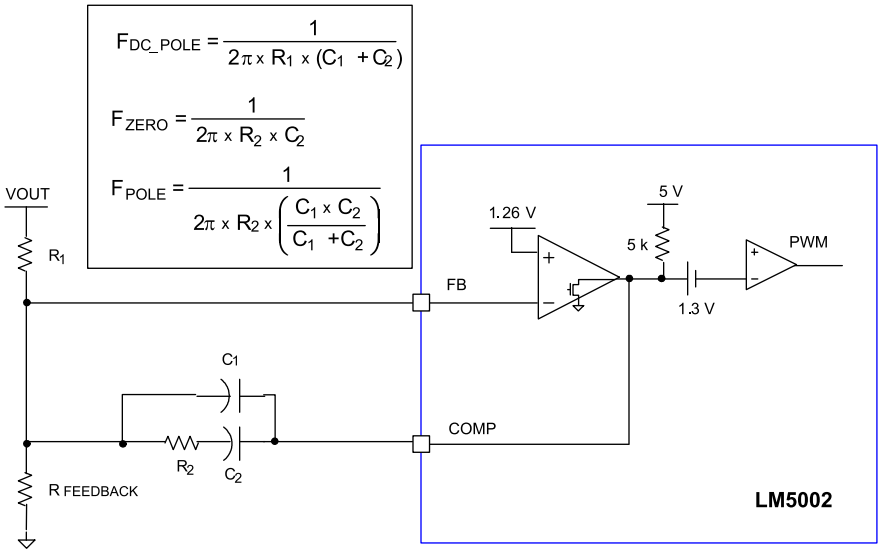


図 7-1. Type II Compensator

When isolation between primary and secondary circuits is required, the Error Amplifier is usually disabled by connecting the FB pin to GND. This allows the COMP pin to be driven directly by the collector of an opto-coupler. In isolated designs the external error amplifier is placed on the secondary circuit and drives the opto-coupler LED. The compensation network is connected to the secondary side error amplifier. An example of an isolated regulator with an opto-coupler is shown in 図 8-6.

7.3.6 Current Amplifier and Slope Compensation

The LM5002 employs peak current-mode control that also provides a cycle-by-cycle overcurrent protection feature. An internal 100-mΩ current sense resistor measures the current in the power MOSFET source. The sense resistor voltage is amplified 30 times to provide a 3 V/A signal into the current limit comparator. Current limiting is initiated if the internal current limit comparator input exceeds the 1.5-V threshold, corresponding to 0.5 A. When the current limit comparator is triggered, the SW output pin immediately switches to a high impedance state.

The current sense signal is reduced to a scale factor of 2.1 V/A for the PWM comparator signal. The signal is then summed with a 450-mV peak slope compensation ramp. The combined signal provides the PWM comparator with a control signal that reaches 1.5 V when the MOSFET current is 0.5 A. For duty cycles greater than 50%, current mode control circuits are subject to subharmonic oscillation (alternating between short and long PWM pulses every other cycle). Adding a fixed slope voltage ramp signal (slope compensation) to the current sense signal prevents this oscillation. The 450-mV ramp (zero volts when the power MOSFET turns on, and 450 mV at the end of the PWM clock cycle) adds a fixed slope to the current sense ramp to prevent oscillation.

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To prevent erratic operation at low duty cycle, a leading edge blanking circuit attenuates the current sense signal when the power MOSFET is turned on. When the MOSFET is initially turned on, current spikes from the power MOSFET drain-source and gate-source capacitances flow through the current sense resistor. These transient currents normally cease within 50 ns with proper selection of rectifier diodes and proper PCB layout.

7.3.7 Power MOSFET

The LM5002 switching regulator includes an N-Channel MOSFET with 850-mΩ ON-resistance. The ON-resistance of the LM5002 MOSFET varies with temperature as shown in セクション 6.6. The typical total gate charge for the MOSFET is 2.4 nC which is supplied from the VCC pin when the MOSFET is turned on.

7.4 Device Functional Modes

7.4.1 Thermal Protection

Internal thermal shutdown circuitry is provided to protect the IC in the event the maximum junction temperature is exceeded. When the 165°C junction temperature threshold is reached, the regulator is forced into a low power standby state, disabling all functions except the VCC regulator. Thermal hysteresis allows the IC to cool down before it is re-enabled. Note that because the VCC regulator remains functional during this period, the soft-start circuit shown in 図 8-4 must be augmented if soft start from thermal shutdown state is required.

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8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The following information is intended to provide guidelines for the power supply designer using the LM5002.

8.1.1 VIN

The voltage applied to the VIN pin can vary within the range of 3.1 V to 75 V. The current into the VIN pin depends primarily on the gate charge of the power MOSFET, the switching frequency, and any external load on the VCC pin. It is recommended to use the filter shown in 図 8-1 to suppress transients that may occur at the input supply. This is particularly important when VIN is operated close to the maximum operating rating of the LM5002.

When power is applied and the VIN voltage exceeds 2.8 V with the EN pin voltage greater than 0.45 V, the VCC regulator is enabled, supplying current into the external capacitor connected to the VCC pin. When the VIN voltage is between 2.8 V and 6.9 V, the VCC voltage is approximately equal to the VIN voltage. When the voltage on the VCC pin exceeds 6.9 V, the VCC pin voltage is regulated at 6.9 V. In typical flyback applications, an auxiliary transformer winding is connected through a diode to the VCC pin. This winding must raise the VCC voltage above 6.9 V to shut off the internal start-up regulator. The current requirements from this winding are relatively small, typically less than 20 mA. If the VIN voltage is much higher than the auxiliary voltage, the auxiliary winding significantly improves the conversion efficiency. It also reduces the power dissipation within the LM5002. The externally applied VCC voltage must never exceed 14 V. Also the applied VCC must never exceed the VIN voltage to avoid reverse current through the internal VCC to VIN diode shown in the LM5002 *セクション 7.2*.

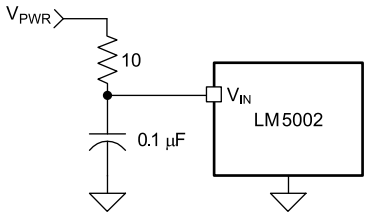


図 8-1. Input Transient Protection

8.1.2 SW PIN

Attention must be given to the PCB layout for the SW pin that connects to the power MOSFET drain. Energy can be stored in parasitic inductance and capacitance that causes switching spikes that negatively affect efficiency, and conducted and radiated emissions. These connections must be as short as possible to reduce inductance and as wide as possible to reduce resistance. The loop area, defined by the SW and GND pin connections, the transformer or inductor terminals, and their respective return paths, must be minimized.

8.1.3 EN or UVLO Voltage Divider Selection

An external setpoint resistor divider from VIN to GND can be used to determine the minimum operating input range of the regulator. The divider must be designed such that the EN pin exceeds the 1.26-V standby threshold when VIN is in the desired operating range. The internal 6-µA current source must be included when determining the resistor values. The shutdown and standby thresholds have 100-mV hysteresis to prevent noise from toggling between modes. When the VIN voltage is below 3.5 VDC during start-up and the operating temperature is below –20°C, the EN pin must have a pullup resistor that provides 2 µA or greater current. The EN pin is

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internally protected by a 6-V Zener diode through a 1-kΩ resistor. The enabling voltage may exceed the Zener voltage, however the Zener current must be limited to less than 4 mA.

Two dedicated comparators connected to the EN pin are used to detect undervoltage and shutdown conditions. When the EN pin voltage is below 0.45 V, the controller is in a low-current shutdown mode where the VIN current is reduced to 95 µA. For an EN pin voltage greater than 0.45 V but less than 1.26 V, the controller is in standby mode, with all internal circuits operational, but the PWM gate driver signal is blocked. Once the EN pin voltage is greater than 1.26 V, the controller is fully enabled. Two external resistors can be used to program the minimum operational voltage for the power converter as shown in 図 8-2. When the EN pin voltage falls below the 1.26 V threshold, an internal 100 mV threshold hysteresis prevents noise from toggling the state, so the voltage must be reduced to 1.16 V to transition to standby. Resistance values for R1 and R2 can be determined from 式 2 and 式 3.

$$R1 = \frac{V_{PWR} - 1.26V}{I_{DIVIDER}} \quad (2)$$

$$R2 = \frac{1.26V}{I_{DIVIDER} + 6\ \mu A} \quad (3)$$

where:

- V_{PWR} is the desired turnon voltage
- $I_{DIVIDER}$ is an arbitrary current through R1 and R2

For example, if the LM5002 is to be enabled when V_{PWR} reaches 16 V, $I_{DIVIDER}$ could be chosen as 501 µA that sets R1 to 29.4 kΩ and R2 to 2.49 kΩ. The voltage at the EN pin must not exceed 10 V unless the current into the 6 V protection Zener diode is limited below 4 mA. The EN pin voltage must not exceed 14 V at any time. Be sure to check both the power and voltage rating (some 0603 resistors are rated as low as 50 V) for the selected R1 resistor.

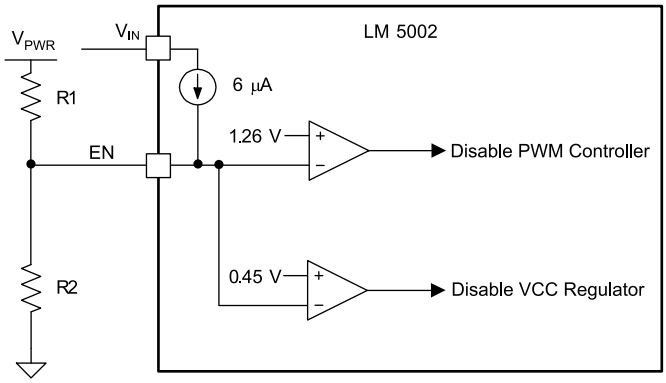


図 8-2. Basic EN (UVLO) Configuration

Remote configuration of the LM5002's operational modes can be accomplished with open drain device(s) connected to the EN pin as shown in 図 8-3. A MOSFET or an NPN transistor connected to the EN pin can force the regulator into the low power *off* state. Adding a PN diode in the drain (or collector) provides the offset to achieve the standby state. The advantage of standby is that the VCC LDO is not disabled and external circuitry powered by VCC remains functional.

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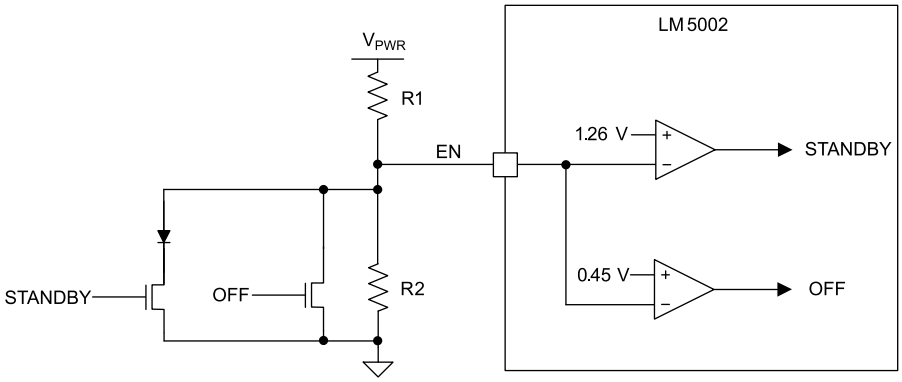


図 8-3. Remote Standby and Disable Control

8.1.4 Soft Start

Soft start (SS) can be implemented with an external capacitor connected to COMP through a diode as shown in 図 8-4. The COMP discharge MOSFET conducts during Shutdown and Standby modes to keep the COMP voltage below the PWM offset (1.3 V), which inhibits PWM pulses. The error amplifier attempts to raise the COMP voltage after the EN pin exceeds the 1.26 V standby threshold. Because the error amplifier output can only sink current, the internal COMP pullup resistor (approximately 5 kΩ) supplies the charging current to the SS capacitor. The SS capacitor causes the COMP voltage to gradually increase until the output voltage achieves regulation and FB assumes control of the COMP and the PWM duty cycle. The SS capacitor continues charging through a large resistance, R_{SS}, preventing the SS circuit from interfering with the normal error amplifier function. During shutdown, the VCC diode discharges the SS capacitor.

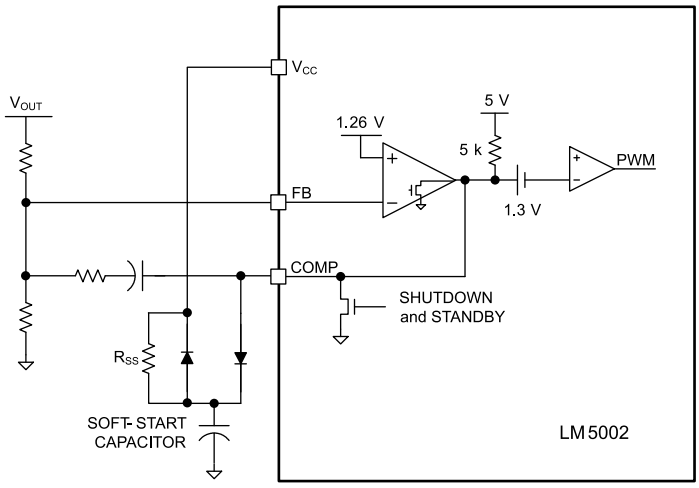


図 8-4. Soft-Start Circuit

8.2 Typical Applications

図 8-5, 図 8-6, 図 8-7, and 図 8-8 present examples of a non-isolated flyback, isolated flyback, boost, 24-V SEPIC, and a 12-V automotive range SEPIC converters utilizing the LM5002 switching regulator.

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8.2.1 Non-Isolated Flyback Regulator

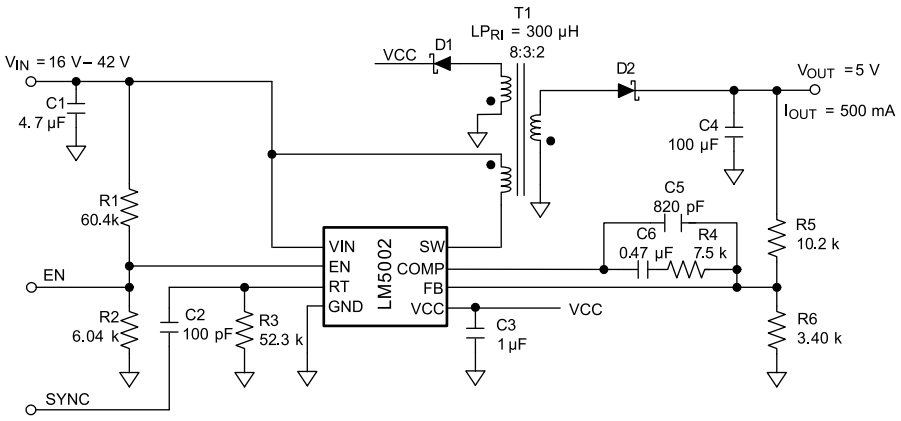


図 8-5. Non-Isolated Flyback Schematic

8.2.1.1 Design Requirements

The non-isolated flyback converter shown in 図 8-5 uses the internal voltage reference for the regulation setpoint. The output is 5 V at 500 mA while the input voltage can vary from 16 V to 42 V. The switching frequency is set to 250 kHz. An auxiliary winding on transformer (T1) provides 7.5 V to power the LM5002 when the output is in regulation. This disables the internal high-voltage VCC LDO regulator and improves efficiency. The input undervoltage threshold is 13.9 V. The converter can be shut down by driving the EN input below 1.26 V with an open-collector or open-drain transistor. An external synchronizing frequency can be applied to the SYNC input. An optional soft-start circuit is connected to the COMP pin input. When power is applied, the soft-start capacitor (C7) is discharged and limits the voltage applied to the PWM comparator by the internal error amplifier. The internal approximate 5-kΩ COMP pullup resistor charges the soft-start capacitor until regulation is achieved. The VCC pullup resistor (R7) continues to charge C7 so that the soft-start circuit does not affect the compensation network in normal operation. If the output capacitance is small, the soft-start circuit can be adjusted to limit the power-on output voltage overshoot. If the output capacitance is sufficiently large, no soft-start circuit is required because the LM5002 gradually charges the output capacitor by current limiting at approximately 500 mA (I_{LIM}) until regulation is achieved.

8.2.1.2 Detailed Design Procedure

8.2.1.2.1 Switching Frequency

The R_T (R3) can be found using 式 1. For 250-kHz operation, a value of 51.3 kΩ was calculated. A 52.3-kΩ resistor is selected as the closest available value.

8.2.1.2.2 Flyback Transformer

Two things require consideration when specifying a flyback transformer. First, the turns ratio to determine the duty cyle D (MOSFET on-time compared to the switching period). Second, the primary inductance (L_{PRI}) to determine the current sense ramp for current-mode control.

To start, the primary inductance in continous current mode (CCM) is designed to provide a ramp during the MOSFET on-time of around 30% of the full load MOSFET current. This produces a good signal-to-noise ratio for current mode control.

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The transfer function of a flyback power stage is 式 4.

$$\frac{V_{OUT}}{V_{IN}} = \frac{D}{1-D} x \frac{N_{SEC}}{N_{PRI}} \tag{4}$$

where:

- V_{IN} is the input voltage
- V_{OUT} is the secondary output voltage
- D is the duty cycle of the MOSFET for one switching cycle
- N_{PRI} is the number of turns on the primary winding of the transformer
- N_{SEC} is the number of turns on the secondary winding of the transformer

The duty cycle can be derived as shown in 式 5.

$$D = \frac{V_{OUT}}{V_{OUT} + \frac{V_{IN} \times N_{SEC}}{N_{PRI}}} \tag{5}$$

And the approximate turns ratio is given by 式 6.

$$\frac{N_{SEC}}{N_{PRI}} = \frac{V_{OUT} \times (1-D)}{V_{IN} \times D} \tag{6}$$

The primary inducance (L_{PRI}) is calculated using 式 7.

$$L_{PRI} = \frac{V_{IN} \times D \times \frac{1}{f_{sw}}}{RR \times I_{OUT(MAX)} \times \frac{N_{SEC}}{N_{PRI}}} \tag{7}$$

where:

- L_{PRI} is the transformer inductance referenced to the primary side
- RR is the ripple ratio of the reflected secondary output current (ypically between 30% and 40%)

The auxillary winding turns ratio can be found with 式 8.

$$N_{AUX} = N_{SEC} \times \frac{V_{AUX}}{V_{OUT}} \tag{8}$$

where:

- N_{AUX} is the number of turns on the auxiliary winding of the transformer
- V_{AUX} is the desired VCC voltage

The CCM duty cycle can be designed for 50% with minimum input voltage. Using 式 6, the turns ratio of the secondary winding to the primay winding can be found to be 0.313. Rounding to a whole number of turns results in a turns ratio of 0.375. The auxillary winding of the transformer can be used to supply the VCC voltage to the LM5002, resulting in better total efficiency by disabling the internal high voltage VCC regulator. To disable the VCC regulator the exteranlly supplied voltage must be greater than 7 V, thus a target voltage of 8 V is selected. The number of turns on the auxillary winding can be found with 式 8, resulting in a turns ratio of the auxillary winding to the secondary winding of 0.6.

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The primary inductance can now be solved for using 式 7. Assuming that V_{IN} is at the minimum specified value and the ripple ratio (RR) is 35% the primary inductance is calculated to be 217 µH. Based on avaliable transformers a 300 µH primary inductance was selected.

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8.2.1.2.3 Peak MOSFET Current

The peak MOSFET current is determined with 式 9.

$$I_{PRI(PEAK)} = \frac{V_{IN} \times D \times \frac{1}{f_{sw}}}{2 \times L_{PRI}} + \frac{V_{OUT} \times I_{OUT}}{V_{IN} \times \eta \times D} \tag{9}$$

where:

- f_{sw} is the switching frequency
- η is the efficiency of the converter

The maximum peak MOSFET current occurs when V_{IN} is at its minimum specified voltage. 式 9 is used to calculate the peak MOSFET current. Assuming η is 90% the peak MOSFET current is calculated as 430 mA.

The internal power MOSFET must withstand the input voltage plus the output voltage multiplied by the turns ratio during the off-time. This is determined with 式 10.

$$V_{SW} = V_{IN} + \left(V_{OUT} \times \frac{N_{PRI}}{N_{SEC}} \right) \tag{10}$$

In addition, any leakage inductance of the transformer causes a turnoff voltage spike in addition to 式 10. This voltage spike is related to the MOSFET drain-to-source capacitance as well as other parasitic capacitances. To limit the spike magnitude, use a RCD termination or a Diode-Zener clamp.

8.2.1.2.4 Output Capacitance

The necessary output capacitance of the secondary side can be found using 式 11.

$$C_{OUT} = I_{OUT_MAX} \times \frac{D_{MAX}}{f_{SW} \times \Delta V_{OUT}} \tag{11}$$

where:

- D_{MAX} is the maximum duty cycle, which occurs at the minimum input voltage

Assuming that an output ripple of 15 mV is specified, states that a 60.60 µF output capacitance must be selected. Accounting for capacitance equivalent series resistance (ESR) ripple, a 100 µF capacitor is selected.

8.2.1.2.5 Output Diode Rating

The average diode current equals the output current under normal circumstances, but the diode must be designed to handle a continuous current limit condition for the worst case:

$$I_{D(WORST-CASE)} = I_{LIMIT(MOSFET)} \times \frac{N_{PRI}}{N_{SEC}} \tag{12}$$

where:

- $I_{LIMIT(MOSFET)}$ is the peak current limit of the interal MOSFET of the LM5002

The maximum reverse voltage applied to the diode occurs during the MOSFET on time in 式 13.

$$V_{D(REVERSE)} = V_{IN(MAX)} \times \frac{N_{SEC}}{N_{PRI}} \tag{13}$$

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The diode's reverse capacitance resonates with the transformer inductance (and other parasitic elements) to some degree and causing ringing that may affect conducted and ratiated emissions compliance. Usually an RC snubber network across the diode anode and cathode cam eliminate the ringing.

8.2.1.2.6 Power Stage Analysis

In any switch-mode topology that has the power MOSFET between the inductor and the output capacitor (boost, buck-boost, Flyback, SEPIC, and so on) a Right Half-Plane Zero (RHPZ) is produced by the power stage in the loop transfer function during Continuous Conduction Mode (CCM). If the topology is operated in Discontinuous Conduction Mode (DCM), the RHPZ does not exist. It is a function of the duty cycle, load and inductance, and causes an increase in loop gain while reducing the loop phase margin. A common practice is to determine the worst case RHPZ frequency and set the loop unity gain frequency below one-third of the RHPZ frequency

In the Flyback topology, the equation for the RHPZ is given by 式 14.

$$f_{RHPZ} = \frac{\frac{V_{OUT}}{I_{OUT}} \times (1-D)^2}{2\pi \times \left[\left(\frac{N_{SEC}}{N_{PRI}}\right)^2 \times L_{PRI}\right]} \tag{14}$$

The worst case RHPZ frequency is at the maximum load where I_{OUT} is the highest and at minimum input voltage where the duty cycle D is the highest. Assuming these conditions f_{RHPZ} is 24.6 kHz.

The LM5002 uses slope compensation to ensure stability when the duty cycle exceeds 45%. This has the affect of adding some Voltage Mode control to this current-mode IC. The effect on the power stage (Plant) transfer function is calculated in the following equations:

Inductor current slope during MOSFET ON time (式 15)

$$s_n = \frac{V_{IN}}{L_{PRI}} \tag{15}$$

Slope compensation ramp (式 16)

$$s_e = 450mV \times f_{SW} \tag{16}$$

Current-mode sampling gain (式 17)

$$f_{MOD} = V_{IN} \times \frac{N_{SEC}}{N_{PRI}} \times \frac{1}{\left(s_n + s_e\right) \times \frac{1}{f_{SW}}} \tag{17}$$

The control-to-output transfer function (G_{VC}) using low ESR ceramic capacitors is 式 18.

$$G_{VC}(f) = \frac{V_{OUT}}{I_{OUT}} \times \frac{1-D}{1+D} \times \frac{1 - j2\pi f \times \frac{D \times L_{SEC}}{(1-D)^2 \times \frac{V_{OUT}}{I_{OUT}}}}{1 + j2\pi f \times \frac{\frac{V_{OUT}}{I_{OUT}} \times C_{OUT}}{(1+D)^2}} \tag{18}$$

where:

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- L_{SEC} is the transformer inductance referenced to the secondary side and is equal to:

$$L_{SEC} = \left(\frac{N_{SEC}}{N_{PRI}}\right)^2 \times L_{PRI} \tag{19}$$

If high ESR capacitors (for example, aluminum electrolytic) are used for the output capacitance, an additional zero appears at frequency in 式 20, which increases the gain slope by +20 dB per decade of frequency and boosts the phase 45° at $F_{ZERO(ESR)}$ and 90° at 10 × $F_{ZERO(ESR)}$.

$$f_{ZERO(ESR)} = \frac{1}{2\pi \times ESR \times C_{OUT}} \tag{20}$$

where:

- ESR is the series resistance of the output capacitor
- C_{OUT} is the output capacitance

With these calculations, an approximate power stage Bode plot can be constructed with 式 21.

$$\left|G_{VC}(f)\right| = 20 \times \log\left(f_{MOD}\sqrt{\left[Re\left(G_{VC}(f)\right)\right]^2 + \left[Im\left(G_{VC}(f)\right)\right]^2}\right) \tag{21}$$

where:

- $[Re(G_{VC}(f))]$ is the real portion of
- $[Im(G_{VC}(f))]$ is the imaginary portion of

$$\theta_{G_{VC}}(f) = \frac{180}{\pi} \times \arctan\left(\frac{Im\left(G_{VC}(f)\right)}{Re\left(G_{VC}(f)\right)}\right) \tag{22}$$

Because these equations don't take into account the various parasitic resistances and reactances present in all power converters, there is some difference between the calculated Bode plot and the gain and phase of the actual circuit. It is therefore important to measure the converter using a network analyzer to quantify the implementation and adjust where appropriate.

8.2.1.2.7 Loop Compensation

The loop bandwidth and phase margin determines the response to load transients, while ensuring that the output noise level meets the requirements. A common choice of loop unity gain frequency is 5% of the switching frequency. This is simple to compensate, low noise and provides sufficient transient response for most applications. The plant bode plot is examined for gain and phase at the desired loop unity-gain frequency and the compensator is designed to adjust the loop gain and phase to meet the intended loop unity gain frequency and phase margin (typically about 55°). When gain is required, the ratio of R_{COMP} and R_{FB_TOP} sets the error amplifier to provide the correct amount.

$$A_{V(xo)} = \frac{R_{COMP}}{R_{FB_TOP}} \tag{23}$$

where (in reference to 図 8-5):

- R_{COMP} is R4
- R_{FB_TOP} is R5

The phase margin is boosted by a transfer function zero at frequency given by 式 23 and a pole at frequency given by 式 24.

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$$f_{ZERO} = \frac{1}{2\pi \times R_{COMP} \times C_{COMP}} \quad (24)$$

where (in reference to):

- C_{COMP} is C6

$$f_{POLE(HIGH)} = \frac{1}{2\pi \times R_{COMP} \times \left(\frac{C_{COMP} \times C_{HF}}{C_{COMP} + C_{HF}} \right)} \quad (25)$$

where (in reference to 図 8-5):

- C_{HF} is C5

The low frequency pole is determined with 式 26.

$$f_{POLE(LOW)} = \frac{1}{2\pi \times R_{FB_TOP} \times \left(C_{COMP} + C_{HF} \right)} \times \frac{1}{A_{VOL}} \quad (26)$$

where (in reference to 図 8-5):

- A_{VOL} is the open loop gain of the error amplifier

Optimal regulation is achieved by setting $F_{POLE(LOW)}$ as high as possible, but still permitting F_{ZERO} to insure the desired phase margin. The feedback resistors (R_{FB_TOP} and R_{FB_BOTTOM}) are chosen to be 10.2 kΩ and 3.4 kΩ respectively. These values produce a feedback signal that has a desirable signal to noise ratio. F_{ZERO} and $F_{POLE(HIGH)}$ are set to be 450 Hz and 25.5 kHz respectively. Based on these values, R_{COMP}, C_{COMP}, and C_{HF} are chosen to be 7.5 kΩ, 0.47 µF, and 820 pF respectively. These values produce a crossover frequency of approximately 3 kHz with a phase margin of 60°.

8.2.2 Isolated Flyback Regulator

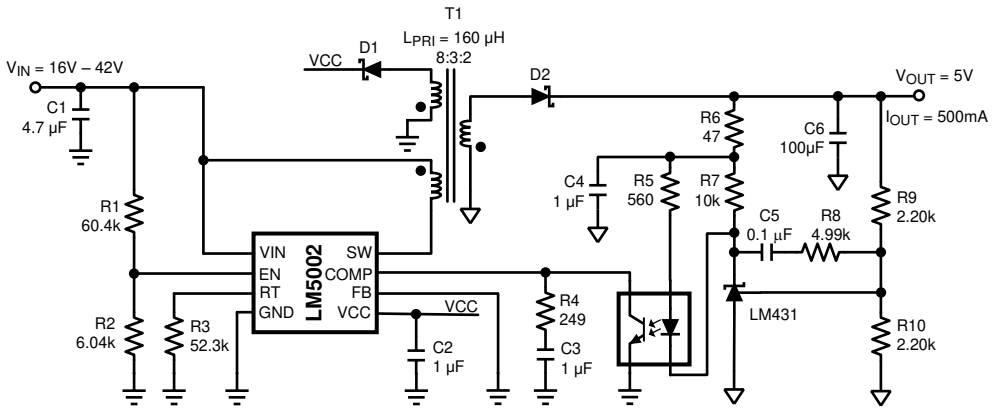


図 8-6. Isolated Flyback Schematic

8.2.2.1 Design Requirements

The isolated flyback converter shown in 図 8-6 uses a 2.5-V voltage reference (LM431) placed on the isolated secondary side for the regulation setpoint. The LM5002 internal error amplifier is disabled by grounding the FB pin. The LM431 controls the current through the opto-coupler LED, which sets the COMP pin voltage. The R4 and C3 network boosts the phase response of the opto-coupler to increase the loop bandwidth. The output is 5 V at 500 mA and the input voltage ranges from 16 V to 42 V. The switching frequency is set to 250 kHz.

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8.2.3 Boost Regulator

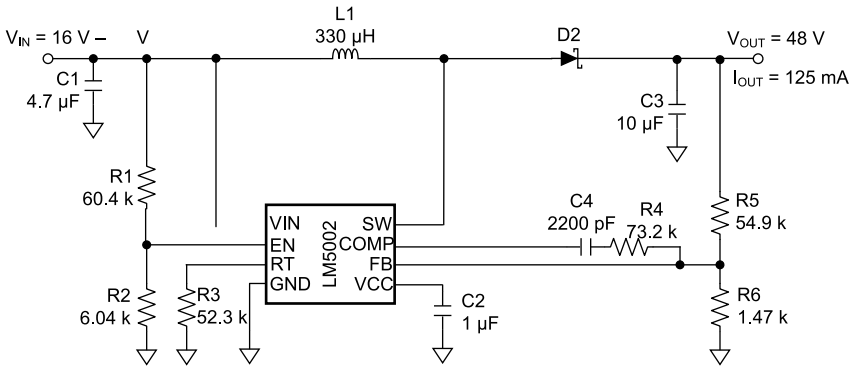


図 8-7. Boost Schematc

8.2.3.1 Design Requirements

The boost converter shown in 図 8-7 uses the internal voltage reference for the regulation setpoint. The output is 48 V at 125 mA, while the input voltage can vary from 16 V to 36 V. The switching frequency is set to 250 kHz. The internal VCC regulator provides 6.9-V bias power, because there is not a simple method for creating an auxiliary voltage with the boost topology. Note that the boost topology does not provide output short-circuit protection because the power MOSFET cannot interrupt the path between the input and the output.

8.2.4 24-V SEPIC Regulator

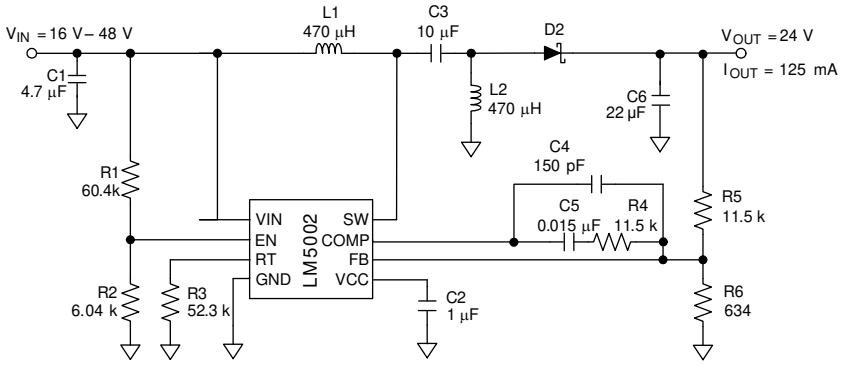


図 8-8. 24-V SEPIC Schematic

8.2.4.1 Design Requirements

The 24-V SEPIC converter shown in 図 8-8 uses the internal voltage reference for the regulation setpoint. The output is 24 V at 125 mA while the input voltage can vary from 16 V to 48 V. The switching frequency is set to 250 kHz. The internal VCC regulator provides 6.9-V bias power for the LM5002. An auxiliary voltage can be created by adding a winding on L2 and a diode into the VCC pin.

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8.2.5 12-V Automotive SEPIC Regulator

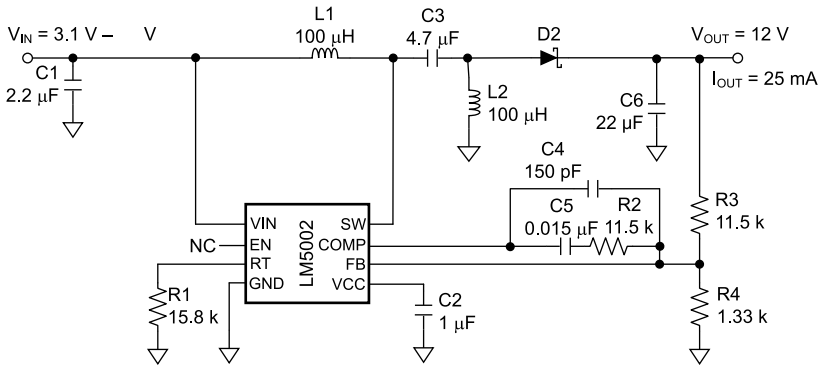


図 8-9. 12-V SEPIC Schematic

8.2.5.1 Design Requirements

The 12-V automotive SEPIC converter shown in 図 8-9 uses the internal bandgap voltage reference for the regulation setpoint. The output is 12 V at 25 mA while the input voltage can vary from 3.1 V to 60 V. The output current rating can be increased if the minimum VIN voltage requirement is increased. The switching frequency is set to 750 kHz. The internal VCC regulator provides 6.9-V bias power for the LM5002. The output voltage can be used as an auxiliary voltage if the nominal VIN voltage is greater than 12 V by adding a diode from the output into the VCC pin. In this configuration, the minimum input voltage must be greater than 12 V to prevent the internal VCC to VIN diode from conducting. If the applied VCC voltage exceeds the minimum VIN voltage, then an external blocking diode is required between the VIN pin and the power source to block current flow from VCC to the input supply.

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9 Power Supply Recommendations

The LM5002 is a power management device. The power supply for the device is any DC voltage source within the specified input voltage range (see *セクション 8.2.1.1*).

10 Layout

10.1 Layout Guidelines

The LM5002 current sense and PWM comparators are very fast and may respond to short duration noise pulses. The components at the SW, COMP, EN and the RT pins must be as physically close as possible to the IC, thereby minimizing noise pickup on the PCB tracks.

The SW pin of the LM5002 must have a short, wide conductor to the power path inductors, transformers and capacitors to minimize parasitic inductance that reduces efficiency and increases conducted and radiated noise. Ceramic decoupling capacitors are recommended between the VIN and GND pins and between the VCC and GND pins. Use short, direct connections to avoid clock jitter due to ground voltage differentials. Small package surface mount X7R or X5R capacitors are preferred for high-frequency performance and limited variation over temperature and applied voltage.

If an application using the LM5002 results high junction temperatures during normal operation, multiple vias from the GND pin to a PCB ground plane help conduct heat away from the IC. Judicious positioning of the PCB within the end product, along with use of any available air flow helps reduce the junction temperatures. If using forced air cooling, avoid placing the LM5002 in the air flow shadow of large components, such as input capacitors, inductors or transformers.

10.2 Layout Example

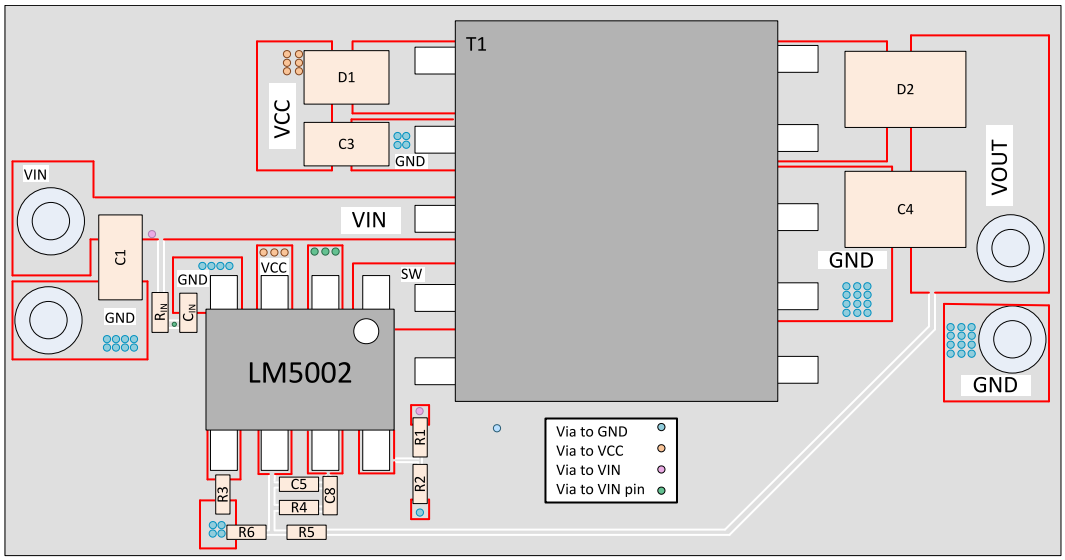


図 10-1. Layout Example for 図 8-5

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11 Device and Documentation Support

11.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.2 サポート・リソース

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11.3 Trademarks

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11.4 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.5 Glossary

TI Glossary — This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LM5002MA/NOPB	Active	Production	SOIC (D) | 8	95 | TUBE	Yes	SN	Level-1-260C-UNLIM	-40 to 125	L5002 MA
LM5002MA/NOPB.A	Active	Production	SOIC (D) | 8	95 | TUBE	Yes	SN	Level-1-260C-UNLIM	-40 to 125	L5002 MA
LM5002MA/NOPB.B	Active	Production	SOIC (D) | 8	95 | TUBE	Yes	SN	Level-1-260C-UNLIM	-40 to 125	L5002 MA
LM5002MAX/NOPB	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	L5002 MA
LM5002MAX/NOPB.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	L5002 MA
LM5002MAX/NOPB.B	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	L5002 MA
LM5002SD/NOPB	Active	Production	WSON (NGT) | 8	1000 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	LM5002
LM5002SD/NOPB.A	Active	Production	WSON (NGT) | 8	1000 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	LM5002
LM5002SD/NOPB.B	Active	Production	WSON (NGT) | 8	1000 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	LM5002
LM5002SDX/NOPB	Active	Production	WSON (NGT) | 8	4500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	LM5002
LM5002SDX/NOPB.A	Active	Production	WSON (NGT) | 8	4500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	LM5002
LM5002SDX/NOPB.B	Active	Production	WSON (NGT) | 8	4500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	LM5002

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

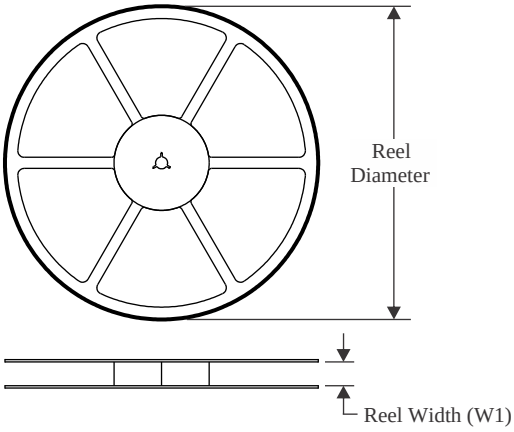
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

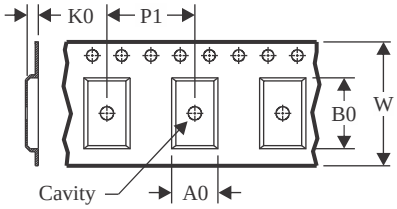
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

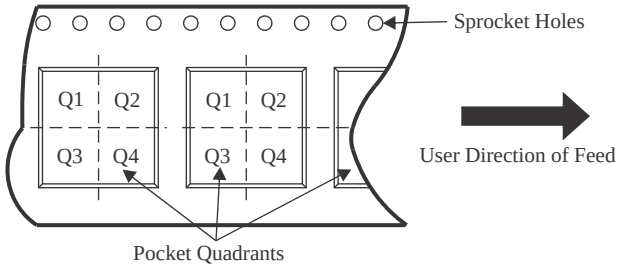


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

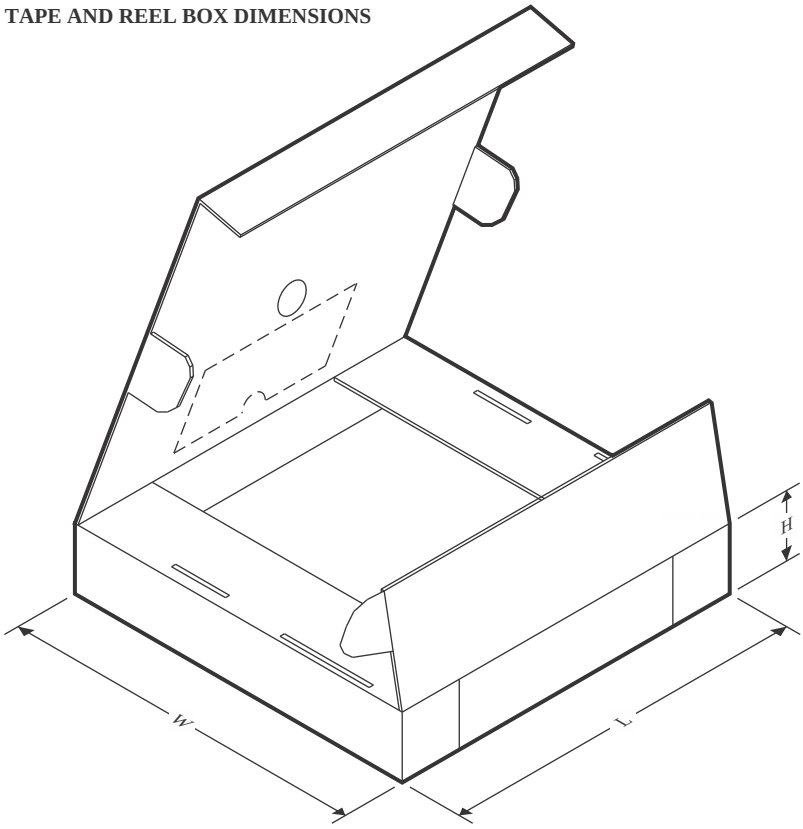
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM5002MAX/NOPB	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM5002SD/NOPB	WSON	NGT	8	1000	177.8	12.4	4.3	4.3	1.3	8.0	12.0	Q1
LM5002SDX/NOPB	WSON	NGT	8	4500	330.0	12.4	4.3	4.3	1.3	8.0	12.0	Q1

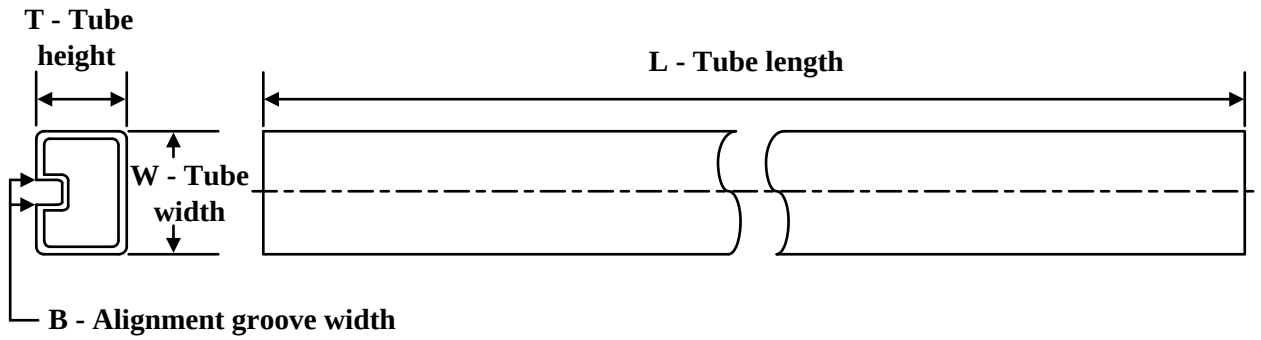
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM5002MAX/NOPB	SOIC	D	8	2500	367.0	367.0	35.0
LM5002SD/NOPB	WSON	NGT	8	1000	208.0	191.0	35.0
LM5002SDX/NOPB	WSON	NGT	8	4500	367.0	367.0	35.0

TUBE



*All dimensions are nominal

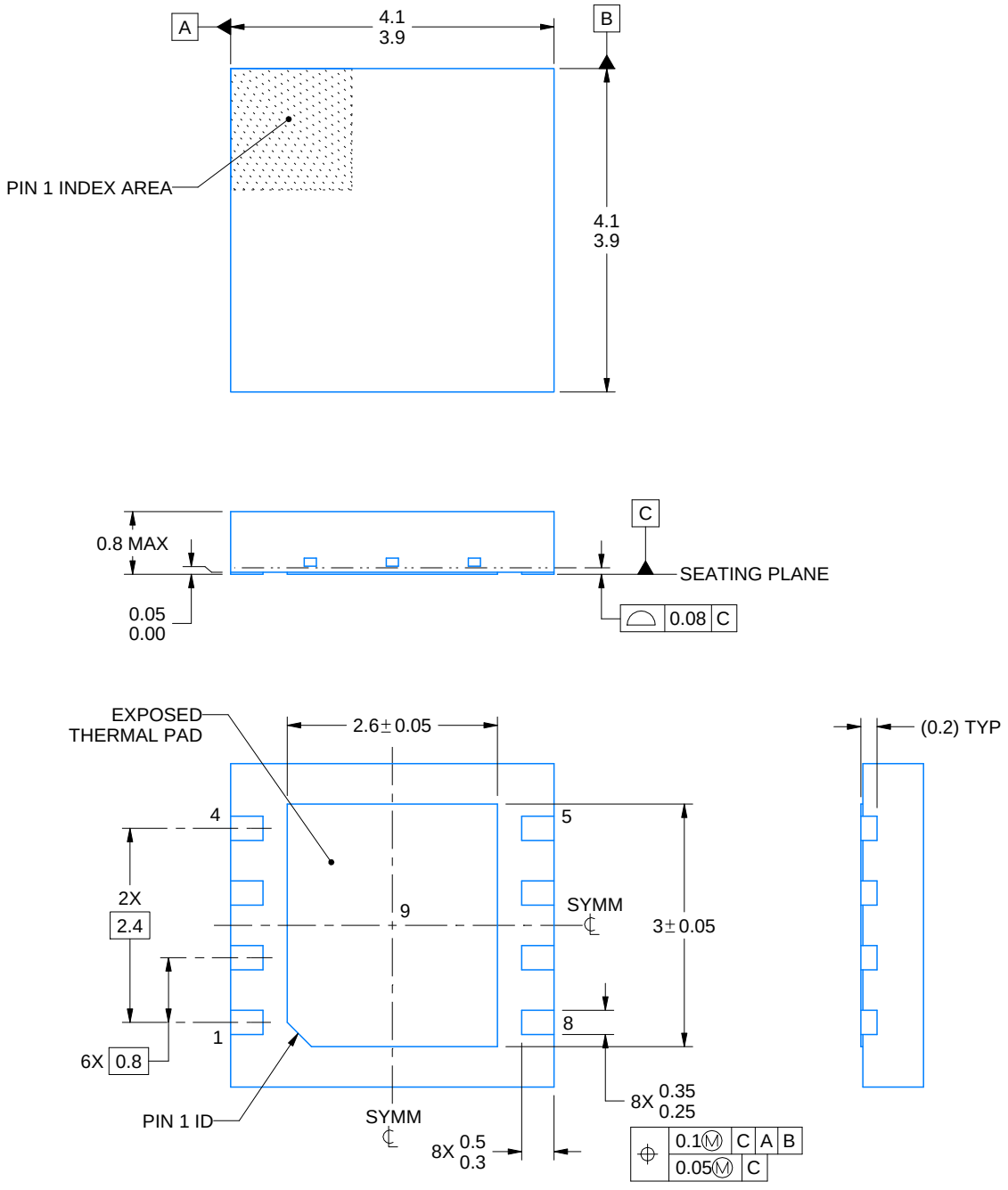
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
LM5002MA/NOPB	D	SOIC	8	95	495	8	4064	3.05
LM5002MA/NOPB.A	D	SOIC	8	95	495	8	4064	3.05
LM5002MA/NOPB.B	D	SOIC	8	95	495	8	4064	3.05

PACKAGE OUTLINE

NGT0008A

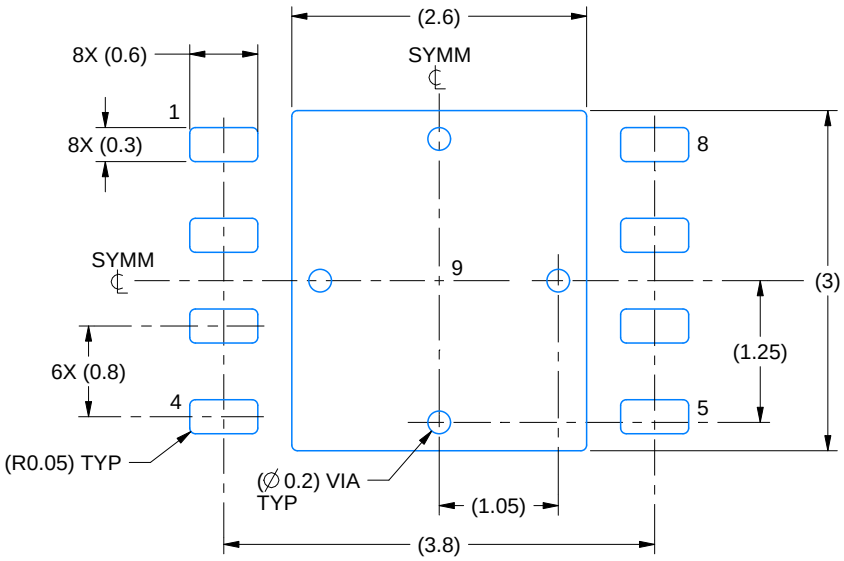
WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

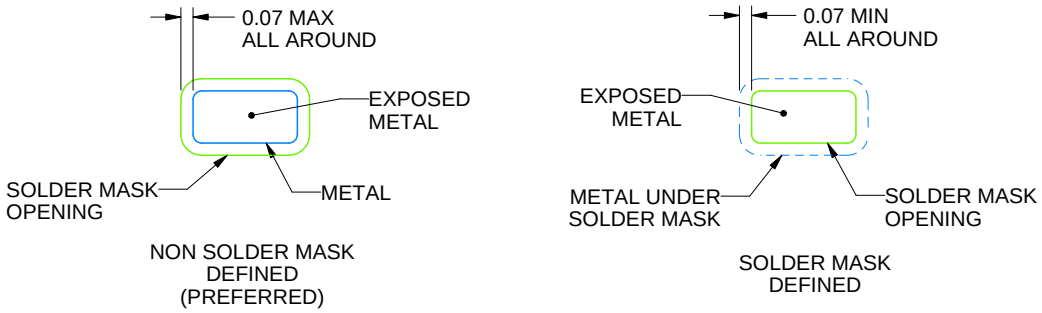


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

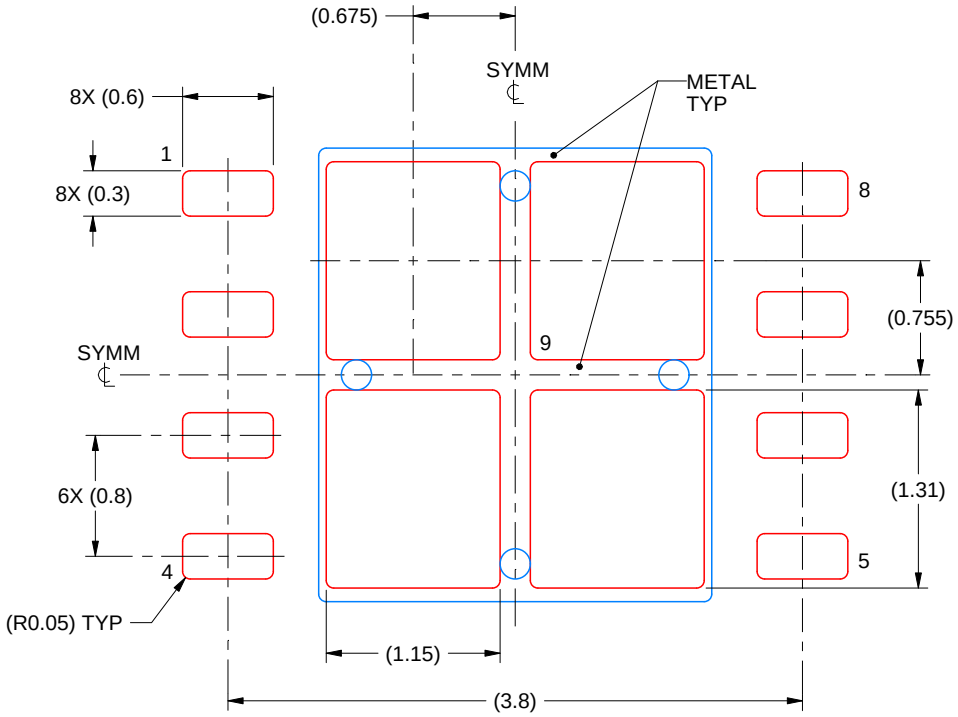


SOLDER MASK DETAILS

4214935/A 08/2020

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



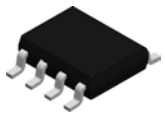
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 9:
77% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

4214935/A 08/2020

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

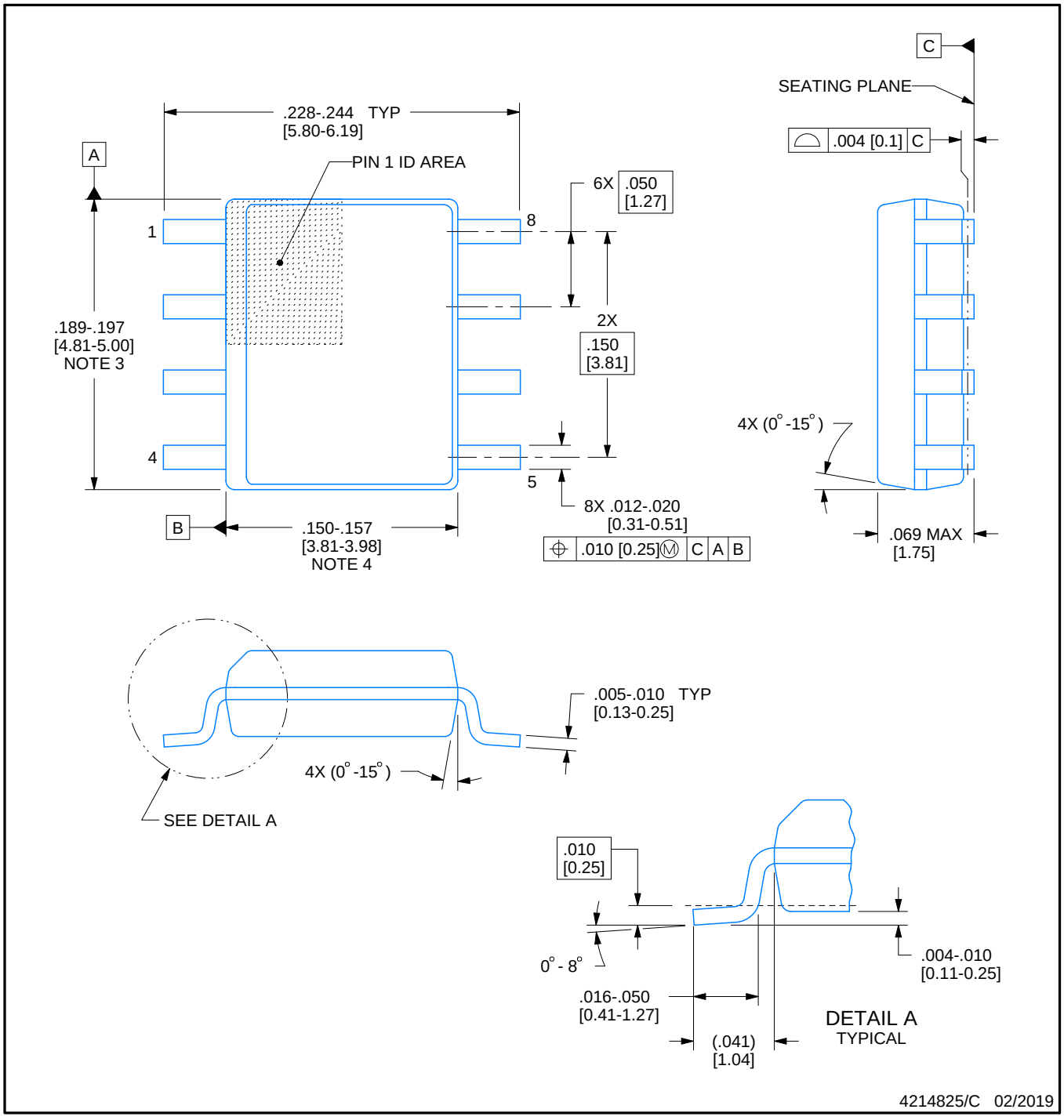


PACKAGE OUTLINE

D0008A

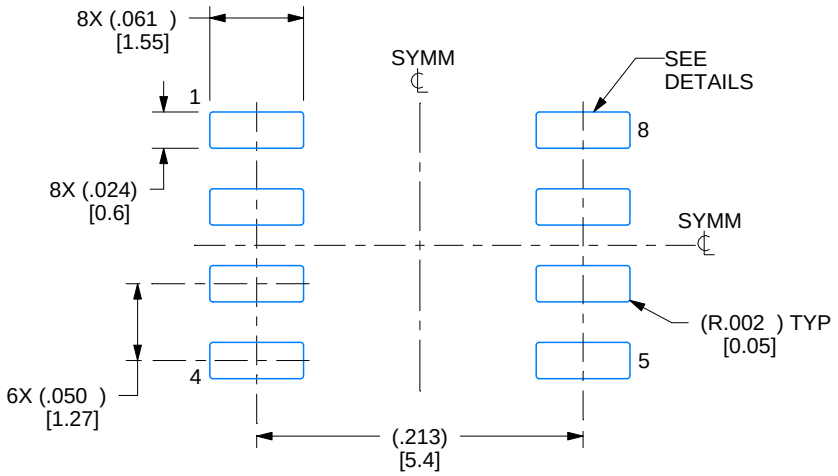
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

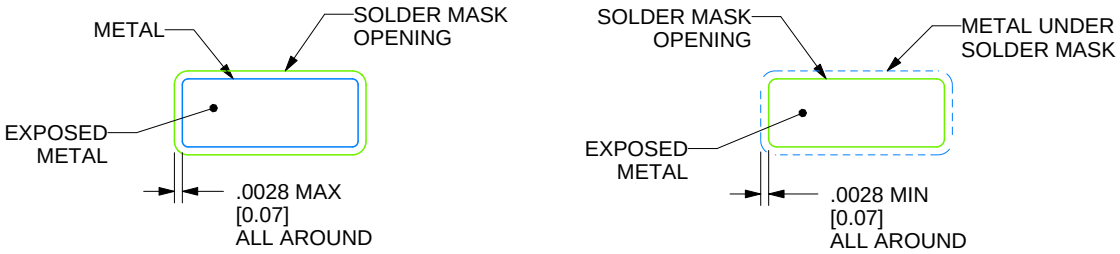


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

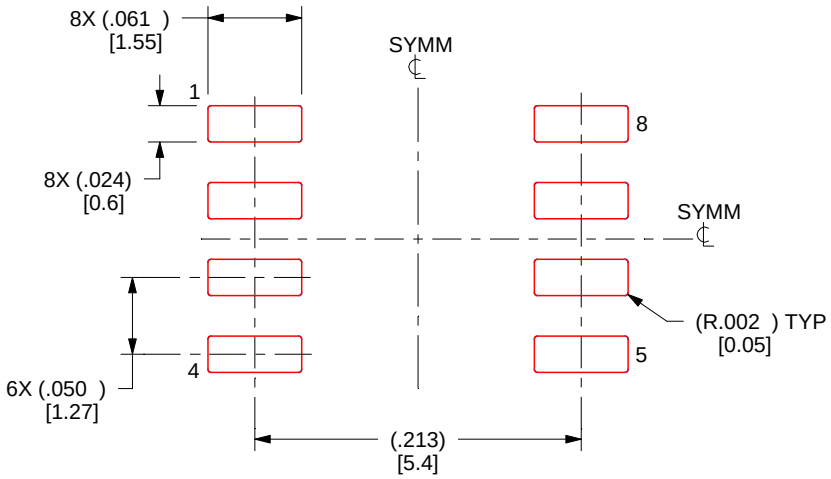
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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最終更新日：2025 年 10 月