LM5008 95V、350mA、コンスタント・オンタイム(COT) DC/DC降圧スイッチング・レギュレータ

1 特長

- 動作入力電圧範囲(6V～95V)
- 100VのNチャネル降圧スイッチを内蔵
- V_{CC}レギュレータを内蔵
- ループ補償が不要
- 超高速の過渡応答
- オン時間はライン電圧と反比例
- ライン電圧や負荷電流の変動に対して動作周波数を一定に維持
- 可変出力電圧
- 高効率動作
- 高精度な内部リファレンス電圧
- 低いバイアス電流
- インテリジェントな電流制限保護機能
- サーマル・シャットダウン
- 8ピンVSSOPおよびWSONパッケージ
- WEBENCH® Power Designerにより、LM5008を使用するカスタム設計を作成

2 アプリケーション

- 通信機器向けの非絶縁型降圧レギュレータ
- 2次側高電圧ポスト・レギュレータ
- 48V車載システム

3 概要

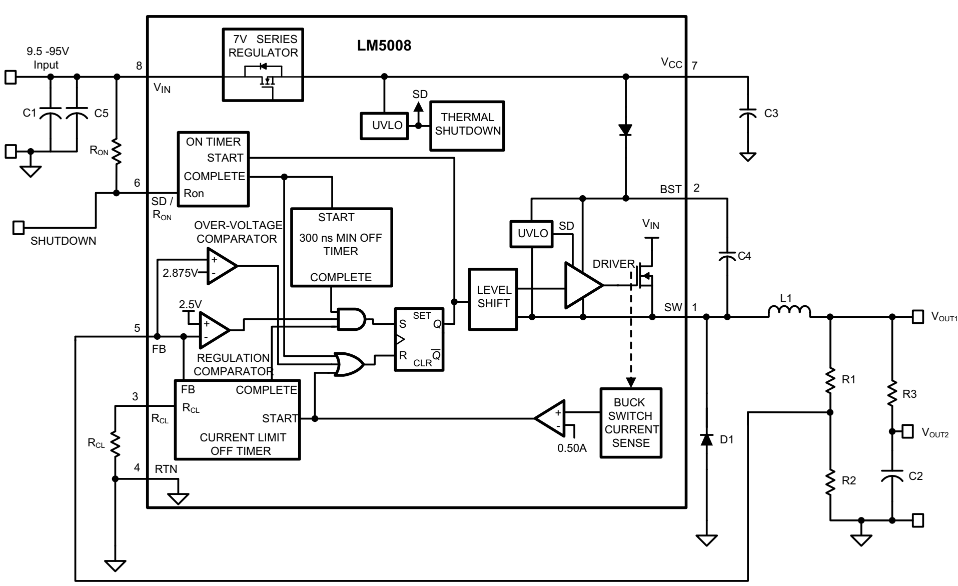
LM5008 350mA降圧スイッチング・コンバータには、低コスト、高効率の降圧レギュレータを実装するために必要な、すべての機能が搭載されています。この高電圧コンバータには、100V Nチャネル降圧スイッチが内蔵されており、9 V～95Vの入力電圧範囲で動作します。このデバイスは実装が簡単で、8ピンVSSOPおよび熱的に強化された8ピンWSONパッケージで供給されます。このコンバータは、PWMオン時間がV_{IN}に反比例するヒステリシス制御方式を使っています。この機能により、動作周波数を比較的一定に保つことが可能になります。このヒステリシス制御方式では、ループ補償は不要です。強制オフ時間を持つインテリジェントな電流制限を実装し、オフ時間はV_{OUT}に反比例します。この方式により、最小限のフォールドバックで短絡保護が実現されます。他の保護機能として、サーマル・シャットダウン、V_{CC}低電圧誤動作防止、ゲート・ドライブ低電圧誤動作防止、最大デューティ・サイクル制限などがあります。

製品情報(1)

型番	パッケージ	本体サイズ(公称)
LM5008	VSSOP (8)	3.00mm×3.00mm
	WSON (8)	4.00mm×4.00mm

(1) 提供されているすべてのパッケージについては、データシートの末尾にある注文情報を参照してください。

代表的なアプリケーション回路とブロック図



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4 改訂履歴

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Revision H (December 2016) から **Revision I** に変更 — **Page**

- WEBENCH用のリンク 追加 1
- 「*製品情報*」で、VSSOP-8の本体サイズを3mm×3mmに 変更 1
- Changed *Layout Guidelines* 17

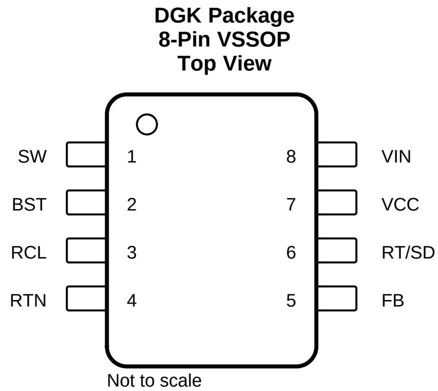
Revision G (March 2013) から **Revision H** に変更 — **Page**

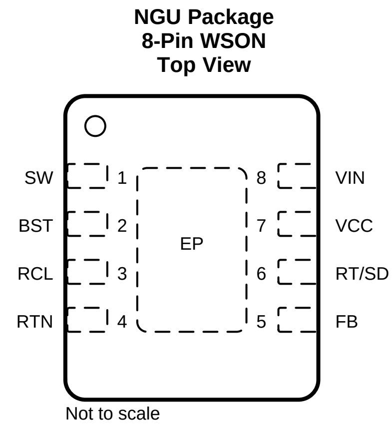
- 「*ESD定格*」表、「*機能説明*」セクション、「*デバイスの機能モード*」セクション、「*アプリケーションと実装*」セクション、「*電源に関する推奨事項*」セクション、「*レイアウト*」セクション、「*デバイスおよびドキュメントのサポート*」セクション、「*メカニカル、パッケージ、および注文情報*」セクション 追加 1
- Deleted Lead temperature, soldering (260°C maximum) 4
- Changed $R_{\theta JA}$ values From: 200°C/W To: 139.7°C/W (VSSOP) and From: 40°C/W To: 42°C/W (WSON) 4

Revision F (March 2013) から **Revision G** に変更 — **Page**

- ナショナル・セミコンダクターのデータシートのレイアウトをTIフォーマットに 変更 1

5 Pin Configuration and Functions





Pin Functions

PIN		TYPE	DESCRIPTION
NO.	NAME		
1	SW	P	Switching node: power switching node. Connect to the output inductor, re-circulating diode, and bootstrap capacitor.
2	BST	I	Boost pin (bootstrap capacitor input): an external capacitor is required between the BST and the SW pins. A 0.01-µF ceramic capacitor is recommended. An internal diode charges the capacitor from V_{CC}.
3	R_{CL}	I	Current limit OFF time set pin: a resistor between this pin and RTN sets the off-time when current limit is detected. The off-time is preset to 35 µs if FB = 0 V. Toff = 10^{-5} / (0.285 + (FB / 6.35 × 10^{-6} × R_{CL}))
4	RTN	G	Ground pin: ground for the entire circuit.
5	FB	I	Feedback input from regulated output: this pin is connected to the inverting input of the internal regulation comparator. The regulation threshold is 2.5 V.
6	R_{ON}/SD	I	On-time set pin: a resistor between this pin and V_{IN} sets the switch on-time as a function of V_{IN}. The minimum recommended on-time is 400 ns at the maximum input voltage. This pin can be used for remote shutdown. Ton = 1.25 × 10^{-10} R_{ON} / V_{IN}
7	V_{CC}	P	Output from the internal high voltage series pass regulator. Regulated at 7 V. If an auxiliary voltage is available to raise the voltage on this pin, above the regulation set point (7 V), the internal series pass regulator will shutdown, reducing the IC power dissipation. Do not exceed 14 V. This voltage provides gate drive power for the internal buck switch. An internal diode is provided between this pin and the BST pin. A local 0.1-µF decoupling capacitor is recommended. Series pass regulator is current limited to 10 mA.
8	V_{IN}	P	Input voltage: recommended operating range is 9.5 V to 95 V.
—	EP	G	Exposed pad: the exposed pad has no electrical contact. Connect to system ground plane for reduced thermal resistance (WSON package only).

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

	MIN	MAX	UNIT
V_{IN} to GND	–0.3	100	V
BST to GND	–0.3	114	V
SW to GND (steady-state)		–1	V
BST to V_{CC}		100	V
BST to SW		14	V
V_{CC} to GND		14	V
All other inputs to GND	–0.3	7	V
Storage temperature, T_{stg}	–55	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)(2)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(3)	±750	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) The human body model is a 100-pF capacitor discharged through a 1.5-kΩ resistor into each pin.
(3) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	MAX	UNIT
V_{IN}	9.5	95	V
Operating junction temperature, T_J	–40	125	°C

6.4 Thermal Information

THERMAL METRIC(1)		LM5008		UNIT
		DGK (VSSOP)	NGU (WSON)	
		8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	139.7	42	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	51.2	27.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	70.5	18.5	°C/W
ψ_{JT}	Junction-to-top characterization parameter	3.4	0.3	°C/W
ψ_{JB}	Junction-to-board characterization parameter	69.5	18.5	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	—	4.3	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics

Specifications are for T_J = 25°C and V_{IN} = 48 V (unless otherwise stated)(1).

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{CC} SUPPLY							
V_{CC} Reg	V_{CC} regulator output	T_J = 25°C			7		V
		T_J = –40°C to 125°C		6.6		7.4	
	V_{CC} current limit(2)				9.5		mA
	V_{CC} undervoltage lockout voltage	V_{CC} increasing			6.3		V
	V_{CC} undervoltage hysteresis				200		mV
	V_{CC} UVLO delay (filter)	100-mV overdrive			10		µs
	I_{IN} operating current	Non-switching, FB = 3 V	T_J = 25°C		485		µA
			T_J = –40°C to 125°C			675	
	I_{IN} shutdown current	R_{ON}/SD = 0 V	T_J = 25°C		76		µA
			T_J = –40°C to 125°C			150	
CURRENT LIMIT							
	Current limit threshold	T_J = 25°C			0.51		A
		T_J = –40°C to 125°C		0.41		0.61	
	Current limit response time	I_{switch} overdrive = 0.1 A, time to switch off			400		ns
	OFF time generator (test 1)	FB = 0 V, R_{CL} = 100 K			35		µs
	OFF time generator (test 2)	FB = 2.3 V, R_{CL} = 100 K			2.56		µs
ON-TIME GENERATOR							
	T_{ON} – 1	V_{IN} = 10 V, R_{ON} = 200 K	T_J = 25°C		2.77		µs
			T_J = –40°C to 125°C	2.15		3.5	
	T_{ON} – 2	V_{IN} = 95 V, R_{ON} = 200 K	T_J = 25°C		300		ns
			T_J = –40°C to 125°C	200		420	
	Remote shutdown threshold	Rising	T_J = 25°C		0.7		V
			T_J = –40°C to 125°C	0.4		1.05	
	Remote shutdown hysteresis				35		mV
MINIMUM OFF-TIME							
	Minimum off-timer	FB = 0 V			300		ns
REGULATION AND OV COMPARATORS							
	FB reference threshold	Internal reference, trip point for switch ON	T_J = 25°C		2.5		V
			T_J = –40°C to 125°C	2.445		2.55	
	FB overvoltage threshold	Trip point for switch OFF			2.875		V
	FB bias current				100		nA
THERMAL SHUTDOWN							
Tsd	Thermal shutdown temperature				165		°C
	Thermal shutdown hysteresis				25		°C

(1) All electrical characteristics having room temperature limits are tested during production with T_A = T_J = 25°C. All hot and cold limits are specified by correlating the electrical characteristics to process and temperature variations and applying statistical process control.
(2) The V_{CC} output is intended as a self bias for the internal gate drive power and control circuits. Device thermal limitations limit external loading.

6.6 Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
Buck switch $R_{DS(on)}$	I_{TEST} = 200 mA(1)	T_J = 25°C		1.15		Ω
		T_J = –40°C to 125°C			2.47	
Gate drive UVLO	V_{BST} – V_{SW} rising	T_J = 25°C		4.5		V
		T_J = –40°C to 125°C	3.4		5.5	
Gate drive UVLO hysteresis				430		mV

(1) For devices procured in the 8-pin WSON package the $R_{DS(on)}$ limits are specified by design characterization data only.

6.7 Typical Characteristics

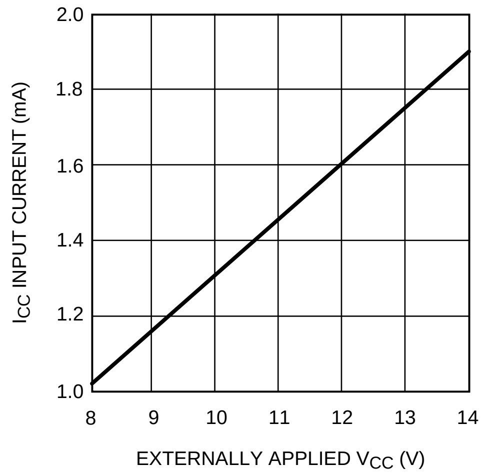


Figure 1. I_{CC} Current vs Applied V_{CC} Voltage

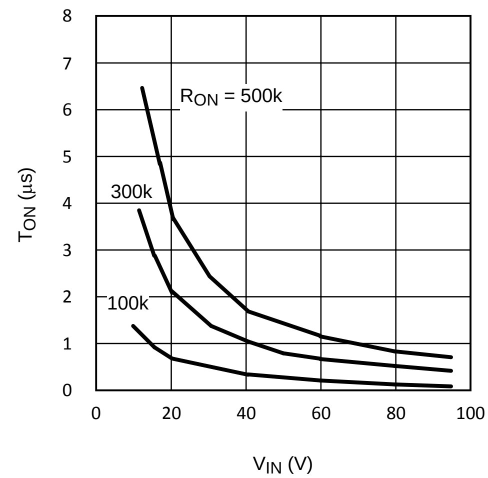


Figure 2. On-Time vs Input Voltage and R_{ON}

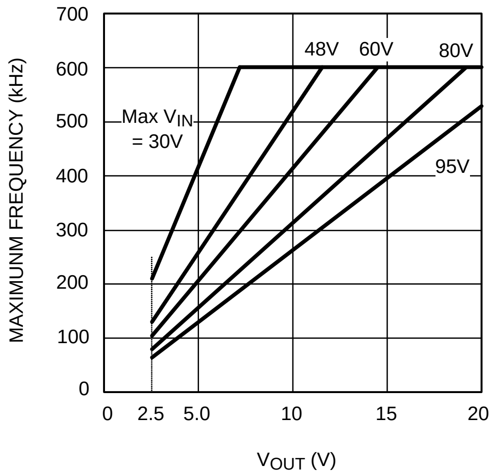


Figure 3. Maximum Frequency vs V_{OUT} and V_{IN}

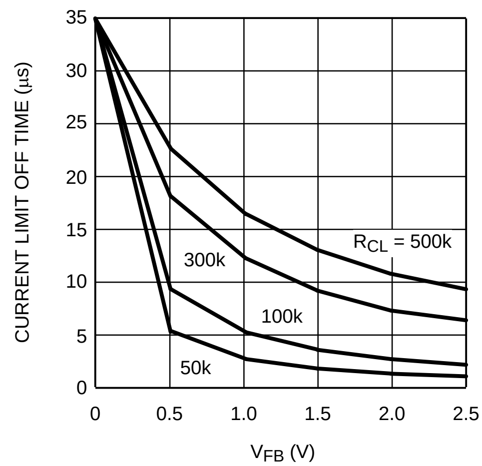


Figure 4. Current Limit Off-Time vs V_{FB} and R_{CL}

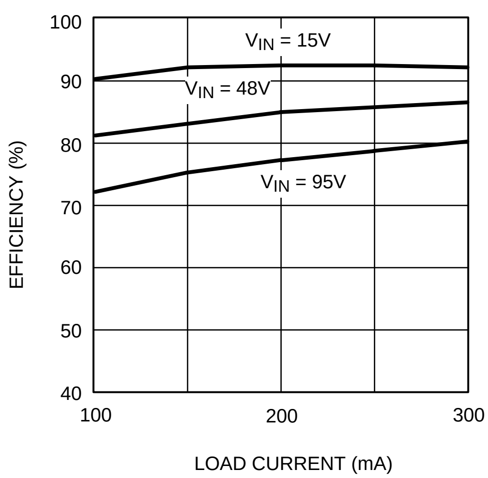


Figure 5. Efficiency vs Load Current vs V_{IN} (Circuit of Figure 10)

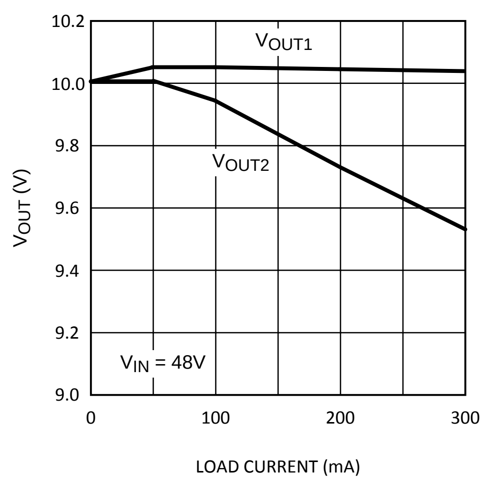


Figure 6. Output Voltage vs Load Current (Circuit of Figure 10)

7 Detailed Description

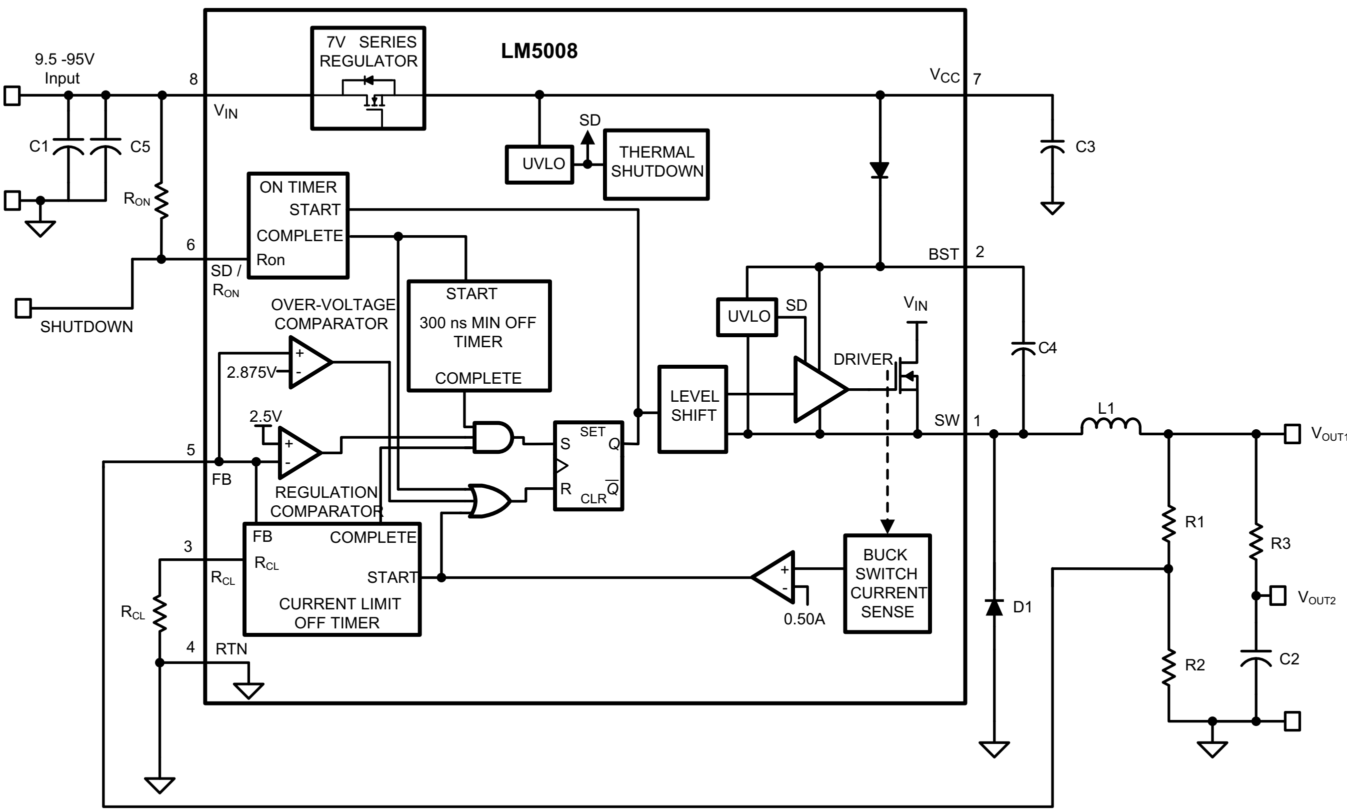
7.1 Overview

The LM5008 regulator is an easy-to-use buck DC-DC converter that operates from 9.5-V to 95-V supply voltage. The device is intended for step-down conversions from 12-V, 24-V, and 48-V unregulated, semi-regulated and fully-regulated supply rails. With integrated buck power MOSFET, the LM5008 delivers up to 350-mA DC load current with exceptional efficiency and low input quiescent current in a very small solution size.

Designed for simple implementation, a nearly fixed-frequency, constant on-time (COT) operation with discontinuous conduction mode (DCM) at light loads is ideal for low-noise, high current, fast transient load requirements. Control loop compensation is not required reducing design time and external component count.

The LM5008 incorporates other features for comprehensive system requirements, including VCC undervoltage lockout (UVLO), gate drive undervoltage lockout, maximum duty cycle limiter, intelligent current limit off timer, a precharge switch, and thermal shutdown with automatic recovery. These features enable a flexible and easy-to-use platform for a wide range of applications. The pin arrangement is designed for simple and optimized PCB layout, requiring only a few external components.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Hysteretic Control Circuit Overview

The LM5008 is a buck DC-DC regulator that uses a control scheme in which the on-time varies inversely with line voltage (V_{IN}). Control is based on a comparator and the on-time one-shot, with the output voltage feedback (FB) compared to an internal reference (2.5 V). If the FB level is below the reference the buck switch is turned on for a fixed time determined by the line voltage and a programming resistor (R_{ON}). Following the ON period, the switch remains off for at least the minimum off-timer period of 300 ns. If FB is still below the reference at that time, the switch turns on again for another on-time period. This will continue until regulation is achieved.

The LM5008 operates in discontinuous conduction mode at light load currents, and continuous conduction mode at heavy load current. In discontinuous conduction mode, current through the output inductor starts at zero and ramps up to a peak during the on-time, then ramps back to zero before the end of the off-time. The next on-time period starts when the voltage at FB falls below the internal reference; until then, the inductor current remains zero. In this mode the operating frequency is lower than in continuous conduction mode, and varies with load current. Therefore at light loads the conversion efficiency is maintained, because the switching losses reduce with the reduction in load and frequency. The discontinuous operating frequency can be calculated with Equation 1.

$$F = \frac{V_{OUT}^2 \times L \times 1.28 \times 10^{20}}{R_L \times (R_{ON})^2}$$

where

- R_L = the load resistance (1)

In continuous conduction mode, current flows continuously through the inductor and never ramps down to zero. In this mode the operating frequency is greater than the discontinuous mode frequency and remains relatively constant with load and line variations. The approximate continuous mode operating frequency can be calculated with Equation 2.

$$F = \frac{V_{OUT}}{1.25 \times 10^{-10} \times R_{ON}} \quad (2)$$

The output voltage (V_{OUT}) can be programmed by two external resistors as shown in *Functional Block Diagram*. The regulation point can be calculated with Equation 3.

$$V_{OUT} = 2.5 \times (R1 + R2) / R2 \quad (3)$$

All hysteretic regulators regulate the output voltage based on ripple voltage at the feedback input, requiring a minimum amount of ESR for the output capacitor C2. A minimum of 25 mV to 50 mV of ripple voltage at the feedback pin (FB) is required for the LM5008. In cases where the capacitor ESR is too small, additional series resistance may be required (R3 in *Functional Block Diagram*).

For applications where lower output voltage ripple is required the output can be taken directly from a low-ESR output capacitor, as shown in Figure 7. However, R3 slightly degrades the load regulation.

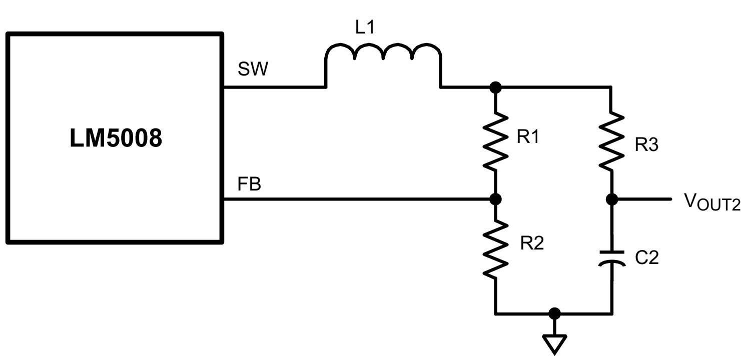


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Figure 7. Low-Ripple Output Configuration

Feature Description (continued)

7.3.2 High Voltage Start-Up Regulator

The LM5008 contains an internal high voltage start-up regulator. The input pin (V_{IN}) can be connected directly to the line voltages up to 95 Volts, with transient capability to 100 V. The regulator is internally current limited to 9.5 mA at V_{CC}. Upon power up, the regulator sources current into the external capacitor at V_{CC} (C3). When the voltage on the V_{CC} pin reaches the undervoltage lockout threshold of 6.3 V, the buck switch is enabled.

In applications involving a high value for V_{IN}, where power dissipation in the V_{CC} regulator is a concern, an auxiliary voltage can be diode connected to the V_{CC} pin. Setting the auxiliary voltage to 8 V to 14 V shuts off the internal regulator, reducing internal power dissipation. See Figure 8. The current required into the V_{CC} pin is shown in Figure 1.

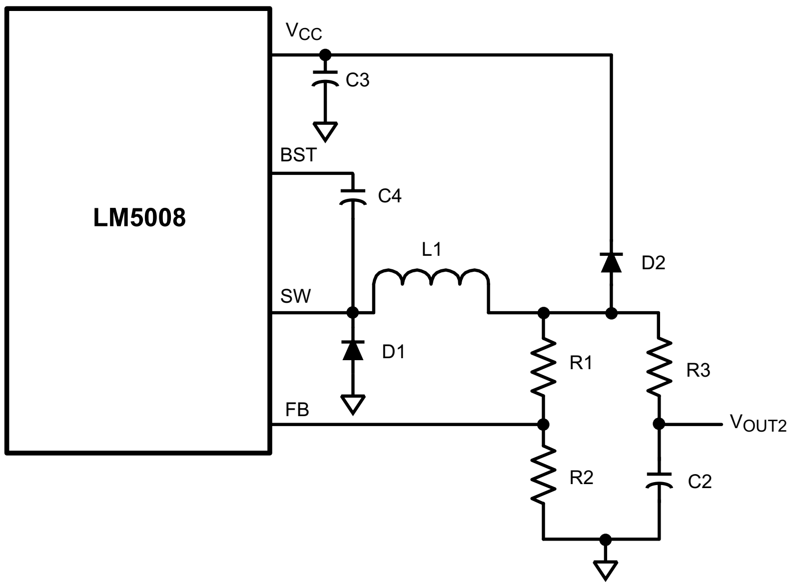

Figure 8. Self-Biased Configuration

7.3.3 Regulation Comparator

The feedback voltage at FB is compared to an internal 2.5-V reference. In normal operation (the output voltage is regulated), an on-time period is initiated when the voltage at FB falls below 2.5 V. The buck switch stays on for the on-time, causing the FB voltage to rise above 2.5 V. After the on-time period, the buck switch stays off until the FB voltage again falls below 2.5 V. During start-up, the FB voltage is below 2.5 V at the end of each on-time, resulting in the minimum off-time of 300 ns. Bias current at the FB pin is nominally 100 nA.

7.3.4 Overvoltage Comparator

The feedback voltage at FB is compared to an internal 2.875-V reference. If the voltage at FB rises above 2.875 V, the on-time pulse is immediately terminated. This condition can occur if the input voltage, or the output load, change suddenly. The buck switch will not turn on again until the voltage at FB falls below 2.5 V.

7.3.5 On-Time Generator and Shutdown

The on-time for the LM5008 is determined by the R_{ON} resistor, and is inversely proportional to the input voltage (V_{IN}), resulting in a nearly constant frequency as V_{IN} is varied over its range. Equation 4 shows the on-time equation for the LM5008.

$$T_{ON} = 1.25 \times 10^{-10} \times R_{ON} / V_{IN} \quad (4)$$

See Figure 2. R_{ON} should be selected for a minimum on-time (at maximum V_{IN}) greater than 400 ns for proper current limit operation. This requirement limits the maximum frequency for each application, depending on V_{IN} and V_{OUT}. See Figure 3.

Feature Description (continued)

The LM5008 can be remotely disabled by taking the R_{ON}/SD pin to ground. See Figure 9. The voltage at the R_{ON}/SD pin is between 1.5 and 3 volts, depending on V_{IN} and the value of the R_{ON} resistor.

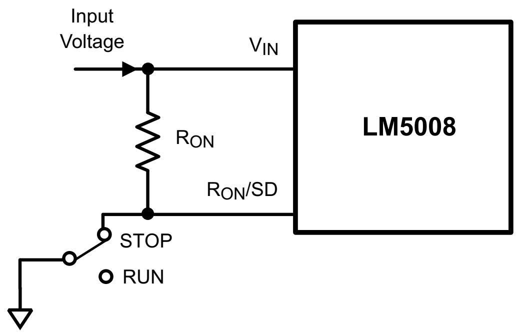

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Figure 9. Shutdown Implementation

7.3.6 Current Limit

The LM5008 contains an intelligent current limit off-timer. If the current in the buck switch exceeds 0.5 A the present cycle is immediately terminated, and a non-resetable off-timer is initiated. The length of off-time is controlled by an external resistor (R_{CL}) and the FB voltage (see Figure 4). When FB = 0 V, a maximum off-time is required, and the time is preset to 35 µs. This condition occurs when the output is shorted, and during the initial part of start-up. This amount of time ensures safe short-circuit operation up to the maximum input voltage of 95 V. In cases of overload where the FB voltage is above zero volts (not a short circuit), the current limit off-time will be less than 35 µs. Reducing the off-time during less severe overloads reduces the amount of foldback, recovery time, and the start-up time. The off-time is calculated from Equation 5.

$$T_{OFF} = \frac{10^{-5}}{0.285 + \frac{V_{FB}}{(6.35 \times 10^{-6} \times R_{CL})}} \quad (5)$$

The current limit sensing circuit is blanked for the first 50-70 ns of each on-time so it is not falsely tripped by the current surge which occurs at turnon. The current surge is required by the re-circulating diode (D1) for its turnoff recovery.

7.3.7 N-Channel Buck Switch and Driver

The LM5008 integrates an N-Channel Buck switch and associated floating high voltage gate driver. The gate driver circuit works in conjunction with an external bootstrap capacitor and an internal high voltage diode. A 0.01-µF ceramic capacitor (C4) connected between the BST pin and SW pin provides the voltage to the driver during the on-time.

During each off-time, the SW pin is at approximately 0 V, and the bootstrap capacitor charges from V_{CC} through the internal diode. The minimum off-timer, set to 300 ns, ensures a minimum time each cycle to recharge the bootstrap capacitor.

An external re-circulating diode (D1) carries the inductor current after the internal Buck switch turns off. This diode must be of the ultra-fast or Schottky type to minimize turnon losses and current overshoot.

7.3.8 Thermal Protection

The LM5008 must be operated so the junction temperature does not exceed 125°C during normal operation. An internal thermal shutdown circuit is provided to protect the LM5008 in the event of a higher than normal junction temperature. When activated, typically at 165°C, the controller is forced into a low power reset state, disabling the buck switch and the V_{CC} regulator. This feature prevents catastrophic failures from accidental device overheating. When the junction temperature reduces below 140°C (typical hysteresis = 25°C), the V_{CC} regulator is enabled, and normal operation is resumed.

7.4 Device Functional Modes

7.4.1 Shutdown Mode

The R^{ON}/SD pin provides ON and OFF control for the LM5008. When V_{SD} is below approximately 0.7 V, the device is in shutdown mode. Both the internal LDO and the switching regulator are off. The quiescent current in shutdown mode drops to 76 µA (typical) at V_{IN} = 48 V. The LM5008 also employs VCC bias rail undervoltage protection. If the V_{CC} bias supply voltage is below its UV threshold, the regulator remains off.

7.4.2 Active Mode

LM5008 is in active mode when the internal bias rail, VCC, is above its UV threshold. Depending on the load current, the device operates in either DCM or CCM mode.

Whenever the load current is reduced to a level less than half the peak-to-peak inductor ripple current, the device enters discontinuous conduction mode (DCM). Calculate the critical conduction boundary using Equation 6.

$$I_{BOUNDARY} = \frac{\Delta I_L}{2} = \frac{V_{OUT} \cdot (1 - D)}{2 \cdot L_F \cdot F_{SW}} \tag{6}$$

When the inductor current reaches zero, the SW node becomes high impedance. Resonant ringing occurs at SW as a result of the LC tank circuit formed by the buck inductor and the parasitic capacitance at the SW node. At light loads, several pulses may be skipped in between switching cycles, effectively reducing the switching frequency and further improving light-load efficiency.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The final circuit is shown in Figure 10. The circuit was tested, and the resulting performance is shown in Figure 12 through Figure 6.

8.1.1 Minimum Load Current

A minimum load current of 1 mA is required to maintain proper operation. If the load current falls below that level, the bootstrap capacitor may discharge during the long off-time, and the circuit will either shutdown or cycle on and off at a low frequency. If the load current is expected to drop below 1 mA in the application, the feedback resistors should be chosen low enough in value so they provide the minimum required current at nominal V_{OUT}.

8.2 Typical Application

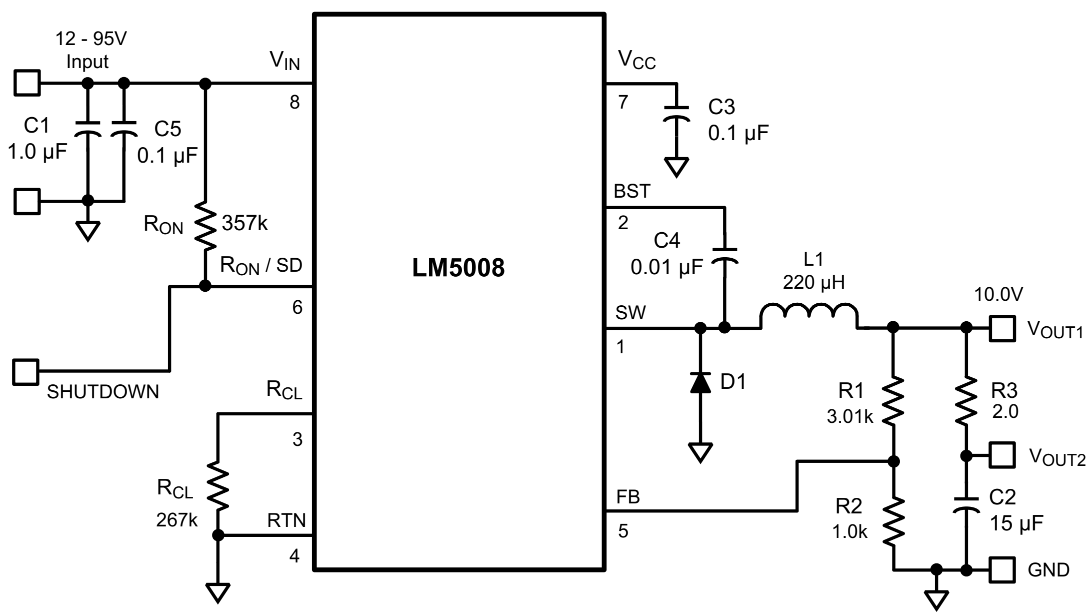

Figure 10. LM5008 Example Circuit

8.2.1 Design Requirements

A guide for determining the component values will be illustrated with a design example. Table 1 lists the bill of materials for this application. The following steps will configure the LM5008 for:

- Input voltage range (V_{IN}): 12 V to 95 V
- Output voltage (V_{OUT1}): 10 V
- Load current (for continuous conduction mode): 100 mA to 300 mA
- Maximum ripple at V_{OUT2}: 100 mVp-p at maximum input voltage

Typical Application (continued)

Table 1. Bill of Materials (Circuit of Figure 10)

ITEM	DESCRIPTION	PART NUMBER	VALUE
C1	Ceramic Capacitor	TDK C4532X7R2A105M	1 µF, 100 V
C2	Ceramic Capacitor	TDK C4532X7R1E156M	15 µF, 25 V
C3	Ceramic Capacitor	Kemet C1206C104K5RAC	0.1 µF, 50 V
C4	Ceramic Capacitor	Kemet C1206C103K5RAC	0.01 µF, 50 V
C5	Ceramic Capacitor	TDK C3216X7R2A104M	0.1 µF, 100 V
D1	Ultra-Fast Power Diode	ON Semi MURA110T3	100 V, 1 A
L1	Power Inductor	Coilcraft DO3316-224 or	220 µH
		TDK SLF10145T-221MR65	
R1	Resistor	Vishay CRCW12063011F	3.01 kΩ
R2	Resistor	Vishay CRCW12061001F	1 kΩ
R3	Resistor	Vishay CRCW12062R00F	2 Ω
R_{ON}	Resistor	Vishay CRCW12063573F	357 kΩ
R_{CL}	Resistor	Vishay CRCW12062673F	267 kΩ
U1	Switching Regulator	Texas Instruments LM5008	

8.2.2 Detailed Design Procedure

8.2.2.1 Custom Design With WEBENCH® Tools

Click here to create a custom design using the LM5008 device with the WEBENCH® Power Designer.

1. Start by entering the input voltage (V_{IN}), output voltage (V_{OUT}), and output current (I_{OUT}) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance
- Run thermal simulations to understand board thermal performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

R1 and R2: From *Functional Block Diagram*, $V_{OUT1} = V_{FB} \times (R1 + R2) / R2$, and because V_{FB} = 2.5 V, the ratio of R1 to R2 calculates as 3:1. Standard values of 3.01 kΩ (R1) and 1.00 kΩ (R2) are chosen. Other values could be used as long as the 3:1 ratio is maintained. The selected values, however, provide a small amount of output loading (2.5 mA) in the event the main load is disconnected. This allows the circuit to maintain regulation until the main load is reconnected.

F_s and R_{ON}: The recommended operating frequency range for the LM5008 is 50 kHz to 600 kHz. Unless the application requires a specific frequency, the choice of frequency is generally a compromise because it affects the size of L1 and C2, and the switching losses. The maximum allowed frequency, based on a minimum on-time of 400 ns, is calculated from Equation 7:

$$F_{MAX} = V_{OUT} / (V_{INMAX} \times 400\ \text{ns}) \tag{7}$$

For this exercise, F_{MAX} = 263 kHz. From Equation 2, R_{ON} calculates to 304 kΩ. A standard value 357-kΩ resistor is used to allow for tolerances in Equation 2, resulting in a frequency of 224 kHz.

L1: The main parameter affected by the inductor is the output current ripple amplitude. The choice of inductor value therefore depends on both the minimum and maximum load currents, keeping in mind that the maximum ripple current occurs at maximum V_{IN}.

a. **Minimum load current:** To maintain continuous conduction at minimum Io (100 mA), the ripple amplitude

(I_{OR}) must be less than 200 mAp-p so the lower peak of the waveform does not reach zero. L1 is calculated using Equation 8.

$$L1 = \frac{V_{OUT1} \times (V_{IN} - V_{OUT1})}{I_{OR} \times F_s \times V_{IN}} \tag{8}$$

At V_{IN} = 95 V, L1 (minimum) calculates to 200 µH. The next larger standard value (220 µH) is chosen and with this value I_{OR} calculates to 181 mAp-p at V_{IN} = 95 V, and 34 mAp-p at V_{IN} = 12 V.

b. **Maximum load current:** At a load current of 300 mA, the peak of the ripple waveform must not reach the minimum value of the LM5008's current limit threshold (410 mA). Therefore the ripple amplitude must be less than 220 mAp-p, which is already satisfied in Equation 8. With L1 = 220 µH, at maximum V_{IN} and I_O, the peak of the ripple will be 391 mA. While L1 must carry this peak current without saturating or exceeding its temperature rating, it also must be capable of carrying the maximum value of the LM5008's current limit threshold (610 mA) without saturating, because the current limit is reached during start-up.

The DC resistance of the inductor should be as low as possible. For example, if the inductor's DCR is 1 Ω, the power dissipated at maximum load current is 0.09 W. While small, it is not insignificant compared to the load power of 3 W.

C3: The capacitor on the V_{CC} output provides not only noise filtering and stability, but its primary purpose is to prevent false triggering of the V_{CC} UVLO at the buck switch ON/OFF transitions. For this reason, C3 should be no smaller than 0.1 µF.

C2, and R3: When selecting the output filter capacitor C2, the items to consider are ripple voltage due to its ESR, ripple voltage due to its capacitance, and the nature of the load.

a. **ESR and R3:** A low ESR for C2 is generally desirable so as to minimize power losses and heating within the capacitor. However, a hysteretic regulator requires a minimum amount of ripple voltage at the feedback input for proper loop operation. For the LM5008 the minimum ripple required at pin 5 is 25 mVp-p, requiring a minimum ripple at V_{OUT1} of 100 mV. Because the minimum ripple current (at minimum V_{IN}) is 34 mAp-p, the minimum ESR required at V_{OUT1} is 100 mV / 34 mA = 2.94 Ω. Because quality capacitors for SMPS applications have an ESR considerably less than this, R3 is inserted as shown in *Functional Block Diagram*. R3's value, along with C2's ESR, must result in at least 25 mVp-p ripple at pin 5. Generally, R3 will be 0.5 to 3 Ω.

b. **Nature of the Load:** The load can be connected to V_{OUT1} or V_{OUT2}. V_{OUT1} provides good regulation, but with a ripple voltage which ranges from 100 mV (at V_{IN} = 12 V) to 500 mV (at V_{IN} = 95 V). Alternatively, V_{OUT2} provides low ripple, but lower regulation due to R3.

For a maximum allowed ripple voltage of 100 mVp-p at V_{OUT2} (at V_{IN} = 95 V), assume an ESR of 0.4 Ω for C2. At maximum V_{IN}, the ripple current is 181 mAp-p, creating a ripple voltage of 72 mVp-p. This leaves 28 mVp-p of ripple due to the capacitance. The average current into C2 due to the ripple current is calculated using the waveform in Figure 11.

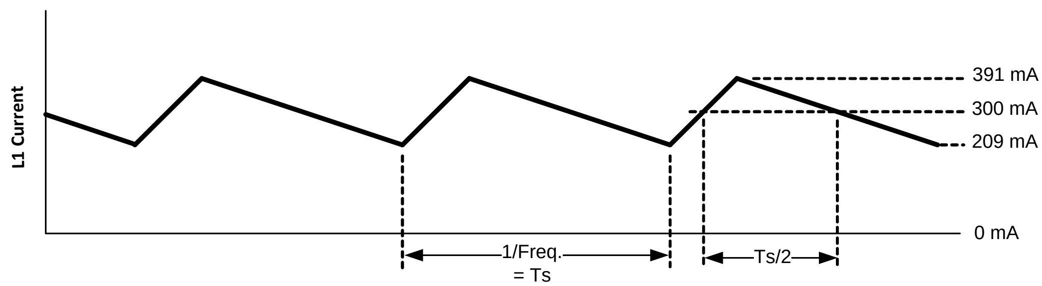

Figure 11. Inductor Current Waveform

Starting when the current reaches Io (300 mA in Figure 11) half way through the on-time, the current continues to increase to the peak (391 mA), and then decreases to 300 mA half way through the off-time. The average value of this portion of the waveform is 45.5 mA, and will cause half of the voltage ripple, or 14 mV. The interval is one half of the frequency cycle time, or 2.23 µs. Using the capacitor's basic equation (see Equation 9), the minimum value for C2 is 7.2 µF.

The ripple due to C2's capacitance is 90° out of phase from the ESR ripple, and the two numbers do not add directly. However, this calculation provides a practical minimum value for C2 based on its ESR and the target spec. To allow for the capacitor's tolerance, temperature effects, and voltage effects, a 15-µF, X7R capacitor is used.

c. **In summary:** The above calculations provide a minimum value for C2 and a calculation for R3. The ESR is just as important as the capacitance. The calculated values are guidelines, and should be treated as starting points. For each application, experimentation is needed to determine the optimum values for R3 and C2.

$$C = I \times \Delta t / \Delta V \tag{9}$$

R_{CL}: When a current limit condition is detected, the minimum off-time set by this resistor must be greater than the maximum normal off-time which occurs at maximum V_{IN}. Using Equation 4, the minimum on-time is 0.47 µs, yielding a maximum off-time of 3.99 µs. This is increased by 117 ns (to 4.11 µs) due to a ±25% tolerance of the on-time. This value is then increased to allow for:

The response time of the current limit detection loop (400 ns).

The off-time determined by Equation 5 has a ±25% tolerance.

$$t_{OFFCL(MIN)} = (4.11\ \mu s + 0.40\ \mu s) \times 1.25 = 5.64\ \mu s \tag{10}$$

Using Equation 5, R_{CL} calculates to 264 kΩ (at V_{FB} = 2.5 V). The closest standard value is 267 kΩ.

D1: The important parameters are reverse recovery time and forward voltage. The reverse recovery time determines how long the reverse current surge lasts each time the buck switch is turned on. The forward voltage drop is significant in the event the output is short-circuited as it is only this diode's voltage which forces the inductor current to reduce during the forced off-time. For this reason, a higher voltage is better, although that affects efficiency. A good choice is an ultra-fast power diode, such as the MURA110T3 from ON Semiconductor. Its reverse recovery time is 30 ns, and its forward voltage drop is approximately 0.72 V at 300 mA at 25°C. Other types of diodes may have a lower forward voltage drop, but may have longer recovery times, or greater reverse leakage. D1's reverse voltage rating must be at least as great as the maximum V_{IN}, and its current rating be greater than the maximum current limit threshold (610 mA).

C1: This capacitor's purpose is to supply most of the switch current during the on-time, and limit the voltage ripple at V_{IN}, on the assumption that the voltage source feeding V_{IN} has an output impedance greater than zero. At maximum load current when the buck switch turns on, the current into pin 8 will suddenly increase to the lower peak of the output current waveform, ramp up to the peak value, then drop to zero at turnoff. The average input current during this on-time is the load current (300 mA). For a worst case calculation, C1 must supply this average load current during the maximum on-time. To keep the input voltage ripple to less than 2 V (for this exercise), C1 is calculated with Equation 11.

$$C1 = \frac{I \times t_{ON}}{\Delta V} = \frac{0.3A \times 3.72\ \mu s}{2.0V} = 0.56\ \mu F \tag{11}$$

Quality ceramic capacitors in this value have a low ESR which adds only a few millivolts to the ripple. It is the capacitance which is dominant in this case. To allow for the capacitor's tolerance, temperature effects, and voltage effects, a 1.0-µF, 100-V, X7R capacitor will be used.

C4: The recommended value is 0.01 µF for C4, as this is appropriate in the majority of applications. A high-quality ceramic capacitor, with low ESR is recommended as C4 supplies the surge current to charge the buck switch gate at turnon. A low ESR also ensures a quick recharge during each off-time. At minimum V_{IN}, when the on-time is at maximum, it is possible during start-up that C4 will not fully recharge during each 300-ns off-time. The circuit will not be able to complete the start-up, and achieve output regulation. This can occur when the frequency is intended to be low (for example, R_{ON} = 500 K). In this case C4 should be increased so it can maintain sufficient voltage across the buck switch driver during each on-time.

C5: This capacitor helps avoid supply voltage transients and ringing due to long lead inductance at V_{IN}. A low-ESR, 0.1-µF ceramic chip capacitor is recommended, placed close to the LM5008.

8.2.3 Application Curves

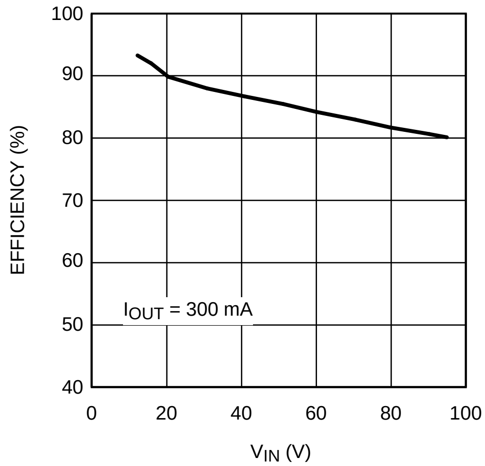

Figure 12. Efficiency vs V_{IN}

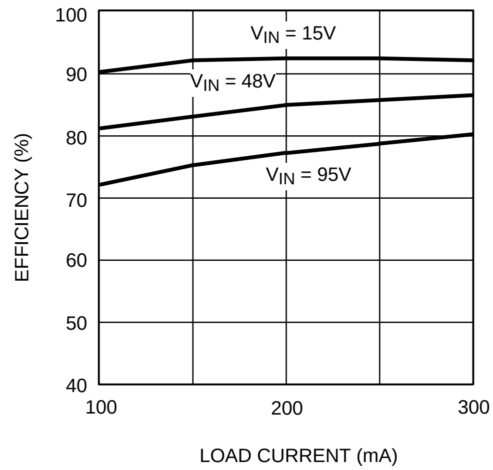

Figure 13. Efficiency vs Load Current vs V_{IN}

9 Power Supply Recommendations

The LM5008 converter is designed to operate from a wide input voltage range from 9.5 V to 95 V. The characteristics of the input supply must be compatible with the *Absolute Maximum Ratings* and *Recommended Operating Conditions*. In addition, the input supply must be capable of delivering the required input current to the fully-loaded regulator. Estimate the average input current with Equation 12.

$$I_{IN} = \frac{V_{OUT} \cdot I_{OUT}}{V_{IN} \cdot \eta}$$

where

- η is the efficiency (12)

If the converter is connected to an input supply through long wires or PCB traces with large impedance, sachieving stable performance requires special care. The parasitic inductance and resistance of the input cables may have an adverse affect on converter operation. The parasitic inductance in combination with the low-ESR ceramic input capacitors form an underdamped resonant circuit. This circuit can cause overvoltage transients at VIN each time the input supply is cycled ON and OFF. The parasitic resistance causes the input voltage to dip during a load transient. If the regulator is operating close to the minimum input voltage, this dip can cause false UVLO fault triggering and a system reset. The best way to solve such issues is to reduce the distance from the input supply to the regulator and use an aluminum or tantalum input capacitor in parallel with the ceramics. The moderate ESR of the electrolytic capacitors helps to damp the input resonant circuit and reduce any voltage overshoots. A capacitance in the range of 10 µF to 47 µF is usually sufficient to provide input damping and helps to hold the input voltage steady during large load transients.

An EMI input filter is often used in front of the regulator that, unless carefully designed, can lead to instability as well as some of the effects mentioned above. The user's guide *Simple Success with Conducted EMI for DC-DC Converters* (SNVA489) provides helpful suggestions when designing an input filter for any switching regulator.

10 Layout

10.1 Layout Guidelines

The LM5008 regulation and overvoltage comparators are very fast, and as such responds to short-duration noise pulses. Layout considerations are therefore critical for optimum performance:

1. Minimize the area of the high di/dt switching current loop consisting of the VIN pin, input ceramic capacitor, SW node and freewheeling power diode. Keep the input capacitor as close as possible to the VIN pin and route a short, direct connection to the RTN pin using polygon copper pours.
2. Minimize SW copper area to reduce radiated noise related to high dv/dt.
3. Locate all components as physically close as possible to their respective pins, thereby minimizing noise pickup in the printed-circuit tracks.
4. Locate the FB trace away from noise sources and inductors. Place the resistor close to the FB pin to minimize the length of the FB trace.

If the internal dissipation of the LM5008 converter produces excessive junction temperatures during normal operation, optimal use of the PCB ground plane can help considerably to dissipate heat. The exposed pad on the bottom of the WSON-8 package can be soldered to a ground plane on the PCB, and that plane should extend out from beneath the IC to help dissipate the heat. Additionally, the use of wide PCB traces for power connection can also help conduct heat away from the IC. Judicious positioning of the LM5008 converter within the end product, along with use of any available air flow (forced or natural convection), can help reduce the operating junction temperature.

10.2 Layout Examples

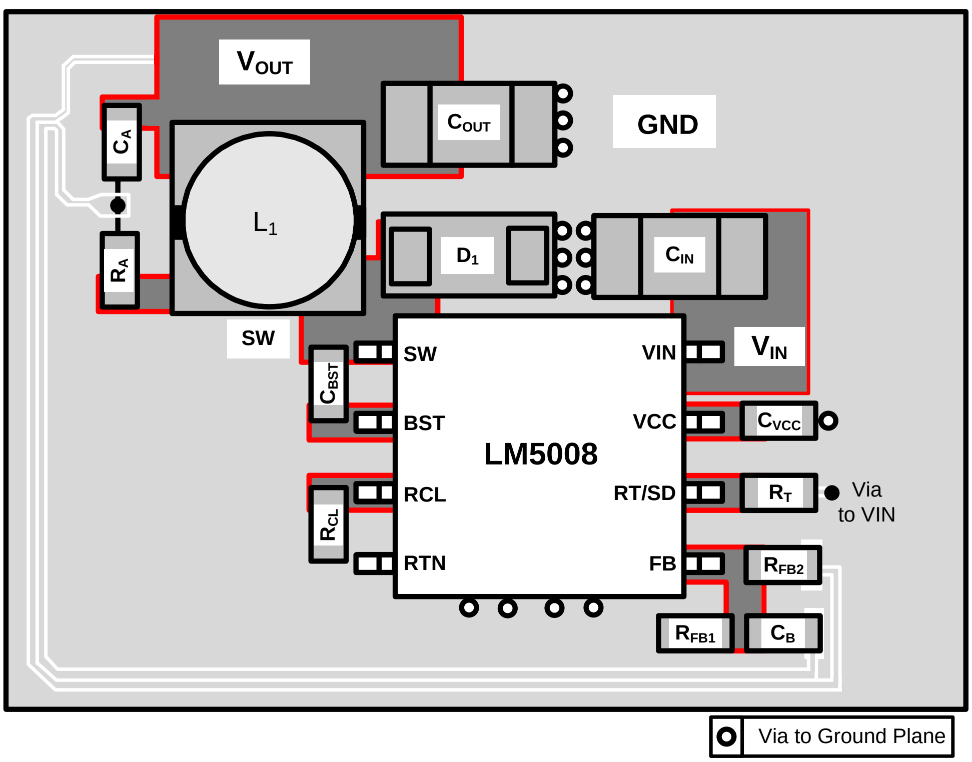

Figure 14. LM5008 Evaluation Board Top Layer

11 デバイスおよびドキュメントのサポート

11.1 デバイス・サポート

11.1.1 デベロッパー・ネットワークの製品に関する免責事項

デベロッパー・ネットワークの製品またはサービスに関するTIの出版物は、単独またはTIの製品、サービスと一緒に提供される場合に関係なく、デベロッパー・ネットワークの製品またはサービスの適合性に関する是認、デベロッパー・ネットワークの製品またはサービスの是認の表明を意味するものではありません。

11.1.2 WEBENCH®ツールによるカスタム設計

ここをクリックすると、WEBENCH® Power Designerにより、LM5008を使用するカスタム設計を作成できます。

1. 最初に、入力電圧(V_{IN})、出力電圧(V_{OUT})、出力電流(I_{OUT})の要件を入力します。
2. オプティマイザのダイヤルを使用して、効率、占有面積、コストなどの主要なパラメータについて設計を最適化します。
3. 生成された設計を、テキサス・インスツルメンツが提供する他の方式と比較します。

WEBENCH Power Designerでは、カスタマイズされた回路図と部品リストを、リアルタイムの価格と部品の在庫情報と併せて参照できます。

通常、次の操作を実行可能です。

- 電気的なシミュレーションを実行し、重要な波形と回路の性能を確認する。
- 熱シミュレーションを実行し、基板の熱特性を把握する。
- カスタマイズされた回路図やレイアウトを、一般的なCADフォーマットで出力する。
- 設計のレポートをPDFで印刷し、設計を共有する。

WEBENCHツールの詳細は、www.ti.com/WEBENCHでご覧になれます。

11.1.3 開発サポート

開発サポートについては、以下を参照してください。

- TIのリファレンス・デザイン・ライブラリについては、TI Designsを参照してください。
- TIのWEBENCH設計環境については、WEBENCH®設計センターを参照してください。

11.2 ドキュメントのサポート

11.2.1 関連資料

関連資料については、以下を参照してください。

- *LM5008クイック・スタート・カリキュレータ*
- *『AN-1330 LM5008評価ボード』*(SNVA380)
- *『AN-1925 LM5008A評価ボード』*(SNVA380)
- *『広い入力/出力電圧差動用の降圧レギュレータ・トポロジ』*(SNVA594)

11.2.1.1 PCBレイアウトについてのリソース

- *『AN-1149 スイッチング電源のレイアウトのガイドライン』*(SNVA021)
- *『AN-1229 Simple Switcher PCBレイアウト・ガイドライン』*(SNVA054)
- *『独自電源の構築 - レイアウトの考慮事項』*(SLUP230)
- *『LM4360xおよびLM4600xによる低放射EMIレイアウトの簡単な作成』*(SNVA721)
- *『AN-2162 DC/DCコンバータから伝導されるEMIでの簡単な成功』*(SNVA489)
- *『誘導性寄生の最小化による降圧コンバータのEMIおよび電圧ストレスの低減』*(SLYT682)
- ホワイト・ペーパー
  - *『コスト効率の優れた、要求の厳しいアプリケーション用の広V_{IN}、低EMIの同期整流降圧回路の評価』*
  - *『電源の伝導EMI仕様の概要』*
  - *『電源の放射EMI仕様の概要』*

ドキュメントのサポート (continued)

11.2.1.2 熱設計についてのリソース

- *『AN-2020 システムの基本設計に応じた熱設計』*(SNVA419)
- *『AN-1520 露出パッド・パッケージで最良の熱抵抗を実現するための基板レイアウト・ガイド』*(SNVA183)
- *『半導体とICパッケージの熱指標』*(SPRA953)
- *『LM43603およびLM43602による簡単な熱設計』*(SNVA719)
- *『放熱特性の優れたPowerPAD™パッケージ』*(SLMA002)
- *『PowerPADの簡単な使用法』*(SLMA004)
- *『新しい熱測定基準の使用』*(SBVA025)
- Power Houseブログ
  - *『DC/DCコンバータの高密度PCBレイアウト』*

11.3 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、ti.comのデバイス製品フォルダを開いてください。右上の隅にある「*通知を受け取る*」をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

11.4 コミュニティ・リソース

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™オンライン・コミュニティ ***TIのE2E（Engineer-to-Engineer）コミュニティ。*** エンジニア間の共同作業を促進するために開設されたものです。e2e.ti.comでは、他のエンジニアに質問し、知識を共有し、アイディアを検討して、問題解決に役立てることができます。

設計サポート ***TIの設計サポート*** 役に立つE2Eフォーラムや、設計サポート・ツールをすばやく見つけることができます。技術サポート用の連絡先情報も参照できます。

11.5 商標

PowerPAD, E2E are trademarks of Texas Instruments.
WEBENCH is a registered trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.6 静電気放電に関する注意事項

これらのデバイスは、限定的なESD（静電破壊）保護機能を内 蔵しています。保存時または取り扱い時は、MOSゲートに対す る静電破壊を防止するために、リード線同士をショートさせて おくか、デバイスを導電フォームに入れる必要があります。

11.7 Glossary

SLYZ022 — *TI Glossary*.
This glossary lists and explains terms, acronyms, and definitions.

12 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。この情報は、そのデバイスについて利用可能な最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LM5008MM/NOPB	Active	Production	VSSOP (DGK) | 8	1000 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	SAYB
LM5008MM/NOPB.A	Active	Production	VSSOP (DGK) | 8	1000 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	SAYB
LM5008MM/NOPB.B	Active	Production	VSSOP (DGK) | 8	1000 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	SAYB
LM5008MMX/NOPB	Active	Production	VSSOP (DGK) | 8	3500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	SAYB
LM5008MMX/NOPB.A	Active	Production	VSSOP (DGK) | 8	3500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	SAYB
LM5008MMX/NOPB.B	Active	Production	VSSOP (DGK) | 8	3500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	SAYB
LM5008SDC/NOPB	Active	Production	WSON (NGU) | 8	1000 | SMALL T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	L5008SD
LM5008SDC/NOPB.A	Active	Production	WSON (NGU) | 8	1000 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	L5008SD
LM5008SDC/NOPB.B	Active	Production	WSON (NGU) | 8	1000 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	L5008SD
LM5008SDCX/NOPB	Active	Production	WSON (NGU) | 8	4500 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	L5008SD
LM5008SDCX/NOPB.A	Active	Production	WSON (NGU) | 8	4500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	L5008SD
LM5008SDCX/NOPB.B	Active	Production	WSON (NGU) | 8	4500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	L5008SD

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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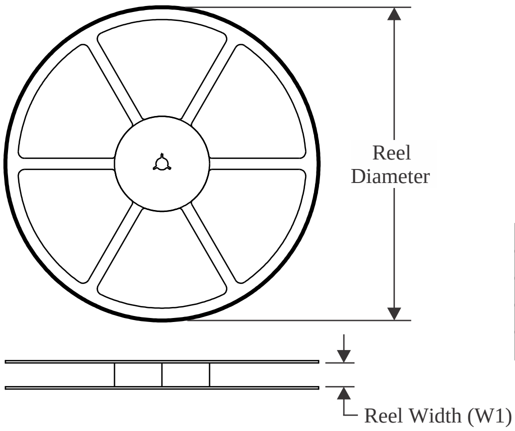
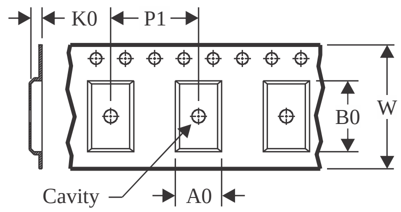
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

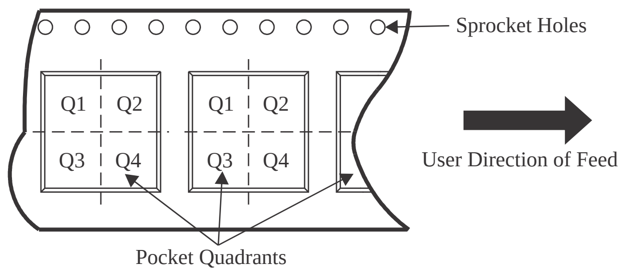


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

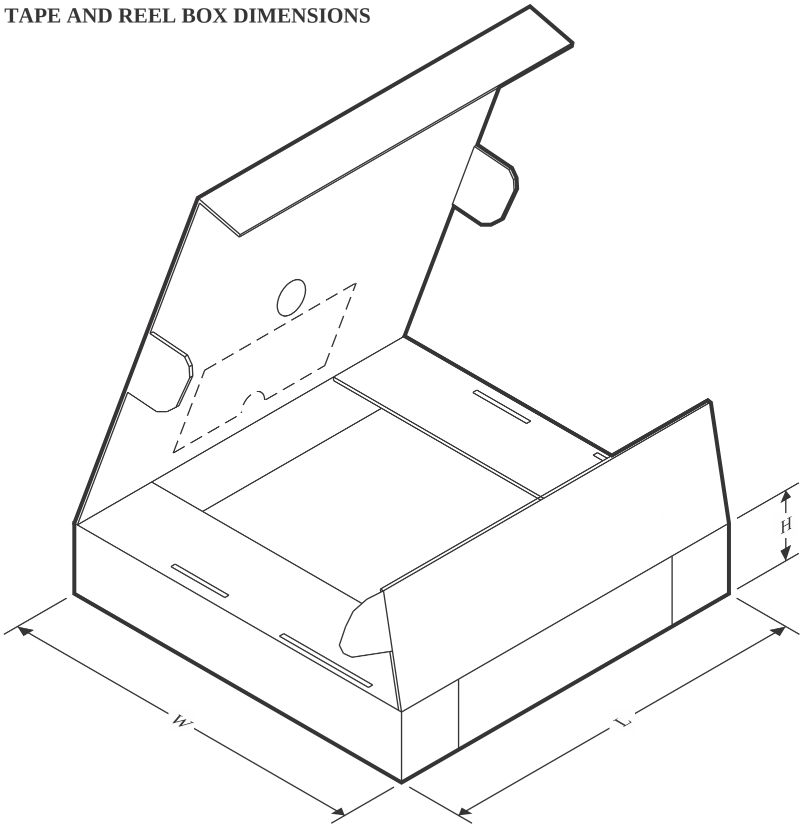
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

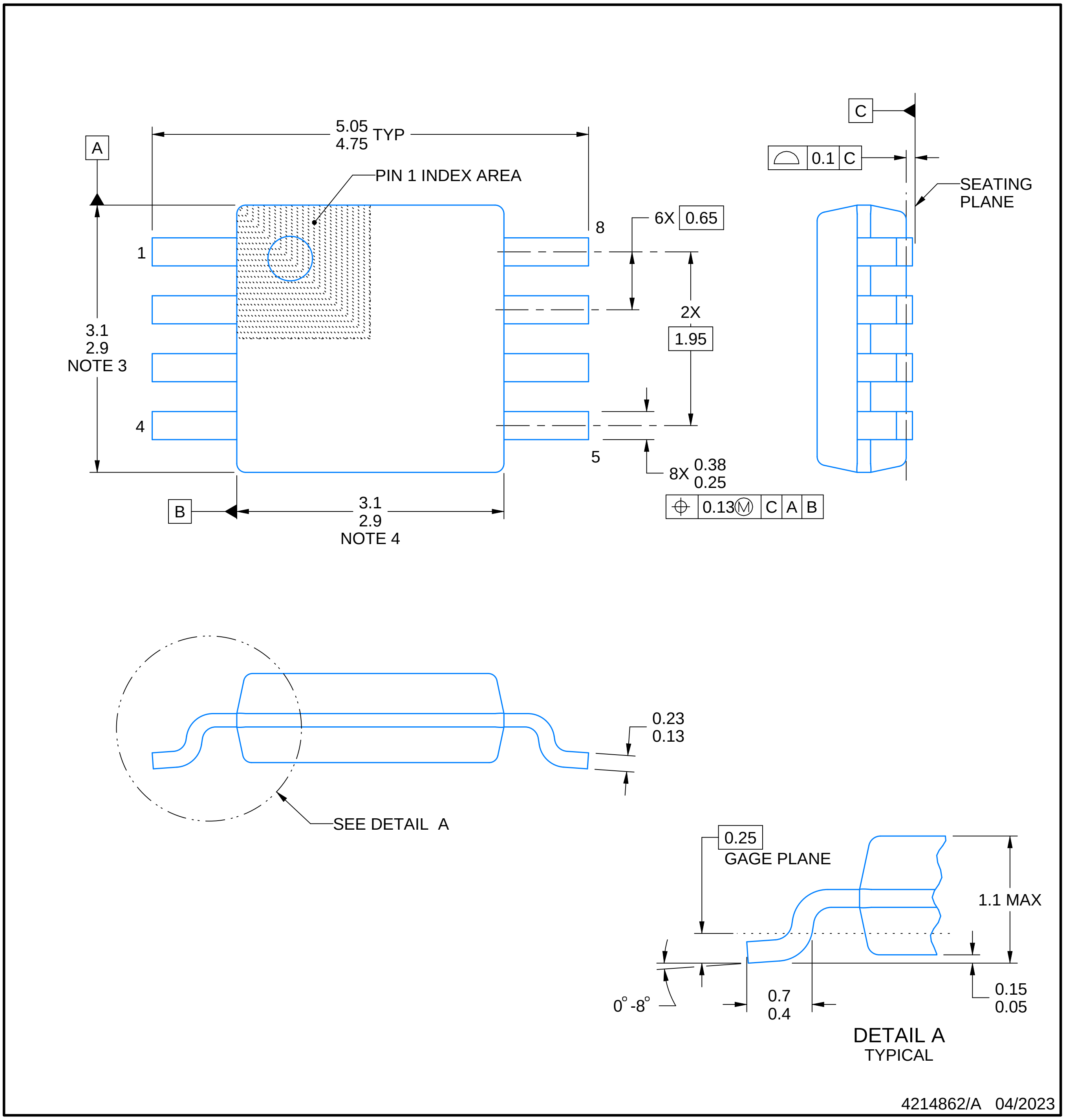
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM5008MM/NOPB	VSSOP	DGK	8	1000	177.8	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM5008MM/NOPB	VSSOP	DGK	8	1000	330.0	12.4	5.25	3.35	1.25	8.0	12.0	Q1
LM5008MMX/NOPB	VSSOP	DGK	8	3500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM5008SDC/NOPB	WSON	NGU	8	1000	177.8	12.4	4.3	4.3	1.3	8.0	12.0	Q1
LM5008SDCX/NOPB	WSON	NGU	8	4500	330.0	12.4	4.3	4.3	1.3	8.0	12.0	Q1
LM5008SDCX/NOPB	WSON	NGU	8	4500	330.0	12.4	4.3	4.3	1.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

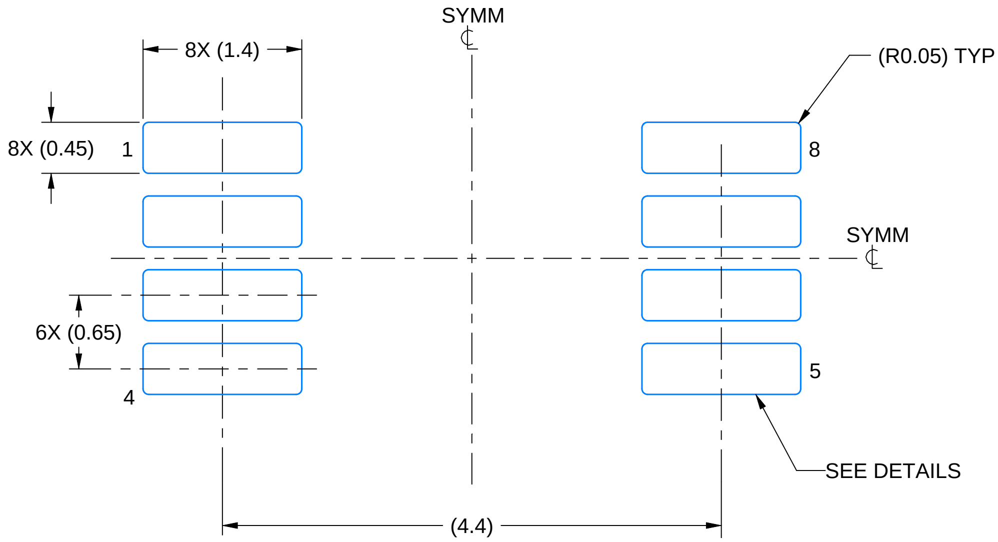
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM5008MM/NOPB	VSSOP	DGK	8	1000	208.0	191.0	35.0
LM5008MM/NOPB	VSSOP	DGK	8	1000	366.0	364.0	50.0
LM5008MMX/NOPB	VSSOP	DGK	8	3500	367.0	367.0	35.0
LM5008SDC/NOPB	WSON	NGU	8	1000	208.0	191.0	35.0
LM5008SDCX/NOPB	WSON	NGU	8	4500	367.0	367.0	35.0
LM5008SDCX/NOPB	WSON	NGU	8	4500	346.0	346.0	35.0



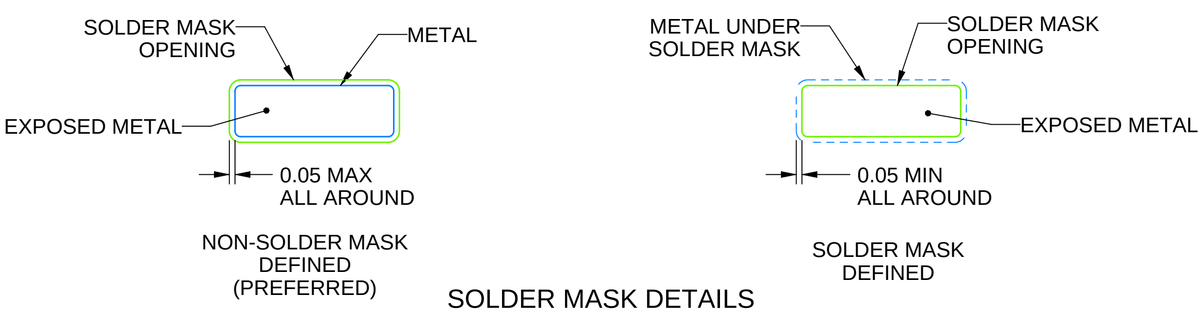
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X

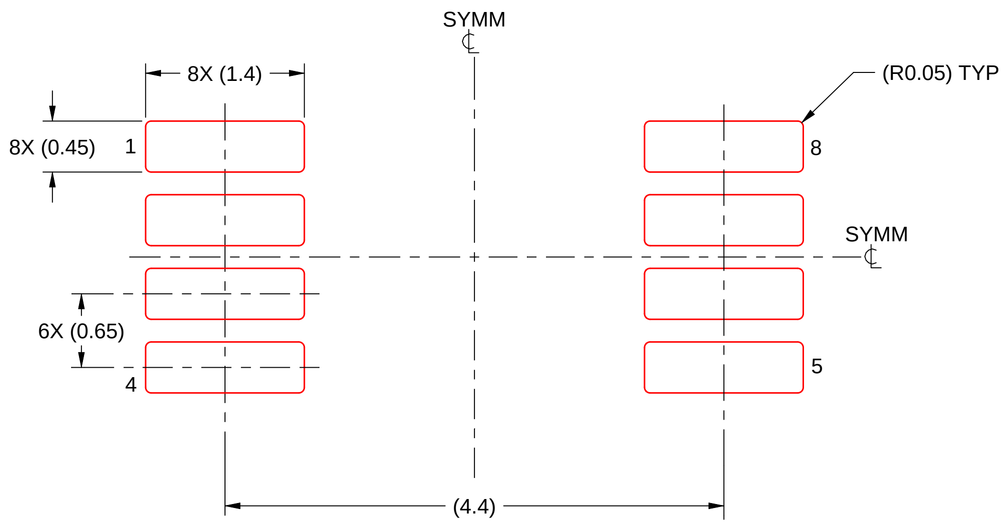


SOLDER MASK DETAILS

4214862/A 04/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.

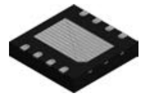


SOLDER PASTE EXAMPLE
SCALE: 15X

4214862/A 04/2023

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

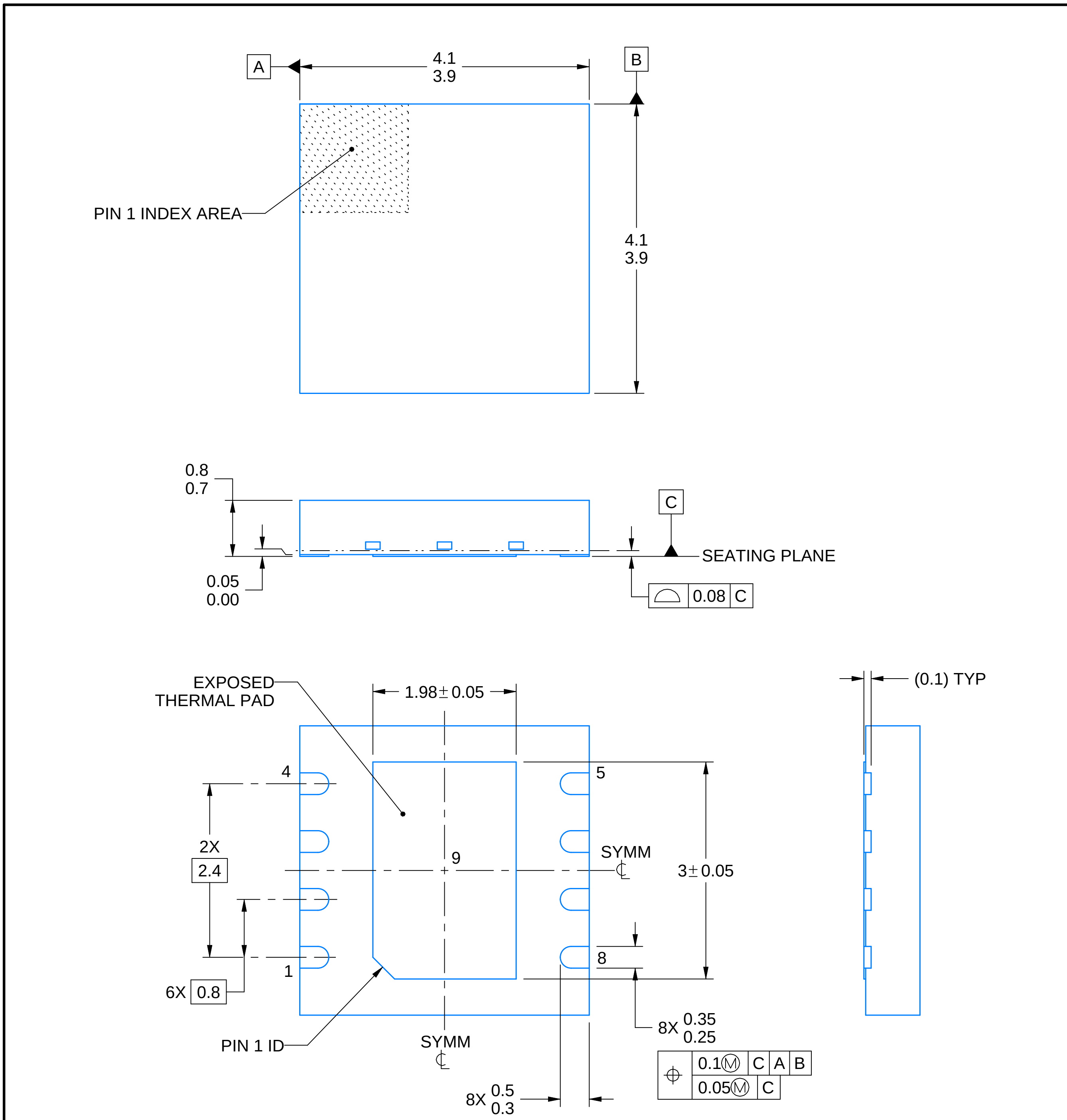


PACKAGE OUTLINE

NGU0008B

WSON - 0.8 mm max height

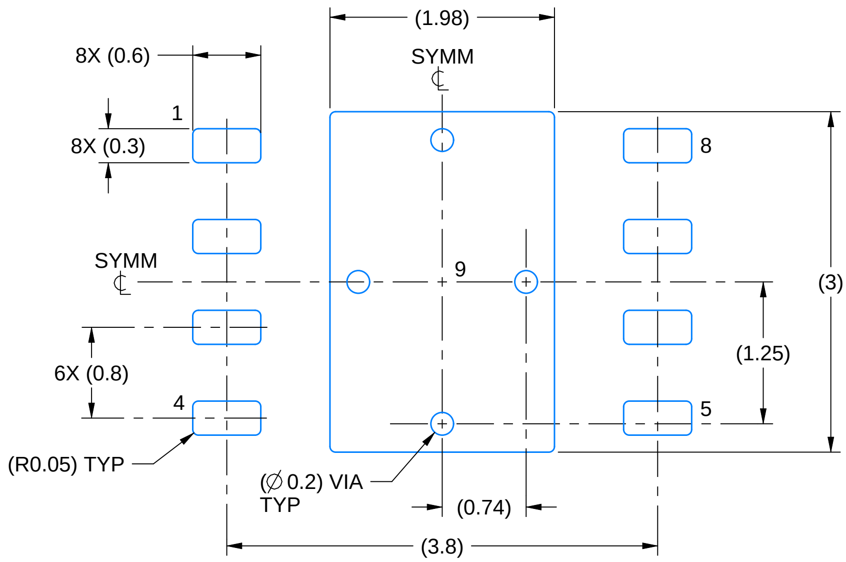
PLASTIC SMALL OUTLINE - NO LEAD



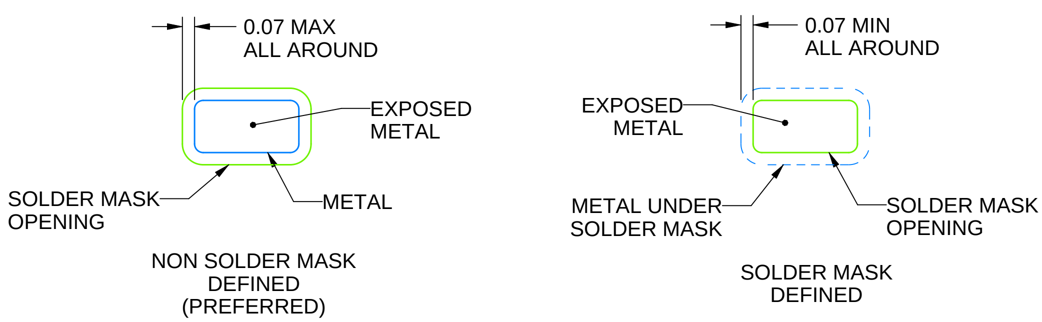
4214936/A 12/2023

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

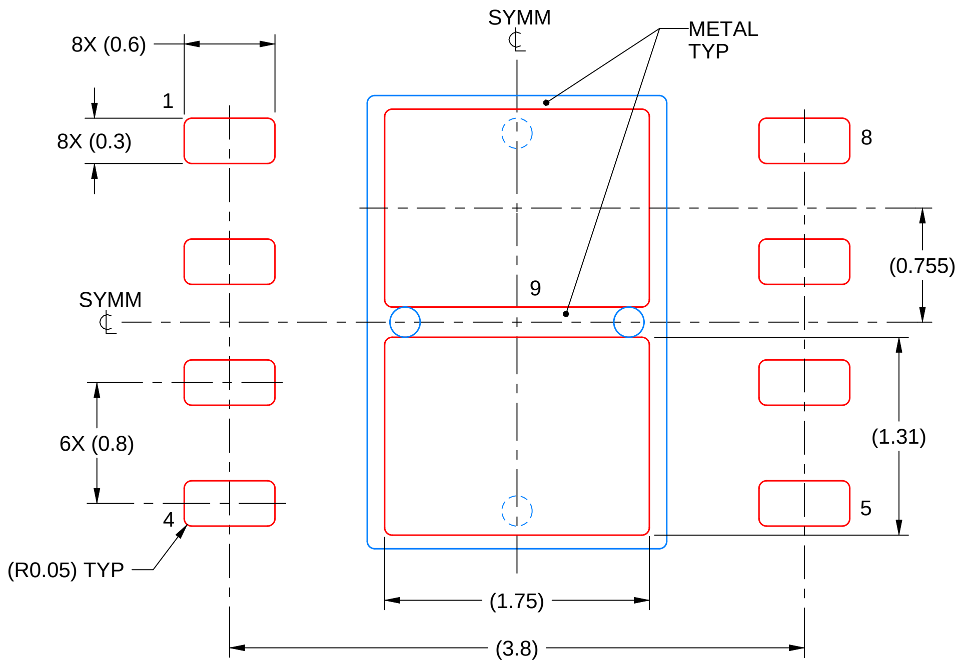


SOLDER MASK DETAILS

4214936/A 12/2023

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 9:
77% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

4214936/A 12/2023

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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