LM5010A, LM5010A-Q1高電圧1A降圧スイッチング・レギュレータ

1 特長

- LM5010A-Q1は、車載アプリケーション向けに認定
- 次の結果でAEC-Q100認定:
  - デバイス温度グレード1: 動作時周囲温度範囲 -40℃～125℃
  - デバイス温度グレード 0: 動作時周囲温度範囲 –40℃～150℃
  - デバイスHBM ESD分類レベル2
  - デバイスCDM ESD分類レベルC5
- 6V～75Vの広い入力電圧範囲
- バレー電流制限1.25A
- スイッチング周波数を最大1MHzまでプログラム可能
- 80VのNチャネル降圧スイッチを内蔵
- 高電圧バイアス・レギュレータを内蔵
- ループ補償が不要
- 超高速の過渡応答
- 入力電圧や負荷の変動に対して動作周波数をほぼ一定に維持
- 可変出力電圧
- 2.5V、±2%のフィードバック・リファレンス電圧源
- ソフトスタートをプログラム可能
- サーマル・シャットダウン
- 放熱特性向上のための露出型熱放散パッド

2 アプリケーション

- 通信機器向けの非絶縁型レギュレータ
- 二次側ポスト・レギュレータ
- 車載用電子機器

3 概要

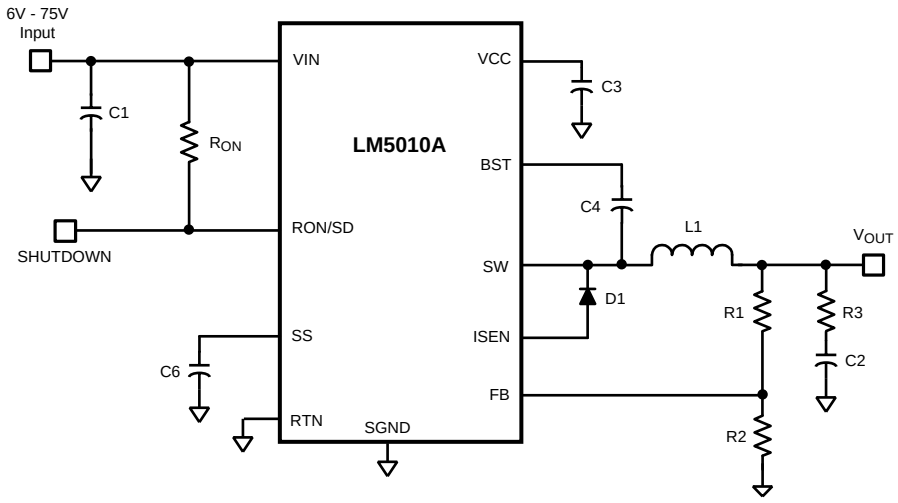
LM5010Ax降圧スイッチング・レギュレータは、LM5010の拡張版で、入力動作範囲が最小6Vに拡張されています。LM5010Axには、1Aを超える負荷電流を供給できる低コストで高効率の降圧レギュレータを実装するため必要な、すべての機能が搭載されています。この高電圧レギュレータはNチャネル降圧スイッチを内蔵し、放熱特性の優れた10ピンWSONパッケージおよび14ピンHTSSOPパッケージで供給されます。コンスタント・オン・タイム制御方式ではループ補償が必要ないため、負荷過渡応答が高速になり、回路の実装が簡単になります。入力電圧とオン時間は反比例の関係にあるため、ラインや負荷が変動しても、動作周波数は一定に保たれます。バレー電流制限の検出は1.25Aに設定されています。追加機能として、VCC低電圧誤動作防止、サーマル・シャットダウン、ゲート駆動低電圧誤動作防止、最大デューティ・サイクル制限機能があります。

製品情報(1)

型番	パッケージ	本体サイズ(公称)
LM5010Ax	WSON (10)	4.00mm×4.00mm
	HTSSOP (14)	4.40mm×5.00mm

(1) 提供されているすべてのパッケージについては、データシートの末尾にある注文情報を参照してください。

基本的な降圧レギュレータ



Copyright © 2016, Texas Instruments Incorporated

英語版のTI製品についての情報を翻訳したこの資料は、製品の概要を確認する目的で便宜的に提供しているものです。該当する正式な英語版の最新情報は、www.ti.comで閲覧でき、その内容が常に優先されます。TIでは翻訳の正確性および妥当性につきましては一切保証いたしません。実際の設計などの前には、必ず最新版の英語版をご参照くださいますようお願いいたします。

目次

1 特長 ... 1
2 アプリケーション ... 1
3 概要 ... 1
4 改訂履歴 ... 2
5 **Pin Configuration and Functions** ... 3
6 **Specifications** ... 4
6.1 Absolute Maximum Ratings ... 4
6.2 ESD Ratings: LM5010A ... 4
6.3 ESD Ratings: LM5010A-Q1, LM5010-Q0 ... 4
6.4 Recommended Operating Conditions ... 4
6.5 Thermal Information ... 5
6.6 Electrical Characteristics ... 5
6.7 Switching Characteristics ... 6
6.8 Typical Characteristics ... 8
7 **Detailed Description** ... 9
7.1 Overview ... 9
7.2 Functional Block Diagram ... 9
7.3 Feature Description ... 9
7.4 Device Functional Modes ... 13
8 **Application and Implementation** ... 14
8.1 Application Information ... 14
8.2 Typical Application ... 14
8.3 Do's and Don'ts ... 20
9 **Power Supply Recommendations** ... 21
10 **Layout** ... 21
10.1 Layout Guidelines ... 21
10.2 Layout Example ... 22
11 デバイスおよびドキュメントのサポート ... 23
11.1 関連リンク ... 23
11.2 コミュニティ・リソース ... 23
11.3 商標 ... 23
11.4 静電気放電に関する注意事項 ... 23
11.5 Glossary ... 23
12 メカニカル、パッケージ、および注文情報 ... 23

4 改訂履歴

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Revision E (February 2013) から **Revision F** に変更 **Page**

- 「*ESD定格*」の表、「*機能概要*」セクション、「*デバイスの機能モード*」セクション、「*アプリケーションと実装*」セクション、「*電源に関する推奨事項*」セクション、「*レイアウト*」セクション、「*デバイスおよびドキュメントのサポート*」セクション、「*メカニカル、パッケージ、および注文情報*」セクションを追加 ... 1

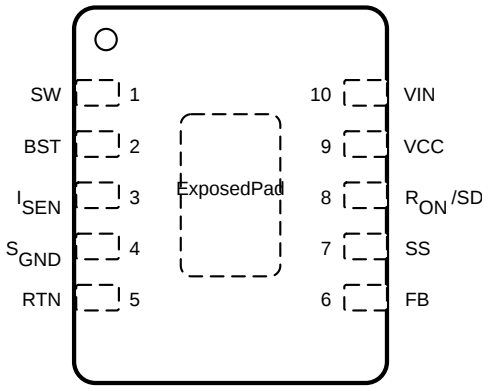
Revision D (February 2013) から **Revision E** に変更 **Page**

- ナショナル セミコンダクターのデータシートのレイアウトをTIフォーマットへ 変更 ... 1

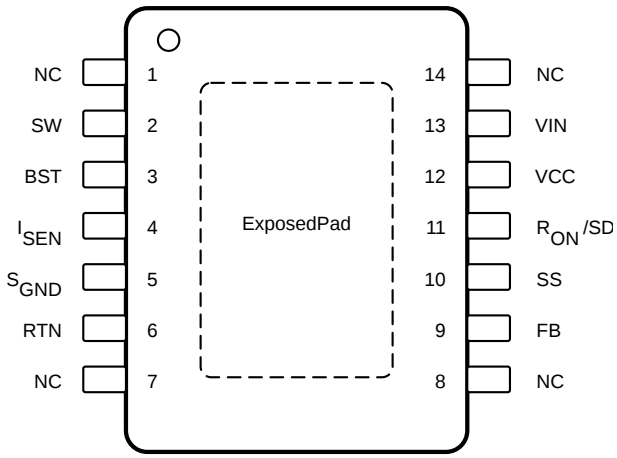
Copyright © 2005–2016, Texas Instruments Incorporated

5 Pin Configuration and Functions

DPR Package
10-Pin WSON
Top View



PWP Package
14-Pin HTSSOP
Top View



Pin Functions

PIN			I/O	DESCRIPTION
NAME	WSON	HTSSOP		
BST	2	3	I	Boost pin for bootstrap capacitor: Connect a capacitor from SW to the BST pin. The capacitor is charged from VCC through an internal diode during the buck switch OFF-time.
EP	—	—	—	Exposed pad
FB	6	9	I	Voltage feedback input from the regulated output: Input to both the regulation and overvoltage comparators. The FB pin regulation level is 2.5 V.
I_{SEN}	3	4	I	Current sense: During the buck switch OFF-time, the inductor current flows through the internal sense resistor, and out of the ISEN pin to the free-wheeling diode. The current limit comparator keeps the buck switch off if the ISEN current exceeds 1.25 A (typical).
NC	—	1, 7, 8, 14	—	No connection. Can be connected to ground plane to improve heat dissipation.
R_{ON}/SD	8	11	I	ON-time control and shutdown: An external resistor from VIN to this pin sets the buck switch ON-time. Grounding this pin shuts down the regulator.
RTN	5	6	—	Circuit ground: Ground return for all internal circuitry other than the current sense resistor.
S_{GND}	4	5	—	Sense ground: Recirculating current flows into this pin to the current sense resistor.
SS	7	10	I	Soft start: An internal 11.5-µA current source charges the SS pin capacitor to 2.5 V to softstart the reference input of the regulation comparator.
SW	1	2	O	Switching node: Internally connected to the buck switch source. Connect to the inductor, free-wheeling diode, and bootstrap capacitor.
VCC	9	12	I	Output of the bias regulator: The voltage at VCC is nominally equal to V_{IN} for V_{IN} < 8.9 V, and regulated at 7 V for V_{IN} > 8.9 V. Connect a 0.47-µF, or larger capacitor from VCC to ground, as close as possible to the pins. An external voltage can be applied to this pin to reduce internal dissipation if V_{IN} is greater than 8.9 V. MOSFET body diodes clamp VCC to V_{IN} if V_{CC} > V_{IN}.
VIN	10	13	I	Input supply: Nominal input range is 6 V to 75 V. Input bypass capacitors should be located as close as possible to the VIN pin and RTN pin.

Copyright © 2005–2016, Texas Instruments Incorporated

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

	MIN	MAX	UNIT
VIN	6	75	V
VIN to RTN	–0.3	76	V
BST to RTN	–0.3	90	V
SW to RTN (steady state)		–1.5	V
BST to VCC		76	V
BST to SW		14	V
VCC to RTN	–0.3	14	V
S_{GND} to RTN	–0.3	0.3	V
SS to RTN	–0.3	4	V
VIN to SW		76	V
All other inputs to RTN	–0.3	7	V
Lead temperature (soldering, 4 sec)(2)		260	°C
Junction temperature (LM5010A, Q1,Q0)	–40	150	°C
Storage temperature, T_{stg}	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* . Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) For detailed information on soldering plastic HTSSOP and WSON packages, see *メカニカル、パッケージ、および注文情報*.

6.2 ESD Ratings: LM5010A

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±750	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 ESD Ratings: LM5010A-Q1, LM5010-Q0

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002(1)(2)	±2000	V
		Charged-device model (CDM), per AEC Q100-011(3)	±750	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.
(2) Level listed above is the passing level per ANSI/ESDA/JEDEC JS-001. JEDEC document JEP155 states that 500 V HBM allows safe manufacturing with a standard ESD control process.
(3) Level listed above is the passing level per EIA-JEDEC JESD22-C101. JEDEC document JEP157 states that 250 V CDM allows safe manufacturing with a standard ESD control process.

6.4 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_{IN}	Input voltage		6		75	V
I_O	Output current				1	A
Ext-V_{CC}	External bias voltage(1)		8		13	V
T_J	Operating junction temperature	LM5010A	–40		125	°C
		LM5010A-Q1, LM5010-Q0	–40		150	°C

(1) V_{CC} provides bias for the internal gate drive and control circuits. Device thermal limitations limit external loading.

Copyright © 2005–2016, Texas Instruments Incorporated

6.5 Thermal Information

THERMAL METRIC(1)		LM5010A, LM5010A-Q1		UNIT
		DPR (WSON)	PWP (HTSSOP)	
		10 PINS	14 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	36	41.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	31.9	26.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	13.2	22.5	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.3	0.7	°C/W
ψ_{JB}	Junction-to-board characterization parameter	13.5	22.2	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	3	3.3	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.6 Electrical Characteristics

Typical values correspond to T_J = 25°C, minimum and maximum limits apply over T_J = –40°C to 125°C, V_{IN} = 48 V, and R_{ON} = 200 kΩ (unless otherwise noted).(1)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{CC} REGULATOR						
V_{CC}Reg	VCC regulated output		6.6	7	7.4	V
	V_{IN} - V_{CC}	I_{CC} = 0 mA, F_S < 200 kHz, 6 V ≤ V_{IN} ≤ 8.5 V		100		mV
	V_{CC} Bypass threshold	V_{IN} increasing		8.9		V
	V_{CC} Bypass hysteresis	V_{IN} decreasing		260		mV
	V_{CC} Output impedance (0 mA ≤ I_{CC} ≤ 5 mA)	V_{IN} = 6 V		55		Ω
		V_{IN} = 8 V		50		
		V_{IN} = 48 V		0.21		
	V_{CC} Current limit	V_{IN} = 48 V, V_{CC} = 0 V		15		mA
$UVLO_{VCC}$	V_{CC} undervoltage lockout threshold	V_{CC} increasing		5.25		V
	$UVLO_{VCC}$ hysteresis	V_{CC} decreasing		180		mV
	$UVLO_{VCC}$ filter delay	100 mV overdrive		3		µs
	I_{IN} Operating current	Non-switching, FB = 3 V		675	950	µA
	I_{IN} Shutdown current	R_{ON}/SD = 0 V		100	200	µA
SOFT-START PIN						
I_{SS}	Internal current source		8	11.5	15	µA
CURRENT LIMIT						
I_{LIM}	Threshold	Current out of I_{SEN}	1	1.25	1.5	A
	Resistance from I_{SEN} to S_{GND}			130		mΩ
	Response time			150		ns
ON TIMER, R_{ON}/SD PIN						
	Shutdown threshold	Voltage at R_{ON}/SD rising	0.3	0.7	1.05	V
	Threshold hysteresis			40		mV
REGULATION AND OVER-VOLTAGE COMPARATORS (FB PIN)						
V_{REF}	FB regulation threshold	T_J ≤ 125°C	2.445	2.5	2.55	V
		T_J ≤ 150°C, over full operating junction temperature range	2.435			
			2.44			
	FB overvoltage threshold			2.9		V
	FB bias current			1		nA

(1) All minimum and maximum limits are specified by correlating the electrical characteristics to process and temperature variations and applying statistical process control.

Copyright © 2005–2016, Texas Instruments Incorporated

Electrical Characteristics (continued)

Typical values correspond to T_J = 25°C, minimum and maximum limits apply over T_J = –40°C to 125°C, V_{IN} = 48 V, and R_{ON} = 200 kΩ (unless otherwise noted).(1)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
THERMAL SHUTDOWN						
T_{SD}	Thermal shutdown temperature			175		°C
	Thermal shutdown hysteresis			20		°C

6.7 Switching Characteristics

Typical values correspond to T_J = 25°C, minimum and maximum limits apply over T_J = –40°C to 125°C, and V_{IN} = 48 V (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$R_{DS(ON)}$	Buck switch	I_{SW} = 200 mA	$T_J \le 125°C$		0.35	0.8	Ω
			$T_J \le 150°C$, over full operating junction temperature range			0.85	
$UVLO_{GD}$	Gate drive UVLO	V_{BST} - V_{SW} increasing		1.7	3	4	V
	$UVLO_{GD}$ Hysteresis				400		mV
OFF TIMER							
t_{OFF}	Minimum OFF-time				260		ns
ON TIMER							
t_{ON} - 1	ON-time	V_{IN} = 10 V, R_{ON} = 200 kΩ		2.1	2.75	3.4	µs
t_{ON} - 2	ON-time	V_{IN} = 75 V, R_{ON} = 200 kΩ		290	390	496	ns

(1) All minimum and maximum limits are specified by correlating the electrical characteristics to process and temperature variations while applying statistical process control.

Copyright © 2005–2016, Texas Instruments Incorporated

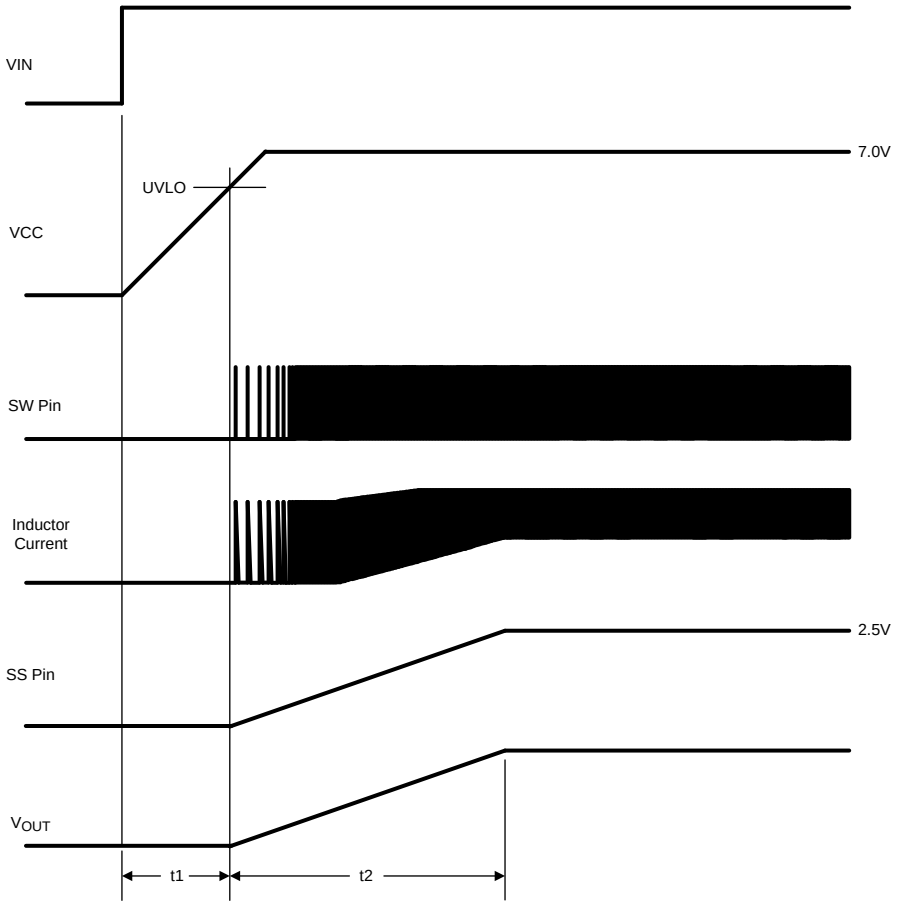


Figure 1. Start-Up Sequence

Copyright © 2005–2016, Texas Instruments Incorporated

6.8 Typical Characteristics

at T_A = 25°C (unless otherwise noted)

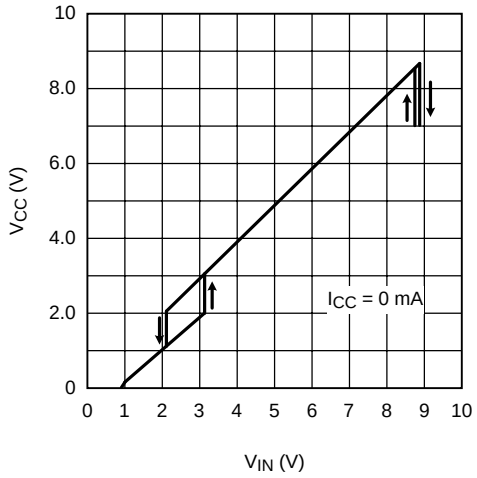


Figure 2. V_{CC} vs V_{IN}

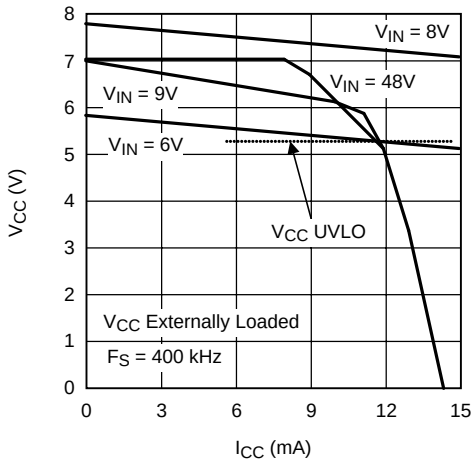


Figure 3. V_{CC} vs I_{CC}

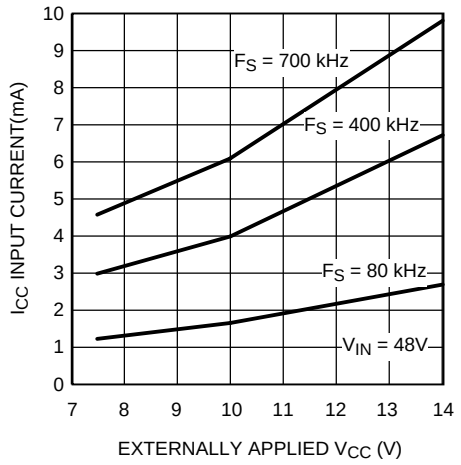


Figure 4. I_{CC} vs Externally Applied V_{CC}

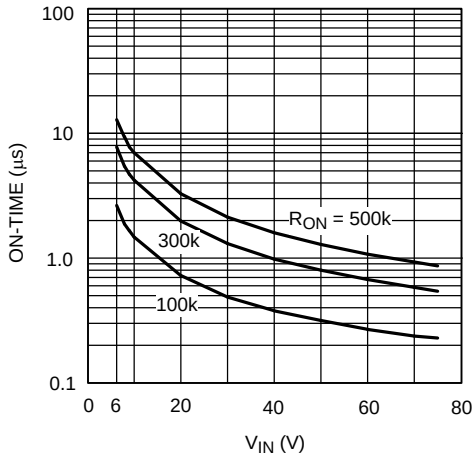


Figure 5. ON-Time vs V_{IN} and R_{ON}

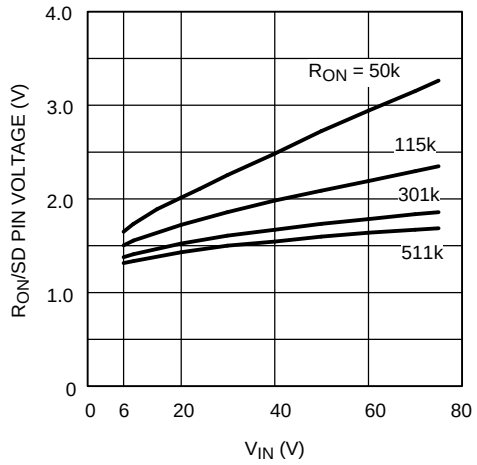


Figure 6. Voltage at R_{ON}/SD Pin

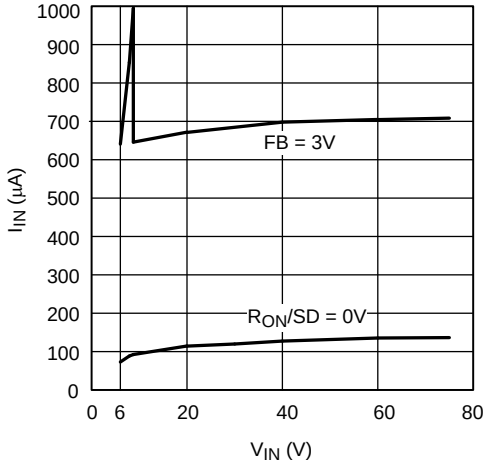


Figure 7. I_{IN} vs V_{IN}

Copyright © 2005–2016, Texas Instruments Incorporated

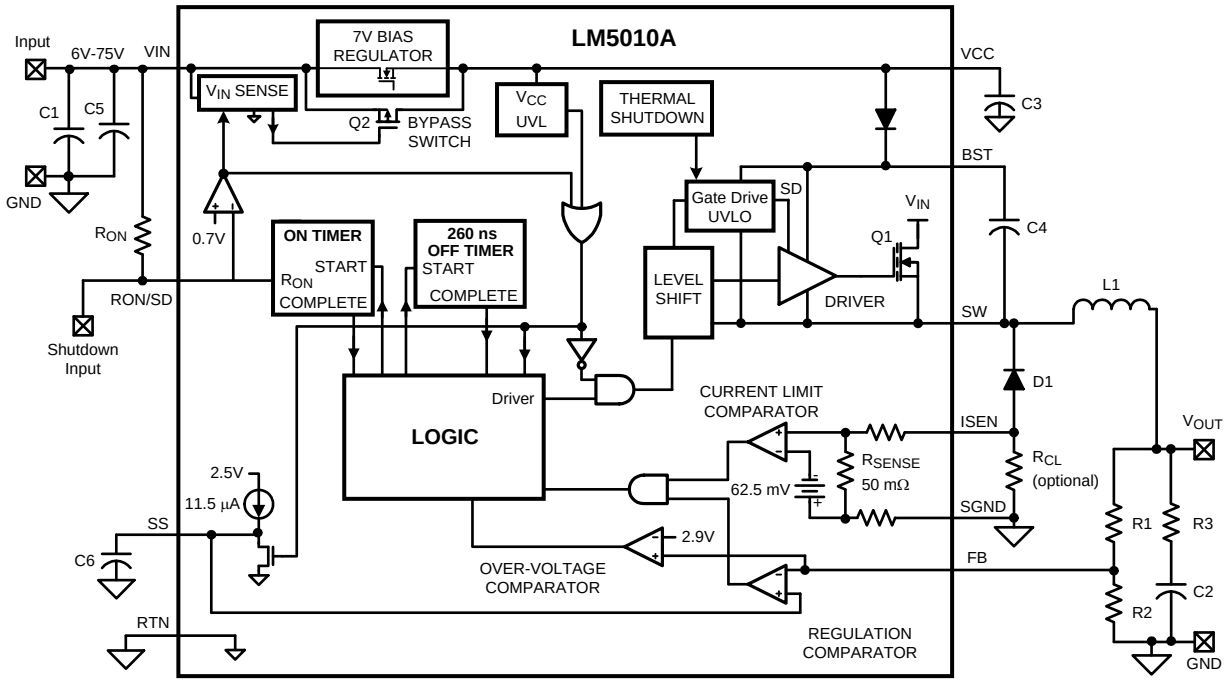
7 Detailed Description

7.1 Overview

The LM5010Ax step-down switching regulator features all the functions needed to implement a low-cost, efficient, buck bias power converter. This high-voltage regulator contains a 75-V N-channel buck switch, is easy to implement, and is provided in HTSSOP-14 and thermally-enhanced, WSON-10 packages. The regulator is based on a control scheme using an ON-time inversely proportional to V_{IN}. The control scheme requires no loop compensation. The functional block diagram of the LM5010Ax is shown in the *Functional Block Diagram*.

The LM5010Ax can be applied in numerous applications to efficiently regulate down higher voltages. This regulator is well-suited for 48-V telecom and 42-V automotive power bus ranges. Additional features include: thermal shutdown, V_{CC} undervoltage lockout, gate drive undervoltage lockout, maximum duty cycle limit timer, and the valley current limit functionality.

7.2 Functional Block Diagram



Copyright © 2016, Texas Instruments Incorporated

7.3 Feature Description

7.3.1 Control Circuit Overview

The LM5010Ax employs a control scheme based on a comparator and a one-shot ON timer, with the output voltage feedback (FB) compared to an internal reference (2.5 V). If the FB voltage is below the reference the buck switch is turned on for a time period determined by the input voltage and a programming resistor (R_{ON}). Following the ON-time the switch remains off for a fixed 260 ns OFF-time, or until the FB voltage falls below the reference, whichever is longer. The buck switch then turns on for another ON-time period. Referring to the Block Diagram, the output voltage is set by R1 and R2. The regulated output voltage is calculated with Equation 1.

$$V_{OUT} = 2.5\ V \times (R1 + R2) / R2 \quad (1)$$

The LM5010Ax requires a minimum of 25 mV of ripple voltage at the FB pin for stable fixed-frequency operation. If the output capacitor's ESR is insufficient, additional series resistance may be required (R3 in the Block Diagram).

Feature Description (continued)

The LM5010Ax operates in continuous conduction mode at heavy load currents, and discontinuous conduction mode at light load currents. In continuous conduction mode current always flows through the inductor, never decaying to zero during the OFF-time. In this mode the operating frequency remains relatively constant with load and line variations. The minimum load current for continuous conduction mode is one-half the inductor's ripple current amplitude. Calculate the operating frequency in the continuous conduction mode with Equation 2.

$$F_S = \frac{V_{OUT} \times (V_{IN} - 1.4V)}{1.18 \times 10^{-10} \times (R_{ON} + 1.4\ k\Omega) \times V_{IN}} \quad (2)$$

The buck switch duty cycle is equal to Equation 3.

$$DC = \frac{t_{ON}}{t_{ON} + t_{OFF}} = t_{ON} \times F_S = \frac{V_{OUT}}{V_{IN}} \quad (3)$$

Under light load conditions, the LM5010Ax operates in discontinuous conduction mode, with zero current flowing through the inductor for a portion of the OFF-time. The operating frequency is always lower than that of the continuous conduction mode, and the switching frequency varies with load current. Conversion efficiency is maintained at a relatively high level at light loads because the switching losses diminish as the power delivered to the load is reduced. Calculate the discontinuous mode operating frequency with Equation 4.

$$F_S = \frac{V_{OUT}^2 \times L1 \times 1.4 \times 10^{20}}{R_L \times R_{ON}^2} \quad (4)$$

where

- R_L is the load resistance

7.3.2 Start-Up Regulator (V_{CC})

A high voltage bias regulator is integrated within the LM5010Ax. The input pin (VIN) can be connected directly to line voltages between 6 and 75 V. Referring to the block diagram and the graph of V_{CC} vs V_{IN}, when V_{IN} is between 6 V and the bypass threshold (nominally 8.9 V), the bypass switch (Q2) is on, and V_{CC} tracks V_{IN} within 100 mV to 150 mV. The bypass switch on-resistance is approximately 50 Ω, with inherent current limiting at approximately 100 mA. When VIN is above the bypass threshold, Q2 is turned off, and V_{CC} is regulated at 7 V. The V_{CC} regulator output current is limited at approximately 15 mA. When the LM5010Ax is shutdown using the RON/SD pin, the V_{CC} bypass switch is shut off, regardless of the voltage at VIN.

When V_{IN} exceeds the bypass threshold, the time required for Q2 to shut off is approximately 2 to 3 µs. The capacitor at VCC (C3) must be a minimum of 0.47 µF to prevent the voltage at VCC from rising above its absolute maximum rating in response to a step input applied at VIN. C3 must be located as close as possible to the LM5010Ax pins.

In applications with a relatively high input voltage, power dissipation in the bias regulator is a concern. An auxiliary voltage of between 7.5 V and 14 V can be diode connected to the VCC pin (D2 in Figure 8) to shut off the VCC regulator, reducing internal power dissipation. The current required into the VCC pin is shown in the Typical Performance Characteristics. Internally a diode connects VCC to VIN requiring that the auxiliary voltage be less than V_{IN}.

The turn-on sequence is shown in Figure 1. When VCC exceeds the undervoltage lockout threshold (UVLO) of 5.25 V (t1 in Figure 1), the buck switch is enabled, and the SS pin is released to allow the soft-start capacitor (C6) to charge up. The output voltage V_{OUT} is regulated at a reduced level which increases to the desired value as the soft-start voltage increases (t2 in Figure 1).

Copyright © 2005–2016, Texas Instruments Incorporated

Feature Description (continued)

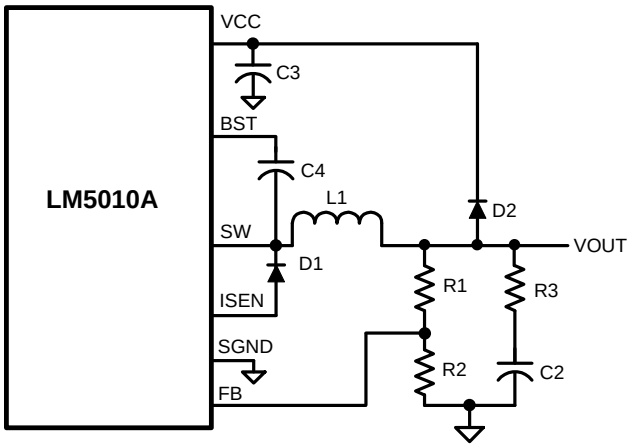


Figure 8. Self Biased Configuration

7.3.3 Regulation Comparator

The feedback voltage at the FB pin is compared to the voltage at the SS pin (2.5 V, ±2%). In normal operation an ON-time period is initiated when the voltage at FB falls below 2.5 V. The buck switch conducts for the ON-time programmed by R_{ON}, causing the FB voltage to rise above 2.5 V. After the ON-time period the buck switch remains off until the FB voltage falls below 2.5 V. Input bias current at the FB pin is less than 5 nA over temperature.

7.3.4 Overvoltage Comparator

The feedback voltage at FB is compared to an internal 2.9-V reference. If the voltage at FB rises above 2.9 V the ON-time is immediately terminated. This condition can occur if the input voltage, or the output load, changes suddenly. The buck switch remains off until the voltage at FB falls below 2.5 V.

7.3.5 ON-Time Control

The ON-time of the internal buck switch is determined by the R_{ON} resistor and the input voltage (V_{IN}), and is calculated with Equation 5.

$$t_{ON} = \frac{1.18 \times 10^{-10} \times (R_{ON} + 1.4k)}{(V_{IN} - 1.4V)} + 67\ ns \quad (5)$$

The R_{ON} resistor can be determined from the desired ON-time by re-arranging Equation 5 to Equation 6.

$$R_{ON} = \frac{(t_{ON} - 67\ ns) \times (V_{IN} - 1.4V)}{1.18 \times 10^{-10}} - 1.4\ k\Omega \quad (6)$$

To set a specific continuous conduction mode switching frequency (f_S), the R_{ON} resistor is determined with Equation 7.

$$R_{ON} = \frac{V_{OUT} \times (V_{IN} - 1.4V)}{V_{IN} \times F_S \times 1.18 \times 10^{-10}} - 1.4\ k\Omega \quad (7)$$

In high frequency applications the minimum value for t_{ON} is limited by the maximum duty cycle required for regulation and the minimum OFF-time of the LM5010Ax (260 ns, ±15%). The fixed OFF-time limits the maximum duty cycle achievable with a low voltage at VIN. The minimum allowed ON-time to regulate the desired V_{OUT} at the minimum V_{IN} is determined with Equation 8.

Copyright © 2005–2016, Texas Instruments Incorporated

Feature Description (continued)

$$t_{ON(min)} = \frac{V_{OUT} \times 300\ ns}{(V_{IN(min)} - V_{OUT})} \quad (8)$$

7.3.6 Soft Start

The soft start feature allows the regulator to gradually reach a steady-state operating point, thereby reducing start-up stresses and current surges. At turnon, while V_{CC} is below the undervoltage threshold (t1 in Figure 1), the SS pin is internally grounded, and V_{OUT} is held at 0 V. When V_{CC} exceeds the undervoltage threshold (UVLO) an internal 11.5-µA current source charges the external capacitor (C6) at the SS pin to 2.5 V (t2 in Figure 1). The increasing SS voltage at the non-inverting input of the regulation comparator gradually increases the output voltage from zero to the desired value. The softstart feature keeps the load inductor current from reaching the current limit threshold during start-up, thereby reducing inrush currents.

An internal switch grounds the SS pin if V_{CC} is below the undervoltage lockout threshold, or if the circuit is shutdown using the R_{ON}/SD pin.

7.3.7 N-Channel Buck Switch and Driver

The LM5010Ax integrates an N-Channel buck switch and associated floating high voltage gate driver. The peak current through the buck switch should not exceed 2 A, and the load current should not exceed 1.5 A. The gate driver circuit is powered by the external bootstrap capacitor between BST and SW (C4), which is recharged each OFF-time from V_{CC} through the internal high voltage diode. The minimum OFF-time, nominally 260 ns, ensures sufficient time during each cycle to recharge the bootstrap capacitor. A 0.022-µF ceramic capacitor is recommended for C4.

7.3.8 Current Limit

Current limit detection occurs during the OFF-time by monitoring the recirculating current through the internal current sense resistor (R_{SENSE}). The detection threshold is 1.25 A, ±0.25 A. Referring to *Functional Block Diagram*, if the current into SGND during the OFF-time exceeds the threshold level the current limit comparator delays the start of the next ON-time period. The next ON-time starts when the current into SGND is below the threshold and the voltage at FB is below 2.5 V. Figure 9 illustrates the inductor current waveform during normal operation and during current limit. The output current I_O is the average of the inductor ripple current waveform. The low load current waveform illustrates continuous conduction mode operation with peak and valley inductor currents below the current limit threshold. When the load current is increased (high load current), the ripple waveform maintains the same amplitude and frequency since the current falls below the current limit threshold at the valley of the ripple waveform. Note the average current in the high load current portion of Figure 9 is above the current limit threshold. Since the current reduces below the threshold in the normal OFF-time each cycle, the start of each ON-time is not delayed, and the circuit's output voltage is regulated at the correct value. When the load current is further increased such that the lower peak would be above the threshold, the OFF-time is lengthened to allow the current to decrease to the threshold before the next ON-time begins (Current Limited portion of Figure 9). Both V_{OUT} and the switching frequency are reduced as the circuit operates in a constant current mode. The load current (I_{OCL}) is equal to the current limit threshold plus half the ripple current (ΔI/2). The ripple amplitude (ΔI) is calculated with Equation 9.

$$\Delta I = \frac{(V_{IN} - V_{OUT}) \times t_{ON}}{L1} \quad (9)$$

The current limit threshold can be increased by connecting an external resistor (R_{CL}) between SGND and ISEN. R_{CL} typically is less than 1 Ω, and the calculation of its value is explained in *Application and Implementation*. If the current limit threshold is increased by adding R_{CL}, the maximum continuous load current should not exceed 1.5 A, and the peak current out of the SW pin should not exceed 2 A.

Copyright © 2005–2016, Texas Instruments Incorporated

Feature Description (continued)

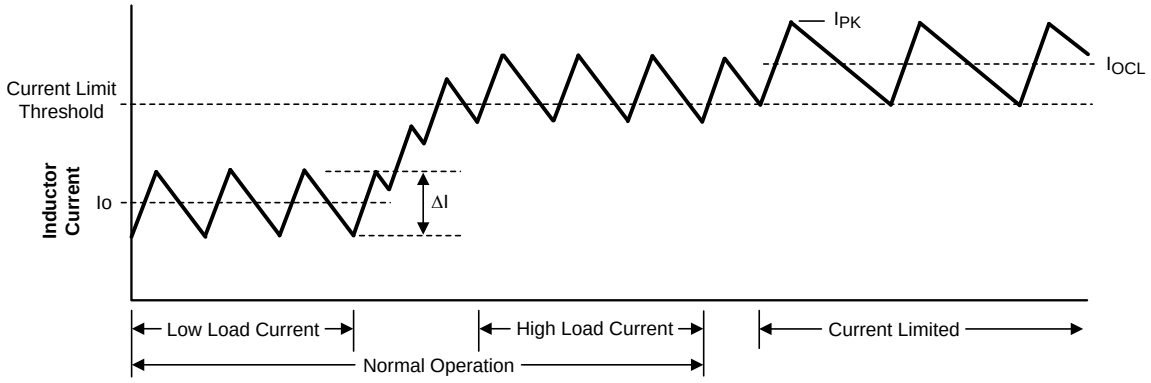


Figure 9. Inductor Current, Current Limit Operation

7.3.9 Thermal Shutdown

The LM5010Ax should be operated below the maximum operating junction temperature rating. If the junction temperature increases during a fault or abnormal operating condition, the internal thermal shutdown circuit activates typically at 175°C. The Thermal Shutdown circuit reduces power dissipation by disabling the buck switch and the ON timer. This feature helps prevent catastrophic failures from accidental device overheating. When the junction temperature reduces below approximately 155°C (20°C typical hysteresis), normal operation resumes.

7.4 Device Functional Modes

7.4.1 Shutdown

The LM5010Ax can be remotely shut down by forcing the R_{ON}/SD pin below 0.7 V with a switch or open drain device. See Figure 10. In the shutdown mode the SS pin is internally grounded, the ON-time one-shot is disabled, the input current at VIN is reduced, and the V_{CC} bypass switch is turned off. The V_{CC} regulator is not disabled in the shutdown mode. Releasing the R_{ON}/SD pin allows normal operation to resume. The nominal voltage at R_{ON}/SD is shown in the Typical Performance Characteristics. When switching the R_{ON}/SD pin, the transition time should be faster than one to two cycles of the regulator's nominal switching frequency.

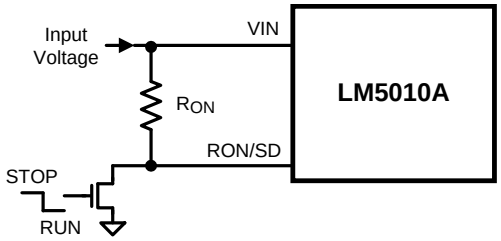


Figure 10. Shutdown Implementation

Copyright © 2005–2016, Texas Instruments Incorporated

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

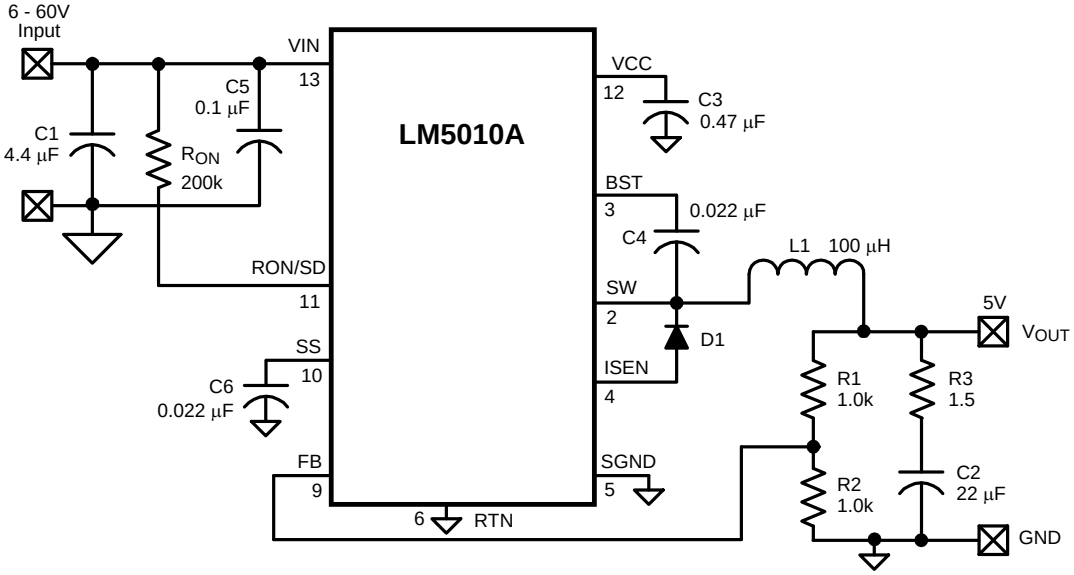
8.1 Application Information

The LM5010A is a non-synchronous buck regulator converter designed to operate over a wide input voltage and output current range. Spreadsheet-based calculator tools, available on the TI product website at Quick-Start Calculator, can be used to design a single output non-synchronous buck converter.

Alternatively, online WEBENCH® software is available to create a complete buck design and generate the bill of materials, estimated efficiency, solution size, and cost of the complete solution.

8.2 Typical Application

The final circuit is shown in Figure 11, and its performance is shown in Figure 16 and Figure 17. Current limit measured at approximately 1.3 A.



Copyright © 2016, Texas Instruments Incorporated

Figure 11. LM5010A Example Circuit

8.2.1 Design Requirements

Table 1 lists the operating parameters for Figure 11.

Table 1. Design Parameters

PARAMETER	EXAMPLE VALUE
Input voltage	6 V to 60 V
Output voltage	5 V
Load current	200 mA to 1 A
Soft-start time	5 ms

Copyright © 2005–2016, Texas Instruments Incorporated

8.2.2 Detailed Design Procedure

The procedure for calculating the external components is illustrated with a design example. Configure the circuit in Figure 11 according to the components listed in Table 2.

Table 2. List of Components for LM5010A Example Circuit

ITEM	DESCRIPTION	VALUE
C1	Ceramic capacitor	(2) 2.2 µF, 100 V
C2	Ceramic capacitor	22 µF, 16 V
C3	Ceramic capacitor	0.47 µF, 16 V
C4, C6	Ceramic capacitor	0.022 µF, 16 V
C5	Ceramic capacitor	0.1 µF, 100 V
D1	Schottky diode	100V, 6 A
L1	Inductor	100 µH
R1	Resistor	1 kΩ
R2	Resistor	1 kΩ
R3	Resistor	1.5 Ω
R_{ON}	Resistor	200 kΩ
U1	LM5010Ax	—

8.2.2.1 Component Selection

8.2.2.1.1 R1 and R2

These resistors set the output voltage, and calculate their ratio with Equation 10.

$$R1/R2 = (V_{OUT} / 2.5\ V) - 1 \quad (10)$$

R1 and R2 calculates to 1. The resistors should be chosen from standard value resistors in the range of 1 kΩ to 10 kΩ. A value of 1 kΩ is used for R1 and R2.

8.2.2.1.2 R_{ON}, F_S

R_{ON} can be chosen using Equation 7 to set the nominal frequency, or from Equation 6 if the ON-time at a particular V_{IN} is important. A higher frequency generally means a smaller inductor and capacitors (value, size and cost), but higher switching losses. A lower frequency means a higher efficiency, but with larger components. Generally, if PC board space is tight, a higher frequency is better. The resulting ON-time and frequency have a ±25% tolerance. Using Equation 7 at a nominal V_{IN} of 8 V, R_{ON} is calculated with Equation 11.

$$R_{ON} = \frac{5V \times (8V - 1.4V)}{8V \times 175\ kHz \times 1.18 \times 10^{-10}} - 1.4\ k\Omega = 198\ k\Omega \quad (11)$$

A value of 200 kΩ will be used for R_{ON}, yielding a nominal frequency of 161 kHz at V_{IN} = 6 V, and 205 kHz at V_{IN} = 60 V.

8.2.2.1.3 L1

The guideline for choosing the inductor value in this example is that it must keep the circuit's operation in continuous conduction mode at minimum load current. This is not a strict requirement since the LM5010Ax regulates correctly when in discontinuous conduction mode, although at a lower frequency. However, to provide an initial value for L1 the above guideline will be used. See Figure 12.

Copyright © 2005–2016, Texas Instruments Incorporated

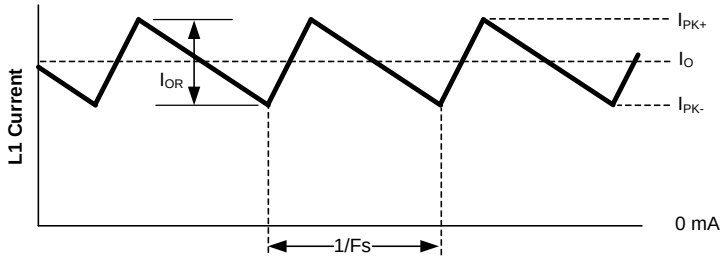


Figure 12. Inductor Current

To keep the circuit in continuous conduction mode, the maximum allowed ripple current is twice the minimum load current, or 400 mAp-p. Using this value of ripple current, the inductor (L1) is calculated using Equation 12 and Equation 13.

$$L1 = \frac{V_{OUT} \times (V_{IN(max)} - V_{OUT})}{I_{OR} \times F_{S(min)} \times V_{IN(max)}}$$

where

- $F_{S(min)}$ is the minimum frequency of 154 kHz (205 kHz - 25%) at $V_{IN(max)}$ (12)

$$L1 = \frac{5V \times (60V - 5V)}{0.40A \times 154\ kHz \times 60V} = 74.4\ \mu H \quad (13)$$

Equation 13 provides the minimum value for inductor L1. When selecting an inductor, use a higher standard value (100 uH). To prevent saturation, and possible destructive current levels, L1 must be rated for the peak current which occurs if the current limit and maximum ripple current are reached simultaneously (I_{PK} in Figure 9). The maximum ripple amplitude is calculated by rearranging Equation 12 using $V_{IN(max)}$, $F_{S(min)}$, and the minimum inductor value, based on the manufacturer's tolerance. Assume for Equation 14, Equation 15, and Equation 16 that the inductor's tolerance is ±20%.

$$I_{OR(max)} = \frac{V_{OUT} \times (V_{IN(max)} - V_{OUT})}{L1_{min} \times F_{S(min)} \times V_{IN(max)}} \quad (14)$$

$$I_{OR(max)} = \frac{5V \times (60V - 5V)}{80\ \mu H \times 154\ kHz \times 60V} = 372\ mAp\text{-}p \quad (15)$$

$I_{PK} = I_{LIM} + I_{OR(max)} = 1.5\ A + 0.372\ A = 1.872\ A$

where

- I_{LIM} is the maximum current limit threshold (16)

At the nominal maximum load current of 1 A, the peak inductor current is 1.186 A.

8.2.2.1.4 R_{CL}

Since it is obvious that the lower peak of the inductor current waveform does not exceed 1 A at maximum load current (see Figure 12), it is not necessary to increase the current limit threshold. Therefore R_{CL} is not needed for this exercise. For applications where the lower peak exceeds 1 A, see *Increasing The Current Limit Threshold*.

Copyright © 2005–2016, Texas Instruments Incorporated

8.2.2.1.5 C1

This capacitor limits the ripple voltage at VIN resulting from the source impedance of the supply feeding this circuit, and the on and off nature of the switch current into VIN. At maximum load current, when the buck switch turns on, the current into VIN steps up from zero to the lower peak of the inductor current waveform (I_{PK-} in Figure 12), ramps up to the peak value (I_{PK+}), then drops to zero at turnoff. The average current into VIN during this ON-time is the load current. For a worst case calculation, C1 must supply this average current during the maximum ON-time. The maximum ON-time is calculated at V_{IN} = 6 V using Equation 5, with a 25% tolerance added in Equation 17.

$$t_{ON(max)} = \left[\frac{1.18 \times 10^{-10} \times (200k + 1.4k)}{6V - 1.4V} + 67\ ns\right] \times 1.25 = 6.5\ \mu s \tag{17}$$

The voltage at VIN should not be allowed to drop below 5.5 V in order to maintain V_{CC} above its UVLO as in Equation 18.

$$C1 = \frac{I_O \times t_{ON}}{\Delta V} = \frac{1.0A \times 6.5\ \mu s}{0.5V} = 13\ \mu F \tag{18}$$

Normally a lower value can be used for C1 since the above calculation is a worst case calculation which assumes the power source has a high source impedance. A quality ceramic capacitor with a low ESR should be used for C1.

8.2.2.1.6 C2 and R3

Since the LM5010Ax requires a minimum of 25 mVp-p of ripple at the FB pin for proper operation, the required ripple at V_{OUT} is increased by R1 and R2, and is equal to Equation 19.

$$V_{RIPPLE} = 25\ mVp\text{-}p \times (R1 + R2) / R2 = 50\ mVp\text{-}p \tag{19}$$

This necessary ripple voltage is created by the inductor ripple current acting on C2's ESR + R3. First, the minimum ripple current is determined which occurs at minimum VIN, maximum inductor value, and calculate the maximum frequency with Equation 20.

$$I_{OR(min)} = \frac{V_{OUT} \times (V_{IN(min)} - V_{OUT})}{L1_{max} \times F_{S(max)} \times V_{IN(min)}}$$

$$= \frac{5V \times (6V - 5V)}{120\ \mu H \times 201\ kHz \times 6V} = 34.5\ mAp\text{-}p \tag{20}$$

The minimum ESR for C2 is then equal to Equation 21.

$$ESR_{(min)} = \frac{50\ mV}{34.5\ mA} = 1.45\Omega \tag{21}$$

If the capacitor used for C2 does not have sufficient ESR, R3 is added in series as shown in the Block Diagram. The value chosen for C2 is application dependent, and it is recommended that it be no smaller than 3.3 µF. C2 affects the ripple at V_{OUT}, and transient response. Experimentation is usually necessary to determine the optimum value for C2.

8.2.2.1.7 C3

The capacitor at the VCC pin provides noise filtering and stability, prevents false triggering of the V_{CC} UVLO at the buck switch ON and OFF transitions, and limits the peak voltage at V_{CC} when a high voltage with a short rise time is initially applied at V_{IN}. C3 should be no smaller than 0.47 µF, and must be a good quality, low ESR, ceramic capacitor, physically close to the IC pins.

8.2.2.1.8 C4

The recommended value for C4 is 0.022 µF. A high quality ceramic capacitor with low ESR is recommended as C4 supplies the surge current to charge the buck switch gate at each turnon. A low ESR also ensures a complete recharge during each OFF-time.

Copyright © 2005–2016, Texas Instruments Incorporated

8.2.2.1.9 C5

This capacitor suppresses transients and ringing due to lead inductance at VIN. TI recommends a low ESR, 0.1 µF ceramic chip capacitor, placed physically close to the LM5010Ax.

8.2.2.1.10 C6

The capacitor at the SS pin determines the soft-start time (that is the time for the reference voltage at the regulation comparator and the output voltage) to reach their final value. Determine the capacitor value with Equation 22.

$$C6 = \frac{t_{SS} \times 11.5\ \mu A}{2.5V} \tag{22}$$

For a 5 ms soft-start time, C6 calculates to 0.022 µF.

8.2.2.1.11 D1

A Schottky diode is recommended. Ultra-fast recovery diodes are not recommended as the high speed transitions at the SW pin may inadvertently affect the IC's operation through external or internal EMI. The diode should be rated for the maximum V_{IN} (60 V), the maximum load current (1 A), and the peak current which occurs when current limit and maximum ripple current are reached simultaneously (I_{PK} in Figure 9), previously calculated to be 1.87 A. The diode's forward voltage drop affects efficiency due to the power dissipated during the OFF-time. The average power dissipation in D1 is calculated from Equation 23.

$$P_{D1} = V_F \times I_O \times (1 - D) \tag{23}$$

where

- I_O is the load current
- D is the duty cycle

8.2.2.2 Low Output Ripple Configurations

For applications where low output voltage ripple is required the output can be taken directly from the low ESR output capacitor (C2) as shown in Figure 13. However, R3 slightly degrades the load regulation. The specific component values, and the application determine if this is suitable.

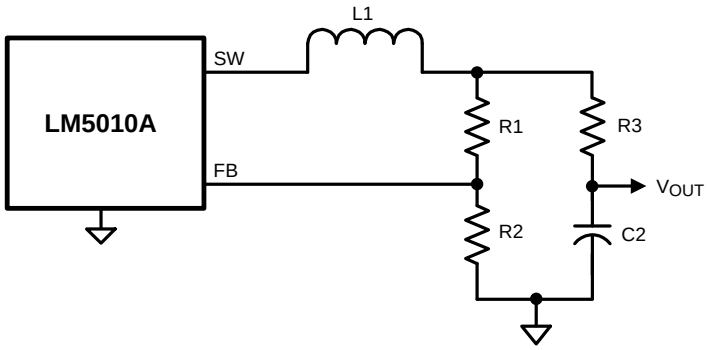


Figure 13. Low Ripple Output

Where the circuit of Figure 13 is not suitable, the circuits of Figure 14 or Figure 15 can be used.

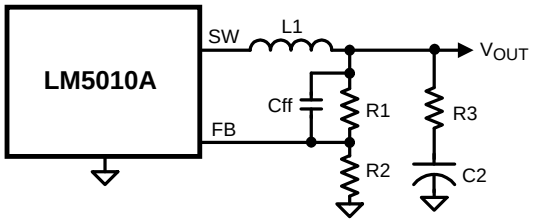


Figure 14. Low Output Ripple Using a Feed-Forward Capacitor

Copyright © 2005–2016, Texas Instruments Incorporated

In Figure 14, Cff is added across R1 to AC-couple the ripple at V_{OUT} directly to the FB pin. This allows the ripple at V_{OUT} to be reduced, in some cases considerably, by reducing R3. In the circuit of Figure 11, the ripple at V_{OUT} ranged from 50 mVp-p at V_{IN} = 6 V to 320 mVp-p at V_{IN} = 60 V. By adding a 1000 pF capacitor at Cff and reducing R3 to 0.75 Ω, the V_{OUT} ripple was reduced by 50%, ranging from 25 mVp-p to 160 mVp-p.

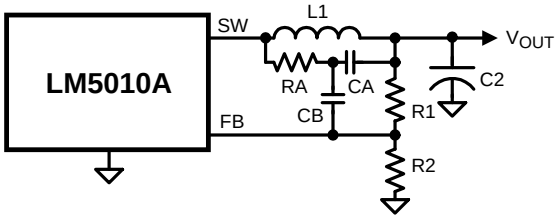


Figure 15. Low Output Ripple Using Ripple Injection

To reduce V_{OUT} ripple further, the circuit of Figure 15 can be used. R3 has been removed, and the output ripple amplitude is determined by C2's ESR and the inductor ripple current. RA and CA are chosen to generate a 40 to 50 mVp-p sawtooth at their junction, and that voltage is AC-coupled to the FB pin via CB. In selecting RA and CA, V_{OUT} is considered a virtual ground as the SW pin switches between V_{IN} and –1 V. Since the ON-time at SW varies inversely with V_{IN}, the waveform amplitude at the RA and CA junction is relatively constant. R1 and R2 must typically be increased to more than 10k each to not significantly attenuate the signal provided to FB through CB. Typical values for the additional components are RA = 200 k, CA = 680 pF, and CB = 0.01 µF.

8.2.2.3 Increasing The Current Limit Threshold

The current limit threshold is nominally 1.25 A, with a minimum value of 1 A. If, at maximum load current, the lower peak of the inductor current (I_{PK-} in Figure 12) exceeds 1 A, resistor R_{CL} must be added between S_{GND} and I_{SEN} to increase the current limit threshold to be equal or exceed that lower peak current. This resistor diverts some of the recirculating current from the internal sense resistor so that a higher current level is needed to switch the internal current limit comparator. Calculate I_{PK-} with Equation 24.

$$I_{PK-} = I_{O(max)} - \frac{I_{OR(min)}}{2} \quad (24)$$

where

- $I_{O(max)}$ is the maximum load current
- $I_{OR(min)}$ is the minimum ripple current calculated using Equation 20

R_{CL} is calculated from Equation 25.

$$R_{CL} = \frac{1.0A \times 0.11\Omega}{I_{PK-} - 1.0A} \quad (25)$$

where

- 0.11 Ω is the minimum value of the internal resistance from SGND to ISEN

The next smaller standard value resistor must be used for R_{CL}. With the addition of R_{CL}, and when the circuit is in current limit, the upper peak current out of the SW pin (I_{PK} in Figure 9) can be as high as Equation 26.

$$I_{PK} = \frac{1.5A \times (150\ m\Omega + R_{CL})}{R_{CL}} + I_{OR(MAX)} \quad (26)$$

where

- $I_{OR(max)}$ is calculated using Equation 14

The inductor L1 and diode D1 must be rated for this current. If I_{PK} exceeds 2 A , the inductor value must be increased to reduce the ripple amplitude. This will necessitate recalculation of $I_{OR(min)}$, I_{PK-}, and R_{CL}.

Increasing the circuit's current limit will increase power dissipation and the junction temperature within the LM5010Ax. See *Layout Guidelines* for guidelines on this issue.

Copyright © 2005–2016, Texas Instruments Incorporated

8.2.3 Application Curves

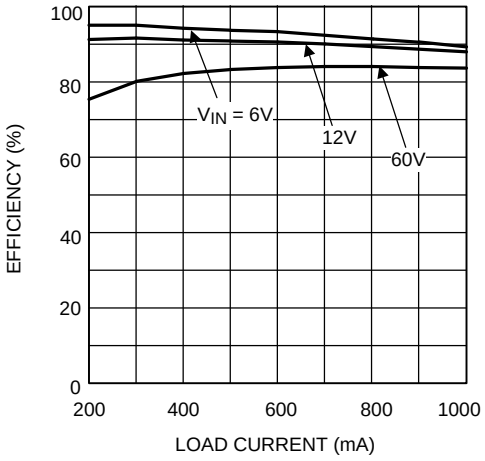


Figure 16. Efficiency vs Load Current and V_{IN}

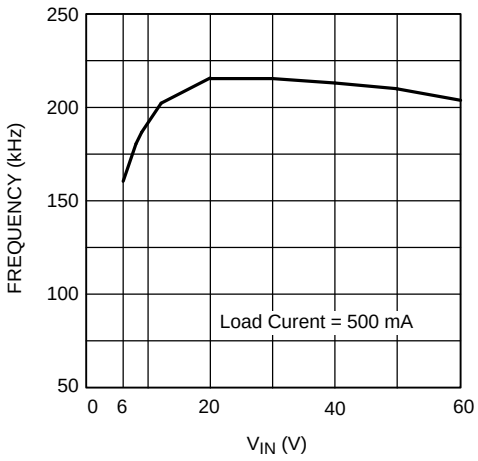


Figure 17. Frequency vs V_{IN}

8.3 Do's and Don'ts

A minimum load current of 500 µA is required to maintain proper operation. If the load current falls below that level, the bootstrap capacitor can discharge during the long OFF-time and the circuit either shuts down or cycles ON and OFF at a low frequency. If the load current is expected to drop below 500 µA in the application, choose the feedback resistors to be low enough in value to provide the minimum required current at nominal V_{OUT}.

Copyright © 2005–2016, Texas Instruments Incorporated

9 Power Supply Recommendations

The LM5010Ax is designed to operate with an input power supply capable of supplying a voltage range from 6 V to 75 V. The input power supply must be well-regulated and capable of supplying sufficient current to the regulator during peak load operation. Also, like in all applications, the power-supply source impedance must be small compared to the module input impedance to maintain the stability of the converter.

10 Layout

10.1 Layout Guidelines

The LM5010Ax regulation, overvoltage, and current limit comparators are very fast, and respond to short duration noise pulses. Therefore, layout considerations are critical for optimum performance. The layout must be as neat and compact as possible, and all the components must be as close as possible to their associated pins. The two major current loops have currents which switch very fast, and so the loops should be as small as possible to minimize conducted and radiated EMI. The first loop is that formed by C1 (C_{IN}), through the VIN to SW pins, L1 (L_{IND}), C2 (C_{OUT}), and back to C1. The second loop is that formed by D1, L1, C2, and the S_{GND} and I_{SEN} pins. The ground connection from C2 to C1 should be as short and direct as possible, preferably without going through vias. Directly connect the S_{GND} and RTN pin to each other, and they should be connected as directly as possible to the C1/C2 ground line without going through vias. The power dissipation within the IC can be approximated by determining the total conversion loss (P_{IN} - P_{OUT}), and then subtracting the power losses in the free-wheeling diode and the inductor. The power loss in the diode is approximately Equation 27.

$$P_{D1} = I_O \times V_F \times (1 - D) \quad (27)$$

where

- I_O is the load current
- V_F is the diode's forward voltage drop
- D is the duty cycle

The power loss in the inductor is approximately Equation 28.

$$P_{L1} = I_O^2 \times R_L \times 1.1 \quad (28)$$

where

- R_L is the inductor's DC resistance
- the 1.1 factor is an approximation for the AC losses

If it is expected that the internal dissipation of the LM5010Ax will produce high junction temperatures during normal operation, good use of the PC board's ground plane can help considerably to dissipate heat. The exposed pad on the IC package bottom should be soldered to a ground plane, and that plane should both extend from beneath the IC, and be connected to exposed ground plane on the board's other side using as many vias as possible. The exposed pad is internally connected to the IC substrate. The use of wide PC board traces at the pins, where possible, can help conduct heat away from the IC. The four no connect pins on the HTSSOP package are not electrically connected to any part of the IC, and may be connected to ground plane to help dissipate heat from the package. Judicious positioning of the PC board within the end product, along with the use of any available air flow (forced or natural convection) can help reduce the junction temperature.

Copyright © 2005–2016, Texas Instruments Incorporated

10.2 Layout Example

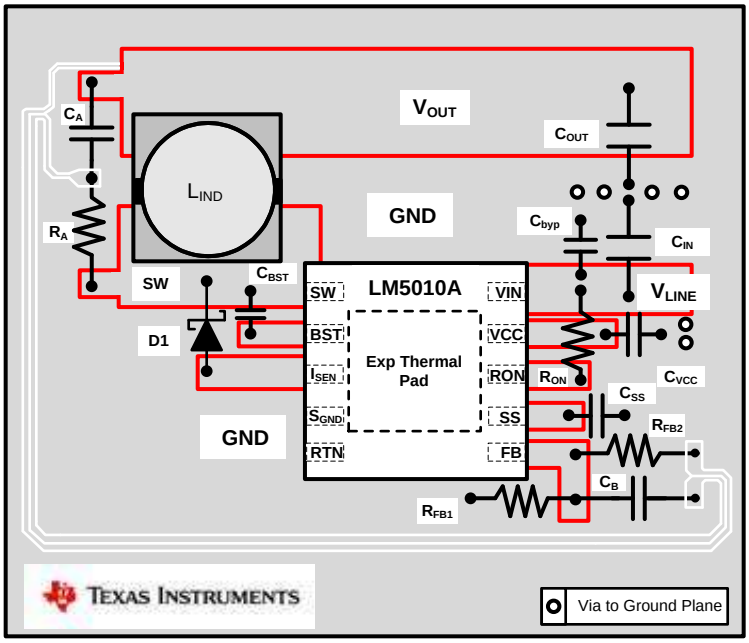


Figure 18. LM5010A Buck Layout Example With the WSON Package

Copyright © 2005–2016, Texas Instruments Incorporated

11 デバイスおよびドキュメントのサポート

11.1 関連リンク

次の表に、クイック・アクセス・リンクを示します。カテゴリには、技術資料、サポートおよびコミュニティ・リソース、ツールとソフトウェア、およびサンプル注文またはご購入へのクイック・アクセスが含まれます。

表 3. 関連リンク

製品	プロダクト・フォルダ	サンプルとご購入	技術資料	ツールとソフトウェア	サポートとコミュニティ
LM5010A	ここをクリック	ここをクリック	ここをクリック	ここをクリック	ここをクリック
LM5010A-Q1	ここをクリック	ここをクリック	ここをクリック	ここをクリック	ここをクリック

11.2 コミュニティ・リソース

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.3 商標

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.4 静電気放電に関する注意事項

これらのデバイスは、限定的なESD（静電破壊）保護機能を内 蔵しています。保存時または取り扱い時は、MOSゲートに対す る静電破壊を防止するために、リード線同士をショートさせて おくか、デバイスを導電フォームに入れる必要があります。

11.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。これらの情報は、指定のデバイスに対して提供されている最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

Copyright © 2005–2016, Texas Instruments Incorporated

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LM5010AMH/NOPB	Active	Production	HTSSOP (PWP) | 14	94 | TUBE	Yes	SN	Level-1-260C-UNLIM	-40 to 150	L5010 AMH
LM5010AMH/NOPB.A	Active	Production	HTSSOP (PWP) | 14	94 | TUBE	Yes	SN	Level-1-260C-UNLIM	-40 to 150	L5010 AMH
LM5010AMH/NOPB.B	Active	Production	HTSSOP (PWP) | 14	94 | TUBE	Yes	SN	Level-1-260C-UNLIM	-40 to 150	L5010 AMH
LM5010AMHE/NOPB	Active	Production	HTSSOP (PWP) | 14	250 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 150	L5010 AMH
LM5010AMHE/NOPB.A	Active	Production	HTSSOP (PWP) | 14	250 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 150	L5010 AMH
LM5010AMHE/NOPB.B	Active	Production	HTSSOP (PWP) | 14	250 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 150	L5010 AMH
LM5010AMHX/NOPB	Active	Production	HTSSOP (PWP) | 14	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 150	L5010 AMH
LM5010AMHX/NOPB.A	Active	Production	HTSSOP (PWP) | 14	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 150	L5010 AMH
LM5010AMHX/NOPB.B	Active	Production	HTSSOP (PWP) | 14	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 150	L5010 AMH
LM5010AQ0MH/NOPB	Active	Production	HTSSOP (PWP) | 14	94 | TUBE	Yes	SN	Level-1-260C-UNLIM	-40 to 150	L5010A Q0MH
LM5010AQ0MH/NOPB.A	Active	Production	HTSSOP (PWP) | 14	94 | TUBE	Yes	SN	Level-1-260C-UNLIM	-40 to 150	L5010A Q0MH
LM5010AQ0MH/NOPB.B	Active	Production	HTSSOP (PWP) | 14	94 | TUBE	Yes	SN	Level-1-260C-UNLIM	-40 to 150	L5010A Q0MH
LM5010AQ0MHX/NOPB	Active	Production	HTSSOP (PWP) | 14	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 150	L5010A Q0MH
LM5010AQ0MHX/NOPB.A	Active	Production	HTSSOP (PWP) | 14	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 150	L5010A Q0MH
LM5010AQ0MHX/NOPB.B	Active	Production	HTSSOP (PWP) | 14	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 150	L5010A Q0MH
LM5010AQ1MH/NOPB	Active	Production	HTSSOP (PWP) | 14	94 | TUBE	Yes	SN	Level-1-260C-UNLIM	-40 to 125	L5010A Q1MH

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LM5010AQ1MH/NOPB.A	Active	Production	HTSSOP (PWP) | 14	94 | TUBE	Yes	SN	Level-1-260C-UNLIM	-40 to 125	L5010A Q1MH
LM5010AQ1MH/NOPB.B	Active	Production	HTSSOP (PWP) | 14	94 | TUBE	Yes	SN	Level-1-260C-UNLIM	-40 to 125	L5010A Q1MH
LM5010AQ1MHX/NOPB	Active	Production	HTSSOP (PWP) | 14	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	L5010A Q1MH
LM5010AQ1MHX/NOPB.A	Active	Production	HTSSOP (PWP) | 14	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	L5010A Q1MH
LM5010AQ1MHX/NOPB.B	Active	Production	HTSSOP (PWP) | 14	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	L5010A Q1MH
LM5010ASD/NOPB	Active	Production	WSON (DPR) | 10	1000 | SMALL T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 150	L00065B
LM5010ASD/NOPB.A	Active	Production	WSON (DPR) | 10	1000 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 150	L00065B
LM5010ASD/NOPB.B	Active	Production	WSON (DPR) | 10	1000 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 150	L00065B
LM5010ASDX/NOPB	Active	Production	WSON (DPR) | 10	4500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 150	L00065B
LM5010ASDX/NOPB.A	Active	Production	WSON (DPR) | 10	4500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 150	L00065B
LM5010ASDX/NOPB.B	Active	Production	WSON (DPR) | 10	4500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 150	L00065B

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF LM5010A, LM5010A-Q1 :

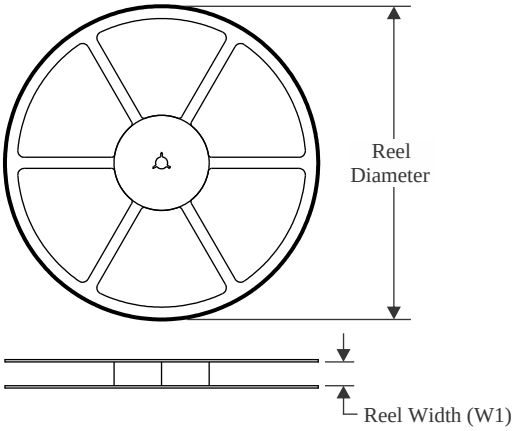
- Catalog : LM5010A
- Automotive : LM5010A-Q1

NOTE: Qualified Version Definitions:

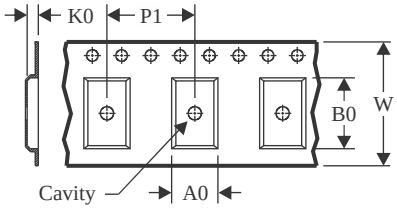
- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

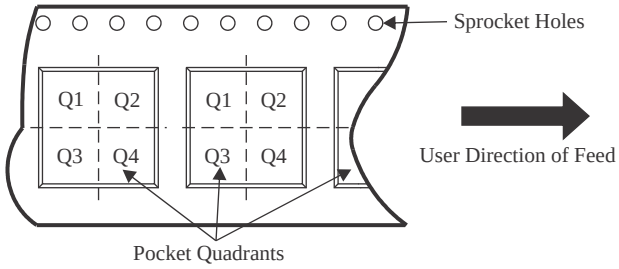


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

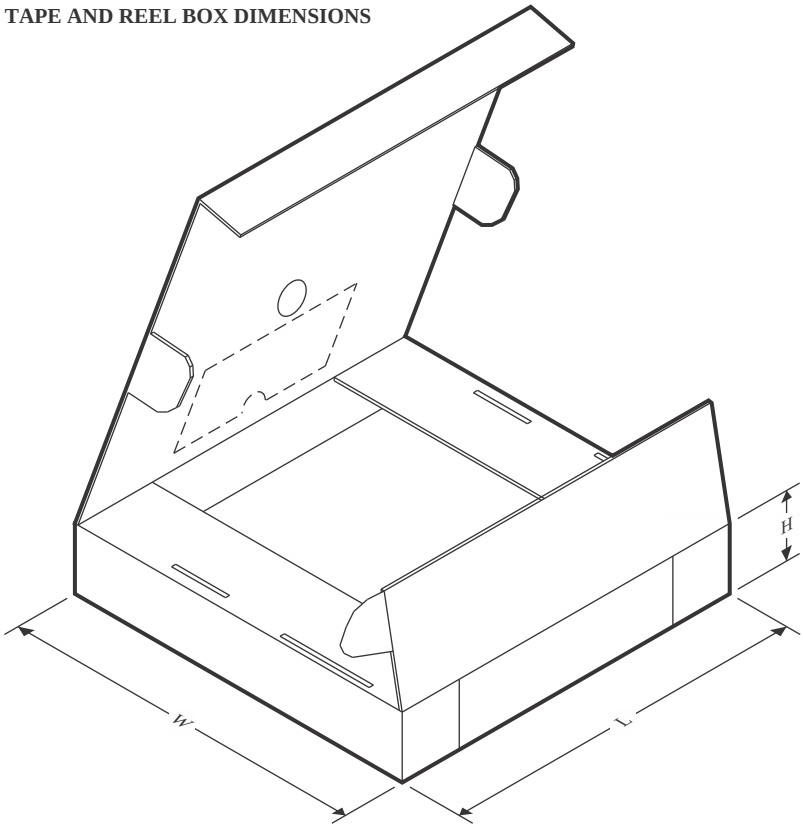
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM5010AMHE/NOPB	HTSSOP	PWP	14	250	177.8	12.4	6.9	5.6	1.6	8.0	12.0	Q1
LM5010AMHX/NOPB	HTSSOP	PWP	14	2500	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
LM5010AQ0MHX/NOPB	HTSSOP	PWP	14	2500	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
LM5010AQ1MHX/NOPB	HTSSOP	PWP	14	2500	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
LM5010ASD/NOPB	WSON	DPR	10	1000	177.8	12.4	4.3	4.3	1.3	8.0	12.0	Q1
LM5010ASDX/NOPB	WSON	DPR	10	4500	330.0	12.4	4.3	4.3	1.3	8.0	12.0	Q1

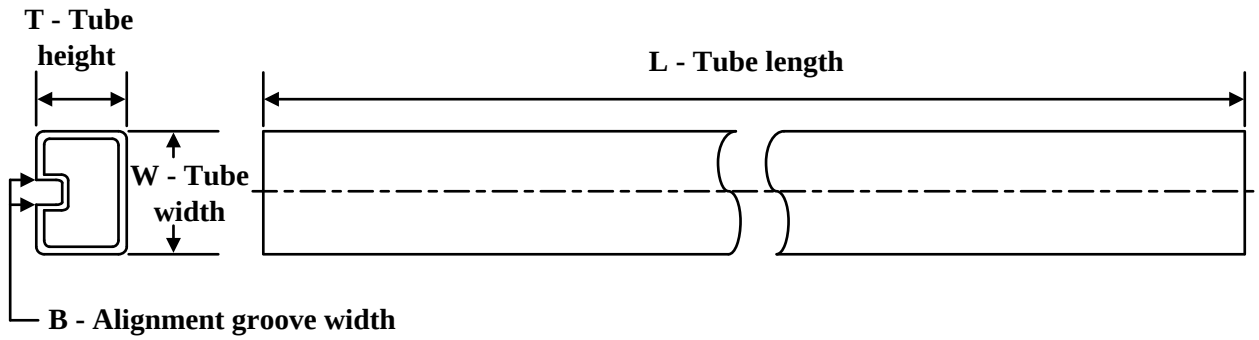
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

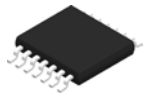
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM5010AMHE/NOPB	HTSSOP	PWP	14	250	208.0	191.0	35.0
LM5010AMHX/NOPB	HTSSOP	PWP	14	2500	367.0	367.0	35.0
LM5010AQ0MHX/NOPB	HTSSOP	PWP	14	2500	367.0	367.0	35.0
LM5010AQ1MHX/NOPB	HTSSOP	PWP	14	2500	367.0	367.0	35.0
LM5010ASD/NOPB	WSON	DPR	10	1000	208.0	191.0	35.0
LM5010ASDX/NOPB	WSON	DPR	10	4500	367.0	367.0	35.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
LM5010AMH/NOPB	PWP	HTSSOP	14	94	495	8	2514.6	4.06
LM5010AMH/NOPB.A	PWP	HTSSOP	14	94	495	8	2514.6	4.06
LM5010AMH/NOPB.B	PWP	HTSSOP	14	94	495	8	2514.6	4.06
LM5010AQ0MH/NOPB	PWP	HTSSOP	14	94	495	8	2514.6	4.06
LM5010AQ0MH/NOPB.A	PWP	HTSSOP	14	94	495	8	2514.6	4.06
LM5010AQ0MH/NOPB.B	PWP	HTSSOP	14	94	495	8	2514.6	4.06
LM5010AQ1MH/NOPB	PWP	HTSSOP	14	94	495	8	2514.6	4.06
LM5010AQ1MH/NOPB.A	PWP	HTSSOP	14	94	495	8	2514.6	4.06
LM5010AQ1MH/NOPB.B	PWP	HTSSOP	14	94	495	8	2514.6	4.06

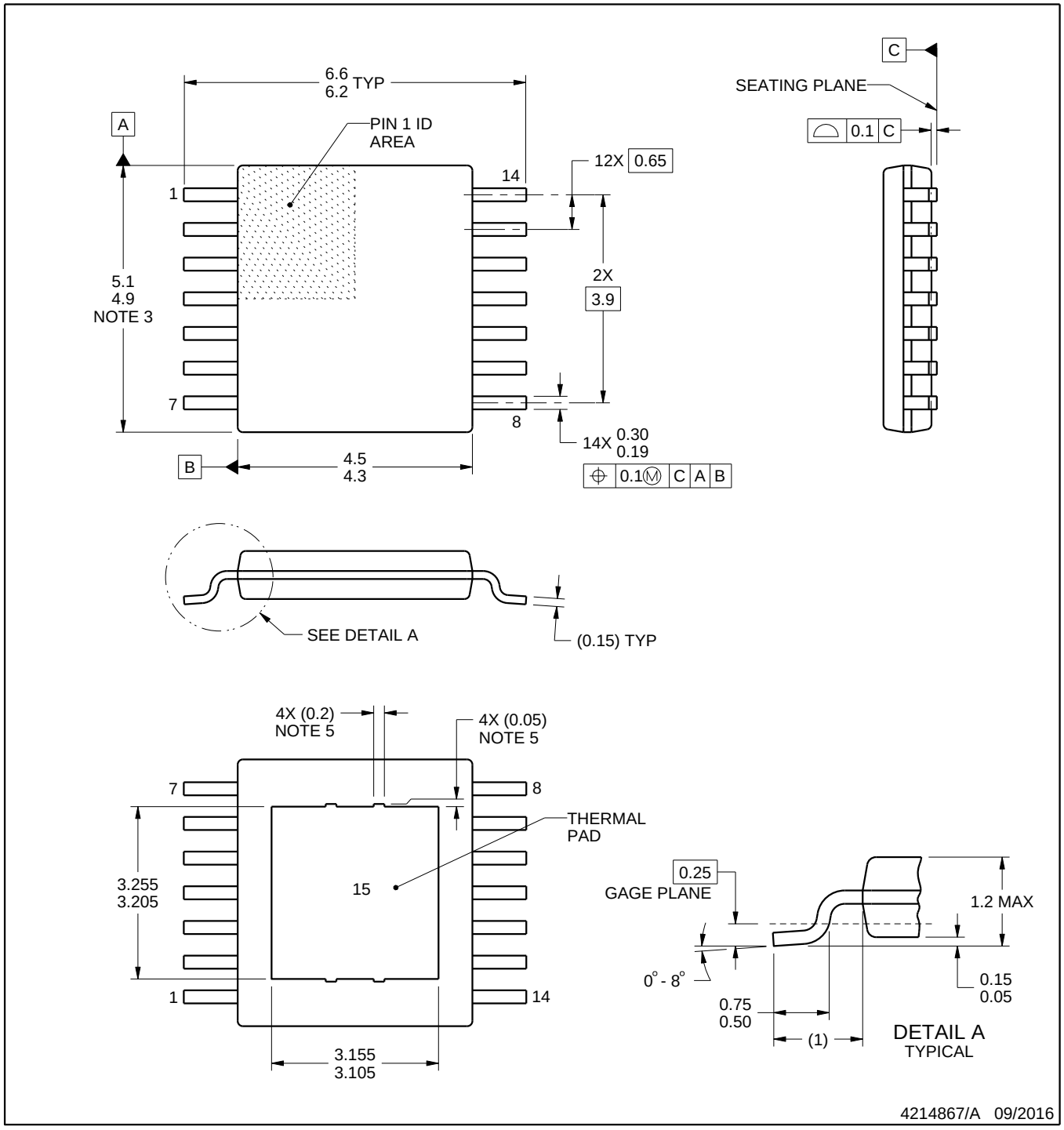


PACKAGE OUTLINE

PWP0014A

PowerPAD™ TSSOP - 1.2 mm max height

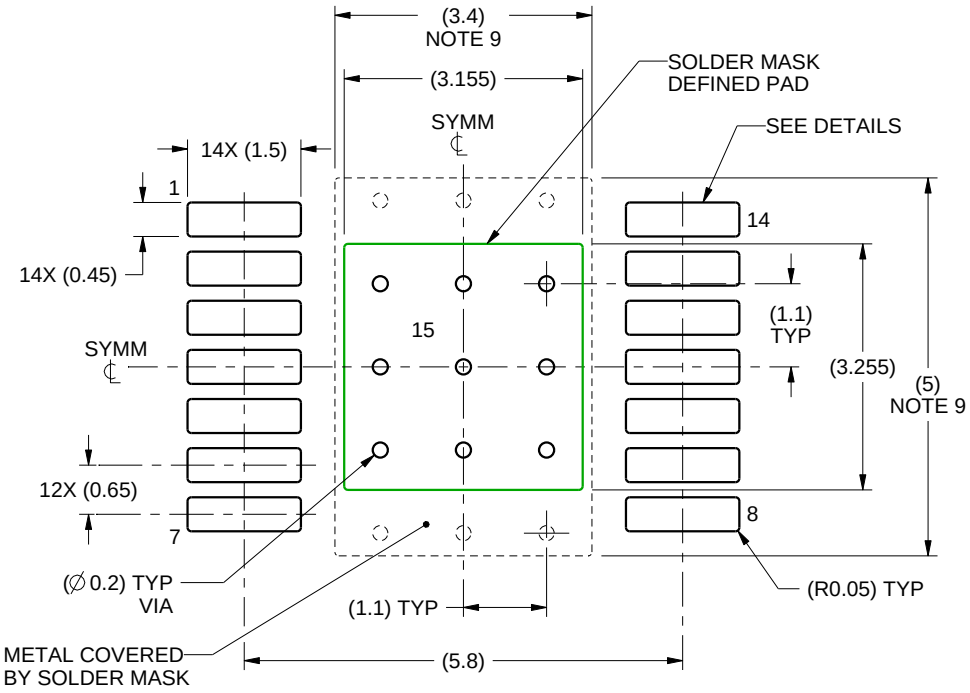
PLASTIC SMALL OUTLINE



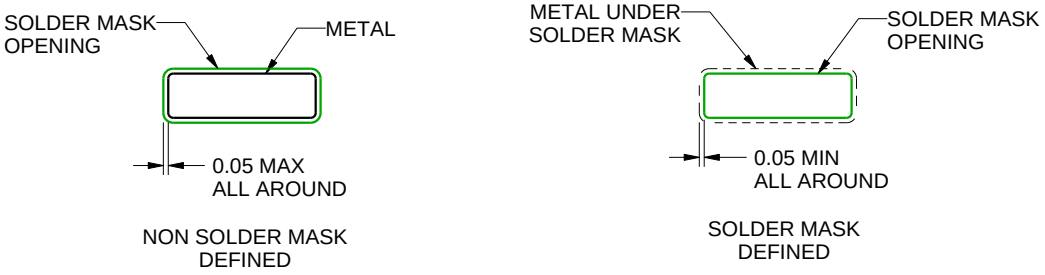
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.
5. Features may differ and may not be present.



LAND PATTERN EXAMPLE
SCALE:10X

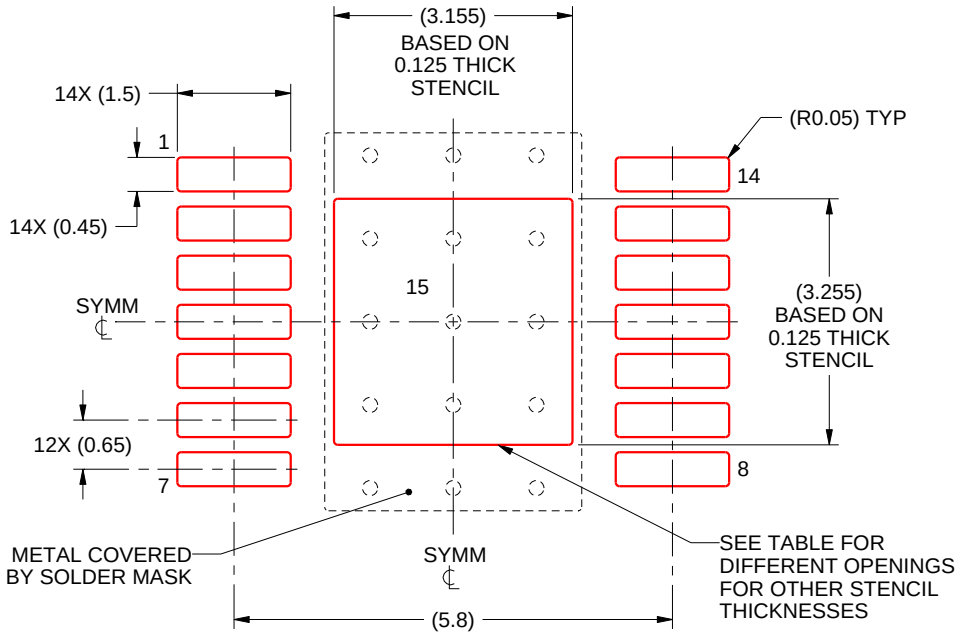


SOLDER MASK DETAILS
PADS 1-14

4214867/A 09/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
EXPOSED PAD
100% PRINTED SOLDER COVERAGE BY AREA
SCALE:10X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	3.53 X 3.64
0.125	3.155 X 3.255 (SHOWN)
0.15	2.88 X 2.97
0.175	2.67 X 2.75

4214867/A 09/2016

NOTES: (continued)

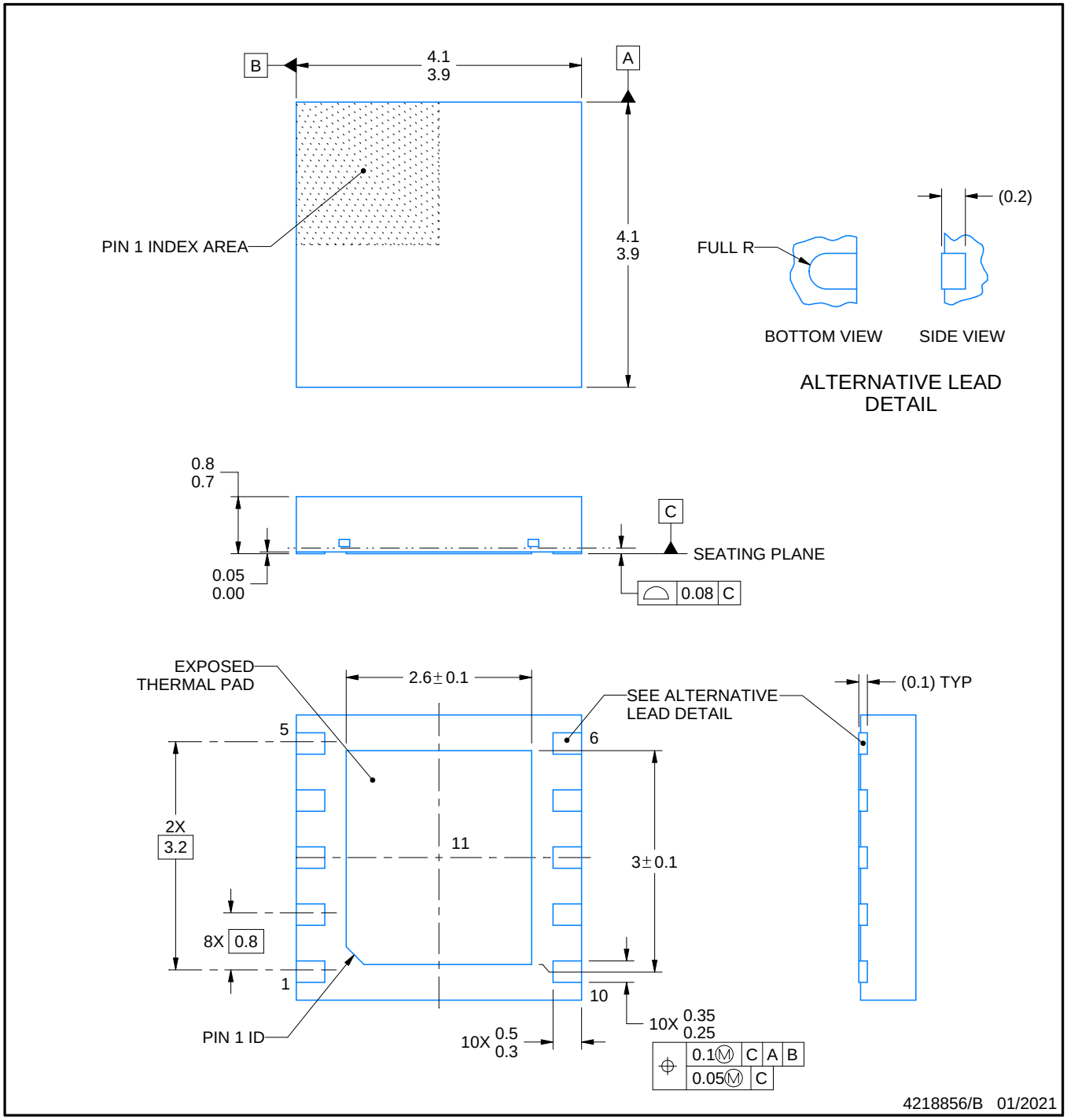
10. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
11. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DPR0010A

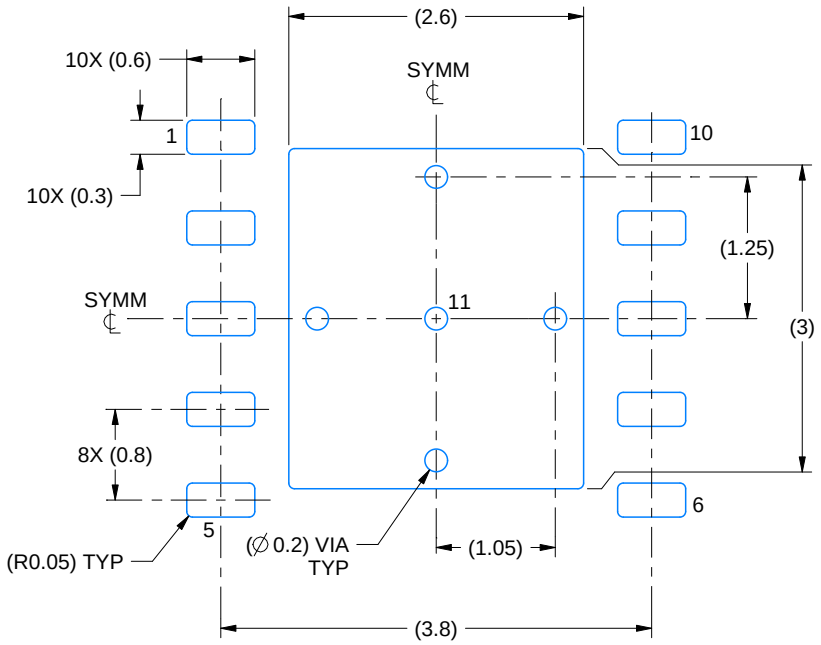
WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

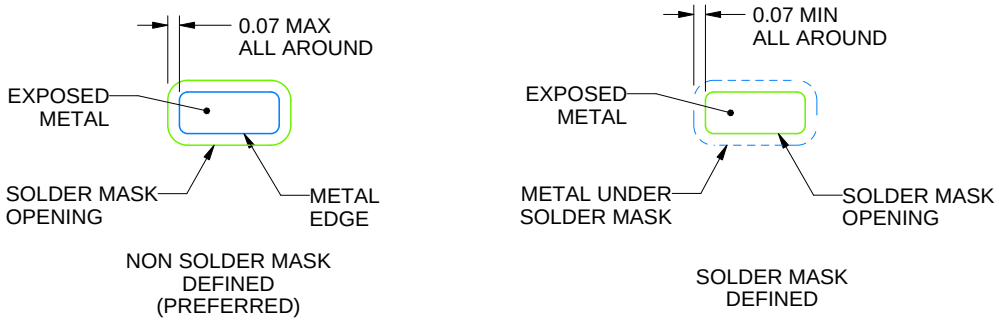


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

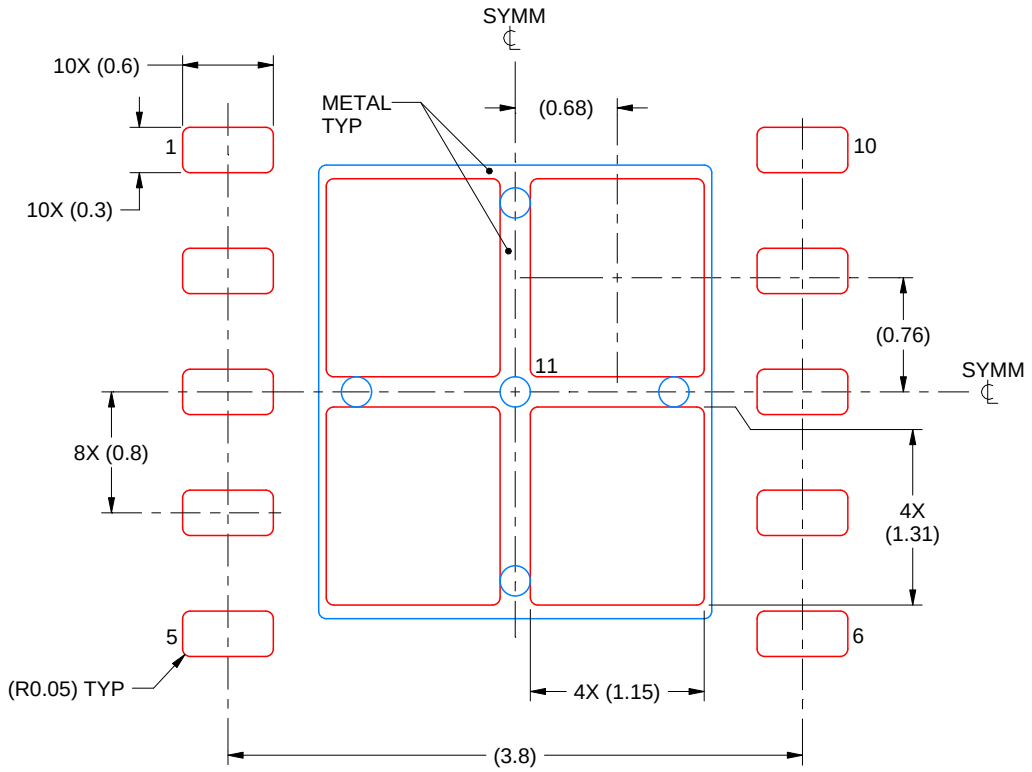


SOLDER MASK DETAILS

4218856/B 01/2021

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 11:
77% PRINTED SOLDER COVERAGE BY AREA
SCALE:20X

4218856/B 01/2021

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

重要なお知らせと免責事項

TI は、技術データと信頼性データ (データシートを含みます)、設計リソース (リファレンス デザインを含みます)、アプリケーションや設計に関する各種アドバイス、Web ツール、安全性情報、その他のリソースを、欠陥が存在する可能性のある「現状のまま」提供しており、商品性および特定目的に対する適合性の黙示保証、第三者の知的財産権の非侵害保証を含むいかなる保証も、明示的または黙示的にかかわらず拒否します。

これらのリソースは、TI 製品を使用する設計の経験を積んだ開発者への提供を意図したものです。(1) お客様のアプリケーションに適した TI 製品の選定、(2) お客様のアプリケーションの設計、検証、試験、(3) お客様のアプリケーションに該当する各種規格や、その他のあらゆる安全性、セキュリティ、規制、または他の要件への確実な適合に関する責任を、お客様のみが単独で負うものとします。

上記の各種リソースは、予告なく変更される可能性があります。これらのリソースは、リソースで説明されている TI 製品を使用するアプリケーションの開発の目的でのみ、TI はその使用をお客様に許諾します。これらのリソースに関して、他の目的で複製することや掲載することは禁止されています。TI や第三者の知的財産権のライセンスが付与されている訳ではありません。お客様は、これらのリソースを自身で使用した結果発生するあらゆる申し立て、損害、費用、損失、責任について、TI およびその代理人を完全に補償するものとし、TI は一切の責任を拒否します。

TI の製品は、 TI の販売条件 、 TI の総合的な品質ガイドライン 、 ti.com または TI 製品などに関連して提供される他の適用条件に従い提供されます。TI がこれらのリソースを提供することは、適用される TI の保証または他の保証の放棄の拡大や変更を意味するものではありません。 TI がカスタム、またはカスタマー仕様として明示的に指定していない限り、TI の製品は標準的なカタログに掲載される汎用機器です。

お客様がいかなる追加条項または代替条項を提案する場合も、TI はそれらに異議を唱え、拒否します。

Copyright © 2026, Texas Instruments Incorporated

最終更新日：2025 年 10 月