TEXAS INSTRUMENTS

LM5025A

JAJSA81F – DECEMBER 2004 – REVISED AUGUST 2016

LM5025A アクティブ・クランプ電圧モードPWMコントローラ

1 特長

- スタートアップ用バイアス・レギュレータを内蔵
- 3Aの複合型メイン・ゲート・ドライバ
- プログラマブルなライン低電圧誤動作防止(UVLO)、ヒステリシスを調整可能
- 電圧モード制御、フィードフォワード付き
- 可変のデュアル・モード過電流保護
- メイン出力とアクティブ・クランプ出力との間でオーバーラップまたはデッドタイムをプログラム可能
- ボルト秒クランプ
- プログラム可能なソフト・スタート
- リーディング・エッジ・ブランキング
- 単一の抵抗でプログラマブルな発振器
- 発振器のアップ/ダウン同期機能
- 高精度の5V基準電圧
- サーマル・シャットダウン
- パッケージ:
  - 16ピンTSSOP
  - 放熱特性の優れた16ピン WSON (5mm×5mm)

2 アプリケーション

- サーバー電源
- 48Vテレコム電源
- 42V車載用途
- 高効率のDC/DC電源

3 概要

LM5025Aは、LM5025アクティブ・クランプPWMコントローラの機能バリアントです。LM5025Aの機能的な相違点は、CS1およびCS2電流制限スレッショルドが0.5Vに引き上げられ、内部のCS2フィルタ放電デバイスがディセーブルされて、毎クロック・サイクル動作せず、ラインのUVLOピンがスレッショルド未満のときは内部のV_{CC}およびV_{REF}レギュレータが引き続き動作することです。

LM5025A PWMコントローラには、アクティブ・クランプ/リセット技法を使用して電力コンバータを実装するために必要なすべての機能が含まれています。アクティブ・クランプ技法により、従来のキャッチ巻線やRDCクランプ/リセット技法と比べて、より高い効率と大きな電力密度を実現できます。制御出力として、メイン電源スイッチ制御(OUT_A)とアクティブ・クランプ・スイッチ制御(OUT_B)の2つが搭載されています。2つの内蔵複合型ゲート・ドライバはMOSデバイスとバイポーラ・デバイスを並列に接続しており、優れたゲート駆動特性が得られます。このコントローラは、発振器の周波数範囲が最大1MHz、PWMおよび電流センスの合計伝搬遅延が100ns未満の高速動作用に設計されています。LM5025Aには、高電圧のスタートアップ・レギュレータが内蔵されており、13V～90Vの広い範囲の入力電圧で動作します。追加機能として、低電圧誤動作防止(UVLO)、ソフトスタート、発振器のアップ/ダウン同期機能、高精度の基準電圧、サーマル・シャットダウン機能があります。

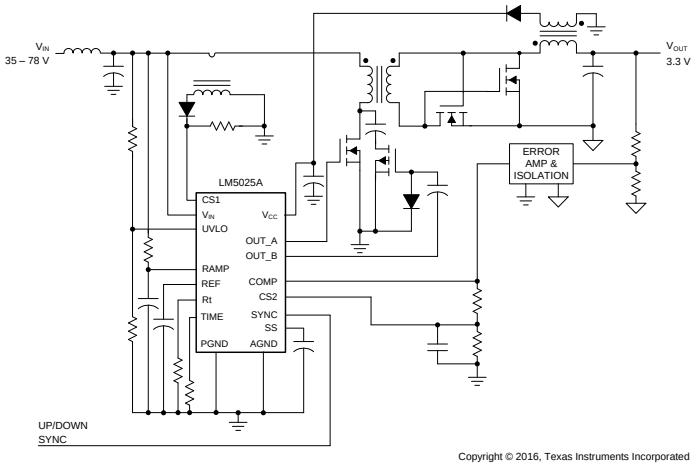
製品情報(1)

型番	パッケージ	本体サイズ(公称)
LM5025A	TSSOP (16)	5.00mm×4.40mm
	WSON (16)	5.00mm×5.00mm

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。

英語版のTI製品についての情報を翻訳したこの資料は、製品の概要を確認する目的で便宜的に提供しているものです。該当する正式な英語版の最新情報は、www.ti.comで閲覧でき、その内容が常に優先されます。TIでは翻訳の正確性および妥当性につきましては一切保証いたしません。実際の設計などの前には、必ず最新版の英語版をご参照くださいますようお願いいたします。

アクティブ・クランプ・フォワード電力コンバータの概略回路図



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4 改訂履歴

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Revision E (March 2013) から **Revision F** に変更 **Page**

- 「*ESD定格*」表、「*機能説明*」セクション、「*デバイスの機能モード*」セクション、「*アプリケーションと実装*」セクション、「*電源に関する推奨事項*」セクション、「*レイアウト*」セクション、「*デバイスおよびドキュメントのサポート*」セクション、「*メカニカル、パッケージ、および注文情報*」セクション 追加 ... 1
- Changed *Thermal Information* table ... 6
- Deleted the THERMAL RESISTANCE row from *Electrical Characteristics* ... 9

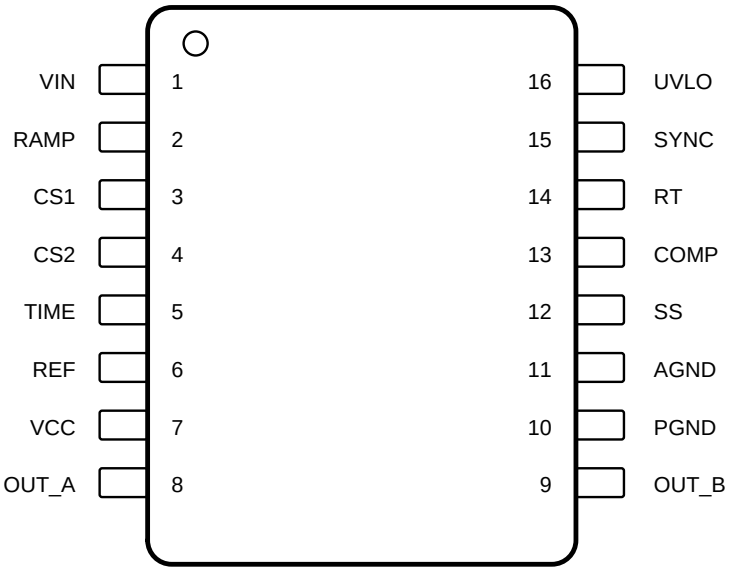
Revision D (March 2013) から **Revision E** に変更 **Page**

- Changed layout of National Semiconductor Data Sheet to TI format ... 19

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5 Pin Configuration and Functions

PW or NHQ Packages
16-Pin TSSOP or WSON
Top View



Not to scale

Pin Functions

PIN		I/O	DESCRIPTION	APPLICATION INFORMATION
NO.	NAME			
1	V_{IN}	I	Source input voltage	Input to start-up regulator. Input range 13 V to 90 V, with transient capability to 105 V.
2	RAMP	I	Modulator ramp signal	An external RC circuit from Vin sets the ramp slope. This pin is discharged at the conclusion of every cycle by an internal FET, initiated by either the internal clock or the V × Sec Clamp comparator.
3	CS1	I	Current sense input for cycle-by-cycle limiting	If CS1 exceeds 0.5 V the outputs goes into Cycle-by-Cycle current limit. CS1 is held low for 50 ns after OUT_A switches high providing leading edge blanking.
4	CS2	I	Current sense input for soft restart	If CS2 exceeds 0.5 V, the outputs will be disabled and a soft start commenced. The soft-start capacitor will be fully discharged and then released with a pullup current of 1 µA. After the first output pulse (when SS =1 V), the SS charge current will revert back to 20 µA.
5	TIME	I	Output overlap and dead-time control	An external resistor (R_{SET}) sets either the overlap time or dead time for the active clamp output. An R_{SET} resistor connected between TIME and GND produces in-phase OUT_A and OUT_B pulses with overlap. An R_{SET} resistor connected between TIME and REF produces out-of-phase OUT_A and OUT_B pulses with dead time.
6	REF	O	Precision 5-V reference output	Maximum output current: 10-mA locally decouple with a 0.1-µF capacitor. Reference stays low until the V_{CC} UV comparator is satisfied.
7	V_{CC}	P	Output from the internal high voltage start-up regulator. The V_{CC} voltage is regulated to 7.6 V.	If an auxiliary winding raises the voltage on this pin above the regulation setpoint, the internal start-up regulator shuts down, reducing the IC power dissipation.
8	OUT_A	O	Main output driver	Output of the main switch PWM output gate driver. Output capability of 3-A peak sink current.

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Pin Functions (continued)

PIN		I/O	DESCRIPTION	APPLICATION INFORMATION
NO.	NAME			
9	OUT_B	O	Active Clamp output driver	Output of the Active Clamp switch gate driver. Capable of 1.25-A peak sink current..
10	PGND	G	Power ground	Connect directly to analog ground.
11	AGND	G	Analog ground	Connect directly to power ground. For the WSON package option, the exposed pad is electrically connected to AGND.
12	SS	I	Soft-start control	An external capacitor and an internal 20-μA current source set the soft-start ramp. The SS current source is reduced to 1 μA initially following a CS2 overcurrent event or an overtemperature event.
13	COMP	I	Input to the Pulse Width Modulator	An internal 5-kΩ resistor pullup is provided on this pin. The external opto-coupler sinks current from COMP to control the PWM duty cycle.
14	RT	I	Oscillator timing resistor pin	An external resistor connected from RT to ground sets the internal oscillator frequency.
15	SYNC	I	Oscillator UP and DOWN synchronization input	The internal oscillator can be synchronized to an external clock with a frequency 20% lower than the internal oscillator's free running frequency. There is no constraint on the maximum sync frequency.
16	UVLO	I	Line undervoltage shutdown	An external voltage divider from the power source sets the shutdown comparator levels. The comparator threshold is 2.5 V. Hysteresis is set by an internal current source (20 μA) that is switched ON or OFF as the UVLO pin potential crosses the 2.5-V threshold.
—	EP	G	Exposed pad, underside of the WSON package option	Internally bonded to the die substrate. Connect to GND potential for low thermal impedance.

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)(2)

	MIN	MAX	UNIT
V_{IN} to GND	–0.3	105	V
V_{CC} to GND	–0.3	16	V
CS1, CS2 to GND	–0.3	1	V
All other inputs to GND	–0.3	7	V
Junction temperature, T_J		150	°C
Storage temperature, T_{stg}	–55	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) If Military/Aerospace specified devices are required, please contact the TI Sales Office/ Distributors for availability and specifications.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM)(1)	±2000	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	MAX	UNIT
V_{IN} voltage	13	90	V
External voltage applied to V_{CC}	8	15	V
Operating junction temperature	–40	125	°C

6.4 Thermal Information

THERMAL METRIC(1)		LM5025A		UNIT
		PW (TSSOP)	NHQ (WSON)	
		16 PINS	16 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	98.7	30	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	27.8	25.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	44.3	9.3	°C/W
ψ_{JT}	Junction-to-top characterization parameter	1.2	0.2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	43.6	9.5	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	—	2.3	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

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6.5 Electrical Characteristics

Typical limits are for T_J = 25°C, and minimum and maximum limits apply over the operating junction temperature range (–40°C to 125°C). V_{IN} = 48 V, V_{CC} = 10 V, RT = 31.3 kΩ, R_{SET} = 27.4 kΩ) unless otherwise stated (1)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
START-UP REGULATOR							
V_{CC} Reg	V_{CC} regulation	No load	T_J = 25°C		7.6		V
			T_J = T_{low} to T_{high}	7.3		7.9	
	V_{CC} current limit	See (2)	T_J = 25°C		25		mA
			T_J = T_{low} to T_{high}	20			
I-V_{IN}	Start-up regulator leakage (external Vcc Supply)	V_{IN} = 100 V	T_J = 25°C		165		µA
			T_J = T_{low} to T_{high}			500	
V_{CC} SUPPLY							
	V_{CC} undervoltage lockout voltage (positive going V_{cc})	T_J = 25°C			V_{CC} Reg - 120 mV		V
		T_J = T_{low} to T_{high}		V_{CC} Reg - 220 mV			
	V_{CC} undervoltage hysteresis	T_J = 25°C			1.5		V
		T_J = T_{low} to T_{high}		1		2	
	V_{CC} supply current (I_{CC})	C_{gate} = 0	T_J = T_{low} to T_{high}			4.2	mA
REFERENCE SUPPLY							
V_{REF}	Ref voltage	I_{REF} = 0 mA	T_J = 25°C		5		V
			T_J = T_{low} to T_{high}	4.85		5.15	
	Ref voltage regulation	I_{REF} = 0 to 10mA	T_J = 25°C		25		mV
			T_J = T_{low} to T_{high}			50	
	Ref current limit	T_J = 25°C			20		mA
		T_J = T_{low} to T_{high}		10			
CURRENT LIMIT							
CS1 Prop	CS1 delay to output	CS1 Step from 0 to 0.6 V, Time to onset of OUT Transition (90%), C_{gate} = 0			40		ns
CS2 Prop	CS2 delay to output	CS2 Step from 0 to 0.6 V, Time to onset of OUT Transition (90%), C_{gate} = 0			50		ns
	Cycle by cycle threshold voltage (CS1)	T_J = 25°C			0.5		V
		over full operating junction temperature		0.45		0.55	
	Cycle skip threshold voltage (CS2)	Resets SS capacitor; auto restart	T_J = 25°C		0.5		V
			T_J = T_{low} to T_{high}	0.45		0.55	
	Leading edge blanking time (CS1)				50		ns
	CS1 sink impedance (clocked)	CS1 = 0.4 V	T_J = 25°C		30		Ω
			T_J = T_{low} to T_{high}			50	
	CS1 sink impedance (post fault discharge)	CS1 = 0.6 V	T_J = 25°C		15		Ω
			T_J = T_{low} to T_{high}			30	
	CS2 sink impedance (post fault discharge)	CS2 = 0.6 V	T_J = 25°C		55		Ω
			T_J = T_{low} to T_{high}			95	
	CS1 and CS2 leakage current	CS = CS Threshold – 100 mV	T_J = T_{low} to T_{high}			1	µA

(1) All electrical characteristics having room temperature limits are tested during production with T_A = T_J = 25°C. All hot and cold limits are specified by correlating the electrical characteristics to process and temperature variations and applying statistical process control.
(2) Device thermal limitations may limit usable range.

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Electrical Characteristics (continued)

Typical limits are for T_J = 25°C, and minimum and maximum limits apply over the operating junction temperature range (–40°C to 125°C). V_{IN} = 48 V, V_{CC} = 10 V, RT = 31.3 kΩ, R_{SET} = 27.4 kΩ) unless otherwise stated (1)

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
SOFT-START						
Soft-start current source normal	T_J = 25°C			22		µA
	over full operating junction temperature		17		27	
Soft-start current source following a CS2 event	T_J = 25°C			1		µA
	over full operating junction temperature		0.5		1.5	
OSCILLATOR						
Frequency1	T_A = 25°C,		180	200	220	kHz
	$T_J = T_{low}$ to T_{high}		175		225	
Frequency2	RT = 10.4 kΩ	T_A = 25°C,		580		kHz
		$T_J = T_{low}$ to T_{high}	510		650	
Sync threshold				2		V
Min sync pulse width	$T_J = T_{low}$ to T_{high}				100	ns
Sync frequency range	$T_J = T_{low}$ to T_{high}		160			kHz
PWM COMPARATOR						
Delay to output	COMP step 5 V to 0 V, Time to onset of OUT_A transition low			40		ns
Duty cycle range	$T_J = T_{low}$ to T_{high}		0%		80%	
COMP to PWM offset	T_A = 25°C,			1		V
	$T_J = T_{low}$ to T_{high}		0.7		1.3	
COMP open-circuit voltage	$T_J = T_{low}$ to T_{high}		4.3		5.9	V
COMP short-circuit current	COMP = 0 V	T_A = 25°C,		1		mA
		$T_J = T_{low}$ to T_{high}	0.6		1.4	
VOLT × SECOND CLAMP						
Ramp clamp level	Delta RAMP measured from onset of OUT_A to Ramp peak, COMP = 5 V	T_A = 25°C,		2.5		V
		$T_J = T_{low}$ to T_{high}	2.4		2.6	
UVLO SHUTDOWN						
Undervoltage shutdown threshold	T_A = 25°C,			2.5		V
	$T_J = T_{low}$ to T_{high}		2.44		2.56	
Undervoltage shutdown hysteresis	T_A = 25°C,			20		µA
	$T_J = T_{low}$ to T_{high}		16		24	
OUTPUT SECTION						
OUT_A high saturation	MOS device at Iout = –10 mA	T_A = 25°C,		5		Ω
		$T_J = T_{low}$ to T_{high}			10	
OUTPUT_A peak current sink	Bipolar Device at Vcc/2			3		A
OUT_A low saturation	MOS device at Iout = 10 mA	T_A = 25°C,		6		Ω
		$T_J = T_{low}$ to T_{high}			9	
OUTPUT_A rise time	C_{gate} = 2.2 nF			20		ns
OUTPUT_A fall time	C_{gate} = 2.2 nF			15		ns
OUT_B high saturation	MOS device at Iout = –10 mA	T_A = 25°C,		10		Ω
		$T_J = T_{low}$ to T_{high}			20	
OUTPUT_B peak current sink	Bipolar device at Vcc/2			1		A

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Electrical Characteristics (continued)

Typical limits are for T_J = 25°C, and minimum and maximum limits apply over the operating junction temperature range (–40°C to 125°C). V_{IN} = 48 V, V_{CC} = 10 V, RT = 31.3 kΩ, R_{SET} = 27.4 kΩ) unless otherwise stated (1)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
	OUT_B low saturation	MOS device at Iout = 10 mA	T_A = 25°C,		12		Ω
			$T_J = T_{low}$ to T_{high}			18	
	OUTPUT_B rise time	C_{gate} = 1 nF			20		ns
	OUTPUT_B fall time	C_{gate} = 1 nF			15		ns
OUTPUT TIMING CONTROL							
	Overlap time	R_{SET} = 38 kΩ connected to GND, 50% to 50% transitions	T_A = 25°C,		105		ns
			$T_J = T_{low}$ to T_{high}	75		135	
	Dead time	R_{SET} = 29.5 kΩ connected to REF, 50% to 50% transitions	T_A = 25°C,		105		ns
			$T_J = T_{low}$ to T_{high}	75		135	
THERMAL SHUTDOWN							
T_{SD}	Thermal shutdown threshold				165		°C
	Thermal shutdown hysteresis				25		°C

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6.6 Typical Characteristics

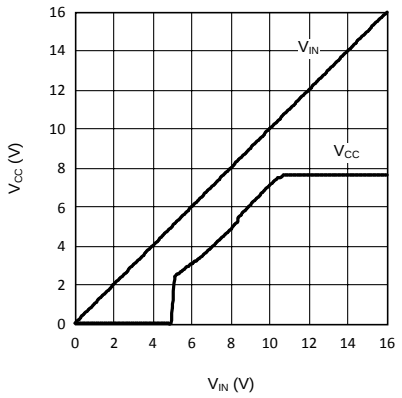


Figure 1. V_{CC} Regulator Start-Up Characteristics, V_{CC} vs V_{IN}

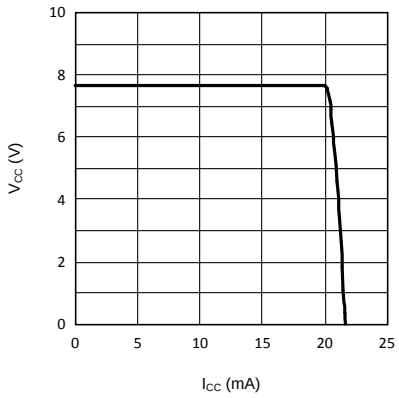


Figure 2. V_{CC} vs I_{CC}

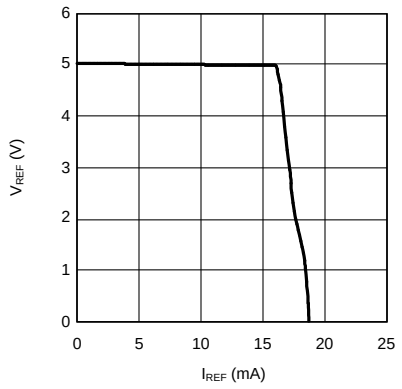


Figure 3. V_{REF} vs I_{REF}

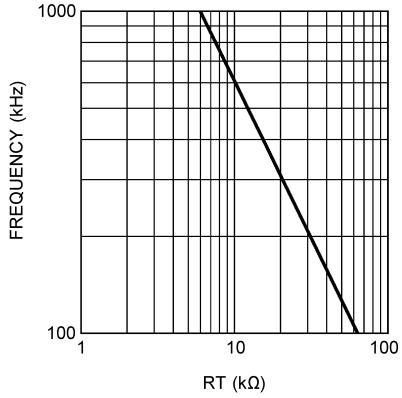


Figure 4. Oscillator Frequency vs RT

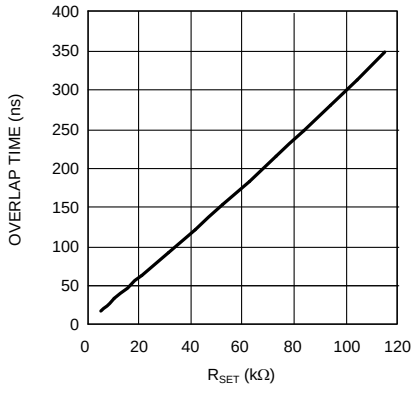
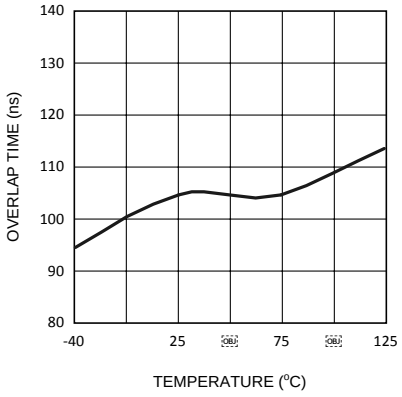


Figure 5. Overlap Time vs R_{SET}



R_{SET} = 38 K

Figure 6. Overlap Time vs Temperature

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Typical Characteristics (continued)

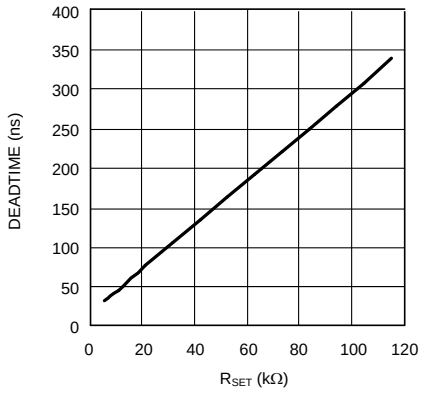
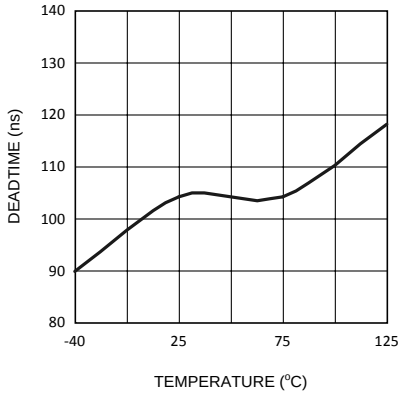


Figure 7. Dead Time vs R_{SET}



R_{SET} = 29.5 K

Figure 8. Dead Time vs Temperature

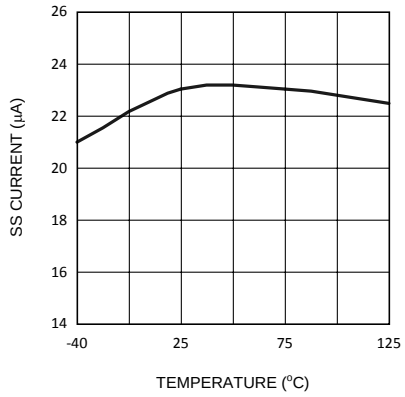


Figure 9. SS Pin Current vs Temperature

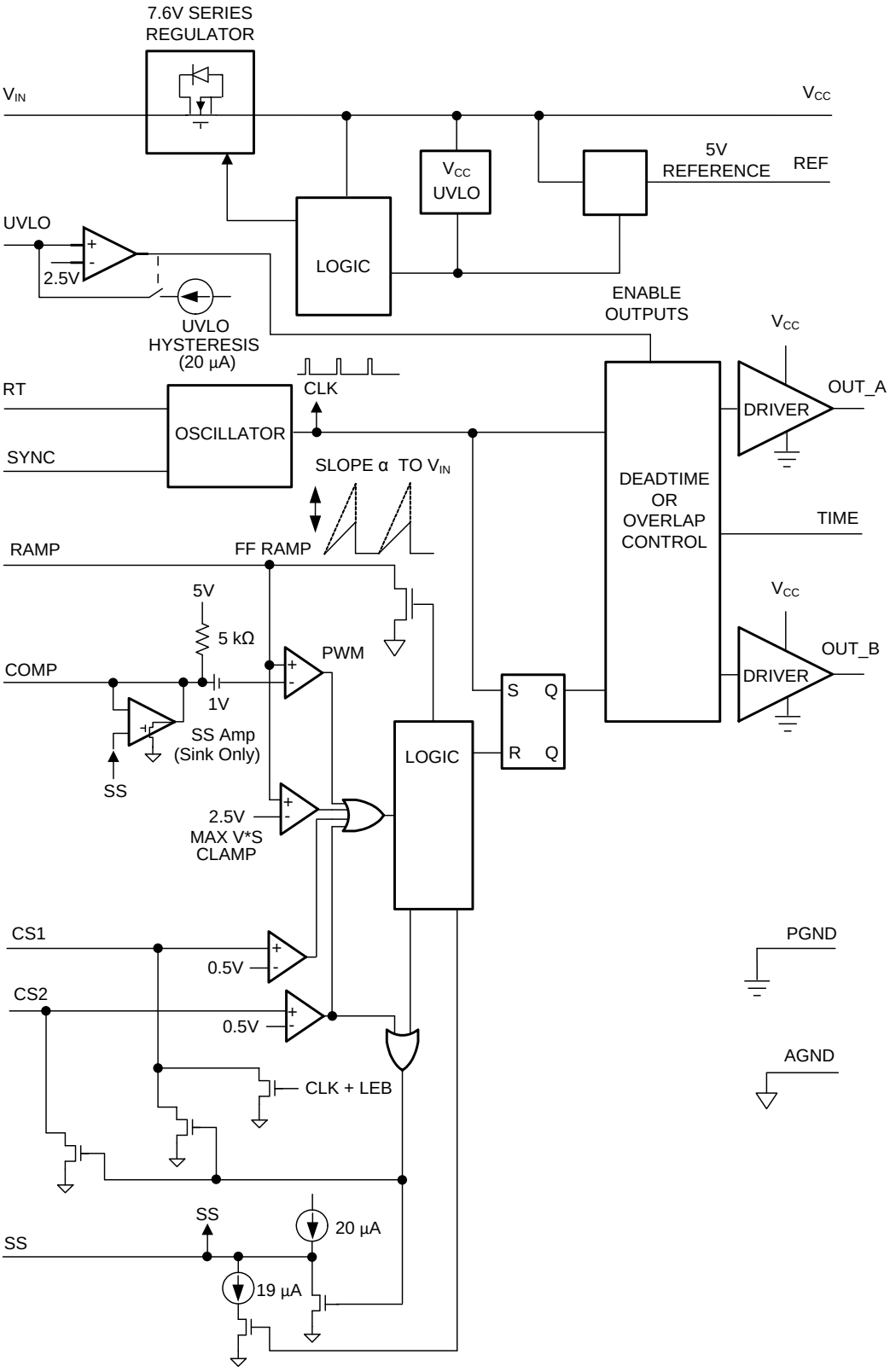
7 Detailed Description

7.1 Overview

The LM5025A PWM controller contains all of the features necessary to implement active clamp / reset technique voltage-mode controlled power converters. Synchronous rectification allows higher conversion efficiency and greater power density than conventional PN or Schottky rectifier techniques. The high voltage start-up regulator of the LM5025A can be configured to operate with input voltages ranging from 13 V to 90 V. Additional features include line undervoltage lockout, cycle-by-cycle current limit, voltage feed-forward compensation, hiccup mode fault protection with adjustable delays, soft-start, a 1-MHz capable oscillator with synchronization capability, precision reference, and thermal shutdown. These features simplify the design of active voltage-mode active clamp / reset DC-DC power converters.

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7.2 Functional Block Diagram



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7.3 Feature Description

7.3.1 High-Voltage Start-Up Regulator

The LM5025A contains an internal high-voltage start-up regulator that allows the input pin (V_{IN}) to be connected directly to the line voltage. The regulator output is internally current-limited to 20 mA. When power is applied, the regulator is enabled and sources current into an external capacitor connected to the V_{CC} pin. The recommended capacitance range for the V_{CC} regulator is 0.1 µF to 100 µF. When the voltage on the V_{CC} pin reaches the regulation point of 7.6 V and the internal voltage reference (REF) reaches its regulation point of 5 V, the controller outputs are enabled. The outputs remain enabled until V_{CC} falls below 6.2 V or the line undervoltage lockout detector indicates that V_{IN} is out of range. In typical applications, an auxiliary transformer winding is connected through a diode to the V_{CC} pin. This winding must raise the V_{CC} voltage above 8 V to shut off the internal start-up regulator. Powering V_{CC} from an auxiliary winding improves efficiency while reducing the controller power dissipation.

When the converter auxiliary winding is inactive, external current draw on the V_{CC} line must be limited so the power dissipated in the start-up regulator does not exceed the maximum power dissipation of the controller.

An external start-up regulator or other bias rail can be used instead of the internal start-up regulator by connecting the V_{CC} and the V_{IN} pins together and feeding the external bias voltage into the two pins.

7.3.2 Line Undervoltage Detector

The LM5025A contains a line undervoltage lockout (UVLO) circuit. An external setpoint voltage divider from V_{IN} to GND, sets the operational range of the converter. The divider must be designed such that the voltage at the UVLO pin is greater than 2.5 V when V_{IN} is in the desired operating range. If the undervoltage threshold is not met, both outputs are disabled, all other functions of the controller remain active. UVLO hysteresis is accomplished with an internal 20-µA current source that is switched ON or OFF into the impedance of the setpoint divider. When the UVLO threshold is exceeded, the current source is activated to instantly raise the voltage at the UVLO pin. When the UVLO pin voltage falls below the 2.5-V threshold, the current source is turned off, causing the voltage at the UVLO pin to fall. The UVLO pin can also be used to implement a remote enable and disable function. Pulling the UVLO pin below the 2.5-V threshold disables the PWM outputs.

7.3.3 PWM Outputs

The relative phase of the main (OUT_A) and active clamp outputs (OUT_B) can be configured for the specific application. For active clamp configurations using a ground-referenced P-channel clamp switch, the two outputs must be in-phase with the active clamp output overlapping the main output. For active clamp configurations using a high-side N-channel switch, the active clamp output must be out-of-phase with main output, and there must be a dead time between the two gate drive pulses. A distinguishing feature of the LM5025A is the ability to accurately configure either dead time (both OFF) or overlap time (both ON) of the gate driver outputs. The overlap and dead-time magnitude is controlled by the resistor value connected to the TIME pin of the controller. The opposite end of the resistor can be connected to either REF for dead-time control or GND for overlap control. The internal configuration detector senses the connection and configures the phase relationship of the main and active clamp outputs. The magnitude of the overlap and dead time can be calculated in Equation 1 and Equation 2.

$$\text{Overlap Time (ns)} = 2.8 \times R_{SET} - 1.2 \quad (1)$$

$$\text{Dead Time (ns)} = 2.9 \times R_{SET} + 20$$

where

- R_{SET} in kΩ
- Time in ns (2)

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Feature Description (continued)

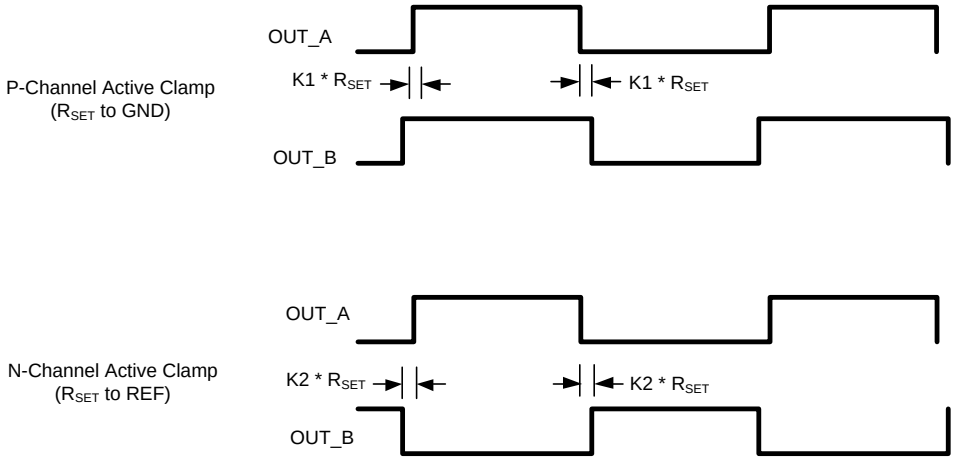


Figure 10. PWM Outputs

7.3.4 Compound Gate Drivers

The LM5025A contains two unique compound gate drivers, which parallel both MOS and Bipolar devices to provide high-drive current throughout the entire switching event. The bipolar device provides most of the drive current capability and provides a relatively constant sink current which is ideal for driving large power MOSFETs. As the switching event nears conclusion and the bipolar device saturates, the internal MOS device continues to provide a low impedance to compete the switching event.

During turnoff at the Miller plateau region, typically around 2 V to 3 V, is where gate driver current capability is needed most. The resistive characteristics of all MOS gate drivers are adequate for turnon because the supply to output voltage differential is fairly large at the Miller region. During turnoff however, the voltage differential is small and the current source characteristic of the bipolar gate driver is beneficial to provide fast drive capability.

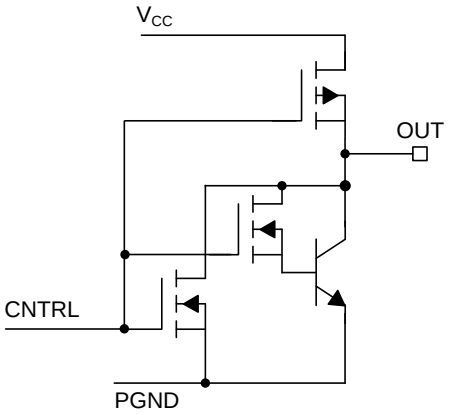


Figure 11. Compound Gate Drivers

7.3.5 PWM Comparator

The PWM comparator compares the ramp signal (RAMP) to the loop error signal (COMP). This comparator is optimized for speed to achieve minimum controllable duty cycles. The internal 5-kΩ pullup resistor, connected between the internal 5-V reference and COMP, can be used as the pullup for an optocoupler. The comparator polarity is such that 0 V on the COMP pin produces a zero duty cycle on both gate driver outputs.

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Feature Description (continued)

7.3.6 Volt Second Clamp

The Volt × Second Clamp comparator compares the ramp signal (RAMP) to a fixed 2.5-V reference. By proper selection of RFF and CFF, the maximum ON-time of the main switch can be set to the desired duration. The ON-time set by Volt × Second Clamp varies inversely with the line voltage because the RAMP capacitor is charged by a resistor connected to V_{IN} while the threshold of the clamp is a fixed voltage (2.5 V). An example illustrates the use of the Volt × Second Clamp comparator to achieve a 50% duty cycle limit, at 200 KHz, at a 48-V line input: A 50% duty cycle at a 200 KHz requires a 2.5 µs of ON-time. At 48-V input the Volt × Second product is 120 V × µs (48 V × 2.5 µs). To achieve this clamp level, use Equation 3 and Equation 4:

$$R_{FF} \times C_{FF} = V_{IN} \times T_{ON} / 2.5\ V \quad (3)$$

$$48 \times 2.5\ \mu / 2.5 = 48\ \mu \quad (4)$$

Select C_{FF} = 470 pF

R_{FF} = 102 kΩ

The recommended capacitor value range for CFF is 100 pF to 1000 pF.

The C_{FF} ramp capacitor is discharged at the conclusion of every cycle by an internal discharge switch controlled by either the internal clock or by the V × S Clamp comparator, whichever event occurs first.

7.3.7 Current Limit

The LM5025A contains two modes of overcurrent protection. If the sense voltage at the CS1 input exceeds 0.5 V the present power cycle is terminated (cycle-by-cycle current limit). If the sense voltage at the CS2 input exceeds 0.5 V, the controller terminates the present cycle, discharge the soft-start capacitor and reduce the soft-start current source to 1 µA. The soft-start (SS) capacitor is released after being fully discharged and slowly charges with a 1-µA current source. When the voltage at the SS pin reaches approximately 1 V, the PWM comparator produces the first output pulse at OUT_A. After the first pulse occurs, the soft-start current source reverts to the normal 20-µA level. Fully discharging and then slowly charging the SS capacitor protects a continuously overloaded converter with a low duty cycle hiccup mode.

These two modes of overcurrent protection allow the user great flexibility to configure the system behavior in over-load conditions. If it is desired for the system to act as a current source during an overload, then the CS1 cycle-by-cycle current limiting must be used. In this case the current sense signal must be applied to the CS1 input and the CS2 input must be grounded. If during an overload condition it is desired for the system to briefly shutdown, followed by soft-start retry, then the CS2 hiccup current limiting mode must be used. In this case the current sense signal must be applied to the CS2 input and the CS1 input must be grounded. This shutdown and soft-start retry repeats indefinitely while the overload condition remains. The hiccup mode greatly reduces the thermal stresses to the system during heavy overloads. The cycle-by-cycle mode has higher system thermal dissipations during heavy overloads, but provides the advantage of continuous operation for short duration overload conditions.

It is possible to use both overcurrent modes concurrently, whereby slight overload conditions activate the CS1 cycle-by-cycle mode while more severe overloading activates the CS2 hiccup mode. Generally the CS1 input is always configured to monitor the main switch FET current each cycle. The CS2 input can be configured in several different ways depending upon the system requirements.

- The CS2 input can also be set to monitor the main switch FET current except scaled to a higher threshold than CS1
- An external overcurrent timer can be configured which trips after a predetermined overcurrent time, driving the CS2 input high, initiating a hiccup event.
- In a closed-loop voltage regulaton system, the COMP input rises to saturation when the cycle-by-cycle current limit is active. An external filter and delay timer and voltage divider can be configured between the COMP pin and the CS2 pin to scale and delay the COMP voltage. If the CS2 pin voltage reaches 0.5 V a hiccup event will initiate.

TI recommends a small RC filter placed near the controller for each of the CS pins. The CS1 input has an internal FET which discharges the current sense filter capacitor at the conclusion of every cycle, to improve dynamic performance. This same FET remains on an additional 50 ns at the start of each main switch cycle to attenuate the leading edge spike in the current sense signal. The CS2 discharge FET only operates following a CS2 event, UVLO, and thermal shutdown.

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Feature Description (continued)

The LM5025A CS comparators are very fast and may respond to short duration noise pulses. Layout considerations are critical for the current sense filter and sense resistor. The capacitor associated with the CS filter must be placed very close to the device and connected directly to the pins of the IC (CS and GND). If a current sense transformer is used, both leads of the transformer secondary must be routed to the filter network, which must be placed close to the IC. If a sense resistor in the source of the main switch MOSFET is used for current sensing, a low inductance type of resistor is required. When designing with a current sense resistor, all of the noise-sensitive, low-power ground connections must be connected together near the IC GND and a single connection must be made to the power ground (sense resistor ground point).



Figure 12. Current Limit

7.3.8 Oscillator and Sync Capability

The LM5025A oscillator is set by a single external resistor connected between the RT pin and GND. To set a desired oscillator frequency (F), the necessary RT resistor can be calculated in Equation 5:

$$RT = (5725/F)^{1.026} \quad (5)$$

where

- F is in kHz and RT in kΩ

The RT resistor must be placed very close to the device and connected directly to the pins of the IC (RT and GND).

A unique feature of LM5025A is the ability to synchronize the oscillator to an external clock with a frequency that is either higher or lower than the frequency of the internal oscillator. The lower frequency sync frequency range is 80% of the free-running internal oscillator frequency. There is no constraint on the maximum SYNC frequency. A minimum pulse width of 100 ns is required for the synchronization clock. If the synchronization feature is not required, the SYNC pin must be connected to GND to prevent any abnormal interference. The internal oscillator can be completely disabled by connecting the RT pin to REF. Once disabled, the sync signal acts directly as the master clock for the controller. Both the frequency and the maximum duty cycle of the PWM controller can be controlled by the SYNC signal (within the limitations of the Volt × Second Clamp). The maximum duty cycle (D) will be (1-D) of the SYNC signal.

7.3.9 Feed-Forward Ramp

An external resistor (R_{FF}) and capacitor (C_{FF}) connected to V_{IN} and GND are required to create the PWM ramp signal. The slope of the signal at the RAMP pin varies in proportion to the input line voltage. This varying slope provides line feedforward information necessary to improve line transient response with voltage mode control. The RAMP signal is compared to the error signal at the COMP pin by the pulse width modulator comparator to control the duty cycle of the main switch output. The Volt Second Clamp comparator also monitors the RAMP pin and if the ramp amplitude exceeds 2.5 V the present cycle is terminated. The ramp signal is reset to GND at the end of each cycle by either the internal clock or the Volt Second comparator, which ever occurs first.

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Feature Description (continued)

7.3.10 Soft Start

The soft-start feature allows the power converter to gradually reach the initial steady-state operating point, thus reducing start-up stresses and surges. At power on, a 20-µA current is sourced out of the soft-start pin (SS) into an external capacitor. The capacitor voltage ramps up slowly and limits the COMP pin voltage and therefore the PWM duty cycle. In the event of a fault as determined by V_{CC} undervoltage, line undervoltage (UVLO) or second level current limit, the output gate drivers are disabled, and the soft-start capacitor is fully discharged. When the fault condition is no longer present a soft-start sequence is initiated. Following a second level current limit detection (CS2), the soft-start current source is reduced to 1 µA until the first output pulse is generated by the PWM comparator. The current source returns to the nominal 20-µA level after the first output pulse (approximately 1 V at the SS pin).

7.4 Device Functional Modes

The LM5025A active clamp voltage mode PWM controller has six functional modes:

- UVLO Mode
- Soft-Start Mode
- Normal Operation Mode
- Cycle-by-Cycle Current Limit Mode
- Hiccup Mode
- Thermal Shut Down Mode

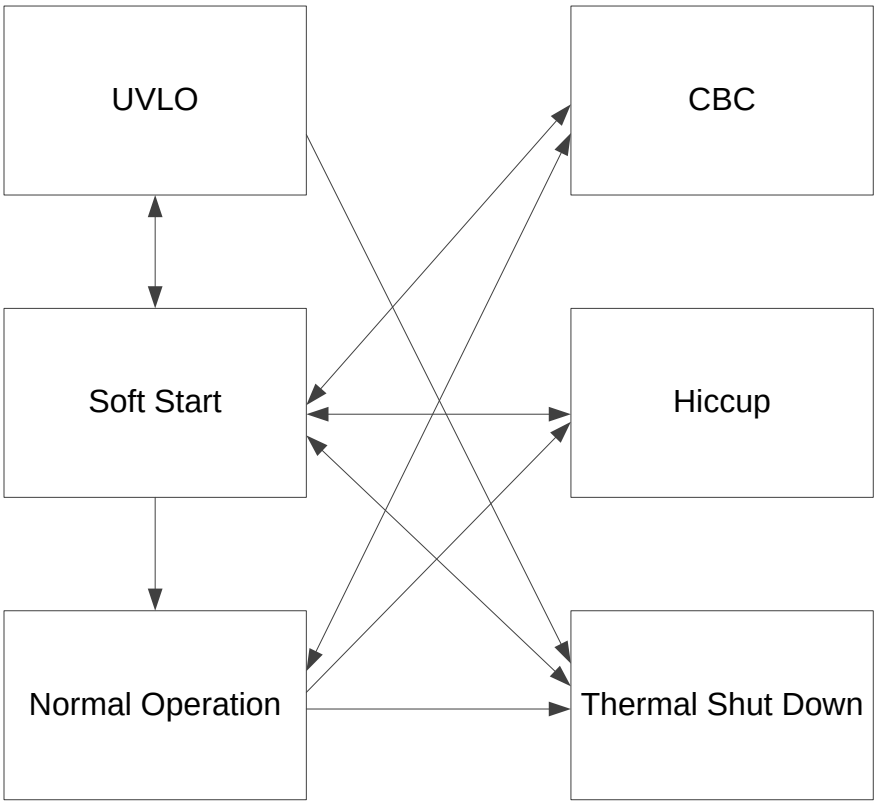


Figure 13. Functional Mode Transition Diagram

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8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The LM5025A PWM controller contains all of the features necessary to implement power converters using the active clamp and reset technique. This section provides design guidance for a typical active clamp forward converter design. An actual application schematic of a 36-V to 78-V input, 3.3-V, 30-A output active clamp forward converter is also provided in Figure 22.

8.2 Typical Application

Figure 14 shows a simplified schematic of an active clamp forward power converter.

Power converters based on the forward topology offer high-efficiency and good power-handling capability in applications up to several hundred Watts. The operation of the transformer in a forward topology does not inherently self-reset each power switching cycle, a mechanism to reset the transformer is required. The active clamp reset mechanism is presently finding extensive use in medium-level power converters in the range of 50 W to 200 W.

The forward converter is derived from the Buck topology family, employing a single modulating power switch. The main difference between the topologies is the forward topology employs a transformer to provide input and output ground isolation and a step-down or step-up function.

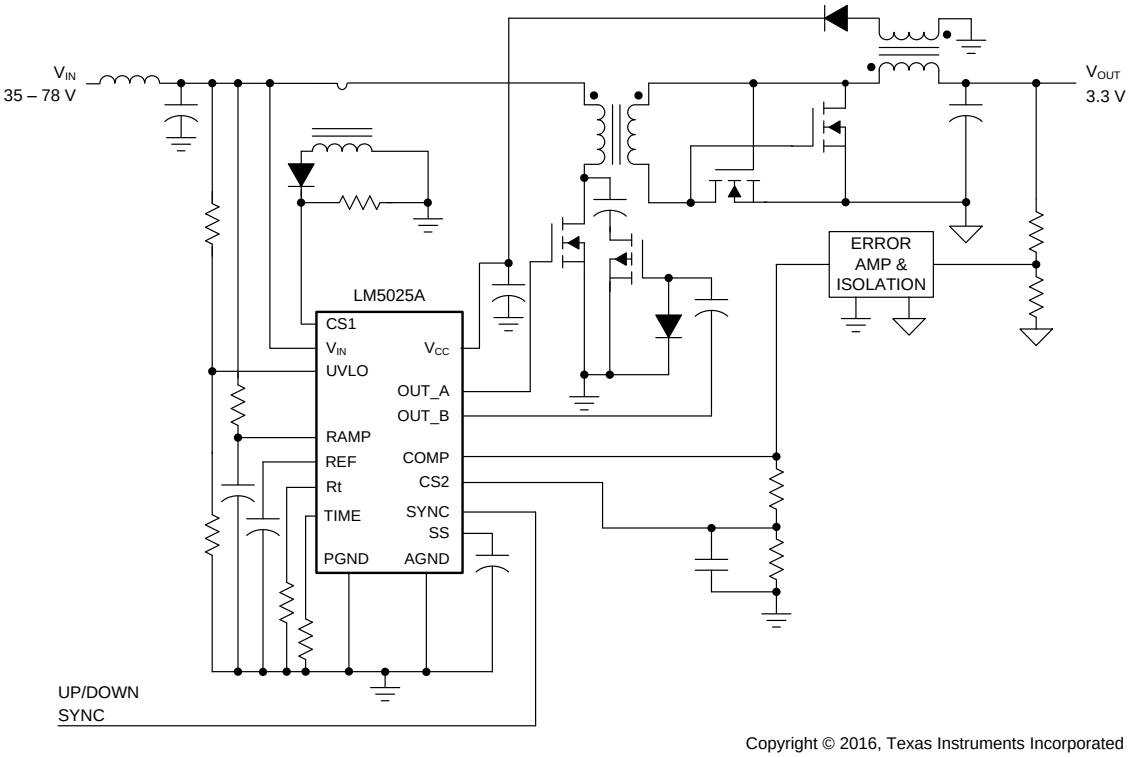
Each cycle, the main primary switch turns on and applies the input voltage across the primary winding. The transformer turns the voltage to a lower-level on the secondary side. The clamp capacitor along with the reset switch reverse biases the transformer primary each cycle when the main switch turns off. This reverse voltage resets the transformer. The clamp capacitor voltage is VIN / (1–D).

The secondary rectification employs self-driven synchronous rectification to maintain high-efficiency and ease of drive.

Feedback from the output is processed by an amplifier and reference, generating an error voltage, which is coupled back to the primary side control through an opto-coupler. The LM5025A voltage mode controller pulse width modulates the error signal with a ramp signal derived from the input voltage. Deriving the ramp signal slope from the input voltage provides line feedforward, which improves line transient rejection. The LM5025A also provides a controlled delay necessary for the reset switch.

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Typical Application (continued)



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Figure 14. Simplified Active Clamp Forward Power Converter

8.2.1 Design Requirements

This typical application provides an example of a fully-functional power converter based on the active clamp forward topology in an industry standard half-brick footprint.

The design requirements are:

- Input: 36 V to 78 V (100-V peak)
- Output voltage: 3.3 V
- Output current: 0 A to 30 A
- Measured efficiency: 90.5% at 30 A, 92.5% at 15 A
- Frequency of operation: 230 kHz
- Board size: 2.3 × 2.4 × 0.5 inches
- Load regulation: 1%
- Line regulation: 0.1%
- Line UVLO, hiccup current limit

8.2.2 Detailed Design Procedure

Before the controller design begins, the power stage design must be completed. This section describes the calculations needed to configure the LM5025A controller to meet the power stage design requirements.

8.2.2.1 Oscillator

The desired switching frequency F is set by a resistor connected between RT pin and ground. The resistance value R_T is calculated from Equation 6:

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Typical Application (continued)

$R_T = (5725/F)^{1.026}$

where

- F is in kHz and R_T in kΩ (6)

8.2.2.2 Soft-Start Ramp Time and Hiccup Interval

The soft-start ramp time and hiccup internal is programmed by a capacitor (C_{SS}) on the SS pin to ground. The soft-start ramp time is determined by comparing the SS pin voltage with COMP pin voltage. When the SS voltage is less than COMP voltage, the COMP voltage is clamped by SS voltage. The PWM duty is limited by the clamped COMP voltage, so that soft start can be achieved. The first PWM pulse is generated after COMP voltage reaches 1 V. So the soft-start ramp time of the output voltage can be estimated by Equation 7:

$$T_{SS}(ms) = C_{SS}(nF) \times \frac{V_{SS} - 1\,V}{20\,\mu A}$$

where

- V_{SS} is the steady-state COMP pin voltage. This voltage is determined by the output voltage, voltage divider, and the compensation network. (7)

In hiccup mode, the SS current source is reduced to 1 µA. When the first PWM pulse is generated, the current source switches to 20 µA, and the power supply tries to start up again. The hiccup interval can be calculated by Equation 8:

$$T_{hiccup}(ms) = C_{SS}(nF) \times \frac{1\,V}{1\,\mu A} \quad (8)$$

8.2.2.3 Feedforward Ramp and Maximum On-Time Clamp

An example illustrates the use of the Volt × Second Clamp comparator to achieve a 50% duty cycle limit, at 200 KHz, at a 48-V line input: A 50% duty cycle at a 200 KHz requires a 2.5 µs of ON-time. At 48-V input the Volt × Second product is 120 V × µs (48 V × 2.5 µs). To achieve this clamp level, see Equation 9 and Equation 10:

$R_{FF} \times C_{FF} = V_{IN} \times T_{ON} / 2.5\,V$ (9)

$48 \times 2.5\,\mu F / 2.5 = 48\,\mu F$ (10)

Select C_{FF} = 470 pF

R_{FF} = 102 kΩ

The recommended capacitor value range for C_{FF} is 100 pF to 1000 pF.

8.2.2.4 Dead Times

The magnitude of the overlap and dead time can be calculated as follows in Equation 11 and Equation 12:

Overlap Time (ns) = $2.8 \times R_{SET} - 1.2$ (11)

Dead Time (ns) = $2.9 \times R_{SET} + 20$

where

- R_{SET} in kΩ, Time in ns (12)

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Typical Application (continued)

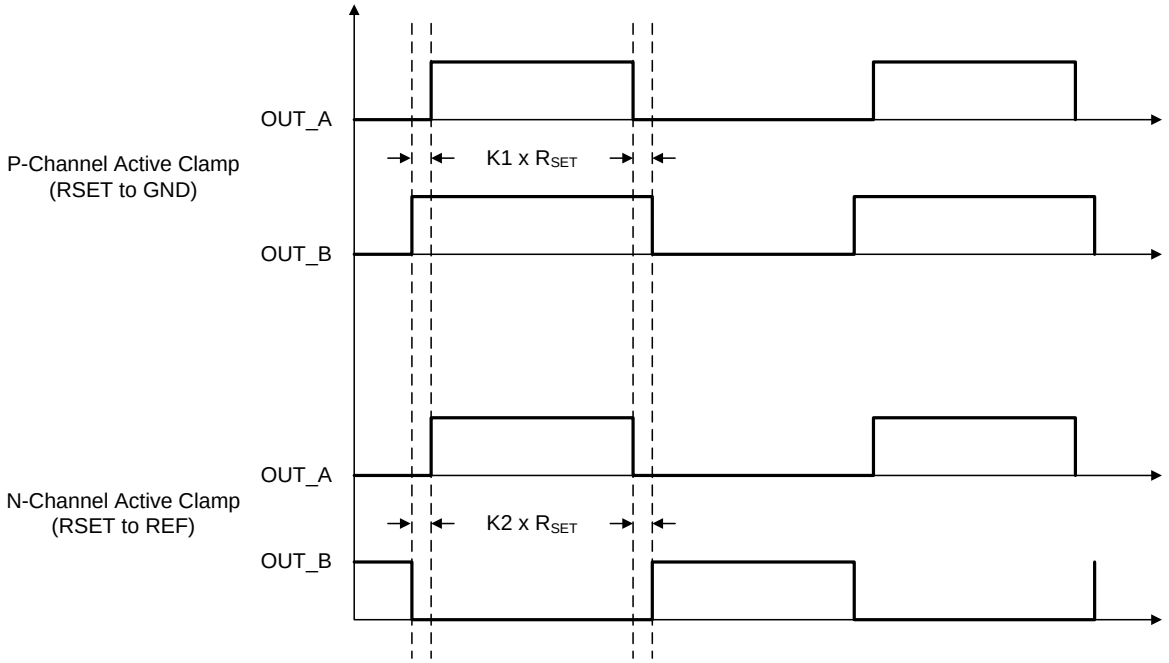
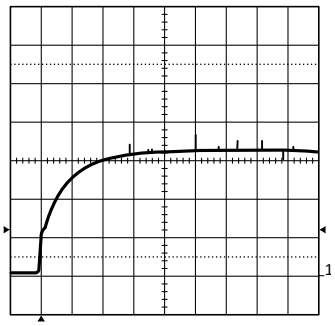


Figure 15. PWM Outputs

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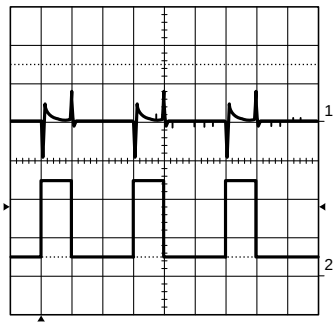
Typical Application (continued)

8.2.3 Application Curves



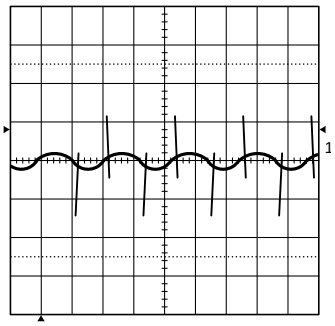
Conditions: input voltage = 48 VDC, output current = 5 A
Trace 1: output voltage Volts/div = 0.5 V
Horizontal resolution = 1 ms/div

Figure 16. Output Voltage During Typical Start-Up



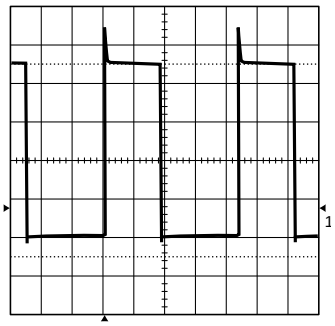
Conditions: input voltage = 48 VDC, output current = 5 A to 25 A
Trace 1: output voltage Volts/div = 0.5 V
Trace 2: output current, Amps/div = 10 A
Horizontal resolution = 1 μs/div

Figure 17. Transient Response



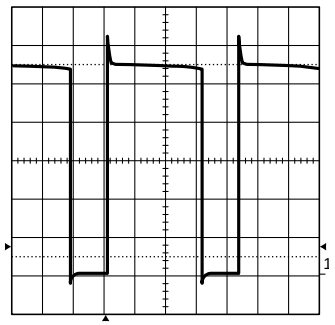
Conditions: input voltage = 48 VDC, output current = 30 A
Bandwidth limit = 25 MHz
Trace 1: output ripple voltage Volts/div = 50 mV
Horizontal resolution = 2 μs/div

Figure 18. Output Ripple



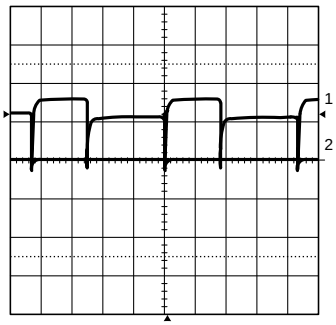
Conditions: input voltage = 38 VDC, output current = 25 A
Trace 1: Q1 drain voltage Volts/div = 20 V
Horizontal resolution = 1 μs/div

Figure 19. Drain Voltage



Conditions: input voltage = 78 VDC, output current = 25 A
Trace 1: Q1 drain voltage Volts/div = 20 V
Horizontal resolution = 1 μs/div

Figure 20. Drain Voltage



Conditions: input voltage = 48 VDC, output current = 5 A
Synchronous rectifier, Q3 gate Volts/div = 5 V
Trace 1: synchronous rectifier, Q3 gate Volts/div = 5 V
Trace 2: synchronous rectifier, Q5 gate Volts/div = 5 V
Horizontal resolution = 1 μs/div

Figure 21. Gate Voltages of the Synchronous Rectifiers

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8.3 System Example

Figure 22 shows an application circuit with 36-V to 78-V input and 3.3-V, 30-A output capability.

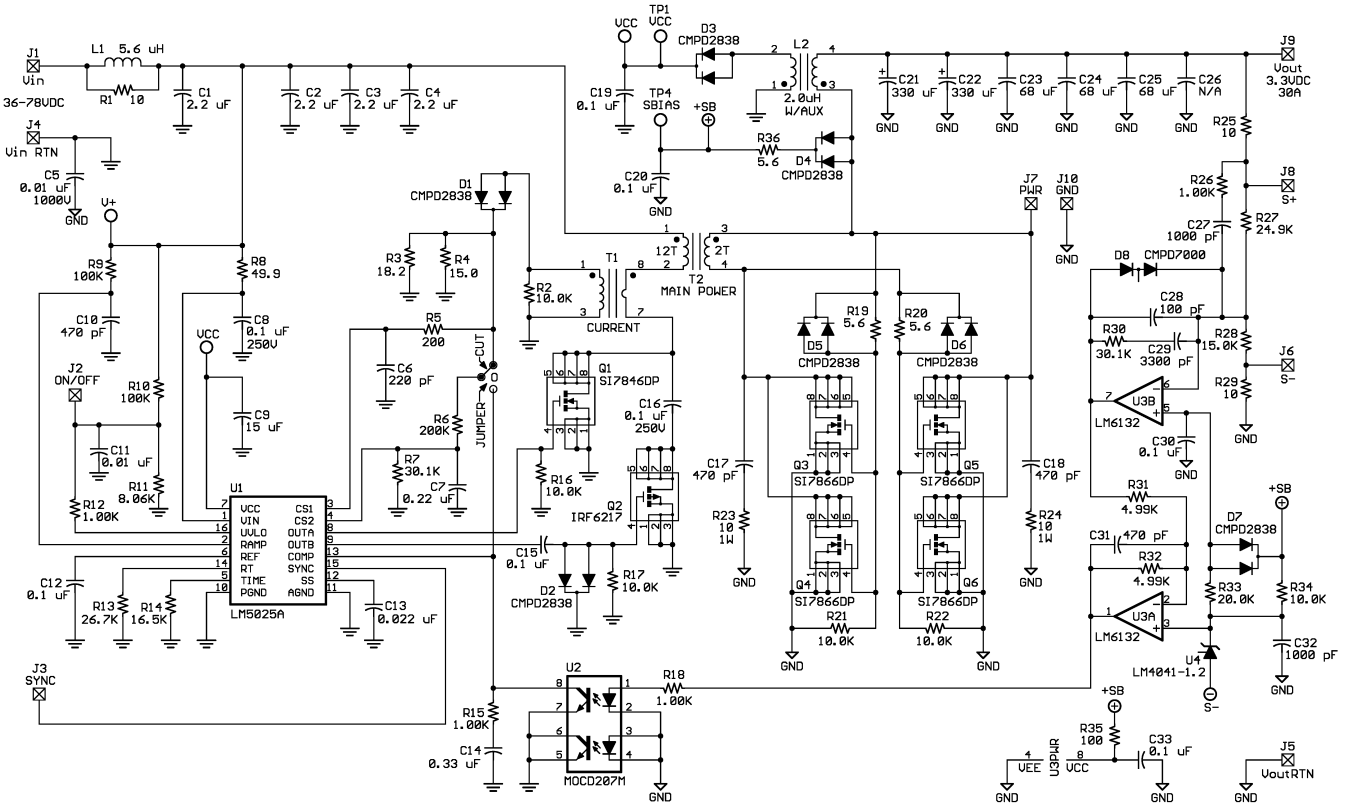


Figure 22. Application Circuit

9 Power Supply Recommendations

The V_{CC} pin is the power supply for the device. There must be a 0.1-µF to approximately 100-µF capacitor directly from V_{CC} to ground. REF pin must be bypassed to ground as close as possible to the device using a 0.1-µF capacitor.

10 Layout

10.1 Layout Guidelines

- Connect two grounds PGND (power ground) and AGND (analog ground) directly as device ground ICGND. The connection must be as close to the pins as possible.
- If there are multiple PCB layers and there is a inner ground layer, use two vias or one big via on GND and connect them to the inner ground layer (ICGND).
- The power stage ground PSGND must be separated with the ICGND. PSGND and ICGND must be connected at a single point close to the device.
- The bypass capacitors to the V_{CC} pin and REF pin must be as close as possible to the pins and ground (ICGND).
- The filtering capacitors connected to CS1 and CS2 pins must have connections as short as possible to ICGND; if an inner ground layer is available, use vias to connect the capacitors to the ground layer (ICGND).
- The resistors and capacitors connected to the timing configuration pins must be as close as possible to the pins and ground (ICGND).

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10.2 Layout Example

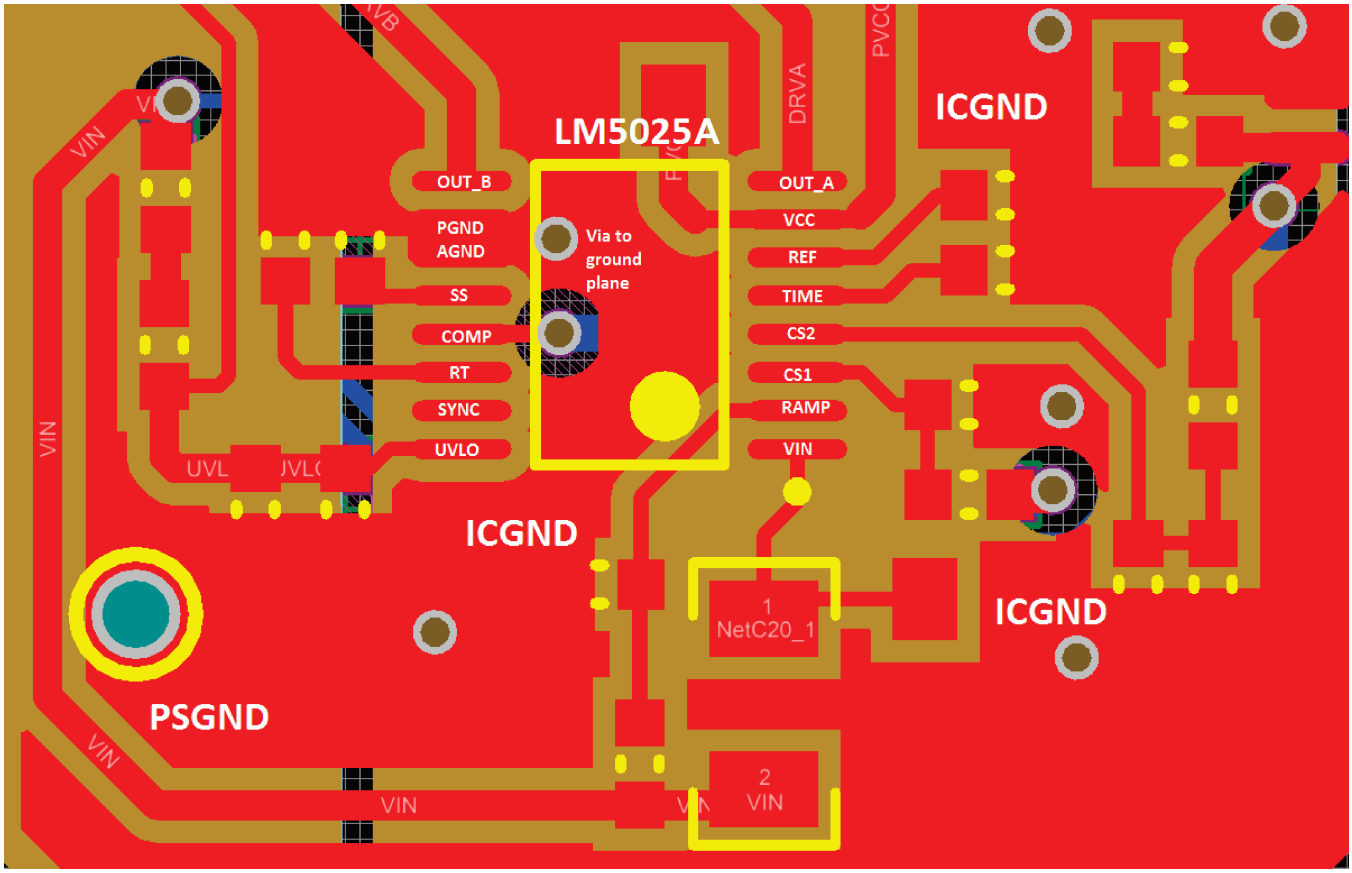


Figure 23. LM5025A Layout Recommendation

10.3 Thermal Protection

Internal thermal shutdown circuitry is provided to protect the integrated circuit in the event the maximum junction temperature is exceeded. When activated, typically at 165°C, the controller is forced into a low-power standby state with the output drivers and the bias regulator disabled. The device restarts after the thermal hysteresis (typically 25°C). During a restart after thermal shutdown, the soft-start capacitor is fully discharged and then charged in the low current mode (1 µA) similar to a second level current limit event. The thermal protection feature is provided to prevent catastrophic failures from accidental device overheating.

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11 デバイスおよびドキュメントのサポート

11.1 ドキュメントのサポート

11.1.1 関連資料

関連資料については、以下を参照してください。

『LM5025 絶縁アクティブ・クランプ・フォワード・コンバータ リファレンス・デザイン・ユーザー・ガイド』(SNVU096)

11.2 ドキュメントの更新通知を受け取る方法

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11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。これらの情報は、指定のデバイスに対して提供されている最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LM5025AMTCX/NOPB	Active	Production	TSSOP (PW) | 16	2500 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	L5025A MTC
LM5025AMTCX/NOPB.A	Active	Production	TSSOP (PW) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	L5025A MTC
LM5025AMTCX/NOPB.B	Active	Production	TSSOP (PW) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	L5025A MTC
LM5025ASD/NOPB	Obsolete	Production	WSON (NHQ) | 16	-	-	Call TI	Call TI	-40 to 125	5025ASD
LM5025ASDX/NOPB	Active	Production	WSON (NHQ) | 16	4500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	5025ASD
LM5025ASDX/NOPB.A	Active	Production	WSON (NHQ) | 16	4500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	5025ASD
LM5025ASDX/NOPB.B	Active	Production	WSON (NHQ) | 16	4500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	5025ASD

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

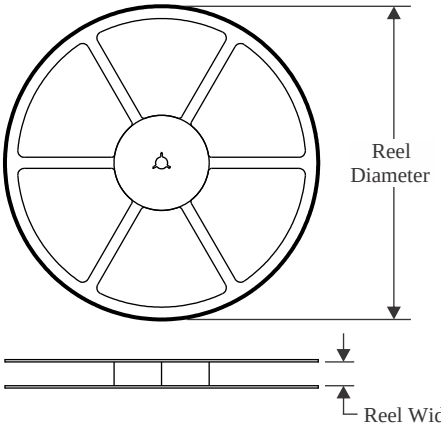
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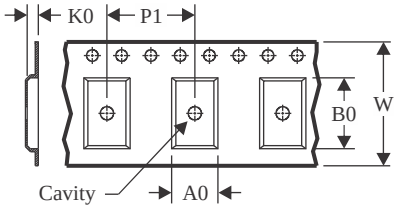
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TAPE AND REEL INFORMATION

REEL DIMENSIONS

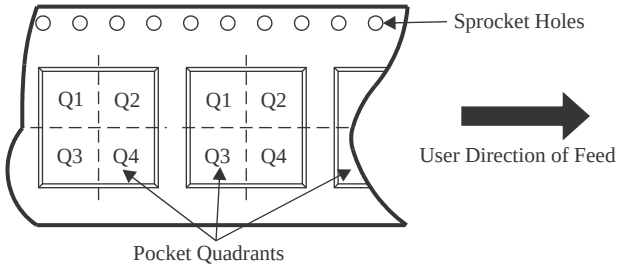


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

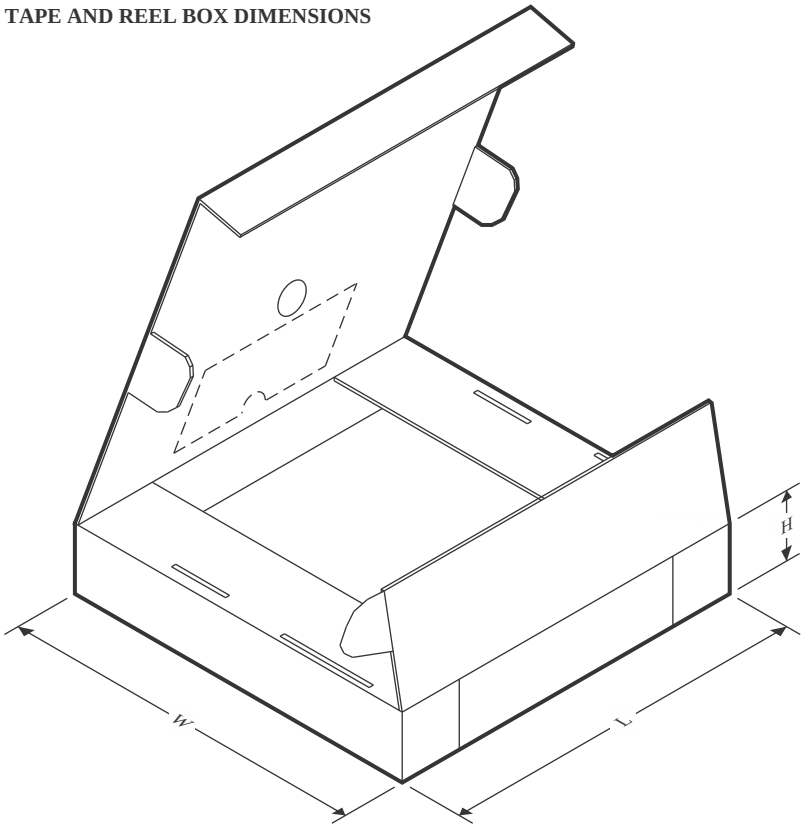
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM5025AMTCX/NOPB	TSSOP	PW	16	2500	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
LM5025AMTCX/NOPB	TSSOP	PW	16	2500	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
LM5025ASDX/NOPB	WSON	NHQ	16	4500	330.0	12.4	5.3	5.3	1.3	8.0	12.0	Q1

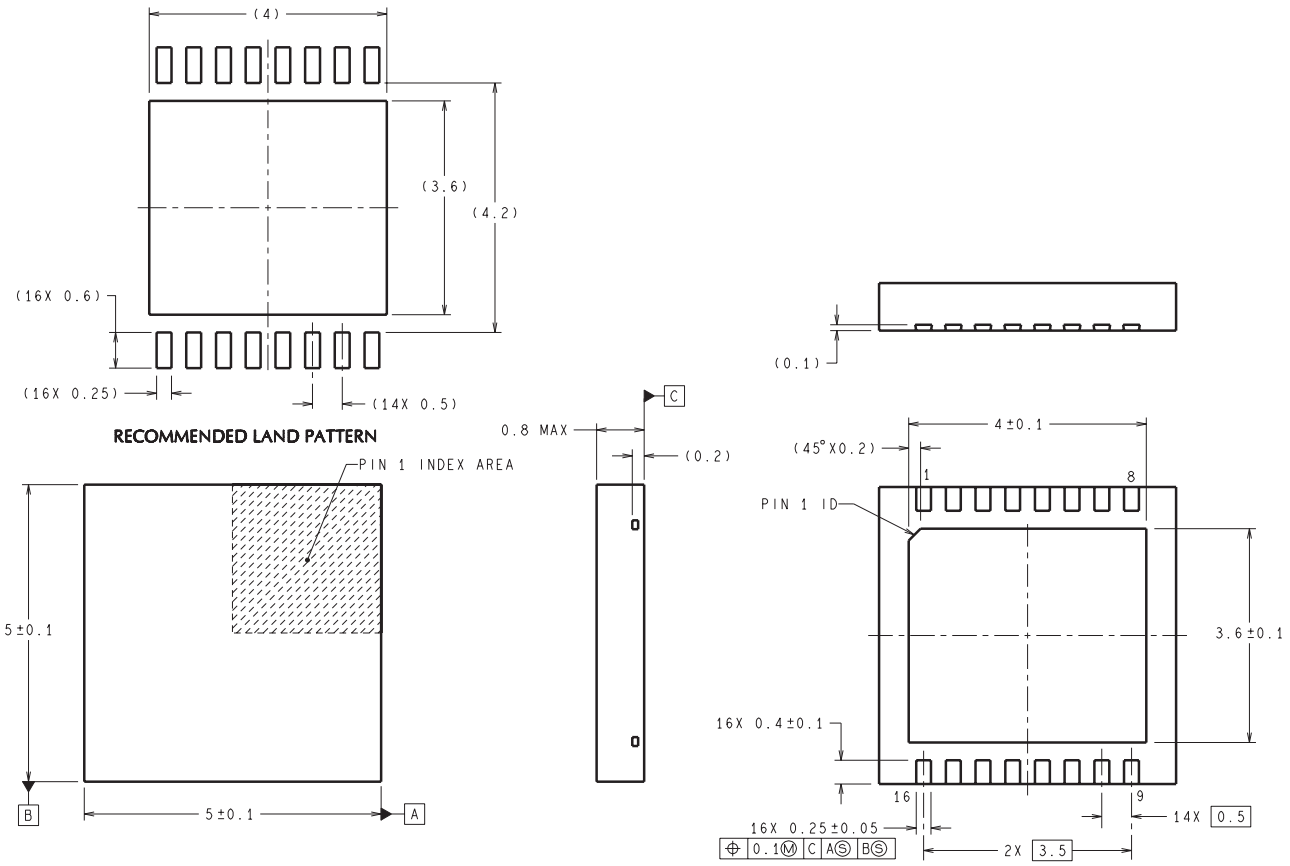
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM5025AMTCX/NOPB	TSSOP	PW	16	2500	353.0	353.0	32.0
LM5025AMTCX/NOPB	TSSOP	PW	16	2500	367.0	367.0	35.0
LM5025ASDX/NOPB	WSON	NHQ	16	4500	367.0	367.0	35.0

NHQ0016A



DIMENSIONS ARE IN MILLIMETERS

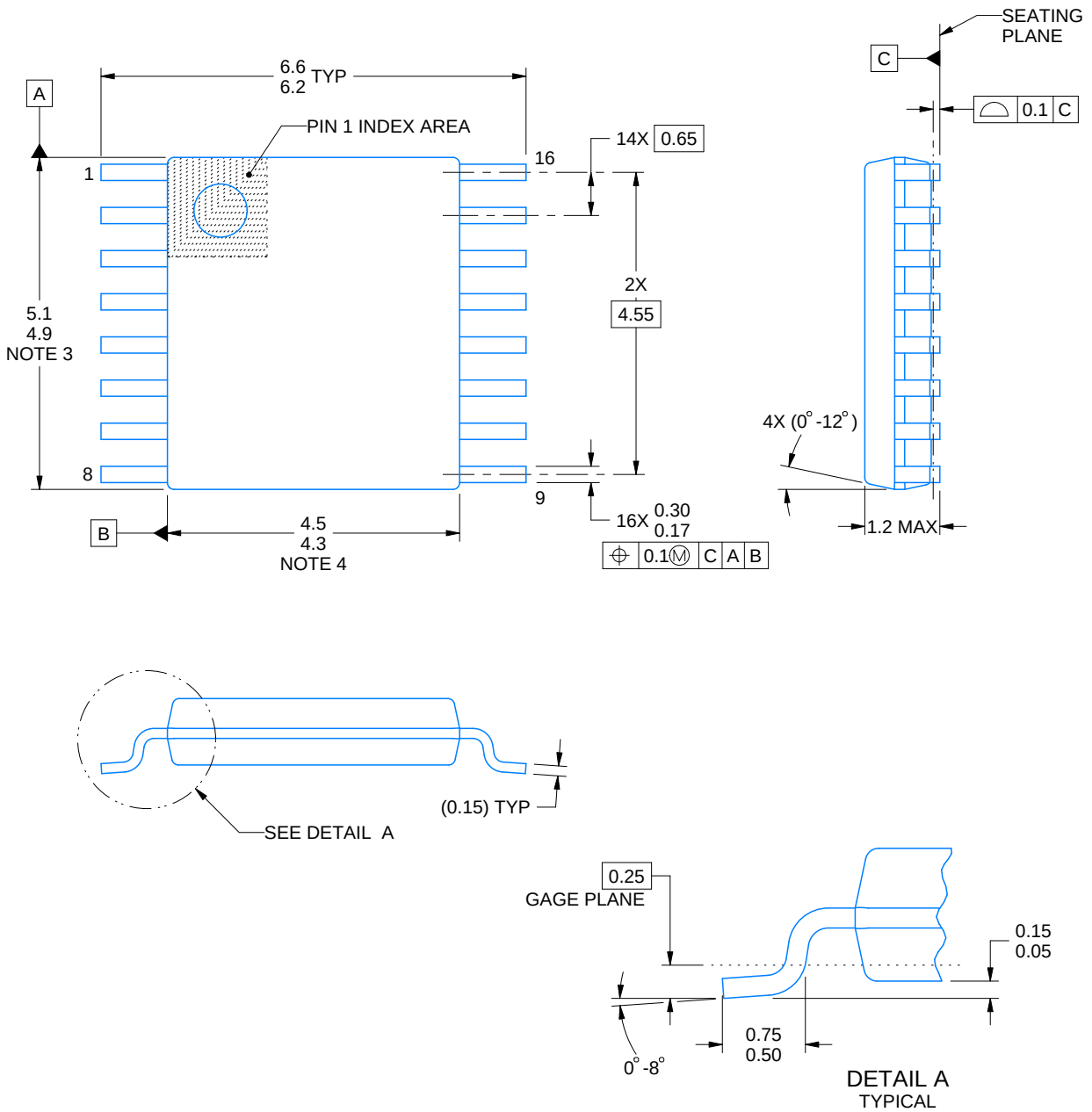
SDA16A (Rev A)

PACKAGE OUTLINE

PW0016A

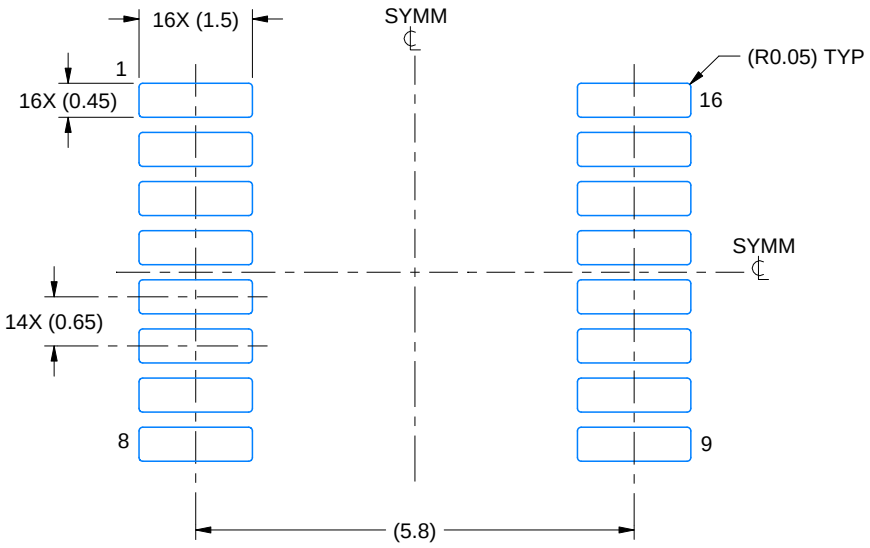
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

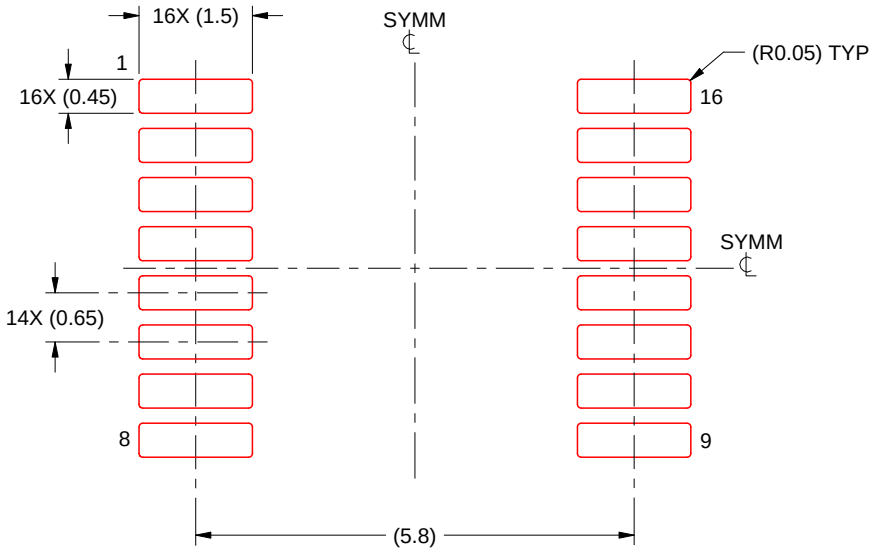


SOLDER MASK DETAILS

4220204/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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