

# LM5105 100V、ハーフ・ブリッジ・ゲート・ドライバ、プログラマブル・デッド・タイム付き

## 1 特長

- ハイサイドとローサイドの両方のNチャンネルMOSFETを駆動
- ピーク・ゲート・ドライバ電流: 1.8A
- ブートストラップ電源電圧範囲: 最大118V DC
- ブートストラップ・ダイオードを内蔵
- TTL互換の単一入力
- ターンオフ遅延(デッドタイム)をプログラム可能
- イネーブル入力ピン
- 短いターンオフ伝搬遅延(標準値26ns)
- 15nsの立ち上がり時間と立ち下がり時間で1000pFを駆動
- 電源レールの低電圧誤動作防止
- 低消費電力
- 放熱特性の優れた10ピンのWSOパッケージ (4mm×4mm)

## 2 アプリケーション

- ソリッド・ステート・モータ・ドライブ
- ハーフ/フルブリッジのパワー・コンバータ

## 3 概要

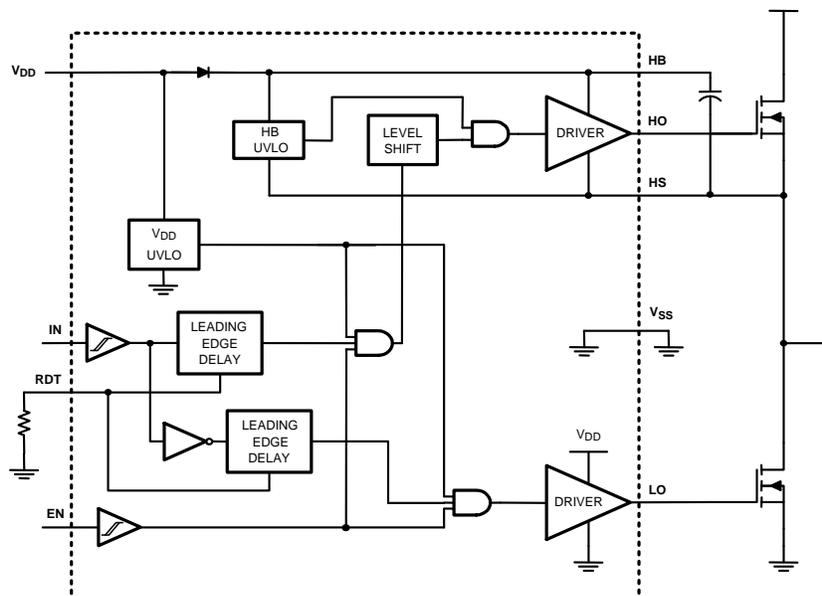
このLM5105は高電圧ゲート・ドライバで、ハイサイドとローサイド両方のNチャンネルMOSFETを同期整流降圧型またはハーフブリッジ構成で駆動するよう設計されています。フローティングのハイサイド・ドライバは、100Vまでのレール電圧で動作できます。単一の制御入力によりTTL信号レベルと互換で、単一の外付け抵抗により、厳密にマッチングされたターンオン遅延回路を使用して、スイッチング遷移デッドタイムをプログラムできます。ハイサイドのゲート駆動ブートストラップ・コンデンサを充電するため、高電圧ダイオードが搭載されています。堅牢なレベル・シフト技術により、消費電力を抑えながら高速で動作し、クリーンな出力遷移を実現します。低電圧誤動作防止機能により、ローサイドまたはブートストラップ付きのハイサイド電源電圧が動作スレッシュホールドを下回ると、ゲート・ドライバがディセーブルされます。LM5105は、熱特性が強化されたWSOプラスチック・パッケージで供給されます。

### 製品情報<sup>(1)</sup>

型番	パッケージ	本体サイズ(公称)
LM5105	WSO (10)	4.00mm×4.00mm

(1) 提供されているすべてのパッケージについては、巻末の注文情報を参照してください。

### アプリケーション概略図



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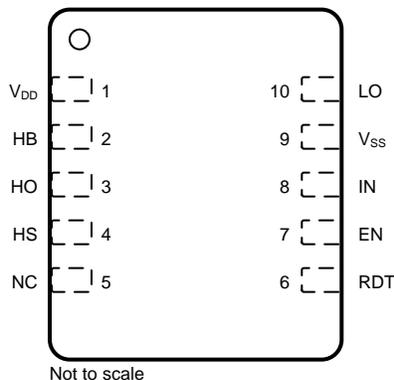
## 4 改訂履歴

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

<b>Revision D (March 2016) から Revision E に変更</b>		<b>Page</b>
•	Updated values in the <i>Thermal Information</i> table to align with JEDEC standards .....	5
<b>Revision C (March 2013) から Revision D に変更</b>		<b>Page</b>
•	「製品情報」表、「ESD定格」表、「詳細説明」セクション、「アプリケーションと実装」セクション、「レイアウト」セクション、「デバイスおよびドキュメントのサポート」セクション、「メカニカル、パッケージ、および注文情報」セクション 追加 .....	1
<b>Revision B (March 2013) から Revision C に変更</b>		<b>Page</b>
•	Changed layout of National Semiconductor Data Sheet to TI format .....	13

## 5 Pin Configuration and Functions

**DPR Package  
10-Pin WSON  
Top View**



**Pin Functions**

PIN		TYPE <sup>(1)</sup>	DESCRIPTION
NO.	NAME		
1	V <sub>DD</sub>	P	Positive gate drive supply. Decouple VDD to VSS using a low ESR/ESL capacitor, placed as close to the IC as possible.
2	HB	P	High-side gate driver bootstrap rail. Connect the positive terminal of bootstrap capacitor to the HB pin and connect negative terminal to HS. The Bootstrap capacitor must be placed as close to IC as possible.
3	HO	O	High-side gate driver output. Connect to the gate of high side N-MOS device through a short, low inductance path.
4	HS	P	High-side MOSFET source connection. Connect to the negative terminal of the bootstrap capacitor and to the source of the high side N-MOS device.
5	NC	—	Not connected.
6	RDT	I	Dead-time programming pin. A resistor from RDT to VSS programs the turnon delay of both the high and low side MOSFETs. The resistor must be placed close to the IC to minimize noise coupling from adjacent PCB traces.
7	EN	I	Logic input for driver disable or enable. TTL compatible threshold with hysteresis. LO and HO are held in the low state when EN is low.
8	IN	I	Logic input for gate driver. TTL compatible threshold with hysteresis. The high side MOSFET is turned on and the low side MOSFET turned off when IN is high.
9	V <sub>SS</sub>	G	Ground return. All signals are referenced to this ground.
10	LO	O	Low-side gate driver output. Connect to the gate of the low side N-MOS device with a short, low inductance path.
—	Exposed Pad	—	It is recommended that the exposed pad on the bottom of the package be soldered to ground plane on the PCB to aid thermal dissipation.

(1) G = Ground, I = Input, O = Output, P = Power

## 6 Specifications

### 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)(2)</sup>

	MIN	MAX	UNIT
$V_{DD}$ to $V_{SS}$	-0.3	18	V
HB to HS	-0.3	18	V
IN and EN to $V_{SS}$	-0.3	$V_{DD} + 0.3$	V
LO to $V_{SS}$	-0.3	$V_{DD} + 0.3$	V
HO to $V_{SS}$	HS - 0.3	HB + 0.3	V
HS to $V_{SS}$ <sup>(3)</sup>	-5	100	V
HB to $V_{SS}$		118	V
RDT to $V_{SS}$	-0.3	5	V
Junction temperature, $T_J$		150	°C
Storage temperature, $T_{stg}$	-55	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/Distributors for availability and specifications.
- (3) In the application the HS node is clamped by the body diode of the external lower N-MOSFET, therefore the HS voltage generally does not exceed -1 V. However, in some applications, board resistance and inductance may result in the HS node exceeding this stated voltage transiently. If negative transients occur on HS, the HS voltage must never be more negative than  $V_{DD} - 15$  V. For example, if  $V_{DD} = 10$  V, the negative transients at HS must not exceed -5 V.

### 6.2 ESD Ratings

	VALUE	UNIT
$V_{(ESD)}$ Electrostatic discharge Human-body model (HBM) <sup>(1)(2)</sup>	±2000	V

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) The human-body model is a 100-pF capacitor discharged through a 1.5-k $\Omega$  resistor into each pin. Pin 2, Pin 3 and Pin 4 are rated at 500 V.

### 6.3 Recommended Operating Conditions

	MIN	NOM	MAX	UNIT
$V_{DD}$	8		14	V
HS <sup>(1)</sup>	-1		100	V
HB	HS + 8		HS + 14	V
HS Slew rate			<50	V/ns
$T_J$ Junction temperature	-40		125	°C

- (1) In the application the HS node is clamped by the body diode of the external lower N-MOSFET; therefore, the HS voltage generally does not exceed -1 V. However in some applications, board resistance and inductance may result in the HS node exceeding this stated voltage transiently. If negative transients occur on HS, the HS voltage must never be more negative than  $V_{DD} - 15$  V. For example, if  $V_{DD} = 10$  V, the negative transients at HS must not exceed -5 V.

## 6.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>		LM5105	
		DPR (WSON)	UNIT
		10 PINS	
R <sub>θJA</sub>	Junction-to-ambient thermal resistance	37.8	°C/W
R <sub>θJC(top)</sub>	Junction-to-case (top) thermal resistance	36.2	°C/W
R <sub>θJB</sub>	Junction-to-board thermal resistance	14.9	°C/W
ψ <sub>JT</sub>	Junction-to-top characterization parameter	0.3	°C/W
ψ <sub>JB</sub>	Junction-to-board characterization parameter	15.2	°C/W
R <sub>θJC(bot)</sub>	Junction-to-case (bottom) thermal resistance	4.4	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

## 6.5 Electrical Characteristics

Unless otherwise noted, V<sub>DD</sub> = HB = 12 V, V<sub>SS</sub> = HS = 0 V, EN = 5 V, no load on LO or HO, RDT = 100 kΩ<sup>(1)</sup>. Typical limits are for T<sub>J</sub> = 25°C, and minimum and maximum limits apply over the operating junction temperature range (–40°C to 125°C).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>SUPPLY CURRENTS</b>						
I <sub>DD</sub>	V <sub>DD</sub> quiescent current	IN = EN = 0 V		0.34	0.6	mA
I <sub>DDO</sub>	V <sub>DD</sub> operating current	f = 500 kHz		1.65	3	mA
I <sub>HB</sub>	Total HB quiescent current	IN = EN = 0 V		0.06	0.2	mA
I <sub>HBO</sub>	Total HB operating current	f = 500 kHz		1.3	3	mA
I <sub>HBS</sub>	HB to V <sub>SS</sub> current, quiescent	HS = HB = 100 V		0.05	10	μA
I <sub>HBSO</sub>	HB to V <sub>SS</sub> current, operating	f = 500 kHz		0.1		mA
<b>INPUT IN AND EN</b>						
V <sub>IL</sub>	Low-level input voltage threshold		0.8	1.8		V
V <sub>IH</sub>	High-level input voltage threshold			1.8	2.2	V
R <sub>pd</sub>	Input pulldown resistance pin IN and EN		100	200	500	kΩ
<b>DEAD-TIME CONTROLS</b>						
VRDT	Nominal voltage at RDT		2.7	3	3.3	V
IRDT	RDT pin current limit	RDT = 0 V	0.75	1.5	2.25	mA
<b>UNDER VOLTAGE PROTECTION</b>						
V <sub>DDR</sub>	V <sub>DD</sub> rising threshold		6	6.9	7.4	V
V <sub>DDH</sub>	V <sub>DD</sub> threshold hysteresis			0.5		V
V <sub>HBR</sub>	HB rising threshold		5.7	6.6	7.1	V
V <sub>HBH</sub>	HB threshold hysteresis			0.4		V
<b>BOOT STRAP DIODE</b>						
V <sub>DL</sub>	Low-current forward voltage	I <sub>VDD-HB</sub> = 100 μA		0.6	0.9	V
V <sub>DH</sub>	High-current forward voltage	I <sub>VDD-HB</sub> = 100 mA		0.85	1.1	V
R <sub>D</sub>	Dynamic resistance	I <sub>VDD-HB</sub> = 100 mA		0.8	1.5	Ω
<b>LO GATE DRIVER</b>						
V <sub>OLL</sub>	Low-level output voltage	I <sub>LO</sub> = 100 mA		0.25	0.4	V
V <sub>OHL</sub>	High-level output voltage	I <sub>LO</sub> = –100 mA, V <sub>OHL</sub> = V <sub>DD</sub> – V <sub>LO</sub>		0.35	0.55	V
I <sub>OHL</sub>	Peak pullup current	LO = 0 V		1.8		A
I <sub>OLL</sub>	Peak pulldown current	LO = 12 V		1.6		A

(1) Minimum and maximum limits are 100% production tested at 25°C. Limits over the operating temperature range are specified through correlation using Statistical Quality Control (SQC) methods. Limits are used to calculate Average Outgoing Quality Level (AOQL).

**Electrical Characteristics (continued)**

Unless otherwise noted,  $V_{DD} = HB = 12\text{ V}$ ,  $V_{SS} = HS = 0\text{ V}$ ,  $EN = 5\text{ V}$ , no load on LO or HO,  $RDT = 100\text{ k}\Omega^{(1)}$ . Typical limits are for  $T_J = 25^\circ\text{C}$ , and minimum and maximum limits apply over the operating junction temperature range ( $-40^\circ\text{C}$  to  $125^\circ\text{C}$ ).

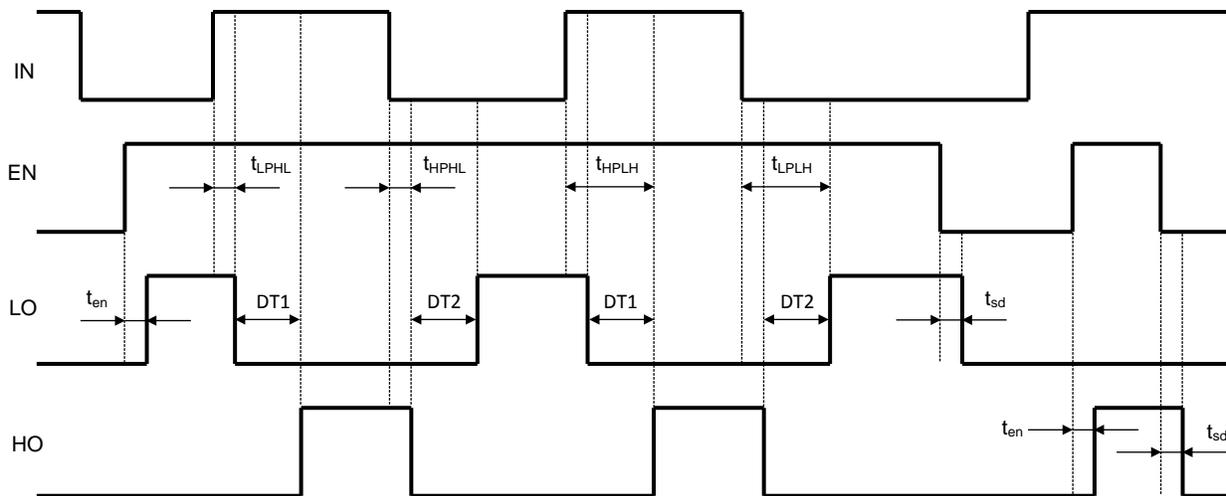
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>HO GATE DRIVER</b>						
$V_{OLH}$	Low-level output voltage	$I_{HO} = 100\text{ mA}$		0.25	0.4	V
$V_{OHH}$	High-level output voltage	$I_{HO} = -100\text{ mA}$ , $V_{OHH} = HB - HO$		0.35	0.55	V
$I_{OHH}$	Peak pullup current	$HO = 0\text{ V}$		1.8		A
$I_{OLH}$	Peak pulldown current	$HO = 12\text{ V}$		1.6		A

**6.6 Switching Characteristics**

Unless otherwise noted,  $V_{DD} = HB = 12\text{ V}$ ,  $V_{SS} = HS = 0\text{ V}$ , no Load on LO or HO<sup>(1)</sup>. Typical limits are for  $T_J = 25^\circ\text{C}$ , and minimum and maximum limits apply over the operating junction temperature range ( $-40^\circ\text{C}$  to  $125^\circ\text{C}$ ).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{LPHL}$	Lower turnoff propagation delay			26	56	ns
$t_{HPHL}$	Upper turnoff propagation delay			26	56	ns
$t_{LPLH}$	Lower turnon propagation delay	$RDT = 100\text{ k}$	485	595	705	ns
$t_{HPLH}$	Upper turnon propagation delay	$RDT = 100\text{ k}$	485	595	705	ns
$t_{LPLH}$	Lower turnon propagation delay	$RDT = 10\text{ k}$	75	105	150	ns
$t_{HPLH}$	Upper turnon propagation delay	$RDT = 10\text{ k}$	75	105	150	ns
$t_{en}, t_{sd}$	Enable and shutdown propagation delay			28		ns
DT1, DT2	Dead-time LO OFF to HO ON and HO OFF to LO ON	$RDT = 100\text{ k}$		570		ns
		$RDT = 10\text{ k}$		80		ns
MDT	Dead-time matching	$RDT = 100\text{ k}$		50		ns
$t_R, t_F$	Either output rise or fall time	$C_L = 1000\text{ pF}$		15		ns
$t_{BS}$	Bootstrap diode turnon or turnoff time	$I_F = 20\text{ mA}, I_R = 200\text{ mA}$		50		ns

(1) Minimum and maximum limits are 100% production tested at  $25^\circ\text{C}$ . Limits over the operating temperature range are specified through correlation using Statistical Quality Control (SQC) methods. Limits are used to calculate Average Outgoing Quality Level (AOQL).



**Figure 1. LM5105 Input - Output Waveforms**

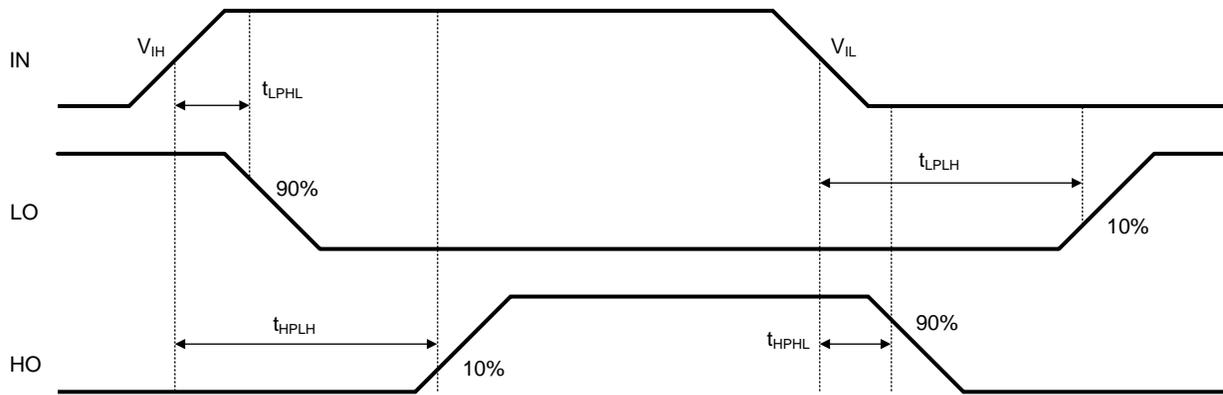


Figure 2. LM5105 Switching Time Definitions:  $T_{LPLH}$ ,  $T_{LPHL}$ ,  $T_{HPLH}$ ,  $T_{HPHL}$

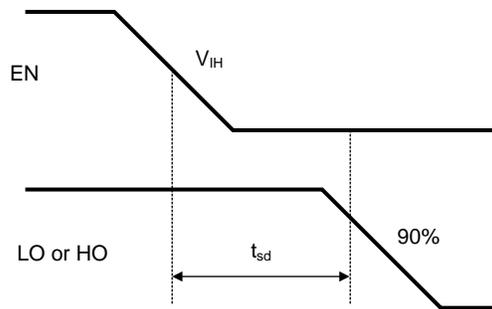


Figure 3. LM5105 Enable:  $T_{sd}$

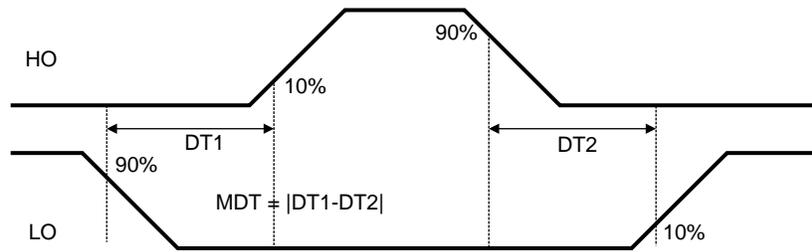


Figure 4. LM5105 Dead-Time: DT

### 6.7 Typical Characteristics

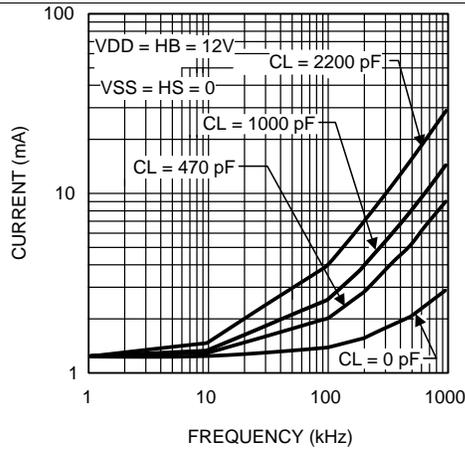


Figure 5.  $V_{DD}$  Operating Current vs Frequency

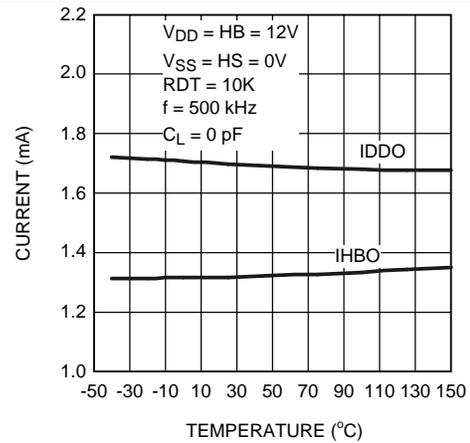


Figure 6. Operating Current vs Temperature

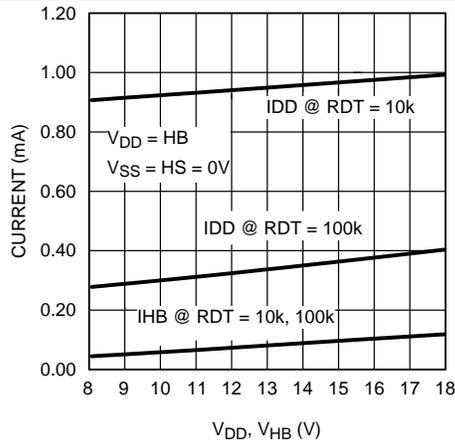


Figure 7. Quiescent Current vs Supply Voltage

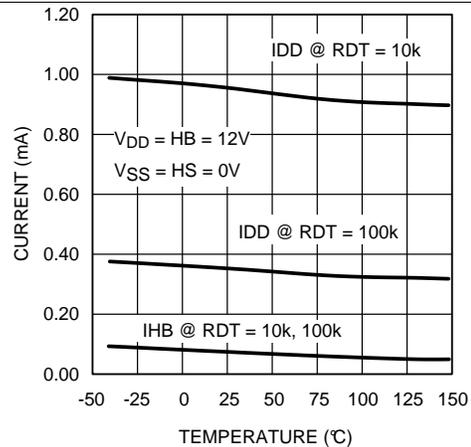


Figure 8. Quiescent Current vs Temperature

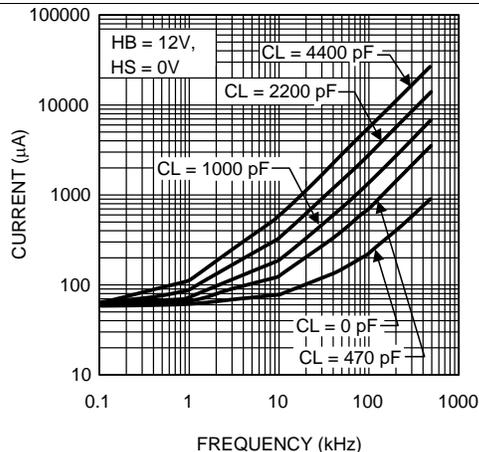


Figure 9. HB Operating Current vs Frequency

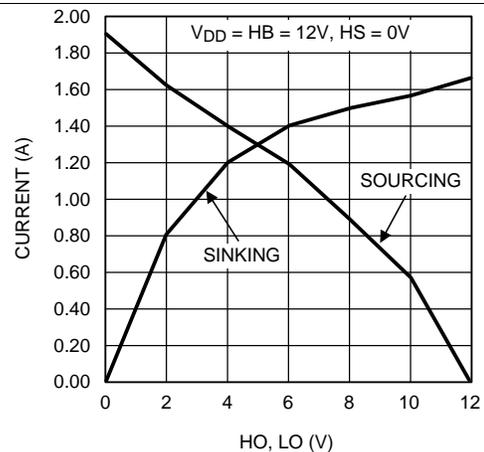


Figure 10. HO & LO Peak Output Current vs Output Voltage

Typical Characteristics (continued)

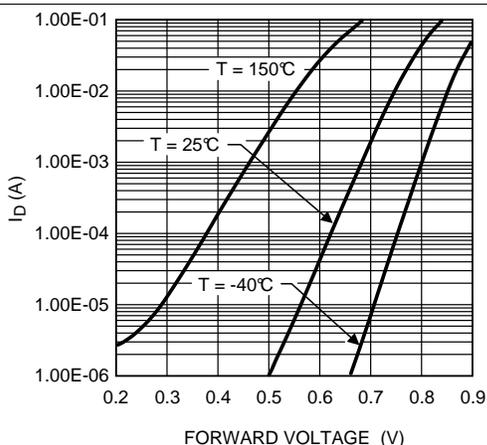


Figure 11. Diode Forward Voltage

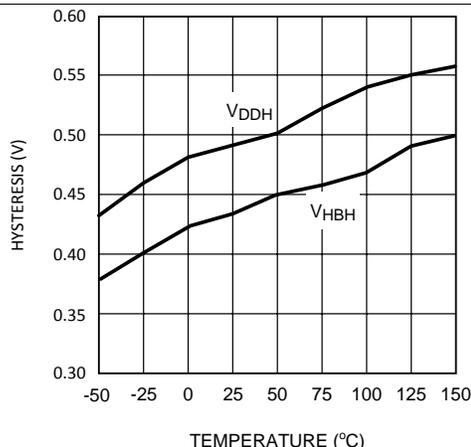


Figure 12. Undervoltage Hysteresis vs Temperature

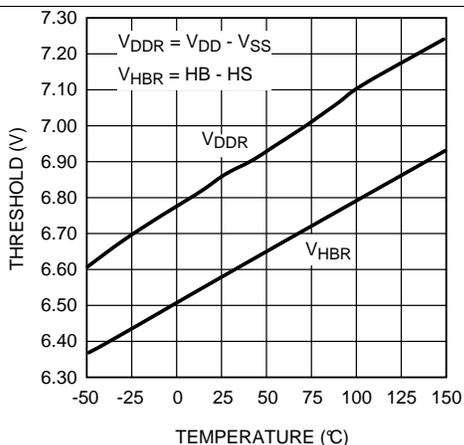


Figure 13. Undervoltage Rising Threshold vs Temperature

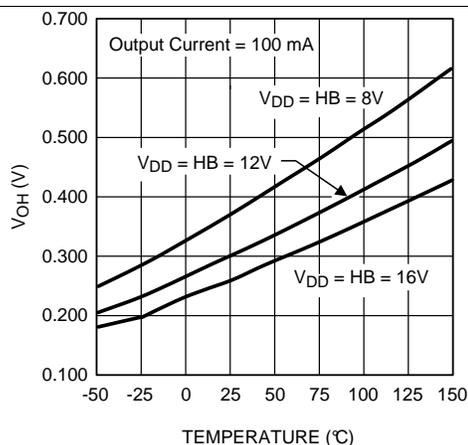


Figure 14. LO & HO High-Level Output Voltage vs Temperature

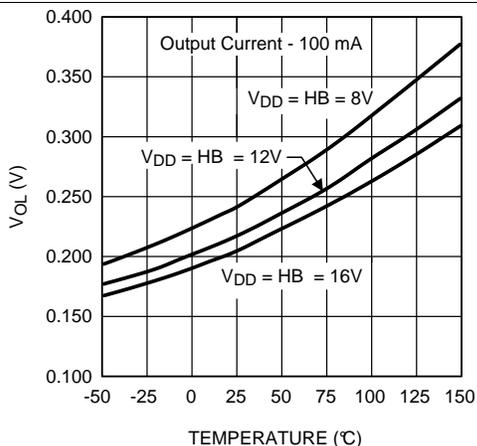


Figure 15. LO & HO Low-Level Output Voltage vs Temperature

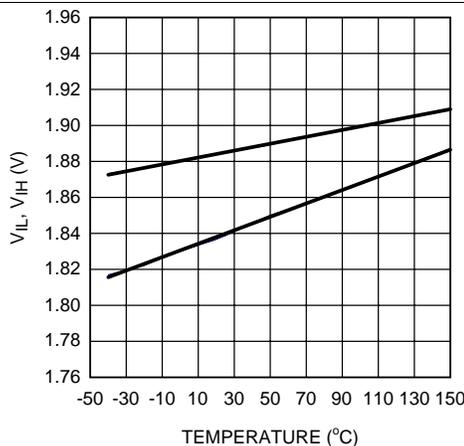
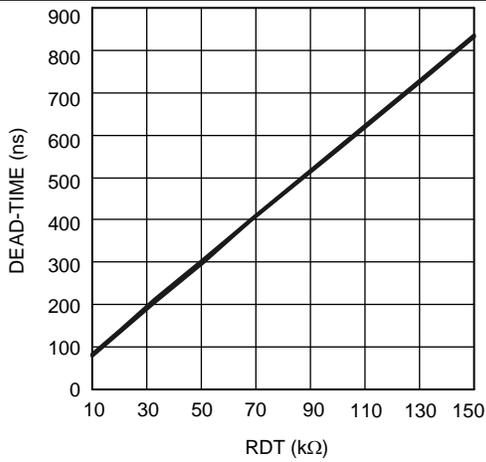
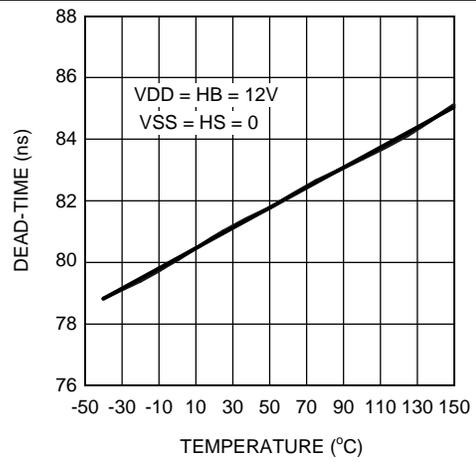


Figure 16. Input Threshold vs Temperature

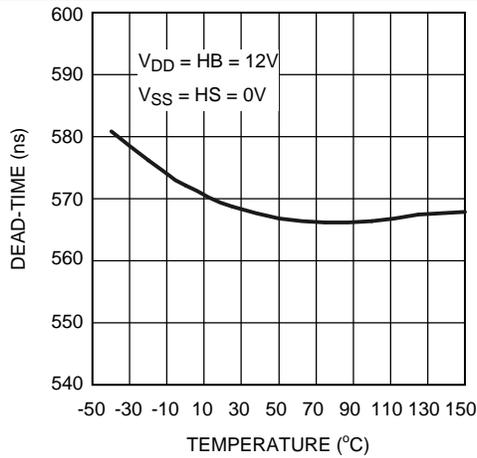
**Typical Characteristics (continued)**



**Figure 17. Dead-Time vs RT Resistor Value**



**Figure 18. Dead-Time vs Temperature (RT = 10 k)**



**Figure 19. Dead-Time vs Temperature (RT = 100 k)**

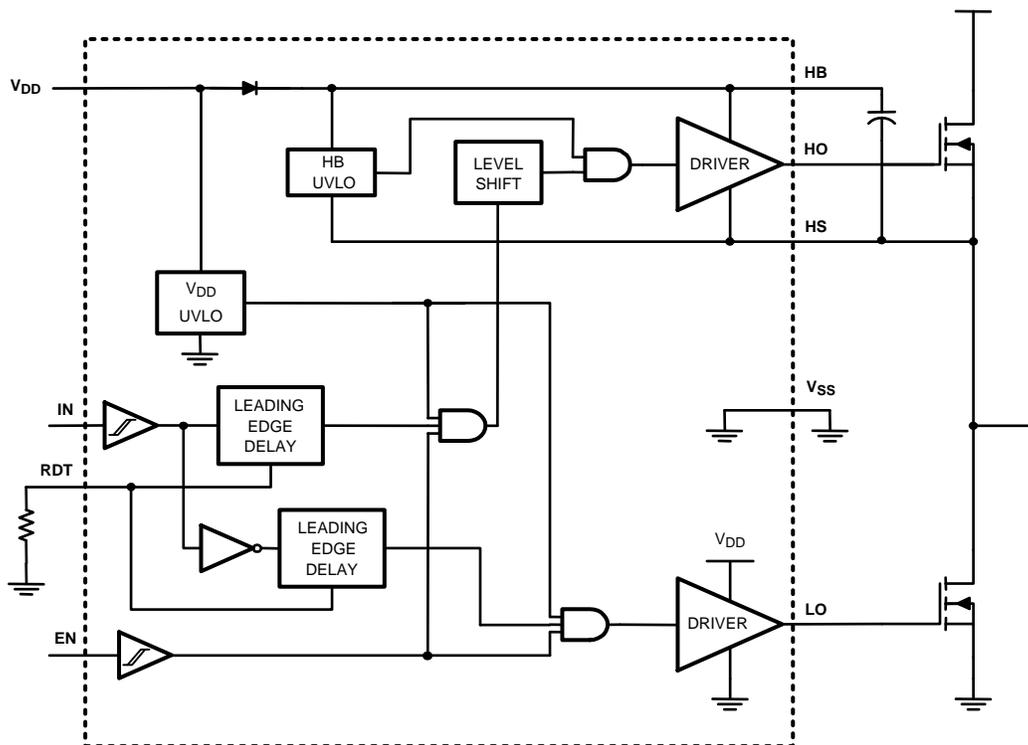
## 7 Detailed Description

### 7.1 Overview

The LM5105 is a single PWM input Gate Driver with Enable that offers a programmable dead time. The dead time is set with a resistor at the RDT pin and can be adjusted from 100 ns to 600 ns. The wide dead-time programming range provides the flexibility to optimize drive signal timing for a wide range of MOSFETs and applications.

The RDT pin is biased at 3 V and current-limited to 1-mA maximum programming current. The time delay generator accommodates resistor values from 5 k to 100 k with a dead time that is proportional to the RDT resistance. Grounding the RDT pin programs the LM5105 to drive both outputs with minimum dead time.

### 7.2 Functional Block Diagram



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### 7.3 Feature Description

#### 7.3.1 Start-Up and UVLO

Both top and bottom drivers include undervoltage lockout (UVLO) protection circuitry, which monitors the supply voltage ( $V_{DD}$ ) and bootstrap capacitor voltage ( $HB - HS$ ) independently. The UVLO circuit inhibits each driver until sufficient supply voltage is available to turn on the external MOSFETs, and the UVLO hysteresis prevents chattering during supply voltage transitions. When the supply voltage is applied to the  $V_{DD}$  pin of LM5105, the top and bottom gates are held low until  $V_{DD}$  exceeds the UVLO threshold, typically about 6.9 V. Any UVLO condition on the bootstrap capacitor disables only the high-side output (HO).

## 7.4 Device Functional Modes

Table 1 lists the functional modes for LM5105.

**Table 1. Function Table**

<b>EN</b>	<b>IN PIN</b>	<b>LO PIN</b>	<b>HO PIN</b>
L	Any	L	L
H	H	L	H
H	L	H	L

## 8 Application and Implementation

### NOTE

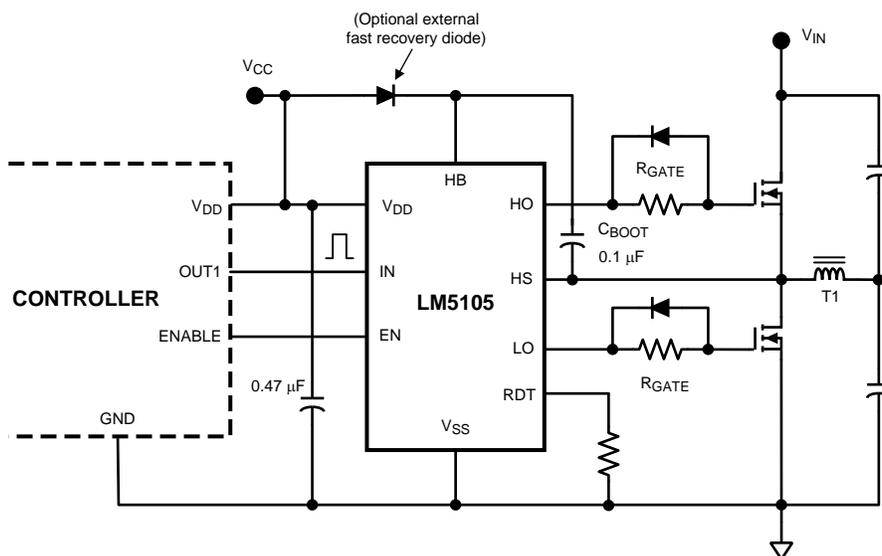
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### 8.1 Application Information

The LM5105 is one of the latest generation of high-voltage gate drivers which are designed to drive both the high-side and low-side N-channel MOSFETs in a half-bridge or full-bridge configuration or in a synchronous buck circuit. The floating high-side driver can operate with supply voltages up to 110 V. This allows for N-channel MOSFET control in half-bridge, full-bridge, push-pull, two-switch forward, and active clamp topologies.

The outputs of the LM5105 are controlled from a single input. The rising edge of each output can be delayed with a programming resistor.

### 8.2 Typical Application



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Figure 20. LM5105 Driving MOSFETs Connected in Half-Bridge Configuration

#### 8.2.1 Design Requirements

Table 2 lists the design parameters for this application example.

Table 2. Design Parameters

PARAMETER	VALUE
Gate Drive IC	LM5105
Mosfet	CSD18531Q5A
$V_{DD}$	10 V
$Q_{gmax}$	43 nC
$F_{sw}$	100 kHz
$D_{Max}$	95%
$I_{HBS}$	10 $\mu$ A
$V_{DH}$	1.1 V

**Table 2. Design Parameters (continued)**

PARAMETER	VALUE
$V_{HBR}$	7.1 V
$V_{HBH}$	0.4 V

### 8.2.2 Detailed Design Procedure

$$\Delta V_{HB} = V_{DD} - V_{DH} - V_{HBL}$$

where

- $V_{DD}$  = Supply voltage of the gate drive IC
- $V_{DH}$  = Bootstrap diode forward voltage drop
- $V_{gsmin}$  = Minimum gate source threshold voltage

$$C_{BOOT} = \frac{Q_{TOTAL}}{\Delta V_{HB}} \quad (2)$$

$$Q_{TOTAL} = Q_{gmax} + I_{HBS} \times \frac{D_{Max}}{F_{SW}} \quad (3)$$

The quiescent current of the bootstrap circuit is 10  $\mu$ A, which is negligible compared to the Qgs of the MOSFET.

$$Q_{TOTAL} = 43nC + 10\mu A \times \frac{0.95}{100kHz} \quad (4)$$

$$Q_{TOTAL} = 43.01 \text{ nC} \quad (5)$$

In practice the value for the  $C_{BOOT}$  capacitor should be greater than that calculated to allow for situations where the power stage may skip pulse due to load transients. In this circumstance the boot capacitor must maintain the HB pin voltage above the UVLO voltage for the HB circuit.

As a general rule the local  $V_{DD}$  bypass capacitor should be 10 times greater than the calculated value of  $C_{BOOT}$ .

$$V_{HBL} = V_{HBR} - V_{HBH} \quad (6)$$

$$V_{HBL} = 6.7 \text{ V} \quad (7)$$

$$\Delta V_{HB} = 10 \text{ V} - 1.1 \text{ V} - 6.7 \text{ V} \quad (8)$$

$$\Delta V_{HB} = 2.2 \text{ V} \quad (9)$$

$$C_{BOOT} = 43.01nC / 2.2 \text{ V} \quad (10)$$

$$C_{BOOT} = 19.6 \text{ nF} \quad (11)$$

In practice, the value of  $C_{BOOT}$  is greater than the calculated value. This allows for the capacitance shift caused by the DC bias voltage and for situations where the power stage would otherwise skip pulses due to load transients. Therefore, it is recommended to include a safety-related margin in the  $C_{BOOT}$  value and place it as close to the VDD and VSS pins as possible. A 50-V, 0.1- $\mu$ F capacitor is chosen in this example.

The bootstrap and bias capacitors should be ceramic types with X7R dielectric. The voltage rating should be twice that of the maximum VDD to allow for loss of capacitance once the devices have a DC bias voltage across them and to ensure long-term reliability of the devices.

The resistor values,  $R_T$ , for setting turnon delay can be found in [Figure 17](#).

8.2.3 Application Curves

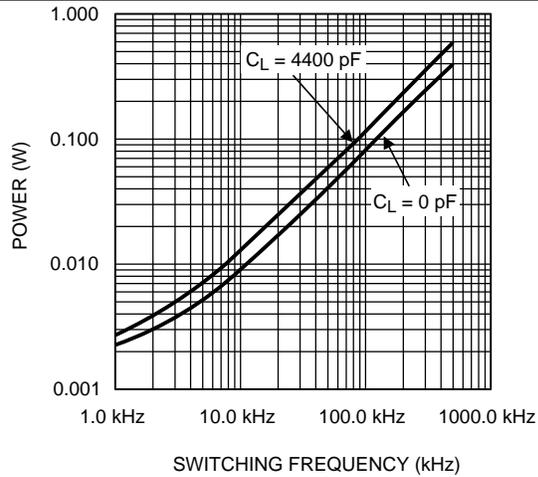


Figure 21. Diode Power Dissipation,  $V_{IN} = 80\text{ V}$

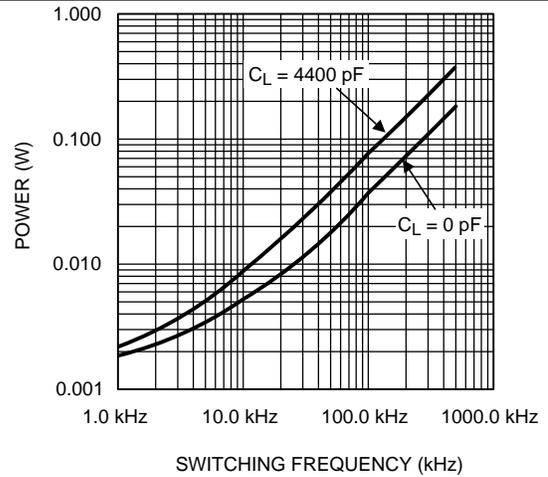


Figure 22. Diode Power Dissipation,  $V_{IN} = 40\text{ V}$

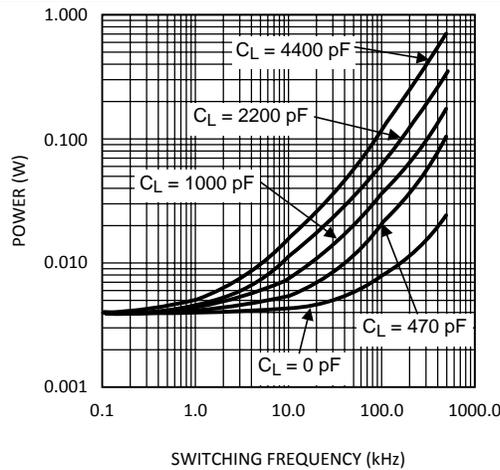


Figure 23. Gate Driver Power Dissipation (LO + HO)  
 $V_{CC} = 12\text{ V}$ , Neglecting Diode Losses

## 9 Power Supply Recommendations

### 9.1 Power Dissipation Considerations

The total IC power dissipation is the sum of the gate driver losses and the bootstrap diode losses. The gate driver losses are related to the switching frequency ( $f$ ), output load capacitance on LO and HO ( $C_L$ ), and supply voltage ( $V_{DD}$ ) and can be roughly calculated with [Equation 12](#).

$$P_{DGATES} = 2 \times f \times C_L \times V_{DD}^2 \quad (12)$$

There are some additional losses in the gate drivers due to the internal CMOS stages used to buffer the LO and HO outputs. [Figure 23](#) shows the measured gate driver power dissipation versus frequency and load capacitance. At higher frequencies and load capacitance values, the power dissipation is dominated by the power losses driving the output loads and agrees well with the previous equation. [Figure 23](#) can be used to approximate the power losses due to the gate drivers.

### 9.2 HS Transient Voltages Below Ground

The HS node is always clamped by the body diode of the lower external FET. In some situations, board resistances and inductances can cause the HS node to transiently swing several volts below ground. The HS node can swing below ground provided:

1. HS must always be at a lower potential than HO. Pulling HO more than  $-0.3$  V below HS can activate parasitic transistors resulting in excessive current flow from the HB supply, possibly resulting in damage to the IC. The same relationship is true with LO and VSS. If necessary, a Schottky diode can be placed externally between HO and HS or LO and GND to protect the IC from this type of transient. The diode must be placed as close to the IC pins as possible in order to be effective.
2. HB to HS operating voltage should be 14 V or less. Hence, if the HS pin transient voltage is  $-5$  V, VDD should be ideally limited to 9 V to keep HB to HS below 14 V.
3. Low ESR bypass capacitors from HB to HS and from VCC to VSS are essential for proper operation. The capacitor should be located at the leads of the IC to minimize series inductance. The peak currents from LO and HO can be quite large. Any inductances in series with the bypass capacitor will cause voltage ringing at the leads of the IC which must be avoided for reliable operation.

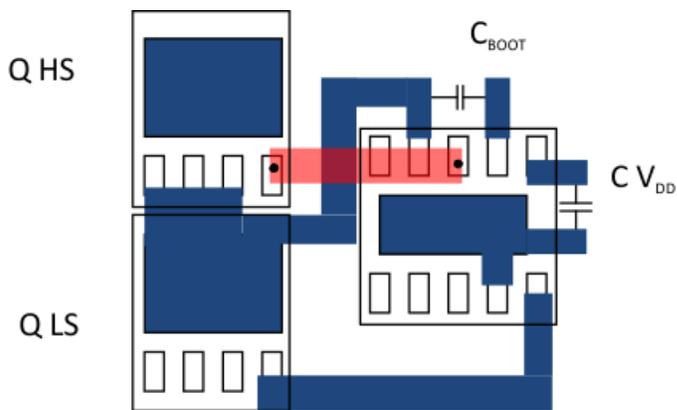
## 10 Layout

### 10.1 Layout Guidelines

The optimum performance of high- and low-side gate drivers cannot be achieved without taking due considerations during circuit board layout. Following points are emphasized.

1. A low ESR or ESL capacitor must be connected close to the IC, and between  $V_{DD}$  and  $V_{SS}$  pins and between HB and HS pins to support high peak currents being drawn from  $V_{DD}$  during turnon of the external MOSFET.
2. To prevent large voltage transients at the drain of the top MOSFET, a low ESR electrolytic capacitor must be connected between MOSFET drain and ground ( $V_{SS}$ ).
3. To avoid large negative transients on the switch node (HS) pin, the parasitic inductances in the source of top MOSFET and in the drain of the bottom MOSFET (synchronous rectifier) must be minimized.
4. Grounding considerations:
  - The first priority in designing grounding connections is to confine the high peak currents from charging and discharging the MOSFET gate in a minimal physical area. This decreases the loop inductance and minimize noise issues on the gate terminal of the MOSFET. The MOSFETs must be placed as close as possible to the gate driver.
  - The second high current path includes the bootstrap capacitor, the bootstrap diode, the local ground referenced bypass capacitor and low side MOSFET body diode. The bootstrap capacitor is recharged on the cycle-by-cycle basis through the bootstrap diode from the ground referenced  $V_{DD}$  bypass capacitor. The recharging occurs in a short time interval and involves high peak current. Minimizing this loop length and area on the circuit board is important to ensure reliable operation.
5. The resistor on the RDT pin must be placed very close to the IC and separated from high current paths to avoid noise coupling to the time delay generator which could disrupt timer operation.

### 10.2 Layout Example



**Figure 24. Component Placement**

## 11 デバイスおよびドキュメントのサポート

### 11.1 ドキュメントのサポート

#### 11.1.1 関連資料

関連資料については、以下を参照してください。

『[AN-1187 リードレス・リードフレーム・パッケージ\(LLP\)](#)』(SNOA401)

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### 11.3 コミュニティ・リソース

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### 11.6 Glossary

**SLYZ022** — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

## 12 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。これらの情報は、指定のデバイスに対して提供されている最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

**PACKAGING INFORMATION**

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
<a href="#">LM5105SD/NOPB</a>	Active	Production	WSON (DPR)   10	1000   SMALL T&R	Yes	NIPDAU   SN	Level-1-260C-UNLIM	-40 to 125	L5105SD
LM5105SD/NOPB.A	Active	Production	WSON (DPR)   10	1000   SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	L5105SD
LM5105SD/NOPB.B	Active	Production	WSON (DPR)   10	1000   SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	L5105SD
<a href="#">LM5105SDX/NOPB</a>	Active	Production	WSON (DPR)   10	4500   LARGE T&R	Yes	NIPDAU   SN	Level-1-260C-UNLIM	-40 to 125	L5105SD
LM5105SDX/NOPB.A	Active	Production	WSON (DPR)   10	4500   LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	L5105SD
LM5105SDX/NOPB.B	Active	Production	WSON (DPR)   10	4500   LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	L5105SD

<sup>(1)</sup> **Status:** For more details on status, see our [product life cycle](#).

<sup>(2)</sup> **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

<sup>(4)</sup> **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

<sup>(6)</sup> **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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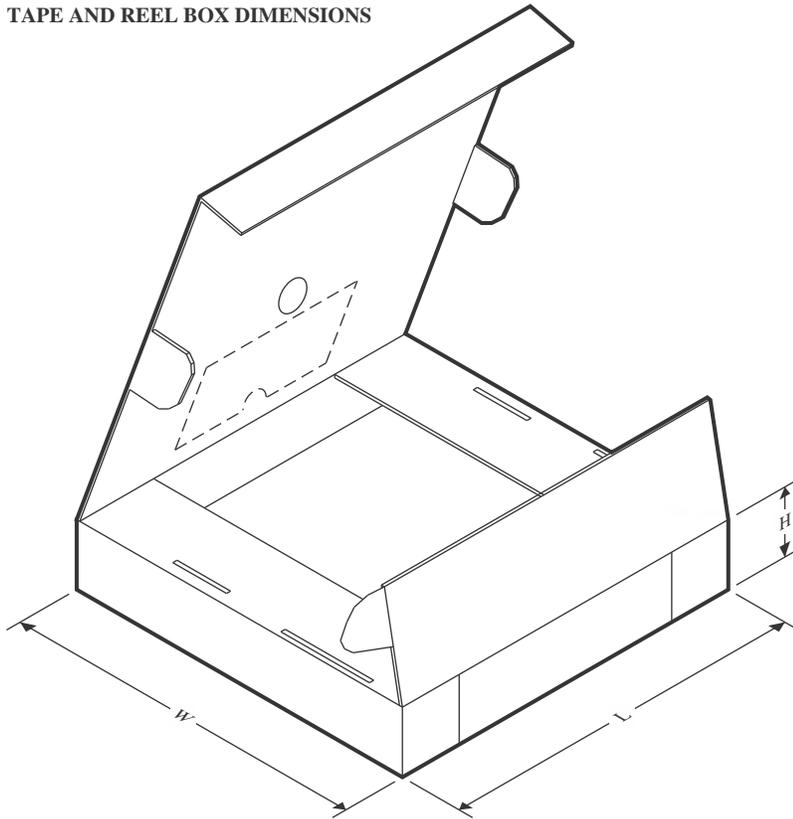


**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**

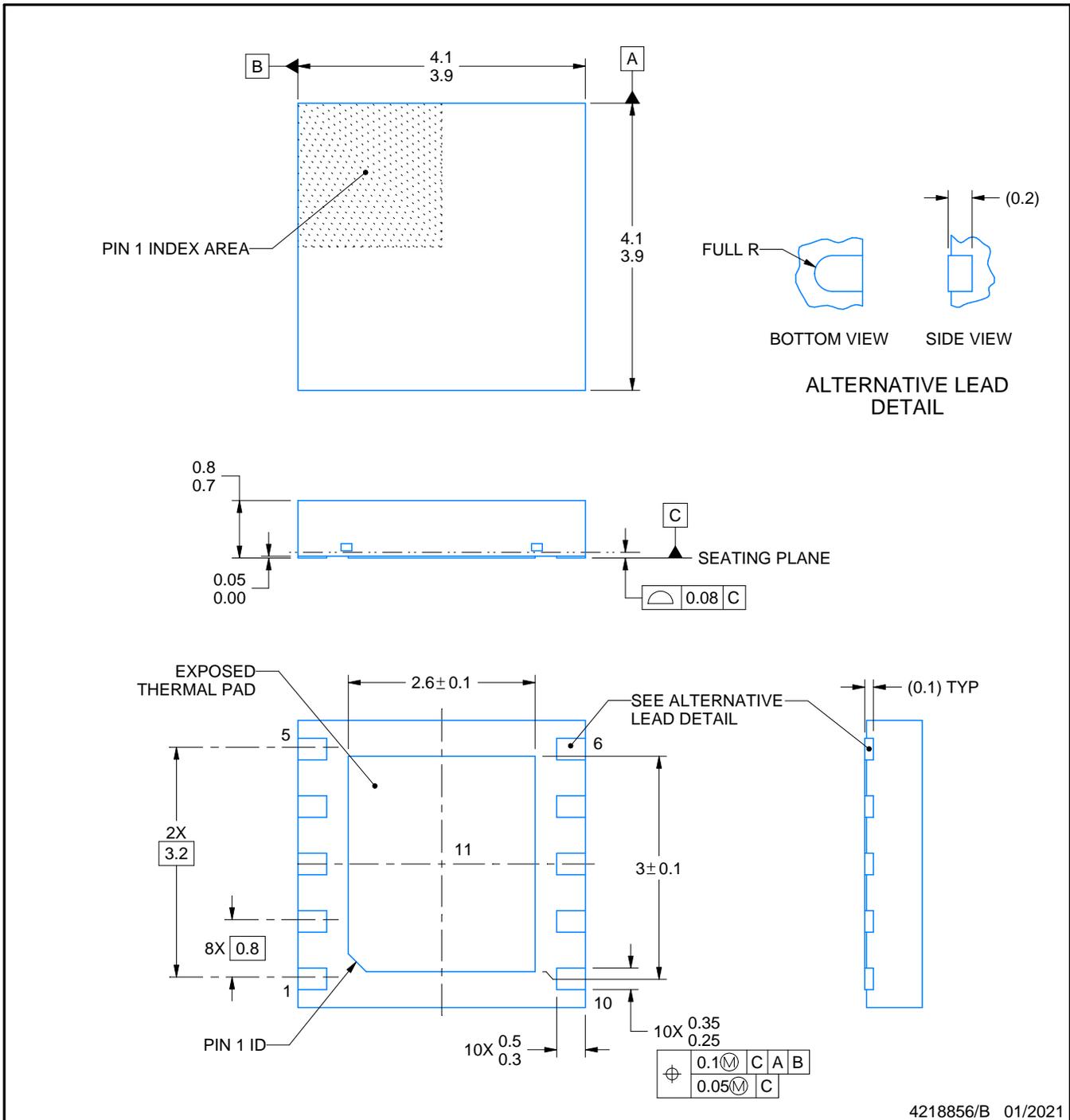
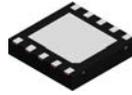

\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM5105SD/NOPB	WSON	DPR	10	1000	177.8	12.4	4.3	4.3	1.3	8.0	12.0	Q1
LM5105SDX/NOPB	WSON	DPR	10	4500	330.0	12.4	4.3	4.3	1.3	8.0	12.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM5105SD/NOPB	WSON	DPR	10	1000	208.0	191.0	35.0
LM5105SDX/NOPB	WSON	DPR	10	4500	367.0	367.0	35.0



**NOTES:**

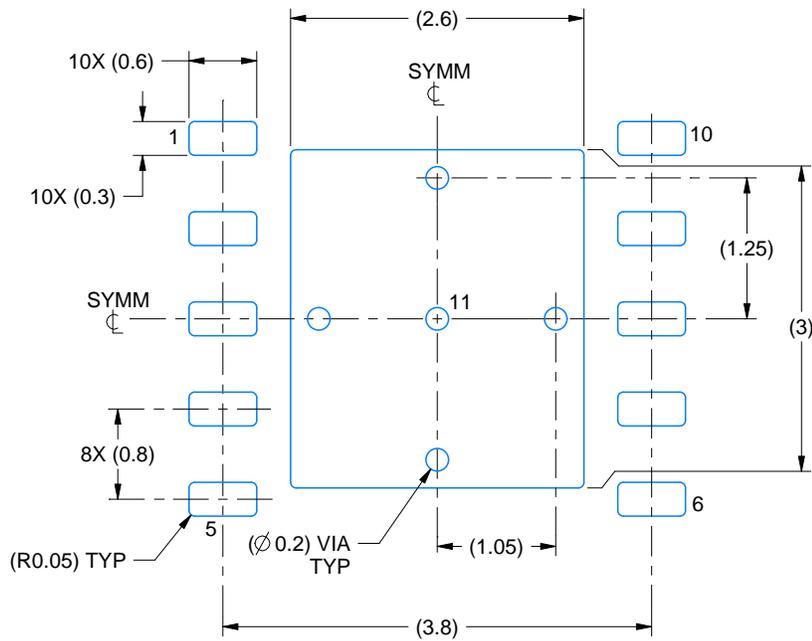
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

# EXAMPLE BOARD LAYOUT

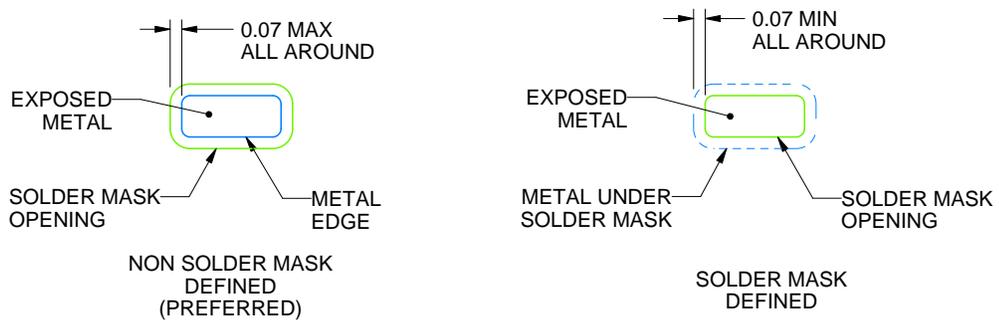
DPR0010A

WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:15X



SOLDER MASK DETAILS

4218856/B 01/2021

NOTES: (continued)

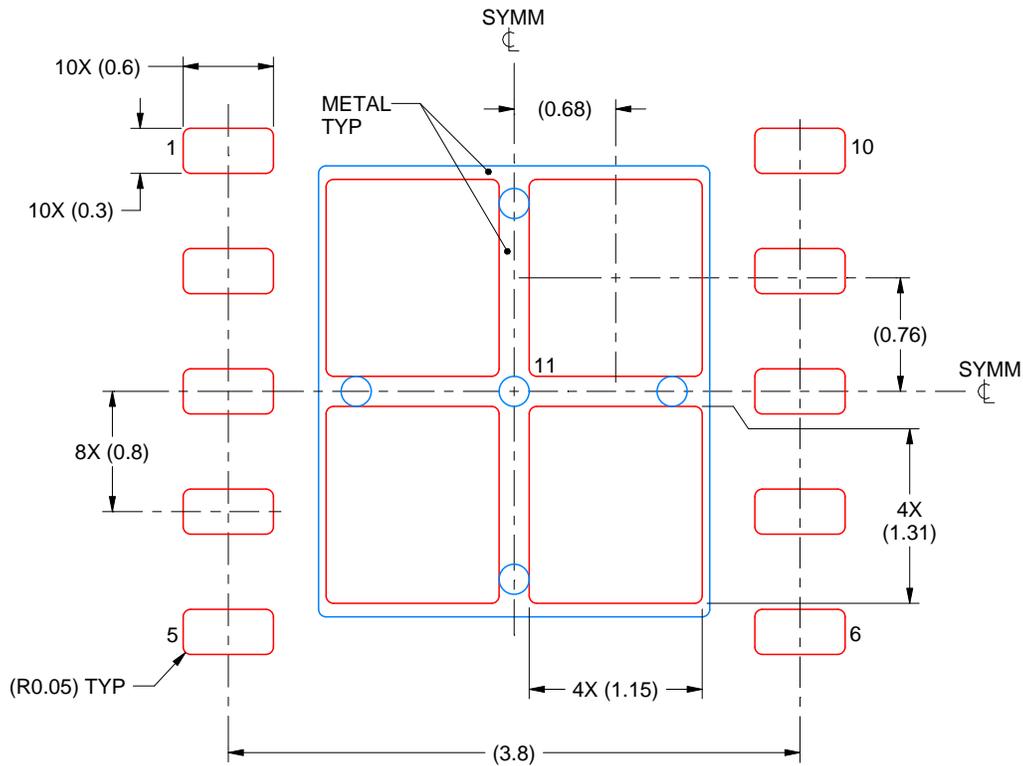
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 ([www.ti.com/lit/slua271](http://www.ti.com/lit/slua271)).

# EXAMPLE STENCIL DESIGN

DPR0010A

WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 11:  
77% PRINTED SOLDER COVERAGE BY AREA  
SCALE:20X

4218856/B 01/2021

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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