TEXAS INSTRUMENTS
LM5143-Q1
JAJSGF1C – OCTOBER 2018 – REVISED JUNE 2021

LM5143-Q1 低 I_Q の 車載用 3.5V～65V デュアル同期整流降圧コントローラ

1 特長

- 車載アプリケーション用に AEC-Q100 認定取得済み
  - デバイス温度グレード 1：–40℃～+125℃の動作時周囲温度範囲
- 機能安全対応
  - 機能安全システムの設計に役立つ資料を利用可能
- 多用途な同期整流降圧 DC/DC コントローラ
  - 3.5V～65V の広い入力電圧範囲
  - 精度 1% の固定 3.3V、5V 出力または可変出力 (0.6V～55V)
  - 最大接合部温度：150℃
  - シャットダウン・モード電流：4μA (標準値)
  - 無負荷時のスタンバイ電流：15μA (標準値)
- 2 つのインターリーブ同期整流降圧チャネル
  - 2 チャネルまたは単一出力多相
  - 65ns の $t_{ON(min)}$ により高い V_{IN}/V_{OUT} 比を実現
  - 60ns の $t_{OFF(min)}$ により低ドロップアウトを実現
- 本質的な保護機能による堅牢な設計
  - ヒカップ・モードによる過電流保護
  - 独立した ENABLE および PGOOD 機能
  - VCC、VDDA、ゲート駆動の UVLO 保護
  - ヒステリシス付きのサーマル・シャットダウン保護
- 超低 EMI 要件に最適化
  - スルーレート制御された適応型ゲート・ドライバ
  - スペクトラム拡散によりピーク・エミッションを削減
  - CISPR 25 Class 5 要件に対して最適化
- スイッチング周波数：100kHz～2.2MHz
  - SYNC In および SYNC Out 機能
  - ダイオード・エミュレーションまたは FPWM を選択可能
- ウェッタブル・フランク・ピン付きの VQFNP-40 パッケージ
- WEBENCH® Power Designer により、LM5143-Q1 を使用するカスタム設計を作成

2 アプリケーション

- 車載電子システム
- インフォテインメント・システム、インストルメント・クラスタ
- 先進運転支援システム (ADAS)

3 概要

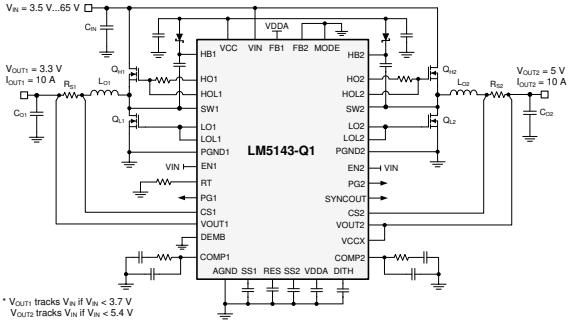
LM5143-Q1 は、大電流の単一出力またはデュアル出力に対応する 65V 同期整流降圧 DC/DC コントローラです。インターリーブ方式のスタック可能な電流モード制御アーキテクチャにより、容易なループ補償、高速な過渡応答、優れた負荷 / ライン制御、並列化した相での正確なカレント・シェア (電流共有) を実現し、より大きな出力電流に対応します。最小オン時間 65ns のハイサイド・スイッチは大きな降圧率に対応できるため、12V、24V、48V の車載入力から低電圧レールへの直接変換が可能になり、システムの複雑性とソリューション・コストを下げることができます。LM5143-Q1 は最低 3.5V の入力電圧ディップ時にも動作を継続でき、必要に応じてほぼ 100% のデューティ・サイクルで動作できます。

電流検出ではインダクタの DCR を使用して最高水準の効率を実現したり、オプションのシャント抵抗で高精度を実現できます。無負荷時静止電流 (出力電圧をレギュレートした状態) は 15μA であるため、バッテリ駆動システムの動作時間を延長できます。LM5143-Q1 に、スイッチング・レギュレータの出力や他の利用可能な電源から電力を供給することで、入力時静止電流と電力損失をさらに低減できます。

製品情報

部品番号	パッケージ(1)	本体サイズ (公称)
LM5143-Q1	VQFNP (40)	6.00mm × 6.00mm

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。



高効率デュアル降圧レギュレータ

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4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision B (October 2019) to Revision C (June 2021)	Page
• 「機能安全」の箇条書き項目が含まれるようにセクション 1 を更新	1
• データシートのタイトルから「DC/DC」を削除	1
• 文書全体にわたって表、図、相互参照の採番方法を更新	1
• Added the Mode pin to the *Absolute Maximum Ratings* and *Recommended Operating Conditions*	7
• Changed resistor value from 100 k to 220 k for $t_{SYNCOUT1}$ and $t_{SYNCOUT2}$	8
• Added note in *セクション 9.2.1.2.7*	46
• Updated *セクション 11.2*	57
• Added 表 12-1 in *セクション 12*	59

Changes from Revision A (May 2019) to Revision B (October 2019)	Page
• デバイス・ステータスを「事前情報」から「量産データ」に変更	1
• 「特長」の低 EMI の箇条書き項目を追加	1

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5 概要 (続き)

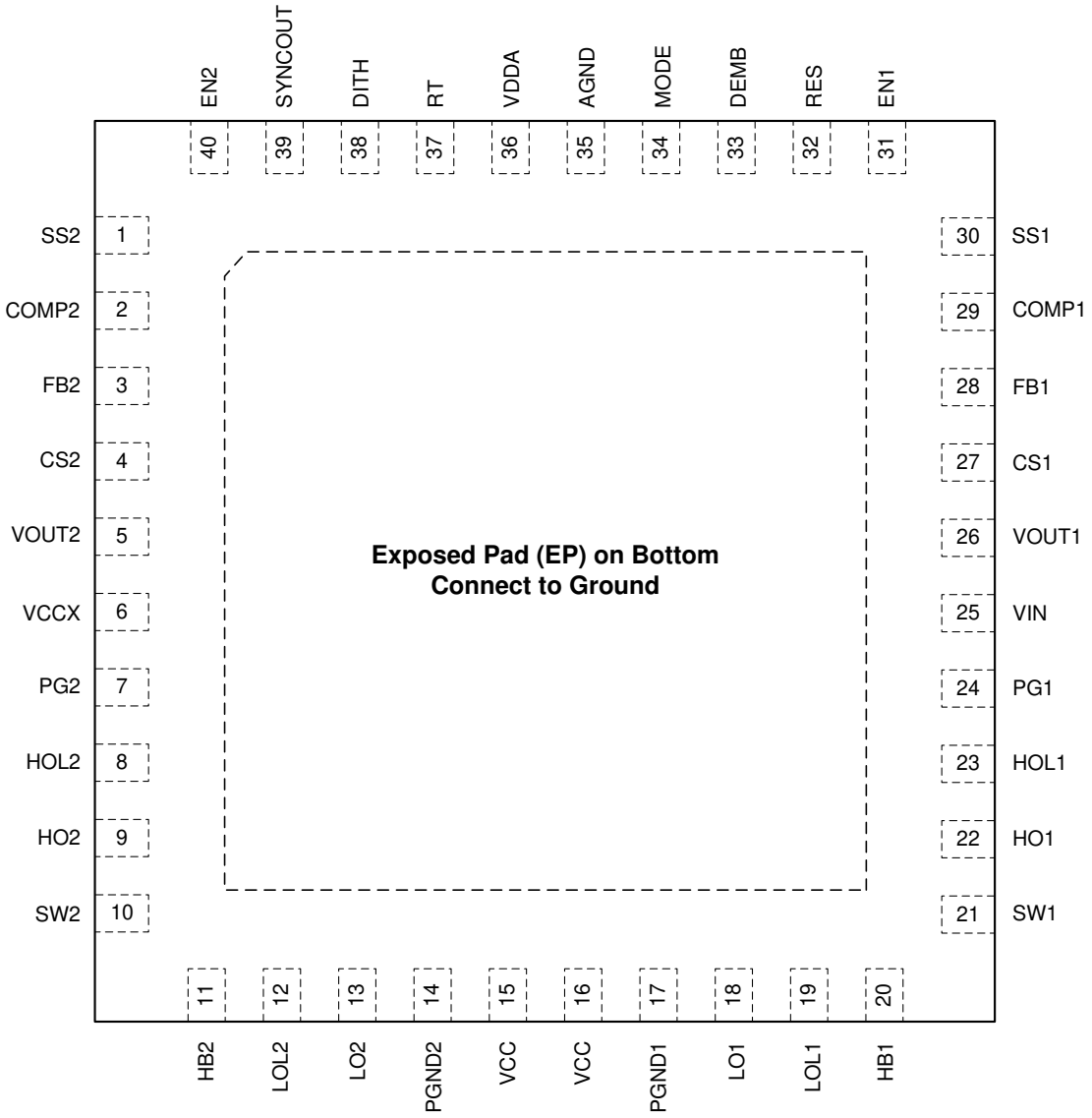
CISPR 25 および車載 EMI 要件への準拠を容易にする複数の機能も搭載されています。可変スルーレート制御により適応的にタイミング制御された大電流 MOSFET ゲート・ドライバは、スイッチング遷移時のボディ・ダイオードの導通を最小限に抑え、スイッチング損失を低減するとともに、高入力電圧および高スイッチング周波数時の熱および EMI 性能を高めます。入力コンデンサのリップル電流を小さくし、EMI フィルタを小型化するために、2 つの出力の 180° インターリーブ動作もサポートしています。90° 位相がずれたクロック出力はカスケード、マルチチャネル、多相電力段に最適です。スイッチング周波数は抵抗により最大 2.2MHz まで設定可能で、最大 2.5MHz の外部クロック・ソースと同期できるため、ノイズに敏感な用途でビート周波数を除去できます。オプションの三角スペクトラム拡散変調により、EMI 性能をさらに向上させることができます。

LM5143-Q1 の追加機能として、最大 150℃の接合部温度での動作、ユーザー選択可能なダイオード・エミュレーションによる軽負荷時消費電流の低減、設定可能なソフト・スタート機能、オープンドレインのパワー・グッド・フラグによるフォルト報告と出力監視、独立したイネーブル入力、プリバイアスされた負荷への単調なスタートアップ、内蔵 VCC バイアス電源レギュレータ、プログラム可能なヒカップ・モード過負荷保護、自動回復機能付きサーマル・シャットダウン保護があります。

LM5143-Q1 コントローラは、6mm × 6mm の放熱特性に優れた 40 ピンのウェッタブル・フランク・ピン付き VQFNP パッケージで供給されるため、製造現場で光学検査を容易に行えます。

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6 Pin Configuration and Functions



Connect Exposed Pad on the bottom to AGND and PGND on the PCB.

図 6-1. RWG Package 40-Pin VQFNP with Wettable Flanks (Top View)

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表 6-1. Pin Functions

PIN		I/O [1]	DESCRIPTION
NO.	NAME		
1	SS2	I	Channel 2 soft-start programming pin. An external ceramic capacitor and an internal 20-µA current source set the ramp rate of the internal error amplifier reference during soft start. Pulling SS2 below 150 mV turns off the channel 2 gate driver outputs, but all the other functions remain active.
2	COMP2	O	Output of the channel 2 transconductance error amplifier. COMP2 is high impedance in interleave or slave mode.
3	FB2	I	Feedback input of channel 2. Connect FB2 to VDDA for a 3.3-V output or connect FB2 to AGND for a fixed 5-V output. A resistive divider from VOUT2 to FB2 sets the output voltage level between 0.6 V and 55 V. The regulation threshold at FB2 is 0.6 V.
4	CS2	I	Channel 2 current sense amplifier input. Connect CS2 to the inductor side of the external current sense resistor (or to the relevant sense capacitor terminal if inductor DCR current sensing is used) using a low-current Kelvin connection.
5	VOUT2	I	Output voltage sense and the current sense amplifier input of channel 2. Connect VOUT2 to the output side of the channel 2 current sense resistor (or to the relevant sense capacitor terminal if inductor DCR current sensing is used).
6	VCCX	P	Optional input for an external bias supply. If V_{VCCX} > 4.3 V, VCCX is internally connected to VCC and the internal VCC regulator is disabled. Connect a ceramic capacitor between VCCX and PGND.
7	PG2	O	An open-collector output which goes low if VOUT2 is outside a specified regulation window.
8	HOL2	O	Channel 2 high-side gate driver turnoff output.
9	HO2	O	Channel 2 high-side gate driver turnon output.
10	SW2	P	Switching node of the channel 2 buck regulator. Connect to the bootstrap capacitor, the source terminal of the high-side MOSFET, and the drain terminal of the low-side MOSFET.
11	HB2	P	Channel 2 high-side driver supply for bootstrap gate drive.
12	LOL2	O	Channel 2 low-side gate driver turnoff output.
13	LO2	O	Channel 2 low-side gate driver turnon output.
14	PGND2	G	Power ground connection pin for low-side NMOS gate driver.
15, 16	VCC	P	VCC bias supply pin. Pins 15 and 16 must to be connected together on the PCB. Connect ceramic capacitors between VCC and PGND1 and between VCC and PGND2.
17	PGND1	G	Power ground connection pin for low-side NMOS gate driver.
18	LO1	O	Channel 1 low-side gate driver turnon output.
19	LOL1	O	Channel 1 low-side gate driver turnoff output.
20	HB1	P	Channel 1 high-side driver supply for bootstrap gate drive.
21	SW1	P	Switching node of the channel 1 buck regulator. Connect to the channel 1 bootstrap capacitor, the source terminal of the high-side MOSFET and the drain terminal of the low-side MOSFET.
22	HO1	O	Channel 1 high-side gate driver turnon output.
23	HOL1	O	Channel 1 high-side gate driver turnoff output.
24	PG1	O	An open-collector output that goes low if VOUT1 is outside a specified regulation window.
25	VIN	P	Supply voltage input source for the VCC regulators.
26	VOUT1	I	Output voltage sense and the current sense amplifier input of channel 1. Connect VOUT1 to the output side of the channel 1 current sense resistor (or to the relevant sense capacitor terminal if inductor DCR current sensing is used).
27	CS1	I	Channel 1 current sense amplifier input. Connect CS1 to the inductor side of the external current sense resistor (or to the relevant sense capacitor terminal if inductor DCR current sensing is used) using a low-current Kelvin connection.
28	FB1	I	Feedback input of channel 1. Connect the FB1 pin to VDDA for a 3.3-V output or connect FB1 to AGND for a 5-V output. A resistive divider from VOUT1 to FB1 sets the output voltage level between 0.6 V and 55 V. The regulation threshold at FB1 is 0.6 V.
29	COMP1	O	Output of the channel 1 transconductance error amplifier (EA).
30	SS1	I	Channel 1 soft-start programming pin. An external capacitor and an internal 20-µA current source set the ramp rate of the internal error amplifier reference during soft start. Pulling the SS1 voltage below 150 mV turns off the channel 1 gate driver outputs, but the all the other functions remain active.

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表 6-1. Pin Functions (continued)

PIN		I/O (1)	DESCRIPTION
NO.	NAME		
31	EN1	I	An active high input (V_{EN1} > 2 V) enables Output 1. If Outputs 1 and 2 are disabled, the LM5143-Q1 is in shutdown mode unless a SYNC signal is present at DEMB. EN1 must never be floating.
32	RES	O	Restart timer pin. An external capacitor configures the hiccup-mode current limiting. A capacitor at the RES pin determines the time the controller remains off before automatically restarting in hiccup mode. The two regulator channels operate independently. One channel can operate in normal mode while the other is in hiccup-mode overload protection. The hiccup mode commences when either channel experiences 512 consecutive PWM cycles with cycle-by-cycle current limiting. Connect RES to VDDA during power-up to disable hiccup-mode protection.
33	DEMB	I	Diode Emulation pin. Connect DEMB to AGND to enable diode emulation mode. Connect DEMB to VDDA to operate the LM5143-Q1 in forced PWM (FPWM) mode with continuous conduction at light loads. DEMB can also be used as a synchronization input to synchronize the internal oscillator to an external clock.
34	MODE	I	Connect MODE to AGND or VDDA for dual-output or interleaved single-output operation, respectively. This also configures the LM5143-Q1 with an EA transconductance of 1200 µS. Connecting a 10-kΩ resistor between MODE and AGND sets the LM5143-Q1 for dual-output operation with an ultra-low I_Q mode and an EA transconductance of 60 µS.
35	AGND	G	Analog ground connection. Ground return for the internal voltage reference and analog circuits.
36	VDDA	O	Internal analog bias regulator output. Connect a ceramic decoupling capacitor from VDDA to AGND.
37	RT	I	Frequency programming pin. A resistor from RT to AGND sets the oscillator frequency between 100 kHz and 2.2 MHz.
38	DITH	I	A capacitor connected between the DITH pin and AGND is charged and discharged with a 20-µA current source. If dithering is enabled, the voltage on the DITH pin ramps up and down modulating the oscillator frequency between –5% and +5% of the internal oscillator. Connecting DITH to VDDA during power-up disables the dither feature. DITH is ignored if an external synchronization clock is used.
39	SYNCOUT	O	SYNCOUT is a logic level signal with a rising edge approximately 90° lagging HO2 (or 90° leading HO1). When the SYNCOUT signal is used to synchronize a second LM5143-Q1 controller, all phases are 90° out of phase.
40	EN2	I	An active high input (V_{EN2} > 2 V) enables Output 2. If Outputs 1 and 2 are disabled, the LM5143-Q1 is in shutdown mode unless a SYNC signal is present on DEMB. EN2 must never be floating.

(1) P = Power, G = Ground, I = Input, O = Output

6.1 Wettable Flanks

100% automated visual inspection (AVI) post-assembly is typically required to meet requirements for high reliability and robustness. Standard quad-flat no-lead (QFN) packages do not have solderable or exposed pins and terminals that are easily viewed. It is therefore difficult to visually determine whether or not the package is successfully soldered onto the printed-circuit board (PCB). The wettable-flank process was developed to resolve the issue of side-lead wetting of leadless packaging. The LM5143-Q1 is assembled using a 40-pin VQFNP package with wettable flanks to provide a visual indicator of solderability, which reduces the inspection time and manufacturing costs.

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7 Specifications

7.1 Absolute Maximum Ratings

Over the recommended operating junction temperature range of –40°C to 150°C (unless otherwise noted)(1)

		MIN	MAX	UNIT
Input voltage	VIN to PGND	–0.3	70	V
	SW1, SW2 to PGND	–0.3	70	
	SW1, SW2 to PGND (20-ns transient)	–5		
	HB1 to SW1, HB2 to SW2	–0.3	6.5	
	HB1 to SW1, HB2 to SW2 (20-ns transient)	–5		
	HO1 to SW1, HOL1 to SW1, HO2 to SW2, HOL2 to SW2	–0.3	V_{HB} + 0.3	
	HO1 to SW1, HOL1 to SW1, HO2 to SW2, HOL2 to SW2 (20-ns transient)	–5		
	LO1, LOL1, LO2, LOL2 to PGND	–0.3	V_{VCC} + 0.3	
	LO1, LOL1, LO2, LOL2 to PGND (20-ns transient)	–1.5	V_{VCC} + 0.3	
	SS1, SS2, COMP1, COMP2, RES, RT, MODE, DITH to AGND	–0.3	V_{VDDA} + 0.3	
	EN1, EN2 to PGND	–0.3	70	
	VCC, VCCX, VDDA, PG1, PG2, DEMB, FB1, FB2 to AGND	–0.3	6.5	
	VOUT1, VOUT2, CS1, CS2	–0.3	60	
	VOUT1 to CS1, VOUT2 to CS2	–0.3	0.3	
PGND to AGND		–0.3	0.3	V
Operating junction temperature, T_J		–40	150	°C
Storage temperature, T_{stg}		–40	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC-Q100-002 (1) HBM ESD Classification Level 2		±2000	V
		Charge device model (CDM), per AEC-Q100-011, CDM ESD Classification Level C4B	Corner pins	±750	V
			Other pins	±500	V

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification

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7.3 Recommended Operating Conditions

Over the recommended operating junction temperature range of –40°C to 150°C (unless otherwise noted).

			MIN	NOM	MAX	UNIT
V_{IN}	Input voltage range	VIN to PGND	–0.3		65	V
		SW1, SW2 to PGND	–0.3		65	
		HB1 to SW1, HB2 to SW2	–0.3	5	5.25	
		HO1 to SW1, HOL1 to SW1, HO2 to SW2, HOL2 to SW2	–0.3		V_{HB} + 0.3	
		LO1, LOL1, LO2, LOL2 to PGND	–0.3	5	5.25	
		FB1, FB2, SS1, SS2, COMP1, COMP2, RES, DEMB, RT, MODE, DITH to AGND	–0.3		5.25	
		EN1, EN2 to PGND	–0.3		65	
		VCC, VCCX, VDDA to PGND	–0.3	5	5.25	
		VOUT1, VOUT2, CS1, CS2 to PGND	–0.3		55	
	PGND to AGND		–0.3		0.3	
T_J	Operating junction temperature		–40		150	°C

7.4 Thermal Information

THERMAL METRIC[1]		LM5143-Q1 RWG (VQFNP) 40 PINS	UNIT
$R_{\Theta JA}$	Junction-to-ambient thermal resistance	34.8	°C/W
$R_{\Theta JC(top)}$	Junction-to-case (top) thermal resistance	22.8	°C/W
$R_{\Theta JB}$	Junction-to-board thermal resistance	9.5	°C/W
$R_{\Theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	1.3	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	9.4	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	0.3	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report, SPRA953.

7.5 Electrical Characteristics

Over the recommended operating junction temperature range of –40°C to 150°C (unless otherwise noted), Typical values correspond to T_J = 25°C, V_{VIN} = 12 V, V_{VCCX} = 5 V, V_{VOUT1} = 3.3 V, V_{VOUT2} = 5 V, V_{EN1} = V_{EN2} = 5 V, R_{RT} = 10 kΩ, F_{SW} = 2.2 MHz, no-load on the drive outputs (HO1, HOL1, LO1, LOL1, HO2, HOL2, LO2 and LOL2).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT VOLTAGE (VIN)						
$I_{SHUTDOWN}$	Shutdown mode current	V_{IN} = 12 V, V_{EN1} = V_{EN2} = 0 V		3.3	7	µA
$I_{STANDBY1}$	Standby current, channel 1	V_{IN} = 12 V, V_{EN1} = 5 V, V_{EN2} = 0 V, V_{VOUT1} = 3.3 V, in regulation, no-load, not switching, DEMB = MODE = GND		24	31	µA
$I_{STANDBY2}$	Standby current, channel 2	V_{IN} = 12 V, V_{EN1} = 0 V, V_{EN2} = 5 V, V_{VOUT2} = 5 V, in regulation, no-load, not switching, DEMB = MODE = AGND		25	43	µA
$I_{STANDBY3}$	Standby current, channel 1, ultra-low I_Q mode	V_{IN} = 12 V, V_{EN1} = 5 V, V_{EN2} = 0 V, V_{VOUT1} = 3.3 V, in regulation, no-load, not switching, DEMB = GND, R_{MODE} = 10 kΩ to GND		15	21	µA
$I_{STANDBY4}$	Standby current, channel 2, ultra-low I_Q mode	V_{IN} = 12 V, V_{EN1} = 0 V, V_{EN2} = 5 V, V_{VOUT2} = 5 V, in regulation, no-load, not switching, DEMB = GND, R_{MODE} = 10 kΩ to AGND		21	33	µA
BIAS REGULATOR (VCC)						

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Over the recommended operating junction temperature range of –40°C to 150°C (unless otherwise noted), Typical values correspond to T_J = 25°C, V_{VIN} = 12 V, V_{VCCX} = 5 V, V_{VOUT1} = 3.3 V, V_{VOUT2} = 5 V, V_{EN1} = V_{EN2} = 5 V, R_{RT} = 10 kΩ, F_{SW} = 2.2 MHz, no-load on the drive outputs (HO1, HOL1, LO1, LOL1, HO2, HOL2, LO2 and LOL2).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{VCC-REG}$	VCC regulation voltage	V_{VIN} = 12 V, I_{VCC} = 100 mA, V_{VCCX} = 0 V	4.7	5	5.3	V
$V_{CC-UVLO}$	VCC UVLO rising threshold	V_{VCC} rising	3.2	3.3	3.4	V
$V_{VCC-HYST}$	VCC UVLO hysteresis			175		mV
$I_{VCC-LIM}$	VCC sourcing current limit			-250		mA
ANALOG BIAS (VDDA)						
$V_{VDDA-REG}$	VDDA regulation voltage		4.75	5	5.25	V
$V_{VDDA-UVLO}$	VDDA UVLO rising threshold	V_{VCC} rising, V_{VCCX} = 0 V	3.1	3.2	3.3	V
$V_{VDDA-HYST}$	VDDA UVLO hysteresis	V_{VCCX} = 0 V		90		mV
R_{VDDA}	VDDA resistance	V_{VCCX} = 0 V		20		Ω
EXTERNAL BIAS (VCCX)						
$V_{VCCX-ON}$	$VCCX_{(ON)}$ rising threshold		4.1	4.3	4.4	V
R_{VCCX}	VCCX resistance	V_{VCCX} = 5 V		1.3		Ω
$V_{VCCX-HYST}$	VCCX hysteresis voltage			130		mV
CURRENT LIMIT (CS1, CS2)						
V_{CS1}	Current limit threshold 1	Measured from CS1 to VOUT1	66	73	80	mV
V_{CS2}	Current limit threshold 2	Measured from CS2 to VOUT2	66	73	80	mV
$T_{CS-DELAY}$	CS delay to output			40		ns
G_{CS}	CS amplifier gain		11.4	12	12.6	V/V
$I_{CS-BIAS}$	CS amplifier input bias current				15	nA
POWER GOOD (PG1, PG2)						
$PG1_{UV}$	PG1 UV trip level	Falling with respect to the regulation voltage	90%	92%	94%	
$PG2_{UV}$	PG2 UV trip level	Falling with respect to the regulation voltage	90%	92%	94%	
$PG1_{OV}$	PG1 OV trip level	Rising with respect to the regulation voltage	108%	110%	112%	
$PG2_{OV}$	PG2 OV trip level	Rising with respect to the regulation voltage	108%	110%	112%	
$PG1_{UV-HYST}$	PG1 UV hysteresis	Rising with respect to the regulation voltage		3.4%		
$PG1_{OV-HYST}$	PG1 OV hysteresis	Rising with respect to the regulation voltage		3.4%		
$PG2_{UV-HYST}$	PG2 UV hysteresis	Rising with respect to the regulation voltage		3.4%		
$PG2_{OV-HYST}$	PG2 OV hysteresis	Rising with respect to the regulation voltage		3.4%		
V_{OL-PG1}	PG1 voltage	Open collector, I_{PG1} = 2 mA			0.4	V
V_{OL-PG2}	PG2 voltage	Open collector, I_{PG2} = 2 mA			0.4	V
$T_{PG-RISE-DLY}$	OV filter time	V_{OUT} rising		25		µs
$T_{PG-FALL-DLY}$	UV filter time	V_{OUT} falling		22		µs
HIGH-SIDE GATE DRIVER (HO1, HO2, HOL1, HOL2)						
V_{HO-LOW}	HO low-state output voltage	I_{HO} = 100 mA		0.04		V
$V_{HO-HIGH}$	HO high-state output voltage	I_{HO} = –100 mA, $V_{HO-HIGH}$ = V_{HB} – V_{HO}		0.09		V
$t_{HO-RISE}$	HO rise time (10% to 90%)	C_{LOAD} = 2.7 nF		24		ns
$t_{HO-FALL}$	HO fall time (90% to 10%)	C_{LOAD} = 2.7 nF		24		ns
I_{HO-SRC}	HO peak source current	V_{HO} = V_{SW} = 0 V, V_{HB} = 5 V, V_{VCCX} = 5 V		3.25		A
$I_{HO-SINK}$	HO peak sink current	V_{VCCX} = 5 V		4.25		A
V_{BT-UV}	BOOT UVLO	V_{VCC} falling		2.4		V
$V_{BT-UV-HYS}$	BOOT UVLO hysteresis			113		mV
I_{BOOT}	BOOT quiescent current			1.2		µA
LOW-SIDE GATE DRIVER (LO1, LO2, LOL1, LOL2)						
V_{LO-LOW}	LO low-state output voltage	I_{LO} = 100 mA		0.04		V

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PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{LO-HIGH}$	LO high-state output voltage	I_{LO} = –100 mA		0.07		V
$t_{LO-RISE}$	LO rise time (10% to 90%)	C_{LOAD} = 2.7 nF		4		ns
$t_{LO-FALL}$	LO fall time (90% to 10%)	C_{LOAD} = 2.7 nF		3		ns
$I_{LO-SOURCE}$	LO peak source current	V_{HO} = V_{SW} = 0 V, V_{HB} = 5 V, V_{VCCX} = 5 V		3.25		A
$I_{LO-SINK}$	LO peak sink current	V_{VCCX} = 5 V		4.25		A
RESTART (RES)						
$I_{RES-SRC}$	RES current source			20		µA
V_{RES-TH}	RES threshold			1.2		V
HIC_{CYCLES}	HICCUP mode fault			512		cycles
R_{RES-PD}	RES pull-down resistance			5.5		Ω
OUTPUT VOLTAGE SETPOINT (VOUT1, VOUT2)						
$VOUT_{33}$	3.3 V output voltage setpoint	V_{FB} = 0 V, V_{IN} = 3.5 V to 65 V	3.267	3.3	3.33	V
$VOUT_{50}$	5 V output voltage setpoint	V_{FB} = 5 V, V_{IN} = 5.5 V to 65 V	4.95	5	5.05	V
FEEDBACK (FB1, FB2)						
$V_{FB-3V3-SEL}$	VOUT select threshold 3.3-V output		4.6			V
R_{FB-5V}	Resistance FB to AGND for 5-V output	V_{MODE} = 0 V or R_{MODE} = 10 kΩ			500	Ω
$R_{FB-EXTRES}$	Thevenin equivelent resistance	V_{MODE} = 0 V or R_{MODE} = 10 kΩ, V_{FB} < 2 V	5			kΩ
$V_{FB2-LOW}$	Master mode select logic level low	MODE = VDDA			0.8	V
$V_{FB2-HIGH}$	Master mode select logic level high	MODE = VDDA	2			V
$V_{FB1-LOW}$	Diode emulation logic level low in slave mode	MODE = FB2 = VDDA			0.8	V
$V_{FB1-HIGH}$	FPWM logic level high in slave mode	MODE = FB2 = VDDA	2			V
V_{FB-REG}	Regulated feedback voltage	T_J = –40°C to 125°C	0.594	0.6	0.606	V
ERROR AMPLIFIER (COMP1, COMP2)						
g_{m1}	EA transconductance	FB to COMP, R_{MODE} < 5 kΩ to AGND	1020	1200		µS
g_{m2}	EA transconductance, ultra-low I_Q mode	MODE = GND, R_{MODE} = 10 kΩ		65		µS
I_{FB}	Error amplifier input bias current				20	nA
$V_{COMP-CLMP}$	COMP clamp voltage	V_{FB} = 0 V		3.3		V
$I_{COMP-SLAVE}$	COMP leakage, slave mode	V_{COMP} = 1 V, MODE = FB2 = VCC			10	nA
$I_{COMP-INTLV}$	COMP2 leakage, Imode	V_{COMP} = 1 V, MODE = VCC, V_{FB2} = 0 V			10	nA
$I_{COMP-SRC1}$	EA source current	V_{COMP} = 1 V, V_{FB} = 0.4 V, V_{MODE} = 0 V		190		µA
$I_{COMP-SINK1}$	EA sink current	V_{COMP} = 1 V, V_{FB} = 0.8 V, V_{MODE} = 0 V		165		µA
$I_{COMP-SRC2}$	EA source current, ultra-low I_Q mode	V_{COMP} = 1 V, V_{FB} = 0.4 V, R_{MODE} = 10 kΩ to AGND		10		µA
$I_{COMP-SINK2}$	EA sink current, ultra-low I_Q mode	V_{COMP} = 1 V, V_{FB} = 0.8 V, R_{MODE} = 10 kΩ to AGND		12		µA
$V_{SS-OFFSET}$	EA SS offset with V_{FB} = 0 V	Raise V_{SS} until V_{COMP} > 300 mV		36		mV
ADAPTIVE DEADTIME CONTROL						
V_{GS-DET}	VGS detection threshold	VGS falling, no-load		2.5		V
t_{DEAD1}	HO off to LO on deadtime			22		ns
t_{DEAD2}	LO off to HO on deadtime			22		ns
DIODE EMULATION (DEMB)						
$V_{DEMB-LOW}$	DEMB input low threshold				0.8	V

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PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{DEMB_Rising}	DEMB input high threshold		2			V
V_{ZC-SW}	Zero-cross threshold	V_{DEMB} = 0 V		–6		mV
V_{ZC-SS}	Zero-cross threshold soft-start	DEMB = VCC, 50 SW cycles after first HO pulse		–5.4		mV
V_{ZC-DIS}	Zero-cross threshold disabled	DEMB = VCC, 1000 SW cycles after first HO pulse		200		mV
ENABLE (EN1, EN2)						
V_{EN-LOW}	EN1/2 low threshold	V_{VCCX} = 0 V			0.8	V
$V_{EN-HIGH-TH}$	EN1/2 high threshold	V_{VCCX} = 0 V	2			V
$I_{EN-LEAK}$	EN1/2 leakage currernt	EN1, EN2 logic inputs only		0.05		µA
SWITCHING FREQUENCY (RT)						
V_{RT}	RT regulation voltage	10 kΩ < R_{RT} < 220 kΩ		0.8		V
MODE						
$R_{MODE-HIGH}$	Resistance to AGND for ultra-low I_Q				5	kΩ
$R_{MODE-LOW}$	Resistance to AGND for normal I_Q				0.5	kΩ
$V_{MODE-LOW}$	Non-interleaved mode input low threshold				0.8	V
$V_{MODE-HIGH}$	Interleaved mode input high threshold		2			V
SYNCHRONIZATION INPUT (SYNCIN)						
$V_{DEMB-LOW}$	DEMB input low threshold				0.8	V
$V_{DEMB-HIGH}$	DEMB input high threshold		2			V
$T_{SYNC-MIN}$	DEMB minimum pulse width	V_{MODE} = 0 V or R_{MODE} = 10 kΩ	20		250	ns
F_{SYNCIN}	External SYNC frequency range	V_{IN} = 8 V to 18 V, % of the nominal frequency set by R_{RT}	–20%		20%	
$t_{SYNCIN-HO1}$	Delay from DEMB rising to HO1 rising edge			100		ns
$t_{SYNCIN-SLAVE}$	Delay from DEMB falling edge to HO2 rising edge	Slave mode, MODE = FB2 = VCC		101		ns
$t_{DEMB-FILTER}$	Delay from DEMB low to diode emulation enable	V_{MODE} = 0 V or R_{MODE} = 10 kΩ	15		50	µs
$t_{AWAKE-FILTER}$	Maximum SYNC period to maintain standby state	V_{EN1} = V_{EN2} = 0 V		27		µs
SYNCHRONIZATION OUTPUT (SYNCOUT)						
$V_{SYNCOUT-LO}$	SYNCOUT low-state voltage	$I_{SYNCOUT}$ = 16 mA			0.8	V
$F_{SYNCOUT}$	SYNCOUT frequency	MODE = FB2 = VDDA			0	Hz
$t_{SYNCOUT1}$	Delay from HO2 rising edge to SYNCOUT rising edge	V_{DEMB} = 0 V, T_S = 1/F_{SW}, F_{SW} set by R_{RT} = 220 kΩ		2.5		µs
$t_{SYNCOUT2}$	Delay from HO2 rising edge to SYNCOUT falling edge	V_{DEMB} = 0 V, T_S = 1/F_{SW}, F_{SW} set by R_{RT} = 220 kΩ		7.5		µs
DITHER (DITH)						
I_{DITH}	Dither source/sink current			21		µA
$V_{DITH-HIGH}$	Dither high-level threshold			1.25		V
	Dither low-level threshold			1.15		V
SOFT START (SS1, SS2)						
I_{SS}	Soft-start current	V_{MODE} = 0 V	16	21	28	µA
R_{SS-PD}	Soft-start pull-down resistance	V_{MODE} = 0 V		3		Ω

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Over the recommended operating junction temperature range of –40°C to 150°C (unless otherwise noted), Typical values correspond to T_J = 25°C, V_{VIN} = 12 V, V_{VCCX} = 5 V, V_{VOUT1} = 3.3 V, V_{VOUT2} = 5 V, V_{EN1} = V_{EN2} = 5 V, R_{RT} = 10 kΩ, F_{SW} = 2.2 MHz, no-load on the drive outputs (HO1, HOL1, LO1, LOL1, HO2, HOL2, LO2 and LOL2).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{SS-FB}	SS to FB clamp voltage	$V_{CS} – V_{OUT}$ > 73 mV		125		mV
$I_{SS-SLAVE}$	SS leakage, slave mode	V_{SS} = 0.8 V, MODE = FB2 = VDDA		36		nA
$I_{SS-INTLV}$	SS2 leakage, interleaved mode	V_{SS} = 0.8 V, MODE = VDDA, V_{FB2} = 0 V		35		nA
THERMAL SHUTDOWN						
T_{SHD}	Thermal shutdown			175		°C
$T_{SHD-HYS}$	Thermal shutdown hysteresis			15		°C

7.6 Switching Characteristics

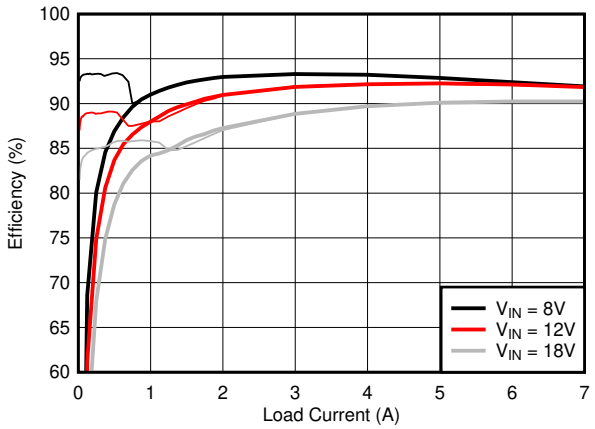
Over the recommended operating junction temperature range of –40°C to 150°C (unless otherwise noted). Typical values correspond to T_J = 25°C, V_{VIN} = 12 V, V_{VCCX} = 5 V, V_{VOUT1} = 3.3 V, V_{VOUT2} = 5 V, V_{EN1} = V_{EN2} = 5 V, R_{RT} = 10 kΩ, F_{SW} = 2.2 MHz, no-load on the gate driver outputs (HO1, HOL1, LO1, LOL1, HO2, HOL2, LO2, and LOL2).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
F_{SW1}	Switching frequency 1	R_{RT} = 100 kΩ	200	220	242	kHz
F_{SW2}	Switching frequency 2	R_{RT} = 10 kΩ		2.2		MHz
F_{SW3}	Switching frequency 3	R_{RT} = 220 kΩ		100		kHz
SLOPE2	Internal slope compensation 2	R_{RT} = 100 kΩ		64		mV/µs
SLOPE1	Internal slope compensation 1	R_{RT} = 10 kΩ		557		mV/µs
$t_{ON(min)}$	Minimum on-time			35	80	ns
$t_{OFF(min)}$	Minimum off-time			80	100	ns
$PH_{HO1-HO2}$	Phase between HO1 and HO2	DEMB = MODE = AGND		180		°

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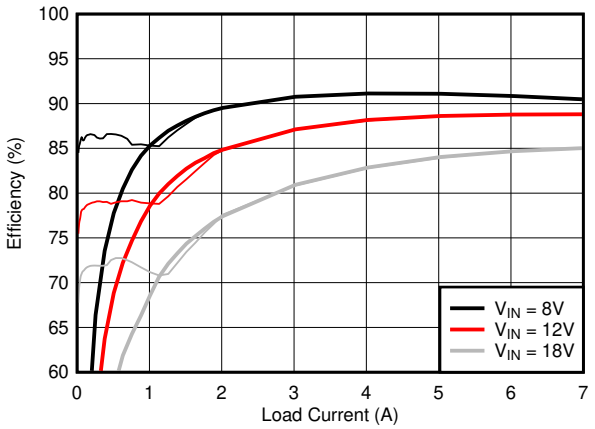
7.7 Typical Characteristics

V_{IN} = V_{EN1} = V_{EN2} = 12 V, T_J = 25°C, unless otherwise stated.



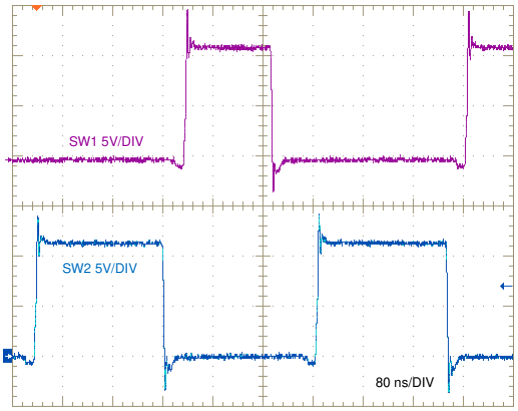
See 図 9-4 V_{OUT} = 5 V F_{SW} = 2.1 MHz

図 7-1. Efficiency versus Load



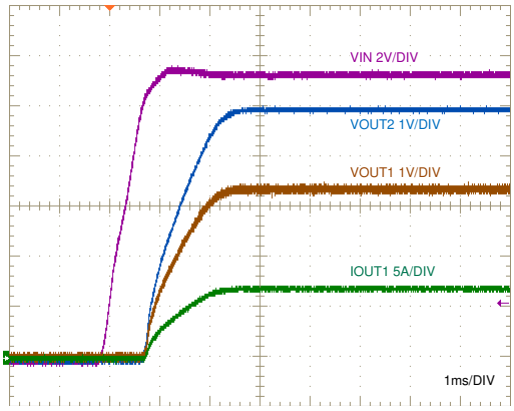
See 図 9-4 V_{OUT} = 3.3 V F_{SW} = 2.1 MHz

図 7-2. Efficiency versus Load



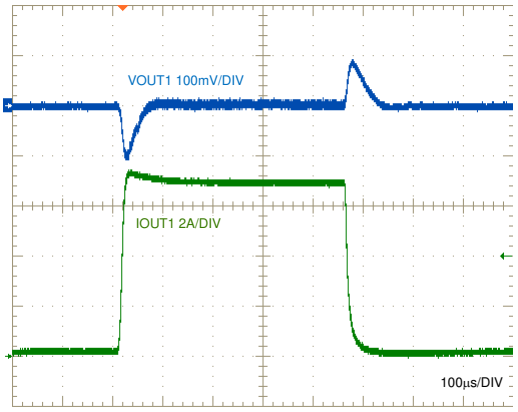
See 図 9-4

図 7-3. Switch Node Voltages



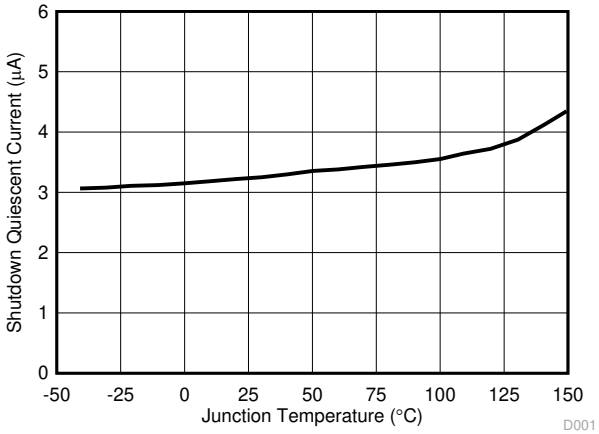
See 図 9-4

図 7-4. Start-up Characteristic



See 図 9-4

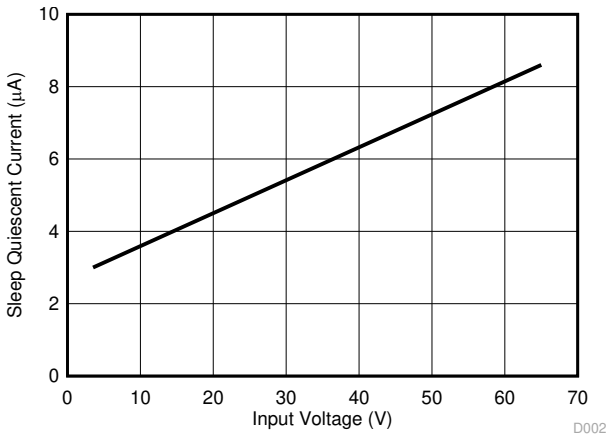
図 7-5. Load Transient Response



V_{EN1} = V_{EN2} = 0 V

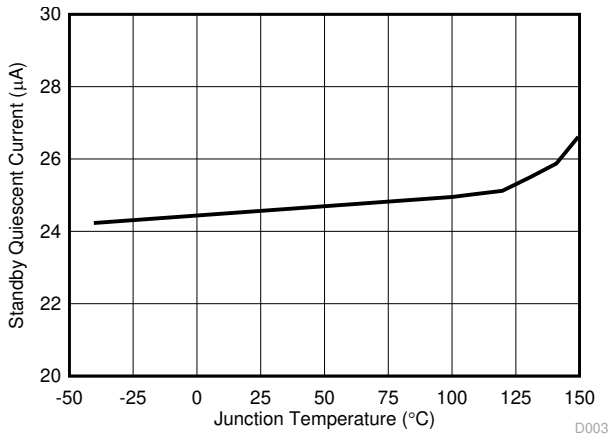
図 7-6. Shutdown Current versus Temperature

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$V_{EN1} = V_{EN2} = 0$ V

図 7-7. Shutdown Current versus Input Voltage



$V_{EN2} = 0$ V

図 7-8. Channel 1 Standby Current versus Temperature

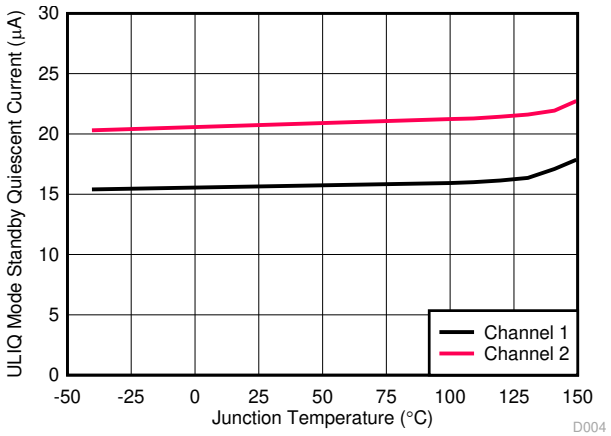


図 7-9. ULIQ Mode Standby Current versus Temperature

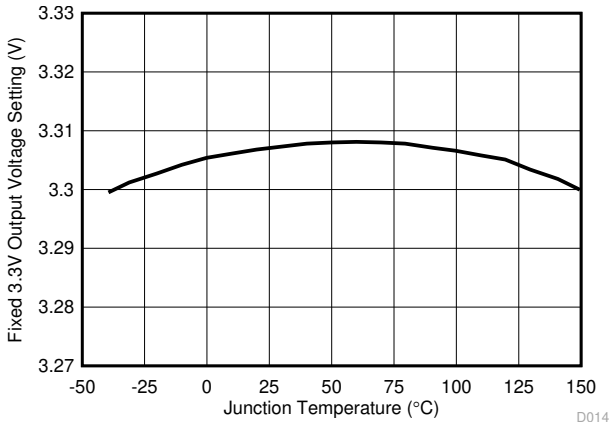


図 7-10. Fixed 3.3-V Output Voltage (VOUT1) versus Temperature

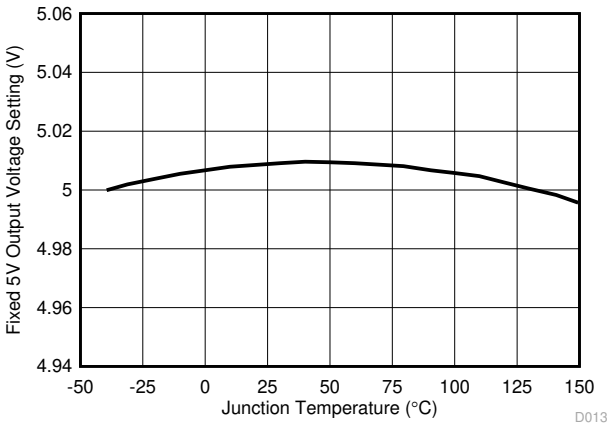


図 7-11. Fixed 5-V Output Voltage (VOUT1) versus Temperature

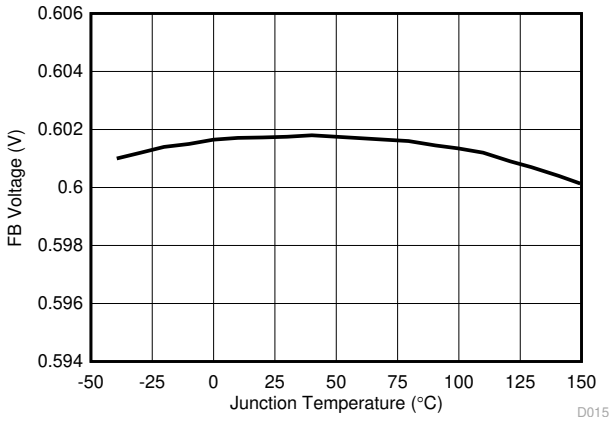


図 7-12. Feedback Voltage versus Temperature

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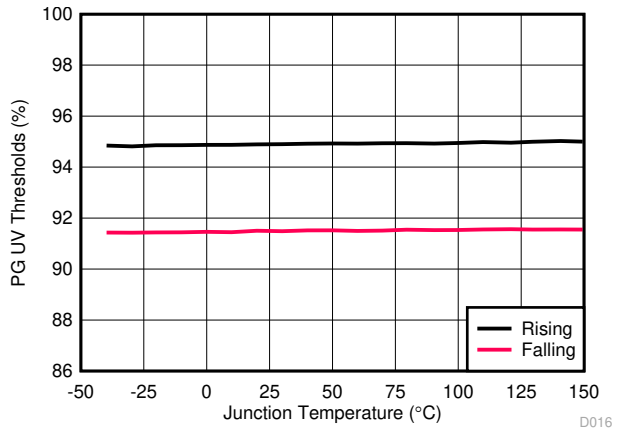


図 7-13. PG UV Thresholds versus Temperature

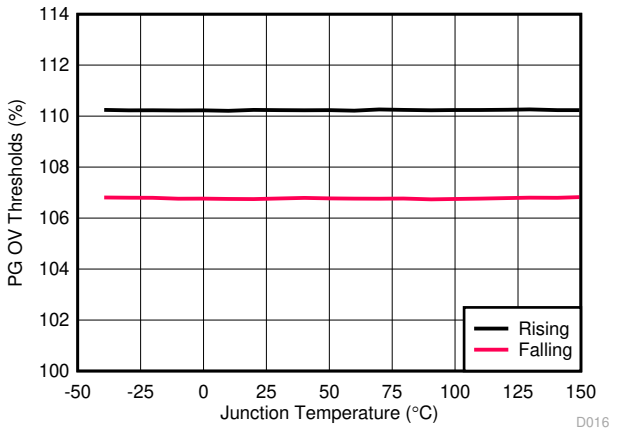


図 7-14. PG OV Thresholds versus Temperature

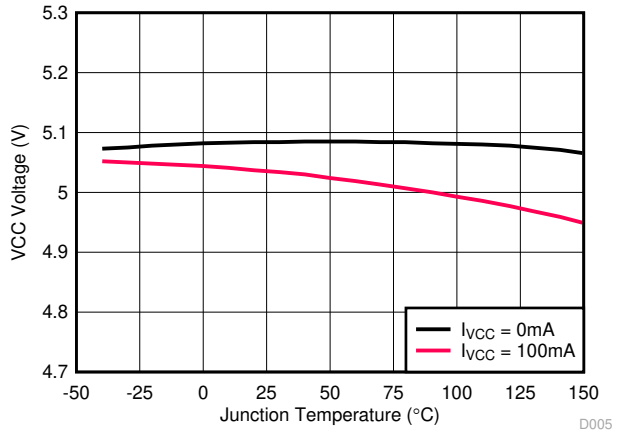


図 7-15. VCC Regulation Voltage versus Temperature

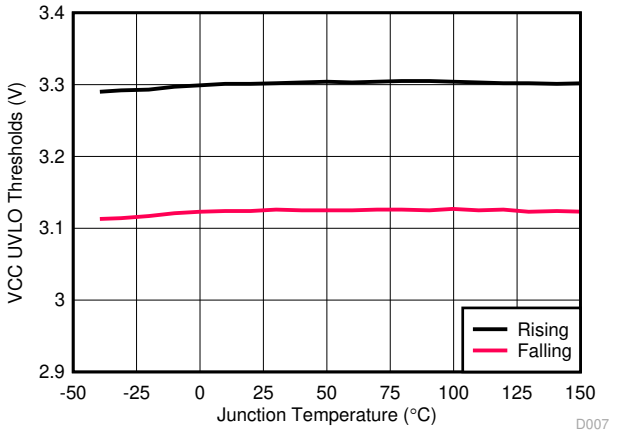


図 7-16. VCC UVLO Thresholds versus Temperature

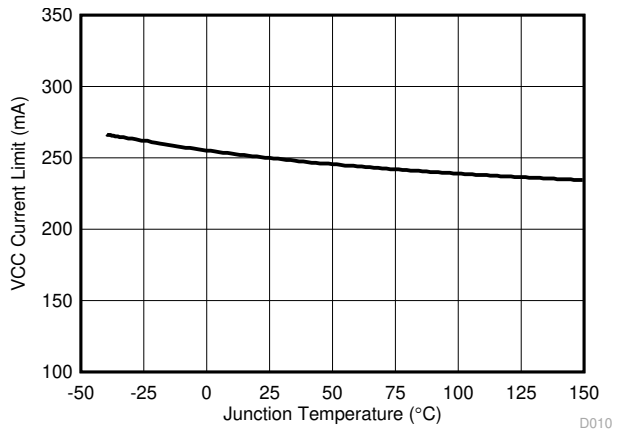


図 7-17. VCC Current Limit versus Temperature

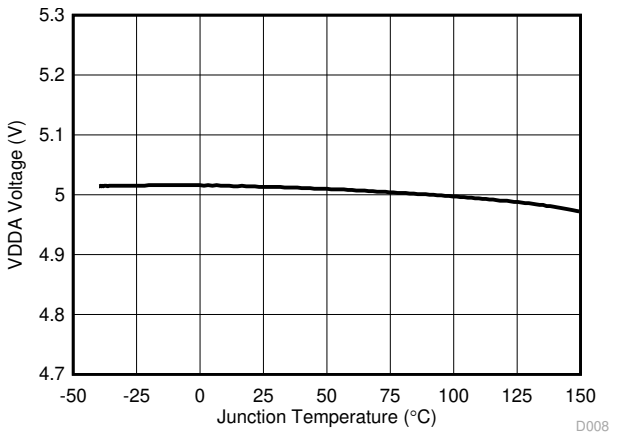


図 7-18. VDDA Regulation Voltage versus Temperature

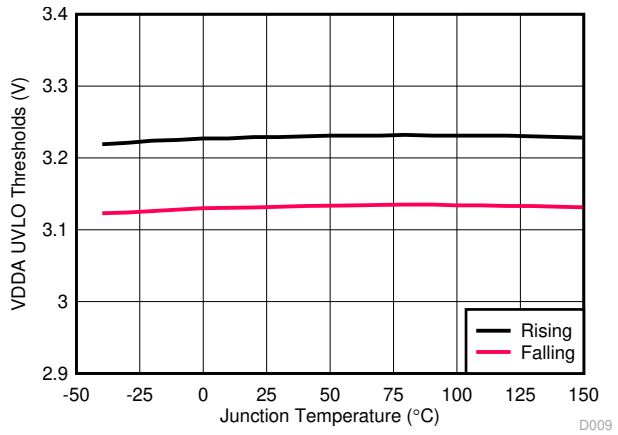


図 7-19. VDDA UVLO Thresholds versus Temperature

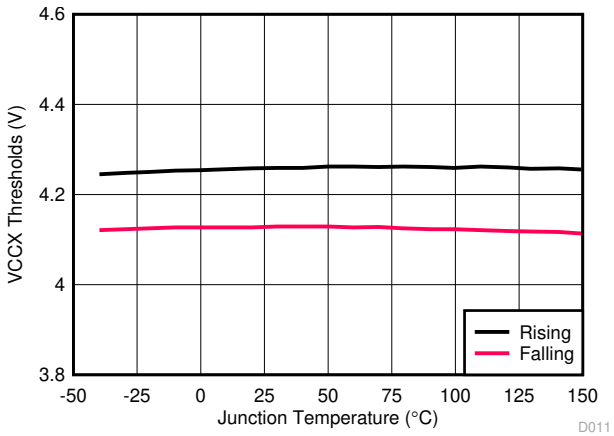


図 7-20. VCCX On/Off Thresholds versus Temperature

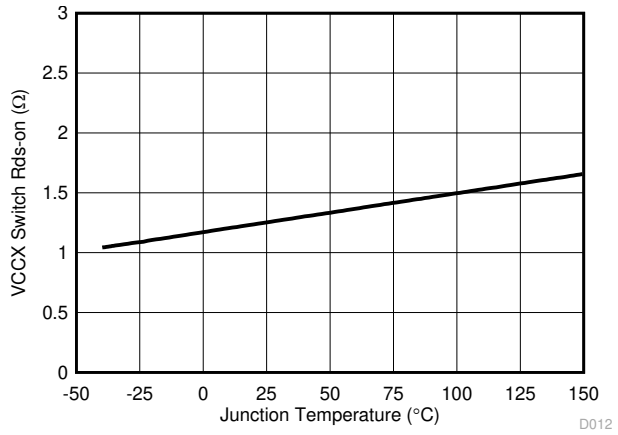


図 7-21. VCCX Switch Resistance versus Temperature

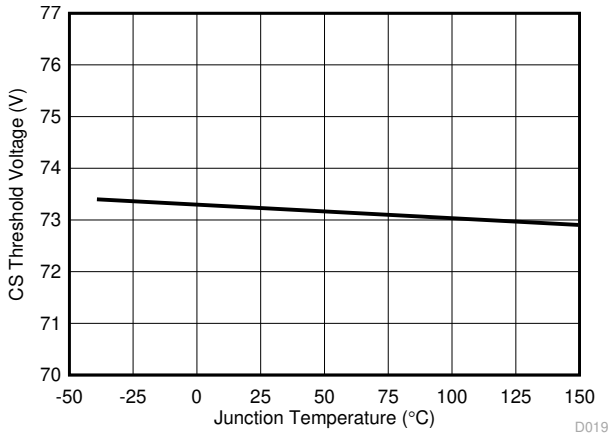


図 7-22. Current Sense (CS1) Threshold versus Temperature

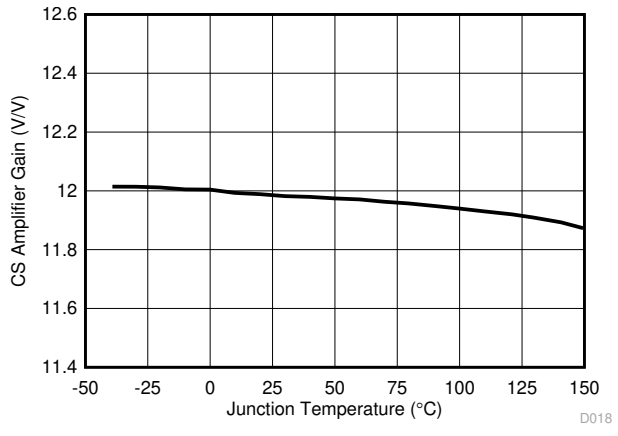


図 7-23. Current Sense (CS1) Amplifier Gain versus Temperature

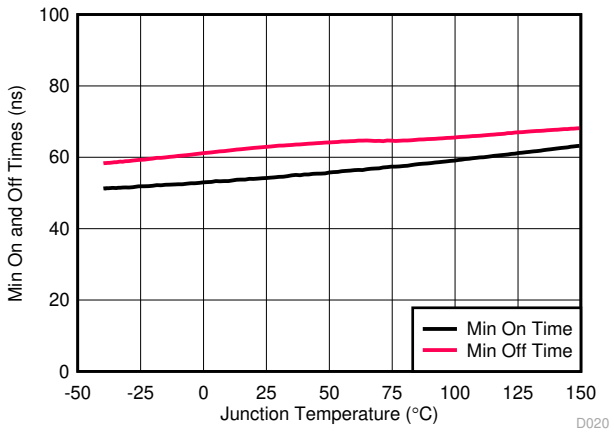


図 7-24. Minimum On Time and Off Time (HO1) versus Temperature

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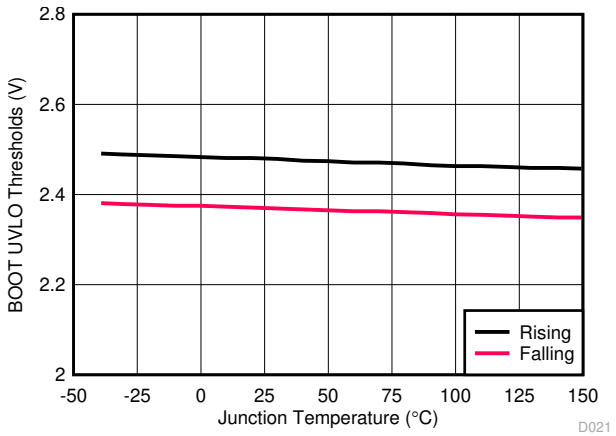


図 7-25. BOOT (HB1) UVLO Thresholds versus Temperature

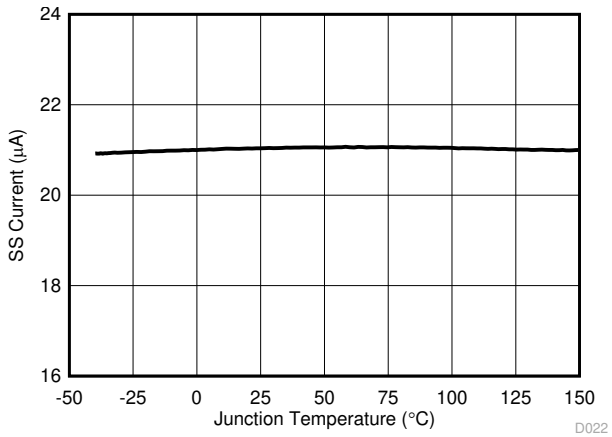


図 7-26. Soft-start (SS1) Current versus Temperature

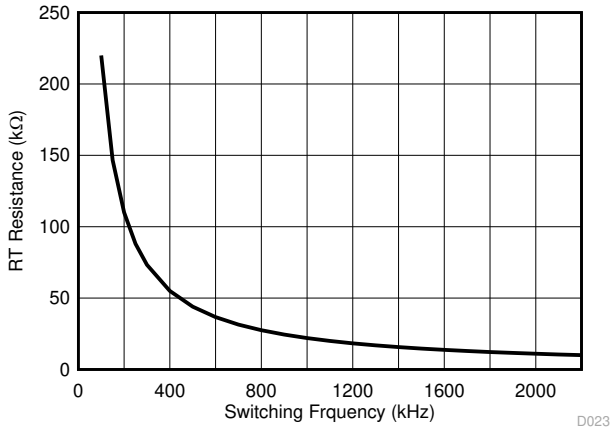


図 7-27. RT Resistance versus Switching Frequency

8 Detailed Description

8.1 Overview

The LM5143-Q1 is a dual-phase or dual-channel switching controller that features all of the functions necessary to implement a high-efficiency synchronous buck power supply operating over a wide input voltage range from 3.5 V to 65 V. The LM5143-Q1 is configured to provide a fixed 3.3-V or 5-V output, or an adjustable output between 0.6 V to 55 V. This easy-to-use controller integrates high-side and low-side MOSFET drivers capable of sourcing 3.25-A and sinking 4.25-A peak current. Adaptive dead-time control is designed to minimize body diode conduction during switching transitions.

Current-mode control using a shunt resistor or inductor DCR current sensing provides inherent line feedforward, cycle-by-cycle peak current limiting, and easy loop compensation. It also supports a wide duty cycle range for high input voltage and low dropout applications as well as when a high voltage conversion ratio (for example, 10-to-1) is required. The oscillator frequency is user-programmable between 100 kHz to 2.2 MHz, and the frequency can be synchronized as high as 2.5 MHz by applying an external clock to DEMB.

An external bias supply can be connected to VCCX to maximize efficiency in high input voltage applications. A user-selectable diode emulation feature enables discontinuous conduction mode (DCM) operation to further improve efficiency and reduce power dissipation during light-load conditions. Fault protection features include the following:

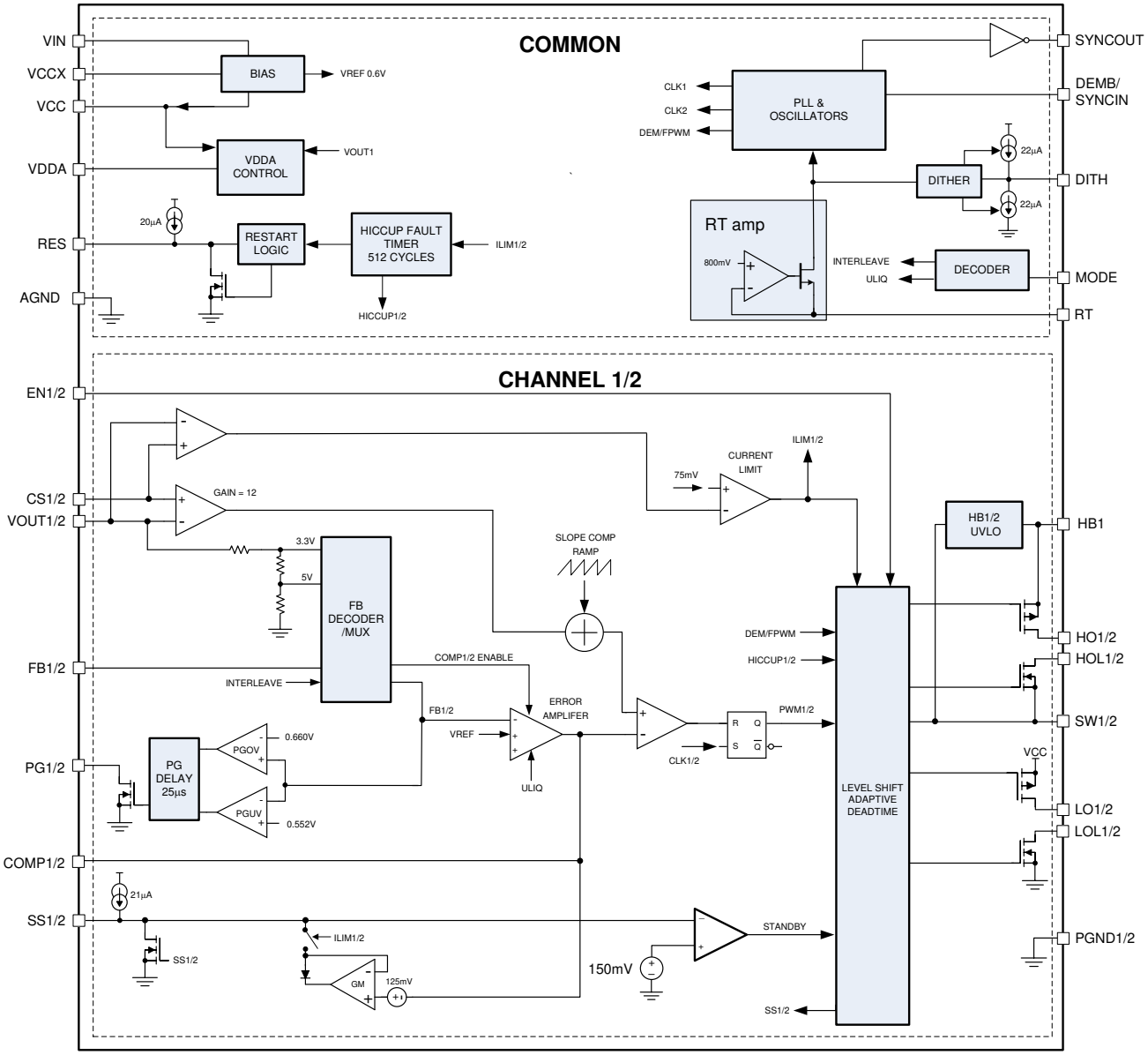
- Current limiting
- Thermal shutdown
- UVLO
- Remote shutdown capability

The LM5143-Q1 incorporates features to simplify the compliance with CISPR 25 automotive EMI requirements. An optional spread spectrum frequency modulation (SSFM) technique reduces the peak EMI signature, while the adaptive gate drivers with slew rate control minimize high-frequency emissions. Finally, 180° out-of-phase interleaved operation of the two controller channels reduces input filtering and capacitor requirements.

The LM5143-Q1 is provided in a 40-pin VQFNP package with wettable flanks and an exposed pad to aid in thermal dissipation.

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8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Input Voltage Range (V_{IN})

The LM5143-Q1 operational input voltage range is from 3.5 V to 65 V. The device is intended for step-down conversions from 12-V, 24-V, and 48-V automotive supply rails. The application circuit in 図 8-1 shows all the necessary components to implement an LM5143-Q1 based wide-V_{IN} dual-output step-down regulator using a single supply. The LM5143-Q1 uses an internal LDO subregulator to provide a 5-V VCC bias rail for the gate drive and control circuits (assuming the input voltage is higher than 5 V plus the necessary subregulator dropout specification).

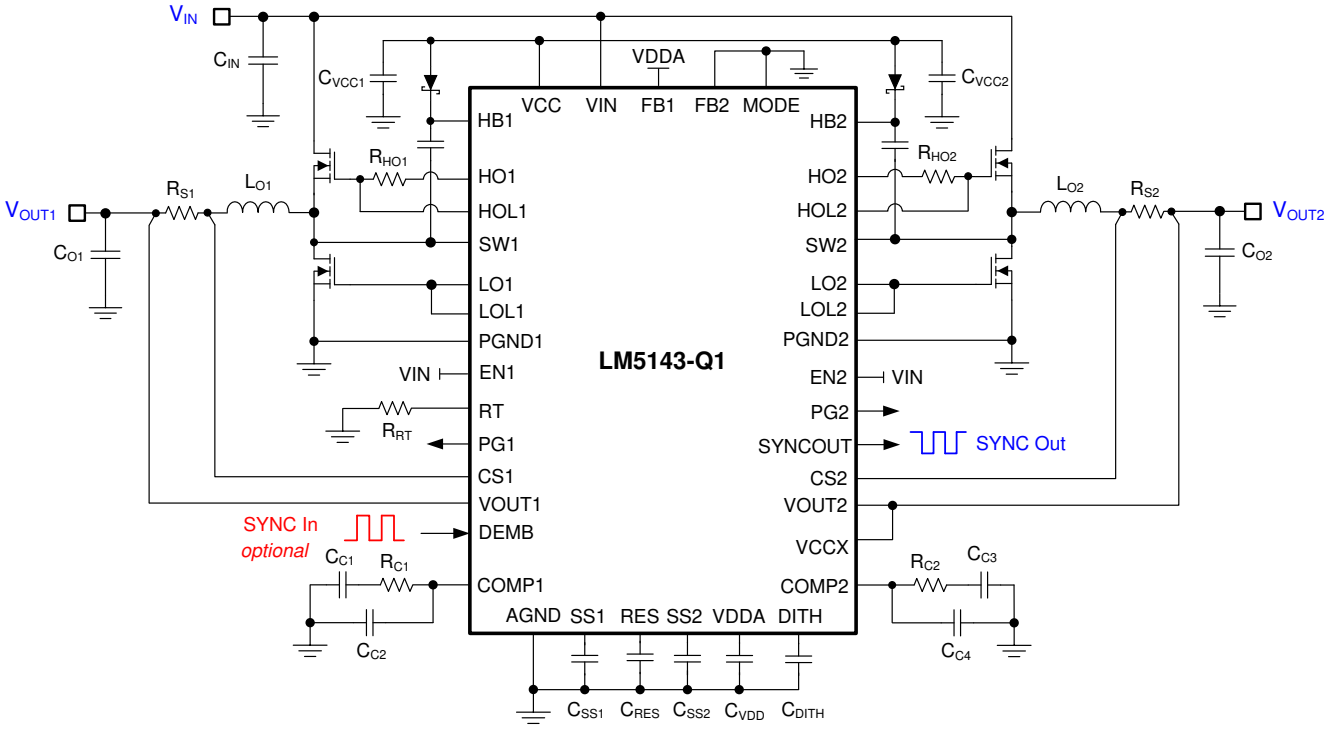


図 8-1. Dual-Output Regulator Schematic Diagram With Input Voltage Range of 3.5 V to 65 V

In high input voltage applications, make sure the VIN and SW pins do not exceed their absolute maximum voltage rating of 70 V during line or load transient events. Voltage excursions that exceed the *Absolute Maximum Ratings* can damage the IC. Proceed carefully during PCB board layout and use high-quality input bypass capacitors to minimize voltage overshoot and ringing.

8.3.2 High-Voltage Bias Supply Regulator (VCC, VCCX, VDDA)

The LM5143-Q1 contains an internal high-voltage VCC bias regulator that provides the bias supply for the PWM controller and the gate drivers for the external MOSFETs. The input voltage pin (VIN) can be connected directly to an input voltage source up to 65 V. However, when the input voltage is below the VCC setpoint level, the VCC voltage tracks VIN minus a small voltage drop.

The VCC regulator output current limit is 170 mA (minimum). At power up, the regulator sources current into the capacitors connected at the VCC pin. When the VCC voltage exceeds 3.3 V, both output channels are enabled (if EN1 and EN2 are connected to a voltage greater than 2 V) and the soft-start sequence begins. Both channels remain active unless the VCC voltage falls below the VCC falling UVLO threshold of 3.1 V (typical) or EN1/2 is switched to a low state. The LM5143-Q1 has two VCC pins that must be connected together on the PCB. TI recommends that two VCC capacitors are connected from VCC to PGND1 and from VCC to PGND2. The recommended range for each VCC capacitor is from 2.2 µF to 10 µF.

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An internal 5-V linear regulator generates the VDDA bias supply. Bypass VDDA with a 470-nF ceramic capacitor to achieve a low-noise internal bias rail. Normally VDDA is 5 V, but there are two operating conditions where it regulates at 3.3 V. The first is in skip cycle mode when V_{OUT1} is set to 3.3 V and V_{OUT2} is disabled. The second is in a cold-crank start-up where V_{IN} is 3.8 V and V_{OUT1} is 3.3 V.

Internal power dissipation of the VCC regulator can be minimized by connecting VCCX to a 5-V output at VOUT1 or VOUT2 or to an external 5-V supply. If the VCCX voltage is above 4.3 V, VCCX is internally connected to VCC and the internal VCC regulator is disabled. Tie VCCX to AGND if it is unused. Never connect VCCX to a voltage greater than 6.5 V or less than –0.3 V. If an external supply is connected to VCCX to power the LM5143-Q1, V_{IN} must be greater than the external bias voltage during all conditions to avoid damage to the controller.

8.3.3 Enable (EN1, EN2)

The LM5143-Q1 contains two enable inputs. EN1 and EN2 facilitate independent start-up and shutdown control of V_{OUT1} and V_{OUT2}. The enable pins can be connected to a voltage as high as 70 V. If an enable input is greater than 2 V, its respective output is enabled. If an enable pin is pulled below 0.4 V, the output is shutdown. If both outputs are disabled, the LM5143-Q1 is in a low-I_Q shutdown mode with a 4-µA typical current drawn from VIN. TI does not recommend leaving EN1 or EN2 floating.

8.3.4 Power Good Monitor (PG1, PG2)

The LM5143-Q1 includes output voltage monitoring signals for V_{OUT1} and V_{OUT2} to simplify sequencing and supervision. The power-good function can be used to enable circuits that are supplied by the corresponding voltage rail or to turn on sequenced supplies. Each power-good output (PG1 and PG2) switches to a high impedance open-drain state when the corresponding output voltage is in regulation. Each output switches low when the corresponding output voltage drops below the lower power-good threshold (92% typical) or rises above the upper power-good threshold (110% typical). A 25-µs deglitch filter prevents false tripping of the power-good signals during transients. TI recommends pullup resistors of 100 kΩ (typical) from PG1 and PG2 to the relevant logic rail. PG1 and PG2 are asserted low during soft start and when the corresponding buck regulator is disabled by EN1 or EN2.

8.3.5 Switching Frequency (RT)

The LM5143-Q1 oscillator is programmed by a resistor between RT and AGND to set an oscillator frequency between 100 kHz to 2.2 MHz. CLK1 is the clock for channel 1 and CLK2 is for channel 2. CLK1 and CLK2 are 180° out of phase. Use 式 1 to calculate the RT resistance for a given switching frequency.

$$R_{RT}\left[k\Omega\right] = \frac{22}{F_{SW}\left[MHz\right]} \tag{1}$$

Under low V_{IN} conditions when either of the on-time of the high-side MOSFETs exceeds the programmed oscillator period, the LM5143-Q1 extends the switching period of that channel until the PWM latch is reset by the current sense ramp exceeding the controller compensation voltage. In such an event, the oscillators (CLK1 and CLK2) operate independently and asynchronously until both channels can maintain output regulation at the programmed frequency.

The approximate input voltage level where this occurs is given by 式 2.

$$V_{IN(min)} = V_{OUT} \cdot \frac{t_{SW}}{t_{SW} - t_{OFF(min)}} \tag{2}$$

where

- where t_{SW} is the switching period
- $t_{OFF(min)}$ is the minimum off-time of 60 ns

8.3.6 Clock Synchronization (DEMB)

To synchronize the LM5143-Q1 to an external source, apply a logic-level clock signal (greater than 2 V) to DEMB. The LM5143-Q1 can be synchronized to ±20% of the programmed frequency up to a maximum of 2.5 MHz. If there is an RT resistor and a synchronization signal, the LM5143-Q1 ignores the RT resistor and synchronizes to the external clock. Under low V_{IN} conditions when the minimum off-time is reached, the synchronization signal is ignored, allowing the switching frequency to reduce to maintain output voltage regulation.

8.3.7 Synchronization Out (SYNCOUT)

The SYNCOUT voltage is a logic level signal with a rising edge approximately 90° lagging HO2 (or 90° leading HO1). When the SYNCOUT signal is used to synchronize a second LM5143-Q1 controller, all four phases are 90° out of phase.

8.3.8 Spread Spectrum Frequency Modulation (DITH)

The LM5143-Q1 provides a frequency dithering option that is enabled by connecting a capacitor from DITH to AGND. This generates a triangular voltage centered at 1.2 V at DITH. See 図 8-2. The triangular waveform modulates the oscillator frequency by ±5% of the nominal frequency set by the RT resistance. Use 式 3 to calculate the required DITH capacitance to set the modulating frequency, F_{MOD}. For the dithering circuit to effectively attenuate the peak EMI, the modulation rate must be less than 20 kHz for proper operation of the clock circuit.

$$C_{DITH} = \frac{22\mu A}{2 \cdot F_{MOD} \cdot 0.1V} \tag{3}$$

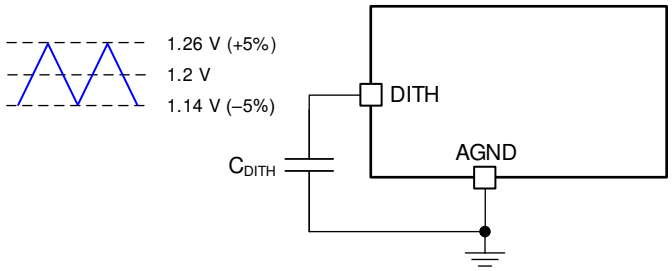


図 8-2. Switching Frequency Dithering

If DITH is connected to VDDA during power up, the dither feature is disabled and cannot be enabled unless VCC is recycled below the VCC UVLO threshold. If DITH is connected to AGND on power up, C_{DITH} is prevented from charging, disabling dither. Also, dither is disabled when the LM5143-Q1 is synchronized to an external clock.

8.3.9 Configurable Soft Start (SS1, SS2)

The soft-start feature allows the regulator to gradually reach the steady-state operating point, thus reducing start-up stresses and surges.

The LM5143-Q1 features an adjustable soft start that determines the charging time of the output or outputs. Soft start limits inrush current as a result of high output capacitance to avoid an overcurrent condition. Stress on the input supply rail is also reduced.

The LM5143-Q1 regulates the FB voltage to the SS voltage or the internal 600-mV reference, whichever is lower. At the beginning of the soft-start sequence when the SS voltage is 0 V, the internal 21-µA soft-start current source gradually increases the voltage on an external soft-start capacitor connected to the SS pin, resulting in a gradual rise of the relevant FB and output voltages. Use 式 4 to calculate the soft-start capacitance.

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$$C_{SS}(nF) = 35 \cdot t_{SS}(ms) \quad (4)$$

where

- t_{SS} is the required soft-start time

SS can be pulled low with an external circuit to stop switching, but this is not recommended. When the controller is in FPWM mode (set by connecting DEMB to VDDA), pulling SS low results in COMP being pulled down internally as well. LO remains on and the low-side MOSFET discharges the output capacitor, resulting in large negative inductor current. In contrast, the LO gate driver is disabled when the LM5143-Q1 internal logic pulls SS low due to a fault condition.

8.3.10 Output Voltage Setpoint (FB1, FB2)

The LM5143-Q1 outputs can be independently configured for one of the two fixed output voltages with no external feedback resistors, or adjusted to the desired voltage using an external resistor divider. V_{OUT1} or V_{OUT2} can be configured as a 3.3-V output by connecting the corresponding FB pin to VDDA, or a 5-V output by connecting FB to AGND. The FB1 and FB2 connections (either VDDA or GND) are detected during power up. The configuration settings are latched and cannot be changed until the LM5143-Q1 is powered down with the VCC voltage decreasing below its falling UVLO threshold, and then powered up again.

Alternatively, the output voltage can be set using external resistive dividers from the output to the relevant FB pin. The output voltage adjustment range is between 0.6 V and 55 V. The regulation threshold at FB is 0.6 V (V_{REF}). Use 式 5 to calculate the upper and lower feedback resistors, designated R_{FB1} and R_{FB2}, respectively. See 図 8-3.

$$R_{FB1} = \left(\frac{V_{OUT}}{V_{REF}} - 1 \right) \cdot R_{FB2} \quad (5)$$

The recommended starting value for R_{FB2} is between 10 kΩ and 20 kΩ.

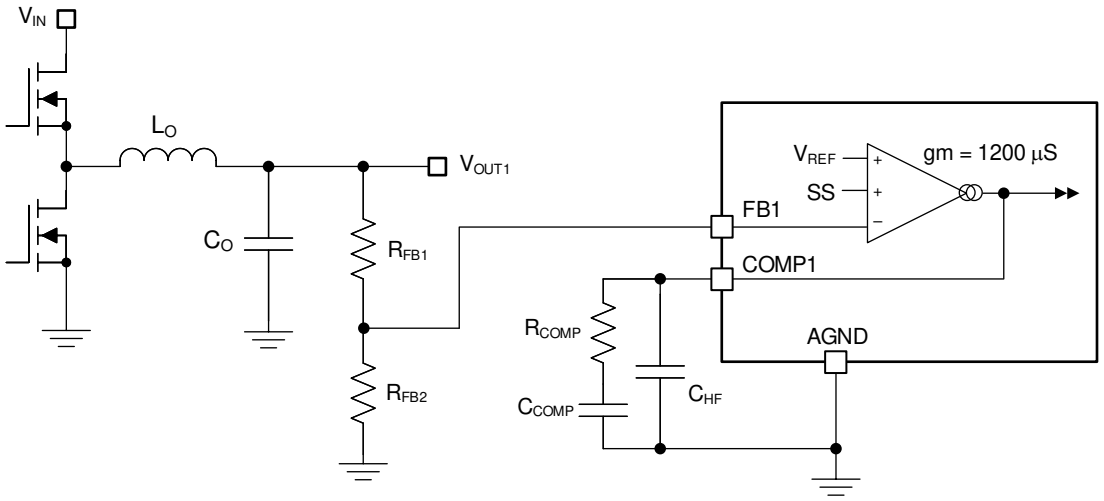


図 8-3. Control Loop Error Amplifier

The Thevenin equivalent impedance of the resistive divider connected to the FB pin must be greater than 5 kΩ for the LM5143-Q1 to detect the divider and set the channel to the adjustable output mode.

$$R_{TH} = \frac{R_{FB1} \cdot R_{FB2}}{R_{FB1} + R_{FB2}} > 5k\Omega \quad (6)$$

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If a low I_Q mode is required, take care when selecting the external resistors. The extra current drawn from the external divider is added to the LM5143-Q1 $I_{STANDBY}$ current (15 µA typical). The divider current reflected to V_{IN} is divided down by the ratio of V_{OUT}/V_{IN}. For example, if V_{OUT} is set to 5.55 V with R_{FB1} equal to 82.5 kΩ and R_{FB2} equal to 10 kΩ, use 式 7 to calculate the input current from a 12-V input required to supply the current in the feedback resistors.

$$I_{VIN(DIVIDER)} = \frac{V_{OUT}}{R_{FB1} + R_{FB2}} \cdot \frac{V_{OUT}}{\eta \cdot V_{IN}} = \frac{5.55\,V}{82.5k\Omega + 10k\Omega} \cdot \frac{5.55\,V}{80\% \cdot 12\,V} \approx 35\mu A$$

$$I_{VIN} = I_{STANDBY} + I_{VIN(DIVIDER)} = 15\mu A + 35\mu A = 50\mu A \quad (7)$$

If one output is enabled and the other disabled, the VCC output is in regulation. The HB voltage of the disabled channel charges to VCC through the bootstrap diode. As a result, the HO driver bias current (approximately 1.5 µA) can increase the output voltage of the disabled channel to approximately 2.2 V. If this is not desired, add a load resistor (100 kΩ) to the output that is disabled to maintain a low-voltage OFF-state.

8.3.11 Minimum Controllable On-Time

There are two limitations to the minimum output voltage adjustment range: the LM5143-Q1 voltage reference of 0.6 V and the minimum controllable switch-node pulse width, $t_{ON(min)}$.

$t_{ON(min)}$ effectively limits the voltage step-down conversion ratio of V_{OUT}/V_{IN} at a given switching frequency. For fixed-frequency PWM operation, the voltage conversion ratio must satisfy 式 8.

$$\frac{V_{OUT}}{V_{IN}} > t_{ON(min)} \cdot F_{SW} \quad (8)$$

where

- $t_{ON(min)}$ is 65 ns (typical)
- F_{SW} is the switching frequency

If the desired voltage conversion ratio does not meet the above condition, the LM5143-Q1 transitions from fixed switching frequency operation to a pulse-skipping mode to maintain output voltage regulation. For example, if the desired output voltage is 5 V with an input voltage is 24 V and switching frequency of 2.1 MHz, the voltage conversion ratio test in 式 9 is satisfied.

$$\frac{5\,V}{24\,V} > 65ns \cdot 2.1\,MHz$$

$$0.208 > 0.137 \quad (9)$$

For wide V_{IN} applications and low output voltages, an alternative is to reduce the LM5143-Q1 switching frequency to meet the requirement of 式 8.

8.3.12 Error Amplifier and PWM Comparator (FB1, FB2, COMP1, COMP2)

Each channel of the LM5143-Q1 has an independent high-gain transconductance amplifier that generates an error current proportional to the difference between the feedback voltage and an internal precision reference (0.6 V). The output of the transconductance amplifier is connected to the COMP pin, allowing the user to provide external control loop compensation. A type-II compensation network is generally recommended for peak current-mode control.

The amplifier has two gain settings, one is for normal operation with a g_m of 1200 µS and the other is for ultra-low I_Q with a g_m of 60 µS. For normal operation, connect MODE to AGND. For ultra-low operation, I_Q connect MODE to AGND through a 10-kΩ resistor.

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8.3.13 Slope Compensation

The LM5143-Q1 provides internal slope compensation for stable operation with peak current-mode control and a duty cycle greater than 50%. Use 式 10 to calculate the buck inductance to provide a slope compensation contribution equal to one times the inductor downslope.

$$L_{O\text{-}IDEAL}(\mu H) = \frac{V_{OUT}(V) \cdot R_S(m\Omega)}{24 \cdot F_{SW}(MHz)} \quad (10)$$

- A lower inductance value generally increases the peak-to-peak inductor current, which minimizes size and cost, and improves transient response at the cost of reduced light-load efficiency due to higher cores losses and peak currents.
- A higher inductance value generally decreases the peak-to-peak inductor current, which increases the full-load efficiency by reducing switch peak and RMS currents at the cost of requiring larger output capacitors to meet load-transient specifications.

8.3.14 Inductor Current Sense (CS1, VOUT1, CS2, VOUT2)

There are two methods to sense the inductor current of the buck power stage. The first uses a current sense resistor (also known as a shunt) in series with the inductor, and the second avails of the DC resistance of the inductor (DCR current sensing).

8.3.14.1 Shunt Current Sensing

図 8-4 illustrates inductor current sensing using a shunt resistor. This configuration continuously monitors the inductor current to provide accurate overcurrent protection across the operating temperature range. For optimal current sense accuracy and overcurrent protection, use a low inductance ±1% tolerance shunt resistor between the inductor and the output, with a Kelvin connection to the LM5143-Q1 current sense amplifier.

If the peak differential current signal sensed from CS to VOUT exceeds the current limit threshold of 73 mV, the current limit comparator immediately terminates the applicable HO output for cycle-by-cycle current limiting. Use 式 11 to calculate the shunt resistance.

$$R_S = \frac{V_{CS}}{I_{OUT(CL)} + \frac{\Delta I_L}{2}} \quad (11)$$

where

- V_{CS} is current sense threshold of 73 mV
- $I_{OUT(CL)}$ is the overcurrent setpoint that is set higher than the maximum load current to avoid tripping the overcurrent comparator during load transients
- ΔI_L is the peak-to-peak inductor ripple current

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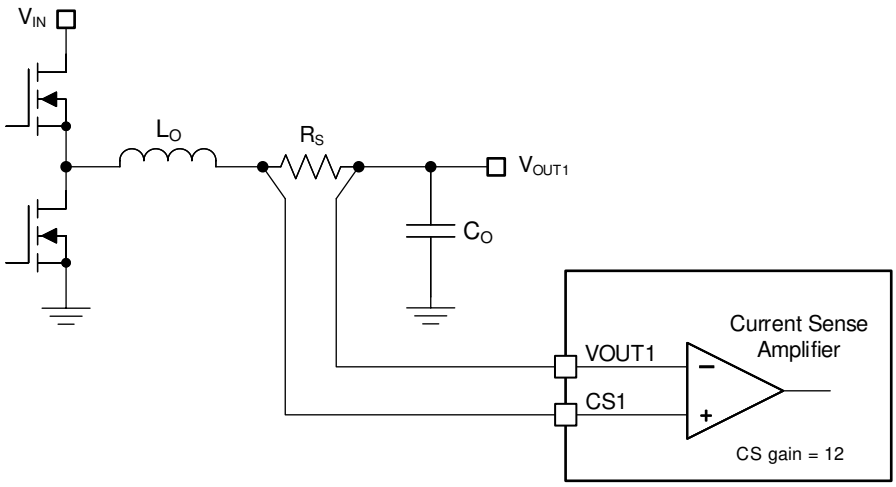


図 8-4. Shunt Current Sensing Implementation

The respective SS voltage is clamped 150 mV above FB during an overcurrent condition for each channel. Sixteen overcurrent events must occur before the SS clamp is enabled. This makes sure that SS can be pulled low during brief overcurrent events, preventing output voltage overshoot during recovery.

8.3.14.2 Inductor DCR Current Sensing

For high-power applications that do not require accurate current-limit protection, inductor DCR current sensing is preferable. This technique provides lossless and continuous monitoring of the inductor current using an RC sense network in parallel with the inductor. Select an inductor with a low DCR tolerance to achieve a typical current limit accuracy within the range of 10% to 15% at room temperature. Components R_{CS} and C_{CS} in 図 8-5 create a low-pass filter across the inductor to enable differential sensing of the voltage drop across the inductor DCR.

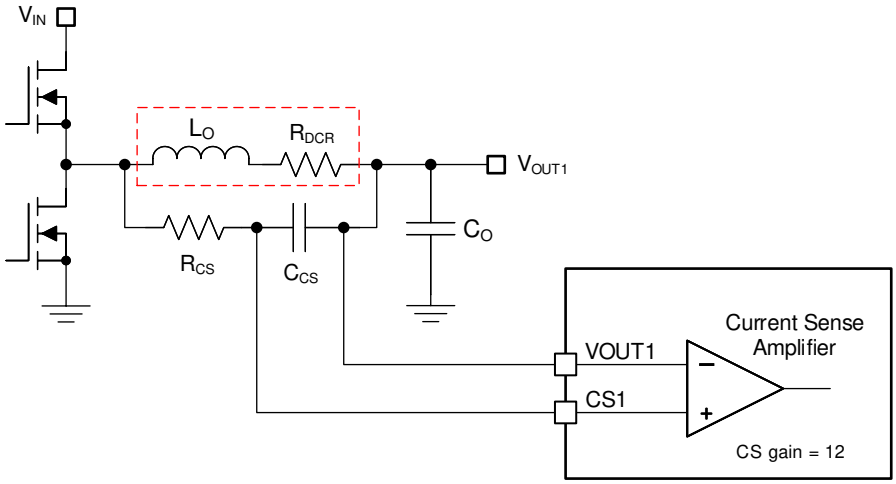


図 8-5. Inductor DCR Current Sensing Implementation

Use 式 12 to calculate the voltage drop across the sense capacitor in the s-domain. When the $R_{CS}C_{CS}$ time constant is equal to L_O/R_{DCR}, the voltage developed across the sense capacitor, C_{CS}, is a replica of the inductor DCR voltage and accurate current sensing is achieved. If the $R_{CS}C_{CS}$ time constant is not equal to the L_O/R_{DCR} time constant, there is a sensing error as follows:

- $R_{CS}C_{CS} > L_O/R_{DCR}$ → the DC level is correct, but the AC amplitude is attenuated.
- $R_{CS}C_{CS} < L_O/R_{DCR}$ → the DC level is correct, but the AC amplitude is amplified.

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$$V_{CS}(s) = \frac{1 + s \cdot \frac{L_O}{R_{DCR}}}{1 + s \cdot R_{CS} \cdot C_{CS}} \cdot R_{DCR} \cdot \left(I_{OUT(CL)} + \frac{\Delta I_L}{2} \right) \quad (12)$$

Choose the C_{CS} capacitance greater than or equal to 0.1 µF to maintain a low-impedance sensing network, thus reducing the susceptibility of noise pickup from the switch node. Carefully observe *セクション 11.1* to make sure that noise and DC errors do not corrupt the differential current sense signals applied between the CS and VOUT pins.

8.3.15 Hiccup Mode Current Limiting (RES)

The LM5143-Q1 includes an optional hiccup mode protection function that is enabled when a capacitor is connected to the RES pin. In normal operation, the RES capacitor is discharged to ground. If 512 cycles of cycle-by-cycle current limiting occurs, SS is pulled low and the HO and LO outputs are disabled (see 図 8-6). A 20-µA current source begins to charge the RES capacitor. When the RES voltage increases to 1.2 V, RES is pulled low and the SS capacitor begins to charge. The 512-cycle hiccup counter is reset if four consecutive switching cycles occur without exceeding the current limit threshold. Separate hiccup counters are provided for each channel, but the RES pin is shared by both channels. One channel can be in hiccup protection while the other operates normally. In the event that both channels are in an overcurrent condition triggering hiccup protection, the last hiccup counter to expire pulls RES low and starts the RES capacitor charging cycle. Both channels then restart together when V_{RES} = 1.2 V. If RES is connected to VDDA at power up, the hiccup function is disabled for both channels.

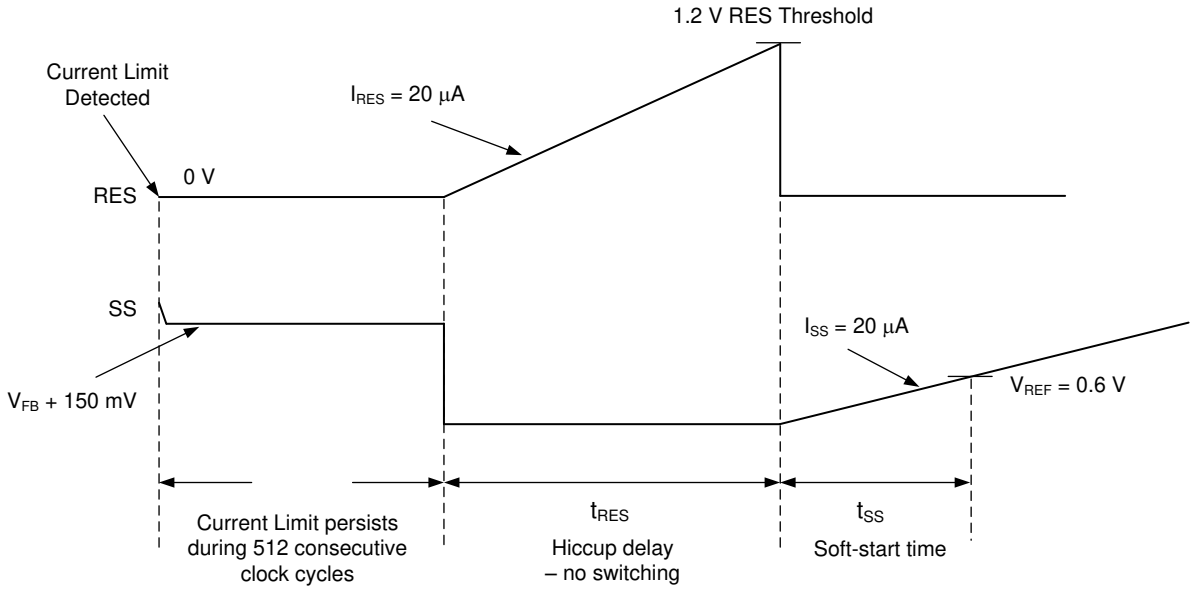


図 8-6. Hiccup Mode Timing Diagram

Use 式 13 to calculate the RES capacitance.

$$C_{RES}(nF) = 17 \cdot t_{RES}(ms) \quad (13)$$

where

- t_{RES} is the specified hiccup delay as shown in 図 8-6

8.3.16 High-Side and Low-Side Gate Drivers (HO1/2, LO1/2, HOL1/2, LOL1/2)

The LM5143-Q1 contains N-channel MOSFET gate drivers and an associated high-side level shifter to drive the external N-channel MOSFET. The high-side gate driver works in conjunction with an external bootstrap diode D_{BST} and bootstrap capacitor C_{BST}. See 図 8-7. During the conduction interval of the low-side MOSFET, the SW voltage is approximately 0 V and C_{BST} is charged from VCC through D_{BST}. TI recommends a 0.1-µF ceramic capacitor connected with short traces between the applicable HB and SW pins.

The LO and HO outputs are controlled with an adaptive dead-time methodology so that both outputs (HO and LO) are never enabled at the same time, preventing cross conduction. When the controller commands LO to be enabled, the adaptive dead-time logic first disables HO and waits for the HO-SW voltage to drop below 2.5 V typical. LO is then enabled after a small delay (HO fall to LO rising delay). Similarly, the HO turnon is delayed until the LO voltage has dropped below 2.5 V. HO is then enabled after a small delay (LO falling to HO rising delay). This technique ensures adequate dead time for any size N-channel MOSFET component or parallel MOSFET configurations.

Caution is advised when adding series gate resistors, as this can decrease the effective dead time. Each of the high-side and low-side drivers has an independent driver source and sink output pins. This allows the user to adjust drive strength to optimize the switching losses for maximum efficiency and control the slew rate for reduced EMI signature. The selected N-channel high-side MOSFET determines the appropriate bootstrap capacitance values C_{BST} in 図 8-7 according to 式 14.

$$C_{BST} = \frac{Q_G}{\Delta V_{BST}} \tag{14}$$

where

- Q_G is the total gate charge of the high-side MOSFET at the applicable gate drive voltage
- ΔV_{BST} is the voltage variation of the high-side MOSFET driver after turnon

To determine C_{BST}, choose ΔV_{BST} so that the available gate drive voltage is not significantly impacted. An acceptable range of ΔV_{BST} is 100 mV to 300 mV. The bootstrap capacitor must be a low-ESR ceramic capacitor, typically 0.1 µF. Use high-side and low-side MOSFETs with logic level gate threshold voltages.

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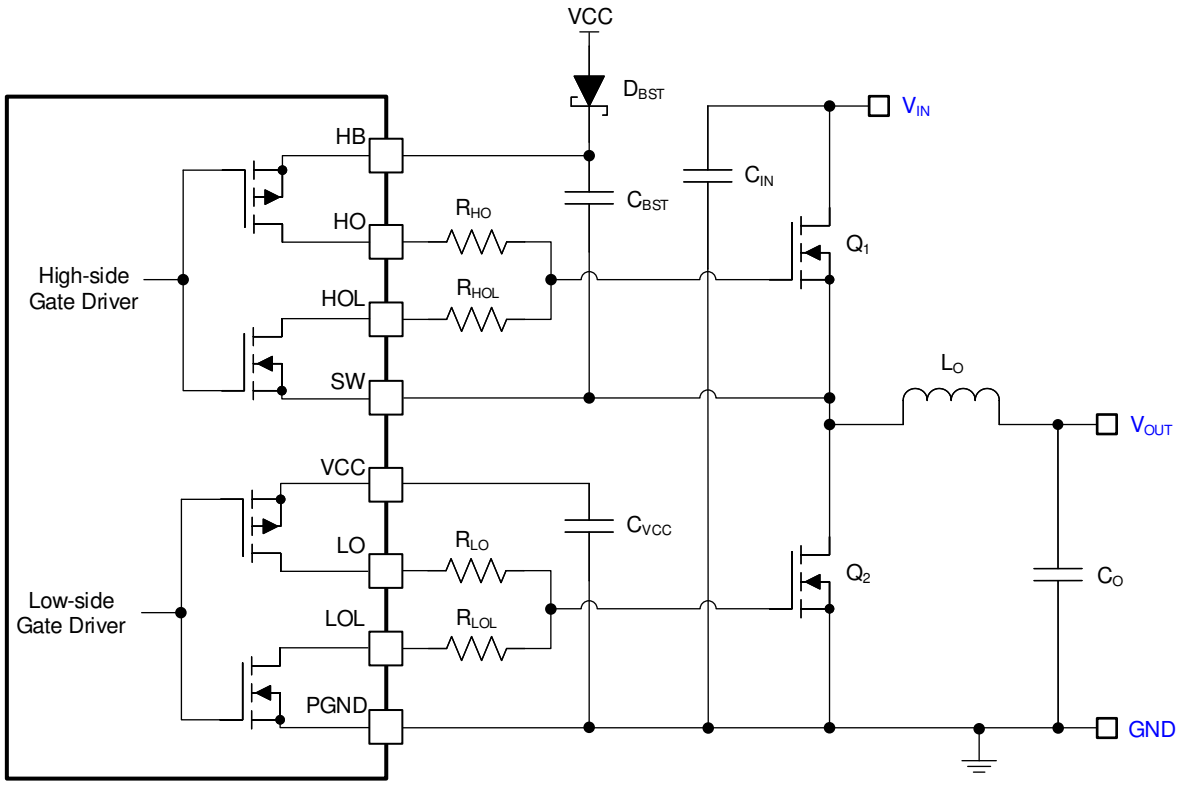


図 8-7. Integrated MOSFET Gate Drivers

8.3.17 Output Configurations (MODE, FB2)

8.3.17.1 Independent Dual-Output Operation

The LM5143-Q1 has two outputs that can operate independently. Both V_{OUT1} and V_{OUT2} can be set at 3.3 V or 5 V without installing external feedback resistors. Alternatively, set the output voltages between 0.6 V to 55 V using external feedback resistors based on 式 5. See 表 8-1 and 図 8-8. Connect MODE directly to AGND for independent outputs.

表 8-1. Output Voltage Settings

MODE	FB1	FB2	VOUT1	VOUT2	ERROR AMPLIFIER gm
AGND	AGND	AGND	5 V	5 V	1200 µS
AGND	VDDA	VDDA	3.3 V	3.3 V	1200 µS
AGND	VDDA	AGND	3.3 V	5 V	1200 µS
AGND	AGND	VDDA	5 V	3.3 V	1200 µS
AGND	Rdivider	Rdivider	0.6 V to 55 V	0.6 V to 55 V	1200 µS
10 kΩ to AGND	AGND	AGND	5 V	5 V	60 µS
10 kΩ to AGND	VDDA	VDDA	3.3 V	3.3 V	60 µS
10 kΩ to AGND	VDDA	AGND	3.3 V	5 V	60 µS
10 kΩ to AGND	AGND	VDDA	5 V	3.3 V	60 µS
10 kΩ to AGND	Rdivider	Rdivider	0.6 V to 55 V	0.6 V to 55 V	60 µS

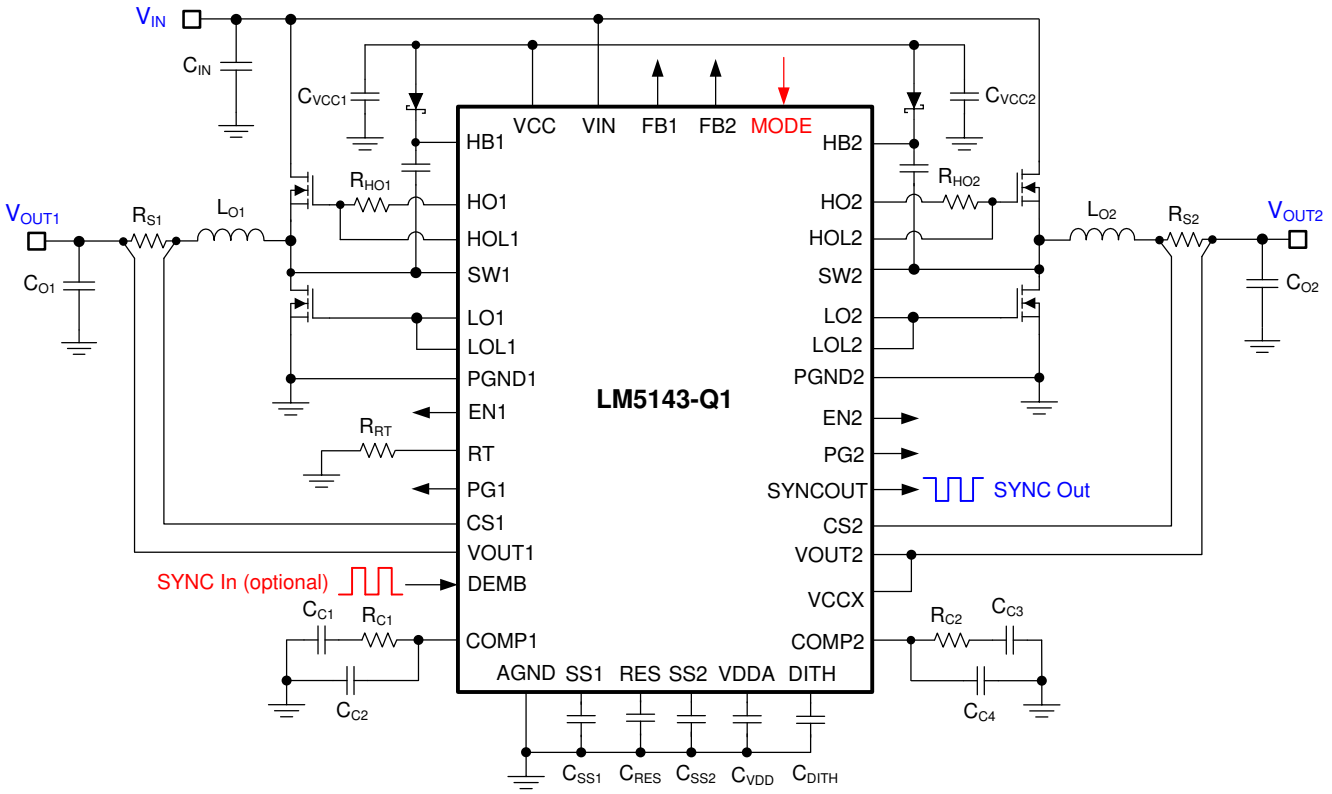


図 8-8. Regulator Schematic Configured for Independent Dual Outputs

8.3.17.2 Single-Output Interleaved Operation

Connect the MODE to VDDA and FB2 to AGND to configure the LM5143-Q1 for interleaved operation. This disables the channel 2 error amplifier and places it in a high impedance state. The controller is then in a master

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and slave configuration. Connect COMP1 to COMP2 and SS1 to SS2. Connect FB1 to VDDA for a 3.3-V output and to AGND for a 5-V output. Connect FB1 to an external feedback divider for an output voltage between 0.6 V to 55 V. See 表 8-2 and 図 8-9.

The LM5143-Q1 in single-output interleaved operation does not support phase shedding when the output voltage is set between 0.6 V to 1.5 V.

表 8-2. Single-Output Interleaved Operation

MODE	FB1	FB2	OUTPUT SETPOINT
VDDA	AGND	AGND	5 V
VDDA	VDDA	AGND	3.3 V
VDDA	Rdivider	AGND	0.6 V to 55 V

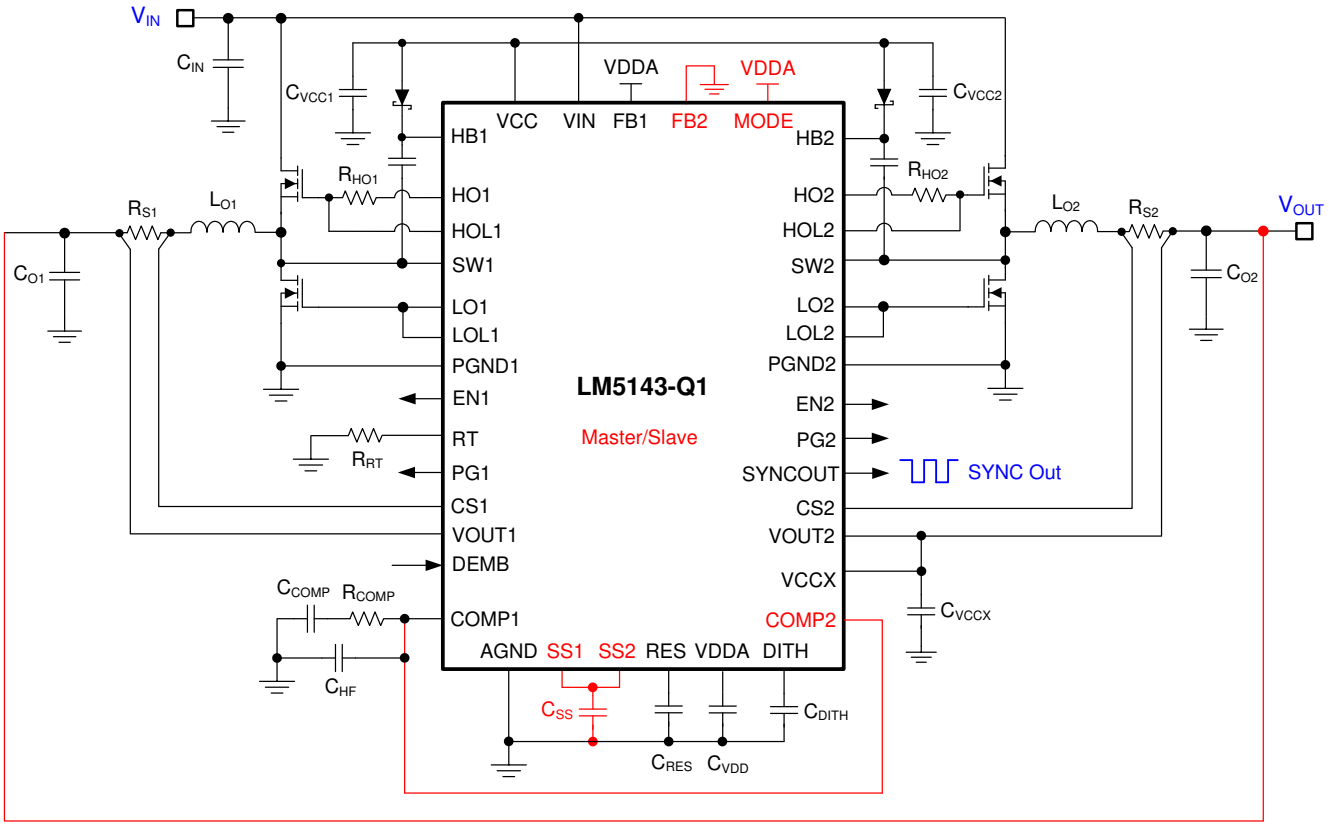


図 8-9. Two-Phase Regulator Schematic Configured for Single-Output Interleaved Operation

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8.3.17.3 Single-Output Multiphase Operation

To configure the LM5143-Q1 for multiphase operation (three or four phases), two LM5143-Q1 controllers are required. See 図 8-10. Configure the first controller (CNTRL1) as a master and the second controller (CNTRL2) as a slave. To configure the second controller as a slave, connect the MODE and FB2 pins to VDDA. This disables both feedback error amplifiers of the slave controller, placing them in a high-impedance state. Connect COMP1 and COMP2 of the master and slave together. Connect SS1 and SS2 of the master and slave together. Connect SYNCOUT of the master to DEMB (SYNCIN) of the slave. The SYNCOUT of the master controller is 90° out-of-phase and facilitates interleaved operation. RT is not used for the oscillator when the LM5143-Q1 is in slave mode but instead used for slope compensation. Therefore, select the RT resistance to be the same as that of the master. The oscillator is derived from the master controller. FPWM or DEM mode for the slave is set by connecting its FB1 to VDDA or GND. FPWM or DEM mode of the master controller is set by its DEMB pin. See 表 8-3.

The LM5143-Q1 in single-output multiphase operation does not support phase shedding when the output voltage is set between 0.6 V to 1.5 V.

See the *Benefits of a Multiphase Buck Converter White Paper* and *Multiphase Buck Design From Start to Finish Application Report* for more information.

表 8-3. Single-Output Multiphase Operation

MODE	FB1 (SLAVE)	FB2 (SLAVE)	DEM or FPWM (SLAVE)
VDDA	GND	VDDA	DEM
VDDA	VDDA	VDDA	FPWM

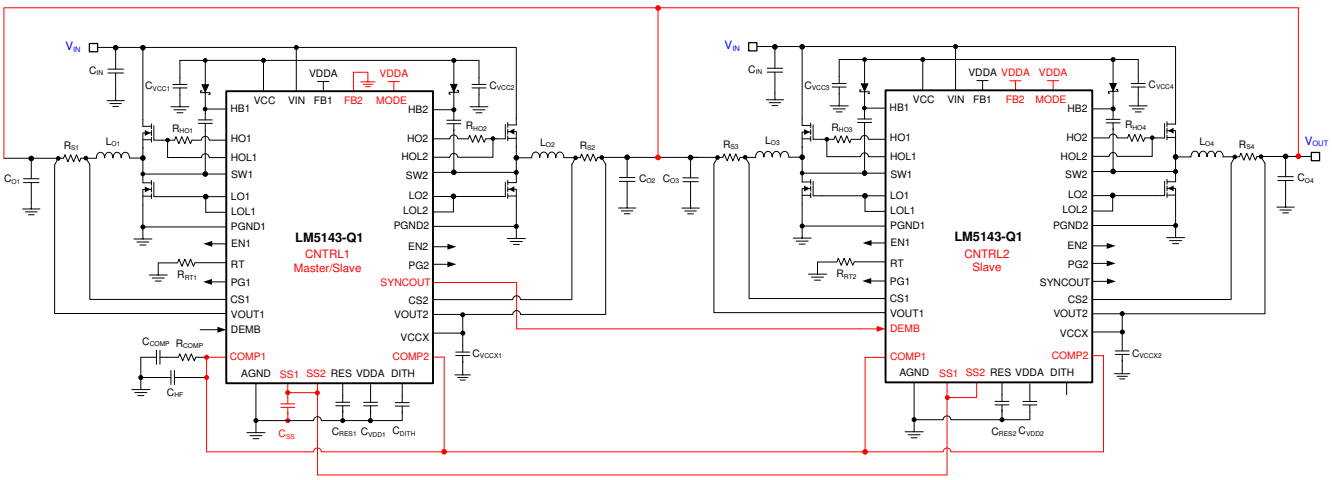


図 8-10. Multiphase Regulator Schematic Configured for Single-Output Interleaved Operation

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8.4 Device Functional Modes

8.4.1 Standby Modes

The LM5143-Q1 operates with peak current-mode control such that the compensation voltage is proportional to the peak inductor current. During no-load or light-load conditions, the output capacitor discharges very slowly. As a result, the compensation voltage does not demand driver output pulses on a cycle-by-cycle basis. When the LM5143-Q1 controller detects 16 missed switching cycles, it enters standby mode and switches to a low I_Q state to reduce the current drawn from the input. For the LM5143-Q1 to go into standby mode, the controller must be programmed for diode emulation (V_{DEMB} < 0.4 V).

There are two standby modes: ultra-low I_Q and normal mode. To enter ultra-low I_Q mode, connect MODE to AGND through a 10-kΩ resistor. In ultra-low I_Q mode, the transconductance amplifier gain is reduced from 1200 µS to 60 µS. The typical ultra-low I_Q is 15 µA with channel 1 set to 3.3 V and the channel 2 disabled. If ultra-low I_Q is not required, connect MODE to AGND. In normal mode, the I_Q is 25 µA with channel 1 set to 3.3 V and the second channel disabled.

8.4.2 Diode Emulation Mode

A fully synchronous buck regulator implemented with a low-side synchronous MOSFET rather than a diode has the capability to sink negative current from the output during light-load, overvoltage, and pre-bias start-up conditions. The LM5143-Q1 provides a diode emulation feature that can be enabled to prevent reverse (drain-to-source) current flow in the low-side MOSFET. When configured for diode emulation (DEM), the low-side MOSFET is switched off when reverse current flow is detected by sensing of the applicable SW voltage using a zero-cross comparator. The benefit of this configuration is lower power loss at light-load conditions; the disadvantage being slower light-load transient response.

The diode emulation feature is configured with the DEMB pin. To enable diode emulation and thus achieve discontinuous conduction mode (DCM) operation at light loads, connect DEMB to AGND. If FPWM or continuous conduction mode (CCM) operation is desired, tie DEMB to VDDA. See 表 8-4. Note that diode emulation is automatically engaged to prevent reverse current flow during a pre-bias start-up in FPWM. A gradual change from DCM to CCM operation provides monotonic start-up performance.

表 8-4. DEMB Settings

DEMB	FPWM / DEM
VDDA	FPWM
AGND	DEM
External clock	FPWM

8.4.3 Thermal Shutdown

The LM5143-Q1 includes an internal junction temperature monitor. If the temperature exceeds 175°C (typical), thermal shutdown occurs. When entering thermal shutdown, the device:

1. Turns off the high-side and low-side MOSFETs
2. Pulls SS1/2 and PG1/2 low
3. Turns off the VCC regulator
4. Initiates a soft-start sequence when the die temperature decreases by the thermal shutdown hysteresis of 15°C (typical)

This is a non-latching protection, and as such, the device cycles into and out of thermal shutdown if the fault persists.

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9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

The LM5143-Q1 is a synchronous buck controller used to convert a higher input voltage to two lower output voltages. The following sections discuss the design procedure for a dual-output implementation using a specific circuit design example. To expedite and streamline the process of designing of a LM5143-Q1-based regulator, a comprehensive *LM5143-Q1 Quickstart Calculator* is available for download to assist the designer with component selection for a given application.

9.1.1 Power Train Components

A comprehensive understanding of the buck regulator power train components is critical to successfully completing a synchronous buck regulator design. The following section discuss the the following:

- Output inductor
- Input and output capacitors
- Power MOSFETs
- EMI input filter

9.1.1.1 Buck Inductor

For most applications, choose a buck inductance such that the inductor ripple current, ΔI_L, is between 30% to 50% of the maximum DC output current at nominal input voltage. Choose the inductance using 式 15 based on a peak inductor current given by 式 16.

$$L_O = \frac{V_{OUT}}{\Delta I_L \cdot F_{SW}} \cdot \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \tag{15}$$

$$I_{L(peak)} = I_{OUT} + \frac{\Delta I_L}{2} \tag{16}$$

Check the inductor data sheet to make sure that the saturation current of the inductor is well above the peak inductor current of a particular design. Ferrite designs have very low core loss and are preferred at high switching frequencies, so design goals can then concentrate on copper loss and preventing saturation. Low inductor core loss is evidenced by reduced no-load input current and higher light-load efficiency. However, ferrite core materials exhibit a hard saturation characteristic and the inductance collapses abruptly when the saturation current is exceeded. This results in an abrupt increase in inductor ripple current and higher output voltage ripple, not to mention reduced efficiency and compromised reliability. Note that the saturation current of an inductor generally decreases as its core temperature increases. Of course, accurate overcurrent protection is key to avoiding inductor saturation.

9.1.1.2 Output Capacitors

Ordinarily, the output capacitor energy store of the regulator combined with the control loop response are prescribed to maintain the integrity of the output voltage within the dynamic (transient) tolerance specifications. The usual boundaries restricting the output capacitor in power management applications are driven by finite available PCB area, component footprint and profile, and cost. The capacitor parasitics—equivalent series resistance (ESR) and equivalent series inductance (ESL)—take greater precedence in shaping the load transient response of the regulator as the load step amplitude and slew rate increase.

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The output capacitor, C_{OUT}, filters the inductor ripple current and provides a reservoir of charge for step-load transient events. Typically, ceramic capacitors provide extremely low ESR to reduce the output voltage ripple and noise spikes, while tantalum and electrolytic capacitors provide a large bulk capacitance in a relatively compact footprint for transient loading events.

Based on the static specification of peak-to-peak output voltage ripple denoted by ΔV_{OUT}, choose an output capacitance that is larger than that given by 式 17.

$$C_{OUT} \geq \frac{\Delta I_L}{8 \cdot F_{SW} \sqrt{\Delta V_{OUT}^2 - \left(R_{ESR} \cdot \Delta I_L\right)^2}} \tag{17}$$

図 9-1 conceptually illustrates the relevant current waveforms during both load step-up and step-down transitions. As shown, the large-signal slew rate of the inductor current is limited as the inductor current ramps to match the new load-current level following a load transient. This slew-rate limiting exacerbates the deficit of charge in the output capacitor, which must be replenished as rapidly as possible during and after the load step-up transient. Similarly, during and after a load step-down transient, the slew rate limiting of the inductor current adds to the surplus of charge in the output capacitor that must be depleted as quickly as possible.

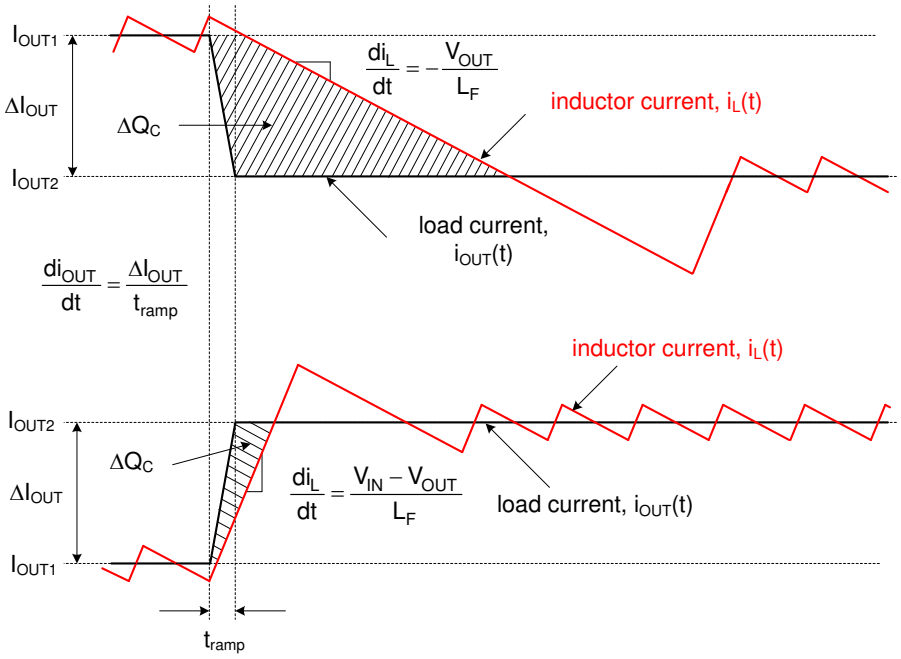


図 9-1. Load Transient Response Representation Showing C_{OUT} Charge Surplus or Deficit

In a typical regulator application of 12-V input to low output voltage (for example, 3.3 V), the load-off transient represents the worst case in terms of output voltage transient deviation. In that conversion ratio application, the steady-state duty cycle is approximately 28% and the large-signal inductor current slew rate when the duty cycle collapses to zero is approximately $-V_{OUT}/L$. Compared to a load-on transient, the inductor current takes much longer to transition to the required level. The surplus of charge in the output capacitor causes the output voltage to significantly overshoot. In fact, to deplete this excess charge from the output capacitor as quickly as possible, the inductor current must ramp below its nominal level following the load step. In this scenario, a large output capacitance can be advantageously employed to absorb the excess charge and minimize the voltage overshoot.

To meet the dynamic specification of output voltage overshoot during such a load-off transient (denoted as $\Delta V_{OVERSHOOT}$ with step reduction in output current given by ΔI_{OUT}), the output capacitance must be larger than:

$$C_{OUT} \geq \frac{L_O \cdot \Delta I_{OUT}^{\ 2}}{\left(V_{OUT} + \Delta V_{OVERSHOOT}\right)^2 - V_{OUT}^{\ 2}} \tag{18}$$

The ESR of a capacitor is provided in the manufacturer's data sheet either explicitly as a specification or implicitly in the impedance versus frequency curve. Depending on type, size, and construction, electrolytic capacitors have significant ESR, 5 mΩ and above, and relatively large ESL, 5 nH to 20 nH. PCB traces contribute some parasitic resistance and inductance as well. Ceramic output capacitors, on the other hand, have low ESR and ESL contributions at the switching frequency, and the capacitive impedance component dominates. However, depending on the package and voltage rating of the ceramic capacitor, the effective capacitance can drop quite significantly with applied DC voltage and operating temperature.

Ignoring the ESR term in 式 17 gives a quick estimation of the minimum ceramic capacitance necessary to meet the output ripple specification. Two to four 47-µF, 10-V, X7R capacitors in 1206 or 1210 footprint is a common choice for a 5-V output. Use 式 18 to determine if additional capacitance is necessary to meet the load-off transient overshoot specification.

A composite implementation of ceramic and electrolytic capacitors highlights the rationale for paralleling capacitors of dissimilar chemistries yet complementary performance. The frequency response of each capacitor is accretive in that each capacitor provides desirable performance over a certain portion of the frequency range. While the ceramic provides excellent mid- and high-frequency decoupling characteristics with its low ESR and ESL to minimize the switching frequency output ripple, the electrolytic device with its large bulk capacitance provides low-frequency energy storage to cope with load transient demands.

9.1.1.3 Input Capacitors

Input capacitors are necessary to limit the input ripple voltage to the buck power stage due to switching-frequency AC currents. TI recommends using X7S or X7R dielectric ceramic capacitors to provide low impedance and high RMS current rating over a wide temperature range. To minimize the parasitic inductance in the switching loop, position the input capacitors as close as possible to the drain of the high-side MOSFET and the source of the low-side MOSFET. Use 式 19 to calculate the input capacitor RMS current for a single-channel buck regulator.

$$I_{CIN,rms} = \sqrt{D \cdot \left(I_{OUT}^{\ 2} \cdot (1 - D) + \frac{\Delta I_L^2}{12} \right)} \tag{19}$$

The highest input capacitor RMS current occurs at D = 0.5, at which point the RMS current rating of the input capacitors is greater than half the output current.

Ideally, the DC component of input current is provided by the input voltage source and the AC component by the input filter capacitors. Neglecting inductor ripple current, the input capacitors source current of amplitude (I_{OUT} − I_{IN}) during the D interval and sink I_{IN} during the 1−D interval. Thus, the input capacitors conduct a square-wave current of peak-to-peak amplitude equal to the output current. It follows that the resultant capacitive component of AC ripple voltage is a triangular waveform. Together with the ESR-related ripple component, use 式 20 to calculate the peak-to-peak ripple voltage amplitude.

$$\Delta V_{IN} = \frac{I_{OUT} \cdot D \cdot (1 - D)}{F_{SW} \cdot C_{IN}} + I_{OUT} \cdot R_{ESR} \tag{20}$$

Use 式 21 to calculate the input capacitance required for a particular load current, based on an input voltage ripple specification of ΔV_{IN}.

$$C_{IN} \geq \frac{D \cdot (1 - D) \cdot I_{OUT}}{F_{SW} \cdot \left(\Delta V_{IN} - R_{ESR} \cdot I_{OUT}\right)} \tag{21}$$

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Low-ESR ceramic capacitors can be placed in parallel with higher valued bulk capacitance to provide optimized input filtering for the regulator and damping to mitigate the effects of input parasitic inductance resonating with high-Q ceramics. One bulk capacitor of sufficiently high current rating and four 10-µF 50-V X7R ceramic decoupling capacitors are usually sufficient for 12-V battery automotive applications. Select the input bulk capacitor based on its ripple current rating and operating temperature range.

Of course, a two-channel buck regulator with 180° out-of-phase interleaved switching provides input ripple current cancellation and reduced input capacitor current stress. The previous equations represent valid calculations when one output is disabled and the other output is fully loaded.

9.1.1.4 Power MOSFETs

The choice of power MOSFETs has significant impact on DC/DC regulator performance. A MOSFET with low on-state resistance, $R_{DS(on)}$, reduces conduction loss, whereas low parasitic capacitances enable faster transition times and reduced switching loss. Normally, the lower the $R_{DS(on)}$ of a MOSFET, the higher the gate charge and output charge (Q_G and Q_{OSS}, respectively), and vice versa. As a result, the product of $R_{DS(on)}$ and Q_G is commonly specified as a MOSFET figure-of-merit. Low thermal resistance of a given package ensures that the MOSFET power dissipation does not result in excessive MOSFET die temperature.

The main parameters affecting power MOSFET selection in a LM5143-Q1 application are as follows:

- $R_{DS(on)}$ at V_{GS} = 5 V
- Drain-source voltage rating, BV_{DSS}, is typically 40 V, 60 V, or 80 V, depending on the maximum input voltage.
- Gate charge parameters at V_{GS} = 5 V
- Output charge, Q_{OSS}, at the relevant input voltage
- Body diode reverse recovery charge, Q_{RR}
- Gate threshold voltage, $V_{GS(th)}$, derived from the Miller plateau evident in the Q_G versus V_{GS} plot in the MOSFET data sheet. With a Miller plateau voltage typically in the range of 2 V to 3 V, the 5-V gate drive amplitude of the LM5143-Q1 provides an adequately-enhanced MOSFET when on and a margin against Cdv/dt shoot-through when off.

The MOSFET-related power losses for one channel are summarized by the equations presented in 表 9-1, where suffixes 1 and 2 represent high-side and low-side MOSFET parameters, respectively. While the influence of inductor ripple current is considered, second-order loss modes, such as those related to parasitic inductances and SW node ringing, are not included. Consult the *LM5143-Q1 Quickstart Calculator*. The calculator is available for download from the LM5143-Q1 product folder to assist with power loss calculations.

表 9-1. MOSFET Power Losses

POWER LOSS MODE	HIGH-SIDE MOSFET	LOW-SIDE MOSFET
MOSFET conduction(2) (3)	$P_{cond1} = D \cdot \left({I_{OUT}}^2 + \frac{\Delta I_L^2}{12} \right) \cdot R_{DS(on)1}$	$P_{cond2} = D' \cdot \left({I_{OUT}}^2 + \frac{\Delta I_L^2}{12} \right) \cdot R_{DS(on)2}$
MOSFET switching	$P_{sw1} = \frac{V_{IN} \cdot F_{SW}}{2} \left[\left(I_{OUT} - \frac{\Delta I_L}{2} \right) \cdot t_R + \left(I_{OUT} + \frac{\Delta I_L}{2} \right) \cdot t_F \right]$	Negligible
MOSFET gate drive(1)	$P_{Gate1} = V_{CC} \cdot F_{SW} \cdot Q_{G1}$	$P_{Gate2} = V_{CC} \cdot F_{SW} \cdot Q_{G2}$
MOSFET output charge(4)	$P_{Coss} = F_{SW} \cdot \left(V_{IN} \cdot Q_{oss2} + E_{oss1} - E_{oss2} \right)$	Negligible
Body diode conduction	N/A	$P_{cond_{BD}} = V_F \cdot F_{SW} \left[\left(I_{OUT} + \frac{\Delta I_L}{2} \right) \cdot t_{dt1} + \left(I_{OUT} - \frac{\Delta I_L}{2} \right) \cdot t_{dt2} \right]$
Body diode reverse recovery(5)	$P_{RR} = V_{IN} \cdot F_{SW} \cdot Q_{RR2}$	

(1) Gate drive loss is apportioned based on the internal gate resistance of the MOSFET, externally added series gate resistance, and the relevant driver resistance of the LM5143-Q1.
(2) MOSFET $R_{DS(on)}$ has a positive temperature coefficient of approximately 4500 ppm/°C. The MOSFET junction temperature, T_J, and its rise over ambient temperature is dependent upon the device total power dissipation and its thermal impedance. When operating at or near minimum input voltage, make sure that the MOSFET $R_{DS(on)}$ is rated for the available gate drive voltage.
(3) D' = 1–D is the duty cycle complement.

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(4) MOSFET output capacitances, C_{oss1} and C_{oss2}, are highly non-linear with voltage. These capacitances are charged losslessly by the inductor current at high-side MOSFET turnoff. During turnon, however, a current flows from the input to charge the output capacitance of the low-side MOSFET. E_{oss1}, the energy of C_{oss1}, is dissipated at turnon, but this is offset by the stored energy E_{oss2} on C_{oss2}. For more detail, refer to "Comparison of deadtime effects on the performance of DC-DC converters with GaN FETs and silicon MOSFETs," ECCE 2016.
(5) MOSFET body diode reverse recovery charge, Q_{RR}, depends on many parameters, particularly forward current, current transition speed, and temperature.

The high-side (control) MOSFET carries the inductor current during the PWM on-time (or D interval) and typically incurs most of the switching losses, so it is imperative to choose a high-side MOSFET that balances conduction and switching loss contributions. The total power dissipation in the high-side MOSFET is the sum of the following:

- Losses due to conduction
- Switching (voltage-current overlap)
- Output charge
- Typically two-thirds of the net loss attributed to body diode reverse recovery

The low-side (synchronous) MOSFET carries the inductor current when the high-side MOSFET is off (or 1–D interval). The low-side MOSFET switching loss is negligible as it is switched at zero voltage – current just commutates from the channel to the body diode or vice versa during the transition deadtimes. The LM5143-Q1, with its adaptive gate drive timing, minimizes body diode conduction losses when both MOSFETs are off. Such losses scale directly with switching frequency.

In high step-down ratio applications, the low-side MOSFET carries the current for a large portion of the switching period. Therefore, to attain high efficiency, it is critical to optimize the low-side MOSFET for low $R_{DS(on)}$. In cases where the conduction loss is too high or the target $R_{DS(on)}$ is lower than available in a single MOSFET, connect two low-side MOSFETs in parallel. The total power dissipation of the low-side MOSFET is the sum of the losses due to channel conduction, body diode conduction, and typically one-third of the net loss attributed to body diode reverse recovery. The LM5143-Q1 is well suited to drive TI's portfolio of NexFET™ power MOSFETs.

9.1.1.5 EMI Filter

Switching regulators exhibit negative input impedance, which is lowest at the minimum input voltage. An underdamped LC filter exhibits a high output impedance at the resonant frequency of the filter. For stability, the filter output impedance must be less than the absolute value of the converter input impedance.

$$Z_{IN} = \left| -\frac{V_{IN(min)}^{2}}{P_{IN}} \right| \tag{22}$$

The EMI filter design steps are as follows:

- Calculate the required attenuation of the EMI filter at the switching frequency, where C_{IN} represents the existing capacitance at the input of the switching converter.
- The input filter inductor L_{IN} is usually selected between 1 µH and 10 µH, but it can be lower to reduce losses in a high-current design.
- Calculate input filter capacitor C_F.

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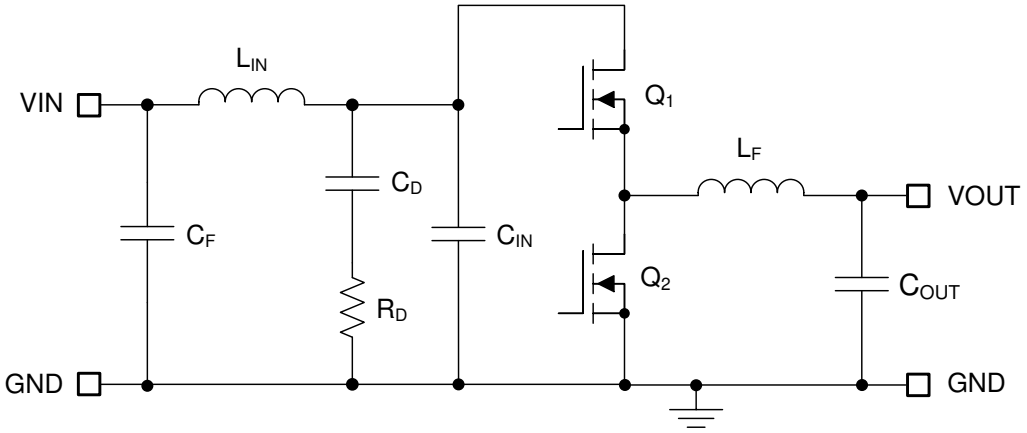


図 9-2. Buck Regulator With π-Stage EMI Filter

By calculating the first harmonic current from the Fourier series of the input current waveform and multiplying it by the input impedance (the impedance is defined by the existing input capacitor C_{IN}), a formula is derived to obtain the required attenuation as shown by 式 23.

$$Attn = 20\log\left(\frac{I_{L(PEAK)}}{\pi^2 \cdot F_{SW} \cdot C_{IN}} \cdot \sin\left(\pi \cdot D_{MAX}\right) \cdot \frac{1}{1\,\mu V}\right) - V_{MAX} \tag{23}$$

where

- V_{MAX} is the allowed dBµV noise level for the applicable conducted EMI specification (for example, CISPR 25 Class 5)
- C_{IN} is the existing input capacitance of the buck regulator
- D_{MAX} is the maximum duty cycle
- I_{PEAK} is the peak inductor current

For filter design purposes, the current at the input can be modeled as a square-wave. Determine the EMI filter capacitance C_F from 式 24.

$$C_F = \frac{1}{L_{IN}}\left(\frac{10^{\frac{|Attn|}{40}}}{2\pi \cdot F_{SW}}\right)^2 \tag{24}$$

Adding an input filter to a switching regulator modifies the control-to-output transfer function. The output impedance of the filter must be sufficiently small such that the input filter does not significantly affect the loop gain of the buck converter. The impedance peaks at the filter resonant frequency. Use 式 25 to calculate the resonant frequency of the filter.

$$f_{res} = \frac{1}{2\pi \cdot \sqrt{L_{IN} \cdot C_F}} \tag{25}$$

The purpose of R_D is to reduce the peak output impedance of the filter at its resonant frequency. Capacitor C_D blocks the DC component of the input voltage to avoid excessive power dissipation in R_D. Capacitor C_D must have lower impedance than R_D at the resonant frequency with a capacitance value greater than that of the input capacitor C_{IN}. This prevents C_{IN} from interfering with the cutoff frequency of the main filter. Added damping is needed when the output impedance of the filter is high at the resonant frequency (Q of the filter formed by L_{IN} and C_{IN} is too high). An electrolytic capacitor C_D can be used for damping with a value given by 式 26.

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$$C_D \geq 4 \cdot C_{IN} \tag{26}$$

Use 式 27 to select the damping resistor R_D.

$$R_D = \sqrt{\frac{L_{IN}}{C_{IN}}} \tag{27}$$

9.1.2 Error Amplifier and Compensation

図 9-3 shows a Type-II compensator using a transconductance error amplifier (EA). The dominant pole of the EA open-loop gain is set by the EA output resistance, $R_{O\text{-}EA}$, and effective bandwidth-limiting capacitance, C_{BW}, as shown in 式 28.

$$G_{EA(open\,loop)}(s) = -\frac{g_m \cdot R_{O\text{-}EA}}{1 + s \cdot R_{O\text{-}EA} \cdot C_{BW}} \tag{28}$$

The EA high-frequency pole is neglected in the 式 28. The compensator transfer function from output voltage to COMP node, including the gain contribution from the (internal or external) feedback resistor network, is calculated in 式 29.

$$G_c(s) = \frac{\hat{v}_c(s)}{\hat{v}_{out}(s)} = -\frac{V_{REF}}{V_{OUT}} \cdot \frac{g_m \cdot R_{O\text{-}EA} \cdot \left(1 + \frac{s}{\omega_{z1}}\right)}{\left(1 + \frac{s}{\omega_{p1}}\right) \cdot \left(1 + \frac{s}{\omega_{p2}}\right)} \tag{29}$$

where

- V_{REF} is the feedback voltage reference of 0.6 V
- g_m is the EA gain transconductance of 1200 µS
- $R_{O\text{-}EA}$ is the error amplifier output impedance of 64 MΩ

$$\omega_{Z1} = \frac{1}{R_{COMP} \cdot C_{COMP}} \tag{30}$$

$$\omega_{p1} = \frac{1}{R_{O\text{-}EA} \cdot (C_{COMP} + C_{HF} + C_{BW})} \cong \frac{1}{R_{O\text{-}EA} \cdot C_{COMP}} \tag{31}$$

$$\omega_{p2} = \frac{1}{R_{COMP} \cdot \left(C_{COMP} \parallel (C_{HF} + C_{BW})\right)} \cong \frac{1}{R_{COMP} \cdot C_{HF}} \tag{32}$$

The EA compensation components create a pole close to the origin, a zero, and a high-frequency pole. Typically, $R_{COMP} << R_{O\text{-}EA}$ and $C_{COMP} >> C_{BW}$ and C_{HF}, so the approximations are valid.

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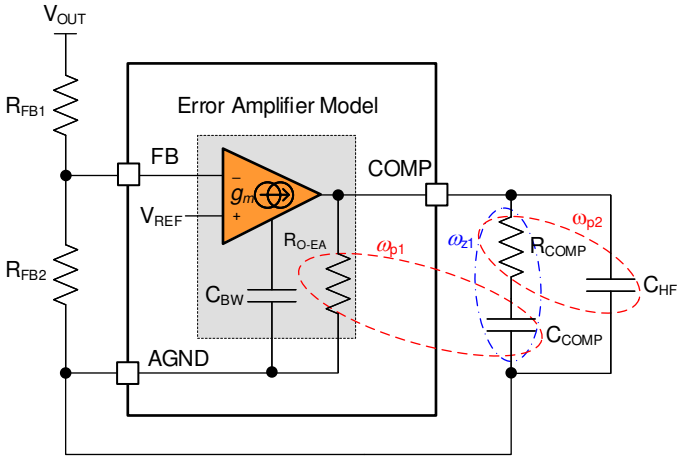


図 9-3. Error Amplifier and Compensation Network

9.2 Typical Applications

9.2.1 Design 1 – High Efficiency, Dual-Output Buck Regulator for Automotive Applications

図 9-4 shows the schematic diagram of a dual-output synchronous buck regulator with output voltages setpoints of 3.3 V and 5 V and a rated load current of 7 A for each output. In this example, the target half-load and full-load efficiencies are 91% and 90%, respectively, based on a nominal input voltage of 12 V that ranges from 3.5 V to 36 V. The switching frequency is set at 2.1 MHz by resistor R_{RT}. The 5-V output is connected to VCCX to reduce IC bias power dissipation and improve efficiency.

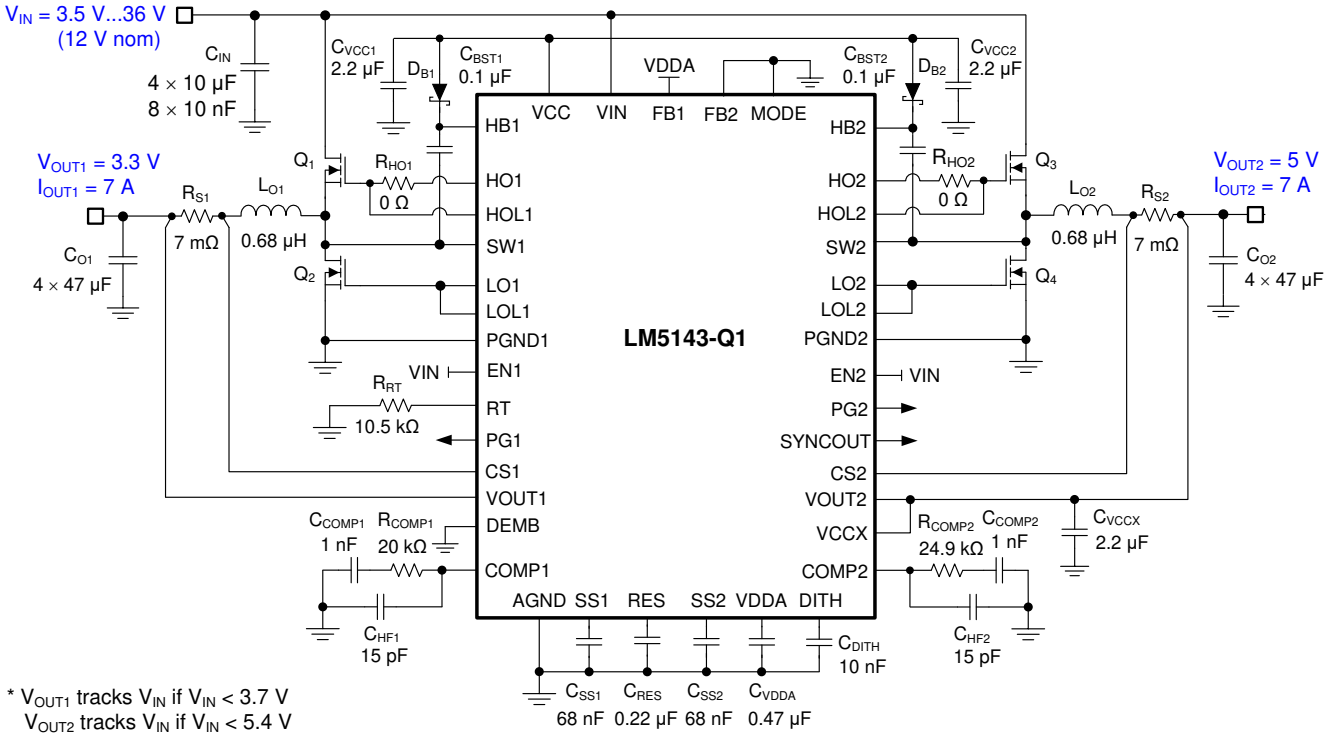


図 9-4. Application Circuit 1 With LM5143-Q1 Buck Regulator at 2.1 MHz

Note

This and subsequent design examples are provided herein to showcase the LM5143-Q1 controller in several different applications. Depending on the source impedance of the input supply bus, an electrolytic capacitor can be required at the input to ensure stability, particularly at low input voltage and high output current operating conditions. See *Section 10* for more details.

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9.2.1.1 Design Requirements

表 9-2 shows the intended input, output, and performance parameters for this automotive design example.

表 9-2. Design Parameters

DESIGN PARAMETER	VALUE
Input voltage range (steady-state)	8 V to 18 V
Min transient input voltage (cold crank)	3.5 V
Max transient input voltage (load dump)	36 V
Output voltages	3.3 V, 5 V
Output currents	7 A
Switching frequency	2.1 MHz
Output voltage regulation	±1%
Standby current, output 1 enabled, no-load	< 50 µA
Shutdown current	4 µA

The switching frequency is set at 2.1 MHz by resistor R_{RT}. In terms of control loop performance, the target loop crossover frequency is 60 kHz with a phase margin greater than 50°. The output voltage soft-start times are set at 2 ms by 68-nF soft-start capacitors.

The selected buck regulator powertrain components are cited in 表 9-3, and many of the components are available from multiple vendors. The MOSFETs in particular are chosen for both lowest conduction and switching power loss, as discussed in detail in *セクション 9.1.1.4*. This design uses a low-DCR, metal-powder composite inductor, and ceramic output capacitor implementation.

表 9-3. List of Materials for Application Circuit 1 (1)

REFERENCE DESIGNATOR	QTY	SPECIFICATION	MANUFACTURER	PART NUMBER
C_{IN}	4	10 µF, 50 V, X7R, 1210, ceramic, AEC-Q200	Taiyo Yuden	UMJ325KB7106KMHT
		10 µF, 50 V, X7S, 1210, ceramic, AEC-Q200	Murata	GCM32EC71H106KA03
			TDK	CGA6P3X7S1H106M
C_O	8	47 µF, 6.3 V, X7R, 1210, ceramic, AEC-Q200	Murata	GCM32ER70J476KE19L
			Taiyo Yuden	JMK325B7476KMHTR
		47 µF, 6.3 V, X7S, 1210, ceramic, AEC-Q200	TDK	CGA6P1X7S0J476M
L_{O1}, L_{O2}	2	0.68 µH, 4.8 mΩ, 25 A, 7.3 × 6.6 × 2.8 mm, AEC-Q200	Würth Electronik	744373460068
		0.68 µH, 4.5 mΩ, 22 A, 6.95 × 6.6 × 2.8 mm, AEC-Q200	Cyntec	VCMV063T-R68MN2T
		0.68 µH, 3.1 mΩ, 20 A, 7 × 6.9 × 3.8 mm, AEC-Q200	Würth Electronik	744311068
		0.68 µH, 7.4 mΩ, 12.2 A, 5.4 × 5.0 × 3 mm, AEC-Q200	TDK	SPM5030VT-R68-D
		0.68 µH, 2.9 mΩ, 15.3 A, 6.71 × 6.51 × 3.1 mm, AEC-Q200	Coilcraft	XGL6030-681
Q_1, Q_2, Q_3, Q_4	4	40 V, 5.7 mΩ, 9 nC, SON 5 × 6, AEC-Q101	Infineon	IPC50N04S5L-5R5
R_{S1}, R_{S2}	2	Shunt, 7 mΩ, 0508, 1 W, AEC-Q200	Susumu	KRL2012E-M-R007
U_1	1	LM5143-Q1 65-V dual-channel buck controller, AEC-Q100	Texas Instruments	LM5143QRGWRQ1

(1) See *Third Party Disclaimer*.

9.2.1.2 Detailed Design Procedure

9.2.1.2.1 Custom Design With WEBENCH® Tools

Click here to create a custom design using the LM5143-Q1 device with the WEBENCH® Power Designer.

1. Start by entering the input voltage (V_{IN}), output voltage (V_{OUT}), and output current (I_{OUT}) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

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The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance
- Run thermal simulations to understand board thermal performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

9.2.1.2.2 Custom Design With Excel Quickstart Tool

Select components based on the regulator specifications using the *LM5143-Q1 Quickstart Calculator* available for download from the LM5143-Q1 product folder.

9.2.1.2.3 Inductor Calculation

1. Use 式 33 to calculate the required buck inductance for each channel based on a 30% inductor ripple current at nominal input voltages.

$$L_{O1} = \frac{V_{OUT1}}{V_{IN(nom)}} \cdot \left(\frac{V_{IN(nom)} - V_{OUT1}}{\Delta I_L \cdot F_{SW}} \right) = \frac{3.3\,V}{12\,V} \cdot \left(\frac{12\,V - 3.3\,V}{2.1A \cdot 2.1MHz} \right) = 0.54\,\mu H$$

$$L_{O2} = \frac{V_{OUT2}}{V_{IN(nom)}} \cdot \left(\frac{V_{IN(nom)} - V_{OUT2}}{\Delta I_L \cdot F_{SW}} \right) = \frac{5\,V}{12\,V} \cdot \left(\frac{12\,V - 5\,V}{2.1A \cdot 2.1MHz} \right) = 0.66\,\mu H \quad (33)$$

2. Select a standard inductor value of 0.68 µH for both channels. Use 式 34 to calculate the peak inductor currents at maximum steady-state input voltage. Subharmonic oscillation occurs with a duty cycle greater than 50% for peak current-mode control. For design simplification, the LM5143-Q1 has an internal slope compensation ramp proportional to the switching frequency that is added to the current sense signal to damp any tendency toward subharmonic oscillation.

$$I_{LO1(PK)} = I_{OUT1} + \frac{\Delta I_{LO1}}{2} = I_{OUT1} + \frac{V_{OUT1}}{2 \cdot L_{O1} \cdot F_{SW}} \cdot \left(1 - \frac{V_{OUT1}}{V_{IN(max)}} \right) = 7\,A + \frac{3.3\,V}{2 \cdot 0.68\,\mu H \cdot 2.1MHz} \cdot \left(1 - \frac{3.3\,V}{18\,V} \right) = 7.94\,A$$

$$I_{LO2(PK)} = I_{OUT2} + \frac{\Delta I_{LO2}}{2} = I_{OUT2} + \frac{V_{OUT2}}{2 \cdot L_{O2} \cdot F_{SW}} \cdot \left(1 - \frac{V_{OUT2}}{V_{IN(max)}} \right) = 7\,A + \frac{5\,V}{2 \cdot 0.68\,\mu H \cdot 2.1MHz} \cdot \left(1 - \frac{5\,V}{18\,V} \right) = 8.27\,A \quad (34)$$

3. Based on 式 10, use 式 35 to cross-check the inductance to set a slope compensation equal to the ideal one times the inductor current downslope.

$$L_{O1(sc)} = \frac{V_{OUT}\,(V) \cdot R_S\,(m\Omega)}{24 \cdot F_{SW}\,(MHz)} = \frac{3.3\,V \cdot 7\,m\Omega}{24 \cdot 2.1\,MHz} = 0.46\,\mu H$$

$$L_{O2(sc)} = \frac{V_{OUT}\,(V) \cdot R_S\,(m\Omega)}{24 \cdot F_{SW}\,(MHz)} = \frac{5\,V \cdot 7\,m\Omega}{24 \cdot 2.1\,MHz} = 0.69\,\mu H \quad (35)$$

9.2.1.2.4 Current-Sense Resistance

1. Calculate the current-sense resistance based on a maximum peak current capability of at least 20% higher than the peak inductor current at full load to provide sufficient margin during start-up and load-on transients. Calculate the current sense resistances using 式 36.

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$$R_{S1} = \frac{V_{CS(th)}}{1.2 \cdot I_{LO1(PK)}} = \frac{73\,mV}{1.2 \cdot 7.94\,A} = 7.66\,m\Omega$$

$$R_{S2} = \frac{V_{CS(th)}}{1.2 \cdot I_{LO2(PK)}} = \frac{73\,mV}{1.2 \cdot 8.27\,A} = 7.36\,m\Omega \quad (36)$$

where

- $V_{CS(th)}$ is the 73-mV current limit threshold.

2. Select a standard resistance value of 7 mΩ for both shunts. A 0508 footprint component with wide aspect ratio termination design provides 1-W power rating, low parasitic series inductance, and compact PCB layout. Carefully observe the *セクション 11.1* to make sure that noise and DC errors do not corrupt the differential current-sense voltages measured at [CS1, VOUT1] and [CS2, VOUT2].
3. Place the shunt resistor close to the inductor.
4. Use Kelvin-sense connections, and route the sense lines differentially from the shunt to the LM5143-Q1.
5. The CS-to-output propagation delay (related to the current limit comparator, internal logic and power MOSFET gate drivers) causes the peak current to increase above the calculated current limit threshold. For a total propagation delay of $t_{CS-DELAY}$ of 40 ns, use 式 37 to calculate the worst-case peak inductor current with the output shorted.

$$I_{LO1(PK-SC)} = I_{LO2(PK-SC)} = \frac{V_{CS(th)}}{R_{S1}} + \frac{V_{IN(max)} \cdot t_{CS-DELAY}}{L_{O1}} = \frac{73\,mV}{7\,m\Omega} + \frac{18\,V \cdot 40\,ns}{0.68\,\mu H} = 11.49\,A \quad (37)$$

6. Based on this result, select an inductor for each channel with saturation current greater than 12 A across the full operating temperature range.

9.2.1.2.5 Output Capacitors

1. Use 式 38 to estimate the output capacitance required to manage the output voltage overshoot during a load-off transient (from full load to no load) assuming a load transient deviation specification of 1.5% (50 mV for a 3.3-V output).

$$C_{OUT1} \geq \frac{L_{O1} \cdot \Delta I_{OUT1}^{\,2}}{\left(V_{OUT1} + \Delta V_{OVERSHOOT1}\right)^2 - V_{OUT1}^{\,2}} = \frac{0.68\,\mu H \cdot (7\,A)^2}{(3.3\,V + 50\,mV)^2 - (3.3\,V)^2} = 100.2\,\mu F$$

$$C_{OUT2} \geq \frac{L_{O2} \cdot \Delta I_{OUT2}^{\,2}}{\left(V_{OUT2} + \Delta V_{OVERSHOOT2}\right)^2 - V_{OUT2}^{\,2}} = \frac{0.68\,\mu H \cdot (7\,A)^2}{(5\,V + 75\,mV)^2 - (5\,V)^2} = 44.1\,\mu F \quad (38)$$

2. Noting the voltage coefficient of ceramic capacitors where the effective capacitance decreases significantly with applied voltage, select four 47-µF, 6.3-V, X7R, 1210 ceramic output capacitors for each channel. Generally, when sufficient capacitance is used to satisfy the load-off transient response requirement, the voltage undershoot during a no-load to full-load transient is also satisfactory.
3. Use 式 39 to estimate the peak-peak output voltage ripple of channel 1 at nominal input voltage.

$$\Delta V_{OUT1} = \sqrt{\left(\frac{\Delta I_{LO1}}{8 \cdot F_{SW} \cdot C_{OUT1}}\right)^2 + \left(R_{ESR} \cdot \Delta I_{LO1}\right)^2} = \sqrt{\left(\frac{1.89\,A}{8 \cdot 2.1\,MHz \cdot 130\,\mu F}\right)^2 + \left(1\,m\Omega \cdot 1.89\,A\right)^2} \approx 2\,mV \quad (39)$$

where

- R_{ESR} is the effective equivalent series resistance (ESR) of the output capacitors.
- 130 µF is the total effective (derated) ceramic output capacitance at 3.3 V.

4. Use 式 40 to calculate the output capacitor RMS ripple current using and verify that the ripple current is within the capacitor ripple current rating.

$$I_{CO1(RMS)} = \frac{\Delta I_{LO1}}{\sqrt{12}} = \frac{1.89\,A}{\sqrt{12}} = 0.55\,A$$

$$I_{CO2(RMS)} = \frac{\Delta I_{LO2}}{\sqrt{12}} = \frac{2.53\,A}{\sqrt{12}} = 0.73\,A \quad (40)$$

9.2.1.2.6 Input Capacitors

A power supply input typically has a relatively high source impedance at the switching frequency. Good-quality input capacitors are necessary to limit the input ripple voltage. As mentioned earlier, dual-channel interleaved operation significantly reduces the input ripple amplitude. In general, the ripple current splits between the input capacitors based on the relative impedance of the capacitors at the switching frequency.

1. Select the input capacitors with sufficient voltage and RMS ripple current ratings.
2. Worst case input ripple for a two-channel buck regulator typically corresponds to when one channel operates at full load and the other channel is disabled or operates at no load. Use 式 41 to calculate the input capacitor RMS ripple current assuming a worst-case duty-cycle operating point of 50%.

$$I_{CIN(RMS)} = I_{OUT1} \cdot \sqrt{D \cdot (1-D)} = 7\,A \cdot \sqrt{0.5 \cdot (1-0.5)} = 3.5\,A \quad (41)$$

3. Use Equation 42 to find the required input capacitance.

$$C_{IN} \geq \frac{D \cdot (1-D) \cdot I_{OUT1}}{F_{SW} \cdot (\Delta V_{IN} - R_{ESR} \cdot I_{OUT1})} = \frac{0.5 \cdot (1-0.5) \cdot 7\,A}{2.1MHz \cdot (120\,mV - 2m\Omega \cdot 7\,A)} = 7.8\,\mu F \quad (42)$$

where

- ΔV_{IN} is the input peak-to-peak ripple voltage specification.
- R_{ESR} is the input capacitor ESR.

4. Recognizing the voltage coefficient of ceramic capacitors, select two 10-µF, 50-V, X7R, 1210 ceramic input capacitors for each channel. Place these capacitors adjacent to the relevant power MOSFETs.
5. Use four 10-nF, 50-V, X7R, 0603 ceramic capacitors near each high-side MOSFET to supply the high di/dt current during MOSFET switching transitions. Such capacitors offer high self-resonant frequency (SRF) and low effective impedance above 100 MHz. The result is lower power loop parasitic inductance, thus minimizing switch-node voltage overshoot and ringing for lower EMI signature. Refer to 図 11-2 in *Layout Guidelines* for more details.

9.2.1.2.7 Compensation Components

Choose compensation components for a stable control loop using the procedure outlined as follows.

1. Based on a specified open-loop gain crossover frequency, f_C, of 60 kHz, use 式 43 to calculate R_{COMP1}, assuming an effective output capacitance of 130 µF. Select R_{COMP1} of 20 kΩ.

$$R_{COMP1} = 2 \cdot \pi \cdot f_C \cdot \frac{V_{OUT}}{V_{REF}} \cdot \frac{R_S \cdot G_{CS}}{g_m} \cdot C_{OUT} = 2 \cdot \pi \cdot 60kHz \cdot \frac{3.3\,V}{0.6\,V} \cdot \frac{7m\Omega \cdot 12}{1200\,\mu S} \cdot 130\,\mu F = 18.9k\Omega \quad (43)$$

2. Calculate C_{COMP1} to create a zero at the higher of (1) one tenth of the crossover frequency, or (2) the load pole. Select a C_{COMP1} capacitor of 1 nF.

$$C_{COMP1} = \frac{10}{2 \cdot \pi \cdot f_C \cdot R_{COMP1}} = \frac{10}{2 \cdot \pi \cdot 60kHz \cdot 20\,k\Omega} = 1.3\,nF \quad (44)$$

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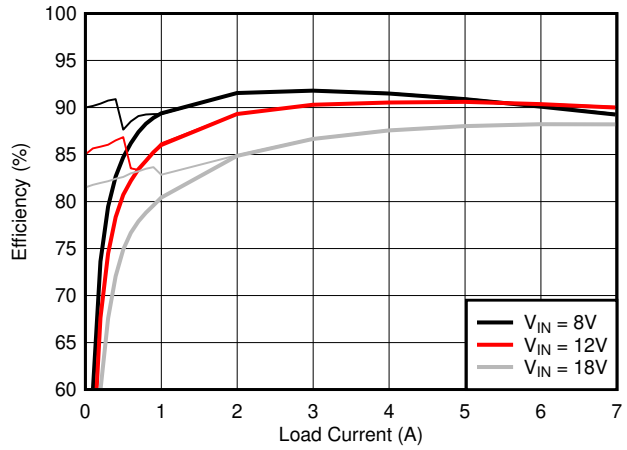
3. Calculate C_{HF1} to create a pole at the ESR zero and to attenuate high-frequency noise at COMP. Select a C_{HF1} capacitor of 15 pF.

$$C_{HF1} = \frac{1}{2 \cdot \pi \cdot f_{ESR} \cdot R_{COMP1}} = \frac{1}{2 \cdot \pi \cdot 500\,kHz \cdot 20\,k\Omega} = 15.9\,pF \quad (45)$$

Note

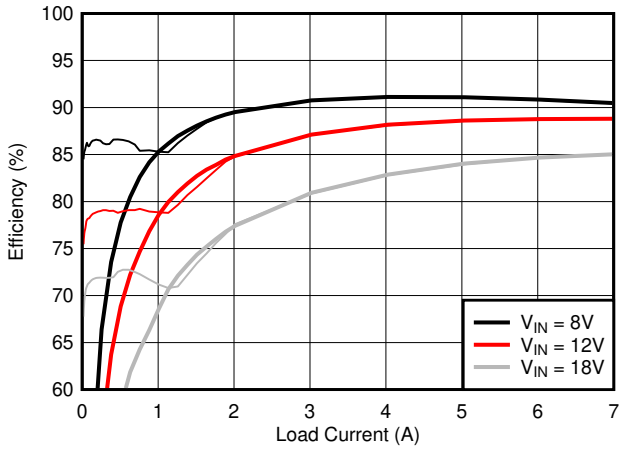
Set a fast loop with high R_{COMP} and low C_{COMP} values to improve the response when recovering from operation in dropout.

9.2.1.3 Application Curves



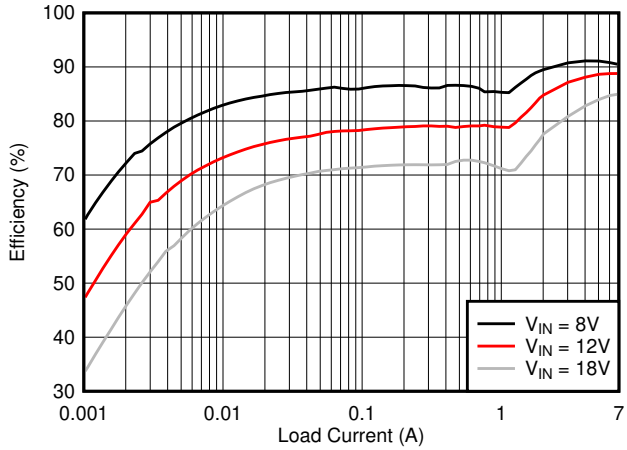
Channels loaded equally

図 9-5. Efficiency versus I_{OUT}



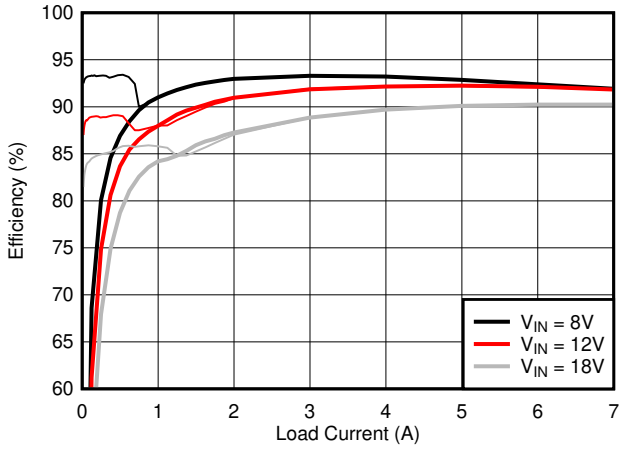
3.3-V output, channel 2 disabled

図 9-6. Efficiency versus I_{OUT}



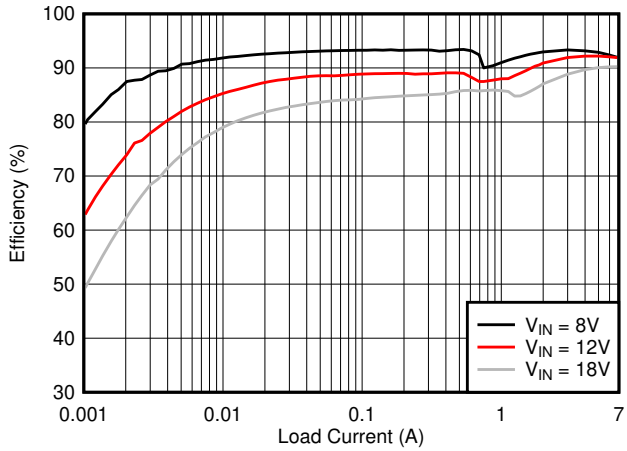
3.3-V output, channel 2 disabled

図 9-7. Efficiency versus I_{OUT}, Log Scale



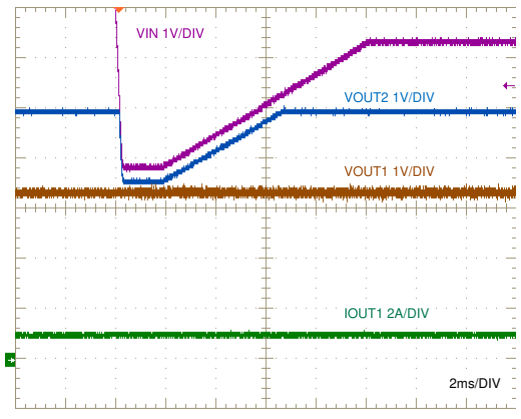
5-V output, channel 1 disabled

図 9-8. Efficiency versus I_{OUT}



5-V output, channel 1 disabled

図 9-9. Efficiency versus I_{OUT}, Log Scale

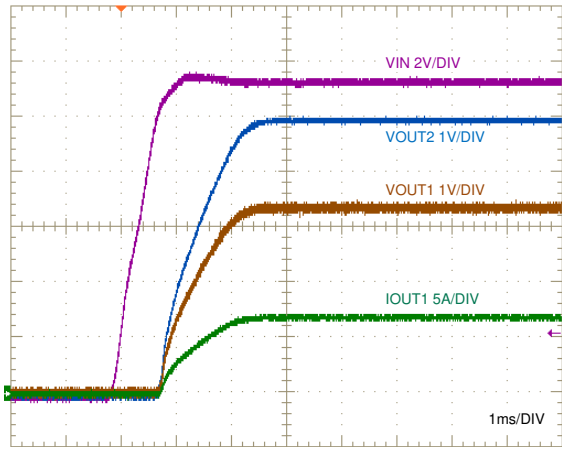


1-A loads

図 9-10. Cold-Crank Response to V_{IN} = 3.8 V

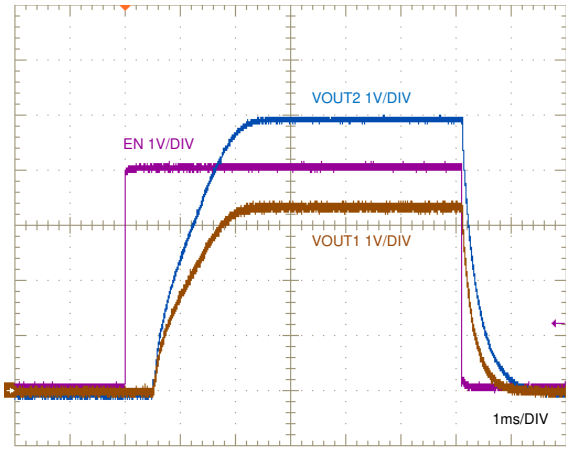
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9.2.1.3 Application Curves (continued)



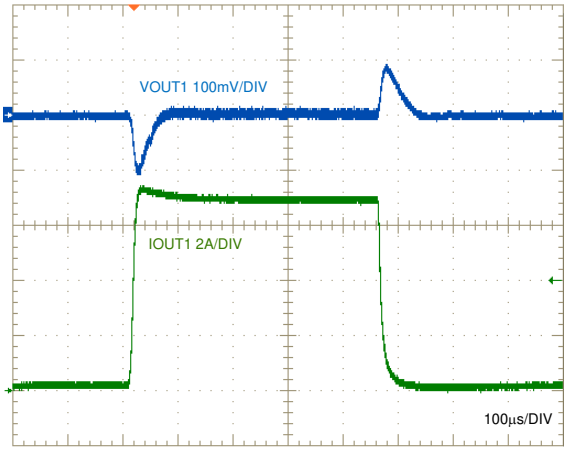
V_{IN} step to 12 V 7-A resistive loads

図 9-11. Start-Up Characteristic



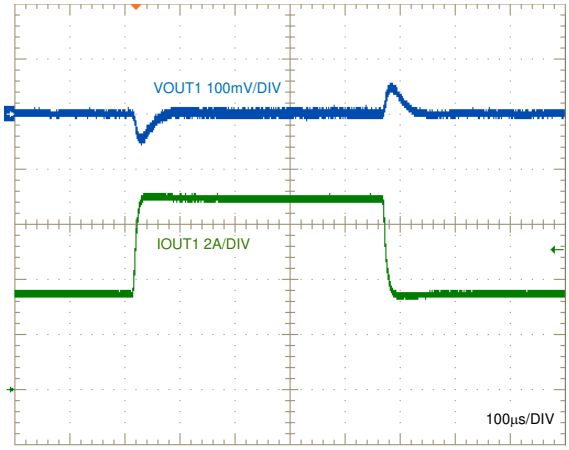
V_{IN} = 12 V 7-A resistive loads

図 9-12. ENABLE ON and OFF Characteristic



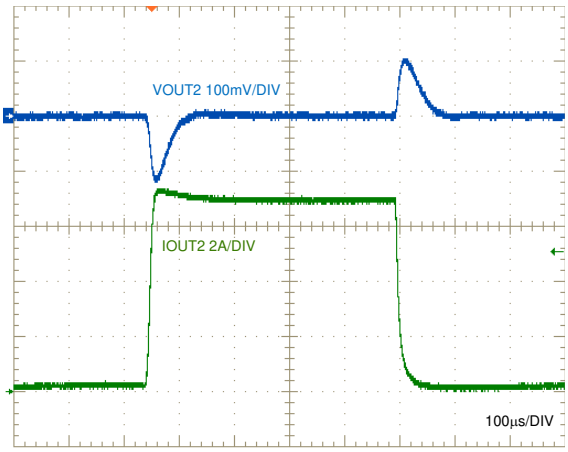
V_{IN} = 12 V FPWM

図 9-13. Load Transient, 3.3-V Output, 0 A to 7 A



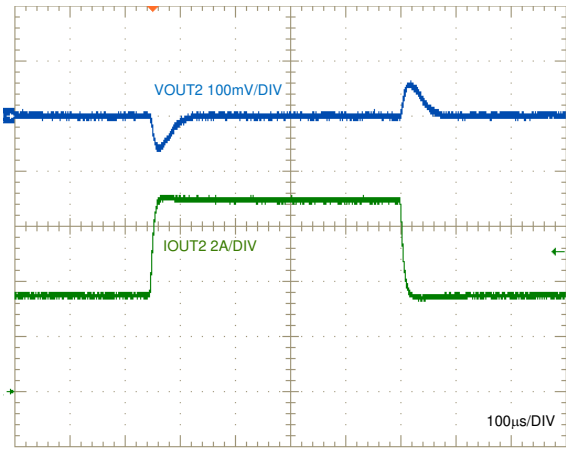
V_{IN} = 12 V FPWM

図 9-14. Load Transient, 3.3-V Output, 3.5 A to 7 A



V_{IN} = 12 V FPWM

図 9-15. Load Transient, 5-V Output, 0 A to 7 A

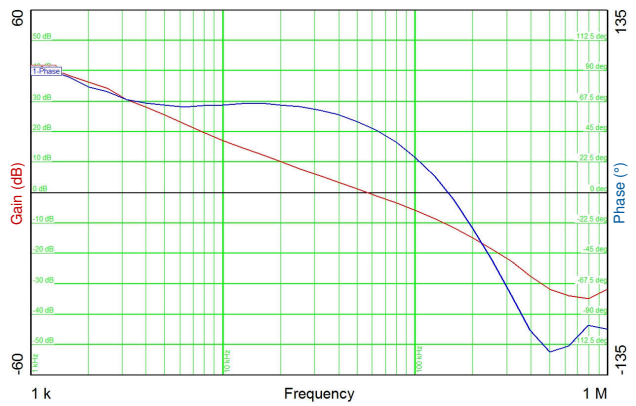


V_{IN} = 12 V FPWM

図 9-16. Load Transient, 5-V Output, 3.5 A to 7 A

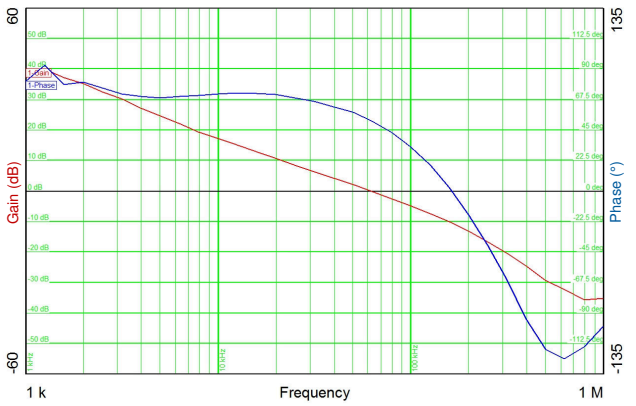
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9.2.1.3 Application Curves (continued)



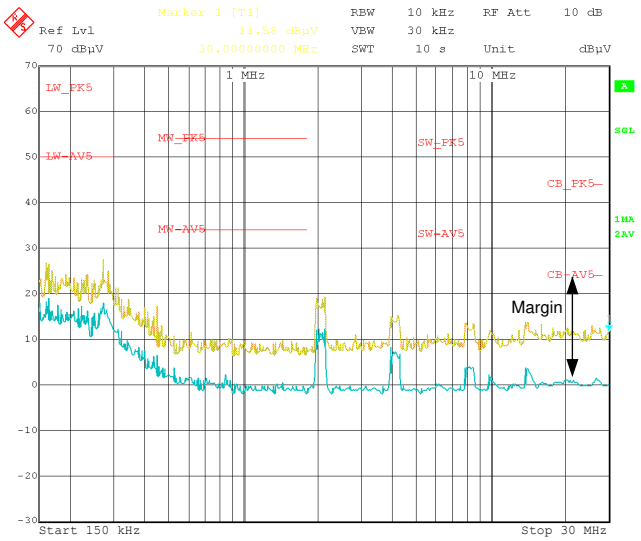
V_{IN} = 12 V 7-A resistive load

図 9-17. Bode Plot, 3.3-V Output



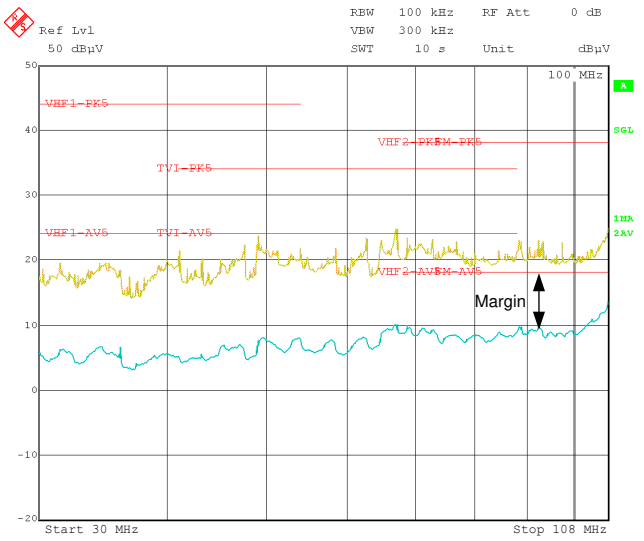
V_{IN} = 12 V 7-A resistive load

図 9-18. Bode Plot, 5-V Output



V_{IN} = 13.5 V V_{OUT} = 5 V 7-A resistive load

図 9-19. CISPR 25 Class 5 Conducted EMI, 150 kHz to 30 MHz



V_{IN} = 13.5 V V_{OUT} = 5 V 7-A resistive load

図 9-20. CISPR 25 Class 5 Conducted EMI, 30 MHz to 108 MHz

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9.2.2 Design 2 – Two-Phase, Single-Output Buck Regulator for Automotive ADAS Applications

図 9-21 shows the schematic diagram of a single-output, two-phase synchronous buck regulator with an output voltage of 5 V and rated load current of 15 A. In this example, the target half-load and full-load efficiencies are 93% and 91%, respectively, based on a nominal input voltage of 12 V that ranges from 5 V to 36 V. The switching frequency is set at 2.1 MHz by resistor R_{RT}. The 5-V output is connected to VCCX to reduce IC bias power dissipation and improve light-load efficiency. An output voltage of 3.3 V is also feasible simply by connecting FB1 to VDDA.

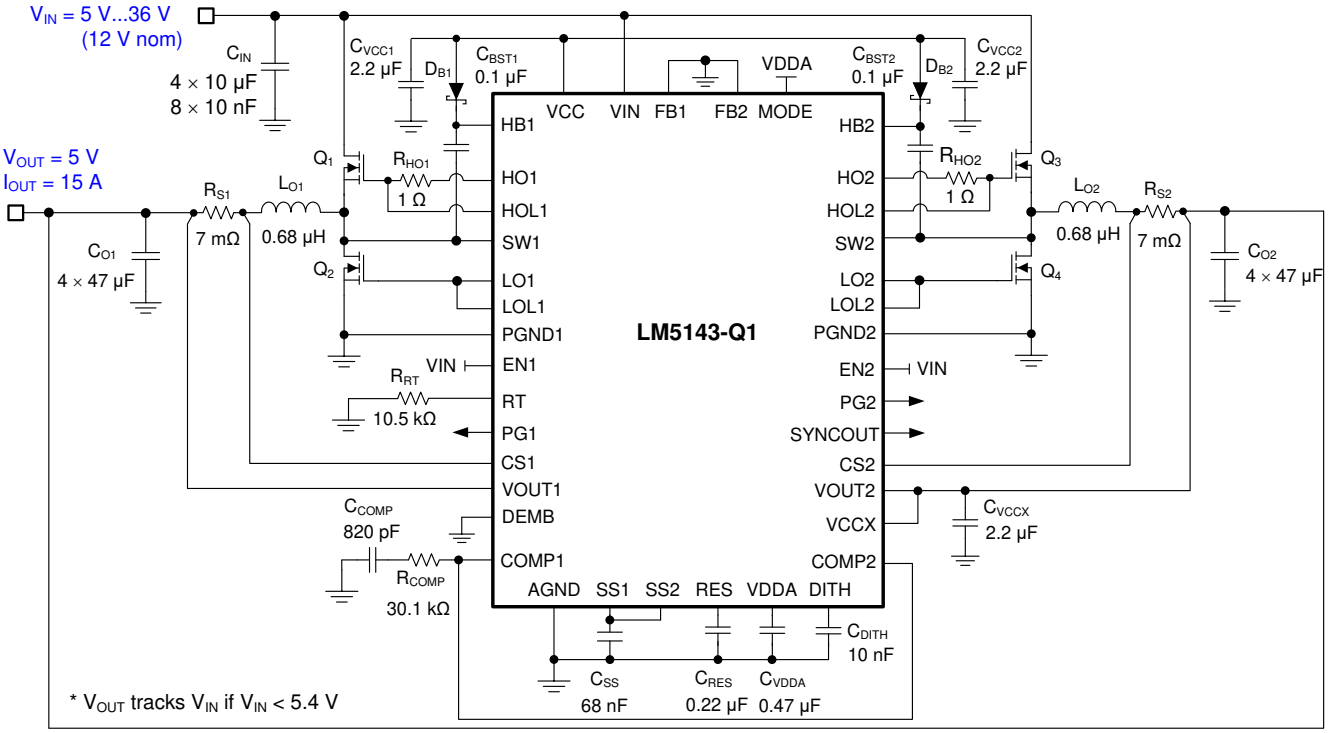


図 9-21. Application Circuit 2 With LM5143-Q1 Buck Regulator at 2.1 MHz

9.2.2.1 Design Requirements

表 9-4 shows the intended input, output, and performance parameters for this automotive application design example.

表 9-4. Design Parameters

DESIGN PARAMETER	VALUE
Input voltage range (steady-state)	5 V to 18 V
Minimum transient input voltage (cold crank)	5 V
Maximum transient input voltage (load dump)	36 V
Output voltages	5 V
Output currents	15 A
Switching frequency	2.1 MHz
Output voltage regulation	±1%
Standby current, output 1 enabled, no-load	< 50 µA
Shutdown current	4 µA

The switching frequency is set at 2.1 MHz by resistor R_{RT}. In terms of control loop performance, the target loop crossover frequency is 60 kHz with a phase margin greater than 50°. The output voltage soft-start time is set at 2 ms by a 68-nF soft-start capacitor.

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The selected buck regulator powertrain components are cited in 表 9-5, and many of the components are available from multiple vendors. Similar to design 1, this design uses a low-DCR, metal-powder composite inductor, and ceramic output capacitor implementation.

表 9-5. List of Materials for Application Circuit 2

REFERENCE DESIGNATOR	QTY	SPECIFICATION	MANUFACTURER	PART NUMBER
C_{IN}	4	10 µF, 50 V, X7R, 1210, ceramic, AEC-Q200	Taiyo Yuden	UMJ325KB7106KMHT
		10 µF, 50 V, X7S, 1210, ceramic, AEC-Q200	Murata	GCM32EC71H106KA03
			TDK	CGA6P3X7S1H106M
C_O	8	47 µF, 6.3 V, X7R, 1210, ceramic, AEC-Q200	Murata	GCM32ER70J476KE19L
			Taiyo Yuden	JMK325B7476KMHTR
		47 µF, 6.3 V, X7S, 1210, ceramic, AEC-Q200	TDK	CGA6P1X7S0J476M
L_{O1}, L_{O2}	2	0.68 µH, 4.8 mΩ, 25 A, 7.3 × 6.6 × 2.8 mm, AEC-Q200	Würth Electronik	744373460068
		0.68 µH, 4.5 mΩ, 22 A, 6.95 × 6.6 × 2.8 mm, AEC-Q200	Cyntec	VCMV063T-R68MN2T
		0.68 µH, 3.1 mΩ, 20 A, 7 × 6.9 × 3.8 mm, AEC-Q200	Würth Electronik	744311068
		0.68 µH, 7.4 mΩ, 12.2 A, 5.4 × 5.0 × 3 mm, AEC-Q200	TDK	SPM5030VT-R68-D
		0.68 µH, 2.9 mΩ, 15.3 A, 6.7 × 6.5 × 3.1 mm, AEC-Q200	Coilcraft	XGL6030-681
Q_1, Q_2, Q_3, Q_4	4	40 V, 5.7 mΩ, 9 nC, SON 5 × 6, AEC-Q101	Infineon	IPC50N04S5L-5R5
R_{S1}, R_{S2}	2	Shunt, 7 mΩ, 0508, 1 W, AEC-Q200	Susumu	KRL2012E-M-R007
U_1	1	LM5143-Q1 65-V dual-channel buck controller, AEC-Q100	Texas Instruments	LM5143QRGWRQ1

9.2.2.2 Detailed Design Procedures

See セクション 9.2.1.2.

9.2.2.3 Application Curves

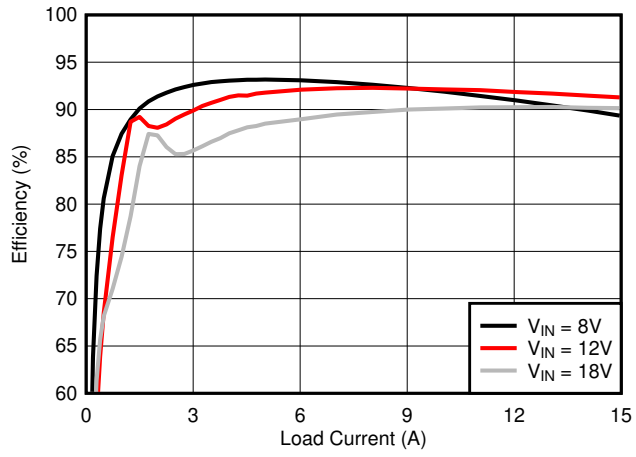
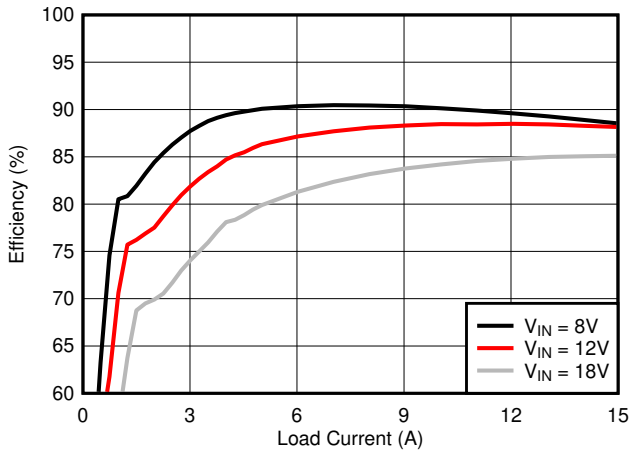


図 9-22. Efficiency versus I_{OUT}, 5-V Output



Configure the regulator as a 3.3-V output by tying FB1 to VDDA.

図 9-23. Efficiency versus I_{OUT}, 3.3-V Output

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10 Power Supply Recommendations

The LM5143-Q1 buck controller is designed to operate over a wide input voltage range of 3.5 V to 65 V. The characteristics of the input supply must be compatible with the *Absolute Maximum Ratings* and *Recommended Operating Conditions* . In addition, the input supply must be capable of delivering the required input current to the fully-loaded regulator. Use 式 46 to estimate the average input current.

$$I_{IN} = \frac{P_{OUT}}{V_{IN} \cdot \eta} \tag{46}$$

where

- η is the efficiency

If the regulator is connected to an input supply through long wires or PCB traces with a large impedance, take special care to achieve stable performance. The parasitic inductance and resistance of the input cables may have an adverse effect on converter operation. The parasitic inductance in combination with the low-ESR ceramic input capacitors form an underdamped resonant circuit. This circuit can cause overvoltage transients at VIN each time the input supply is cycled ON and OFF. The parasitic resistance causes the input voltage to dip during a load transient. The best way to solve such issues is to reduce the distance from the input supply to the regulator and use an aluminum or tantalum input capacitor in parallel with the ceramics. The moderate ESR of the electrolytic capacitors helps to damp the input resonant circuit and reduce any voltage overshoots. A capacitance in the range of 10 µF to 47 µF is usually sufficient to provide parallel input damping and helps to hold the input voltage steady during large load transients.

An EMI input filter is often used in front of the regulator that, unless carefully designed, can lead to instability as well as some of the affects mentioned above. The *Simple Success with Conducted EMI for DC-DC Converters Application Report* provides helpful suggestions when designing an input filter for any switching regulator.

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11 Layout

11.1 Layout Guidelines

Proper PCB design and layout is important in a high-current, fast-switching circuits (with high current and voltage slew rates) to achieve a robust and reliable design. As expected, certain issues must be considered before designing a PCB layout using the LM5143-Q1. The high-frequency power loop of a buck regulator power stage is denoted by loop 1 in the shaded area of 図 11-1. The topological architecture of a buck regulator means that particularly high di/dt current flows in the components of loop 1, and it becomes mandatory to reduce the parasitic inductance of this loop by minimizing its effective loop area. Also important are the gate drive loops of the low-side and high-side MOSFETs, denoted by 2 and 3, respectively, in 図 11-1.

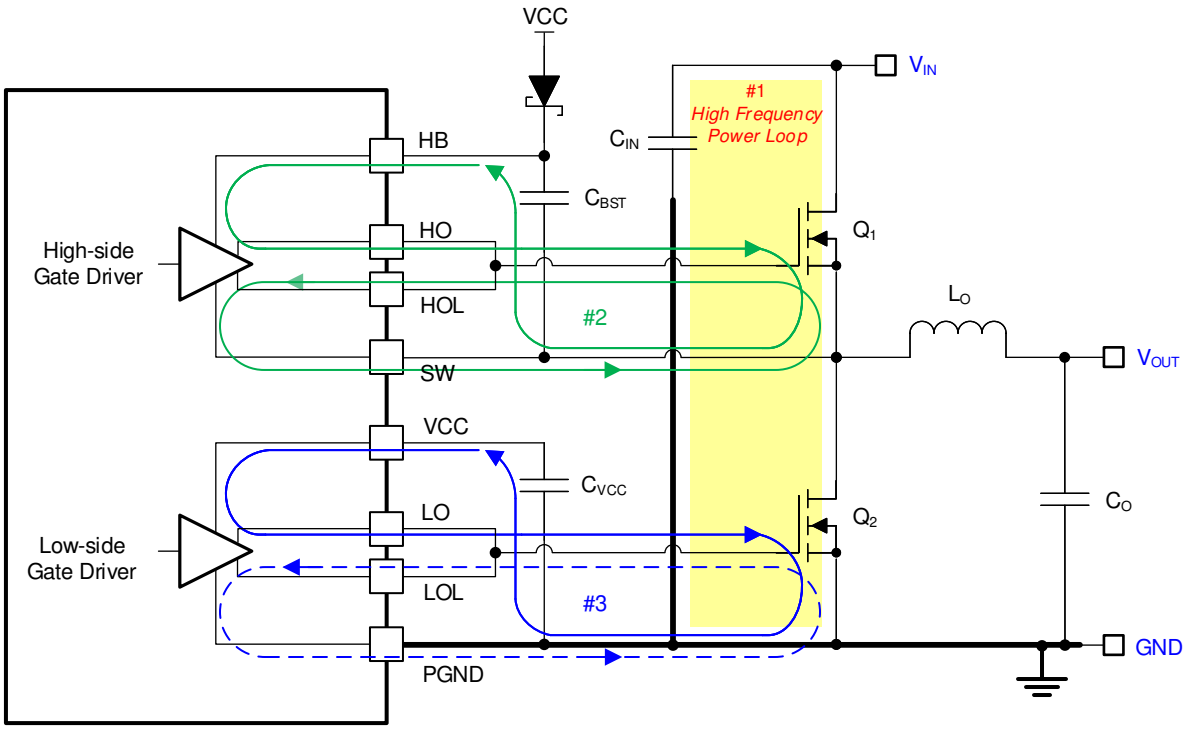


図 11-1. DC/DC Regulator Ground System With Power Stage and Gate Drive Circuit Switching Loops

11.1.1 Power Stage Layout

1. Input capacitors, output capacitors, and MOSFETs are the constituent components of the power stage of a buck regulator and are typically placed on the top side of the PCB (solder side). The benefits of convective heat transfer are maximized because of leveraging any system-level airflow. In a two-sided PCB layout, small-signal components are typically placed on the bottom side (component side). Insert at least one inner plane, connected to ground, to shield and isolate the small-signal traces from noisy power traces and lines.
2. The DC/DC regulator has several high-current loops. Minimize the area of these loops in order to suppress generated switching noise and optimize switching performance.
   - Loop 1: The most important loop area to minimize is the path from the input capacitor or capacitors through the high- and low-side MOSFETs, and back to the capacitor or capacitors through the ground connection. Connect the input capacitor or capacitors negative terminal close to the source of the low-side MOSFET (at ground). Similarly, connect the input capacitor or capacitors positive terminal close to the drain of the high-side MOSFET (at VIN). Refer to loop 1 of 図 11-1.
   - Another loop, not as critical as loop 1, is the path from the low-side MOSFET through the inductor and output capacitor or capacitors, and back to source of the low-side MOSFET through ground. Connect the source of the low-side MOSFET and negative terminal of the output capacitor or capacitors at ground as close as possible.

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3. The PCB trace defined as SW node, which connects to the source of the high-side (control) MOSFET, the drain of the low-side (synchronous) MOSFET and the high-voltage side of the inductor, must be short and wide. However, the SW connection is a source of injected EMI and thus must not be too large.
4. Follow any layout considerations of the MOSFETs as recommended by the MOSFET manufacturer, including pad geometry and solder paste stencil design.
5. The SW pin connects to the switch node of the power conversion stage and acts as the return path for the high-side gate driver. The parasitic inductance inherent to loop 1 in 図 11-1 and the output capacitance (C_{OSS}) of both power MOSFETs form a resonant circuit that induces high frequency (greater than 50 MHz) ringing at the SW node. The voltage peak of this ringing, if not controlled, can be significantly higher than the input voltage. Make sure that the peak ringing amplitude does not exceed the absolute maximum rating limit for the SW pin. In many cases, a series resistor and capacitor snubber network connected from the SW node to GND damps the ringing and decreases the peak amplitude. Provide provisions for snubber network components in the PCB layout. If testing reveals that the ringing amplitude at the SW pin is excessive, then include snubber components as needed.

11.1.2 Gate-Drive Layout

The LM5143-Q1 high-side and low-side gate drivers incorporate short propagation delays, adaptive dead-time control, and low-impedance output stages capable of delivering large peak currents with very fast rise and fall times to facilitate rapid turnon and turnoff transitions of the power MOSFETs. Very high di/dt can cause unacceptable ringing if the trace lengths and impedances are not well controlled.

Minimization of stray or parasitic gate loop inductance is key to optimizing gate drive switching performance, whether it be series gate inductance that resonates with MOSFET gate capacitance or common source inductance (common to gate and power loops) that provides a negative feedback component opposing the gate drive command, thereby increasing MOSFET switching times. The following loops are important:

- Loop 2: high-side MOSFET, Q_1. During the high-side MOSFET turnon, high current flows from the bootstrap (boot) capacitor through the gate driver and high-side MOSFET, and back to the negative terminal of the boot capacitor through the SW connection. Conversely, to turn off the high-side MOSFET, high current flows from the gate of the high-side MOSFET through the gate driver and SW, and back to the source of the high-side MOSFET through the SW trace. Refer to loop 2 of 図 11-1.
- Loop 3: low-side MOSFET, Q_2. During the low-side MOSFET turnon, high current flows from the VCC decoupling capacitor through the gate driver and low-side MOSFET, and back to the negative terminal of the capacitor through ground. Conversely, to turn off the low-side MOSFET, high current flows from the gate of the low-side MOSFET through the gate driver and GND, and back to the source of the low-side MOSFET through ground. Refer to loop 3 of 図 11-1.

TI strongly recommends following circuit layout guidelines when designing with high-speed MOSFET gate drive circuits.

1. Connections from gate driver outputs, HO1/2, HOL1/2, LO1/2, and LOL1/2 to the respective gates of the high-side or low-side MOSFETs must be as short as possible to reduce series parasitic inductance. Be aware that peak gate drive currents can be as high as 4.25 A. Use 0.65 mm (25 mils) or wider traces. Use via or vias, if necessary, of at least 0.5 mm (20 mils) diameter along these traces. Route HO and SW gate traces as a differential pair from the LM5143-Q1 to the high-side MOSFET, taking advantage of flux cancellation.
2. Minimize the current loop path from the VCC and HB pins through their respective capacitors as these provide the high instantaneous current, up to 4.25 A, to charge the MOSFET gate capacitances. Specifically, locate the bootstrap capacitor, C_{BST}, close to the HB and SW pins of the LM5143-Q1 to minimize the area of loop 2 associated with the high-side driver. Similarly, locate the VCC capacitor, C_{VCC}, close to the VCC and PGND pins of the LM5143-Q1 to minimize the area of loop 3 associated with the low-side driver.

11.1.3 PWM Controller Layout

With the provison to locate the controller as close as possible to the power MOSFETs to minimize gate driver trace runs, the components related to the analog and feedback signals as well as current sensing are considered in the following:

1. Separate power and signal traces, and use a ground plane to provide noise shielding.

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2. Place all sensitive analog traces and components related to COMP1/2, FB1/2, CS1/2, SS1/2, RES and RT away from high-voltage switching nodes such as SW1/2, HO1/2, LO1/2 or HB1/2 to avoid mutual coupling. Use internal layer or layers as ground plane or planes. Pay particular attention to shielding the feedback (FB) trace from power traces and components.
3. Locate the upper and lower feedback resistors (if required) close to the respective FB pins, keeping the FB traces as short as possible. Route the trace from the upper feedback resistor or resistors to the required output voltage sense point(s) at the load or loads.
4. Route the CS1/2 and VOUT1/2 traces as differential pairs to minimize noise pickup and use Kelvin connections to the applicable shunt resistor (if shunt current sensing is used) or to the sense capacitor (if inductor DCR current sensing is used).
5. Minimize the loop area from the VCC1/2 and VIN pins through their respective decoupling capacitors to the relevant PGND pins. Locate these capacitors as close as possible to the LM5143-Q1.

11.1.4 Thermal Design and Layout

The useful operating temperature range of a PWM controller with integrated gate drivers and bias supply LDO regulator is greatly affected by the following:

- Average gate drive current requirements of the power MOSFETs
- Switching frequency
- Operating input voltage (affecting bias regulator LDO voltage drop and hence its power dissipation)
- Thermal characteristics of the package and operating environment

For a PWM controller to be useful over a particular temperature range, the package must allow for the efficient removal of the heat produced while keeping the junction temperature within rated limits. The LM5143-Q1 controller is available in a small 6-mm × 6-mm 40-pin VQFNP (RGW) PowerPAD package to cover a range of application requirements. *Thermal Information* summarizes the thermal metrics of this package.

The 40-pin VQFNP package offers a means of removing heat from the semiconductor die through the exposed thermal pad at the base of the package. While the exposed pad of the package is not directly connected to any leads of the package, it is thermally connected to the substrate of the LM5143-Q1 device (ground). This allows a significant improvement in heat sinking, and it becomes imperative that the PCB is designed with thermal lands, thermal vias, and a ground plane to complete the heat removal subsystem. The exposed pad of the LM5143-Q1 is soldered to the ground-connected copper land on the PCB directly underneath the device package, reducing the thermal resistance to a very low value.

Numerous vias with a 0.3-mm diameter connected from the thermal land to the internal and solder-side ground plane or planes are vital to help dissipation. In a multi-layer PCB design, a solid ground plane is typically placed on the PCB layer below the power components. Not only does this provide a plane for the power stage currents to flow but it also represents a thermally conductive path away from the heat generating devices.

The thermal characteristics of the MOSFETs also are significant. The drain pads of the high-side MOSFETs are normally connected to a VIN plane for heat sinking. The drain pads of the low-side MOSFETs are tied to the respective SW planes, but the SW plane area is purposely kept as small as possible to mitigate EMI concerns.

11.1.5 Ground Plane Design

As mentioned previously, using one or more of the inner PCB layers as a solid ground plane is recommended. A ground plane offers shielding for sensitive circuits and traces and also provides a quiet reference potential for the control circuitry. Connect the PGND1 and PGND2 pins to the system ground plane using an array of vias under the exposed pad. Also connect the PGND1 and PGND2 pins directly to the return terminals of the input and output capacitors. The PGND nets contain noise at the switching frequency and can bounce because of load current variations. The power traces for PGND1/2, VIN and SW1/2 can be restricted to one side of the ground plane. The other side of the ground plane contains much less noise and is ideal for sensitive analog trace routes.

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11.2 Layout Example

Based on the *LM5143-Q1EVM-2100* design, 図 11-2 shows a single-sided layout of a dual-output synchronous buck regulator. Each power stage is surrounded by a GND pad geometry to connect an EMI shield if needed. The design uses layer 2 of the PCB as a power-loop return path directly underneath the top layer to create a low-area switching power loop of approximately 2 mm². This loop area, and hence parasitic inductance, must be as small as possible to minimize EMI as well as switch-node voltage overshoot and ringing. Refer to the *LM5143-Q1EVM-2100 Evaluation Module User's Guide* for more detail.

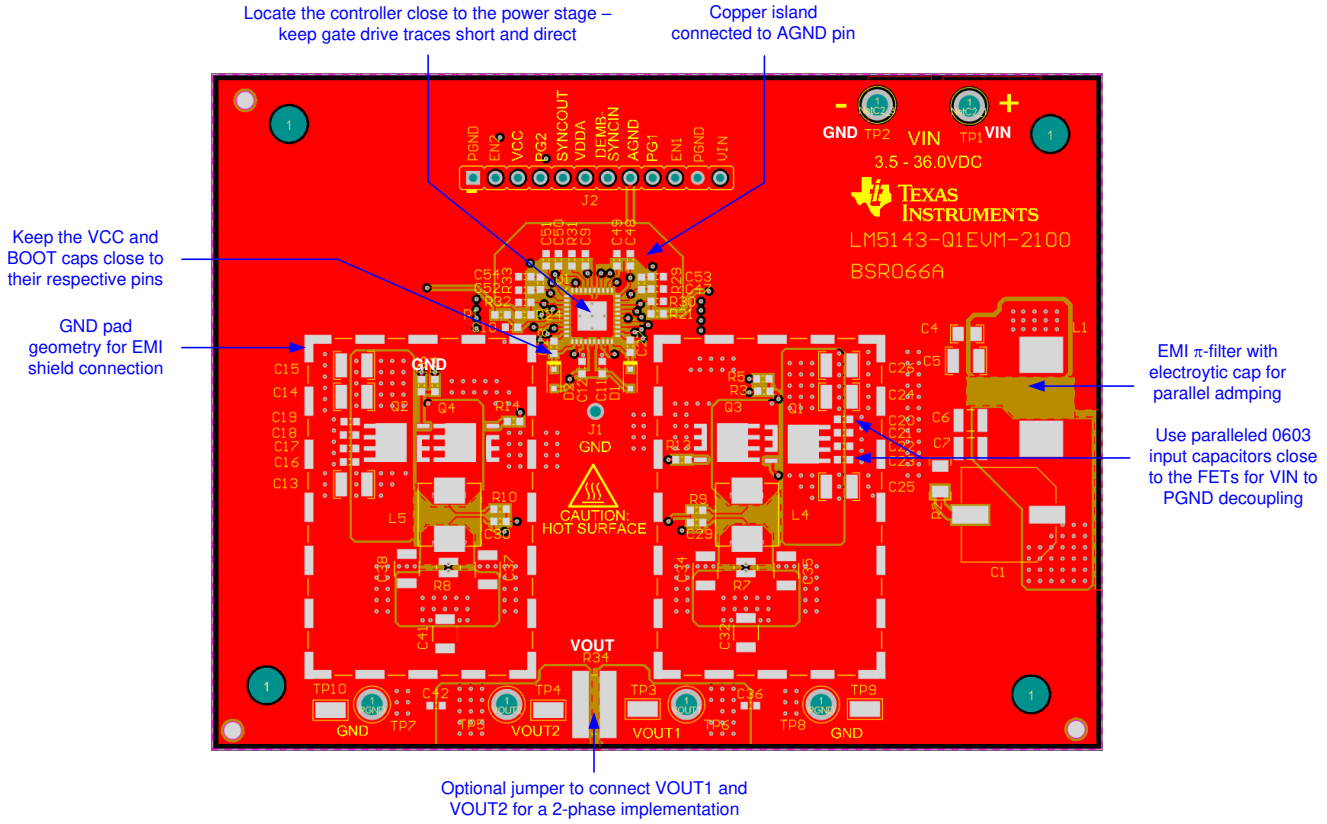


図 11-2. PCB Top Layer

As shown in 図 11-3, the high-frequency power loop current of one channel flows through MOSFETs Q2 and Q4, through the power ground plane on layer 2, and back to VIN through the 0603 ceramic capacitors C16 through C19. The currents flowing in opposing directions in the vertical loop configuration provide field self-cancellation, reducing parasitic inductance. 図 11-4 shows a side view to illustrate the concept of creating a low-profile, self-canceling loop in a multilayer PCB structure. The layer-2 GND plane layer, shown in 図 11-3, provides a tightly-coupled current return path directly under the MOSFETs to the source terminals of Q2.

Four 10-nF input capacitors with small 0402 or 0603 case size are placed in parallel very close to the drain of each high-side MOSFET. The low equivalent series inductance (ESL) and high self-resonant frequency (SRF) of the small footprint capacitors yield excellent high-frequency performance. The negative terminals of these capacitors are connected to the layer-2 GND plane with multiple 12-mil (0.3-mm) diameter vias, further minimizing parasitic loop inductance.

Additional steps used in this layout example include:

- Keep the SW connection from the power MOSFETs to the inductor (for each channel) at minimum copper area to reduce radiated EMI.
- Locate the controller close to the gate terminals of the MOSFETs such that the gate drive traces are routed short and direct.

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- Create an analog ground plane near the controller for sensitive analog components. The analog ground plane for AGND and power ground planes for PGND1 and PGND2 must be connected at a single point directly under the IC – at the die attach pad (DAP).

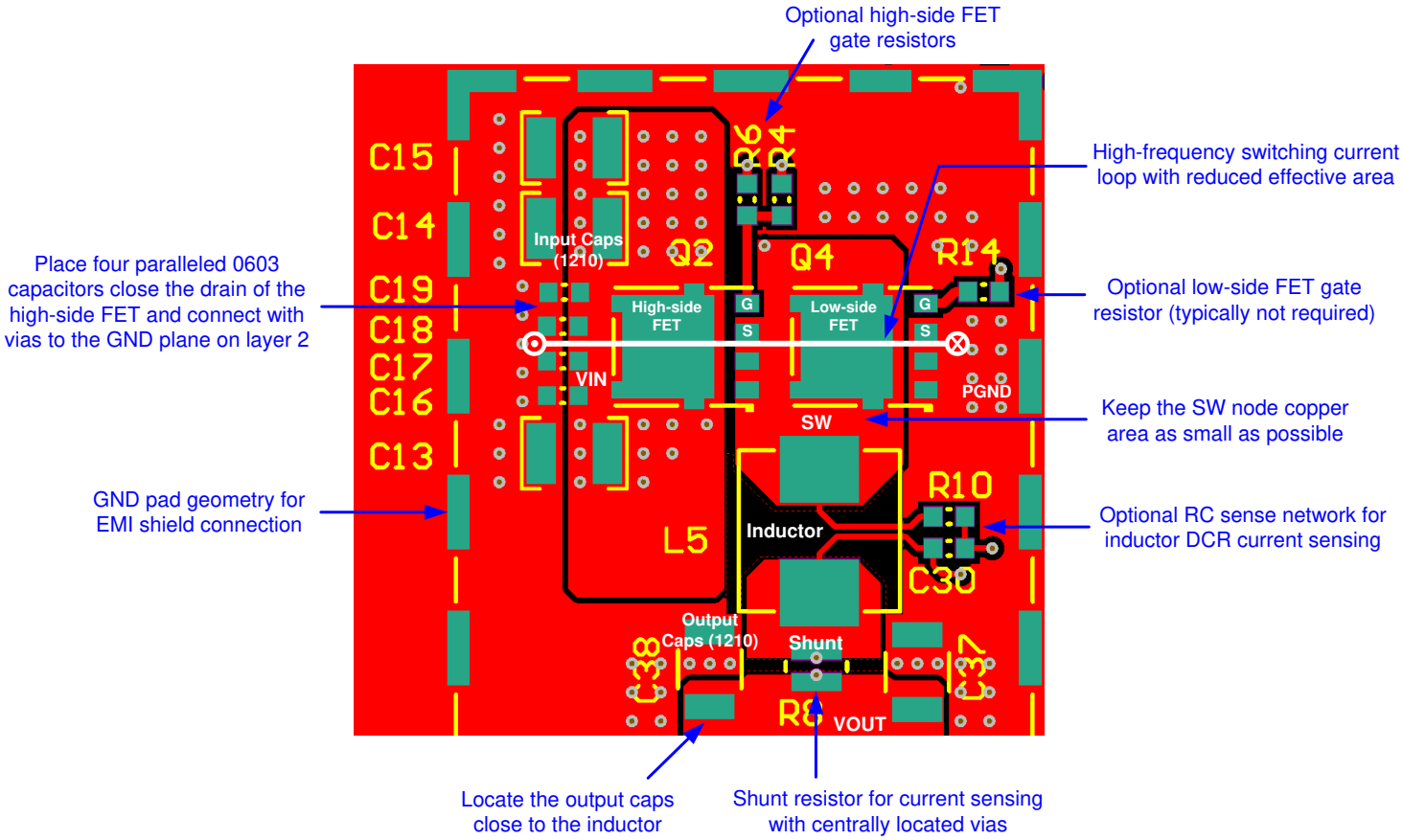
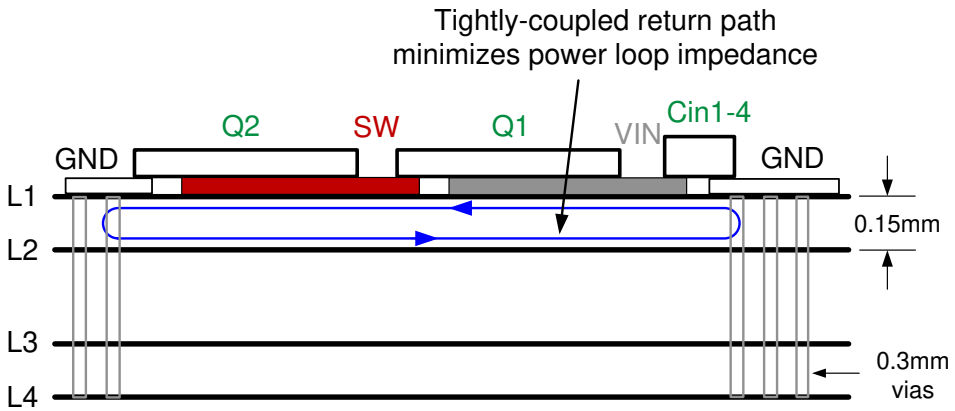


図 11-3. Power Stage Component Layout



Note

See the *Improve High-current DC/DC Regulator Performance for Free with Optimized Power Stage Layout* application report for more detail.

図 11-4. PCB Stack-up Diagram With Low L1-L2 Intra-layer Spacing

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12 Device and Documentation Support

12.1 Device Support

12.1.1 Third-Party Products Disclaimer

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12.1.2 Development Support

With an input operating voltage as low as 3.5 V and up to 100 V as specified in 表 12-1, the LM(2)514x-Q1 family of automotive synchronous buck controllers from TI provides flexibility, scalability and optimized solution size for a range of applications. These controllers enable DC/DC solutions with high density, low EMI and increased flexibility. Available EMI mitigation features include dual-random spread spectrum (DRSS) or triangular spread spectrum (TRSS), split gate driver outputs for slew rate (SR) control, and integrated active EMI filtering (AEF). All controllers are rated for a maximum operating junction temperature of 150°C, have AEC-Q100 grade 1 qualification, and are functional safety capable.

表 12-1. Automotive Synchronous Buck DC/DC Controller Family

DC/DC CONTROLLER	SINGLE or DUAL	V_{IN} RANGE	CONTROL METHOD	GATE DRIVE VOLTAGE	SYNC OUTPUT	EMI MITIGATION
LM25148-Q1	Single	3.5 V to 42 V	Peak current mode	5 V	180° phase shift	N/A
LM25149-Q1	Single	3.5 V to 42 V	Peak current mode	5 V	180° phase shift	N/A
LM25141-Q1	Single	3.8 V to 42 V	Peak current mode	5 V	N/A	SR control, TRSS
LM5141-Q1	Single	3.8 V to 65 V	Peak current mode	5 V	N/A	SR control, TRSS
LM5143-Q1	Dual	3.5 V to 65 V	Peak current mode	5 V	90° phase shift	SR control, TRSS
LM5145-Q1	Single	5.5 V to 75 V	Voltage mode	7.5 V	180° phase shift	N/A
LM5146-Q1	Single	5.5 V to 100 V	Voltage mode	7.5 V	180° phase shift	N/A

For development support, see the following:

- *LM5143-Q1 Quickstart Calculator*
- *LM5143-Q1 Simulation Models*
- *TI Reference Design Library*
- *WEBENCH® Design Center*
- To design a low-EMI power supply, review TI's comprehensive EMI Training Series
- TI Designs:
  - *Automotive wide V_{IN} front-end reference design for digital cockpit processing units*
- Technical Articles:
  - *High-density PCB layout of DC/DC converters*
  - *Synchronous buck controller solutions support wide V_{IN} performance and flexibility*
  - *How to use slew rate for EMI control*
  - *How to reduce EMI and shrink power-supply size with an integrated active EMI filter*

12.1.3 Custom Design With WEBENCH® Tools

Click here to create a custom design using the LM5143-Q1 device with the WEBENCH® Power Designer.

1. Start by entering the input voltage (V_{IN}), output voltage (V_{OUT}), and output current (I_{OUT}) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer gives a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

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- Run electrical simulations to see important waveforms and circuit performance
- Run thermal simulations to understand board thermal performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

12.2 Documentation Support

12.2.1 Related Documentation

For related documentation see the following:

- User's Guides:
  - *LM5143-Q1 Synchronous Buck Controller EVM*
  - *LM5140-Q1 Synchronous Buck Controller High Density EVM*
  - *LM5141-Q1 Synchronous Buck Controller EVM*
  - *LM5146-Q1 EVM User's Guide*
  - *LM5145 EVM User's Guide*
- Application Reports:
  - *LM5143-Q1 Synchronous Buck Controller High-Density 4-Phase Design*
  - *AN-2162 Simple Success with Conducted EMI from DC-DC Converters*
  - *Maintaining Output Voltage Regulation During Automotive Cold-Crank with LM5140-Q1 Dual Synchronous Buck Controller*
- Technical Briefs:
  - *Reduce Buck Converter EMI and Voltage Stress by Minimizing Inductive Parasitics*
- White Papers:
  - *An Overview of Conducted EMI Specifications for Power Supplies*
  - *An Overview of Radiated EMI Specifications for Power Supplies*
  - *Valuing Wide V_{IN}, Low EMI Synchronous Buck Circuits for Cost-driven, Demanding Applications*

12.2.1.1 PCB Layout Resources

- Application Reports:
  - *Improve High-current DC/DC Regulator Performance for Free with Optimized Power Stage Layout*
  - *AN-1149 Layout Guidelines for Switching Power Supplies*
  - *Low Radiated EMI Layout Made SIMPLE with LM4360x and LM4600x*
- Seminars:
  - *Constructing Your Power Supply – Layout Considerations*

12.2.1.2 Thermal Design Resources

- Application Reports:
  - *AN-2020 Thermal Design by Insight, Not Hindsight*
  - *AN-1520 A Guide to Board Layout for Best Thermal Resistance for Exposed Pad Packages*
  - *Semiconductor and IC Package Thermal Metrics*
  - *Thermal Design Made Simple with LM43603 and LM43602*
  - *PowerPAD™ Thermally Enhanced Package*
  - *PowerPAD Made Easy*
  - *Using New Thermal Metrics*

12.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

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12.4 サポート・リソース

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12.6 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.7 Glossary

TI Glossary This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages show mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LM5143QRWGRQ1	Active	Production	VQFNP (RWG) | 40	2500 | LARGE T&R	Yes	NIPDAUAG	Level-3-260C-168 HR	-40 to 150	LM5143 A2
LM5143QRWGRQ1.A	Active	Production	VQFNP (RWG) | 40	2500 | LARGE T&R	Yes	NIPDAUAG	Level-3-260C-168 HR	-40 to 150	LM5143 A2

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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OTHER QUALIFIED VERSIONS OF LM5143-Q1 :

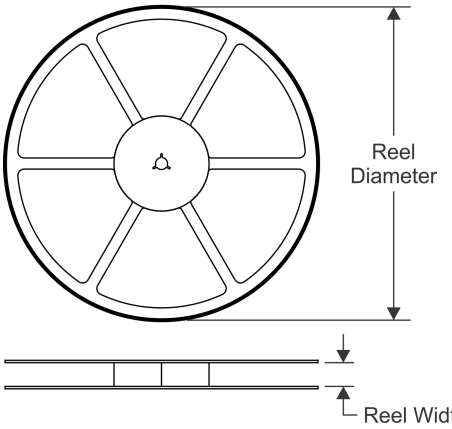
- Catalog : LM5143

NOTE: Qualified Version Definitions:

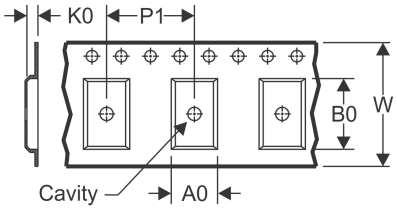
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

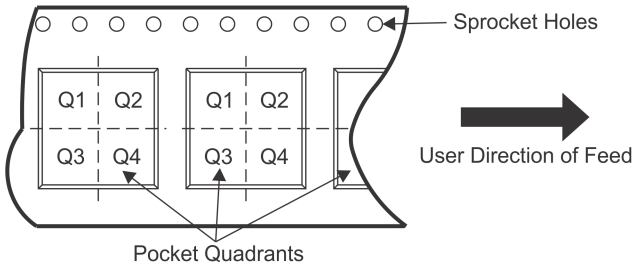


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

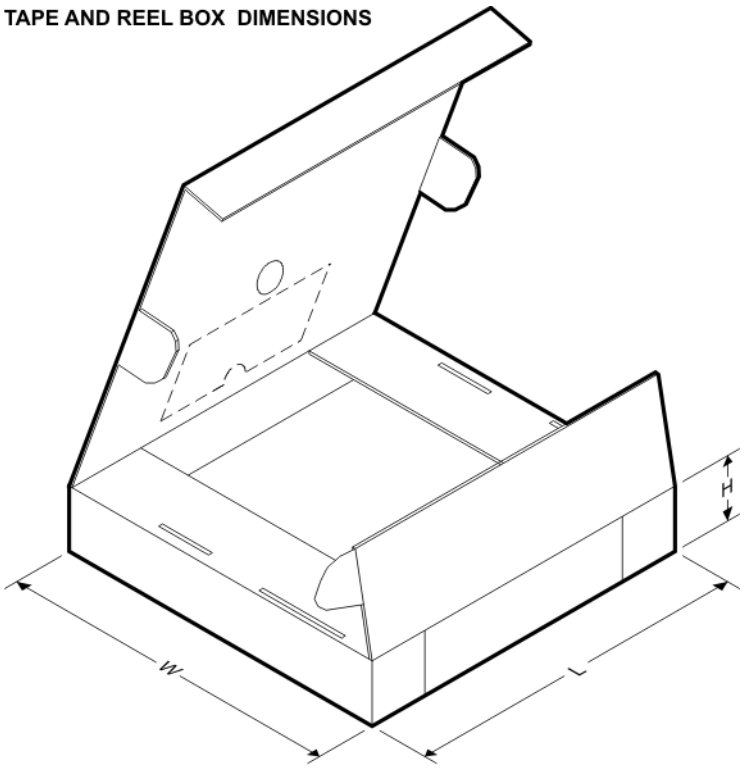
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM5143QRWGRQ1	VQFNP	RWG	40	2500	330.0	17.5	6.3	6.3	1.1	12.0	16.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

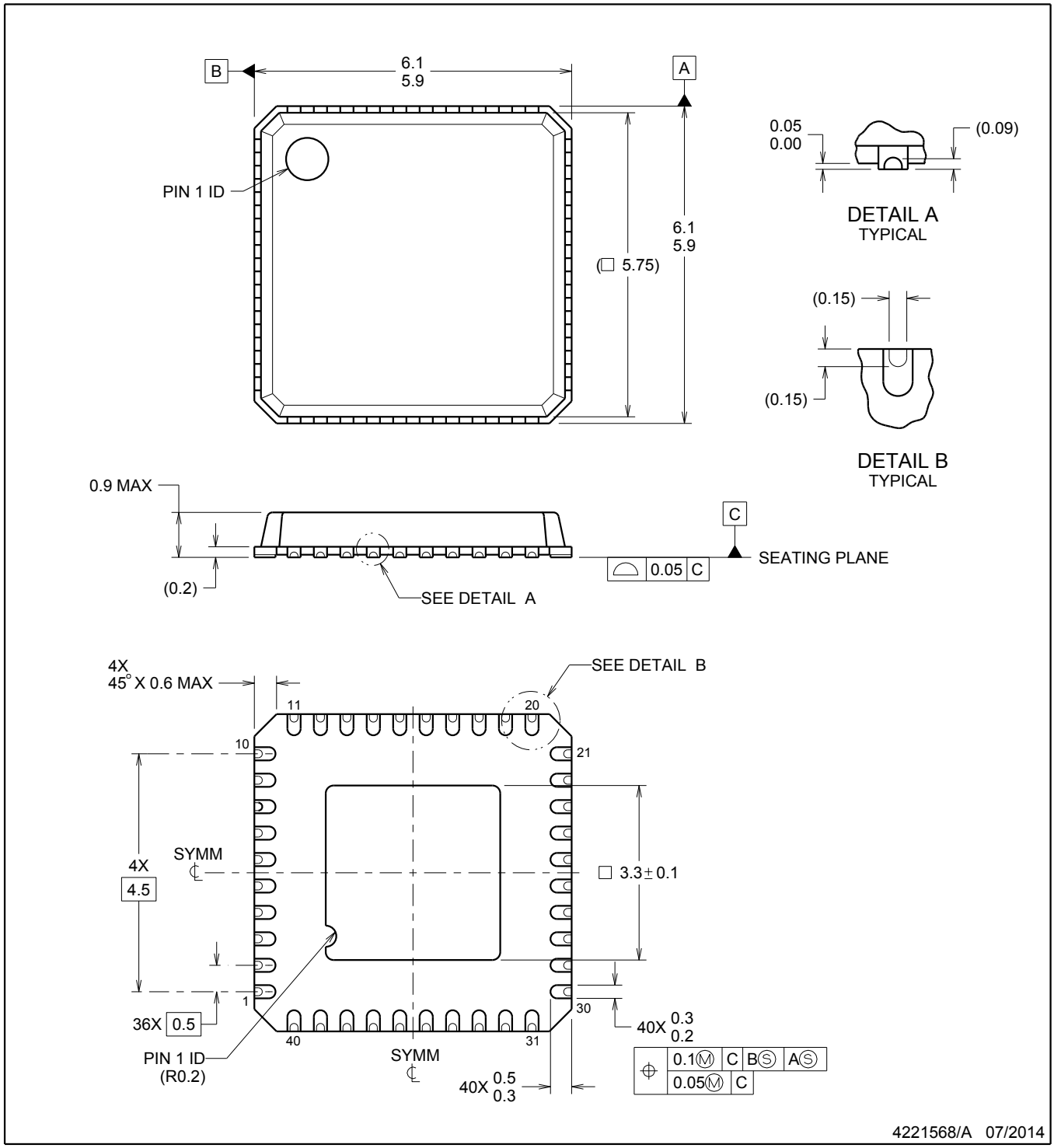
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM5143QRWGRQ1	VQFNP	RWG	40	2500	336.6	336.6	41.3

PACKAGE OUTLINE

RWG0040A

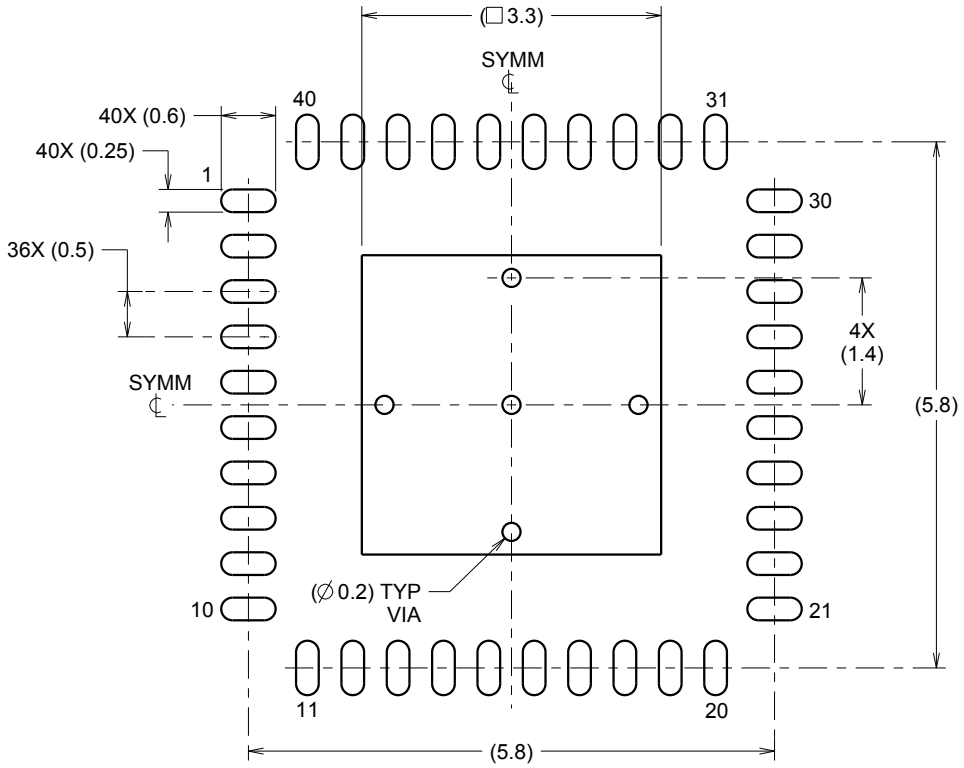
VQFN - 0.9 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

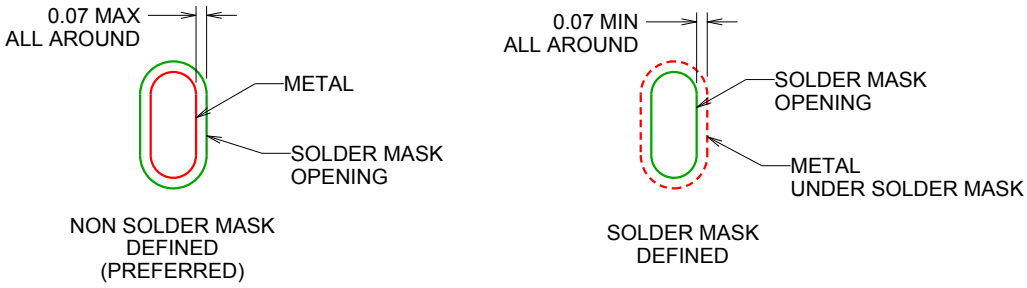


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:12X

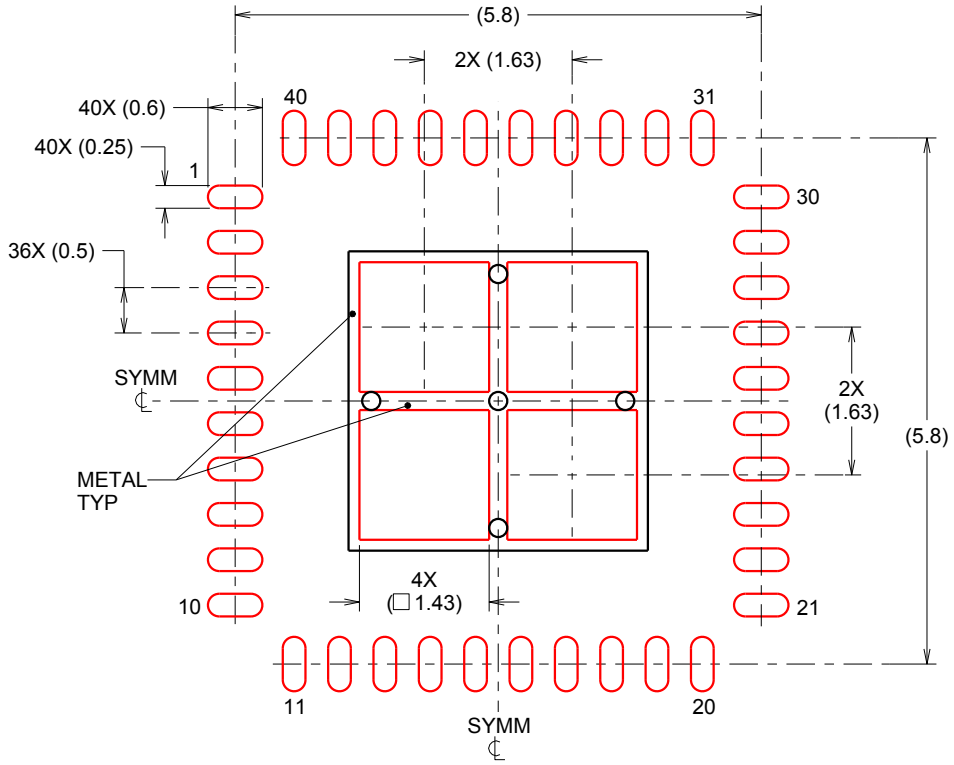


SOLDER MASK DETAILS

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NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
75% PRINTED SOLDER COVERAGE BY AREA
SCALE:12X

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NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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最終更新日：2025 年 10 月