TEXAS INSTRUMENTS
LM53625-Q1, LM53635-Q1
JAJSM35B – DECEMBER 2015 – REVISED JULY 2021

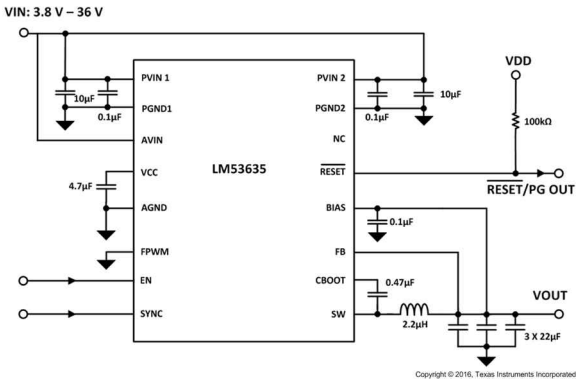
LM53625/35-Q1 2.5A/3.5A、36V 同期整流、2.1MHz、降圧 DC/DC コンバータ

1 特長

- AEC-Q100 車載認証済み:
  - デバイス温度グレード 1:–40℃～+125℃の動作時周囲温度範囲
  - デバイス HBM 分類レベル 2
  - デバイス CDM 分類レベル C6
- –40℃～+150℃の接合部温度範囲
- 15µA (標準値) の静止電流 (無負荷、3.3V 出力時)
- ウェッタブル・フランク付き / なしの 5.0mm × 4.0mm VQFN パッケージ (V_{IN} 間隔 0.6mm)
- 低 EMI およびスイッチ・ノイズ
- スペクトラム拡散オプション
- 外部周波数同期
- 内部フィルタおよび 3ms リリース・タイマ付きの $\overline{\text{RESET}}$ 出力
- 強制 PWM モードをピンにより選択可能
- 補償、ソフトスタート、電流制限、サーマル・シャットダウン、UVLO を内蔵
- 0.6V のドロップアウト (3.5A、T_A = 105℃)
- ±1% の出力電圧精度 (T_J = –40℃～125℃)
- 固定出力 (5V、3.3V)、可変出力の製品を提供

2 アプリケーション

- テレマティクス
- ヘッド・ユニット
- メーター・クラスタ
- バッテリ駆動のアプリケーション



代表的なアプリケーション回路

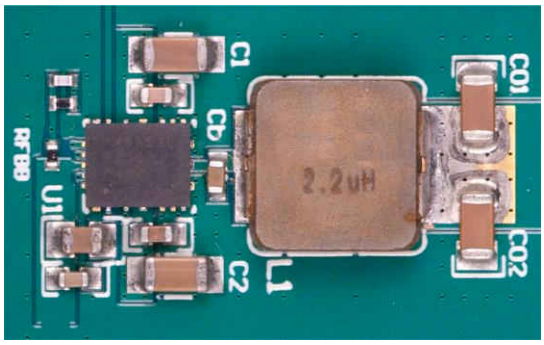
3 概要

LM53625-Q1/LM53635-Q1 同期整流式降圧レギュレータは車載用アプリケーションに最適化されており、5V、3.3V、可変出力のいずれかを出力します。高度な高速回路により、LM53625-Q1/LM53635-Q1 は 2.1MHz の固定周波数で 18V の入力から 3.3V の出力をレギュレートできます。革新的なアーキテクチャにより、このデバイスはわずか 3.55V の入力電圧から 3.3V の出力をレギュレートできます。LM53625-Q1/LM53635-Q1 のあらゆる要素は、車載用顧客と性能を重視する産業用顧客のために最適化されています。最高 36V の入力電圧と、最高 42V の過渡耐圧により、入力サージ保護の設計が簡単になります。車載認定済みのウェッタブル・フランク付き HotRod QFN パッケージは、寄生インダクタンスおよび抵抗を低減すると同時に、効率の向上、スイッチ・ノード・リンギングの最小化、電磁干渉 (EMI) の大幅な低減を実現します。フィルタリングと遅延を備えたオープン・ドレインのリセット出力により、システムの真の状態を示すことができます。この機能により、追加のスーパーバイザ部品が必要なくなるため、コストと基板面積を削減できます。PWM モードと PFM モードの間のシームレスな遷移と、小さい静止電流 (3.3V オプションでわずか 15µA) により、あらゆる負荷で高い効率と優れた過渡応答を実現します。

製品情報

型番	パッケージ(1)	本体サイズ
LM53625-Q1	VQFN-HR (22)	5.00mm × 4.00mm
LM53635-Q1		

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。



代表的な車載用のレイアウト (22mm x 12.5mm)

英語版の TI 製品についての情報を翻訳したこの資料は、製品の概要を確認する目的で便宜的に提供しているものです。該当する正式な英語版の最新情報は、www.ti.com で閲覧でき、その内容が常に優先されます。TI では翻訳の正確性および妥当性につきましては一切保証いたしません。実際の設計などの前には、必ず最新版の英語版をご参照くださいますようお願いいたします。

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4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision A (May 2016) to Revision B (July 2021)	Page
• 文書全体にわたって表、図、相互参照の採番方法を更新	1
• 「アプリケーション」を更新	1
• Added the non-wettable flank options	3

Changes from Revision * (December 2015) to Revision A (May 2016)	Page
• 製品プレビューから量産データへ	1

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5 Device Comparison

表 5-1. LM53625-Q1 Devices (2.5-A Output)

PART NUMBER	OUTPUT VOLTAGE	SPREAD SPECTRUM	PACKAGE QTY	WETTABLE FLANKS
LM53625AQRNLRQ1	Adjustable	No	3000	Y
LM53625AQRNLTQ1	Adjustable	No	250	Y
LM536253QRNLRQ1	3.3 V	No	3000	Y
LM536253QRNLTQ1	3.3 V	No	250	Y
LM536255QRNLRQ1	5 V	No	3000	Y
LM536255QRNLTQ1	5 V	No	250	Y
LM53625MQRNLRQ1	Adjustable	Yes	3000	Y
LM53625MQRNLTQ1	Adjustable	Yes	250	Y
LM53625NQRNLRQ1	3.3 V	Yes	3000	Y
LM53625NQRNLTQ1	3.3 V	Yes	250	Y
LM53625LQRNLRQ1	5 V	Yes	3000	Y
LM53625LQRNLTQ1	5 V	Yes	250	Y
LM53625NQURNLRQ1	3.3 V	Yes	3000	N
LM53625MQURNLRQ1	Adjustable	Yes	3000	N
LM53625LQURNLRQ1	5 V	Yes	3000	N

表 5-2. LM53635-Q1 Devices (3.5-A Output)

PART NUMBER	OUTPUT VOLTAGE	SPREAD SPECTRUM	PACKAGE QTY	Wettable Flanks
LM53635AQRNLRQ1	Adjustable	No	3000	Y
LM53635AQRNLTQ1	Adjustable	No	250	Y
LM536353QRNLRQ1	3.3 V	No	3000	Y
LM536353QRNLTQ1	3.3 V	No	250	Y
LM536355QRNLRQ1	5 V	No	3000	Y
LM536355QRNLTQ1	5 V	No	250	Y
LM53635MQRNLRQ1	Adjustable	Yes	3000	Y
LM53635MQRNLTQ1	Adjustable	Yes	250	Y
LM53635NQRNLRQ1	3.3 V	Yes	3000	Y
LM53635NQRNLTQ1	3.3 V	Yes	250	Y
LM53635LQRNLRQ1	5 V	Yes	3000	Y
LM53635LQRNLTQ1	5 V	Yes	250	Y
LM53635MQURNLRQ1	Adjustable	Yes	3000	N
LM53635NQURNLRQ1	3.3 V	Yes	3000	N

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6 Pin Configuration and Functions

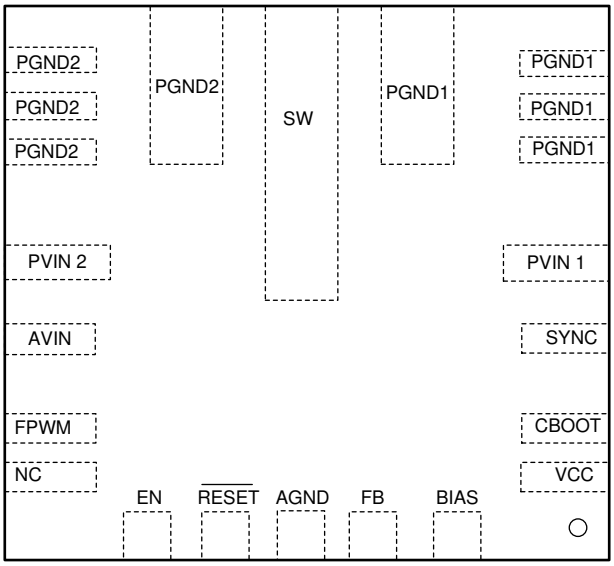


図 6-1. RNL Package 22-Pin VQFN Top View

表 6-1. Pin Functions

PIN		I/O(1)	DESCRIPTION
NO.	NAME		
1	VCC	A	Internal 3.1-V LDO output. Used as supply to internal control circuits. Connect a high-quality 4.7-µF capacitor from this pin to AGND.
2	CBOOT	P	Bootstrap capacitor connection for gate drivers. Connect a high quality 470-nF capacitor from this pin to the SW pin.
3	SYNC	I	Synchronization input to regulator. Used to synchronize the device switching frequency to a system clock. Triggers on rising edge of external clock; frequency must be in the range of 1.9 MHz and 2.3 MHz.
4	PVIN1	P	Input supply to regulator. Connect input bypass capacitors directly to this pin and PGND pins. Connect PVIN1 and PVIN2 pins directly together at PCB.
5, 6, 7, 8	PGND1	G	Power ground to internal low side MOSFET. These pins must be tied together on the PCB. Connect PGND1 and PGND2 directly together at PCB. Connect to AGND and system ground.
9	SW	P	Regulator switch node. Connect to power inductor.
10, 11, 12, 13	PGND2	G	Power ground to internal low side MOSFET. These pins must be tied together. Connect PGND1 and PGND2 directly together at PCB. Connect to AGND and system ground.
14	PVIN2	P	Input supply to regulator. Connect input bypass capacitors directly to this pin and PGND pins. Connect PVIN1 and PVIN2 pins directly together at PCB.
15	AVIN	A	Analog VIN, Connect to PVIN1 and PVIN2 on PCB.
16	FPWM	I	Do not float. Mode control input of regulator. High = FPWM, low = Automatic light load mode.
17	NC	—	No internal connection
18	EN	I	Enable input to regulator. High = on, Low = off. Can be connected to VIN. Do not float.
19	$\overline{\text{RESET}}$	O	Open drain reset output flag. Connect to suitable voltage supply through a current limiting resistor. High = regulator OK, Low = regulator fault. Goes low when EN = low.
20	AGND	G	Analog ground for regulator and system. All electrical parameters are measured with respect to this pin. Connect to PGND on PCB
21	FB	A	Feedback input to regulator. Connect to output voltage node for fixed VOUT options. Connect to feedback voltage divider for adjustable option.
22	BIAS	P	Input to auxiliary bias regulator. Connect to output voltage node.

(1) A = Analog, O = Output, I = Input, G = Ground, P = Power

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7 Specifications

7.1 Absolute Maximum Ratings

over the recommended operating junction temperature range of –40°C to +150°C (unless otherwise noted)(1)

PARAMETER	MIN	MAX	UNIT
VIN (AVIN,PVIN1 and PVIN2) to AGND, PGND1 and PGND2(2)	–0.3	40	V
SW to AGND, PGND(3)	–0.3	V_{IN} + 0.3	V
CBOOT to SW	–0.3	3.6	V
EN to AGND, PGND(2) (4)	–0.3	40	V
BIAS to AGND, PGND	–0.3	16	V
FB to AGND, PGND	–0.3	16	V
$\overline{\text{RESET}}$ to AGND, PGND	–0.3	8	V
$\overline{\text{RESET}}$ sink current(5)		10	mA
SYNC to AGND,PGND(2) (4)	–0.3	40	V
FPWM to AGND,PGND(4)	–0.3	40	V
VCC to AGND,PGND	–0.3	3.6	V
Junction temperature	–40	150	°C
Storage temperature, T_{stg}	–40	150	°C

(1) Stresses beyond those listed under *セクション 7.1* may cause permanent damage to the device. These are stress ratings only, functional operation of the device at these or any other conditions beyond those indicated under *セクション 7.3* are not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) A maximum of 42 V can be sustained at this pin for a duration of ≤ 500 ms at a duty cycle of ≤ 0.01%.
(3) A voltage of 2 V below PGND and 2 V above VIN can appear on this pin for ≤ 200 ns with a duty cycle of ≤ 0.01%.
(4) Under no conditions should the voltage on this pin be allowed to exceed the voltage on the PVIN1,PVIN2 or AVIN pins by more than 0.3 V.
(5) Do not exceed the voltage rating on this pin.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002(1)	±2500	V
		Charged-device model (CDM), per AEC Q100-011	±1000	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

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7.3 Recommended Operating Conditions

over the recommended operating junction temperature range of –40°C to +150°C (unless otherwise noted)

	MIN	NOM	MAX	UNIT
Input voltage after start-up(1)	3.9		36	V
Output voltage for 3.3-V LM53625/35-Q1(2)			3.4	V
Output voltage for 5-V LM53625/35-Q1(2)			5.2	V
Output adjustment for adjustable version of LM53625/35-Q1(2)	3.3		10	V
Load current for LM53625-Q1, fixed output option and adjustable			2.5	A
Load current for LM53635-Q1, fixed output option and adjustable			3.5	A
Junction temperature for 1000-hour lifetime	–40		125	°C
Junction temperature for 408-hour lifetime	–40		150	°C

(1) An extended input voltage range to 3.5 V is possible; see *セクション 7.6* table. See *Input UVLO* for start-up conditions.
(2) The output voltage must not be allowed to fall below zero volts during normal operation.

7.4 Thermal Information

THERMAL METRIC(1)		LM53625/35-Q1 RNL (VQFN) 22 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	29.4	°C/W
$R_{\theta JC}$	Junction-to-case (top) thermal resistance	14.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	5.4	°C/W
ψ_{JT}	Junction-to-top characterization parameter	1.2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	5.4	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	2.4	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

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7.5 Electrical Characteristics

Limits apply over the recommended operating junction temperature range of –40°C to +150°C, unless otherwise noted. Minimum and maximum limits are specified through test, design, or statistical correlation. Typical values represent the most likely parametric norm at T_j = 25°C, and are provided for reference purposes only. Unless otherwise stated the following conditions apply: V_{IN} = 13.5 V.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{FB}	Initial output voltage accuracy	V_{IN} = 3.8 V to 36 V, T_J = 25°C	–1%		1%	
		V_{IN} = 3.8 V to 36 V	–1.5%		1.5%	
I_Q	Operating quiescent current; measured at VIN pin when enabled and not switching(1)	V_{IN} = 13.5 V, V_{BIAS} = 5 V		6		µA
		V_{IN} = 13.5 V, V_{BIAS} = 5 V, T_J = 85°C			16	
I_B	Bias current into BIAS pin, enabled, not switching	V_{IN} = 13.5 V, V_{BIAS} = 5 V, FPWM = 0 V		35		µA
		V_{IN} = 13.5 V, V_{BIAS} = 3.3 V, FPWM = 0 V		35		
I_{SD}	Shutdown quiescent current; measured at VIN pin	EN ≤ 0.4 V, T_J = 25°C		2		µA
		EN ≤ 0.4 V, T_J = 85°C			3	
		EN ≤ 0.4V, T_J = 150°C			5	
$V_{IN-OPERATE}$	Minimum input voltage to operate	Rising	3.2	3.55	3.95	V
		Falling	2.95	3.25	3.55	
		Hysteresis	0.28	0.3	0.4	
V_{RESET}	$\overline{RESET}$ upper threshold voltage	Rising, % of V_{OUT}	105%	107%	110%	
	$\overline{RESET}$ lower threshold voltage	Falling, % V_{OUT}	92%	94%	96.5%	
	Magnitude of $\overline{RESET}$ lower threshold from steady state output voltage	Steady-state output voltage and $\overline{RESET}$ threshold read at the same T_J and V_{IN}			96%	
V_{RESET_HYST}	$\overline{RESET}$ hysteresis as a percent of output voltage setpoint			±1		
V_{RESET_VALID}	Minimum input voltage for proper $\overline{RESET}$ function	50-µA pullup to $\overline{RESET}$ pin, EN = 0 V, T_J= 25°C			1.5	V
V_{OL}	Low level $\overline{RESET}$ function output voltage	50-µA pullup to $\overline{RESET}$ pin, V_{IN} =1.5 V, EN = 0 V			0.4	V
		0.5-mA pullup to $\overline{RESET}$ pin, V_{IN} =13.5 V, EN=0 V			0.4	
		1-mA pullup to $\overline{RESET}$ pin, V_{IN} =13.5 V, EN=3.3 V			0.4	
F_{SW}	Switching frequency	V_{IN} = 13.5 V, center frequency with spread spectrum, PWM operation	1.85	2.1	2.35	MHz
		V_{IN} = 13.5 V, without spread spectrum, PWM operation	1.85	2.1	2.35	
F_{SYNC}	Sync frequency range		1.9	2.1	2.3	MHz
D_{SYNC}	Sync input duty cycle range	High state input < 5.5 V and > 2.3 V	25%		75%	
V_{FPWM}	FPWM input threshold voltage	FPWM input high (MODE = FPWM)	1.5			V
		FPWM input low (MODE = AUTO with diode emulation)			0.4	
		FPWM input hysteresis	0.15		1	
FS_{SS}	Frequency span of spread spectrum operation			±3%		
F_{PSS}	Spread-spectrum pattern frequency(2)				9	Hz
F_{SW-SS}	Switching Frequency while in spread spectrum	V_{IN} = 13.5 V, PWM operation	1.81			MHz

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Limits apply over the recommended operating junction temperature range of –40°C to +150°C, unless otherwise noted. Minimum and maximum limits are specified through test, design, or statistical correlation. Typical values represent the most likely parametric norm at T_j = 25°C, and are provided for reference purposes only. Unless otherwise stated the following conditions apply: V_{IN} = 13.5 V.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{FPWM}	FPWM leakage current	V_{IN} = 13.5 V, V_{FPWM} = 3.3 V		1		µA
		V_{IN} = V_{FPWM} = 13.5 V		5		
I_{SYNC}	SYNC leakage current	V_{IN} = 13.5 V, V_{SYNC} = 3.3 V		1		µA
		V_{IN} = V_{SYNC} = 13.5 V		5		
I_{L-HS}	High-side switch current limit	LM53625	3.5	5	6.5	A
		LM53635	4.5	6	7.5	
I_{L-LS}	Low-side switch current limit	LM53625	2.5	3.5	4.1	A
		LM53635	3.5	4.5	5.1	
I_{L-ZC}	Zero-cross current limit FPWM = low			–0.02		A
I_{L-NEG}	Negative current limit FPWM = high			–1.5		
R_{DSON}	Power switch on-resistance	High-side MOSFET R_{DSON}, V_{IN} = 13 V, IL=1A		60	130	mΩ
		Low-side MOSFET R_{DSON}, V_{IN} = 13 V, IL=1A		40	80	
V_{EN}	Enable input threshold voltage - rising	Enable rising	1.7		2	V
V_{EN_HYST}	Enable threshold hysteresis		0.45		0.55	V
V_{EN_WAKE}	Enable wake-up threshold		0.4			V
I_{EN}	EN pin input current	V_{IN} = V_{EN} = 13.5 V		2	5	µA
V_{CC}	Internal V_{CC} voltage	V_{IN} 13.5 V, V_{BIAS} = 0 V		3.05		V
		V_{IN} = 13.5 V, V_{BIAS} = 3.3 V		3.15		
V_{CC_UVLO}	Internal V_{CC} input undervoltage lockout	V_{IN} rising		2.7		V
		Hysteresis below $V_{CC-UVLO}$		185		mV
I_{FB}	Input current from FB to AGND	Adjustable LM53625/35-Q1, FB=1 V		20		nA
V_{REF}	Reference voltage for adjustable option only	T_J = 25°C	0.993	1	1.007	V
		T_J = –40°C to 125°C	0.99	1	1.01	
		T_J = –40°C to 150°C	0.985	1	1.015	
R_{RESET}	R_{DSON} of $\overline{RESET}$output	Pull FB pin low. Sink 1-mA at RESET pin		50	85	Ω
V_{SYNC}	V_{IH}		1.5			V
	V_{IL}				0.4	
	V_{HYST}		0.15		1	
T_{SD}	Thermal shutdown thresholds(2)	Rising	155		175	°C
		Hysteresis		15		
D_{MAX}	Maximum switch duty cycle	F_{sw} = 2.1 MHz		80%		
		While in dropout(2)	98%			

(1) This is the current used by the device while not switching, open loop on the ATE. It does not represent the total input current from the regulator system.
(2) Ensured by Design, Not tested at production.

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7.6 System Characteristics

The following specifications are ensured by design provided that the component values in the typical application circuit are used. These parameters are not ensured by production testing. Limits apply over the recommended operating junction temperature range of –40°C to +150°C, unless otherwise noted. Minimum and maximum limits are specified through test, design, or statistical correlation. Typical values represent the most likely parametric norm at T_J = 25°C, and are provided for reference purposes only. Unless otherwise stated the following conditions apply: V_{IN} = 13.5 V.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IN-MIN}	Minimum input voltage for full functionality at 1.5 A load, after start-up.	V_{OUT} = 3.3 V +2/–3% regulation		3.5		V
	Minimum input voltage for full functionality at maximum rated load 3.5 A after start-up.	V_{OUT} = 3.3 V +2/–3% regulation		3.9		
V_{OUT}	Output voltage for 5-V option	V_{IN} = 5.6 V to 36 V, I_{OUT} = 3.5 A	4.925	5	5.08	V
	Output voltage for 3.3-V option	V_{IN} 3.9 V to 36 V, I_{OUT} = 3.5 A	3.24	3.3	3.35	
	Output voltage for 5-V option	V_{IN} = 5.5 V to 36 V, I_{OUT} = 100 µA to 100 mA	4.92	5.05	5.125	
	Output voltage for 3.3-V option	V_{IN} = 3.8 V to 36 V, I_{OUT} = 100 µA to 100 mA	3.24	3.33	3.38	
	Output voltage for adjustable option	V_{IN} = V_{OUT} + 1 V to 36 V, I_{OUT} = 3.5 A	–2.25%		2.25%	
I_{Q-VIN}	Input current to VIN pin	V_{IN}= 13.5 V, V_{OUT} = 3.3 V, I_{OUT} = 0 A FPWM = 0		15	40	µA
		V_{IN} = 13.5 V, V_{OUT} = 5.0 V and I_{OUT} = 0 A FPWM = 0		20		
V_{DROP1}	Minimum input to output voltage differential to maintain regulation accuracy without inductor DCR drop	V_{OUT} = 3.3 V/5 V, I_{OUT}= 3.5 A, +2/–3% output accuracy		0.35	0.6	V
V_{DROP2}	Minimum input to output voltage differential to maintain F_{SW} ≥ 1.85 MHz without inductor DCR drop	V_{OUT} = 3.3 V/5 V, I_{OUT}=3.5 A, F_{SW} = 1.85 MHz, 2% regulation accuracy		1.1	1.4	V
Efficiency	Typical Efficiency without inductor loss	V_{IN} = 13.5 V, V_{OUT}= 5.0 V, I_{OUT} = 3.5 A		90%		
		V_{IN} = 13.5 V, V_{OUT} = 3.3 V, I_{OUT} = 3.5 A		84%		
		V_{IN} = 13.5 V, V_{OUT} = 5 V, I_{OUT} = 100 mA		88%		

7.7 Timing Characteristics

Limits apply over the recommended operating junction temperature range of –40°C to +150°C, unless otherwise noted. Minimum and maximum limits are ensured through test, design or statistical correlation. Typical values represent the most likely parametric norm at T_J = 25°C, and are provided for reference purposes only. Unless otherwise stated the following conditions apply: V_{IN} = 13.5 V.

		MIN	NOM	MAX	UNIT
t_{ON}	Minimum switch on time, V_{IN} = 18 V, I_L=1 A		65	84	ns
t_{OFF}	Minimum switch off time, V_{IN} = 3.8 V, I_L=1 A		60	80	ns
$t_{RESET-act}$	Delay time to $\overline{RESET}$ high signal	2	3	4	ms
$t_{RESET-filter}$	Glitch filter time for $\overline{RESET}$ function(1)	12	25	45	µs
t_{SS}	Soft-Start Time from first switching pulse to V_{REF} at 90%	2	3.2	5	ms
t_{EN}	Turn-on delay, C_{VCC} = 2.2 µF(2)		1		ms
t_W	Short circuit wait time (*hiccup* time)(3)		6		ms
t_{FPWM}	Change transition time from AUTO to FPWM MODE, 20-mA load, V_{IN} = 13.5 V		100		µs
	Change transition time from FPWM to AUTO MODE, 20-mA load, V_{IN} = 13.5 V		80		µs

(1) See セクション 8.
(2) This is the time from the rising edge of EN to the time that the soft-start ramp begins.

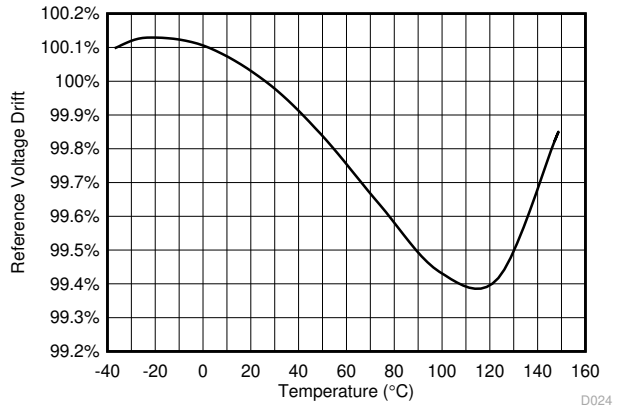
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(3) T_w is the wait time between current limit trip and re-start. T_w is nominally 4× the soft-start time. However, provision must be made to make T_w longer to ensure survivability during an output short circuit.

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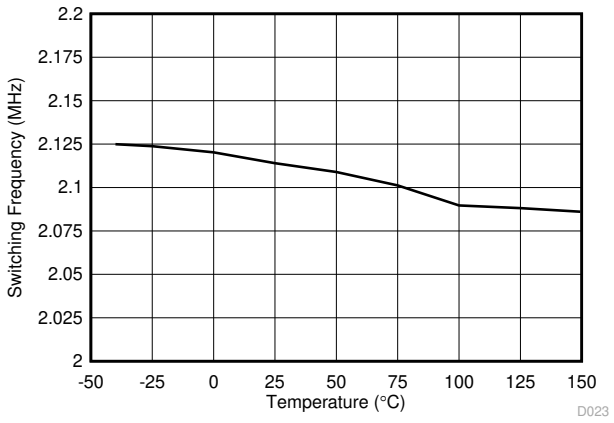
7.8 Typical Characteristics

Unless otherwise specified the following conditions apply: V_{IN} = 12 V, T_A = 25°C. Specified temperatures are ambient.



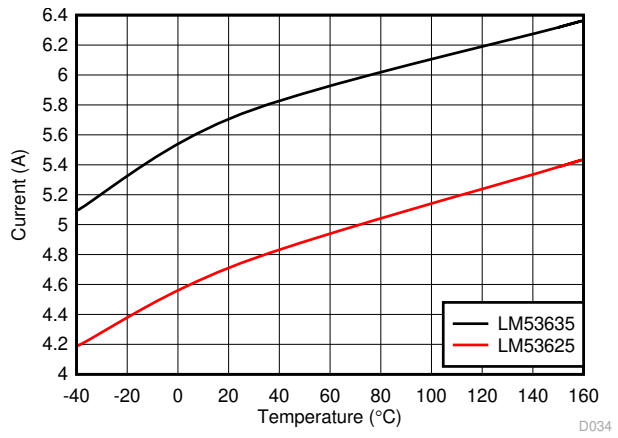
V_{IN} = 12 V

図 7-1. Reference Voltage Drift



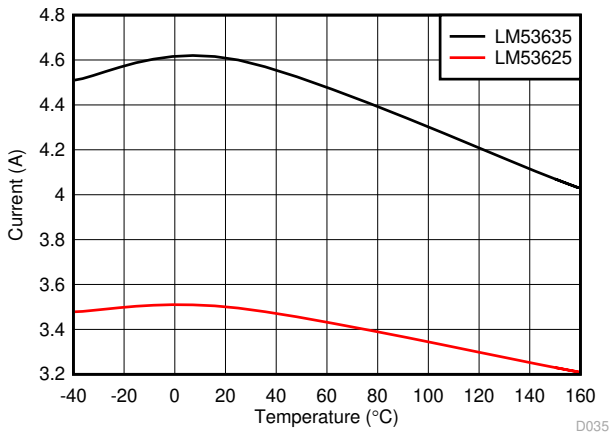
V_{IN} = 12 V

図 7-2. Switching Frequency vs Temperature



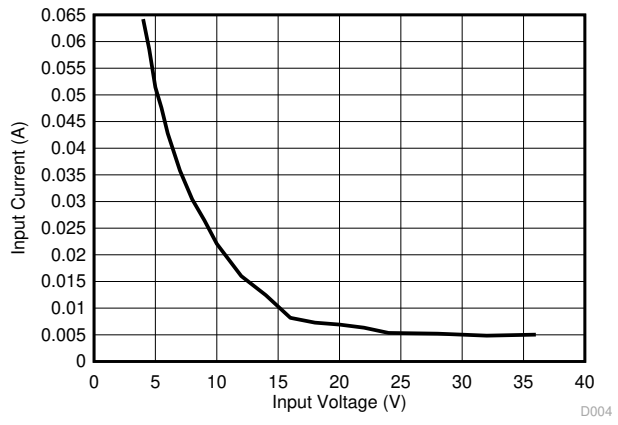
V_{IN} = 12 V

図 7-3. High Side/Peak Current Limit for LM53625/35-Q1



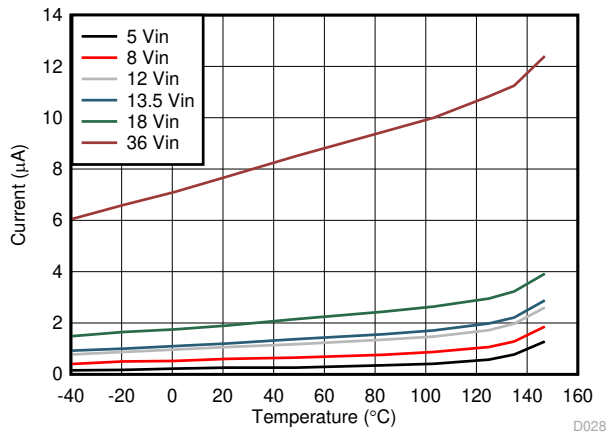
V_{IN} = 12V

図 7-4. Low Side/Valley Current Limit for LM53625/35-Q1



V_{IN} = 12 V

図 7-5. Short Circuit Average Input Current for LM53635-Q1



V_{IN} = 12 V

図 7-6. Shutdown Current

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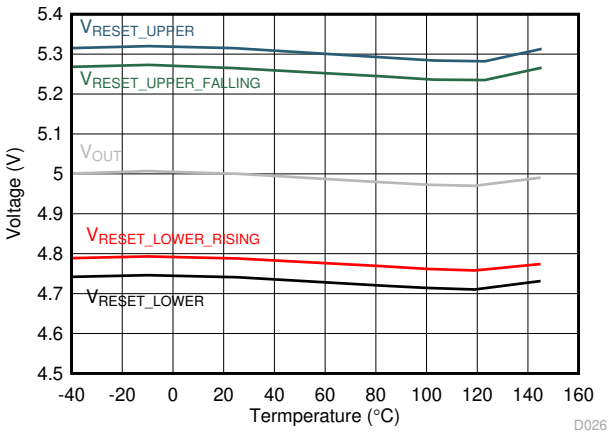


図 7-7. RESET Threshold Fixed 5-V output

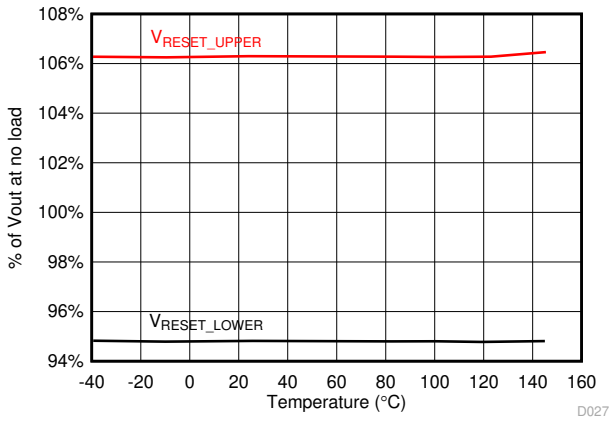


図 7-8. RESET Threshold as Percentage of Output Voltage

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8 Detailed Description

8.1 Overview

The LM53625/35-Q1 is a wide input voltage range, low quiescent current, high performance regulator with internal compensation designed specifically for the automotive market. This device is designed to minimize end-product cost and size while operating in demanding automotive environments. Normal operating frequency is 2.1 MHz allowing the use of small passive components. Because the operating frequency is above the AM band, significant saving in input filtering is also achieved. This device has a low unloaded current consumption eliminating the need for an external back-up LDO. The LM53625/35-Q1 low shutdown current and high maximum operating voltage also allows the elimination of an external load switch. To further reduce system cost, an advanced reset output is provided, which can often eliminate the use of an external reset device.

The LM53625/35-Q1 is designed with a flip-chip or HotRod technology, greatly reducing the parasitic inductance of pins. In addition, the layout of the device allows for reduction in the radiated noise generated by the switching action through partial cancellation of the current generated magnetic field.

As a result the switch-node waveform exhibits less overshoot and ringing.

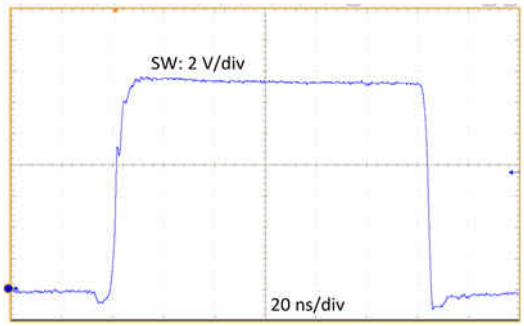


図 8-1. Switch Node Waveform (V_{IN}=13.5V, I_{OUT}=3.5A)

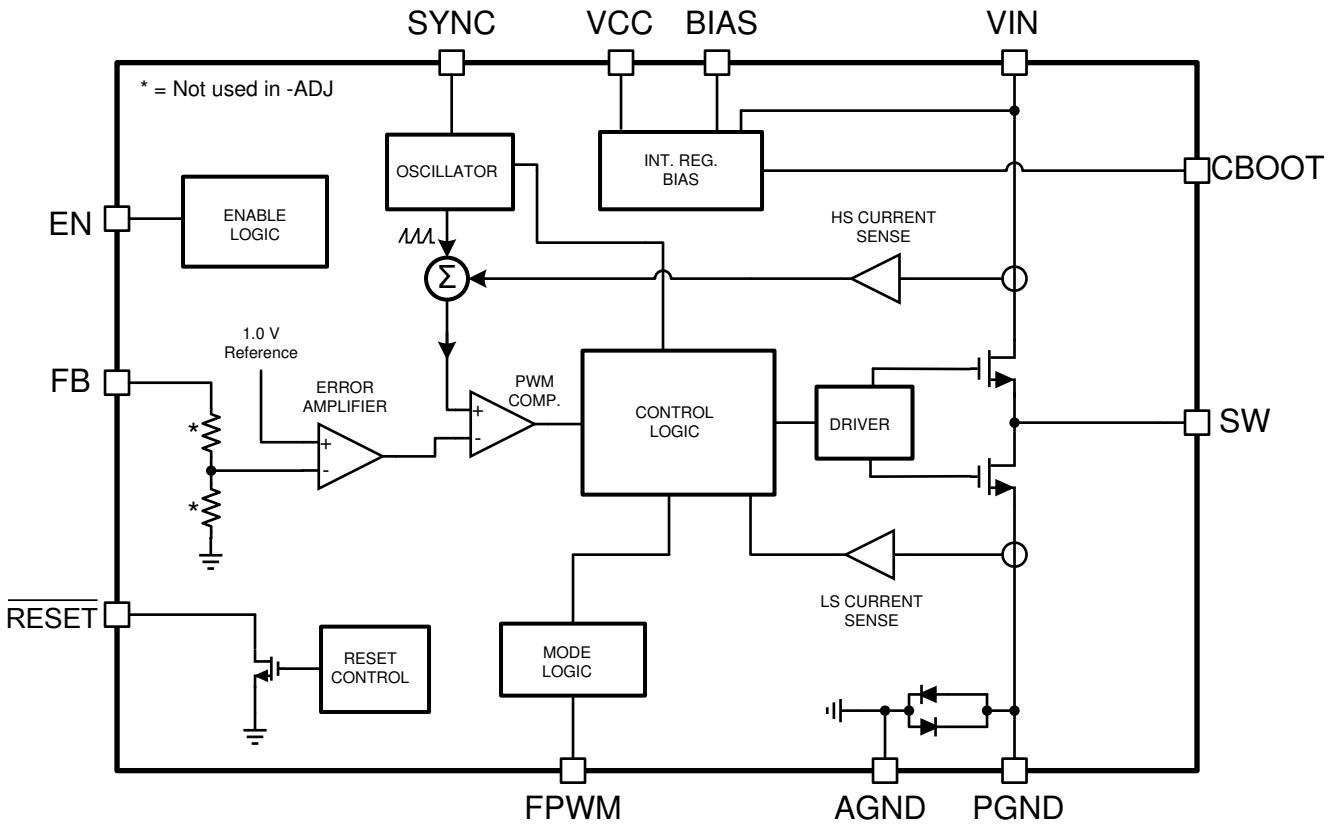
The LM53625/35-Q1 is AEC-Q1 qualified as well as having electrical characteristics ensured up to a maximum junction temperature of 150°C.

The LM53625/35-Q1 is available in VQFN package with wettable-flanks which allows easy inspection of the soldering job without the requirement of X-ray checks.

Please note that, throughout this data sheet, references to the LM53625 apply equally to the LM53635. The difference between the two devices is the maximum output current and specified MOSFET current limits.

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8.2 Functional Block Diagram



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8.2.1 Control Scheme

The LM53625/35-Q1 control scheme allows this device to operate under a wide range of conditions with a low number of external components. Peak current mode control allows a wide range of input voltages and output capacitance values, while maintaining a constant switching frequency. Stable operation is maintained while output capacitance is changed during operation as well. This allows use in systems that require high performance during load transients and which have load switches that remove loads as system operating state changes. Short minimum on and off times ensure constant frequency regulation over a wide range of conversion ratios. These on and off times allow for a duty factor window of 13% to 87% at 2.1-MHz switching frequency.

This architecture uses frequency spreading in order to achieve low dropout voltage maintaining output regulation as the input voltage falls close to output voltage. The frequency spreading is smooth and continuous, and activated as off time approaches its minimum. Under these conditions, the LM53625/35-Q1 operates much like a constant off-time converter allowing the maximum duty cycle to reach 98% and output voltage regulation with 300-mV dropout at 3.5 A.

While input voltage is high enough to require duty factor below 13%, frequency is reduced smoothly to allow lower duty factors. In this mode many of the beneficial properties of current-mode control such as insensitivity to output capacitance is maintained. The LM53625/35-Q1 has short enough minimum on time to maintain 2.1-MHz operation while converting a 18 V input to a 3.3-V output.

As load current is reduced, the LM53625/35-Q1 transitions to light load mode. In this mode, diode emulation is used to reduce RMS inductor current and switching frequency is reduced. Also, fixed voltage versions do not need a voltage divider connected to FB saving additional power. As a result, only 15 µA (typical, while converting 13.5 V to 3.3 V) is consumed to regulate output voltage if output is unloaded. Average output voltage increases slightly while lightly loaded as well.

For applications that require constant operating frequency regardless of the load condition, the FPWM pin allows the user to disable the light load operating mode. The device then switches at 2.1 MHz regardless of the output current. Diode emulation is also turned off when the FPWM pin is set high.

8.3 Feature Description

8.3.1 $\overline{\text{RESET}}$ Flag Output

The $\overline{\text{RESET}}$ function, built into the LM53625/35-Q1, has special features not found in the ordinary Power-Good function. A glitch filter prevents false flag operation for short excursions in the output voltage, such as during line and load transients. Furthermore, there is a delay between the point at which the output voltage is within specified limits and the flag asserts Power Good. Because the $\overline{\text{RESET}}$ comparator and the regulation loop share the same reference, the thresholds track with the output voltage. This allows the LM53625/35-Q1 to be specified with a 96.5% maximum threshold, while at the same time specifying a 94 % worst case threshold with respect to the actual output voltage for that device. This allows tighter tolerance than is possible with an external supervisor device. The net result is a more accurate Power-Good function while expanding the system allowance for transients, and so forth. $\overline{\text{RESET}}$ operation can best be understood by reference to 図 8-2 and 図 8-3. The values for the various filter and delay times can be found in *セクション 7.7*. Output voltage excursions lasting less than $T_{RESET\text{-}filter}$ do not trip $\overline{\text{RESET}}$. Once the output voltage is within the prescribed limits, a delay of $T_{RESET\text{-}act}$ is imposed before $\overline{\text{RESET}}$ goes high.

This output consists of an open-drain NMOS; requiring an external pullup resistor to a suitable logic supply. It can also be pulled up to either V_{CC} or V_{OUT}, through an appropriate resistor, as desired. The pin can be left floating or grounded if the $\overline{\text{RESET}}$ function is not used in the application. When EN is pulled low, the flag output isl also be forced low. With EN low, $\overline{\text{RESET}}$ remains valid as long as the input voltage is ≥ 1.5 V. The maximum current into this pin should be limited to 10 mA, while the maximum voltage must be less than 8 V.

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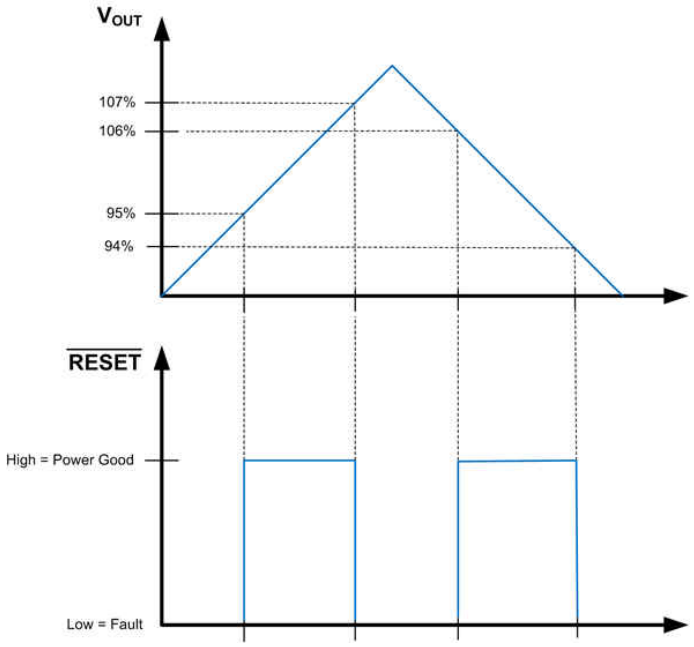


図 8-2. Static $\overline{\text{RESET}}$ Operation

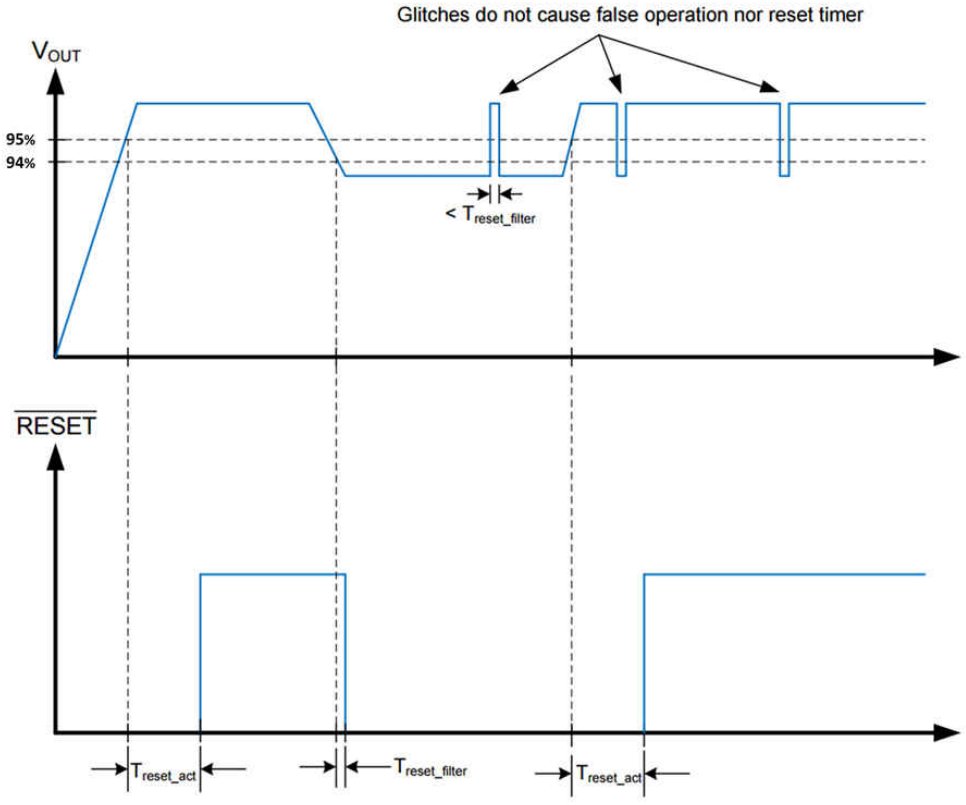


図 8-3. RESET Timing Behavior

While the LM53625/35-Q1 reset function resembles a standard Power-Good function, its functionality is designed to replace a discrete reset device, reducing additional component cost. There are three major differences between the reset function and the normal power good function seen in most regulators.

- A delay has been added for release of reset. See 図 8-2 and 図 8-3 for more detail.

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- $\overline{\text{RESET}}$ Output signals a fault (pulls its output to ground) while the part is disabled.
- $\overline{\text{RESET}}$ Continues to operate with input voltage as low as 1.5 V. Below this input voltage, $\overline{\text{RESET}}$ Output may be high impedance.

The threshold voltage for the $\overline{\text{RESET}}$ function is specified taking advantage of the availability of the LM53625/35-Q1 internal feedback threshold to the $\overline{\text{RESET}}$ circuit. This allows a maximum threshold of 96.5% of selected output voltage to be specified at the same time as 96 % of actual set point. The net result is a more accurate reset function while expanding the system allowance for transient response without the need for extremely accurate internal circuitry.

8.3.2 Enable and Start-Up

Start-up and shutdown of the LM53625/35-Q1 are controlled by the EN input. Applying a voltage of ≥ 2 V activates the device, while a voltage of ≤ 0.8 V is required to shut it down. The EN input may also be connected directly to the input voltage supply. This input must not be left floating. The LM53625/35-Q1 utilizes a reference-based soft start that prevents output voltage overshoots and large inrush currents as the regulator is starting up. A typical start-up waveform is shown in 図 8-4 along with timing definitions.

The waveforms shown in 図 8-4 indicate the sequence and timing between the enable input and the output voltage and $\overline{\text{RESET}}$. From the figure we can define several different start-up times depending on what is relevant to the application. 表 8-1 lists some definitions and typical values for the timings.

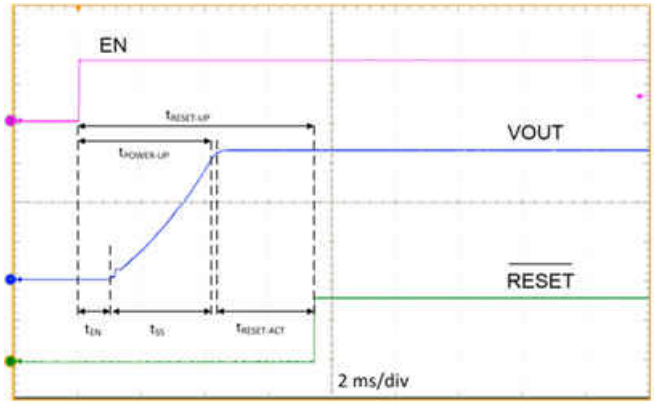


図 8-4. Typical Start-up Waveform

表 8-1. Typical Start-up Times

PARAMETER		DEFINITION	VALUE	UNIT
$t_{RESET-READY}$	Total start-up sequence time	Time from EN to $\overline{\text{RESET}}$ released	7.5	ms
$t_{POWER-UP}$	Start-up time	Time from EN to 90% of V_{OUT}	4	ms
t_{SS}	Soft-start time	Rise time of V_{OUT} from 10% to 90%	3.2	ms
t_{EN}	Delay time	Time from EN to start of V_{OUT} rising	1	ms
$t_{RESET-ACT}$	$\overline{\text{RESET}}$ time	Time from output voltage within 94% and $\overline{\text{RESET}}$ released	3	ms

8.3.3 Soft-Start Function

Soft-start time is fixed internally at about 3 ms. Soft start is achieved by ramping the internal reference. The LM53625/35-Q1 operates correctly even if there is a voltage present on the output before activation of the LM53625/35-Q1 (pre-biased start-up). The device operates in AUTO mode during soft start, and the state of the FPWM pin is ignored during that period.

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8.3.4 Current Limit

The LM53625/35-Q1 incorporates valley current limit for normal overloads and for short-circuit protection. In addition, the low-side switch is also protected from excessive negative current when the device is in FPWM mode. Finally, a high-side peak-current limit is employed for protection of the top NMOS FET.

During overloads the low-side current limit, $I_{L\text{-}LS}$ (see *セクション 7.5*), determines the maximum load current that the LM53625/35-Q1 can supply. When the low-side switch turns on, the inductor current begins to ramp down. If the current does not fall below $I_{L\text{-}LS}$ before the next turnon cycle, then that cycle is skipped, and the low-side FET is left on until the current falls below $I_{L\text{-}LS}$. This is somewhat different than the more typical peak current limit, and results in 式 1 for the maximum load current.

$$I_{OUT}\big|_{max} = I_{LS} + \frac{(V_{IN} - V_{OUT})}{2 \cdot F_S \cdot L} \cdot \frac{V_{OUT}}{V_{IN}} \quad (1)$$

The LM53625/35-Q1 uses two current limits, which allow use of smaller inductors than systems utilizing a single current limit. A coarse high side or peak current limit is provided to protect against faults and saturated inductors. A precision valley current limit prevents excessive average output current from the buck converter of the LM53625/35-Q1. A new switching cycle is not initiated until inductor current drops below the valley current limit. This scheme allows use of inductors with saturation current rated less than twice the rated operating current of the LM53625/35-Q1.

If the converter keeps triggering valley current limit for more than about 64 clock cycles, the device turns off both high and low side switches for approximately 5.5 ms (see T_W in *セクション 7.7*. If the overload is still present after the hiccup time, another 64 cycles is counted, and the process is repeated. If the current limit is not tripped for two consecutive clock cycles, the counter is reset. 図 8-5 shows the inductor current with a hard short on the output. The hiccup time allows the inductor current to fall to zero, resetting the inductor volt-second balance. This is the method used for short-circuit protection and keeps the power dissipation low during a fault. Of course the output current is greatly reduced in this condition (see *セクション 7.8*. A typical short-circuit transient and recovery is shown in 図 8-6.

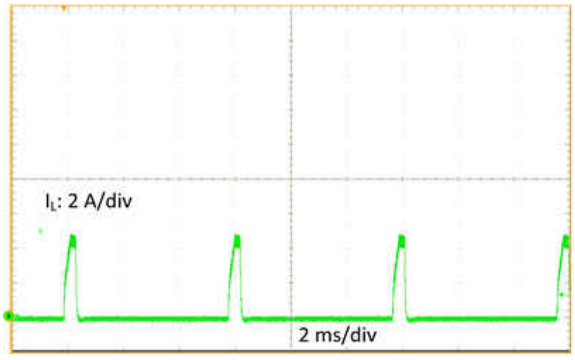


図 8-5. Inductor Current Bursts in Short Circuit

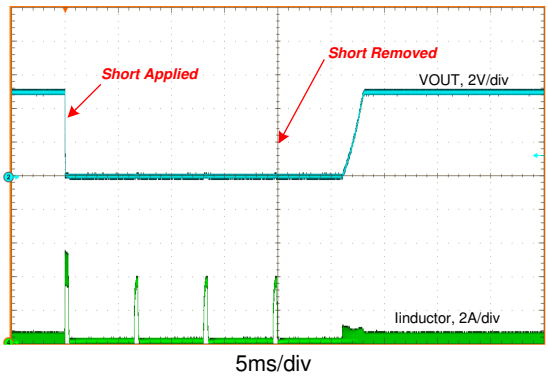


図 8-6. Short-Circuit Transient and Recovery

The high-side current limit trips when the peak inductor current reaches $I_{L\text{-}HS}$ (see *セクション 7.5*). This is a cycle-by-cycle current limit and does not produce any frequency or current foldback. It is meant to protect the high-side MOSFET from excessive current. Under some conditions, such as high input voltage, this current limit may trip before the low-side protection. The peak value of this current limit varies with duty cycle.

In FPWM mode, the inductor current is allowed to go negative. Should this current exceed I_{NEG}, the low side switch is turned off until the next clock cycle. This is used to protect the low-side switch from excessive negative current. When the device is in AUTO mode, the negative current limit is increased to about I_{ZC} (about 0 A). This allows the device to operate in DCM.

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The LM53625/35-Q1 response to a short circuit is: Peak current limit prevents excessive peak current while valley current limit prevents excessive average inductor current. After a small number of cycles of valley current limit triggers, hiccup mode is activated.

8.3.5 Hiccup Mode

In order to prevent excessive heating and power consumption under sustained short circuit conditions, a hiccup mode is included. If an overcurrent condition is maintained, the LM53625/35-Q1 shuts off its output and waits for T_W (approximately 6 ms), after which the LM53625/35-Q1 restarts operation beginning by activating soft start.

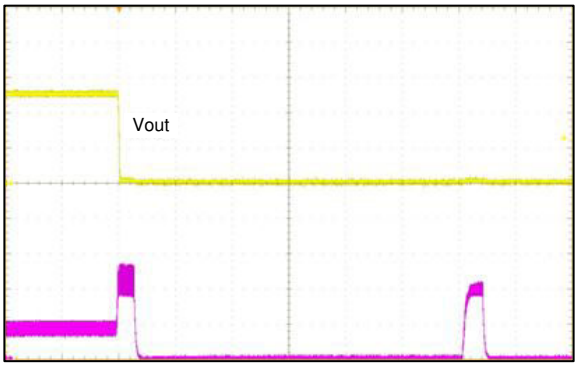


図 8-7. Hiccup Operation

During hiccup mode operation the switch node of the LM53625/35-Q1 is high impedance after a short circuit or overcurrent persists for a short duration. Periodically, the LM53625/35-Q1 attempts to restart. If the short has been removed before one of these restart attempts, the LM53625/35-Q1 operates normally.

8.3.6 Synchronizing Input

It is often desirable to synchronize the operation of multiple regulators in a single system. This technique results in better-defined EMI and can reduce the need for capacitance on some power rails. The LM53625/35-Q1 provides a SYNC input which allows synchronization with an external clock. The LM53625/35-Q1 implements an in-phase locking scheme – the rising edge of the clock signal provided to the LM53625/35-Q1 input corresponds to turning on the high-side device within the LM53625/35-Q1. This function is implemented using phase locking over a limited frequency range eliminating large glitches upon initial application of an external clock. The clock fed into the LM53625/35-Q1 replaces the internal free running clock but does not affect frequency foldback operation. Output voltage continues to be well regulated with duty factors outside of the normal 15% through 87% range though at reduced frequency.

The internal clock of the LM53625/35-Q1 can be synchronized to a system clock through the SYNC input. This input recognizes a valid high level as that ≥ 1.5 V, and a valid low as that ≤ 0.4 V. The frequency synchronization signal must be in the range of 1.9 MHz to 2.3 MHz with a duty cycle of from 10% to 90%. The internal clock is synced to the rising edge of the external clock. Ground this input if not used. The maximum voltage on this input is 5.5 V and should not be allowed to float. See *セクション 8.4* to determine which modes are valid for synchronizing the clock.

The device remains in FPWM mode and operates in CCM for light loads when synchronization input is provided.

8.3.7 Undervoltage Lockout (UVLO) and Thermal Shutdown (TSD)

The LM53625/35-Q1 incorporates an input UVLO function. The device accepts an EN command when the input voltage rises above about 3.64 V and shuts down when the input falls below about 3.3 V. See *セクション 7.5* under $V_{IN\text{-}OPERATE}$ for detailed specifications.

TSD is provided to protect the device from excessive temperature. When the junction temperature reaches about 165°C, the device shuts down; re-start occurs at a temperature of about 150°C.

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8.3.8 Input Supply Current

The LM53625/35-Q1 is designed to have very low input supply current when regulating light loads. One way this is achieved is by powering much of the internal circuitry from the output. The BIAS pin is the input to the LDO that powers the majority of the control circuits. By connecting the BIAS input to the output of the regulator, this current acts as a small load on the output. This current is reduced by the ratio of V_{OUT}/V_{IN}, just like any other load. Another advantage of the LM53625/35-Q1 is that the feedback divider is integrated into the device. This allows the use of much larger resistors than can be used externally; >> 100 kΩ. This results in much lower divider current than is possible with external resistors.

式 2 can be used as a guide to indicate how the various terms affect the input supply current in AUTO mode in unloaded conditions. The *セクション 9.2.2.3* show measured values for the input supply current for both the 3.3-V and the 5-V output voltage versions.

8.4 Device Functional Modes

Please refer to 表 8-2 and the following paragraphs for a detailed description of the functional modes for the LM53625/35-Q1. These modes are controlled by the FPWM input as shown in 表 8-2. This input can be controlled by any compatible logic, and the mode changed, while the regulator is operating. If it is desired to fix the mode for a given application, the input can be either connected to ground, a logic supply, or the VCC pin, as desired. The maximum input voltage on this pin is 5.5 V; the FPWM pin should not be allowed to float.

表 8-2. Mode Selection

FPWM INPUT VOLTAGE	OPERATING MODE
> 1.5 V	**Forced PWM**: The regulator operates as a constant frequency, current mode, full-synchronous converter for all loads; without diode emulation.
< 0.4 V	**AUTO**: The regulator moves between PFM and PWM as the load current changes, utilizing diode-emulation mode to allow DCM (see the *Glossary*).

8.4.1 AUTO Mode

In AUTO mode the device moves between PWM and PFM as the load changes. At light loads the regulator operates in PFM . At higher loads the mode changes to PWM. The load currents at which the mode changes can be found in the *セクション 9.2.2.3*.

In PWM, the converter operates as a constant frequency, current mode, full synchronous converter using PWM to regulate the output voltage. While operating in this mode the output voltage is regulated by switching at a constant frequency and modulating the duty cycle to control the power to the load. This provides excellent line and load regulation and low output voltage ripple. When in PWM the converter synchronizes to any valid clock signal on the SYNC input (see *セクション 8.4.3* and *セクション 8.4.4*).

In PFM the high side FET is turned on in a burst of one or more cycles to provide energy to the load. The frequency of these bursts is adjusted to regulate the output, while diode emulation is used to maximize efficiency (see the *Glossary*). This mode provides high light-load efficiency by reducing the amount of input supply current required to regulate the output voltage at small loads. This trades off very good light load efficiency for larger output voltage ripple and variable switching frequency. Also, a small increase in the output voltage occurs in PFM. The actual switching frequency and output voltage ripple will depend on the input voltage, output voltage, and load. Typical switching waveforms for PFM are shown in 図 8-8. See the *セクション 9.2.2.3* for output voltage variation in AUTO mode. The SYNC input is ignored during PFM operation.

A unique feature of this device is that a minimum input voltage is required for the regulator to switch from PWM to PFM at light load. This feature is a consequence of the advanced architecture employed to provide high efficiency at light loads. 図 8-9 and 図 8-10 indicates typical values of input voltage required to switch modes at no load. Also, once the regulator switches to PFM, at light load, it remains in that mode if the input voltage is reduced.

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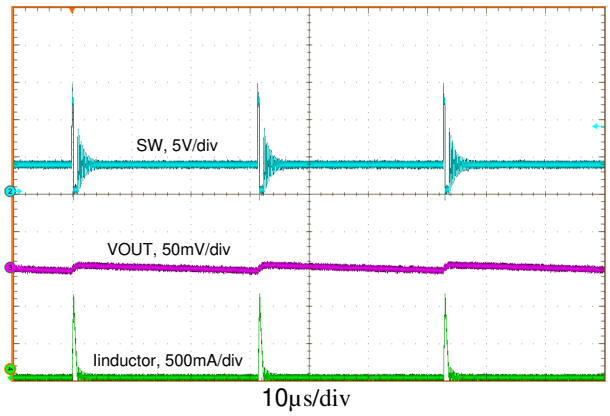


図 8-8. Typical PFM Switching Waveforms

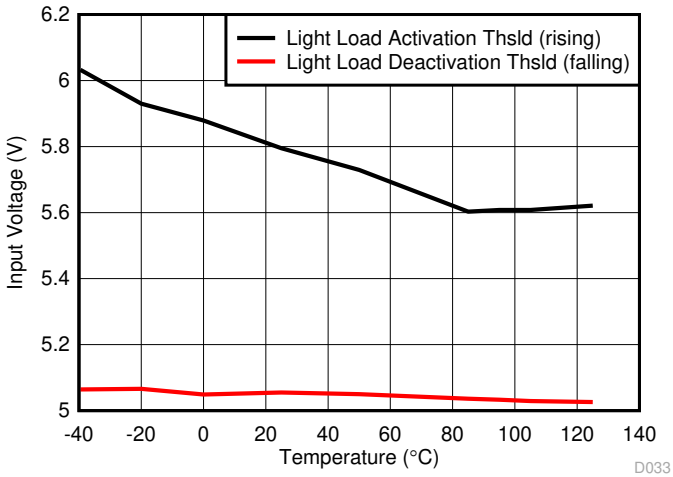


図 8-9. Input Voltage for Mode Change — Fixed 5-V Output, 2.2-µH Inductor

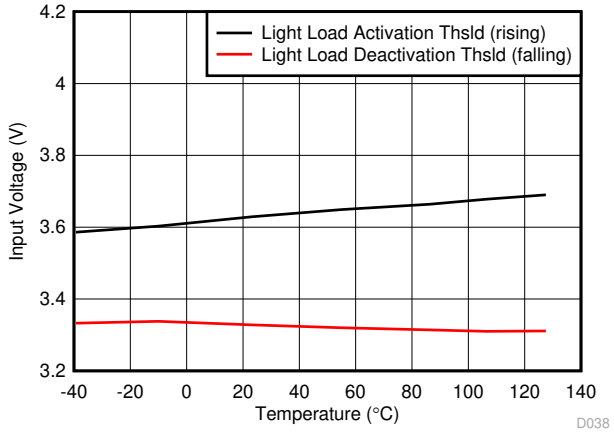


図 8-10. Input Voltage for Mode Change — Fixed 3.3-V Output, 2.2-µH Inductor

I_{Q_VIN} is the current consumed by a converter utilizing a LM53635-Q1 or LM53625-Q1 device while regulating without a load. While operating without a load, the LM53635-Q1 or LM53625-Q1 is only powering itself. The device draws power from two sources, its V_{IN} pin, I_Q, and either its FB pin for fixed versions or BIAS pin for adjustable versions, I_B. Since BIAS or FB is connected to the output of the circuit, the power consumed is converted from input power with an effective efficiency, ηeff, of approximately 80 %. Here, effective efficiency is the added input power needed when lightly loading the converter of the LM53625-Q1 and LM53635- Q1 devices and is divided by the corresponding additional load. This allows unloaded current to be calculated as follows:

$$I_{Q_VIN} = I_Q + I_{EN} + (I_B + I_{div}) \frac{\text{Output Voltage}}{\eta_{eff} \times \text{Input Voltage}} \quad (2)$$

where

- I_{Q_VIN} is the current consumed by the operating (switching) buck converter utilizing the LM53625-Q1 or LM53635-Q1 while unloaded.
- I_Q is the current drawn by the LM53625-Q1 or LM53635-Q1 from its V_{IN} terminal. See I_Q in *セクション 7.5*.
- I_{EN} is current drawn by the LM53625-Q1 or LM53635-Q1 from its EN terminal. Include this current if EN is connected to VIN. See I_{EN} in セクション 7.5. Note that this current drops to a very low value if connected to a voltage less than 5 V.
- I_B is bias/feedback current drawn by the LM53625-Q1 or LM53635-Q1 while the Buck converter utilizing it is unloaded. See I_B in *セクション 7.5*.

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- I_{div} is the current drawn by the feedback voltage divider used to set output voltage for adjustable devices. This current is zero for fixed output voltage devices.
- η_{eff} is the light load efficiency of the Buck converter with I_{Q_VIN} removed from the input current of the buck converter input current. 0.8 is a conservative value that can be used under normal operating conditions.

Note

The EN pin consumes a few micro-amperes when tied to high; see I_{EN}. Add I_{EN} to I_Q as shown in 式 2 if EN is tied to V_{IN}. If EN is tied to a voltage less than 5 V, virtually no current is consumed allowing EN to be used as an UVLO pin once a voltage divider is added.

8.4.2 FPWM Mode

With a logic high on the FPWM input, the device is locked in PWM mode. This operation is maintained, even at no-load, by allowing the inductor current to reverse its normal direction. This mode trades off reduced light load efficiency for low output voltage ripple, tight output voltage regulation, and constant switching frequency. In this mode, a negative current limit of I_{NEG} is imposed to prevent damage to the low-side FET of the regulator. When in FPWM the converter synchronizes to any valid clock signal on the SYNC input (see *セクション 8.4.3* and *セクション 8.4.4*.

When constant frequency operation is more important than light load efficiency, pull the LM53625/35-Q1 FPWM input high or provide a valid synchronization input. Once activated, this feature ensures that the switching frequency stays above the AM frequency band, while operating between the minimum and maximum duty cycle limits. Essentially, the diode emulation feature is turned off in this mode. This means that the device remains in CCM under light loads. Under conditions where the device must reduce the on time or off time below the ensured minimum, the frequency reduces to maintain the effective duty cycle required for regulation. This can occur for high input/output voltage ratios.

With the FPWM pin pulled low (*normal* mode), the diode emulation feature is activated. Device operation is the same as above; however, the regulator goes into DCM operation when the valley of the inductor current reaches zero.

This feature may be activated and deactivated while the part is regulating without removing the load. This feature activates and deactivates gradually, over approximately 40 µs, preventing perturbation of output voltage. When in FPWM mode, a limited reverse current is allowed through the inductor allowing power to pass from the regulators output to its input. In this case, care must be taken to ensure that a large enough input capacitor is used to absorb this reverse current.

Note

While FPWM is activated, larger currents pass through the inductor than in AUTO mode when lightly loaded. This may result in more EMI, though at a predictable frequency. Once loads are heavy enough to necessitate CCM operation, FPWM has no measurable effect on the operation of the regulator.

8.4.3 Dropout

One of the parameters that influences the dropout performance of a buck regulator is the minimum off time. As the input voltage is reduced, to near the output voltage, the off time of the high-side switch starts to approach the minimum value (see *セクション 7.5*). Beyond this point the switching may become erratic and/or the output voltage falls out of regulation. To avoid this problem, the LM53625/35-Q1 automatically reduces the switching frequency to increase the effective duty cycle. This results in two specifications regarding dropout voltage, as shown in セクション 7.6. One specification indicates when the switching frequency drops to 1.85 MHz; avoiding the A.M. radio band. The other specification indicates when the output voltage has fallen to 3% of nominal. See the *セクション 9.2.2.3* for typical dropout values. The overall dropout characteristic for the 5-V option can be seen in 図 8-11 and 図 8-12. The SYNC input is ignored during frequency foldback in dropout. Additional dropout information is discussed in for 5-V output (*セクション 9.2.2.3* and for 3.3 V output (*セクション 9.2.3.3*).

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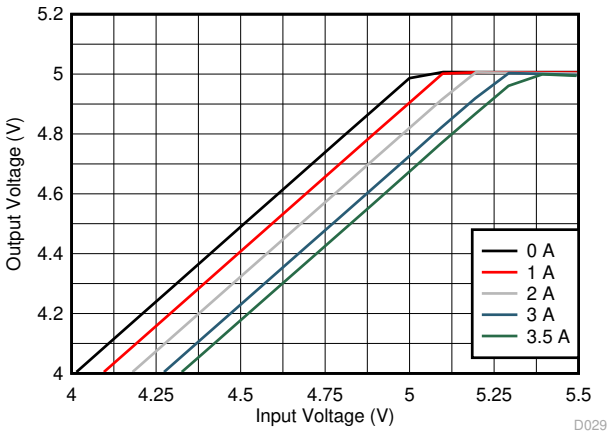


図 8-11. Overall Dropout Characteristics (V_{OUT} = 5 V)

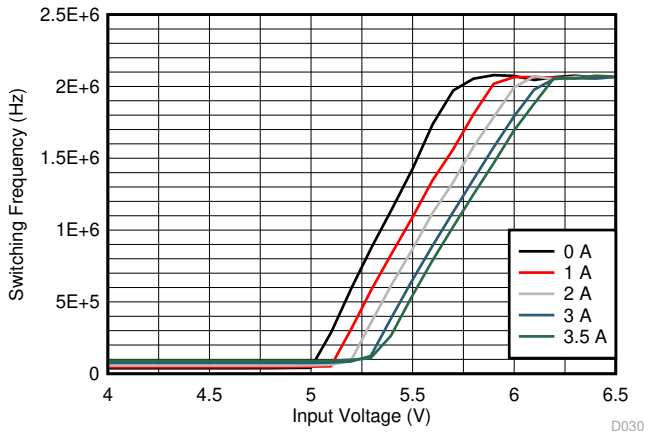


図 8-12. Frequency Dropout Characteristics (V_{OUT} = 5 V)

8.4.4 Input Voltage Frequency Foldback

At higher input voltages the on time of the high-side switch becomes small. When the minimum is reached (see *セクション 7.5*), the switching may become erratic and/or the output voltage may fall out of regulation. To avoid this behavior, the LM53625/35-Q1 automatically reduces the switching frequency at input voltages above about 20 V (see *セクション 9.2.2.3*). In this way the device avoids the minimum on-time restriction and maintains regulation at abnormally high battery voltages. The SYNC input is ignored during frequency foldback at high input voltages. Frequency foldback patterns are different for the fixed 3.3-V and the 5-V output options. The fixed 3.3-V option has a deeper foldback pattern to accommodate the lower duty cycle. The adjustable option has a fold-back patterns is similar to that of the fixed 3.3-V option.

8.5 Spread-Spectrum Operation

The spread spectrum is a factory option. In order to find which parts have spread spectrum enabled, see *セクション 5*.

The purpose of the spread spectrum is to eliminate peak emissions at specific frequencies by spreading emissions across a wider range of frequencies than a part with fixed frequency operation. In most systems containing the LM53625-Q1 and LM53635-Q1 devices, low frequency conducted emissions from the first few harmonics of the switching frequency can be easily filtered. A more difficult design criterion is reduction of emissions at higher harmonics which fall in the FM band. These harmonics often couple to the environment through electric fields around the switch node. The LM53625-Q1 and LM53635-Q1 devices use a ±3% spread of frequencies which spread energy smoothly across the FM band but is small enough to limit sub-harmonic emissions below its switching frequency. Peak emissions at the part's switching frequency are only reduced by slightly less than 1 dB, while peaks in the FM band are typically reduced by more than 6 dB.

The LM53625-Q1 and LM53635-Q1 devices use a cycle to cycle frequency hopping method based on a linear feedback shift register (LFSR). Intelligent pseudo random generator limits cycle to cycle frequency changes to limit output ripple. Pseudo random pattern repeats by approximately 8 Hz which is below the audio band.

The spread spectrum is only available while the clock of the LM53625-Q1 and LM53635-Q1 devices is free running at its natural frequency. Any of the following conditions overrides spread spectrum, turning it off:

1. An external clock is applied to the SYNC/MODE terminal.
2. The clock is slowed due to operation low input voltage – this is operation in dropout.
3. The clock is slowed due to high input voltage – input voltage above approximately 21 V disables spread spectrum.
4. The clock is slowed under light load in Auto mode – this is normally not seen above 200 mA of load. In FPWM mode, spread spectrum is active even if there is no load.

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9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

The LM53625/35-Q1 is a step-down DC-DC converter, typically used to convert a higher DC voltage to a lower DC voltage with a maximum output current of 2.5 A or 3.5 A. The following design procedures can be used to select components for the LM53625/35-Q1. Alternately, the WEBENCH® Design Tool may be used to generate a complete design. This tool utilizes an iterative design procedure and has access to a comprehensive database of components. This allows the tool to create an optimized design and allows the user to experiment with various design options.

9.2 Typical Applications

9.2.1 General Application

図 9-1 shows a general application schematic. FPWM, SYNC and EN are digital inputs. $\overline{\text{RESET}}$ is an open-drain output. FB connection is different for the fixed output options and the adjustable option.

- The FPWM pin can be connected to GND to enable light-load PFM operation. Select this option if current consumption at light load is critical. The pin can be connected to VCC or VIN for forced 2-MHz operation. Select this option if constant switching frequency is critical over the entire load range. The pin can also be driven by an external signal and can be toggled while the part is in operation (by an MCU for example.) Refer to the *セクション 7.5* and *セクション 8.4* for more details on the operation and signal requirements of the FPWM pin.
- The SYNC pin can be used to control the switching frequency and the phase of the converter. If the function is not needed, tie the SYNC pin to GND or 3 V.
- The $\overline{\text{RESET}}$ pin can be left floating if the function is not required. If the function is needed, the pin must be connected to a DC rail through a pullup resistor (100 kΩ is the typical recommended value). Check *セクション 7.5* and *セクション 8.3.1* for the details of the $\overline{\text{RESET}}$-pin function.
- If the device is a fixed-output version (3.3 V or 5 V output option), connect the FB pin directly to the output. In the case of an adjustable-output part, connect the output to the FB pin through a voltage divider. See *セクション 9.2.1.2* for details on component selection.
- The BIAS pin can be connected directly to the output except in applications that can experience inductive shorts (such as cases with long leads on the output). In those cases, a 3 Ω or so is necessary between the output and the BIAS pin, and a small capacitor to GND is necessary close to the BIAS pin (C_{BIAS}). Alternatively, a Schottky diode can be connected between the OUT and GND to limit the negative voltage that can arise on the output during inductive shorts. In addition, BIAS can also be connected to an external rail if necessary and if available. The typical current into the bias pin is 15 mA when the device is operating in PWM mode at 2.1 MHz.
- Power components must be chosen carefully for proper operation of the converter. *セクション 9.2.1.2* discusses the details of the process of choosing the input capacitors, output capacitors, and inductor for the application.

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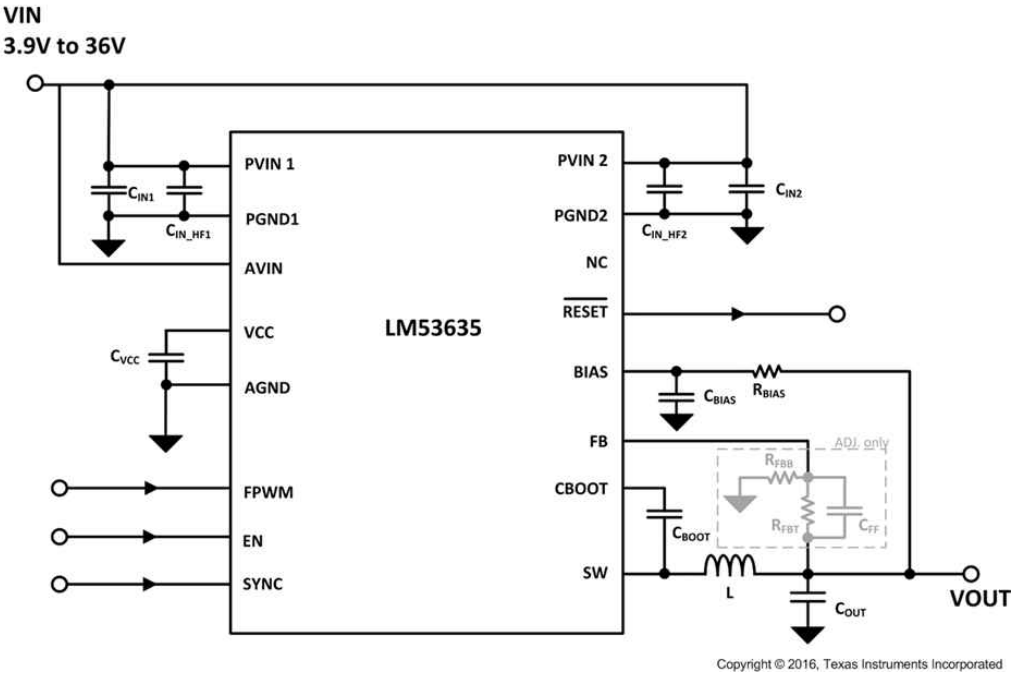


図 9-1. General Application Circuit

9.2.1.1 Design Requirements

See 表 9-4, 表 9-5, and 表 9-6. The minimum input voltage shown in 図 9-1 is not the minimum operating voltage of the LM53625-Q1/LM53635-Q1. Rather, it is a typical operating range for the systems. For the complete information regarding minimum input voltage, please refer to *セクション 7.5*

9.2.1.2 Detailed Design Procedure

9.2.1.2.1 External Components Selection

The device requires input capacitors and an output inductor-capacitor filter. These components are critical to the performance of the device.

9.2.1.2.1.1 Input Capacitors

The input capacitor supplies the AC switching current drawn from the switching action of the internal power FETs. The input current of a buck converter is discontinuous, so the ripple current supplied by the input capacitor is large. The input capacitor must be rated to handle both the RMS current and the dissipated power.

The device is designed to be used with ceramic capacitors on the input of the buck regulator. The recommended dielectric type of these capacitors is X5R, X7R, or of comparable material to maintain proper tolerances over voltage and temperature.

The device requires a minimum of 22 µF of ceramic capacitance at the input. TI recommends 2 × 10 µF, 10 µF for PVIN1 and 10 µF for PVIN2. Place these capacitors close to the PVIN1 and PGND1 / PVIN2 and PGND2 pads.

In addition, it is especially important to have small ceramic capacitors of 10 nF to 100 nF very close to the PVIN1 and PVIN2 inputs in order to minimize ringing and EMI generation due to the high speed switching of the device coupled with trace inductance.

Many times it is desirable to use an additional electrolytic capacitor on the input, in parallel with the ceramics. This is especially true if longs leads/traces are used to connect the input supply to the regulator. The moderate ESR of this capacitor can help damp any ringing on the input supply caused by long power leads. The use of this additional capacitor will also help with voltage dips caused by input supplies with unusually high impedance.

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9.2.1.2.1.1.1 Input Capacitor Selection

The ceramic input capacitors provide a low impedance source to the regulator in addition to supplying ripple current and isolating switching noise from other circuits. 表 9-1 shows the nominal and minimum values of total input capacitance recommenced for the LM53625/35-Q1. Also shown are the measured values of *effective* capacitance for the indicated capacitor. In addition, small high frequency bypass capacitors connected directly between the VIN and PGND pins are very helpful in reducing noise spikes and aid in reducing conducted EMI. TI recommends that a small case size 10-nF ceramic capacitor be placed across the input, as close to the device as possible. Additional high-frequency capacitors can be used to help manage conducted EMI or voltage spike issues that may be encountered.

表 9-1. Recommended Input Capacitors

NOMINAL INPUT CAPACITANCE		MINIMUM INPUT CAPACITANCE		PART NUMBER
RATED CAPACITANCE	MEASURED CAPACITANCE(1)	RATED CAPACITANCE	MEASURED CAPACITANCE(1)	
3 × 10 µF	22.5 µF	2 × 10 µF	15 µF	CL32B106KBJNNNE

(1) Measured at 14 V and 25°C.

9.2.1.2.1.2 Output Inductors and Capacitors Selection

There are several design considerations related to the selection of output inductors and capacitors:

- Load transient response
- Stability
- Efficiency
- Output ripple voltage
- Overcurrent ruggedness

The device has been optimized for use with nominal LC values as shown in the 図 9-1.

9.2.1.2.1.2.1 Inductor Selection

The LM53625/35-Q1 is optimized for a nominal inductance of 2.2 µH for the 5-V and 3.3-V versions. This gives a ripple current that is approximately 20% to 30% of the full load current of 3.5 A. For output voltages greater than 5 V, a proportionally larger inductor can be used, thus keeping the ratio of inductor current slope to internal compensating slope constant.

The most important inductor parameters are saturation current and parasitic resistance. Inductors with a saturation current of between 7 A and 8 A are appropriate for most applications when using the LM53625/35-Q1. Of course, the inductor parasitic resistance must be as low as possible to reduce losses at heavy loads. 表 9-2 gives a list of several possible inductors that can be used with the LM53625/35-Q1.

The LM53625 and LM53635 devices run in current mode and with internal compensation. This compensation is stable with inductance between 1.5 µH and 10 µH. For most applications, use 2.2 µH with the fixed 5-V and 3.3-V versions of the LM53625 and LM53635 devices. Adjustable devices operate at the same frequency under high input-voltage conditions as devices set to deliver 3.3 V (see 図 9-28). Inductor current ripple at high input voltages can become excessive when using a 2.2-µH inductor with an adjustable device that is delivering output voltage above 6 V. A 4.7-µH inductor might be necessary. Inductance that is too high is not recommended as it can result in poor load transient behavior and instability for extreme inductance choice. See 表 9-2 for typical recommended values.

The inductor must be rated to handle the peak load current plus the ripple current — take care when reviewing the different saturation current ratings specified by different manufacturers. Saturation current ratings are typically specified at 25°C, so ratings at maximum ambient temperature of the application should be requested from the manufacturer. For the LM53635, TI recommends a saturation current of 7.5 A or higher, and for the LM53625, a saturation current of 6.5 A or higher is recommended

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表 9-2. Recommended Inductors

MANUFACTURER	PART NUMBER	SATURATION CURRENT	DC RESISTANCE
Würth	7440650022	6 A	15 mΩ
Coilcraft	DO3316T-222MLB	7.8 A	11 mΩ
Coiltronics	MPI4040R3-2R2-R	7.9 A	48 mΩ
Vishay	IHLP2525CZER2R2M01	8 A	18 mΩ
Vishay	IHLP2525BDER2R2M01	6.5 A	28 mΩ

The designer should choose the inductors that best match the system requirements. A very wide range of inductors are available as regarding physical size, height, maximum current (thermally limited, and inductance loss limited), series resistance, maximum operating frequency, losses, and so forth. In general, inductors of smaller physical size have higher series resistance (DCR) and implicitly lower overall efficiency is achieved. Very low-profile inductors may have even higher series resistance. TI recommends finding the best compromise between system performance and cost.

9.2.1.2.1.2.2 Output Capacitor Selection

The LM53625/35-Q1 is designed to work with low-ESR ceramic capacitors. For automotive applications, TI recommends X5R and X7R type capacitors. The *effective* value of these capacitors is defined as the actual capacitance under voltage bias and temperature. All ceramic capacitors have a large voltage coefficient, in addition to normal tolerances and temperature coefficients. Under DC bias, the capacitance value drops considerably. Larger case sizes and/or higher voltage capacitors are better in this regard. To help mitigate these effects, multiple small capacitors can be used in parallel to bring the minimum *effective* capacitance up to the desired value. This can also ease the RMS current requirements on a single capacitor. 表 9-3 shows the nominal and minimum values of total output capacitance recommended for the LM53625/35-Q1. The values shown also provide a starting point for other output voltages, when using the adjustable option. Also shown are the measured values of *effective* capacitance for the indicated capacitor. More output capacitance can be used to improve transient performance and reduce output voltage ripple.

In practice, the output capacitor has the most influence on the transient response and loop phase margin. Load transient testing and Bode plots are the best way to validate any given design and should always be completed before the application goes into production. Make a careful study of temperature and bias voltage variation of any candidate ceramic capacitor in order to ensure that the minimum value of *effective* capacitance is provided. The best way to obtain an optimum design is to use the Texas Instruments WEBENCH Design Tool.

In adjustable applications the feed-forward capacitor, C_{FF}, provides another degree of freedom when stabilizing and optimizing the design. Refer to *Optimizing Transient Response of Internally Compensated dc-dc Converters With Feedforward Capacitor* (SLVA289) for helpful information when adjusting the feed-forward capacitor.

In addition to the capacitance shown in 表 9-3, a small ceramic capacitor placed on the output can help to reduce high frequency noise. Small case-size ceramic capacitors in the range of 1 nF to 100 nF can be very helpful in reducing spikes on the output caused by inductor parasitics.

Limit the maximum value of total output capacitance to between 300 µF and 400 µF. Large values of output capacitance can prevent the regulator from starting up correctly and adversely effect the loop stability. If values in the range given above, or greater, are to be used, then a careful study of start-up at full load and loop stability must be performed.

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表 9-3. Recommended Output Capacitors

OUTPUT VOLTAGE	NOMINAL OUTPUT CAPACITANCE		MINIMUM OUTPUT CAPACITANCE		PART NUMBER
	RATED CAPACITANCE	MEASURED CAPACITANCE(1)	RATED CAPACITANCE	MEASURED CAPACITANCE(1)	
3.3 V (fixed option)	3 × 22 µF	63 µF	2 × 22 µF	42 µF	C3225X7R1C226M250AC
5 V (fixed option)	3 × 22 µF	60 µF	2 × 22 µF	40 µF	C3225X7R1C226M250AC
6 V	5 × 22 µF	98 µF	3 × 22 µF	58 µF	C3225X7R1C226M250AC
10 V(2)	5 × 22 µF	80 µF	3 × 22 µF	48 µF	C3225X7R1C226M250AC

(1) Measured at indicated V_{OUT} at 25°C.
(2) L = 4.7 µH.

The output capacitor of a switching converter absorbs the AC ripple current from the inductor and provides the initial response to a load transient. The ripple voltage at the output of the converter is the product of the ripple current flowing through the output capacitor and the impedance of the capacitor. The impedance of the capacitor can be dominated by capacitive, resistive, or inductive elements within the capacitor, depending on the frequency of the ripple current. Ceramic capacitors have very low ESR and remain capacitive up to high frequencies. Their inductive component can be usually neglected at the frequency ranges the switcher operates.

The output-filter capacitor smooths out the current flow from the inductor to the load and helps maintain a steady output voltage during transient load changes. It also reduces output voltage ripple. These capacitors must be selected with sufficient capacitance and low enough ESR to perform these functions.

Consult *Output Ripple Voltage for Buck Switching Regulator* (SLVA630) for more details on the estimation of the output voltage ripple for this converter.

9.2.1.2.2 Setting the Output Voltage

For the fixed output voltage versions, the FB input is connected directly to the output voltage node. Preferably, near the top of the output capacitor. If the feedback point is located further away from the output capacitors (that is, remote sensing), then a small 100-nF capacitor may be needed at the sensing point.

9.2.1.2.2.1 FB for Adjustable Versions

The adjustable version of the LM53625-Q1 and LM53635-Q1 devices regulates output voltage to a level that results in the FB node being V_{REF}, which is approximately 1 V; see *セクション 7.5*. Output voltage given a specific feedback divider can be calculated using 式 3:

$$\text{Output Voltage} = V_{ref} \times \frac{R_{FBB} + R_{FBT}}{R_{FBB}} \tag{3}$$

See 図 9-34 for an example of the use of adjustable versions of the LM53625-Q1 and LM53635-Q1 devices. To ensure proper behavior for all modes of operation, a 50 kΩ resistor is recommended for R_{FBT}. R_{FBB} can then be determined using :

$$R_{FBB} = \frac{V_{ref} \times R_{FBT}}{\text{Output Voltage} - V_{ref}} \tag{4}$$

In addition a feed-forward capacitor C_{FF} may be required to optimize the transient response. For output voltages greater than 6 V, the WEBENCH Design Tool can be used to optimize the design.

9.2.1.2.3 VCC

The VCC pin is the output of the internal LDO used to supply the control circuits of the LM53625/35-Q1. This output requires a 4.7-µF, 10-V ceramic capacitor connected from VCC to GND for proper operation. X7R type is recommended for automotive applications. In general this output must not be loaded with any external circuitry. However, it can be used to supply a logic level to the FPWM input or for the pullup resistor used with the $\overline{\text{RESET}}$ output. The nominal output of the LDO is 3.15 V.

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9.2.1.2.4 BIAS

The BIAS pin is the input to the internal LDO. As mentioned in セクション 8.3.8, this input is connected to V_{OUT} in order to provide the lowest possible supply current at light loads. Because this input is connected directly to the output, it must be protected from negative voltage transients. Such transients may occur when the output is shorted at the end of a long PCB trace or cable. If this is likely in a given application, then place a small resistor in series between the BIAS input and V_{OUT}, as shown in 図 9-4. Size the resistor to limit the current out of the BIAS pin to < 100 mA. Values in the range of 2 Ω to 5 Ω are usually sufficient. Values greater than 5 Ω are not recommended. As a rough estimate, assume that the full negative transient will appear across R_{BIAS} and design for a current of < 100 mA. In severe cases, a Schottky diode can be placed in parallel with the output to limit the transient voltage and current.

When a resistor is used between the output and the BIAS pin, a 0.1-µF capacitor is required close to the BIAS pin. In general, TI recommends having a 0.1-µF capacitor near the BIAS pin, regardless of the presence or not of the resistor, unless the trace between the output capacitors and the BIAS pin is very short.

The typical current into the bias pin is 15 mA when the device is operating in PWM mode at 2.1 MHz.

9.2.1.2.5 CBOOT

The LM53625/35-Q1 requires a *boot-strap* capacitor between the CBOOT pin and the SW pin. This capacitor stores energy that is used to supply the gate drivers for the power MOSFETs. A ceramic capacitor of 0.47 µF, ≥ 6.3 V is required.

9.2.1.2.6 Maximum Ambient Temperature

As with any power conversion device, the LM53625/35-Q1 dissipates internal power while operating. The effect of this power dissipation is to raise the internal temperature of the converter above ambient. The internal die temperature (T_J) is a function of the ambient temperature, the power loss, and the effective thermal resistance, $R_{\theta JA}$ of the device and PCB combination. The maximum internal die temperature for the LM53625/35-Q1 is 150°C, thus establishing a limit on the maximum device power dissipation and therefore load current at high ambient temperatures. 式 5 shows the relationships between the important parameters.

$$I_{OUT} = \frac{(T_J - T_A)}{R_{\theta JA}} \cdot \frac{\eta}{(1-\eta)} \cdot \frac{1}{V_{OUT}} \tag{5}$$

The device uses an advanced package technology that utilizes the pads/pins as heat spreading paths. As a result, the pads should be connected to large copper areas in order to dissipate the heat from the IC. All pins provide some heat relief capability but the PVINs, PGNDs and SW pins are of particular importance for proper heat dissipation. Utilization of all the board layers for heat dissipation using vias as heat pipes is recommended. The Layout Guideline section includes example that shows layout for proper heat management.

9.2.1.3 Application Curves

These parameters are not tested and represent typical performance only. Unless otherwise stated, the following conditions apply: V_{IN} = 12 V, T_A = 25°C. For the purpose of offering the more information to the designer, information for the application with FPWM pin high (FPWM mode) and FPWM pin low (AUTO mode) is included, although the schematic shows the application running specifically in FPWM mode. The mode is specified under each following graph.

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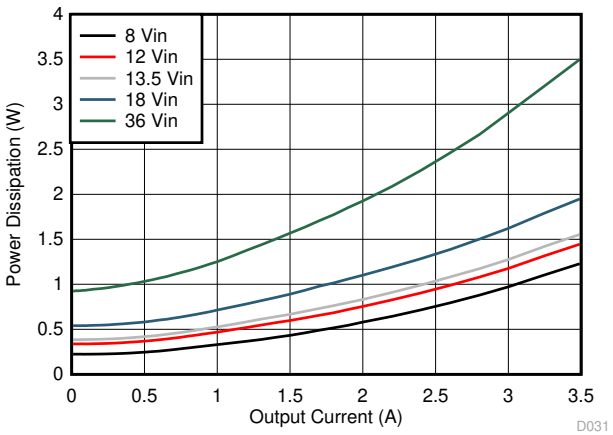


図 9-2. Power Dissipation 5-V Output

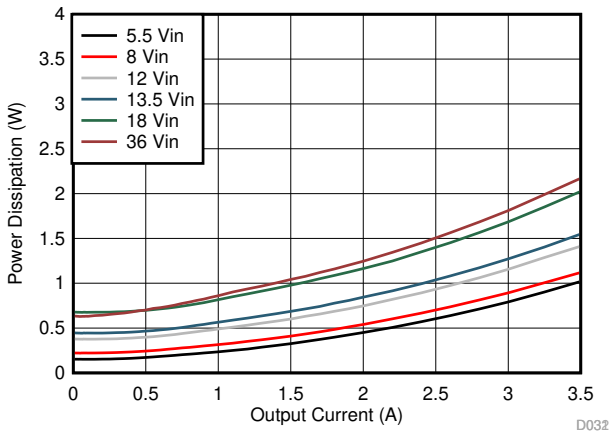


図 9-3. Power Dissipation 3.3-V Output

9.2.2 Fixed 5-V Output for USB-Type Applications

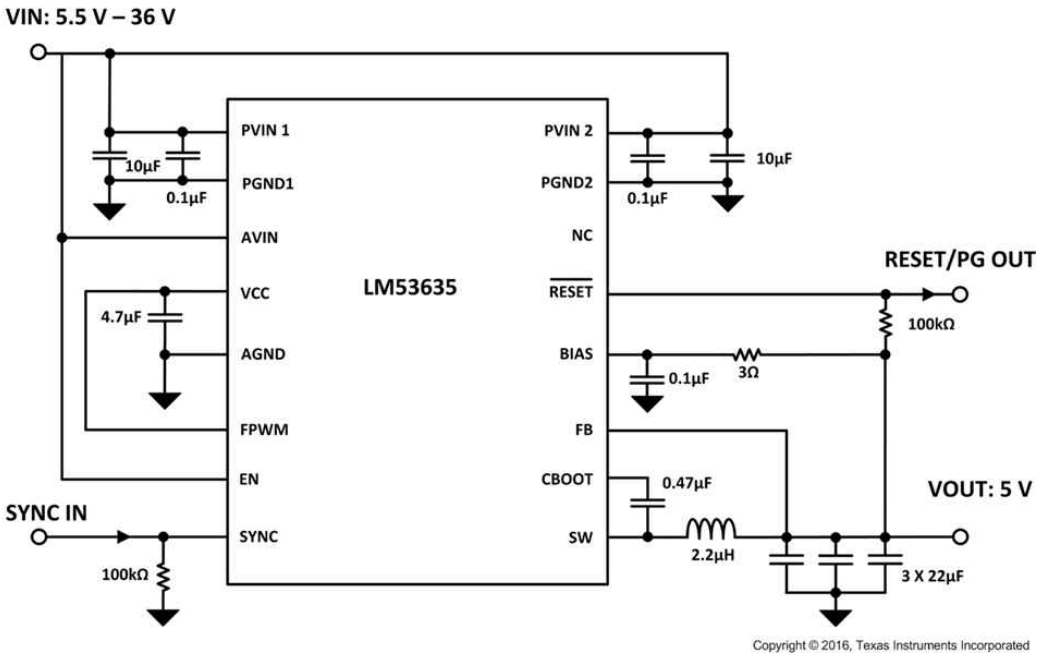


図 9-4. Fixed 5-V, 3.5-A Output Power Supply

9.2.2.1 Design Requirements

Example requirements for a typical 5-V application. The input voltages are here for illustration purposes only. See *セクション 7.5* for minimum operating input voltage. The minimum input voltage necessary to achieve proper output regulation depends on the components used. See 図 9-11 for typical drop-out behavior.

表 9-4. Example Requirements for 5-V Typical Application

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage range	8 V to 18 V steady state, 5.5 V to 36 V transients
Output current	0 A to 3.5 A
Switching Frequency at 0-A load	Critical: must have > 1.85 MHz
Current Consumption at 0-A load	Not critical: < 100 mA acceptable
Synchronization	Yes: 1.9 MHz supplied by MCU

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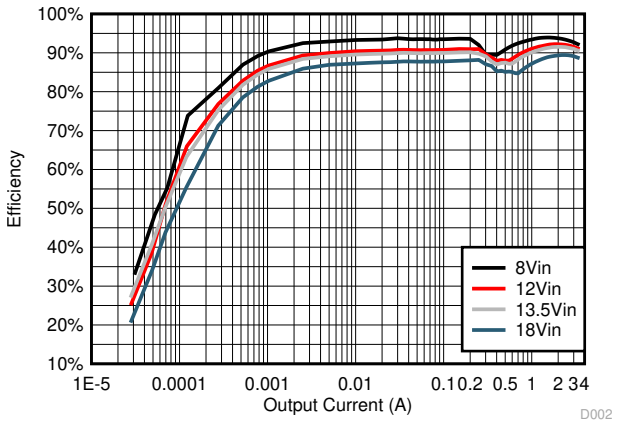
9.2.2.2 Detailed Design Procedure

- BIAS is connected to the output. This example assumes that the load is connected to the output through long wires so a 3 Ω resistor is inserted to minimize risks of damage to the part during load shorts. As a result a 0.1-µF capacitor is required close to the bias pin.
- FB is connected directly to the output. BIAS and FB are connected to the output via separate traces. This is important in order to reduce noise and achieve good performances. See *セクション 11.1* for more details on the proper layout method.
- SYNC is connected to ground through a pulldown resistor, and an external synchronization signal can be applied. The pulldown resistor ensures that the pin is not floating when the SYNC pin is not driven by any source.
- EN is connected to VIN so the device operates as soon as the input voltage rises above the $V_{IN-OPERATE}$ threshold.
- FPWM is connected to VCC. This causes the device to operate in FPWM mode. In this mode, the switching frequency is not affected by the output current and is ensured to be within the boundaries set by F_{SW}. The drawback is that the efficiency is not optimized for light loads. See *セクション 8.4* for more details.
- A 4.7-µF capacitor is connected between VCC and GND close to the VCC pin This ensures stable operation of the internal LDO.
- $\overline{\text{RESET}}$ is biased to the output in this example. A pullup resistor is necessary. A 100-kΩ is selected for this application and is generally sufficient. The value can be selected to match the needs of the application but must not lead to excessive current into the $\overline{\text{RESET}}$ pin when $\overline{\text{RESET}}$ is in a low state. Consult *セクション 7.1* for the maximum current allowed. In addition, a low pullup resistor could lead to an incorrect logic level due to the value of R_{RESET} . Consult *セクション 7.5* for details on the $\overline{\text{RESET}}$ pin.
- Input capacitor selection is detailed in *セクション 9.2.1.2.1.1*. It is important to connect small high-frequency capacitors C_{IN_HF1} and C_{IN_HF2} as close to both inputs PVIN1 and PVIN2 as possible.
- Output capacitor selection is detailed in *セクション 9.2.1.2.1.2.2*.
- Inductor selection is detailed in *セクション 9.2.1.2.1.2.1*. In general, a 2.2-µH inductor is recommended for the fixed output options. For the adjustable options, the inductance can vary with the output voltage due to ripple and current limit requirements.

9.2.2.3 Application Curves

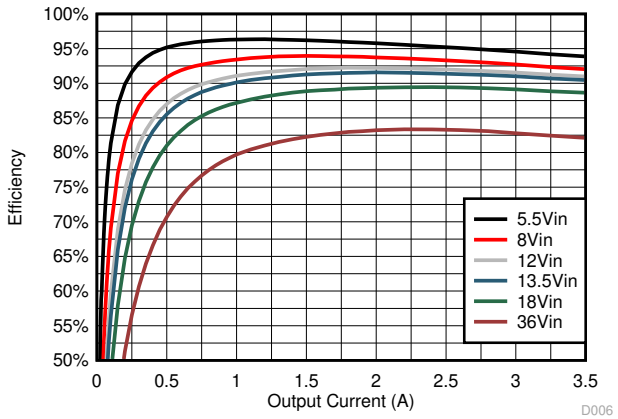
The following characteristics apply only to the circuit of *セクション 9.2.2*. *These parameters are not tested and represent typical performance only.* Unless otherwise stated, the following conditions apply: V_{IN} = 12 V, T_A = 25°C. For the purpose of offering the more information to the designer, information for the application with FPWM pin high (FPWM mode) and FPWM pin low (AUTO mode) is included, although the schematic shows the application running specifically in FPWM mode. The mode is specified under each following graph.

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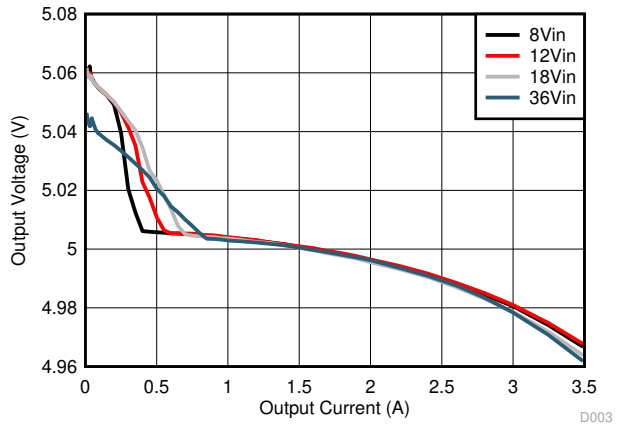
V_{OUT} = 5 V AUTO

図 9-5. Efficiency



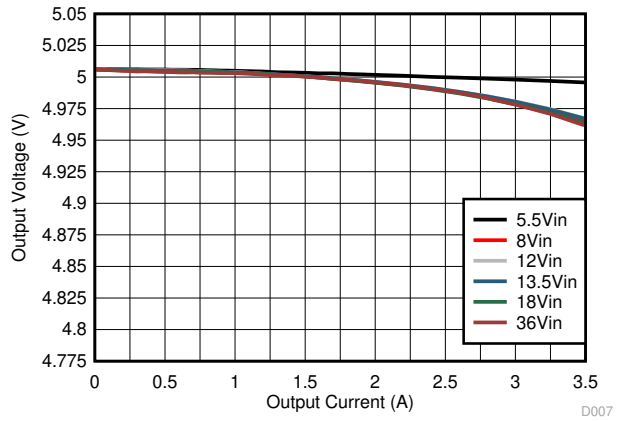
V_{OUT} = 5 V FPWM

図 9-6. Efficiency



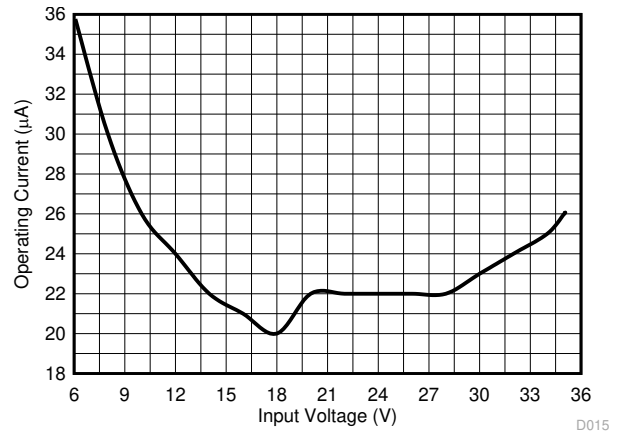
V_{OUT} = 5 V AUTO

図 9-7. Load and Line Regulation



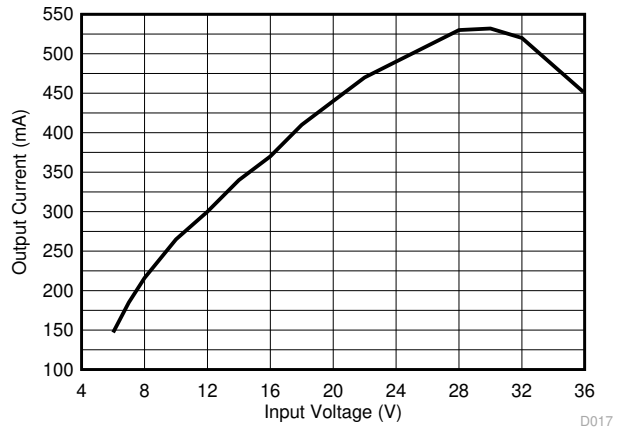
V_{OUT} = 5 V FPWM

図 9-8. Load and Line Regulation



V_{OUT} = 5 V AUTO I_{OUT} = 0 A

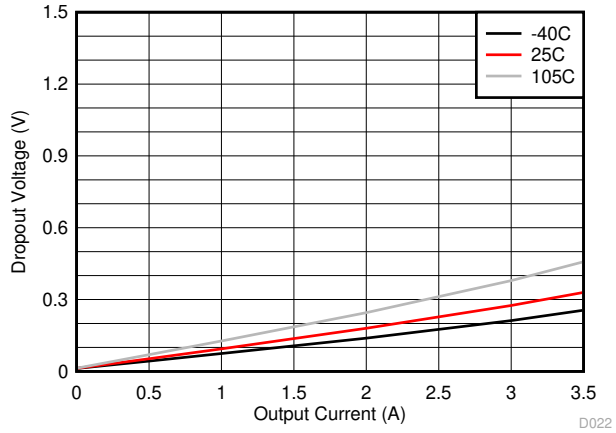
図 9-9. Input Supply Current (includes Leakage Current of the Capacitor)



V_{OUT} = 5 V

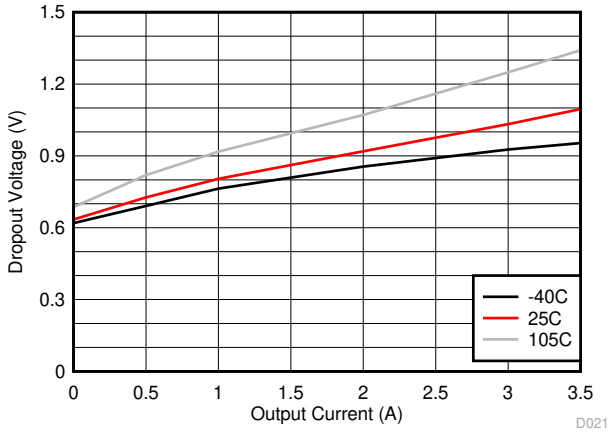
図 9-10. Load Current for PFM-to-PWM transition

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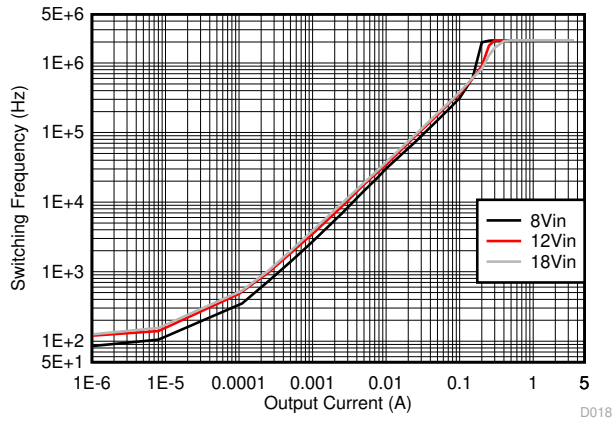
V_{OUT} = 5 V

図 9-11. Dropout for –3% Regulation



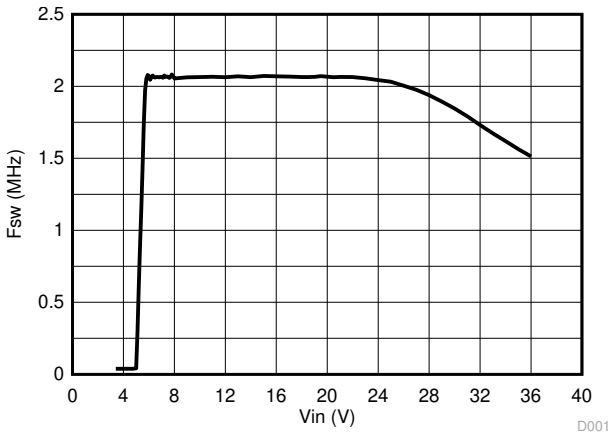
V_{OUT} = 5 V

図 9-12. Dropout for ≥ 1.85 MHz



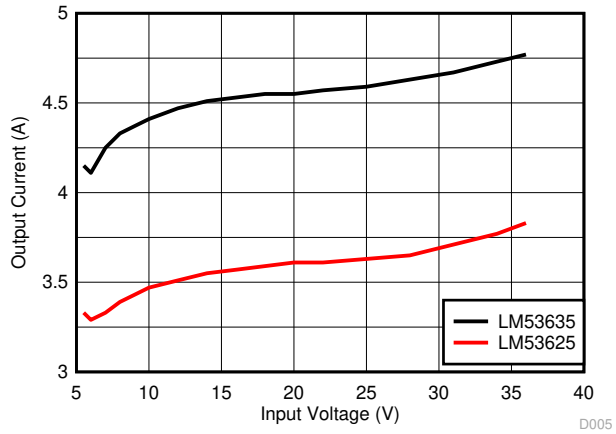
V_{OUT} = 5 V AUTO

図 9-13. Switching Frequency vs Load Current



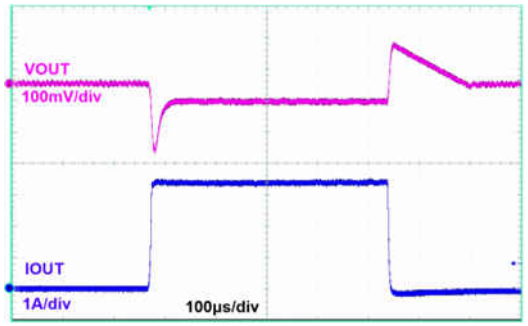
V_{OUT} = 5 V FPWM

図 9-14. Switching Frequency vs Input Voltage



V_{OUT} = 5 V L = 2.2µH

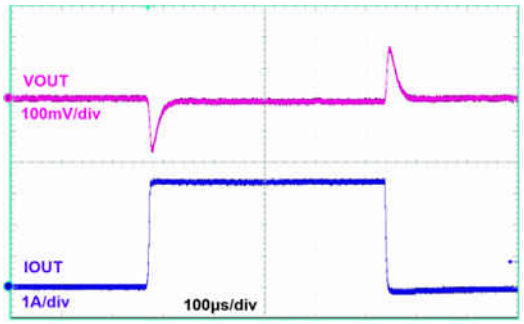
図 9-15. Output Current Level Limit Before Overcurrent Protection



AUTO
C_{OUT} = 3 × 22 µF
V_{OUT} = 5 V
I_{OUT} = 10 mA to 3.5 A
L = 2.2 µH
T_R = T_F = 1 µs

図 9-16. Load Transients

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FPWM | V_{OUT} = 5 V | L = 2.2 µH
C_{OUT} = 3 × 22 µF | I_{OUT} = 0 A to 3.5 A | T_R = T_F = 1µs

図 9-17. Load Transient

9.2.3 Fixed 3.3-V Output

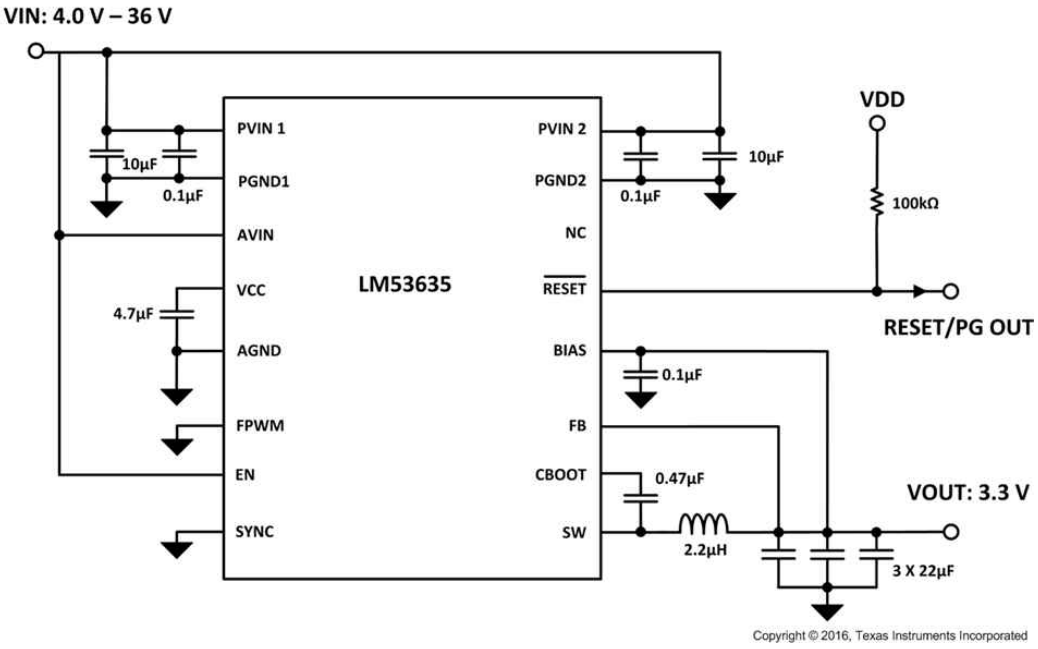


図 9-18. Fixed 3.3-V, 3.5-A Output Power Supply

9.2.3.1 Design Requirements

Example requirements for a typical 3.3-V application. The input voltages are here for illustration purposes only. See *セクション 7.5* for minimum operating input voltage. The minimum input voltage necessary to achieve proper output regulation depends on the components used. See 図 9-25 for typical drop-out behavior.

表 9-5. Example Requirements for 3.3-V Application

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage range	8-V to 18-V steady state, 4.0-V to 36-V transients
Output current	0 A to 3.5 A
Swtiching Frequency at 0-A load	Not critical: Need >1.85 MHz at high load only
Current Consumption at 0-A load	Critical: Need to ensure low current consumption to reduce battery drain
Synchronization	No

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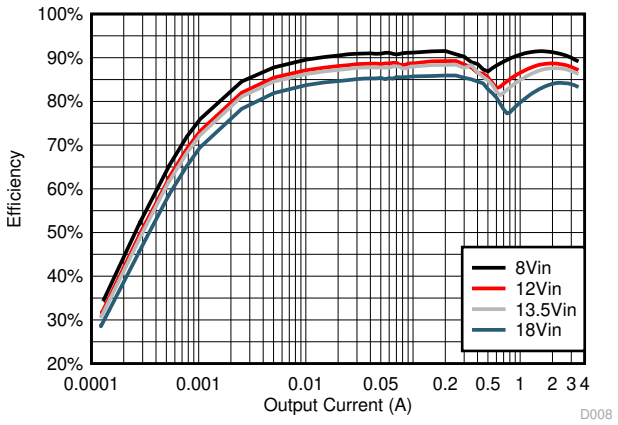
9.2.3.2 Detailed Design Procedure

- BIAS is connected to the output. This example assumes that the load is close to the output so no bias resistance is necessary. A 0.1-µF capacitor is still recommended close to the bias pin.
- FB is connected directly to the output. BIAS and FB are connected to the output via separate traces. This is important to reduce noise and achieve good performances. See *セクション 11.1* for more details on the proper layout method.
- SYNC is connected to ground directly as there is no need for this function in this application.
- EN is connected to VIN so the device perates as soon as the input voltage rises above the $V_{IN-OPERATE}$ threshold.
- FPWM is connected to GND. This causes the device to operate in AUTO mode. In this mode, the switching frequency is adjusted at light loads to keep efficiency maximum. As a result the switching frequency will change with the output current until medium load is reached. The part will then switch at the frequency defined by F_{SW}. See *セクション 8.4* for more details.
- A 4.7-µF capacitor is connected between VCC and GND close to the VCC pin This ensures stable operation of the internal LDO.
- $\overline{\text{RESET}}$ is biased to an external rail in this example. A pullup resistor is necessary. A 100 kΩ is selected for this application and is generally sufficient. The value can be selected to match the needs of the application but must not lead to excessive current into the $\overline{\text{RESET}}$ pin when $\overline{\text{RESET}}$ is in a low state. Consult *セクション 7.1* for the maximum current allowed. In addition, a low pull-up resistor could lead to an incorrect logic level due to the value of R_{RESET} . Consult *セクション 7.5* for details on the $\overline{\text{RESET}}$ pin.
- it is important to connect small high frequency capacitors C_{IN_HF1} and C_{IN_HF2} as close to both inputs PVIN1 and PVIN2 as possible. For the detailed process of choosing input capacitors, refer to *セクション 9.2.1.2.1.1*.
- Output capacitor selection is detailed in *セクション 9.2.1.2.1.2.2*.
- Inductor selection is detailed in *セクション 9.2.1.2.1.2.1*. In general, a 2.2-µH inductor is recommended for the fixed output options. For the adjustable options, the inductance can vary with the output voltage due to ripple and current limit requirements.

9.2.3.3 Application Curves

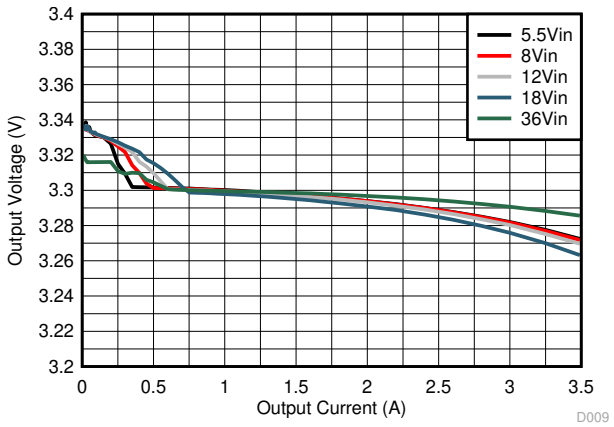
The following characteristics apply only to the circuit of 図 9-18. *These parameters are not tested and represent typical performance only.* Unless otherwise stated, the following conditions apply: V_{IN} = 12 V, T_A = 25°C. For the purpose of offering the more information to the designer, information for the application with FPWM pin high (FPWM mode) and FPWM pin low (AUTO mode) is included, although the schematic shows the application running specifically in AUTO mode. The mode is specified under each of the following graphs.

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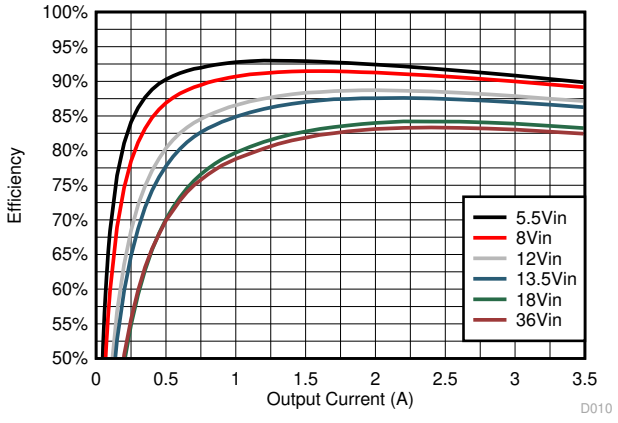
V_{OUT} = 3.3 V AUTO

図 9-19. Efficiency



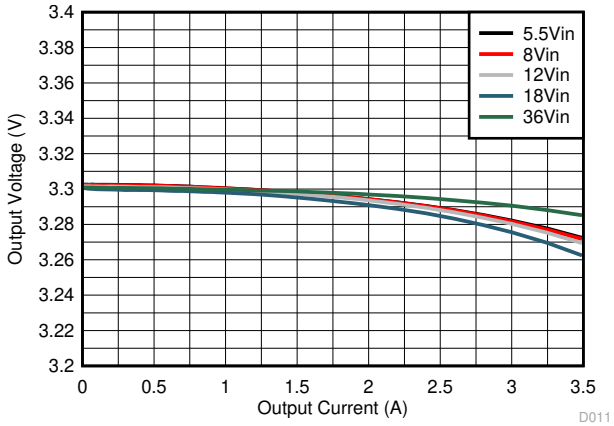
V_{OUT} = 3.3 V AUTO

図 9-20. Load and Line Regulation



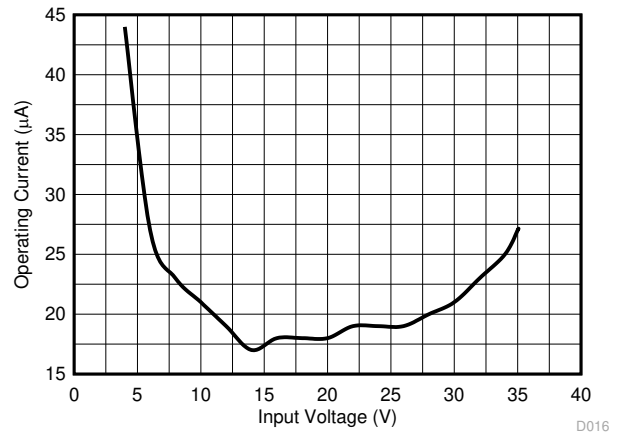
V_{OUT} = 3.3 V FPWM

図 9-21. Efficiency



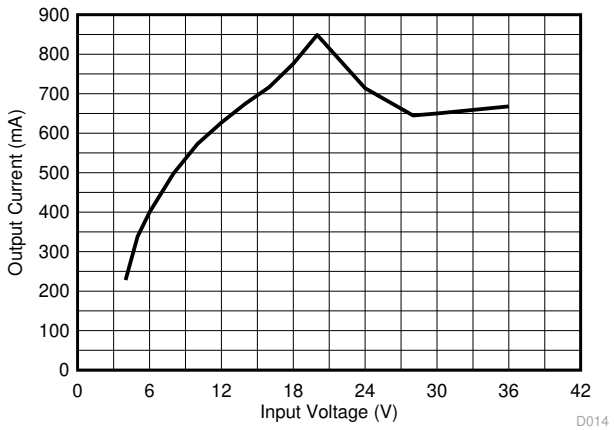
V_{OUT} = 3.3 V FPWM

図 9-22. Load and Line Regulation



V_{OUT} = 3.3 V AUTO I_{OUT} = 0A

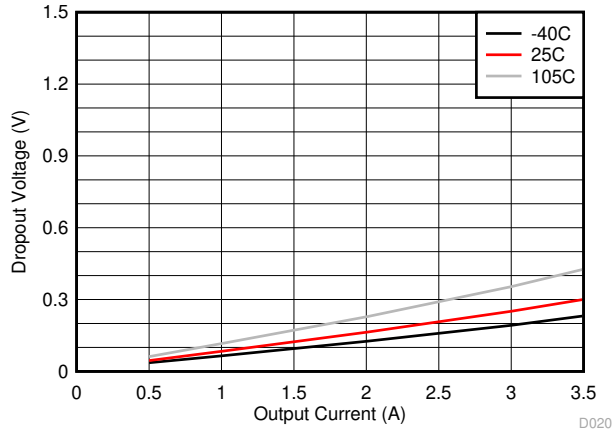
図 9-23. Input Supply Current (Includes Leakage Current of Capacitor)



V_{OUT} = 3.3 V

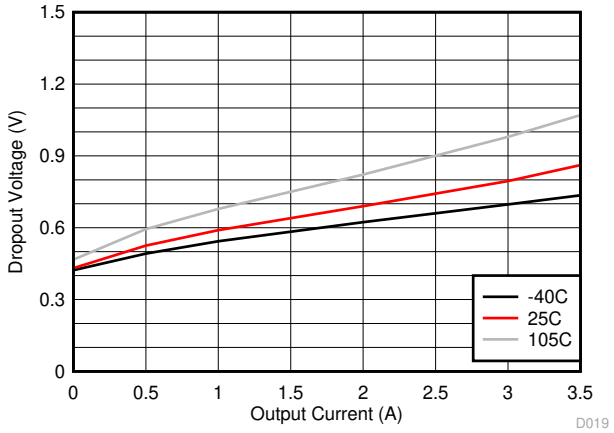
図 9-24. Load Current for PFM-to-PWM Transition

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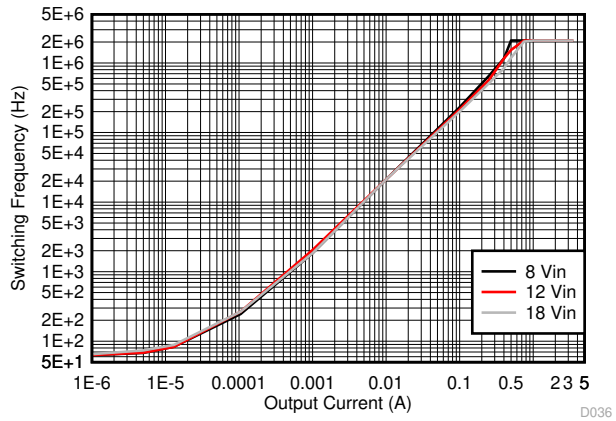
V_{OUT} = 3.3 V

図 9-25. Dropout for –3% Regulation



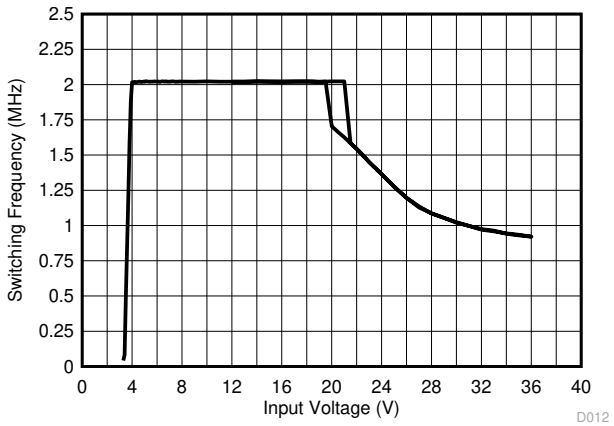
V_{OUT} = 3.3 V

図 9-26. Dropout for ≥ 1.85 MHz



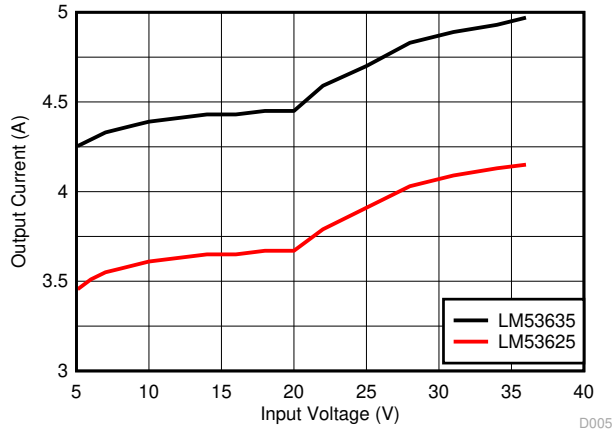
V_{OUT} = 3.3 V AUTO

図 9-27. Switching Frequency vs Load Current



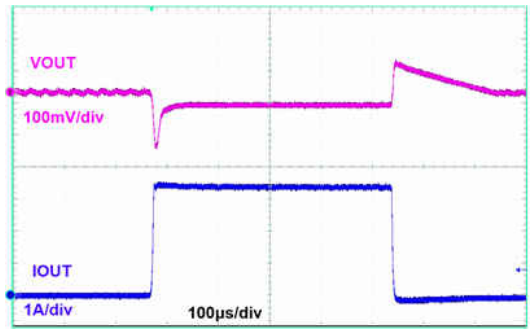
V_{OUT} = 3.3 V FPWM I_{OUT} = 1 A

図 9-28. Switching Frequency vs Input Voltage



V_{OUT} = 3.3 V L=2.2 µH I_{OUT} = 1 A

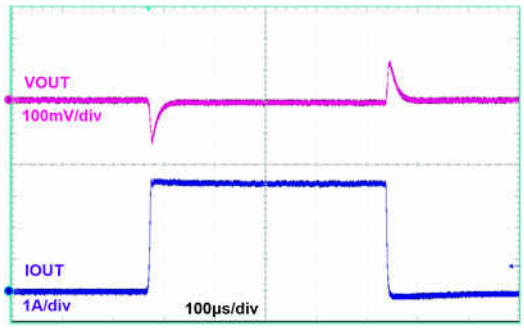
図 9-29. Output Current Level for Overcurrent Protection Trip



AUTO V_{OUT} = 3.3 V L = 2.2 µH,
C_{OUT} = 3 × 22 µF I_{OUT} = 0 A to 3.5 A $T_R = T_F$ = 1 µs

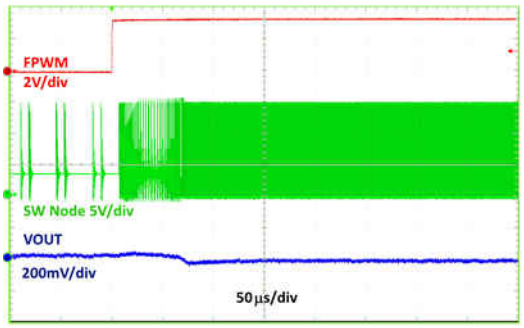
図 9-30. Load Transient

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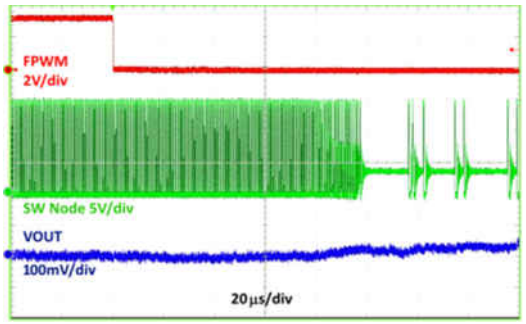
FPWM V_{OUT} = 3.3 V L = 2.2 µH,
C_{OUT} = 3 × 22 µF I_{OUT} = 0 A to 3.5 A $T_R = T_F$ = 1 µs

図 9-31. Load Transient



V_{OUT} = 3.3 V I_{OUT} = 10 mA

図 9-32. Mode Change Transient AUTO to FPWM mode



V_{OUT} = 3.3 V I_{OUT} = 10 mA

図 9-33. Mode Change Transient FPWM to AUTO Mode

9.2.4 Adjustable Output

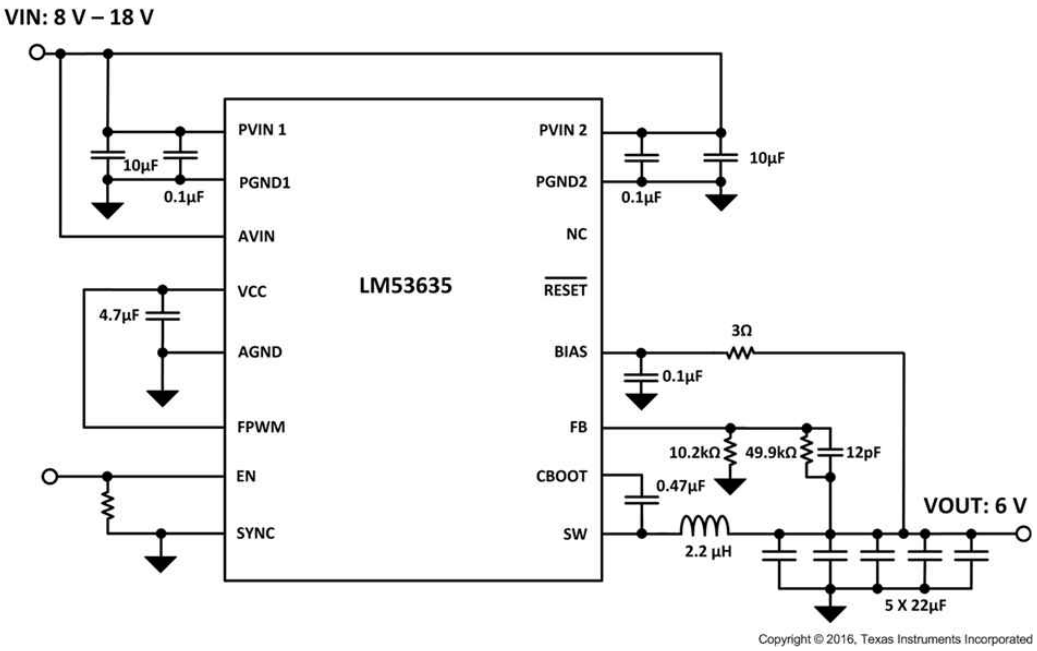


図 9-34. 6 V Output Power Supply

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9.2.4.1 Design Requirements

The application highlighted in this section is for a typical 6-V system but can be used as a basis for the implementation of the adjustable version of the LM53625/LM53635 for other output voltages as well. The input voltages are here for illustration purposes only. See セクション 7.5 for minimum operating input voltage.

表 9-6. Example Requirements for 6-V Application

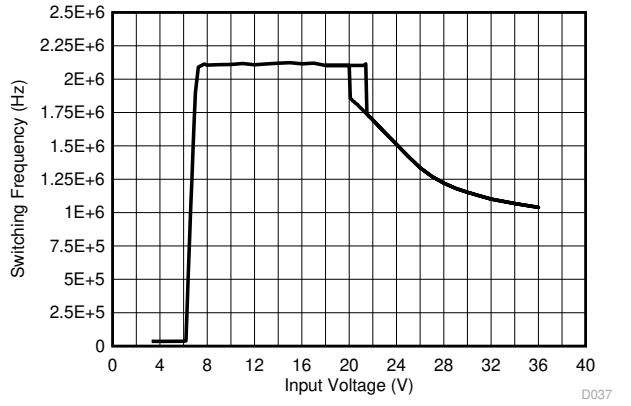
DESIGN PARAMETER	EXAMPLE VALUE
Input voltage range	8-V to 18-V steady state
Output current	0 A to 3.5 A
Swtiching Frequency at 0-A load	Constant frequency preferred
Current Consumption at 0-A load	Not critical
Synchronization	No

9.2.4.2 Detailed Design Procedure

- BIAS is connected to the output. This example assumes that inductive short are a risk for this application so a 3-Ω resistor is added between BIAS and the output. A 0.1-µF capacitor is added close the BIAS pin.
- FB is connected to the output through a voltage divider in order to create a voltage of 1 V at the FB pin when the output is at 6 V. A 12-pF capacitance is added in parallel with the top feedback resistor in order to improve transient behavior. BIAS and FB are connected to the output via separate traces. This is important to reduce noise and achieve good performances. See セクション 11.1 for more details on the proper layout method.
- SYNC is connected to ground directly as there is no need for this function in this application.
- EN is toggled by an external device (like an MCU for example). A pulldown resistor is placed to ensure the part does not turn on if the external source is not driving the pin (Hi-Z condition).
- FPWM is connected to GND. This leads the device to operate in AUTO mode. In this mode, the switching frequency is adjusted at light loads to keep efficiency maximum. As a result the switching frequency changes with the output current until medium load is reached. The device then switches at the frequency defined by F_{SW}. See セクション 8.4 for more details.
- A 4.7-µF capacitor is connected between VCC and GND close to the VCC pin. This ensure stable operation of the internal LDO.
- $\overline{\text{RESET}}$ is not used in this example so the pin has been left floating. Other possible connections can be seen in the previous typical applications and in セクション 8.3.1.
- Power components (input capacitor, output capacitor, and inductor) selection can be found here in セクション 9.2.1.2.1.

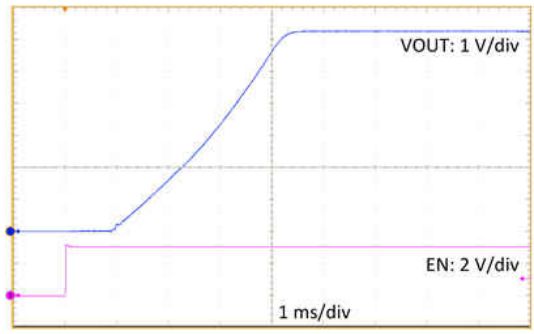
9.2.4.3 Application Curves

The following characteristics apply only to the circuit of 図 9-34. *These parameters are not tested and represent typical performance only.* Unless otherwise stated, the following conditions apply: V_{IN} = 12 V, T_A = 25°C. For the purpose of offering meaningful information to the designer, information is included for the application with FPWM pin high (FPWM mode) and FPWM pin low (AUTO mode) although the schematic shows the application running specifically in AUTO mode. The mode is specified under each of the following graphs.



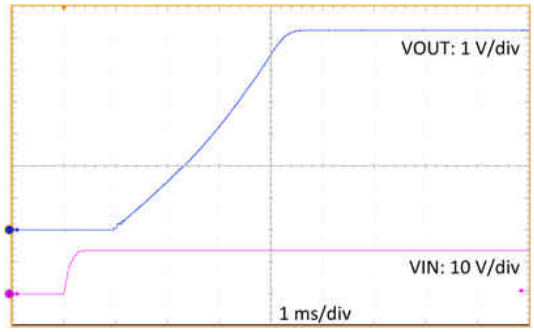
V_{OUT} = 6 V (ADJ part) FPWM I_{OUT} = 0 A

図 9-35. Switching Frequency vs Input Voltage



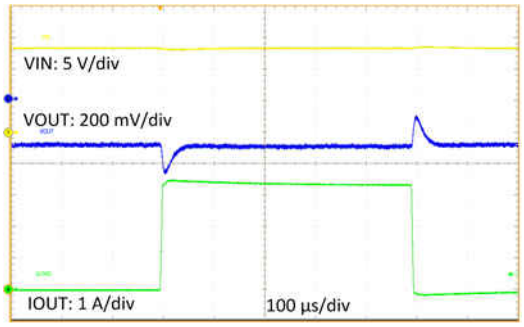
V_{OUT} = 6 V (ADJ part) FPWM I_{OUT} = 0 A

図 9-36. Start-up Waveform



V_{OUT} = 6 V (ADJ part) FPWM I_{OUT} = 0 A

図 9-37. Start-up Waveform (EN tied to VIN)



V_{OUT} = 6 V (ADJ part) FPWM

図 9-38. Load Transient

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9.3 What to Do and What Not to Do

- **Don't:** Exceed the *セクション 7.1*.
- **Don't:** Exceed the *セクション 7.3*.
- **Don't:** Allow the EN, FPWM or SYNC input to float.
- **Don't:** Allow the output voltage to exceed the input voltage, nor go below ground.
- **Don't:** Use the thermal data given in the *セクション 7.4* table to design your application.
- **Do:** Follow all of the guidelines and/or suggestions found in this data sheet before committing a design to production. TI Application Engineers are ready to help critique designs and PCB layouts to help ensure successful projects.
- **Do:** Refer to the helpful documents found in *セクション 12.2.1*.

10 Power Supply Recommendations

The characteristics of the input supply must be compatible with the *セクション 7.1* and *セクション 7.3* found in this data sheet. In addition, the input supply must be capable of delivering the required input current to the loaded regulator. The average input current can be estimated with 式 6:

$$I_{IN} = \frac{V_{OUT} \cdot I_{OUT}}{V_{IN} \cdot \eta} \tag{6}$$

where

- η is the efficiency.

If the regulator is connected to the input supply through long wires or PCB traces, special care is required to achieve good performance. The parasitic inductance and resistance of the input cables can have an adverse effect on the operation of the regulator. The parasitic inductance, in combination with the low ESR ceramic input capacitors, can form an under-damped resonant circuit. This circuit may cause overvoltage transients at the VIN pin, each time the input supply is cycled on and off. The parasitic resistance causes the voltage at the VIN pin to dip when the load on the regulator is switched on or exhibits a transient. If the regulator is operating close to the minimum input voltage, this dip may cause the device to shut down and/or reset. The best way to solve these kinds of issues is to reduce the distance from the input supply to the regulator and/or use an aluminum or tantalum input capacitor in parallel with the ceramics. The moderate ESR of these types of capacitors helps to damp the input resonant circuit and reduce any voltage overshoots. A value in the range of 20 µF to 100 µF is usually sufficient to provide input damping and help to hold the input voltage steady during large load transients.

Sometimes, for other system considerations, an input filter is used in front of the regulator. This can lead to instability, as well as some of the effects mentioned above, unless it is designed carefully. SNVA538 and SNVA489c provide helpful suggestions when designing an input filter for any switching regulator.

In some cases a transient voltage suppressor (TVS) is used on the input of regulators. One class of this device has a *snap-back* V-I characteristic (thyristor type). The use of a device with this type of characteristic is not recommend. When the TVS fires, the clamping voltage drops to a very low value. If this holding voltage is less than the output voltage of the regulator, the output capacitors are discharged through the regulator back to the input. This uncontrolled current flow could damage the regulator.

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11 Layout

11.1 Layout Guidelines

The PCB layout of a DC-DC converter is critical for optimal performance of the application. For a buck converter the input loop formed by the input capacitors and power grounds are very critical. The input loop carries fast transient currents that cause larger transient voltages when reacting with a parasitic loop inductance. The IC uses two input loops in parallel IN1 and IN2 as shown in 図 11-1 that cuts the parasitic input inductance in half. To get the minimum input loop area two small high frequency capacitors CIN1 and CIN2 are placed as close as possible.

To further reduce inductance, an input current return path should be placed underneath the loops IN1 and IN2. The closest metal plane is MID1 Layer2, and with a solid copper plane placed right under the IN1 and IN2 loop the parasitic loop inductance is minimized. Connecting this MID1 Layer2 plane then to GND will provide a nice bridge connection between GND1 and GND2 as well. Minimizing the parasitic input loop inductance will minimize switch node ringing and EMI.

The output current loop can be optimized as well by using two ceramic output caps COUT1 and COUT2 to each side. They will form two parallel ground return paths OUT1 from COUT1 back to the low side FET PGND1 pins 5,6,7,8 and a second symmetric ground return path OUT2 from COUT2 back to low side FET PGND2 pins 10,11,12 and 13. Having two parallel ground return path will yield into reduced “ground bouncing” and reduced sensitivity of surrounding circuits sensitive to it.

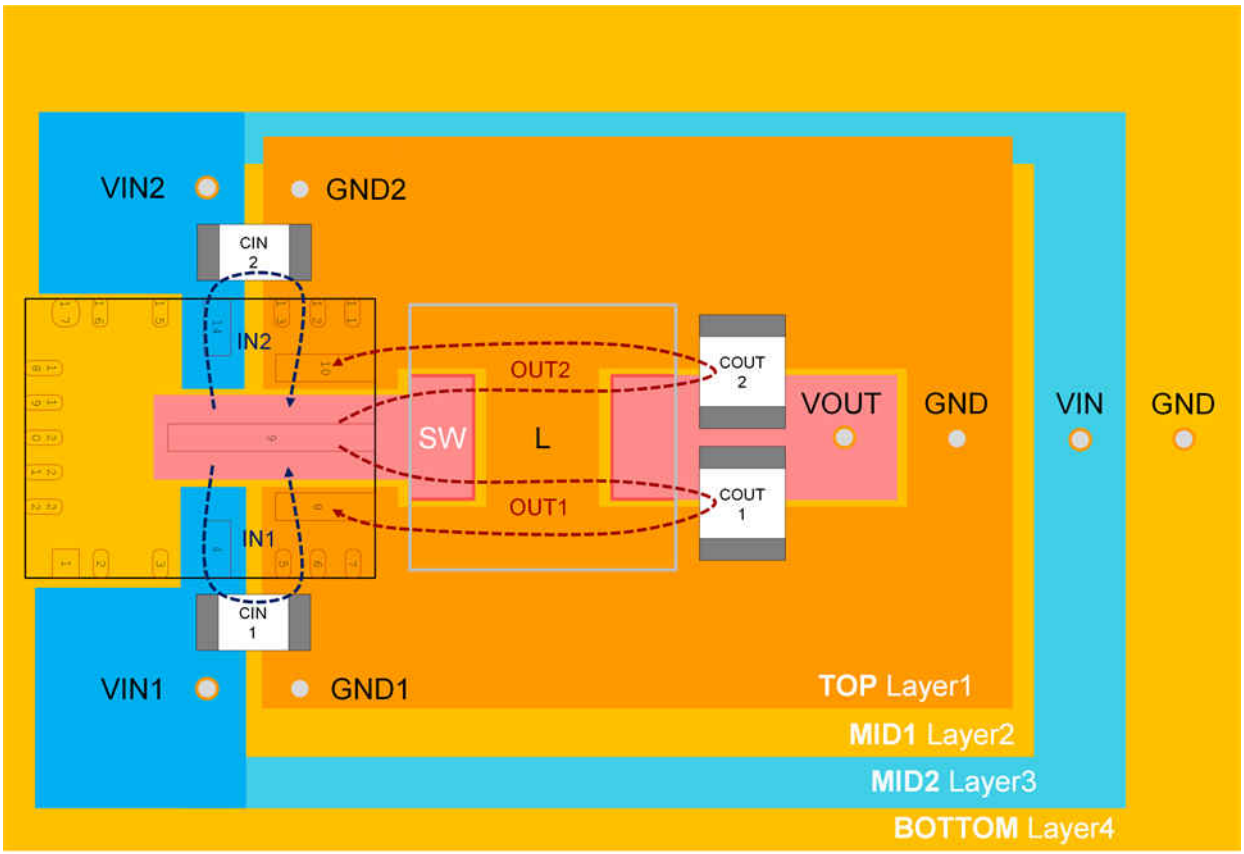


図 11-1. Layout of the Power Components and Current Flow

Providing adequate thermal paths to dissipate heat is critical for operation at full current. The recommended method for heat dissipation is to use large solid 2 oz copper planes well connected to the power pins VIN1, VIN2, GND1 and GND2 which transfer the heat out of the IC over the TOP Layer1 copper planes. It is important to leave the TOP Layer1 copper planes as unbroken as much as possible so that heat is not trapped near the IC. The heat flow can be further optimized by thermally connecting the TOP Layer 1 plane to large BOTTOM Layer4

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2oz. copper planes with vias. MID2 Layer3 is then open for all other signal routing. A fully filled / solid BOTTOM Layer4 ground plane without any interruptions or ground splitting is beneficial for EMI as well. Most important for low EMI is to use the smallest possible switch node copper area. The switch node including the C_{BOOT} cap has the largest dv/dt signal causing common mode noise coupling. Using any kind of grounded shield around the switch node will "shorten" and reduce this e-field.

All these DC/DC converter descriptions can be transformed into layout guidelines:

1. *Place two 0.047-µF / 50-V high frequency input capacitors C_{IN1} and C_{IN2} as close as possible* to the VIN1/2 and PGND1/2 pins to minimize switch node ringing.
2. *Place bypass capacitors for VCC and BIAS close to their respective pins.* Make sure AGND pin "sees" the C_{VCC} and C_{BIAS} capacitors first before connecting it to GND.
3. *Place C_{BOOT} capacitor with smallest parasitic loop.* Shielding the C_{BOOT} capacitor and switch node will have biggest impact to reduce common mode noise. Placing a small R_{BOOT} resistor (less than 3 Ω is recommended) in series to C_{BOOT} will slow down the dV/dt of the switch node and reduce EMI.
4. *Place the feedback resistor divider for adjustable parts as close as possible to the FB pin and to AGND pin of the device*. Use dedicated feedback trace and away from switch node and C_{BOOT} capacitor to avoid any cross coupling into sensitive analog feedback.
5. *Use dedicated BIAS trace to avoid noise into feedback trace.*
6. *Use a 3-Ω to 5-Ω resistor between the output and BIAS* if the load is far from the output of the converter or inductive shorts on the output are possible.
7. *Use well connected large 2-oz. TOP and BOTTOM copper planes for all power pins VIN1/2 and PGND1/2.*
8. *Minimize switch node and C_{BOOT} area for lowest EMI common mode noise.*
9. *For lowest EMI place input and output wires on same side of PCB, using EMI filter and away from switch node.*
10. *The resources in セクション 12 provide additional important guidelines.*

11.2 Layout Example

This example layout is the one used in REV A of the LM53635 EVM. It shows the C_{IN} and C_{IN_HF} capacitors placed symmetrically either side of the device.

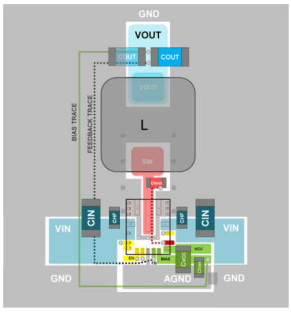


図 11-2. Recommended Layout for LM53625/35-Q1

12 Device and Documentation Support

12.1 Device Support

12.1.1 Third-Party Products Disclaimer

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12.2 Documentation Support

12.2.1 Related Documentation

For additional information, see the following:

- *Optimizing Transient Response of Internally Compensated dc-dc Converters With Feedforward Capacitor* (SLVA289)
- *Output Ripple Voltage for Buck Switching Regulator* (SLVA630)
- *AN-1149 Layout Guidelines for Switching Power Supplies* (SNVA021)
- *AN-1229 Simple Switcher® PCB Layout Guidelines* (SNVA054)
- *Constructing Your Power Supply- Layout Considerations* (SLUP230)
- *AN-2020 Thermal Design By Insight, Not Hindsight* (SNVA419)
- *Semiconductor and IC Package Thermal Metrics* (SPRA953)

12.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

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WEBENCH® is a registered trademark of TI.
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12.6 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.7 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LM536253QRNLRQ1	Active	Production	VQFN-HR (RNL) | 22	3000 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 150	L536253
LM536253QRNLRQ1.A	Active	Production	VQFN-HR (RNL) | 22	3000 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 150	L536253
LM536253QRNLTQ1	Active	Production	VQFN-HR (RNL) | 22	250 | SMALL T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 150	L536253
LM536253QRNLTQ1.A	Active	Production	VQFN-HR (RNL) | 22	250 | SMALL T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 150	L536253
LM536255QRNLRQ1	Active	Production	VQFN-HR (RNL) | 22	3000 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 150	L536255
LM536255QRNLRQ1.A	Active	Production	VQFN-HR (RNL) | 22	3000 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 150	L536255
LM536255QRNLTQ1	Active	Production	VQFN-HR (RNL) | 22	250 | SMALL T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 150	L536255
LM536255QRNLTQ1.A	Active	Production	VQFN-HR (RNL) | 22	250 | SMALL T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 150	L536255
LM53625AQRNLRQ1	Active	Production	VQFN-HR (RNL) | 22	3000 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 150	L53625A
LM53625AQRNLRQ1.A	Active	Production	VQFN-HR (RNL) | 22	3000 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 150	L53625A
LM53625AQRNLTQ1	Active	Production	VQFN-HR (RNL) | 22	250 | SMALL T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 150	L53625A
LM53625AQRNLTQ1.A	Active	Production	VQFN-HR (RNL) | 22	250 | SMALL T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 150	L53625A
LM53625LQRNLRQ1	Active	Production	VQFN-HR (RNL) | 22	3000 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 150	L53625L
LM53625LQRNLRQ1.A	Active	Production	VQFN-HR (RNL) | 22	3000 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 150	L53625L
LM53625LQRNLTQ1	Active	Production	VQFN-HR (RNL) | 22	250 | SMALL T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 150	L53625L
LM53625LQRNLTQ1.A	Active	Production	VQFN-HR (RNL) | 22	250 | SMALL T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 150	L53625L
LM53625LQURNLRQ1	Active	Production	VQFN-HR (RNL) | 22	3000 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 150	U53625L
LM53625LQURNLRQ1.A	Active	Production	VQFN-HR (RNL) | 22	3000 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 150	U53625L
LM53625MQRNLRQ1	Active	Production	VQFN-HR (RNL) | 22	3000 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 150	L53625M
LM53625MQRNLRQ1.A	Active	Production	VQFN-HR (RNL) | 22	3000 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 150	L53625M
LM53625MQRNLTQ1	Active	Production	VQFN-HR (RNL) | 22	250 | SMALL T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 150	L53625M
LM53625MQRNLTQ1.A	Active	Production	VQFN-HR (RNL) | 22	250 | SMALL T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 150	L53625M
LM53625MQURNLRQ1	Active	Production	VQFN-HR (RNL) | 22	3000 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 150	U53625M
LM53625MQURNLRQ1.A	Active	Production	VQFN-HR (RNL) | 22	3000 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 150	U53625M
LM53625NQRNLRQ1	Active	Production	VQFN-HR (RNL) | 22	3000 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 150	L53625N
LM53625NQRNLRQ1.A	Active	Production	VQFN-HR (RNL) | 22	3000 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 150	L53625N
LM53625NQRNLTQ1	Active	Production	VQFN-HR (RNL) | 22	250 | SMALL T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 150	L53625N
LM53625NQRNLTQ1.A	Active	Production	VQFN-HR (RNL) | 22	250 | SMALL T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 150	L53625N
LM53625NQURNLRQ1	Active	Production	VQFN-HR (RNL) | 22	3000 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 150	U53625N

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LM53625NQURNLRQ1.A	Active	Production	VQFN-HR (RNL) | 22	3000 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 150	U53625N
LM536353QRNLRQ1	Active	Production	VQFN-HR (RNL) | 22	3000 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 150	L536353
LM536353QRNLRQ1.A	Active	Production	VQFN-HR (RNL) | 22	3000 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 150	L536353
LM536353QRNLTQ1	Active	Production	VQFN-HR (RNL) | 22	250 | SMALL T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 150	L536353
LM536353QRNLTQ1.A	Active	Production	VQFN-HR (RNL) | 22	250 | SMALL T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 150	L536353
LM536355QRNLRQ1	Active	Production	VQFN-HR (RNL) | 22	3000 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 150	L536355
LM536355QRNLRQ1.A	Active	Production	VQFN-HR (RNL) | 22	3000 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 150	L536355
LM536355QRNLTQ1	Active	Production	VQFN-HR (RNL) | 22	250 | SMALL T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 150	L536355
LM536355QRNLTQ1.A	Active	Production	VQFN-HR (RNL) | 22	250 | SMALL T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 150	L536355
LM53635AQRNLRQ1	Active	Production	VQFN-HR (RNL) | 22	3000 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 150	L53635A
LM53635AQRNLRQ1.A	Active	Production	VQFN-HR (RNL) | 22	3000 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 150	L53635A
LM53635AQRNLTQ1	Active	Production	VQFN-HR (RNL) | 22	250 | SMALL T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 150	L53635A
LM53635AQRNLTQ1.A	Active	Production	VQFN-HR (RNL) | 22	250 | SMALL T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 150	L53635A
LM53635LQRNLRQ1	Active	Production	VQFN-HR (RNL) | 22	3000 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 150	L53635L
LM53635LQRNLRQ1.A	Active	Production	VQFN-HR (RNL) | 22	3000 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 150	L53635L
LM53635LQRNLTQ1	Active	Production	VQFN-HR (RNL) | 22	250 | SMALL T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 150	L53635L
LM53635LQRNLTQ1.A	Active	Production	VQFN-HR (RNL) | 22	250 | SMALL T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 150	L53635L
LM53635MQRNLRQ1	Active	Production	VQFN-HR (RNL) | 22	3000 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 150	L53635M
LM53635MQRNLRQ1.A	Active	Production	VQFN-HR (RNL) | 22	3000 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 150	L53635M
LM53635MQRNLTQ1	Active	Production	VQFN-HR (RNL) | 22	250 | SMALL T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 150	L53635M
LM53635MQRNLTQ1.A	Active	Production	VQFN-HR (RNL) | 22	250 | SMALL T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 150	L53635M
LM53635MQURNLRQ1	Active	Production	VQFN-HR (RNL) | 22	3000 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 150	U53635M
LM53635MQURNLRQ1.A	Active	Production	VQFN-HR (RNL) | 22	3000 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 150	U53635M
LM53635NQRNLRQ1	Active	Production	VQFN-HR (RNL) | 22	3000 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 150	L53635N
LM53635NQRNLRQ1.A	Active	Production	VQFN-HR (RNL) | 22	3000 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 150	L53635N
LM53635NQRNLTQ1	Active	Production	VQFN-HR (RNL) | 22	250 | SMALL T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 150	L53635N
LM53635NQRNLTQ1.A	Active	Production	VQFN-HR (RNL) | 22	250 | SMALL T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 150	L53635N
LM53635NQURNLRQ1	Active	Production	VQFN-HR (RNL) | 22	3000 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 150	U53635N
LM53635NQURNLRQ1.A	Active	Production	VQFN-HR (RNL) | 22	3000 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 150	U53635N

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

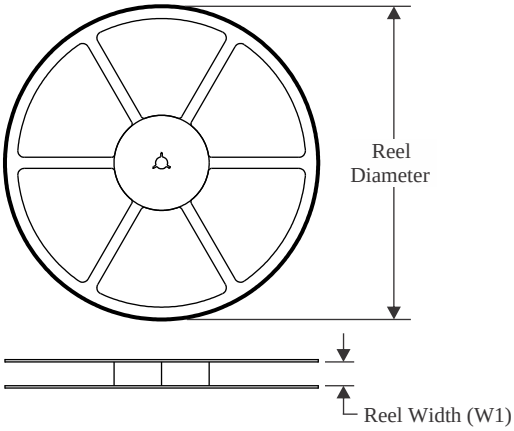
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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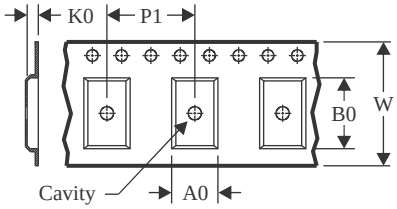
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

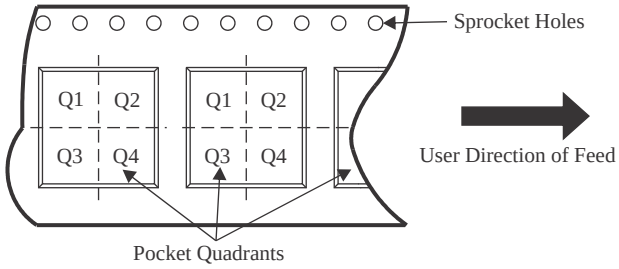


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

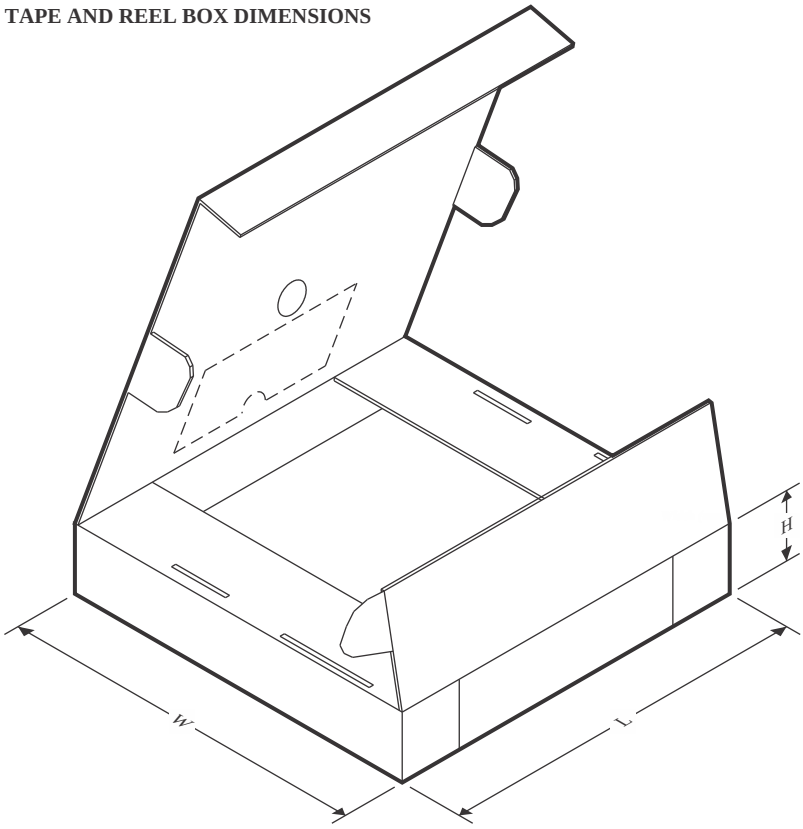


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM536253QRNLRQ1	VQFN-HR	RNL	22	3000	330.0	12.4	4.3	5.3	1.3	8.0	12.0	Q1
LM536253QRNLTQ1	VQFN-HR	RNL	22	250	180.0	12.4	4.3	5.3	1.3	8.0	12.0	Q1
LM536255QRNLRQ1	VQFN-HR	RNL	22	3000	330.0	12.4	4.3	5.3	1.3	8.0	12.0	Q1
LM536255QRNLTQ1	VQFN-HR	RNL	22	250	180.0	12.4	4.3	5.3	1.3	8.0	12.0	Q1
LM53625AQRNLRQ1	VQFN-HR	RNL	22	3000	330.0	12.4	4.3	5.3	1.3	8.0	12.0	Q1
LM53625AQRNLTQ1	VQFN-HR	RNL	22	250	180.0	12.4	4.3	5.3	1.3	8.0	12.0	Q1
LM53625LQRNLRQ1	VQFN-HR	RNL	22	3000	330.0	12.4	4.3	5.3	1.3	8.0	12.0	Q1
LM53625LQRNLTQ1	VQFN-HR	RNL	22	250	180.0	12.4	4.3	5.3	1.3	8.0	12.0	Q1
LM53625LQURNLRQ1	VQFN-HR	RNL	22	3000	330.0	12.4	4.3	5.3	1.3	8.0	12.0	Q1

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM53625MQRNLRQ1	VQFN-HR	RNL	22	3000	330.0	12.4	4.3	5.3	1.3	8.0	12.0	Q1
LM53625MQRNLTQ1	VQFN-HR	RNL	22	250	180.0	12.4	4.3	5.3	1.3	8.0	12.0	Q1
LM53625MQURNLRQ1	VQFN-HR	RNL	22	3000	330.0	12.4	4.3	5.3	1.3	8.0	12.0	Q1
LM53625NQRNLRQ1	VQFN-HR	RNL	22	3000	330.0	12.4	4.3	5.3	1.3	8.0	12.0	Q1
LM53625NQRNLTQ1	VQFN-HR	RNL	22	250	180.0	12.4	4.3	5.3	1.3	8.0	12.0	Q1
LM53625NQURNLRQ1	VQFN-HR	RNL	22	3000	330.0	12.4	4.3	5.3	1.3	8.0	12.0	Q1
LM536353QRNLRQ1	VQFN-HR	RNL	22	3000	330.0	12.4	4.3	5.3	1.3	8.0	12.0	Q1
LM536353QRNLTQ1	VQFN-HR	RNL	22	250	180.0	12.4	4.3	5.3	1.3	8.0	12.0	Q1
LM536355QRNLRQ1	VQFN-HR	RNL	22	3000	330.0	12.4	4.3	5.3	1.3	8.0	12.0	Q1
LM536355QRNLTQ1	VQFN-HR	RNL	22	250	180.0	12.4	4.3	5.3	1.3	8.0	12.0	Q1
LM53635AQRNLRQ1	VQFN-HR	RNL	22	3000	330.0	12.4	4.3	5.3	1.3	8.0	12.0	Q1
LM53635AQRNLTQ1	VQFN-HR	RNL	22	250	180.0	12.4	4.3	5.3	1.3	8.0	12.0	Q1
LM53635LQRNLRQ1	VQFN-HR	RNL	22	3000	330.0	12.4	4.3	5.3	1.3	8.0	12.0	Q1
LM53635LQRNLTQ1	VQFN-HR	RNL	22	250	180.0	12.4	4.3	5.3	1.3	8.0	12.0	Q1
LM53635MQRNLRQ1	VQFN-HR	RNL	22	3000	330.0	12.4	4.3	5.3	1.3	8.0	12.0	Q1
LM53635MQRNLTQ1	VQFN-HR	RNL	22	250	180.0	12.4	4.3	5.3	1.3	8.0	12.0	Q1
LM53635MQURNLRQ1	VQFN-HR	RNL	22	3000	330.0	12.4	4.3	5.3	1.3	8.0	12.0	Q1
LM53635NQRNLRQ1	VQFN-HR	RNL	22	3000	330.0	12.4	4.3	5.3	1.3	8.0	12.0	Q1
LM53635NQRNLTQ1	VQFN-HR	RNL	22	250	180.0	12.4	4.3	5.3	1.3	8.0	12.0	Q1
LM53635NQURNLRQ1	VQFN-HR	RNL	22	3000	330.0	12.4	4.3	5.3	1.3	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM536253QRNLRQ1	VQFN-HR	RNL	22	3000	367.0	367.0	38.0
LM536253QRNLTQ1	VQFN-HR	RNL	22	250	213.0	191.0	35.0
LM536255QRNLRQ1	VQFN-HR	RNL	22	3000	367.0	367.0	38.0
LM536255QRNLTQ1	VQFN-HR	RNL	22	250	213.0	191.0	35.0
LM53625AQRNLRQ1	VQFN-HR	RNL	22	3000	367.0	367.0	38.0
LM53625AQRNLTQ1	VQFN-HR	RNL	22	250	213.0	191.0	35.0
LM53625LQRNLRQ1	VQFN-HR	RNL	22	3000	367.0	367.0	38.0
LM53625LQRNLTQ1	VQFN-HR	RNL	22	250	213.0	191.0	35.0
LM53625LQURNLRQ1	VQFN-HR	RNL	22	3000	367.0	367.0	38.0
LM53625MQRNLRQ1	VQFN-HR	RNL	22	3000	367.0	367.0	38.0
LM53625MQRNLTQ1	VQFN-HR	RNL	22	250	213.0	191.0	35.0
LM53625MQURNLRQ1	VQFN-HR	RNL	22	3000	367.0	367.0	38.0
LM53625NQRNLRQ1	VQFN-HR	RNL	22	3000	367.0	367.0	38.0
LM53625NQRNLTQ1	VQFN-HR	RNL	22	250	213.0	191.0	35.0
LM53625NQURNLRQ1	VQFN-HR	RNL	22	3000	367.0	367.0	38.0
LM536353QRNLRQ1	VQFN-HR	RNL	22	3000	367.0	367.0	38.0
LM536353QRNLTQ1	VQFN-HR	RNL	22	250	213.0	191.0	35.0
LM536355QRNLRQ1	VQFN-HR	RNL	22	3000	367.0	367.0	38.0

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM536355QRNLTQ1	VQFN-HR	RNL	22	250	213.0	191.0	35.0
LM53635AQRNLRQ1	VQFN-HR	RNL	22	3000	367.0	367.0	38.0
LM53635AQRNLTQ1	VQFN-HR	RNL	22	250	213.0	191.0	35.0
LM53635LQRNLRQ1	VQFN-HR	RNL	22	3000	367.0	367.0	38.0
LM53635LQRNLTQ1	VQFN-HR	RNL	22	250	213.0	191.0	35.0
LM53635MQRNLRQ1	VQFN-HR	RNL	22	3000	367.0	367.0	38.0
LM53635MQRNLTQ1	VQFN-HR	RNL	22	250	213.0	191.0	35.0
LM53635MQURNLRQ1	VQFN-HR	RNL	22	3000	367.0	367.0	38.0
LM53635NQRNLRQ1	VQFN-HR	RNL	22	3000	367.0	367.0	38.0
LM53635NQRNLTQ1	VQFN-HR	RNL	22	250	213.0	191.0	35.0
LM53635NQURNLRQ1	VQFN-HR	RNL	22	3000	367.0	367.0	38.0

GENERIC PACKAGE VIEW

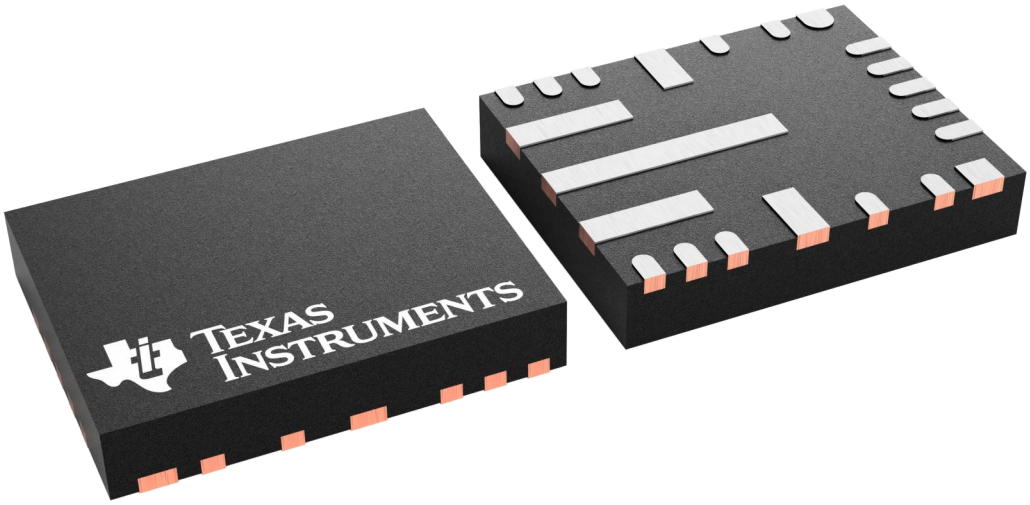
RNL 22

VQFN-HR - 1 mm max height

5 X 4, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



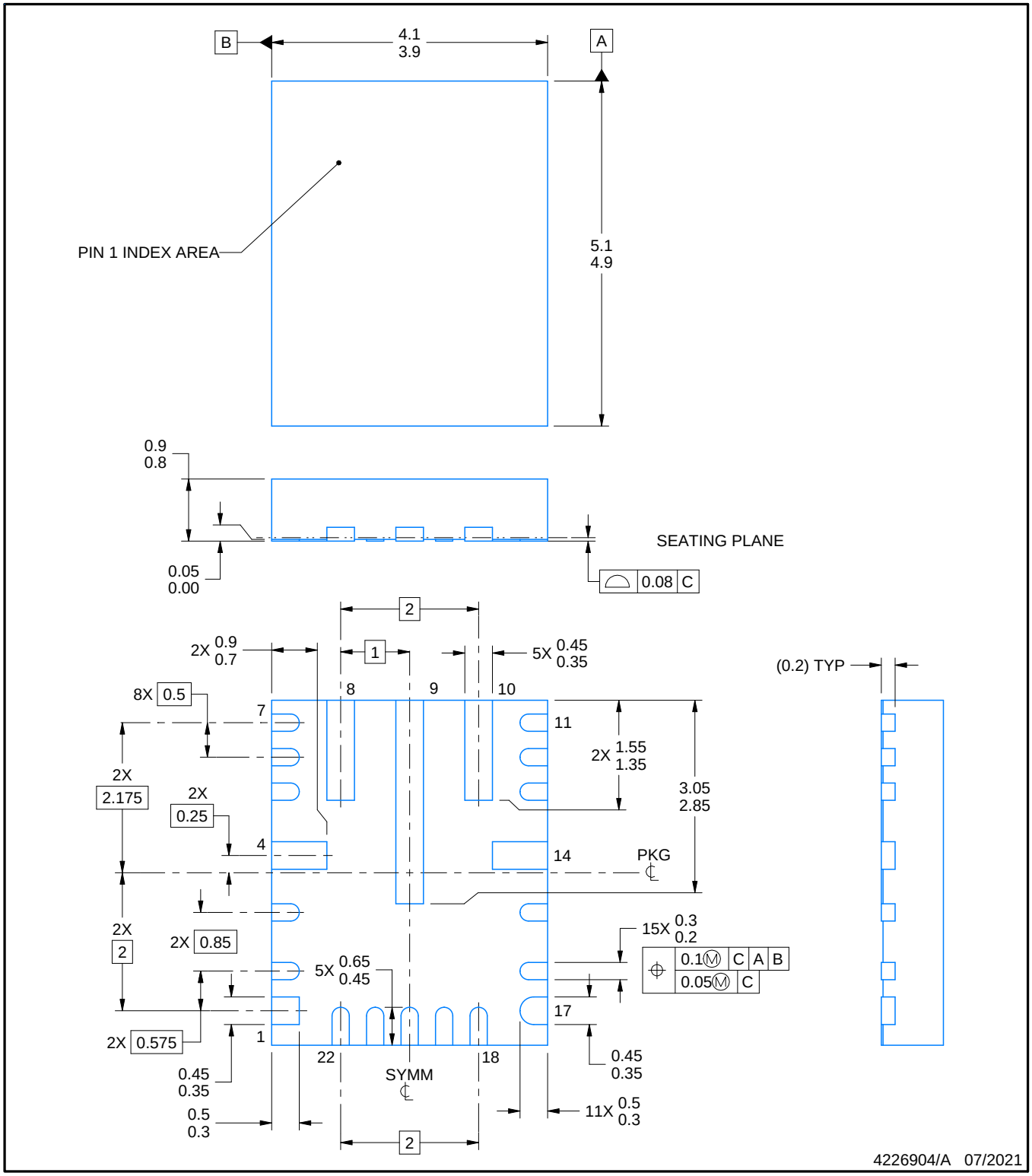
4226989/A

PACKAGE OUTLINE

RNL0022B

VQFN-HR - 0.9 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES:

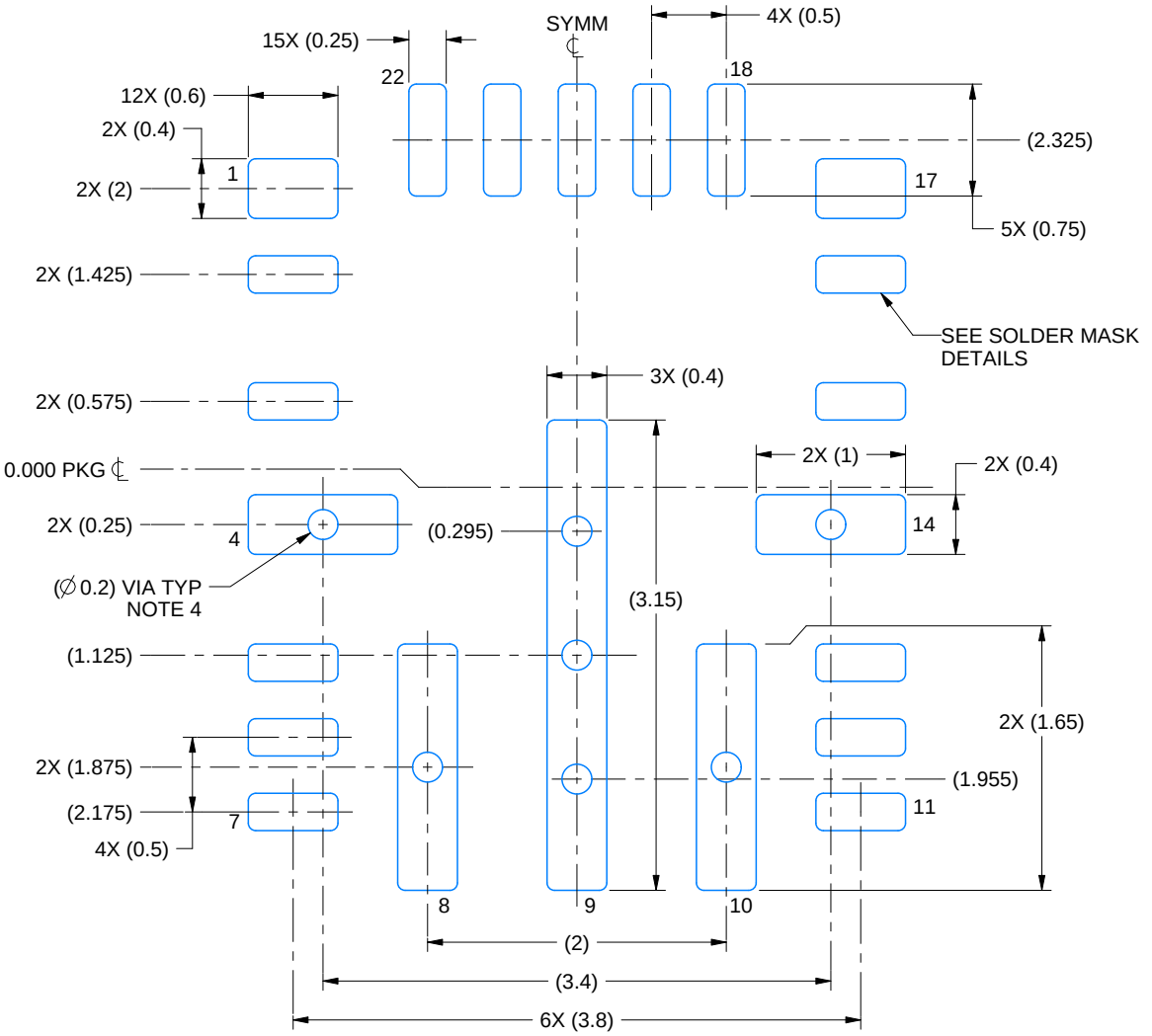
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

EXAMPLE BOARD LAYOUT

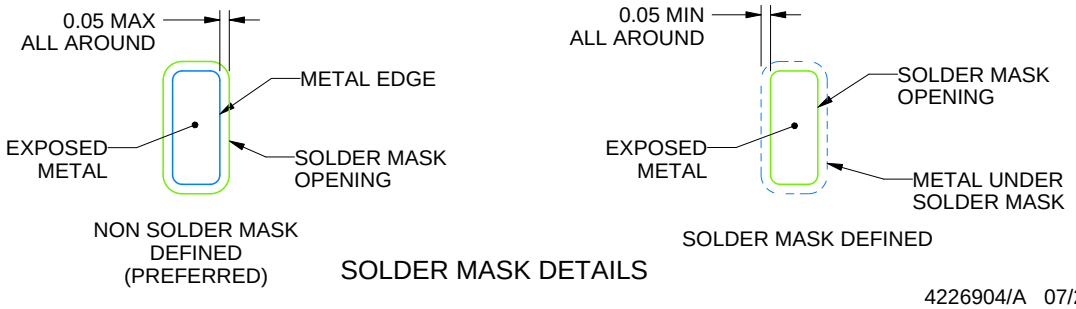
RNL0022B

VQFN-HR - 0.9 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X



SOLDER MASK DETAILS

4226904/A 07/2021

NOTES: (continued)

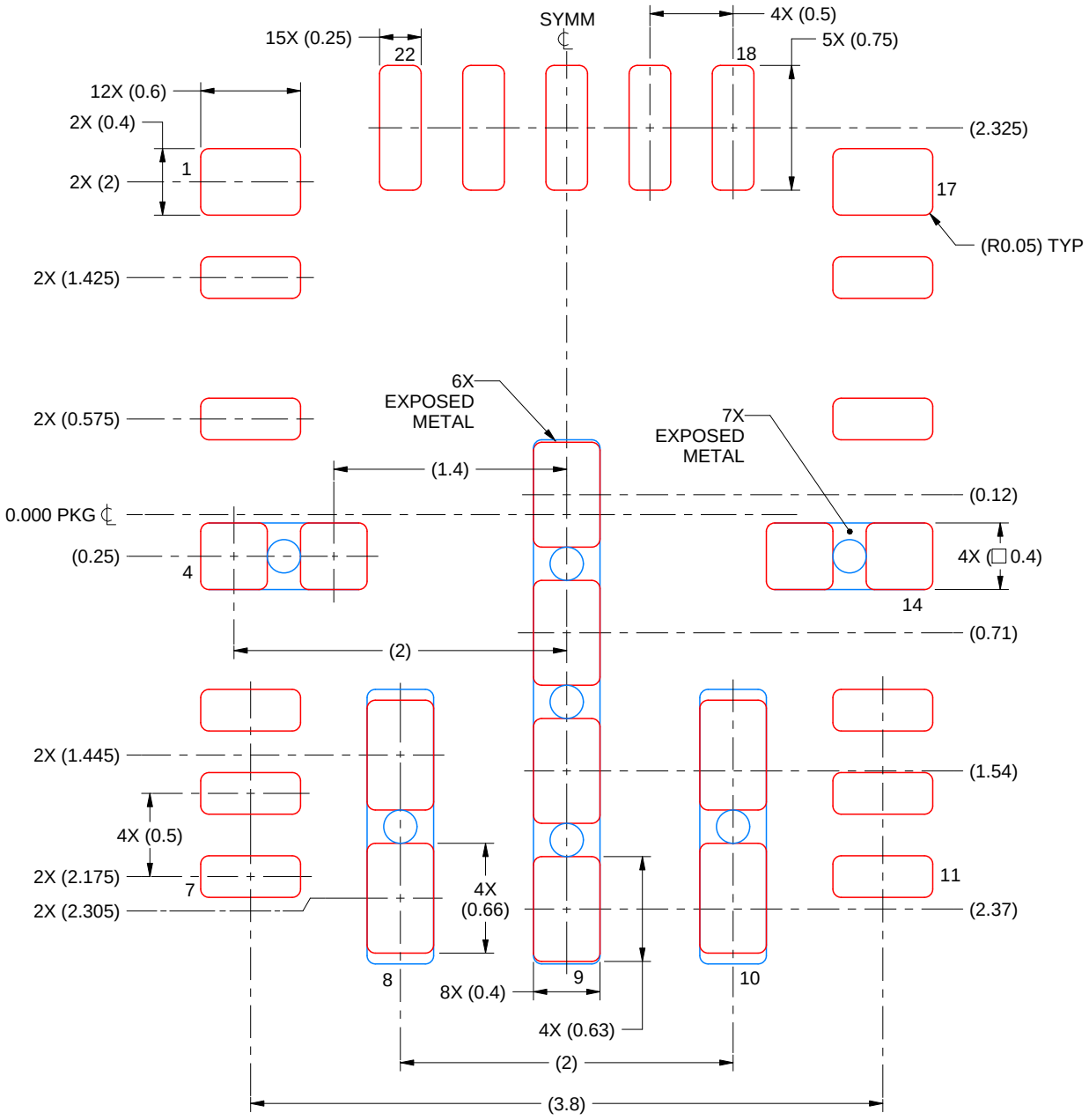
3. This package is designed to be soldered to thermal pads on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
4. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

RNL0022B

VQFN-HR - 0.9 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

FOR PADS 4,8,9,10 & 14
80% PRINTED SOLDER COVERAGE BY AREA
SCALE:25X

4226904/A 07/2021

NOTES: (continued)

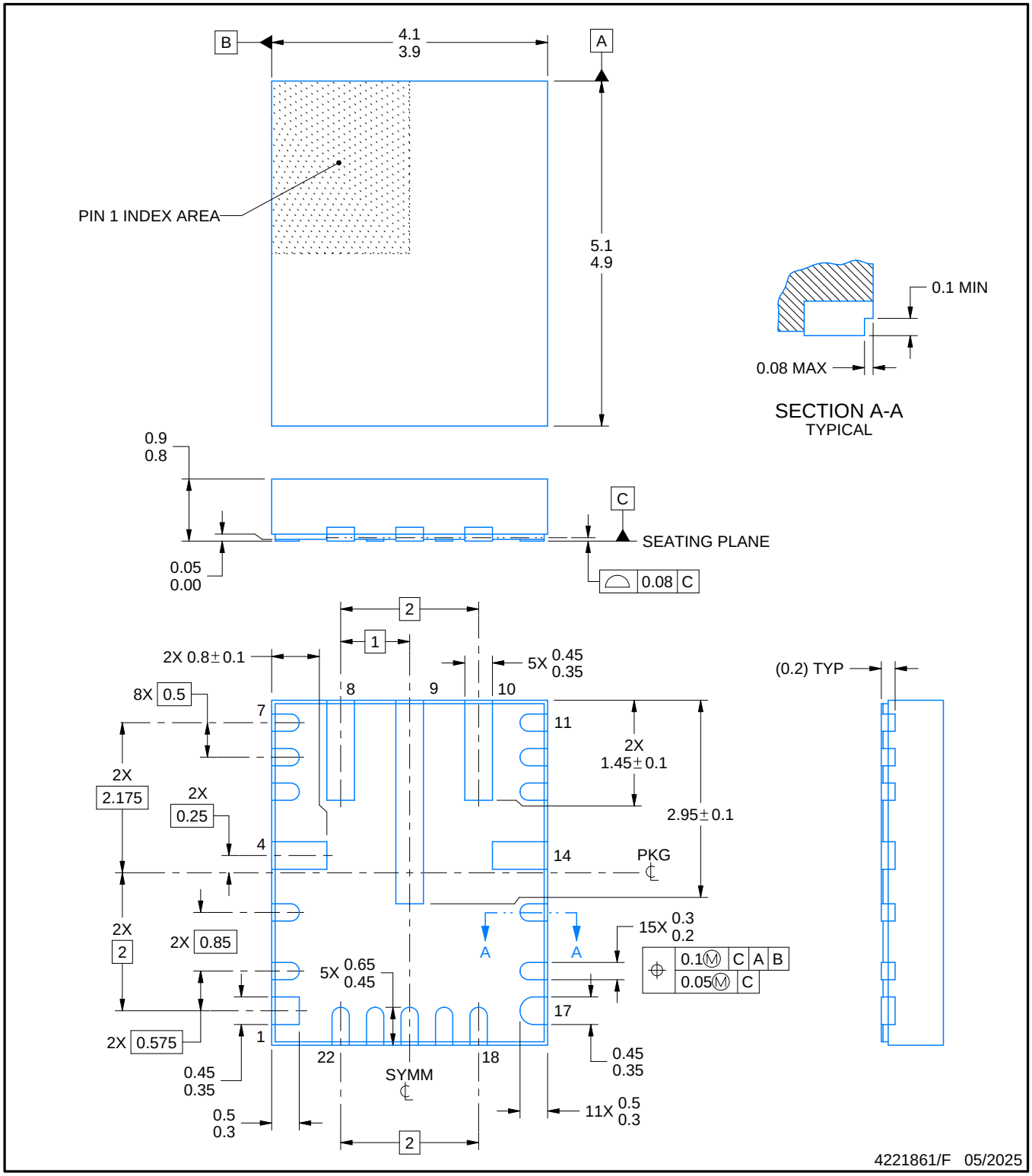
5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGE OUTLINE

RNL0022A

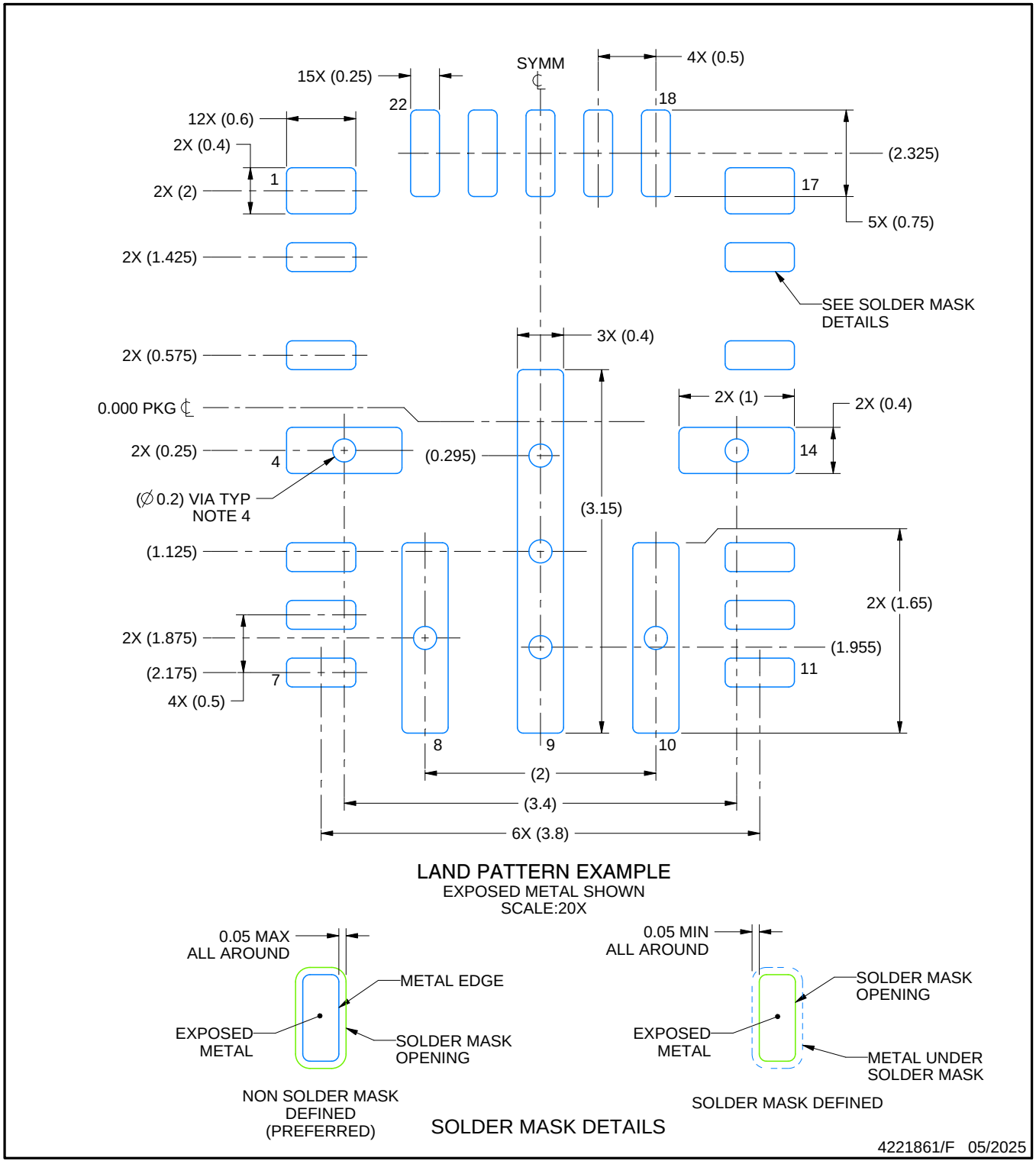
VQFN-HR - 0.9 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



NOTES: (continued)

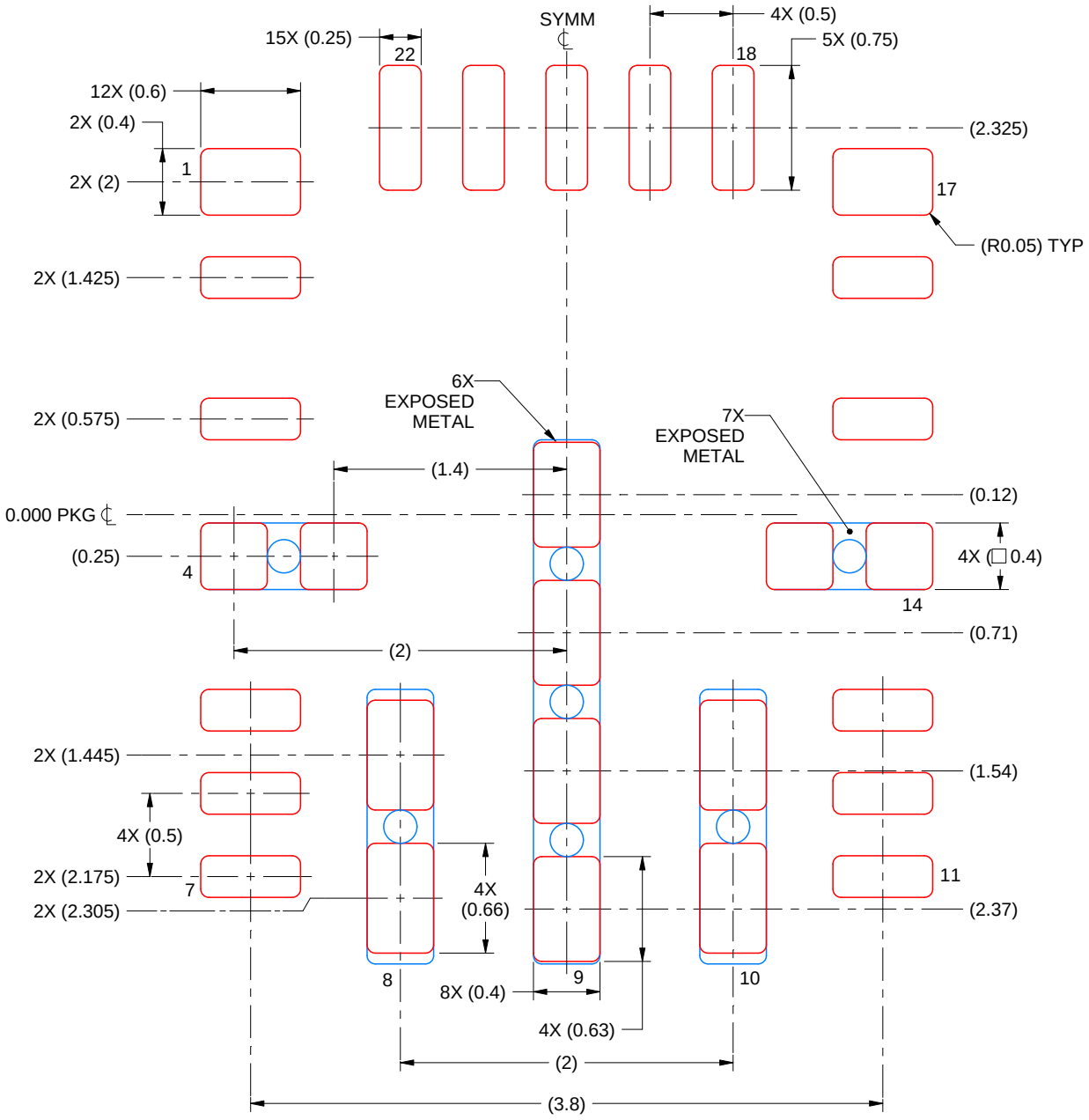
3. This package is designed to be soldered to thermal pads on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
4. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

RNL0022A

VQFN-HR - 0.9 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

FOR PADS 4,8,9,10 & 14
80% PRINTED SOLDER COVERAGE BY AREA
SCALE:25X

4221861/F 05/2025

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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最終更新日：2025 年 10 月