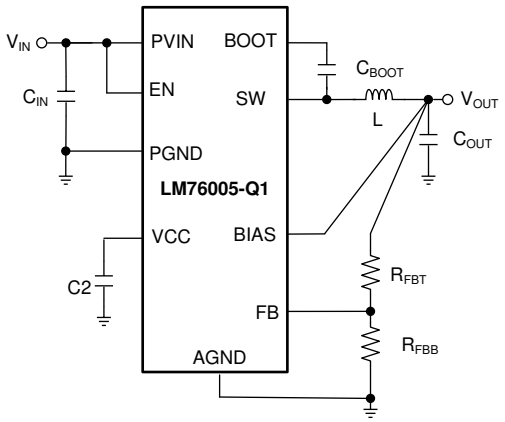
TEXAS INSTRUMENTS
LM76005-Q1
JAJSIL9A – FEBRUARY 2020 – REVISED JULY 2020

LM76005-Q1 3.5V～60V、5A の車載用同期整流降圧型コンバータ

1 特長

- 車載アプリケーション向けに AEC-Q100 認証済み
  - 温度グレード 1:–40℃～+125℃、T_A
- 機能安全対応
  - 機能安全システムの設計に役立つ資料を利用可能
- 車載用アプリケーション向けの設計
  - 最大 65V の入力過渡保護
  - 低 EMI 要件に対して最適化
  - FPWM 動作をピンで選択可能
  - 可変周波数範囲:200kHz～500kHz
  - プリバイアス出力電圧付きのスタートアップ
  - 保護機能:サーマル・シャットダウン、入力低電圧誤動作防止、サイクル単位の電流制限、ヒカップ短絡保護
- スケーラブルな電源に最適
  - 次の製品とピン互換:
    - LM76002/3-Q1 (60V、2.5A または 3.5A)
  - 出力電圧:1V から V_{IN} の 95% まで
  - 外部クロックへの同期
  - 可変ソフトスタート (デフォルト 6.3ms)
- 負荷スペクトラム全体にわたって低消費電力
  - レギュレーション時の静止電流:15µA
  - 400kHz で 95% の効率 ($12V_{IN}$、$5V_{OUT}$、2A)
  - 10mA で 92% の PFM 効率 ($12V_{IN}$、$5V_{OUT}$)
  - 外部バイアス・オプションによる効率向上
- LM76005-Q1 を使用するカスタム設計を WEBENCH® Power Designer により作成



概略回路図

2 アプリケーション

- 24V バッテリをサポートする車載用 ADAS
- インフォテインメントとクラスタ
- HEV/EV

3 概要

LM76005-Q1 レギュレータは、最高 60V の入力から最大 5A (LM76005-Q1) の負荷電流を駆動できる、使いやすい同期整流降圧型 DC-DC コンバータです。65V 許容であるため、入力サージ保護が簡単です。

LM76005-Q1 は、ピーク電流モード制御を使用して、小さいソリューション・サイズで非常に高い効率と出力精度を実現します。PWM モードと PFM モードの間のシームレスな移行、非常に小さな MOSFET ON 抵抗、外部バイアス入力により、負荷範囲全体にわたって非常に優れた効率が得られます。

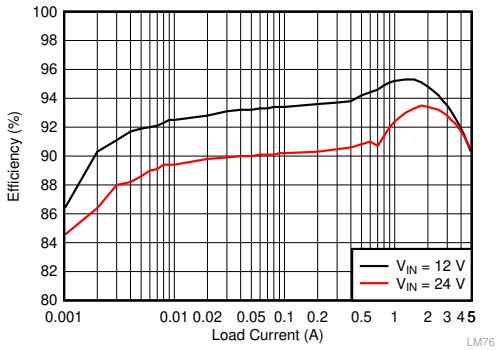
このデバイスは、必要な外付けコンポーネントが少なく、PCB レイアウトが単純になるようにピン配置が設計されており、クラス最高の EMI (CISPR25) および熱性能を実現しています。LM76005-Q1 の小さなソリューション・サイズと機能セットは、広範な最終機器を簡単に実装できるように設計されています。

LM76005-Q1 デバイスは、ウェッタブル・フランク付きの WQFN 30 ピン・リードレス・パッケージで供給されます。

製品情報

部品番号(1)	パッケージ	本体サイズ (公称)
LM76005-Q1	WQFN (30)	6.00mm × 4.00mm

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。



効率：V_{OUT} = 5V、f_{SW} = 400kHz、自動モード

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4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision * (February 2020) to Revision A (July 2020)	Page
• デバイス・ステータスを「事前情報」から「量産データ」に変更	1
• 文書全体にわたって表、図、相互参照の採番方法を更新	1

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5 Pin Configuration and Functions

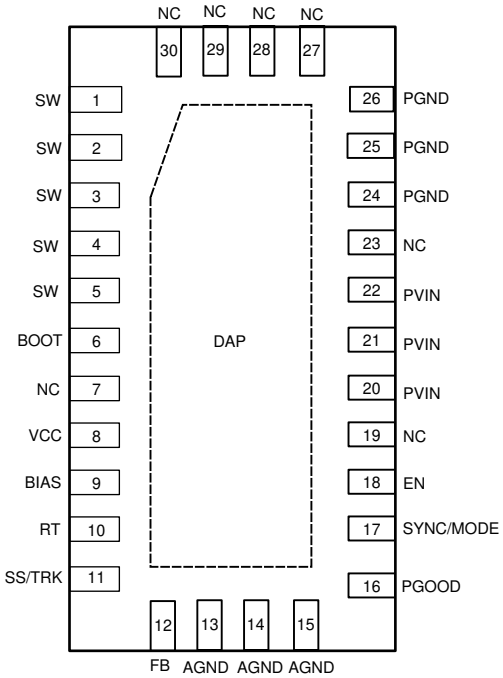


図 5-1. RNP Package 30-Pin WQFN Top View

Pin Functions

PIN		I/O(1)	DESCRIPTION
NO.	NAME		
1, 2, 3, 4, 5	SW	P	Switching output of the regulator. Internally connected to the source of the HS FET and drain of the LS FET. Connect to power inductor and bootstrap capacitor.
6	BOOT	P	Bootstrap capacitor connection for high-side driver. Connect a high-quality 470-nF capacitor from this pin to the SW pin.
7, 19, 23, 27, 28, 29, 30	NC	—	Not internally connected. Connect pins 19, 27, 28, 29, and 30 to ground copper on PCB to improve heat-sinking of the device and board level reliability. Leave pins 7 and 23 floating in order to maximize distance from the high voltage input to ground.
8	VCC	P	Output of internal bias supply. Used as supply to internal control circuits. Connect a high-quality 2.2-µF capacitor from this pin to GND. TI does not recommended loading this pin by external circuitry.
9	BIAS	P	Optional BIAS LDO supply input. TI recommends tying this to V_{OUT} when 3.3 V ≤ V_{OUT} ≤ 18 V, or tying to an external 3.3-V or 5-V rail if available, to improve efficiency. When used, place a 1-µF capacitor from this terminal to ground. Tie to ground when not in use.
10	RT	A	Switching frequency setting pin. Place a resistor from this pin to ground to set the switching frequency. If floating, the default switching frequency is 400 kHz. Do not short to ground.
11	SS/TRK	A	Soft-start control pin. Leave this pin floating to use the 6.3-ms internal soft-start ramp. An external capacitor can be connected from this pin to ground to extend the soft-start time. A 2-µA current sourced from this pin can charge the capacitor to provide the ramp. Connect to external ramp for tracking. Do not short to ground.
12	FB	A	Feedback input for output voltage regulation. Connect a resistor divider to set the output voltage. Never short this terminal to ground during operation.
16	PGOOD	A	Open-drain power-good flag output. Connect to suitable voltage supply through a current limiting resistor. High = V_{OUT} regulation OK, Low = V_{OUT} regulation fault. PGOOD = Low when EN = Low
17	SYNC/MODE	A	Synchronization input and mode setting pin. Do not float, tie to ground if not used. Tie to ground: DCM/PFM operation under light loads, improved efficiency Tie to logic high: forced PWM under light loads, constant switching frequency over load Tie to external clock source: synchronize switching action to the clock, forced PWM under light loads. Triggers on the rising edge of external clock.
18	EN	A	Precision-enable input to regulator. Do not float. High = on, Low = off. Can be tied to V_{IN}. Precision-enable input allows adjustable UVLO by external resistor divider.
13, 14, 15	AGND	G	Analog ground. Ground reference for internal references and logic. All electrical parameters are measured with respect to this pin. Connect to system ground on PCB.
20, 21, 22	PVIN	P	Supply input to internal bias LDO and HS FET. Connect to input supply and input bypass capacitors C_{IN}. C_{IN} must be placed right next to this pin and PGND and connected with short traces.
24, 25, 26	PGND	G	Power ground, connected to the source of LS FET internally. Connect to system ground, DAP/EP, AGND, and ground side of C_{IN} and C_{OUT}. Path to C_{IN} must be as short as possible.
EP	DAP	—	Low impedance connection to AGND. Connect to system ground on PCB. Major heat dissipation path for the die. Must be used for heat sinking by soldering to ground copper on PCB. Thermal vias are preferred.

(1) A = Analog, O = Output, I = Input, G = Ground, P = Power

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6 Specifications

6.1 Absolute Maximum Ratings

Over operating free-air temperature range of –40°C to +125°C (unless otherwise noted)(1)

	PARAMETER	MIN	MAX	UNIT
Input voltages	PVIN to PGND	–0.3	65	V
	EN to AGND	–0.3	V_{IN} + 0.3	
	FB, RT, SS/TRK to AGND	–0.3	5	
	PGOOD to AGND	–0.1	20	
	SYNC to AGND	–0.3	5.5	
	BIAS to AGND	–0.3	Lower of (V_{IN} + 0.3) or 30	
	AGND to PGND	–0.3	0.3	
Output voltages	SW to PGND	–0.3	V_{IN} + 0.3	V
	SW to PGND less than 10-ns transients	–3.5	65	
	BOOT to SW	–0.3	5.5	
	VCC to AGND	–0.3	5.5	
Junction temperature, T_J		–40	150	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002(1)	±2000	V
		Charged-device model (CDM), per AEC Q100-011	±500	V

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification

6.3 Recommended Operating Conditions

Over the recommended operating junction temperature range of -40°C to 125°C (unless otherwise noted)(1)

		MIN	MAX	UNIT
Input voltages	PVIN to PGND	3.5	60	V
	EN	0	V_{IN}	
	FB	0	4.5	
	PGOOD	0	18	
	BIAS input not used	0	0.3	
	BIAS input used	0	Lower of (V_{IN} + 0.3) or 24	
	AGND to PGND	–0.1	0.1	
Switching Frequency	F_{SW}	200	500	kHz
Output voltage	V_{OUT}	1	95% of V_{IN}	V
Output current	I_{OUT}	0	5	A
Temperature	Operating junction temperature, T_J	–40	125	°C

(1) Recommended operating rating indicate conditions for which the device is intended to be functional, but do not ensure specific performance limits. For ensured specifications, see Electrical Characteristics Table.

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6.4 Thermal Information

THERMAL METRIC[1]		LM76005-Q1 RNP (WQFN) 30 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	29.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	17.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	9.1	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	9.0	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	1.0	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

6.5 Electrical Characteristics

Limits apply over the recommended operating junction temperature (T_J) range of –40°C to +125°C, unless otherwise stated. Minimum and maximum limits are specified through test, design or statistical correlation. Typical values represent the most likely parametric norm at T_J = 25°C, and are provided for reference purposes only. Unless otherwise stated, the following conditions apply: V_{IN} = 24 V, V_{OUT} = 3.3 V, f_{SW} = 400 kHz.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY VOLTAGE (PVIN PINS)						
V_{IN}	Operating input voltage range		3.5		60	V
I_{SD}	Shutdown quiescent current; measured at PVIN pin[1]	V_{EN} = 0 V		1.2	10	µA
I_{Q_NONSW}	Operating quiescent current from V_{IN} (non-switching)	V_{EN} = 2 V, V_{FB} = 1.5 V, V_{BIAS} = 3.3 V external		2	12	µA
ENABLE (EN PIN)						
$V_{EN_VCC_H}$	Enable input high level for V_{CC} output	V_{EN} rising			1.2	V
$V_{EN_VCC_L}$	Enable input low level for V_{CC} output	V_{EN} falling	0.3			V
$V_{EN_VOUT_H}$	Enable input high level for V_{OUT}	V_{EN} rising	1.14	1.204	1.25	V
$V_{EN_VOUT_HYS}$	Enable input hysteresis for V_{OUT}	V_{EN} falling hysteresis		–150		mV
I_{LKG_EN}	Enable input leakage current	V_{EN} = 2 V		1.4	200	nA
INTERNAL LDO (VCC PIN, BIAS PIN)						
V_{CC}	Internal V_{CC} voltage	PWM operation		3.29		V
		PFM operation		3.1		V
V_{CC_UVLO}	Internal V_{CC} undervoltage lockout	V_{CC} rising	2.96	3.14	3.27	V
		V_{CC} falling hysteresis		–565		mV
V_{BIAS_ON}	Input change over	V_{BIAS} rising		3.11	3.25	V
		V_{BIAS} falling hysteresis		–63		mV
I_{BIAS_NONSW}	Operating quiescent current from external V_{BIAS} (non-switching)	V_{EN} = 2 V, V_{FB} = 1.5 V, V_{BIAS} = 3.3 V external		21	50	µA
VOLTAGE REFERENCE (FB PIN)						
V_{FB}	Feedback voltage	PWM mode	0.987	1.006	1.017	V
I_{LKG_FB}	Input leakage current at FB pin	V_{FB} = 1 V		0.2	60	nA

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Limits apply over the recommended operating junction temperature (T_J) range of –40°C to +125°C, unless otherwise stated. Minimum and maximum limits are specified through test, design or statistical correlation. Typical values represent the most likely parametric norm at T_J = 25°C, and are provided for reference purposes only. Unless otherwise stated, the following conditions apply: V_{IN} = 24 V, V_{OUT} = 3.3 V, f_{SW} = 400 kHz.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
HIGH SIDE DRIVER (BOOT PIN)						
V_{BOOT_UVLO}	BOOT - SW undervoltage lockout		1.6	2.2	2.7	V
CURRENT LIMITS AND HICCUP						
I_{HS_LIMIT} (2)	Short-circuit, high-side current limit		6.0	6.8	7.8	A
I_{LS_LIMIT} (2)	Low-side current limit		4.5	5.1	5.8	A
I_{NEG_LIMIT}	Negative current limit			–4.1		A
V_{HICCUP}	Hiccup threshold on FB pin		0.38	0.42	0.46	V
I_{L_ZC}	Zero cross-current limit			0.05		A
SOFT START (SS/TRK PIN)						
I_{SSC}	Soft-start charge current		1.8	2	2.2	µA
R_{SSD}	Soft-start discharge resistance	UVLO, TSD, OCP; or EN = 0 V		2		kΩ
POWER GOOD (PGOOD PIN) and OVERVOLTAGE PROTECTION						
V_{PGOOD_OV}	Power-good overvoltage threshold	% of FB voltage	106%	110%	113%	
V_{PGOOD_UV}	Power-good undervoltage threshold	% of FB voltage	86%	90%	93%	
V_{PGOOD_HYS}	Power-good hysteresis	% of FB voltage		2.5%		
V_{PGOOD_VALID}	Minimum input voltage for proper PGOOD function	50-µA pullup to PGOOD pin, V_{EN} = 0 V		1.3	2	V
R_{PGOOD}	Power-good on-resistance	V_{EN} = 2.5 V		40	100	Ω
		V_{EN} = 0 V		30	90	
MOSFETS						
$R_{DS_ON_HS}$ (3)	High-side MOSFET on-resistance	I_{OUT} = 1 A, V_{BIAS} = V_{OUT} = 3.3 V		95	150	mΩ
$R_{DS_ON_LS}$ (3)	Low-side MOSFET on-resistance	I_{OUT} = 1 A, V_{BIAS} = V_{OUT} = 3.3 V		45	85	mΩ
THERMAL SHUTDOWN						
T_{SD} (4)	Thermal shutdown threshold	Shutdown threshold		150		°C
	Recovery threshold			135		°C

(1) Shutdown current includes leakage current of the switching transistors.
(2) This current limit was measured as the internal comparator trip point. Due to inherent delays in the current limit comparator and drivers, the peak current limit measured in closed loop with faster slew rate will be larger, and valley current limit will be lower.
(3) Measured at pins.
(4) Ensured by design.

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6.6 Timing Characteristics

			MIN	NOM	MAX	UNIT
CURRENT LIMITS AND HICCUP						
N_{OC} (1)	Number of switching cycles before hiccup is tripped			128		Cycles
t_{OC}	Overcurrent hiccup retry delay time			46		ms
SOFT START (SS/TRK PIN)						
t_{SS}	Internal soft-start time	CSS = OPEN, from EN rising edge to PGOOD rising edge	3.5	6.3		ms
POWER GOOD (PGOOD PIN) and OVERVOLTAGE PROTECTION						
t_{PGOOD_RISE}	PGOOD rising edge deglitch delay		80	140	200	µs
t_{PGOOD_FALL}	PGOOD falling edge deglitch delay		80	140	200	µs

(1) Ensured by design

6.7 Switching Characteristics

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
PWM LIMITS (SW PINS)						
t_{ON-MIN}	Minimum switch on-time			65	95	ns
$t_{OFF-MIN}$	Minimum switch off-time			95	130	ns
t_{ON-MAX}	Maximum switch on-time	HS timeout in dropout	3.8	8	11.4	µs
OSCILLATOR (RT and SYNC PINS)						
f_{ADJ}	Adjustable frequency by R_T or SYNC	R_T =133 kΩ, 0.1%	270	300	330	kHz
f_{OSC}	Internal oscillator frequency	R_T = Open	350	400	450	kHz
V_{SYNC_HIGH}	Sync input high level threshold				2	V
V_{SYNC_LOW}	Sync input low level threshold		0.4			V
V_{MODE_HIGH}	Mode input high level threshold for FPWM			0.42		V
V_{MODE_LOW}	Mode input low level threshold for AUTO mode			0.4		V
t_{SYNC_MIN}	Sync input minimum on- and off-time			80		ns

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6.8 System Characteristics

The following specifications apply to the circuit found in the typical application schematic with appropriate modifications. These parameters are not tested in production and represent typical performance only. Unless otherwise stated the following conditions apply: T_A = 25°C, V_{IN} = 24 V, V_{OUT} = 3.3 V, f_{SW} = 400 kHz.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{FB_PFM}	Output voltage offset at no load in auto mode	V_{IN} = 3.8 V to 36 V, V_{SYNC} = 0 V, auto mode I_{OUT} = 0 A		2%		
V_{drop}	Minimum input to output voltage differential to maintain specified accuracy	V_{OUT} = 5 V, I_{OUT} = 1.5 A, f_{SW} = 400 kHz		0.65		V
I_{Q_SW}	Operating quiescent current (switching)	V_{EN} = 3.3 V, I_{OUT} = 0 A, R_T = open, V_{BIAS} = V_{OUT} = 3.3 V, R_{FBT} = 1 Meg		15		µA
I_{PEAK_MIN}	Minimum inductor peak current	V_{SYNC} = 0 V, I_{OUT} = 10 mA		1		A
I_{BIAS_SW}	Operating quiescent current from external V_{BIAS} (switching)	f_{SW} = 400 kHz, I_{OUT} = 1 A		7		mA
D_{MAX}	Maximum switch duty cycle	While in frequency foldback	97.5%			
t_{DEAD}	Dead time between high-side and low-side MOSFETs			4		ns

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6.9 Typical Characteristics

Unless otherwise specified, V_{IN} = 24 V. Curves represent most likely parametric norm at specified condition.

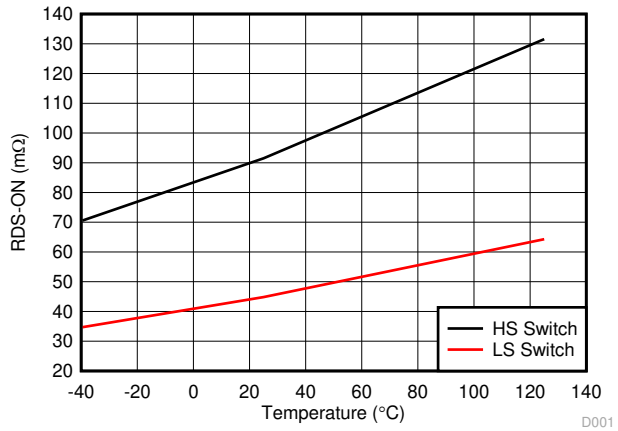


図 6-1. High-Side and Low-Side Switch R_{DS-ON}

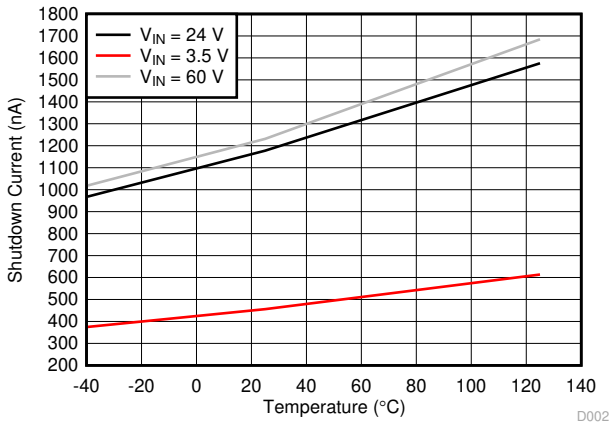


図 6-2. Shutdown Quiescent Current

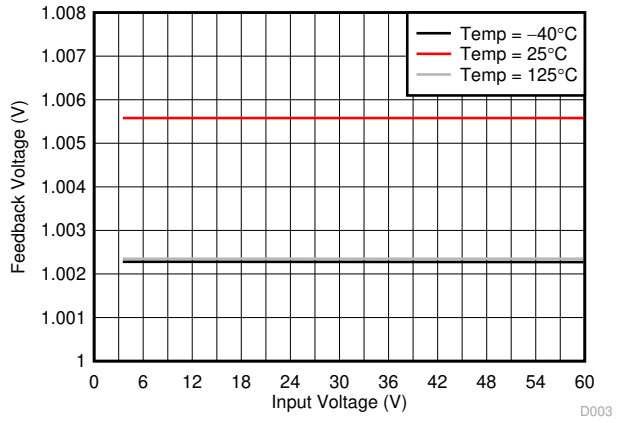


図 6-3. Feedback Voltage

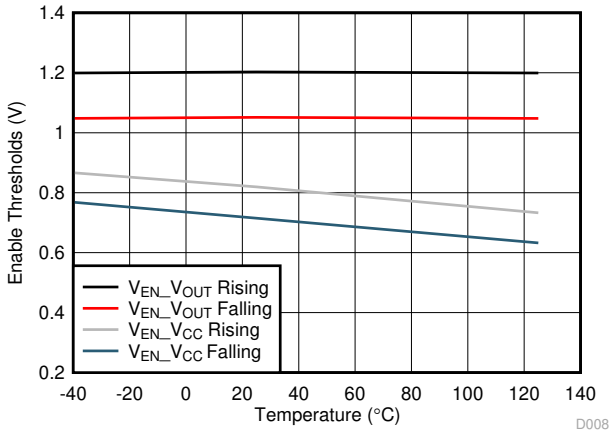


図 6-4. Enable Threshold

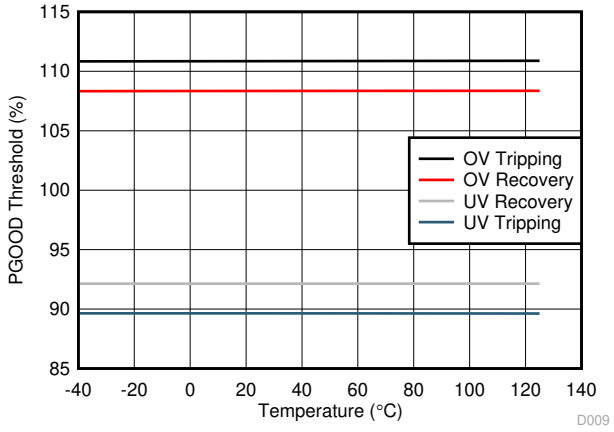


図 6-5. PGOOD Threshold

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7 Detailed Description

7.1 Overview

The LM76005-Q1 regulator is an easy-to-use synchronous step-down DC-DC converter that operates from 3.5-V to 60-V supply voltage. The device is capable of delivering up to 5-A DC load current with exceptional efficiency and thermal performance in a very small solution size.

The LM76005-Q1 employs fixed-frequency peak-current-mode control with configurable discontinuous conduction mode (DCM) and pulse frequency modulation (PFM) mode at light loads to achieve high efficiency across the load range. The device can also be configured as forced-PWM (FPWM) operation to keep constant switching frequency over the load range. The device is internally compensated, which reduces design time and requires fewer external components. The switching frequency is programmable from 200 kHz to 500 kHz by an external resistor. The LM76005-Q1 is also capable of synchronization to an external clock operating within the 200-kHz to 500-kHz frequency range. The wide switching frequency range allows the device to meet a wide range of design requirements. It can be optimized for a very small solution size with higher frequency or for very high efficiency with lower switching frequency. It has very small minimum HS MOSFET on-time (t_{ON-MIN}) and minimum off-time ($t_{OFF-MIN}$) to provide wide range of voltage conversion. Automated frequency foldback is employed under t_{ON-MIN} or $t_{OFF-MIN}$ condition to further extend the operation range.

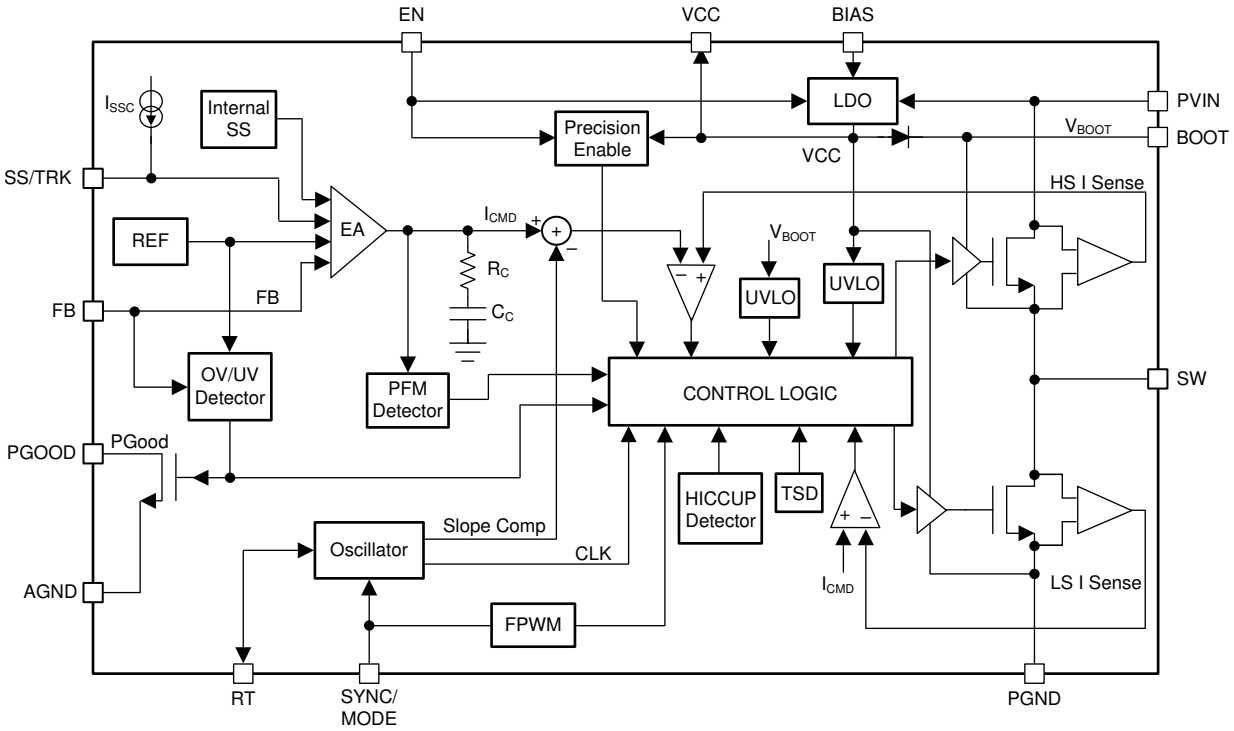
The LM76005-Q1 also features the following:

- A power-good (PGOOD) flag
- Precision enable
- Internal or adjustable soft-start rate
- Start-up with pre-bias voltage
- Output voltage tracking

It provides a flexible and easy-to-use solution for wide range of applications. Protection features include thermal shutdown, V_{CC} undervoltage lockout, cycle-by-cycle current limiting, and short-circuit hiccup protection.

The family requires very few external components and has a pinout designed for simple, optimum PCB layout for EMI and thermal performance. The LM76005-Q1 device is available in a 30-pin WQFN lead-less package.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Fixed-Frequency, Peak-Current-Mode Control

The following operation description of the LM76005-Q1 refers to セクション 7.2 and to the waveforms in 図 7-1. The LM76005-Q1 supplies a regulated output voltage by turning on the internal high-side (HS) and low-side (LS) NMOS switches with varying duty cycle (D). During high-side switch on-time, t_{ON}, the SW pin voltage V_{SW} swings up to approximately V_{IN}, and the inductor current, i_L, increases with linear slope. The HS switch is turned off by the control logic. During the HS switch off-time, t_{OFF}, the LS switch is turned on. Inductor current discharges through the LS switch, which forces the V_{SW} to swing below ground by the voltage drop across the LS switch. The regulator loop adjusts the duty cycle to maintain a constant output voltage. The control parameter of a buck converter is defined as duty cycle $D = t_{ON} / T_{SW}$. In an ideal buck converter, where losses are ignored, D is proportional to the output voltage and inversely proportional to the input voltage: $D = V_{OUT} / V_{IN}$.

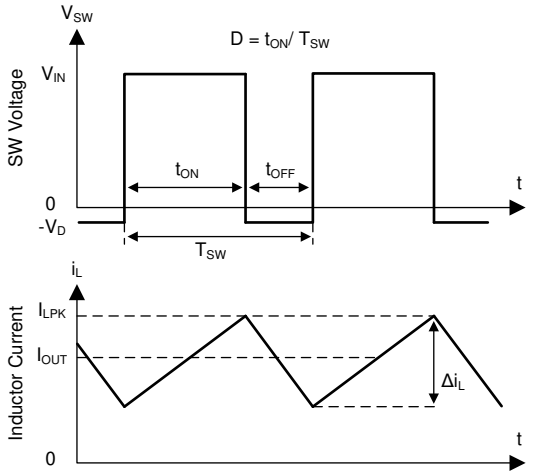


図 7-1. SW Node and Inductor Current Waveforms in Continuous Conduction Mode

The LM76005-Q1 synchronous buck converter employs peak current-mode control topology. A voltage-feedback loop is used to get accurate DC-voltage regulation by adjusting the peak current command based on voltage offset. The peak inductor current is sensed from the HS switch and compared to the peak current to control the on-time of the HS switch. The voltage feedback loop is internally compensated, which allows for fewer external components, makes it easy to design, and provides stable operation with almost any combination of output capacitors. The regulator operates with fixed switching frequency in continuous conduction mode (CCM) and discontinuous conduction mode (DCM). At very light load, the LM76005-Q1 operates in PFM to maintain high efficiency, and the switching frequency decreases with reduced load current.

7.3.2 Light Load Operation Modes — PFM and FPWM

DCM operation is employed in the LM76005-Q1 when the inductor current valley reaches zero. The LM76005-Q1 is in DCM when load current is less than half of the peak-to-peak inductor current ripple in CCM. In DCM, the LS switch is turned off when the inductor current reaches zero. Switching loss is reduced by turning off the LS FET at zero current, and the conduction loss is lowered by not allowing negative current conduction. Power conversion efficiency is higher in DCM than CCM under the same conditions.

In DCM, the HS switch on-time reduces with lower load current. When either the minimum HS switch on-time (t_{ON-MIN}) or the minimum peak inductor current ($I_{PEAK-MIN}$) is reached, the switching frequency decreases to maintain regulation. At this point, the LM76005-Q1 operates in PFM. In PFM, switching frequency is decreased by the control loop when load current reduces to maintain output voltage regulation. Reference the セクション 8.2.3 for typical steady state switching behavior in PFM. Switching loss is further reduced in PFM operation due to less frequent switching actions.

In PFM operation, a small positive DC offset is required at the output voltage to activate the PFM detector. The lower the frequency is in PFM, the more DC offset is needed at V_{OUT}. See セクション 6.9 for typical DC offset at very light load. If the DC offset on V_{OUT} is not acceptable for a given application, TI recommends a static load at

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output to reduce or eliminate the offset. Lowering values of the feedback divider R_{FBT} and R_{FBB} can also serve as a static load. In conditions with low V_{IN} and high frequency, the LM76005-Q1 may not enter PFM mode if the output voltage cannot be charged up to provide the trigger to activate the PFM detector. Once the LM76005-Q1 is operating in PFM mode at higher V_{IN}, it remains in PFM operation when V_{IN} is reduced.

Alternatively, the device can run in a forced pulse-width-modulation (FPWM) mode where the switching frequency does not lower with load, and no offset is added to affect the V_{OUT} accuracy unless the minimum on-time of the converter is reached.

7.3.3 Adjustable Output Voltage

The voltage regulation loop in the LM76005-Q1 regulates the FB voltage to be the same as the internal reference voltage. The output voltage of the LM76005-Q1 is set by a resistor divider to program the ratio from V_{OUT} to V_{FB}. The resistor divider is connected from the output node to ground with the mid-point connecting to the FB pin.

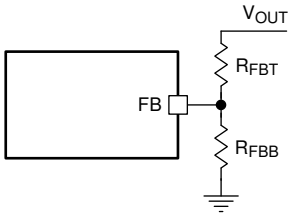


図 7-2. Output Voltage Setting

The voltage reference system produces a precise ±1% voltage reference over temperature. TI recommends using divider resistors with 1% tolerance or better with temperature coefficient of 100 ppm or lower. Selection of R_{FBT} equal or lower than 100 kΩ is also recommended. R_{FBB} can be calculated by 式 1:

$$R_{FBB} = \frac{V_{FB}}{V_{OUT} - V_{FB}} R_{FBT} \quad (1)$$

Larger R_{FBT} and R_{FBB} values reduce the current that goes through the divider, helping to increase light load efficiency. However, larger values also make the feedback path more susceptible to noise. If efficiency at very light load is not critical in a certain application, TI recommends R_{FBT} = 10 kΩ to 100 kΩ. If the resistor divider is not connected properly, output voltage cannot be regulated because the feedback loop is broken. If the FB pin is shorted to ground or disconnected, the output voltage is driven close to V_{IN} because the regulator detects very low voltage on the FB node. The load connected to V_{OUT} can be damaged in this case. It is important to route the feedback trace away from the noisy area of the PCB. For more layout recommendations, see *セクション 10*.

The minimum output voltage achievable equals V_{FB}, with R_{FBB} open. The maximum V_{OUT} is limited by the maximum duty cycle at a given frequency:

$$D_{MAX} = 1 - (t_{OFF_MIN} / T_{SW}) \quad (2)$$

where

- t_{OFF_MIN} is the minimum off-time of the HS switch
- $T_{SW} = 1 / f_{SW}$ is the switching period

Ideally, without frequency foldback, $V_{OUT_MAX} = V_{IN_MIN} \times D_{MAX}$

Maximum output voltage with frequency foldback can be estimated using Equation 3:

$$V_{OUT_MAX} = V_{IN_MIN} \times \frac{t_{ON_MAX}}{t_{ON_MAX} + t_{OFF_MIN}} - I_{OUT} \times \left(R_{DS_ON_HS} + DCR\right) \quad (3)$$

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7.3.4 Enable (EN Pin) and UVLO

System UVLO by EN and V_{CC_UVLO} voltage on the EN pin (V_{EN}) controls the ON/OFF functionality of the LM76005-Q1. Applying a voltage less than 0.3 V to the EN input shuts down the operation of the LM76005-Q1. In shutdown mode, the quiescent current drops to typically 1.2 µA at V_{IN} = 24 V.

The internal LDO output voltage V_{CC} is turned on when V_{EN} is higher than 1.2 V. The LM76005-Q1 switching action and output regulation are enabled when V_{EN} is greater than 1.204 V (typical). The LM76005-Q1 supplies regulated output voltage when enabled and output current up to 5 A. The EN pin is an input and cannot be open circuit or floating. The simplest way to enable the operation of the LM76005-Q1 is to connect the EN pin to PVIN pins directly. This allows self-start-up of the LM76005-Q1 when V_{IN} is within the operation range.

Many applications can benefit from the employment of an enable divider R_{ENT} and R_{ENB} (see 図 7-3) to establish a precision system UVLO level for the stage. System UVLO can be used for supplies operating from utility power as well as battery power. It can be used for sequencing, ensuring reliable operation, or supply protection, such as a battery. An external logic signal can also be used to drive EN input for system sequencing and protection.

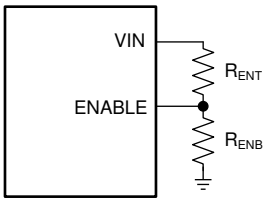


図 7-3. V_{IN} UVLO

With a selected R_{ENT}, the R_{ENB} can be calculated by:

$$R_{ENB} = \frac{V_{EN_VOUT_H} \times R_{ENT}}{V_{IN_ON_H} - V_{EN_VOUT_H}} \quad (4)$$

where

- $V_{IN_ON_H}$ is the desired supply voltage threshold to turn on this device
- $V_{EN_VOUT_H}$ can be taken from device data sheet

Note that the divider adds to supply quiescent current by V_{IN} / (R_{ENT} + R_{ENB}). Small R_{ENT} and R_{ENB} values add more quiescent current loss. However, large divider values make the node more sensitive to noise. R_{ENT} in the hundreds of kΩ range is a good starting point.

7.3.5 Internal LDO, VCC UVLO, and Bias Input

The LM76005-Q1 has an internal LDO generating VCC voltage for control circuitry and MOSFET drivers. The nominal voltage for VCC is 3.29 V. The VCC pin must have a 1-µF to 4.7-µF bypass capacitor placed as close as possible to the pin and properly grounded. Do not load or short the VCC pin to ground during operation. Shorting the VCC pin to ground during operation can damage the device.

A UVLO prevents the LM76005-Q1 from operating until the VCC voltage exceeds V_{CC_UVLO}. The V_{CC_UVLO} threshold is 3.14 V and has approximately 565 mV of hysteresis, so the device operates until V_{CC} drops below 2.575 V (typical). Hysteresis prevents the device from turning off during power up if V_{IN} droops due to input current demands.

The LDO can generate V_{CC} from two inputs: the supply voltage V_{IN} and the BIAS input. The LDO power loss is calculated by I_{LDO} × (V_{INLDO} – V_{OUTLDO}). The higher the difference between the input and output voltages of the LDO, the more losses occur to supply the same LDO output current. The BIAS input is designed to reduce the difference of the input and output voltages of the LDO to improve efficiency, especially at light load. TI recommends tying the BIAS pin to V_{OUT} when the output voltage is equal to or greater than 3.3 V and less than 18 V. Tie the BIAS pin to ground for applications less than 3.3 V or greater than 18 V. BIAS can also tie to external voltage source if available to improve efficiency. When used, TI recommends a 1-µF to 10-µF high-quality ceramic capacitor be used to bypass the BIAS pin to ground. If there is high-frequency noise or voltage

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spikes present on V_{OUT} (during transient events or fault conditions), TI recommends connecting a resistor (1 to 10 Ω) between V_{OUT} and BIAS.

The V_{CC} voltage is typically 3.29 V. When the LM76005-Q1 is operating in PFM mode with frequency foldback, V_{CC} voltage is reduced to 3.1 V (typical) to further decrease the quiescent current and improve efficiency at very light loads.

7.3.6 Soft Start and Voltage Tracking (SS/TRK)

The LM76005-Q1 has a flexible and easy-to-use start-up rate control pin: SS/TRK. The soft-start feature prevents inrush current from impacting the LM76005-Q1 and its supply when power is first applied. Soft start is achieved by slowly ramping up the target regulation voltage when the device is first enabled or powered up. The simplest way to use the device is to leave the SS/TRK pin open circuit or floating. The LM76005-Q1 employs the internal soft-start control ramp and starts up to the regulated output voltage in 6.3 ms typically. In applications with a large amount of output capacitors, higher V_{OUT}, or other special requirements, the soft-start time can be extended by connecting an external capacitor, C_{SS}, from SS/TRK pin to AGND. Extended soft-start time further reduces the supply current required to charge up output capacitors and supply any output loading. An internal current source (I_{SSC} = 2.2 µA) charges C_{SS} and generates a ramp from 0 V to V_{FB} to control the ramp-up rate of the output voltage. For a desired soft-start time t_{SS}, the capacitance for C_{SS} can be found by Equation 5:

$$C_{SS} = I_{SSC} \times t_{SS} \quad (5)$$

where

- C_{SS} = soft-start capacitor value (µF)
- I_{SSC} = soft-start charging current (µA)
- t_{SS} = desired soft-start time (s)

The soft-start capacitor C_{SS} is discharged by an internal FET when V_{OUT} is shut down by hiccup protection or ENABLE = logic low. When a large C_{SS} is applied, and EN is toggled low only for a short period of time, C_{SS} may not be fully discharged. The next soft-start ramp follows internal soft-start ramp before reaching the leftover voltage on C_{SS} and then follows the ramp programmed by C_{SS}. If this is not acceptable for a certain application, an R-C low-pass filter can be added to EN to slow down the shutting down of VCC, allowing more time to discharge C_{SS}.

The LM76005-Q1 is capable of start-up into pre-biased output conditions. When the inductor current reaches zero, the LS switch is turned off to avoid negative current conduction. This operation mode is also called diode emulation mode. It is built-in by the DCM operation in light loads. With a pre-biased output voltage, the LM76005-Q1 waits until the soft-start ramp allows regulation above the pre-biased voltage and then follows the soft-start ramp to the regulation level. When an external voltage ramp is applied to the SS/TRK pin, the LM76005-Q1 FB voltage follows the ramp if the ramp magnitude is lower than the internal soft-start ramp. A resistor divider pair can be used on the external control ramp to the SS/TRK pin to program the tracking rate of the output voltage. The final voltage detected by the SS/TRK pin must not fall below 1.2 V to avoid abnormal operation.

V_{OUT} tracked to an external voltage ramp has the option of ramping up slower or faster than the internal voltage ramp. V_{FB} always follows the lower potential of the internal voltage ramp and the voltage on the SS/TRK pin. 図 7-4 shows resistive divider connection if external ramp tracking is desired.

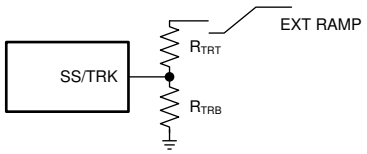


図 7-4. Soft-Start Tracking External Ramp

図 7-5 shows the case when V_{OUT} ramps more slowly than the internal ramp, while 図 7-6 shows when V_{OUT} ramps faster than the internal ramp. Faster start-up time can result in inductor current tripping current protection during start-up. Use with special care.

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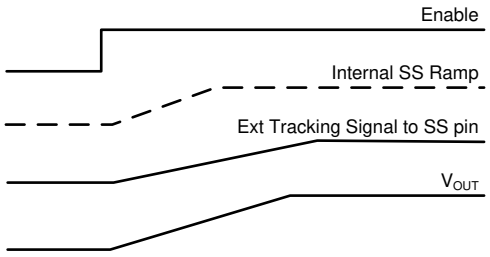


図 7-5. Tracking with Longer Start-up Time than the Internal Ramp

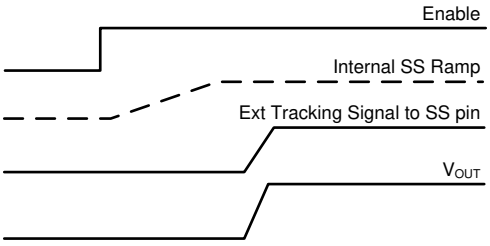


図 7-6. Tracking with Shorter Start-up Time than the Internal Ramp

The LM76005-Q1 is capable of start-up into pre-biased output conditions. During start-up, the device sets the minimum inductor current to zero to avoid discharging a pre-biased load.

7.3.7 Adjustable Switching Frequency (RT) and Frequency Synchronization

The switching frequency of the LM76005-Q1 can be programmed by the impedance R_T from the RT pin to ground. The frequency is inversely proportional to the R_T resistance. The RT pin can be left floating, and the LM76005-Q1 operates at 400-kHz default switching frequency. The RT pin is not designed to be shorted to ground.

For an desired frequency, R_T can be found by:

$$R_T(k\Omega) = \frac{38400}{\text{Frequency(kHz)} - 14.33} \quad (6)$$

表 7-1. Switching Frequency vs RT

SWITCHING FREQUENCY (kHz)	RT RESISTANCE (kΩ)
200	206.82
300	134.42
400	99.57
500	79.07

The LM76005-Q1 switching action can also be synchronized to an external clock from 200 kHz to 500 kHz. TI recommends connecting an external clock to the SYNC pin with an appropriate termination resistor. Ground the SYNC pin if not used.

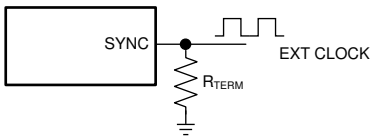


図 7-7. Frequency Synchronization

The recommendations for the external clock include high level no lower than 2 V, low level no higher than 0.4 V, duty cycle between 10% and 90%, and both positive and negative pulse width no shorter than 80 ns. When the external clock fails at logic high or low, the LM76005-Q1 switches at the frequency programmed by the R_T

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resistor after a time-out period. TI recommends connecting a resistor R_T to the RT pin so that the internal oscillator frequency is the same as the target clock frequency when the LM76005-Q1 is synchronized to an external clock. This allows the regulator to continue operating at approximately the same switching frequency if the external clock fails.

The choice of switching frequency is usually a compromise between conversion efficiency and the size of the circuit. Lower switching frequency implies reduced switching losses (including gate charge losses, switch transition losses, and so forth) and usually results in higher overall efficiency. However, higher switching frequency allows use of smaller LC output filters and hence a more compact design. Lower inductance also helps transient response (higher large signal slew rate of inductor current), and reduces the DCR loss. The optimal switching frequency is usually a trade-off in a given application and thus needs to be determined on a case-by-case basis. It is related to the following:

- Input voltage
- Output voltage
- Most frequent load current level or levels
- External component choices
- Circuit size requirement

The choice of switching frequency can also be limited if an operating condition triggers t_{ON-MIN} or $t_{OFF-MIN}$.

7.3.8 Minimum On-Time, Minimum Off-Time, and Frequency Foldback at Dropout Conditions

Minimum on-time, t_{ON-MIN}, is the smallest duration of time that the HS switch can be on. t_{ON-MIN} is typically 65 ns in the LM76005-Q1. Minimum off-time, $t_{OFF-MIN}$, is the smallest duration that the HS switch can be off. $t_{OFF-MIN}$ is typically 95 ns in the LM76005-Q1. In CCM operation, t_{ON-MIN} and $t_{OFF-MIN}$ limits the voltage conversion range given a selected switching frequency. The minimum duty cycle allowed is:

$$D_{MIN} = t_{ON-MIN} \times f_{SW} \quad (7)$$

And the maximum duty cycle allowed is:

$$D_{MAX} = 1 - t_{OFF-MIN} \times f_{SW} \quad (8)$$

Given fixed t_{ON-MIN} and $t_{OFF-MIN}$, the higher the switching frequency the narrower the range of the allowed duty cycle. In the LM76005-Q1, frequency foldback scheme is employed to extend the maximum duty cycle when $t_{OFF-MIN}$ is reached. The switching frequency decreases once longer duty cycle is needed under low V_{IN} conditions. Such a wide range of frequency foldback allows the LM76005-Q1 output voltage to stay in regulation with a much lower supply voltage V_{IN}. This leads to a lower effective dropout voltage.

Given an output voltage, the choice of the switching frequency affects the allowed input voltage range, solution size, and efficiency. The maximum operational supply voltage can be found by:

$$V_{IN_MAX} = V_{OUT} / (f_{SW} \times t_{ON-MIN}) \quad (9)$$

At lower supply voltage, the switching frequency decreases once $t_{OFF-MIN}$ is tripped. The minimum V_{IN} without frequency foldback can be approximated by:

$$V_{IN_MIN} = V_{OUT} / (f_{SW} \times t_{OFF-MIN}) \quad (10)$$

Considering power losses in the system with heavy load operation, V_{IN-MIN} is higher than the result calculated in Equation 10. With frequency foldback, V_{IN-MIN} is lowered by decreased f_{SW}. When the device is operating in auto mode at voltages near maximum rated input voltage and light load conditions, an increased output voltage ripple during load transient can be observed. For this reason, TI recommends that the device operating point be calculated with sufficient operational margin so that minimum on-time condition is not triggered.

7.3.9 Bootstrap Voltage and VBOOT UVLO (BOOT Pin)

The driver of the power switch (HS switch) requires bias higher than V_{IN} when the HS switch is ON. The capacitor connected between C_{BOOT} and SW works as a charge pump to boost voltage on the BOOT pin to (V_{SW}

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+ V_{CC}). The boot diode is integrated on the LM76005-Q1 die to minimize physical size. TI recommends a 0.47-µF, 6.3-V or higher capacitor for C_{BOOT}. The V_{BOOT_UVLO} threshold is typically 2.2 V. If the C_{BOOT} capacitor is not charged above this voltage with respect to SW, the device initiates a charging sequence using the low-side FET.

7.3.10 Power Good and Overvoltage Protection (PGOOD)

The LM76005-Q1 has a built-in power-good flag shown on the PGOOD pin to indicate whether the output voltage is within its regulation level. The PGOOD signal can be used for start-up sequencing of multiple rails. The PGOOD pin is an open-drain output that requires a pullup resistor to an appropriate logic voltage (any voltage below 12 V). The pin can sink 5 mA of current and maintain its specified logic low level. A typical range of pullup resistor value is 10 kΩ to 100 kΩ. When the FB voltage is outside the power-good band, +10% above and –10% below the internal reference V_{REF} typically, the PGOOD switch is turned on, and the PGOOD pin voltage is pulled to ground. When the FB is 2.5% (typical) closer to FB than the PGOOD threshold, the PGOOD switch is turned off, and the pin is pulled up to the voltage connected to the pullup resistor. Both rising and falling edges of the power-good flag have a built-in 140-µs (typical) deglitch delay. To pull up the PGOOD pin to a voltage higher than 15 V, a resistor divider can be used to divide the voltage down.

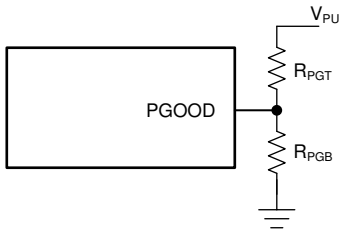


図 7-8. PGOOD Resistor Divider

For given pullup voltage, V_{PU}, the desired voltage on PGOOD pin, V_{PG}, and R_{PGT} chosen, use Equation 11 to calculate R_{PGB}:

$$R_{PGB} = \frac{V_{PG}}{V_{PU} - V_{PG}} R_{PGT} \tag{11}$$

7.3.11 Overcurrent and Short-Circuit Protection

The LM76005-Q1 is protected from overcurrent conditions by cycle-by-cycle current limiting on both peak and valley of the inductor current. Hiccup mode is activated if a fault condition persists to prevent overheating.

High-side MOSFET overcurrent protection is implemented by the nature of the peak current-mode control. The HS switch current is sensed when the HS is turned on after a blanking time. The HS switch current is compared to either the minimum of a fixed current set point (I_{HS_Limit}) or the output of the voltage regulation loop minus slope compensation every switching cycle.

When the LS switch is turned on, the current going through it is also sensed and monitored. Before turning off the LS switch at the end of every clock cycle, the LS current is compared to the LS current limit. If the LS current limit is exceeded, the LS MOSFET stays on, and the HS switch is not turned on. The LS switch is kept ON so that inductor current keeps ramping down, until the inductor current ramps below I_{LS_LIMIT}. The LS switch is turned off once the LS current falls below the limit, and the HS switch is turned on again after a dead time.

If the current of the LS switch is higher than the LS current limit for 128 consecutive cycles, and the feedback voltage falls 60% below regulation, hiccup current-protection mode is activated. In hiccup mode, the regulator is shut down and kept off for 46 ms typically before the LM76005-Q1 tries to start again. If overcurrent or a short-circuit fault condition still exists, hiccup repeats until the fault condition is removed. Hiccup mode reduces power dissipation under severe overcurrent conditions, and prevents overheating and potential damage to the device. Under non-severe overcurrent conditions when the feedback voltage has not fallen 60% below regulation, the LM76005-Q1 reduces the switching frequency and keeps the inductor current valley clamped at the LS current limit level. This operation mode allows slight overcurrent operation during load transients without tripping hiccup.

If tracking was used for initial sequencing, the device attempts to restart using the internal soft-start circuit until the tracking voltage is reached.

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7.3.12 Thermal Shutdown

Thermal shutdown limits total power dissipation by turning off the internal switches when the device junction temperature exceeds 150°C (typical). After thermal shutdown occurs, hysteresis prevents the device from switching until the junction temperature drops to approximately 135°C. When the junction temperature falls below 135°C, the LM76005-Q1 attempts to soft start.

7.4 Device Functional Modes

7.4.1 Shutdown Mode

The EN pin provides electrical on/off control for the LM76005-Q1. When the EN pin voltage is below 0.3 V (typical), both the regulator and the internal LDO have no output voltages, and the device is in shutdown mode. In shutdown mode the quiescent current drops to typically 1.2 µA. The LM76005-Q1 also employs UVLO protection. If V_{CC} voltage is below the UVLO level, the output of the regulator is turned off.

7.4.2 Standby Mode

The internal LDO has a lower EN threshold than the regulator. When the EN pin voltage is above 1.2 V (maximum) and below the precision enable threshold for the output voltage, the internal LDO regulates the V_{CC} voltage at 3.29 V typically. The precision enable circuitry is ON once V_{CC} is above the UVLO. The internal MOSFETs remain in tri-state unless the voltage on EN pin goes above the precision enable threshold. The LM76005-Q1 also employs UVLO protection. If V_{CC} voltage is below the UVLO level, the output of the regulator is turned off.

7.4.3 Active Mode

The LM76005-Q1 is in active mode when the EN pin and UVLO high threshold levels are satisfied. The simplest way to enable the operation of the LM76005-Q1 is to connect the EN pin to VIN, which allows self start-up of the LM76005-Q1 when the input voltage is in the operation range: 3.5 V to 60 V. See *セクション 7.3.4* for details on setting these operating levels.

In active mode, depending on the load current, the LM76005-Q1 will be in one of five sub modes:

1. CCM with fixed switching frequency with load between half of I_{MINPK} to full load
2. DCM when the load current is lower than half of the inductor current ripple
3. Light load mode where the device uses pulse frequency modulation (PFM) and lowers the switching frequency at load under half of I_{PEAK_MIN} to improve efficiency
4. Foldback mode when switching frequency is reduced to maintain output regulation with supply voltages that cause the minimum t_{ON} or t_{OFF} to be exceeded
5. Forced-pulse-width modulation (FPWM) is similar to CCM with fixed switching frequency, but extends the fixed frequency range of operation from full to no load.

7.4.4 CCM Mode

CCM operation is employed in the LM76005-Q1 when the load current is higher than ½ of the peak-to-peak inductor current. If the load current is decreased, the device enters DCM mode. In CCM operation, the frequency of operation is constant and fixed unless the minimum t_{ON} or t_{OFF} are exceeded which causes the part to enter foldback mode (refer to *セクション 7.3.5* for details). In these cases, PWM is still maintained, but the frequency of operation is folded back (reduced) to maintain proper regulation.

7.4.5 DCM Mode

DCM operation is employed in the LM76005-Q1 when the load current is lower than ½ of the peak-to-peak inductor current. In DCM operation (also known as diode emulation mode), the LS FET is turned off when the inductor current drops below 0 A to keep operation as efficient as possible by reducing switching losses and preventing negative current conduction. In PWM operation, the frequency of operation is constant and fixed unless the load current is reduced below I_{PEAK_MIN}, which causes the part to enter light load mode, or if the minimum t_{ON} or t_{OFF} are exceeded, which cause the device to enter foldback mode.

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7.4.6 Light Load Mode

At light output current loads, PFM is activated for the highest efficiency possible. When the inductor current does not reach I_{PEAK_MIN} during a switching cycle, the on-time is increased, and the switching frequency reduces as needed to maintain proper regulation. The on-time has a maximum value of 8 µs to avoid large output voltage ripple in dropout conditions. Efficiency is greatly improved by reducing switching and gate-drive losses. During light-load mode of operation, the LM76005-Q1 operates with a minimum quiescent current of 10 to 15 µA (typical).

7.4.7 Foldback Mode

Foldback protection modes are entered when the duty cycle exceeds the minimum on- and off-times of the device. At very high duty cycles, where the minimum off-time is not satisfied, the frequency folds back to allow more time for the peak current command to be reached. The maximum on-time is 8 µs, which limits the maximum duty cycle in dropout to 98%. At very low duty cycles when the minimum on-time is reached, the device maintains regulation by dropping the frequency to allow more time for the inductor current to discharge the output capacitor. Foldback mode is exited once the minimum on-time and off-times are satisfied.

7.4.8 Forced Pulse-Width-Modulation Mode

FPWM is employed when the FPWM pin is pulled high, or the device is synchronized to an external clock. In this mode, diode emulation is turned off, and the device remains in CCM over the full load range. In FPWM operation, the frequency of operation is constant and fixed unless the minimum t_{ON} or t_{OFF} are exceeded, which cause the device to enter foldback mode. In these cases, PWM operation is still maintained, but the frequency of operation is folded back (reduced) to maintain proper regulation. DC accuracy is highest in FPWM mode.

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8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The LM76005-Q1 is a step-down DC-DC converter. It is typically used to convert a higher DC voltage to a lower DC voltage with a maximum output current of 5 A. The following design procedure can be used to select component values for the LM76005-Q1. Alternately, the WEBENCH® software may be used to generate a complete design. The WEBENCH software uses an iterative design procedure and accesses a comprehensive database of components when generating a design.

8.2 Typical Applications

The LM76005-Q1 only requires a few external components to convert from a wide range of supply voltages to output voltage, as shown in 図 8-1:

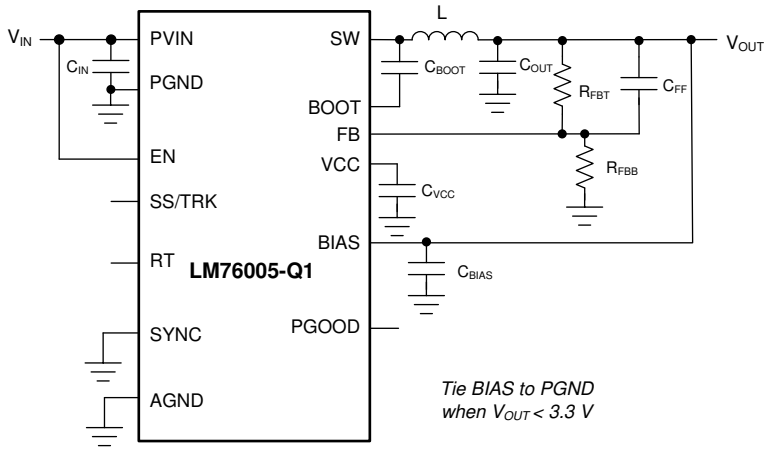


図 8-1. LM76005-Q1 Basic Schematic

The LM76005-Q1 also integrates a full list of features to aid system design requirements, such as the following:

- VCC UVLO
- Programmable soft start
- Start-up tracking
- Programmable switching frequency
- Clock synchronization
- Power-good indication

Each system can select the features needed in a specific application. A comprehensive schematic with all features utilized is shown in 図 8-2:

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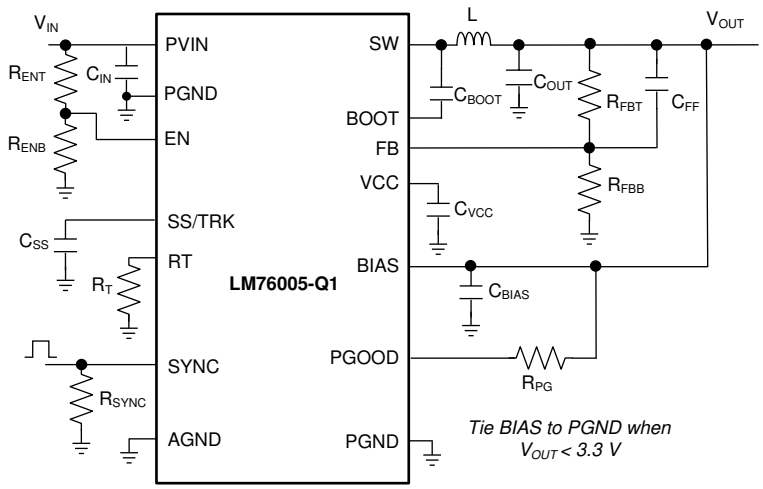


図 8-2. LM76005-Q1 Comprehensive Schematic

The external components must fulfill the requirements of the application, but also the stability criteria of the device control loop. The LM76005-Q1 is optimized to work within a range of external components. Inductance and capacitance of the LC output filter each create poles that have to be considered in the control of the converter. For V_{OUT} = 1 V, 3.3 V, 5V, the recommended output capacitors have been generated assuming typical derating for 16-V, X7R, automotive grade capacitors. For V_{OUT} = 12 V, the recommended output capacitors have been generated assuming typical derating for 25-V, X7R, automotive grade capacitors, and for V_{OUT} = 24 V, the recommended output capacitors have been generated assuming typical derating for 50-V, X7R, automotive grade capacitors. If lower voltage, nonautomotive grade, or lower temperature rated capacitors are used, more capacitors than listed are likely to be needed.表 8-1 can be used to simplify the output filter component selection.

表 8-1. Typical Component Selection

f_{SW} (kHz)	V_{OUT} (V)	L (µH)	C_{OUT} (µF)	R_{FBT} (kΩ)	R_{FBB} (kΩ)
200	1	2.5	720	100	OPEN
400	1	1.2	600	100	OPEN
500	1	1	470	100	OPEN
200	3.3	10	300	100	43.5
400	3.3	4.7	220	100	43.5
500	3.3	4.7	200	100	43.5
200	5	15	250	100	25
400	5	6.8	180	100	25
500	5	5.2	150	100	25
200	12	22	200	100	9.09
400	12	10	150	100	9.09
500	12	7.2	120	100	9.09
200	24	44	150	100	4.37
400	24	22	100	100	4.37
500	24	15	88	100	4.37

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8.2.1 Design Requirements

セクション 8.2.2 is based on a design example. For this design example, use the parameters listed in 表 8-2 as the input parameters.

表 8-2. Design Example Parameters

DESIGN PARAMETER	VALUE
Input voltage range	3.5 V to 60 V
Output voltage	5 V
Input ripple voltage	400 mV
Output ripple voltage	30 mV
Output current rating	5 A
Operating frequency	400 kHz

8.2.2 Detailed Design Procedure

8.2.2.1 Custom Design With WEBENCH® Tools

Click here to create a custom design using the LM76005-Q1 device with the WEBENCH® Power Designer.

1. Start by entering the input voltage (V_{IN}), output voltage (V_{OUT}), and output current (I_{OUT}) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance
- Run thermal simulations to understand board thermal performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

8.2.2.2 Output Voltage Setpoint

The output voltage of the LM76005-Q1 device is externally adjustable using a resistor divider network. In the application circuit of 図 8-2, this divider network is comprised of top feedback resistor, R_{FBT}, and bottom feedback resistor, R_{FBB}. Equation 12 is used to determine the output voltage of the converter:

$$R_{FBB} = \frac{V_{FB}}{V_{OUT} - V_{FB}} R_{FBT} \tag{12}$$

Choose the value of the R_{FBT} to be around 1 MΩ to minimize quiescent current during light load operation or 100 kΩ to improve noise immunity. With the desired output voltage set to be 5 V and with a V_{FB} = 1 V, the R_{FBB} value can then be calculated using Equation 12. The formula yields a value of 24.9 kΩ when R_{FBT} = 100 kΩ.

8.2.2.3 Switching Frequency

The default switching frequency of the LM76005-Q1 device is set at 400 kHz. If the R_T is left open, the LM76005-Q1 switches at 400 kHz in CCM mode. Use Equation 13 to calculate the required value for R_T to operate the LM76005-Q1 at different frequencies.

$$R_T(k\Omega) = \frac{38400}{\text{Frequency(kHz)} - 14.33} \tag{13}$$

The result for 400 kHz is 99.57 kΩ.

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The choice of switching frequency is a compromise between conversion efficiency and overall solution size. Lower switching frequency implies reduced switching losses and usually results in higher system efficiency. However, higher switching frequency allows for the use of smaller inductors and output capacitors, hence, a more compact design. When choosing operating frequency, the most important consideration is thermal limitations. This constraint typically dominates frequency selection. For the LM76005, the safe operating area is controlled by the thermal performance ($R_{\theta JA}$=18.8 °C/W); see 図 8-3.

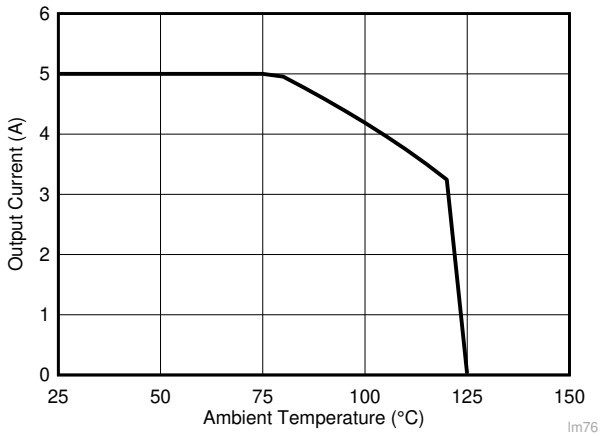


図 8-3. LM76005-Q1 Safe Operating Area (5 V_{OUT}, 400 kHz, $R_{\theta JA}$=18.8 °C/W)

8.2.2.4 Input Capacitors

The LM76005-Q1 device requires an input decoupling and, depending on the application, a bulk input capacitor. The typical recommended value for the high frequency decoupling capacitor is 10 µF to 22 µF. TI recommends a high-quality ceramic type X5R or X7R with sufficiency voltage rating. The voltage rating must be greater than the maximum input voltage. To compensate the derating of ceramic capacitors, a voltage rating of twice the maximum input voltage is recommended.

Many times, it is desirable and necessary to use an electrolytic capacitor on the input in parallel with the ceramics. This is especially true if the LM76005-Q1 circuit is not located within approximately 5 cm from the input voltage source. This capacitor can help damp any ringing on the input supply caused by the long power leads and the associated inductance. The use of this additional capacitor also helps with momentary voltage dips caused by input supplies with unusually high impedance. The optimum value for this capacitor is four times the ceramic input capacitance with ESR close to the characteristic impedance of the LC filter formed by the application input inductance and ceramic input capacitors.

For this design, two 4.7-µF, X7R dielectric capacitors rated for 100 V are used for the input decoupling capacitance. A single capacitor can aslo be used that has an equivalent series resistance (ESR) of approximately 3 mΩ, and an RMS current rating of 5 A. Include a capacitor with a value of 47 nF for high-frequency filtering and place it as close as possible to the device pins.

Note

DC-Bias Effect: High capacitance ceramic capacitors have a DC-bias derating effect, which has a strong influence on the final effective capacitance. Therefore, choose the right capacitor value carefully. Package size and voltage rating in combination with dielectric material are responsible for differences between the rated capacitor value and the effective capacitance.

8.2.2.5 Inductor Selection

The first criterion for selecting an output inductor is the inductance itself. In most buck converters, this value is based on the desired peak-to-peak ripple current, Δi_L that flows in the inductor along with the load current. As with switching frequency, the selection of the inductor is a tradeoff between size and cost. Higher inductance means lower ripple current and hence lower output voltage ripple. Lower inductance results in smaller, less expensive devices. An inductance that gives a ripple current of 20% to 40% of the maximum output current is a

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good starting point. (Δi_L = (1/5 to 2/5) × I_{OUT}). The peak-to-peak inductor current ripple can be found by Equation 15 and the range of inductance can be found by Equation 14 with the typical input voltage used as V_{IN}.

$$\Delta i_L = \frac{(V_{IN} - V_{OUT}) \times D}{L \times f_{SW}} \tag{14}$$

$$\frac{(V_{IN} - V_{OUT}) \times D}{0.4 \times f_{SW} \times I_{LOAD\text{-}MAX}} \leq L \leq \frac{(V_{IN} - V_{OUT}) \times D}{0.2 \times f_{SW} \times I_{LOAD\text{-}MAX}} \tag{15}$$

D is the duty cycle of the converter which in a buck converter it can be approximated as D = V_{OUT} / V_{IN}, assuming no loss power conversion. By calculating in terms of amperes, volts, and megahertz, the inductance value comes out in micro henries. The inductor ripple current ratio is defined by:

$$r = \frac{\Delta i_L}{I_{OUT}} \tag{16}$$

The second criterion is the inductor saturation-current rating. The inductor must be rated to handle the maximum load current plus the ripple current:

$$I_{L\text{-}PEAK} = I_{LOAD\text{-}MAX} + \Delta i_L / 2 \tag{17}$$

The LM76005-Q1 has both valley current limit and peak current limit. During an instantaneous short, the peak inductor current can be high due to a momentary increase in duty cycle. The inductor current rating must be higher than the HS current limit. TI recommends selection of an inductor with a larger core saturation margin and preferably a softer roll off of the inductance value over load current.

In general, it is preferable to choose lower inductance in switching power supplies, because it usually corresponds to faster transient response, smaller DCR, and reduced size for more compact designs. However, too low of an inductance can generate too large of an inductor current ripple such that overcurrent protection at the full load can be falsely triggered. It also generates more conduction loss because the RMS current is slightly higher relative that with lower current ripple at the same DC current. Larger inductor current ripple also implies larger output voltage ripple with the same output capacitors. With peak-current-mode control, it is not recommended to have an inductor current ripple that is too small. Enough inductor current ripple improves signal-to-noise ratio on the current comparator and makes the control loop more immune to noise.

Once the inductance is determined, the type of inductor must be selected. Ferrite designs have very low core losses and are preferred at high switching frequencies, so design goals can concentrate on copper loss and preventing saturation. Ferrite core material saturates hard, which means that inductance collapses abruptly when the peak design current is exceeded. The hard saturation results in an abrupt increase in inductor ripple current and consequent output voltage ripple. Do not allow the core to saturate.

For the design example, a standard 6.8-µH inductor from Wurth, Coiltronics, or Vishay can be used for the 5-V.

8.2.2.6 Output Capacitor Selection

The device is designed to be used with a wide variety of LC filters. TI generally recommends using as little output capacitance as possible to keep cost and size down. Choose the output capacitor or capacitors, C_{OUT}, with care as it directly affects the steady-state output-voltage ripple, loop stability, and the voltage over/undershoot during load current transients.

The output voltage ripple is essentially composed of two parts. One is caused by the inductor current ripple going through the equivalent series resistance (ESR) of the output capacitors:

$$\Delta V_{OUT\text{-}ESR} = \Delta i_L \times ESR \tag{18}$$

The other is caused by the inductor current ripple charging and discharging the output capacitors:

$$\Delta V_{OUT\text{-}C} = \Delta i_L / (8 \times f_{SW} \times C_{OUT}) \tag{19}$$

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The two components in the voltage ripple are not in phase, so the actual peak-to-peak ripple is smaller than the sum of the two peaks.

Output capacitance is usually limited by transient performance specifications if the system requires tight voltage regulation in the presence of large current steps and fast slew rates. When a fast large load transient happens, output capacitors provide the required charge before the inductor current can slew to the appropriate level. The initial output voltage step is equal to the load current step multiplied by the ESR. V_{OUT} continues to droop until the control loop response increases or decreases the inductor current to supply the load. To maintain a small overshoot or undershoot during a transient, small ESR, and large capacitance are desired. But these also come with higher cost and size. Thus, the motivation is to seek a fast control loop response to reduce the output voltage deviation.

For a given input and output requirement, Equation 20 gives an approximation for an absolute minimum output cap required:

$$C_{OUT} > \frac{1}{(f_{SW} \times r \times \Delta V_{OUT} / I_{OUT})} \times \left[\left(\frac{r^2}{12} \times (1 + D') \right) + (D' \times (1 + r)) \right] \quad (20)$$

Along with this for the same requirement, calculate the maximum ESR as per Equation 21:

$$ESR < \frac{D'}{f_{SW} \times C_{OUT}} \times \left(\frac{1}{r} + 0.5 \right) \quad (21)$$

where

- r = ripple ratio of the inductor ripple current (Δi_L / I_{OUT})
- ΔV_O = target output voltage undershoot
- D’ = 1 – duty cycle
- f_{SW} = switching frequency
- I_{OUT} = load current

A general guideline for C_{OUT} range is that C_{OUT} must be larger than the minimum required output capacitance calculated by Equation 20. Limit the maximum value of total output capacitance to between 800 µF and 1200 µF. Large values of output capacitance can prevent the regulator from starting up correctly and adversely effect the loop stability. If values greater than the given range are to be used, then a careful study of start-up at full load and loop stability must be performed.

In applications with V_{OUT} less than 3.3 V, it is critical that low ESR output capacitors are selected. This limits potential output voltage overshoots as the input voltage falls below the device normal operating range. To optimize the transient behavior a feedforward capacitor can be added in parallel with the upper feedback resistor. For this design example, three 47-µF, 10-V, X7R ceramic capacitors are used in parallel.

8.2.2.7 Feedforward Capacitor

The LM76005-Q1 is internally compensated. Depending on the V_{OUT} and frequency F_S, if the output capacitor C_{OUT} is dominated by low ESR (ceramic types) capacitors, it can result in low phase margin. To improve the phase boost an external feedforward capacitor, C_{FF} can be added in parallel with R_{FBT}. C_{FF} is chosen such that phase margin is boosted at the crossover frequency without C_{FF}. A simple estimation for the crossover frequency without C_{FF} (f_x) is shown in Equation 22, assuming C_{OUT} has very small ESR.

$$f_X = \frac{15.46}{V_{OUT} \times C_{OUT}} \quad (22)$$

Equation 23 for C_{FF} was tested:

$$C_{FF} = \frac{1}{2\pi f_x} \times \frac{1}{\sqrt{R_{FBT} \times (R_{FBT} \,//\, R_{FBB})}} \quad (23)$$

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If capacitors with high ESR are used, C_{FF} is not required. The C_{FF} capacitor creates a time constant with R_{FBT} that couples the attenuated output voltage ripple to the FB node. Using a value that is too large for C_{FF} can couple too much ripple to FB node and affect output voltage regulation. For capacitors with medium ESR (20 – 200 mΩ), 式 23 can be used as a quick starting point. For the application in this design example, a 47-pF C0G capacitor is used.

8.2.2.8 Bootstrap Capacitors

Every LM76005-Q1 design requires a bootstrap capacitor, C_{BOOT}. The recommended bootstrap capacitor is 0.47 µF and rated at 6.3 V or greater. The bootstrap capacitor is located between the SW pin and the BOOT pin. The bootstrap capacitor must be a high-quality ceramic type with X7R or X5R grade dielectric for temperature stability.

For improved EMI performance, a boot resistor can be added in series with the bootstrap capacitor. The boot resistor will slow down the rising edge of the switch node.

8.2.2.9 VCC Capacitors

The VCC pin is the output of an internal LDO for LM76005-Q1. The input for this LDO comes from either VIN or BIAS (please refer to functional block diagram for LM76005-Q1). To ensure stability of the part, place a 1-µF to 2.2-µF, 10-V capacitor for this pin. Never short VCC pin to ground during operation.

8.2.2.10 BIAS Capacitors

For an output voltage of 3.3 V and greater, connect the BIAS pin to the output to increase light load efficiency. The BIAS pin is one of the two inputs for the VCC LDO. When BIAS voltage is below $V_{BIAS-ON}$ threshold, the input for the VCC LDO is internally connected to VIN. Because this is an LDO, the voltage differences between the input and output affects the efficiency of the LDO. If necessary, a capacitor with a value of 1 µF can be added close to the BIAS pin as an input capacitor for the LDO.

8.2.2.11 Soft-Start Capacitors

The SS pin can be left floating, and the LM76005-Q1 implements a soft-start time of 6.3 ms. To use an external soft-start capacitor, the capacitor must be sized so that the soft-start time is greater than 6.3 ms. Use Equation 24 to calculate the soft-start capacitor value:

$$C_{SS} = I_{SSC} \times t_{SS} \quad (24)$$

With a desired soft-start time of 11 ms, a soft-start charging current of 2 µA, and an internal V_{REF} of 1 V, Equation 24 yields a soft-start capacitor value of 22 nF.

8.2.2.12 Undervoltage Lockout Setpoint

The undervoltage lockout (UVLO) is adjusted using the external voltage divider network of R_{ENT} and R_{ENB}. R_{ENT} is connected between the PVIN pin and the EN pin of the LM76005-Q1. R_{ENB} is connected between the EN pin and the GND pin. The UVLO has two thresholds, one for power up when the input voltage is rising and one for power down or brownouts when the input voltage is falling. Equation 25 can be used to determine the V_{IN} UVLO level.

$$V_{IN-UVLO-RISING} = V_{ENH} \times (R_{ENB} + R_{ENT}) / R_{ENB} \quad (25)$$

The EN rising threshold (V_{ENH}) for LM76005-Q1 is set to be 1.204 V (typical). Choose the value of R_{ENB} to be 100 kΩ to minimize input current from the supply. If the desired V_{IN} UVLO level is at 5 V, then the value of R_{ENT} can be calculated using Equation 26:

$$R_{ENT} = (V_{IN-UVLO-RISING} / V_{ENH} – 1) \times R_{ENB} \quad (26)$$

Equation 26 yields a value of 315 kΩ. The resulting falling UVLO threshold, can be calculated by Equation 27, where EN falling threshold (V_{ENL}) is 1.05 V (typical).

$$V_{IN-UVLO-FALLING} = V_{ENL} \times (R_{ENB} + R_{ENT}) / R_{ENB} \quad (27)$$

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8.2.2.13 PGOOD

A typical pullup resistor value is 10 kΩ to 100 kΩ from the PGOOD pin to a voltage no higher than 18 V. If it is desired to pull up the PGOOD pin to a voltage higher than 18 V, a resistor can be added from the PGOOD pin to ground to divide the voltage detected by the PGOOD pin to a value no higher than 18 V.

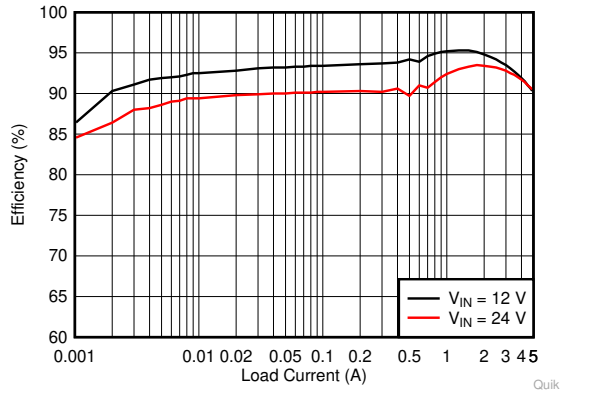
8.2.2.14 Synchronization

The LM76005-Q1 switching action can synchronize to an external clock from 200 kHz to 500 kHz. TI recommends connecting an external clock to the SYNC pin with a 50-Ω to 100-Ω termination resistor. Ground the SYNC pin if not used.

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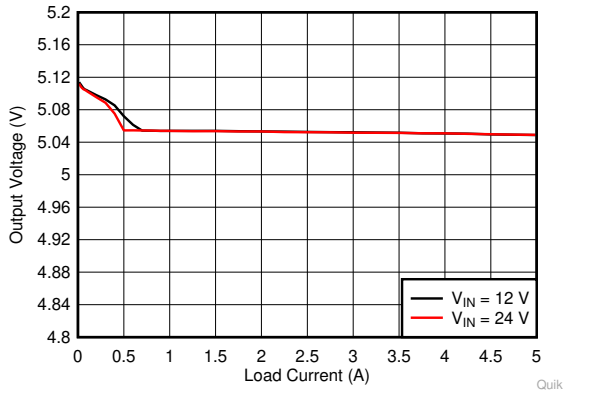
8.2.3 Application Curves

Unless otherwise specified the following conditions apply:



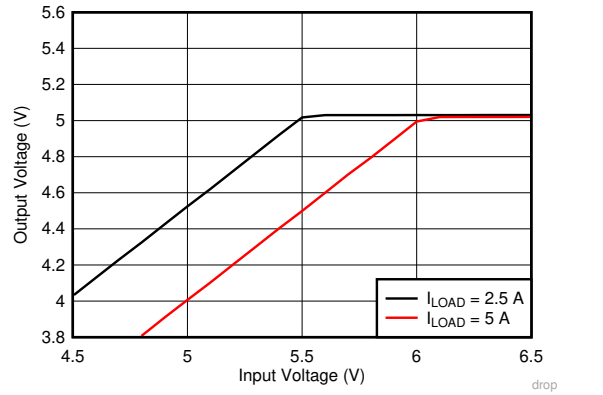
V_{OUT} = 5 V f_{SW} = 400 kHz Auto Mode

図 8-4. LM76005-Q1 Efficiency



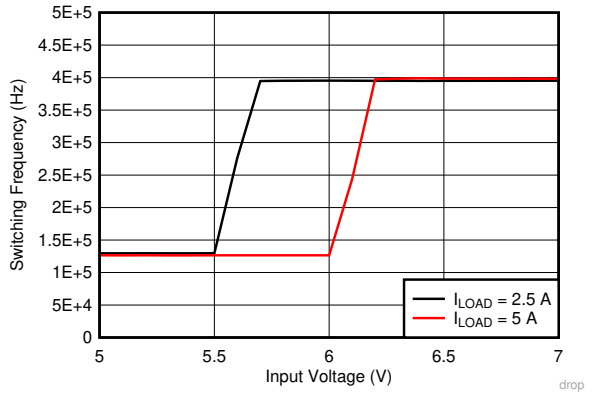
V_{OUT} = 5 V f_{SW} = 400 kHz Auto Mode

図 8-5. LM76005-Q1 Load and Line Regulation



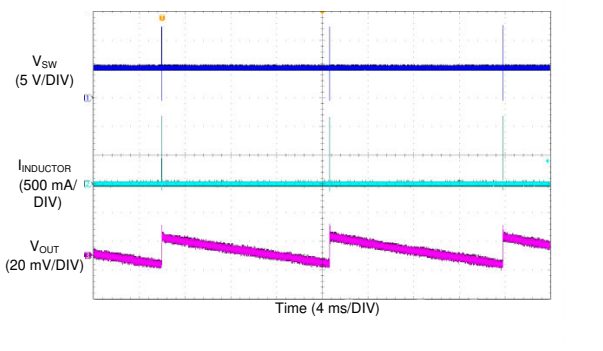
V_{OUT} = 5 V f_{SW} = 400 kHz FPWM Mode

図 8-6. LM76005-Q1 Voltage Dropout



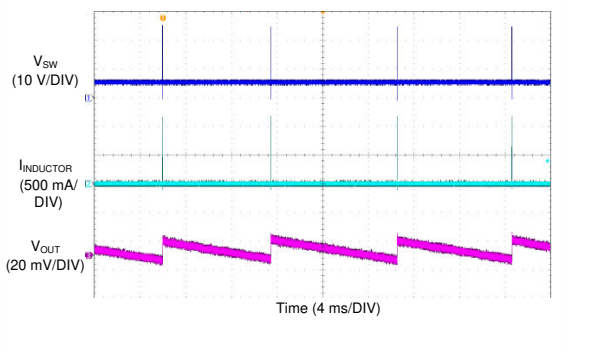
V_{OUT} = 5 V f_{SW} = 400 kHz FPWM Mode

図 8-7. LM76005-Q1 Frequency Dropout



V_{IN} = 12 V V_{OUT} = 5 V f_{SW} = 400 kHz
No Load Auto Mode

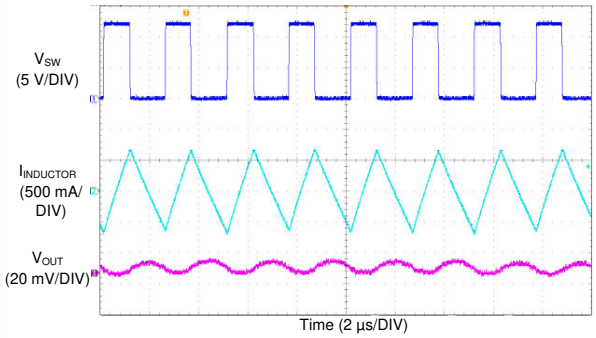
図 8-8. LM76005-Q1 Switching Waveform and Output Ripple



V_{IN} = 24 V V_{OUT} = 5 V f_{SW} = 400 kHz
No Load Auto Mode

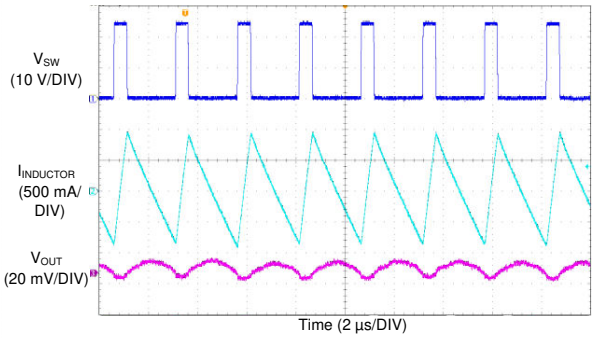
図 8-9. LM76005-Q1 Switching Waveform and Output Ripple

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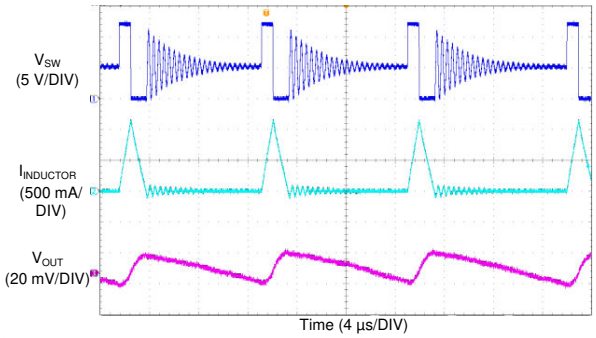
V_{IN} = 12 V V_{OUT} = 5 V f_{SW} = 400 kHz
No Load FPWM Mode

図 8-10. LM76005-Q1 Switching Waveform and Output Ripple



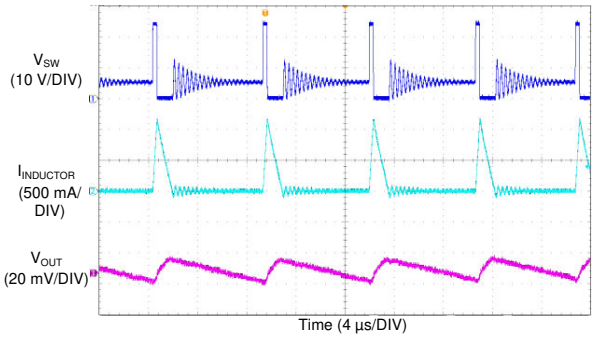
V_{IN} = 24 V V_{OUT} = 5 V f_{SW} = 400 kHz
No Load FPWM Mode

図 8-11. LM76005-Q1 Switching Waveform and Output Ripple



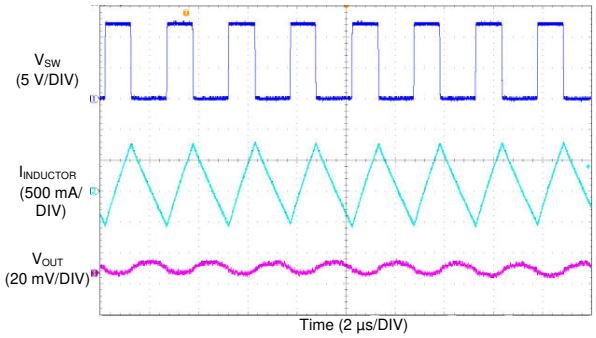
V_{IN} = 12 V V_{OUT} = 5 V f_{SW} = 400 kHz
100-mA Load Auto Mode

図 8-12. LM76005-Q1 Switching Waveform and Output Ripple



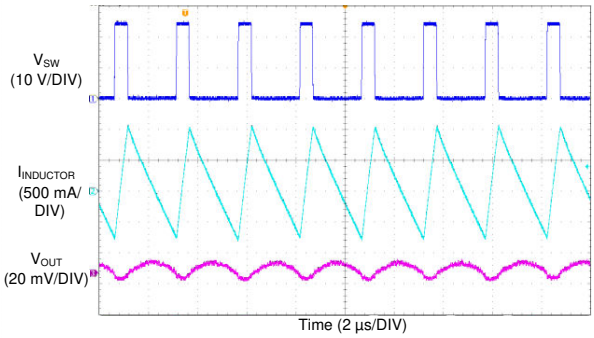
V_{IN} = 24 V V_{OUT} = 5 V f_{SW} = 400 kHz
100-mA Load Auto Mode

図 8-13. LM76005-Q1 Switching Waveform and Output Ripple



V_{IN} = 12 V V_{OUT} = 5 V f_{SW} = 400 kHz
100-mA Load FPWM Mode

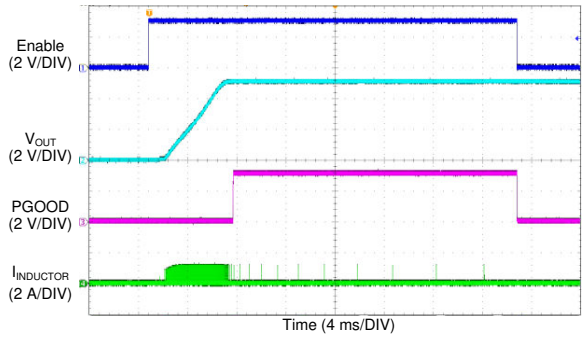
図 8-14. LM76005-Q1 Switching Waveform and Output Ripple



V_{IN} = 24 V V_{OUT} = 5 V f_{SW} = 400 kHz
100-mA Load FPWM Mode

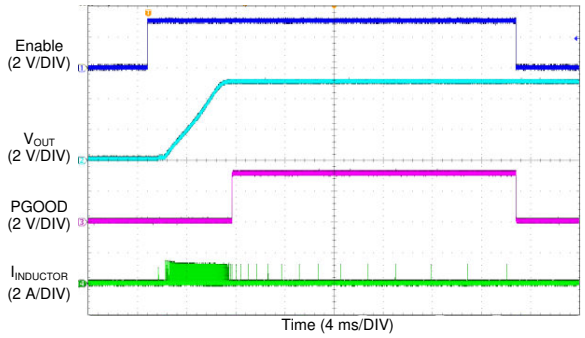
図 8-15. LM76005-Q1 Switching Waveform and Output Ripple

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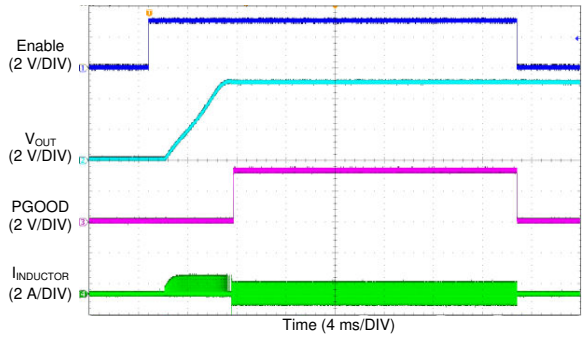
V_{IN} = 12 V V_{OUT} = 5 V f_{SW} = 400 kHz
No Load Auto Mode

図 8-16. LM76005-Q1 Start-up Waveform



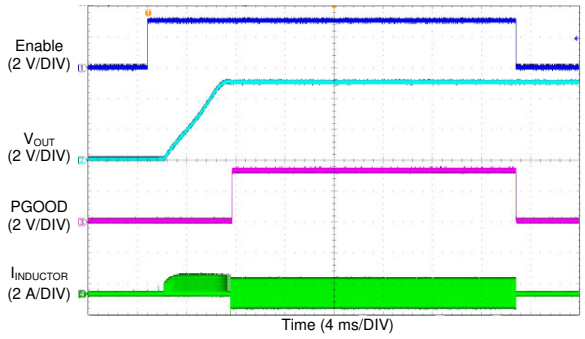
V_{IN} = 24 V V_{OUT} = 5 V f_{SW} = 400 kHz
No Load Auto Mode

図 8-17. LM76005-Q1 Start-up Waveform



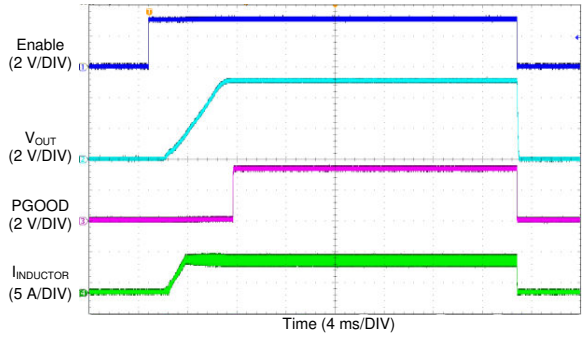
V_{IN} = 12 V V_{OUT} = 5 V f_{SW} = 400 kHz
No Load FPWM Mode

図 8-18. LM76005-Q1 Start-up Waveform



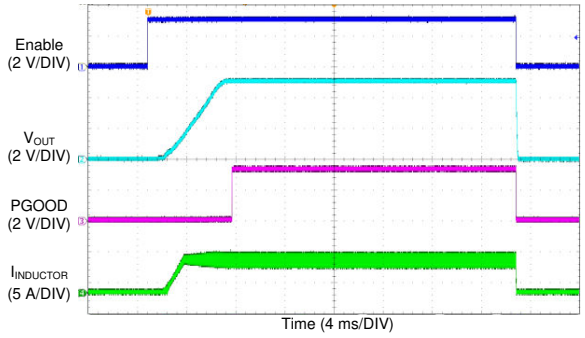
V_{IN} = 24 V V_{OUT} = 5 V f_{SW} = 400 kHz
No Load FPWM Mode

図 8-19. LM76005-Q1 Start-up Waveform



V_{IN} = 12 V V_{OUT} = 5 V f_{SW} = 400 kHz
5-A Load

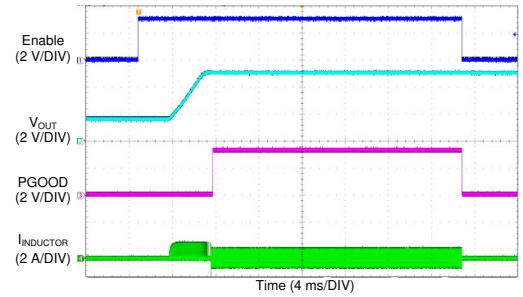
図 8-20. LM76005-Q1 Start-up Waveform



V_{IN} = 24V V_{OUT} = 5 V f_{SW} = 400 kHz
5-A Load

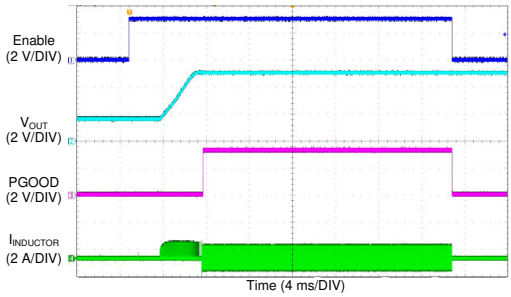
図 8-21. LM76005-Q1 Start-up Waveform

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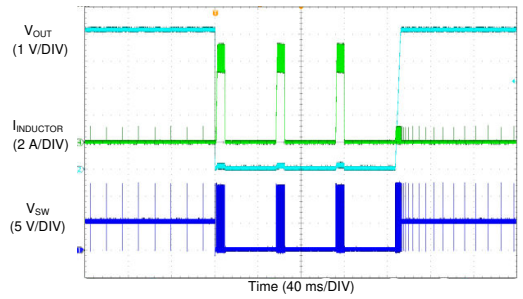
V_{IN} = 12 V V_{OUT} = 5 V f_{SW} = 400 kHz
No Load Auto Mode

図 8-22. LM76005-Q1 Start-up With Pre-Biased Output



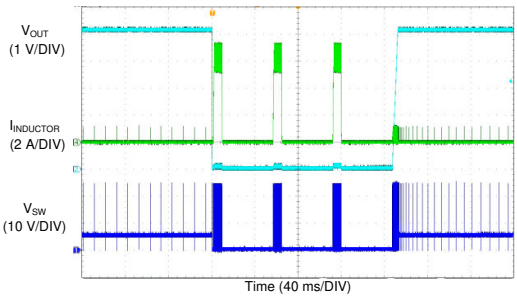
V_{IN} = 24V V_{OUT} = 5 V f_{SW} = 400 kHz
No Load Auto Mode

図 8-23. LM76005-Q1 Start-up With Pre-Biased Output



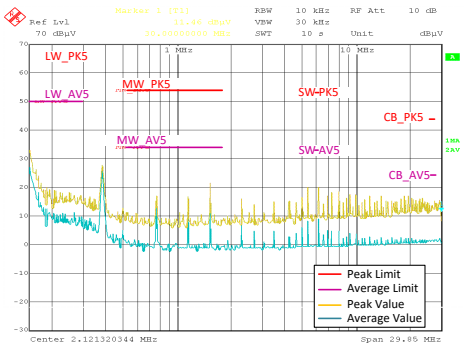
V_{IN} = 12 V V_{OUT} = 5 V f_{SW} = 400 kHz
Auto Mode

図 8-24. LM76005-Q1 Short-Circuit Behavior With Hiccup



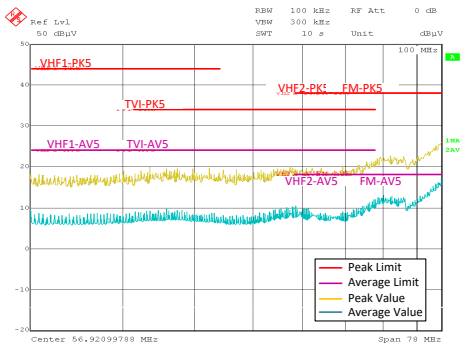
V_{IN} = 24 V V_{OUT} = 5 V f_{SW} = 400 kHz
Auto Mode

図 8-25. LM76005-Q1 Short-Circuit Behavior With Hiccup



V_{IN} = 13.5 V V_{OUT} = 5 V f_{SW} = 400 kHz
C_{FLT} = 4 × 2.2 µF, L_{FLT} = 1 µH I_{OUT} = 3.5 A

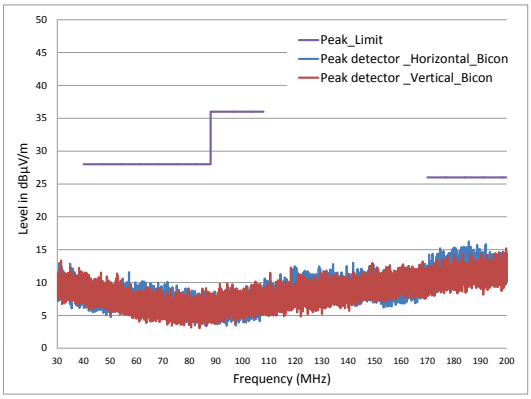
図 8-26. LM76005-Q1 Conducted EMI Result vs. CISPR25 Limits - Low Frequency



V_{IN} = 13.5 V V_{OUT} = 5 V f_{SW} = 400 kHz
C_{FLT} = 4 × 2.2 µF, L_{FLT} = 1 µH I_{OUT} = 3.5 A

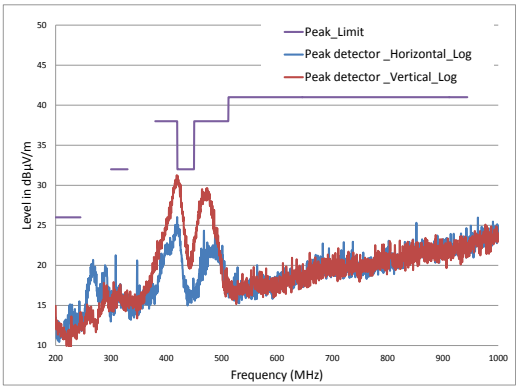
図 8-27. LM76005-Q1 Conducted EMI Result vs. CISPR25 Limits - High Frequency

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V_{IN} = 13.5 V　V_{OUT} = 5 V　f_{SW} = 400 kHz
C_{FLT} = 4 × 2.2 µF,　I_{OUT} = 3.5 A
L_{FLT} = 1 µH

図 8-28. LM76005-Q1 Radiated EMI Result vs. CISPR25 Limits - Low Frequency



V_{IN} = 13.5 V　V_{OUT} = 5 V　f_{SW} = 400 kHz
C_{FLT} = 4 × 2.2 µF,　I_{OUT} = 3.5 A
L_{FLT} = 1 µH

図 8-29. LM76005-Q1 Radiated EMI Result vs. CISPR25 Limits - High Frequency

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9 Power Supply Recommendations

The LM76005-Q1 is designed to operate from an input voltage supply range between 3.5 V and 60 V. This input supply must be able to withstand the maximum input current and maintain a voltage above 3.5 V. The resistance of the input supply rail must be low enough that an input current transient does not cause a high enough drop at the LM76005-Q1 supply voltage that can cause a false UVLO fault triggering and system reset.

If the input supply is located more than a few inches from the LM76005-Q1, additional bulk capacitance can be required in addition to the ceramic bypass capacitors. The amount of bulk capacitance is not critical, but a 47-µF or 100-µF electrolytic capacitor is a typical choice.

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10 Layout

10.1 Layout Guidelines

The performance of any switching converter depends as much upon the layout of the PCB as the component selection. The following guidelines will help the user design a circuit with maximum rejection of outside EMI and minimum generation of unwanted EMI.

1. Place ceramic high frequency bypass C_{IN} as close as possible to the LM76005-Q1 PVIN and PGND pins. Grounding for both the input and output capacitors must consist of localized top-side planes that connect to the PGND pins and PAD.
2. Place bypass capacitors for VCC and BIAS close to the pins and ground the bypass capacitors to device ground.
3. Minimize trace length to the FB pin. Both feedback resistors, R_{FBT} and R_{FBB}, must be located close to the FB pin. Place C_{FF} directly in parallel with R_{FBT}. If V_{OUT} accuracy at the load is important, make sure V_{OUT} sense is made at the load. Route the V_{OUT} sense path away from noisy nodes and preferably through a layer on the other side of a shielding layer.
4. Use ground plane in one of the middle layers as noise shielding and heat dissipation path. Have a single point ground connection to the plane. Route the ground connections for the feedback, soft start, and enable components to the ground plane. This prevents any switched or load currents from flowing in the analog ground traces. If not properly handled, poor grounding can result in degraded load regulation or erratic output voltage ripple behavior.
5. Make V_{IN}, V_{OUT} and ground bus connections as wide as possible. This reduces any voltage drops on the input or output paths of the converter and maximizes efficiency.
6. Provide adequate device heat-sinking. Use an array of heat-sinking vias to connect the exposed pad to the ground plane on the bottom PCB layer. If the PCB has multiple copper layers, these thermal vias can also be connected to inner layer heat-spreading ground planes. Ensure enough copper area is used for heat-sinking to keep the junction temperature below 125°C.

10.1.1 Layout Highlights

1. Minimize the area of switched current loops. From an EMI reduction standpoint, it is imperative to minimize the high di/dt paths during PC board layout as shown in the figure above. The high current loops that do not overlap have high di/dt content that causes observable high frequency noise on the output pin if the input capacitor C_{IN} is placed at a distance away from the LM76005-Q1. Therefore, place C_{IN} as close as possible to the LM76005-Q1 PVIN and PGND pins. This minimizes the high di/dt area and reduce radiated EMI. Additionally, grounding for both the input and output capacitor must consist of a localized top-side plane that connects to the PGND pin.
2. Have a single point ground. The ground connections for the feedback, soft-start, and enable components must be routed to the AGND pin of the device. This prevents any switched or load currents from flowing in the analog ground traces. If not properly handled, poor grounding can result in degraded load regulation or erratic output voltage ripple behavior.
3. Minimize trace length to the FB pin net. Place both feedback resistors, R_{FBT} and R_{FBB}, close to the FB pin. Because the FB node is high impedance, maintain the copper area as small as possible. Route the traces from R_{FBT}, R_{FBB} away from the body of the LM76005-Q1 to minimize possible noise pickup. Place C_{ff} directly in parallel with R_{FBT}.
4. Make input and output bus connections as wide as possible. This reduces any voltage drops on the input or output of the converter and maximizes efficiency. To optimize voltage accuracy at the load, ensure that a separate feedback voltage sense trace is made to the load. Doing so corrects for voltage drops and provide optimum output accuracy.
5. Provide adequate device heat-sinking. Use an array of heat-sinking vias to connect the exposed pad to the ground plane on the bottom PCB layer. If the PCB has multiple copper layers, these thermal vias can also be connected to inner layer heat-spreading ground planes. For best results use a 10 × 10 via array (or greater) with a minimum via diameter of 12 mil thermal vias spaced 46.8 mil apart. Ensure enough copper area is used for heat-sinking to keep the junction temperature below 125°C.

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10.1.2 Compact Layout for EMI Reduction

Radiated EMI is generated by the high di/dt components in pulsing currents in switching converters. The larger the area covered by the path of a pulsing current, the more electromagnetic emission is generated. The key to minimize radiated EMI is to identify the pulsing current path and minimize the area of the path. In buck converters, the pulsing current path is from the V_{IN} side of the input capacitors to HS switch, to the LS switch, and then return to the ground of the input capacitors, as shown in 図 10-1.

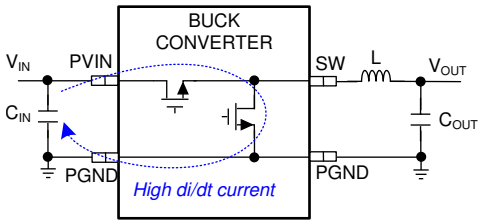


図 10-1. Buck Converter High di / dt Path

High frequency ceramic bypass capacitors at the input side provide primary path for the high di/dt components of the pulsing current. Placing ceramic bypass capacitor or capacitors as close as possible to the PVIN and PGND pins is the key to EMI reduction. The SW pin connecting to the inductor must be as short as possible, and just wide enough to carry the load current without excessive heating. Short, thick traces or copper pours (shapes) must be used for high current conduction path to minimize parasitic resistance. The output capacitors must be placed close to the V_{OUT} end of the inductor and closely grounded to PGND pin and exposed PAD. Place the bypass capacitors on VCC and BIAS pins as close as possible to the pins respectively and closely grounded to PGND and the exposed PAD.

10.1.3 Ground Plane and Thermal Considerations

TI recommends using one of the middle layers as a solid ground plane. Ground plane provides shielding for sensitive circuits and traces. It also provides a quiet reference potential for the control circuitry. Connect the AGND and PGND pins to the ground plane using vias right next to the bypass capacitors. PGND pins are connected to the source of the internal LS switch; connect the PGND pins directly to the grounds of the input and output capacitors. The PGND net contains noise at the switching frequency and can bounce due to load variations. The PGND trace, as well as PVIN and SW traces, must be constrained to one side of the ground plane. The other side of the ground plane contains much less noise — use for sensitive routes.

Provide adequate device heat sinking by utilizing the PAD of the device as the primary thermal path. Use a minimum 4 x 4 array of 10-mil thermal vias to connect the PAD to the system ground plane for heat sinking. Distribute the vias evenly under the PAD. Use as much copper as possible for system ground plane on the top and bottom layers for the best heat dissipation. TI recommends using a four-layer board with the copper thickness, for the four layers, starting from the top one, 2 oz / 1 oz / 1 oz / 2 oz. Four layer boards with enough copper thickness and proper layout provides low current conduction impedance, proper shielding and lower thermal resistance.

The thermal characteristics of the LM76005-Q1 are specified using the parameter $R_{\theta JA}$, which characterize the junction temperature of the silicon to the ambient temperature in a specific system. Although the value of $R_{\theta JA}$ is dependant on many variables, it still can be used to approximate the operating junction temperature of the device.

To obtain an estimate of the device junction temperature, you can use the following relationship:

$$T_J = P_D \times R_{\theta JA} + T_A \quad (28)$$

where

- T_J = junction temperature in °C
- $P_D = V_{IN} \times I_{IN} \times (1 - \text{efficiency}) - (1.1 \times (I_{OUT})^2 \times \text{DCR})$
- DCR = inductor DC parasitic resistance in Ω
- $R_{\theta JA}$ = junction-to-ambient thermal resistance of the device in °C/W

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- T_A = ambient temperature in °C.

The maximum operating junction temperature of the LM76005-Q1 is 125°C. $R_{\theta JA}$ is highly related to PCB size and layout, as well as environmental factors such as heat sinking and air flow. 図 10-2 shows measured results of $R_{\theta JA}$ with different copper area on a 2-layer board and a 4-layer board.

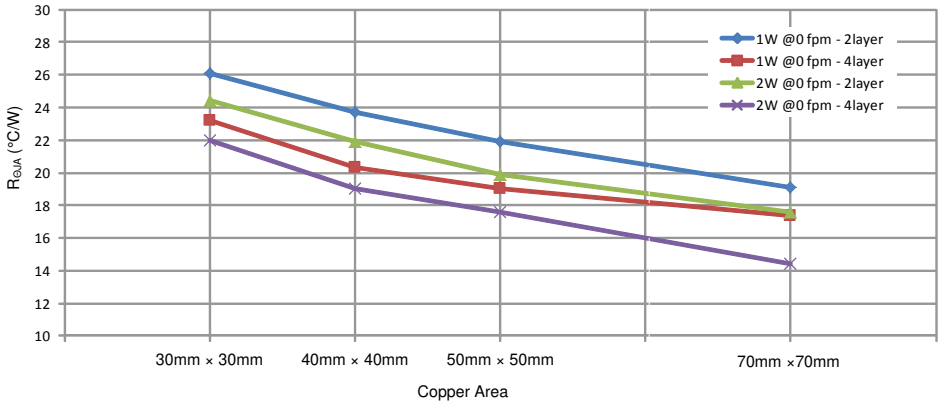


図 10-2. Measured $R_{\theta JA}$ versus PCB Copper Area on a 2-Layer Board and a 4-Layer Board

10.1.4 Feedback Resistors

To reduce noise sensitivity of the output voltage feedback path, it is important to place the resistor divider and C_{FF} close to the FB pin, rather than close to the load. The FB pin is the input to the error amplifier, so it is a high impedance node and very sensitive to noise. Placing the resistor divider and C_{FF} closer to the FB pin reduces the trace length of FB signal and reduces noise coupling. The output node is a low impedance node, so the trace from V_{OUT} to the resistor divider can be long if short path is not available.

If voltage accuracy at the load is important, make sure voltage sense is made at the load. Doing so corrects for voltage drops along the traces and provide the best output accuracy. The voltage sense trace from the load to the feedback resistor divider must be routed away from the SW node path, the inductor, and VIN path to avoid contaminating the feedback signal with switch noise, while also minimizing the trace length. This is most important when high value resistors are used to set the output voltage. TI recommends routing the voltage sense trace on a different layer than the inductor, SW node, and VIN path, such that there is a ground plane in between the feedback trace and inductor / SW node / VIN polygon. This provides further shielding for the voltage feedback path from switching noises.

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10.2 Layout Example

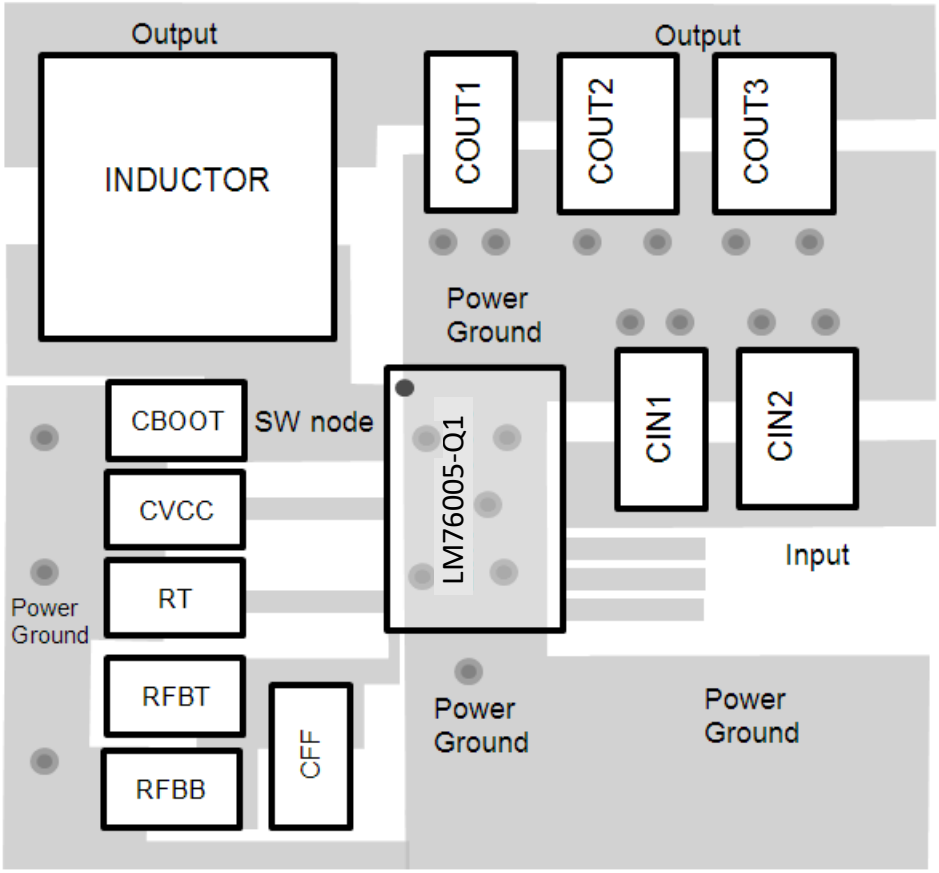


図 10-3. LM76005-Q1 Layout

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11 Device and Documentation Support

11.1 Device Support

11.1.1 Development Support

11.1.1.1 Custom Design With WEBENCH® Tools

Click here to create a custom design using the LM76005-Q1 device with the WEBENCH® Power Designer.

1. Start by entering the input voltage (V_{IN}), output voltage (V_{OUT}), and output current (I_{OUT}) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance
- Run thermal simulations to understand board thermal performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

11.2 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、ti.com のデバイス製品フォルダを開いてください。*「更新通知を受け取る」をクリック*して登録すると、変更されたすべての製品情報の 1 週間分のダイジェストを受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

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12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LM76005QRNPRQ1	Active	Production	WQFN (RNP) | 30	3000 | LARGE T&R	Yes	NIPDAU | SN	Level-2-260C-1 YEAR	-40 to 125	LM76005R NPQ1
LM76005QRNPRQ1.B	Active	Production	WQFN (RNP) | 30	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	LM76005R NPQ1

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF LM76005-Q1 :

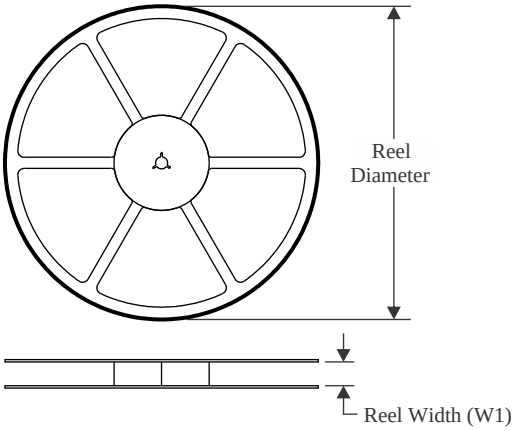
- Catalog : LM76005

NOTE: Qualified Version Definitions:

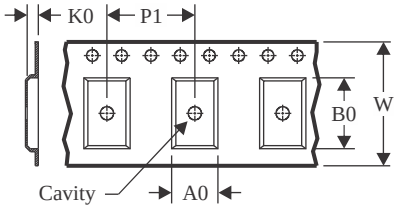
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

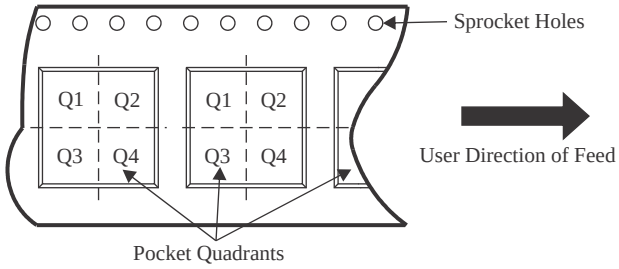


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

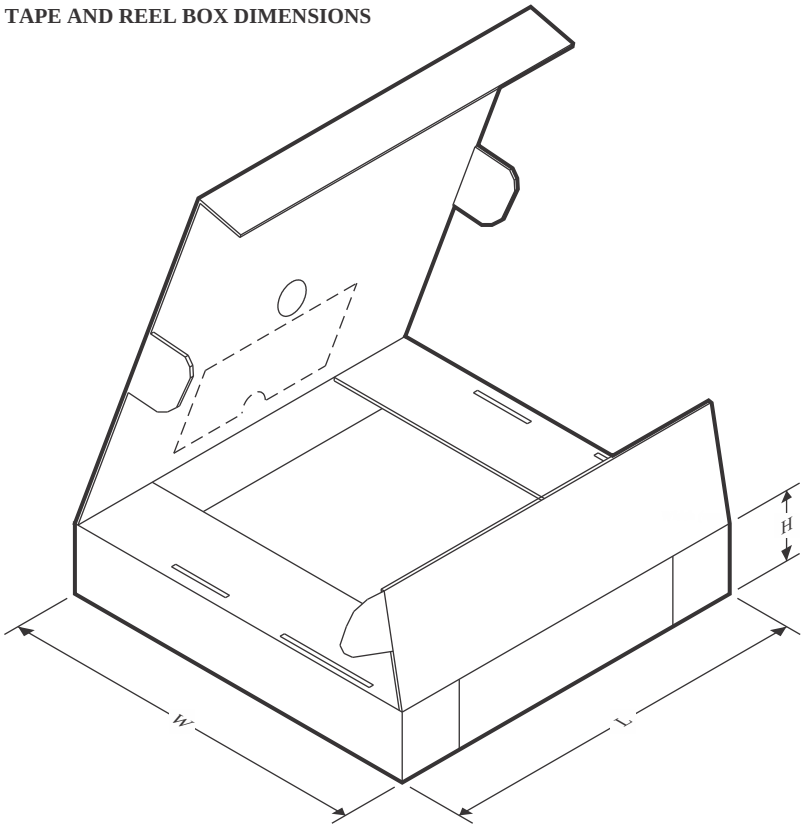
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM76005QRNPRQ1	WQFN	RNP	30	3000	330.0	12.4	4.3	6.3	1.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM76005QRNPRQ1	WQFN	RNP	30	3000	367.0	367.0	35.0

GENERIC PACKAGE VIEW

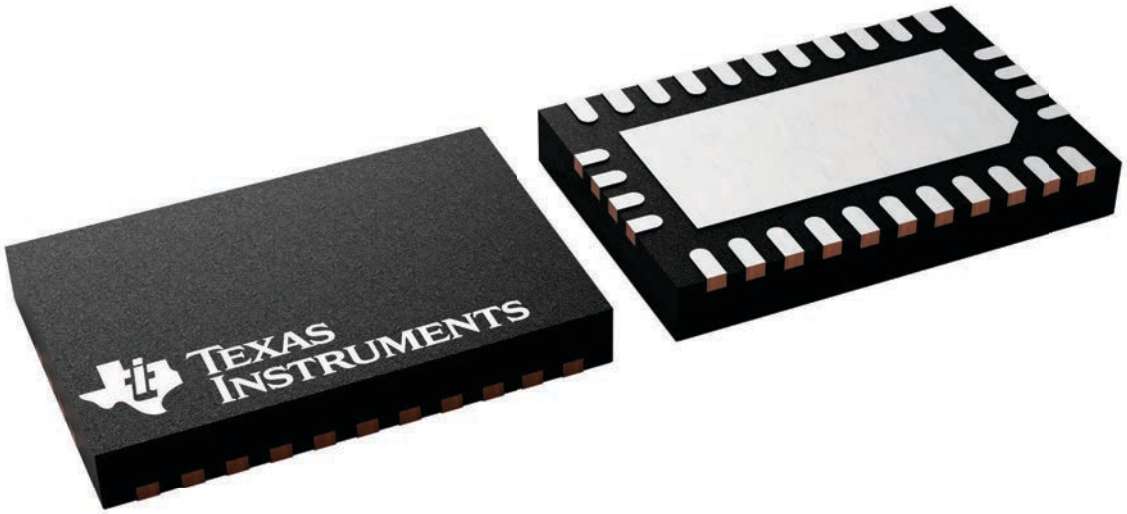
RNP 30

WQFN - 0.8 mm max height

4 x 6, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



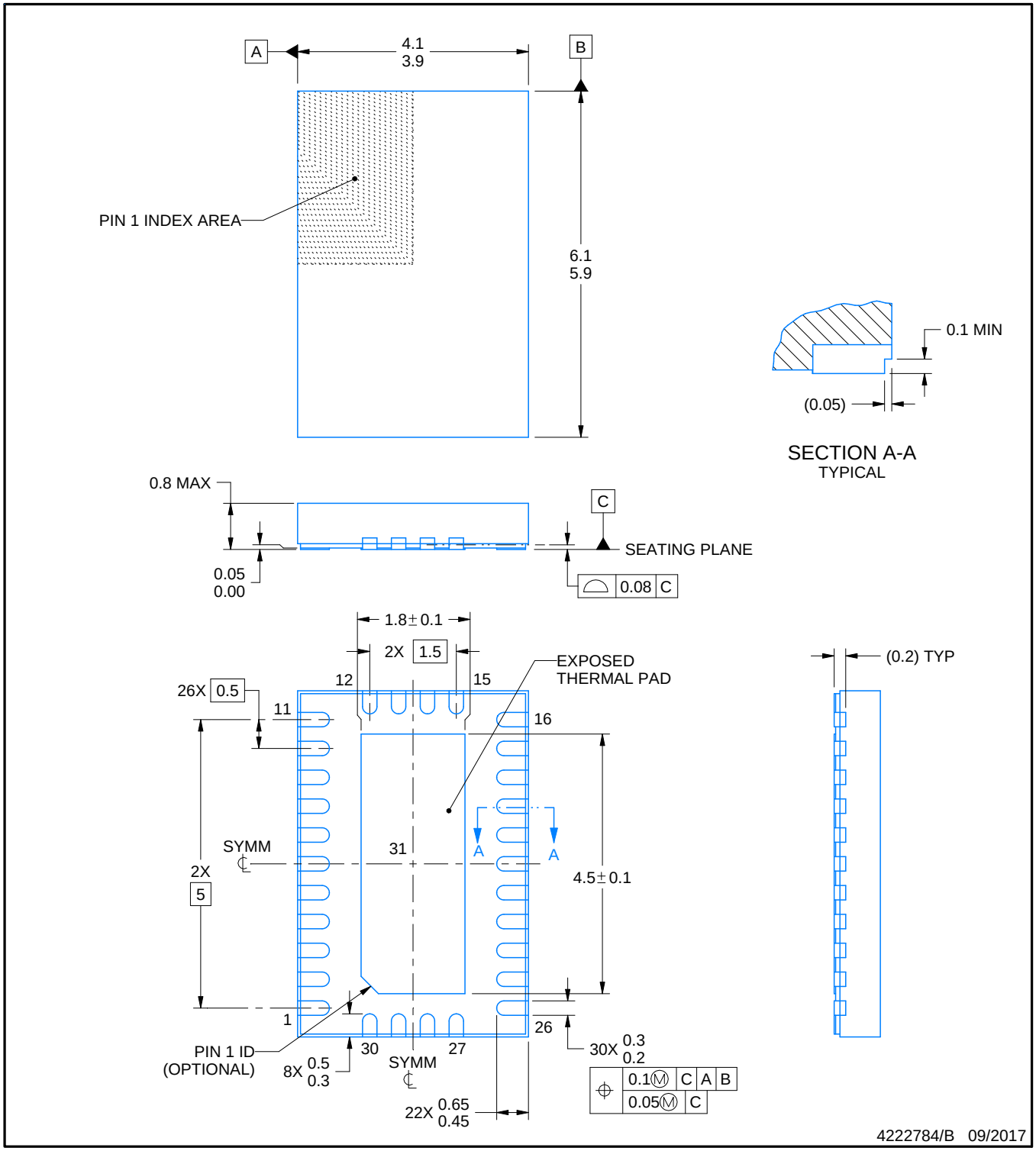
4225831/A

PACKAGE OUTLINE

RNP0030B

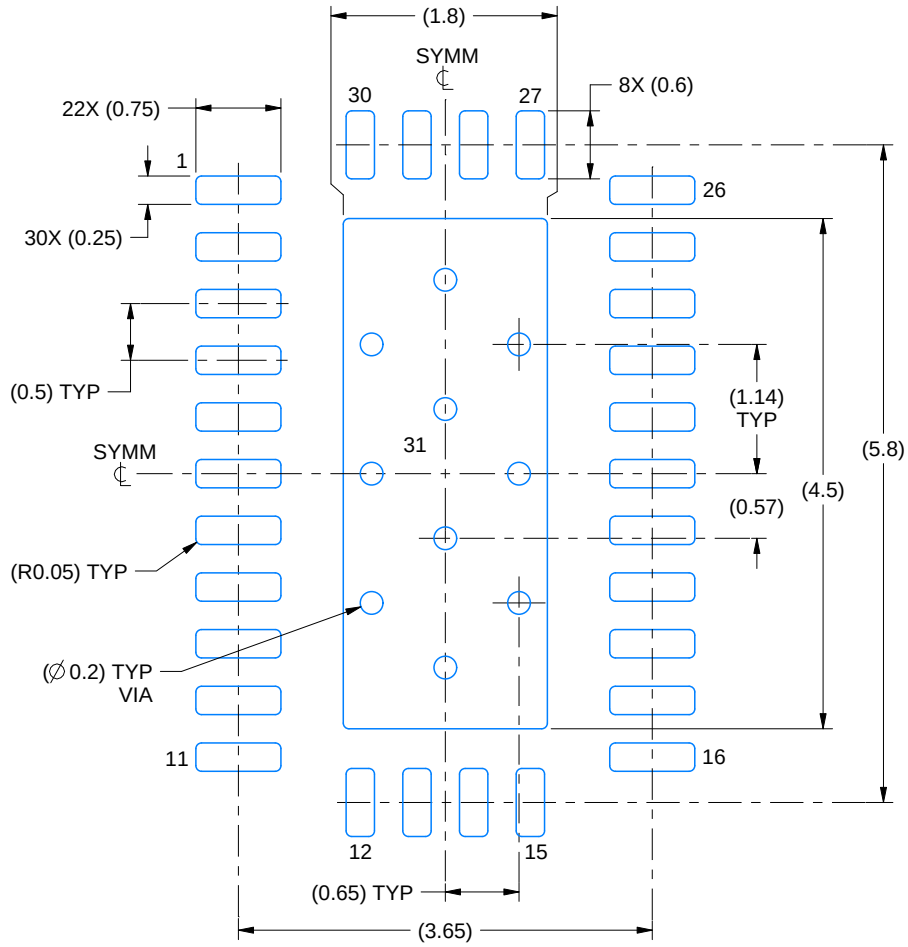
WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

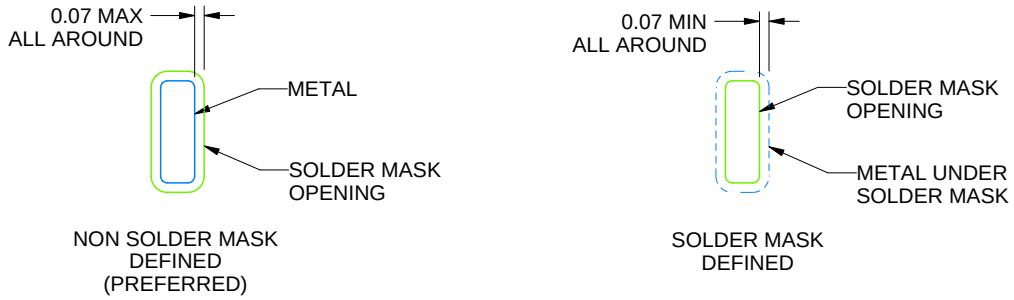


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:15X

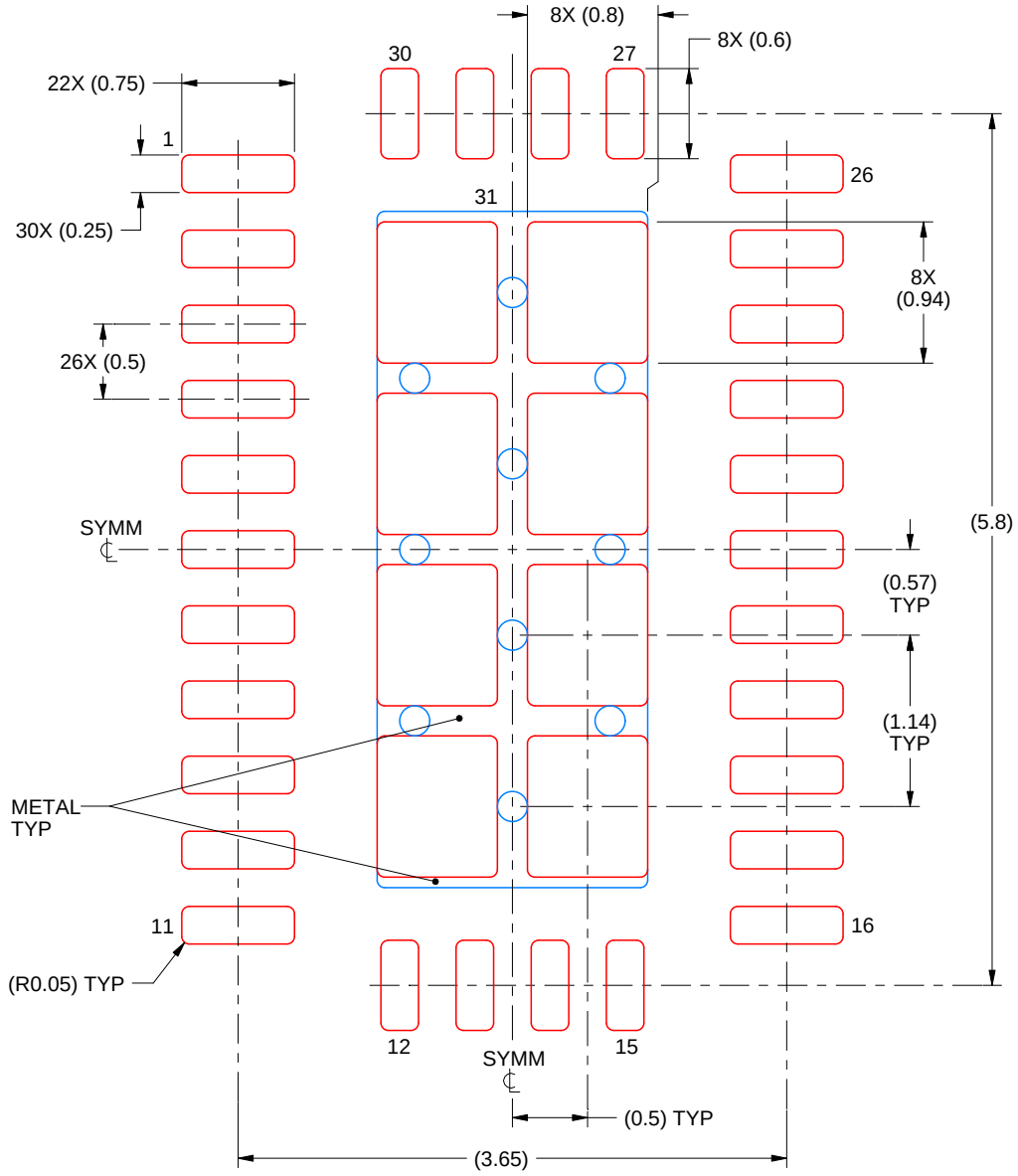


SOLDER MASK DETAILS

4222784/B 09/2017

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 31:
74.3% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

4222784/B 09/2017

NOTES: (continued)

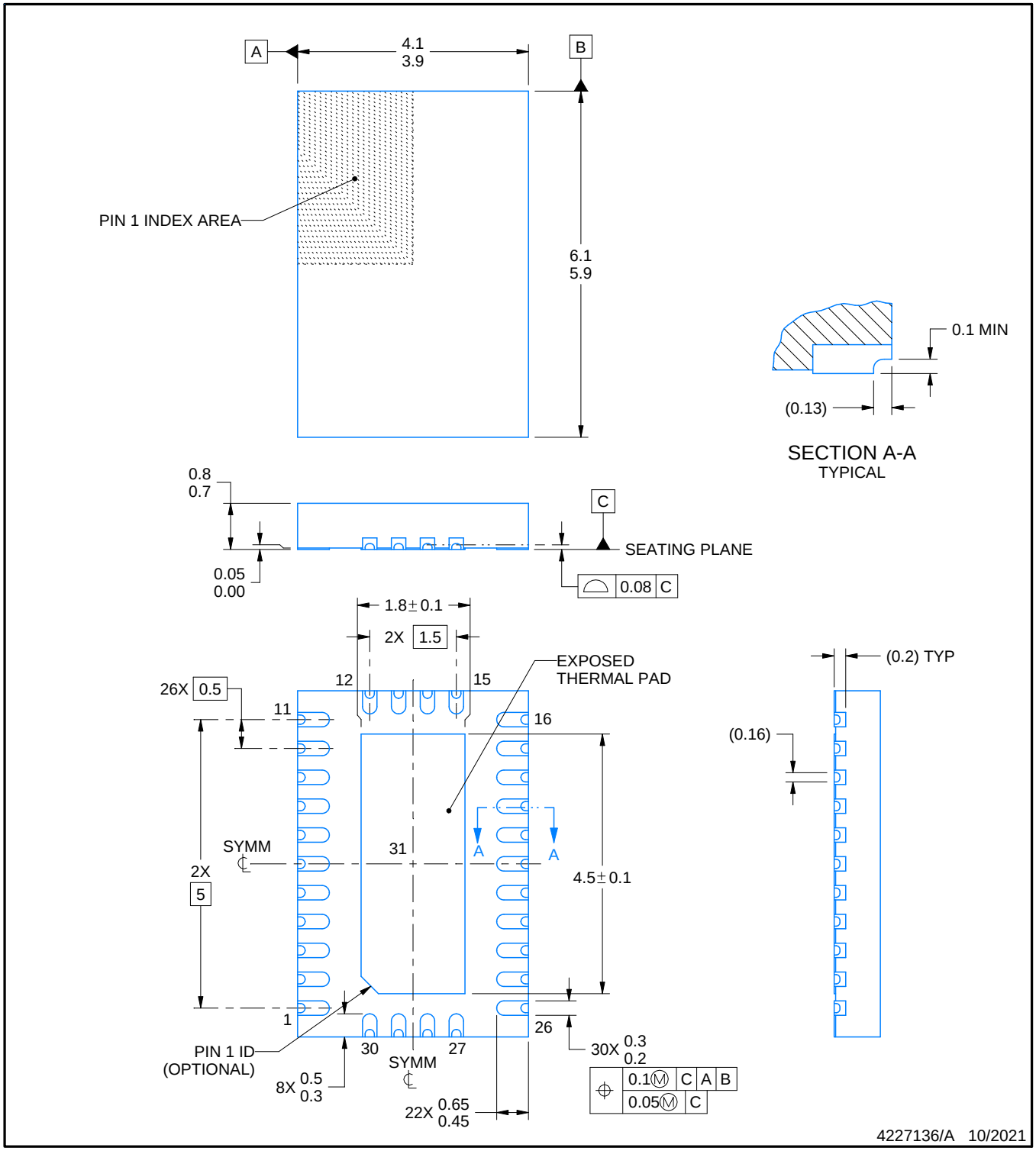
6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

RNP0030E

PACKAGE OUTLINE

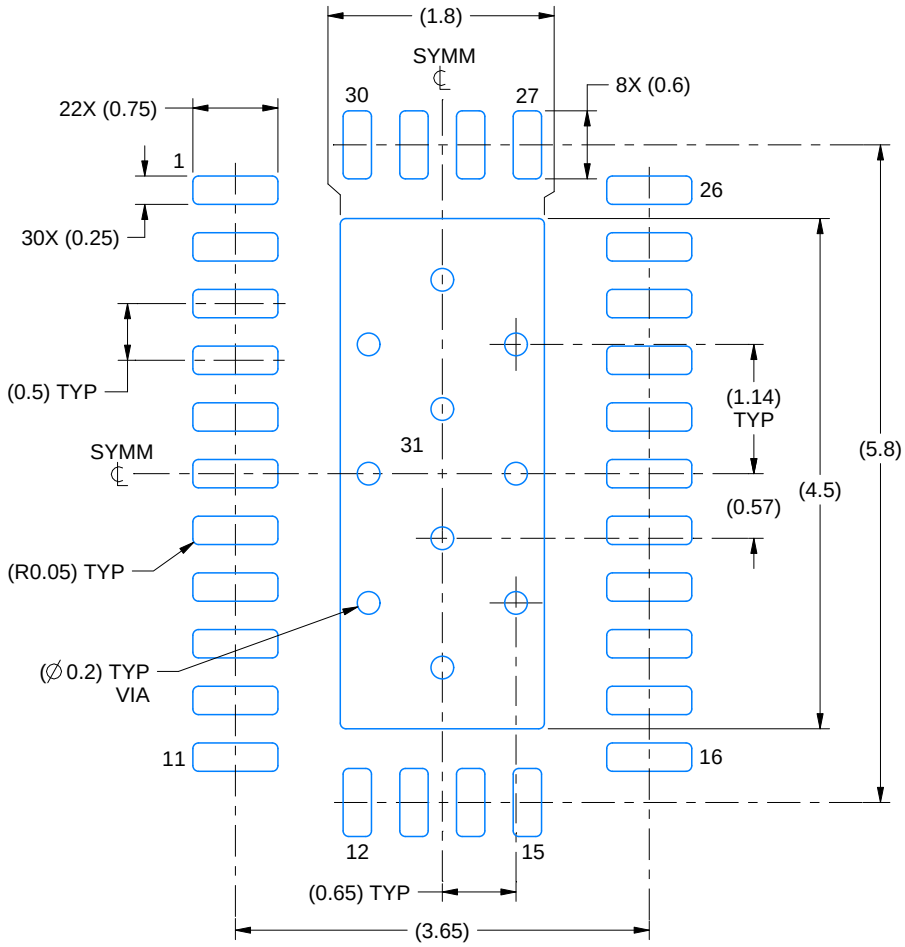
WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

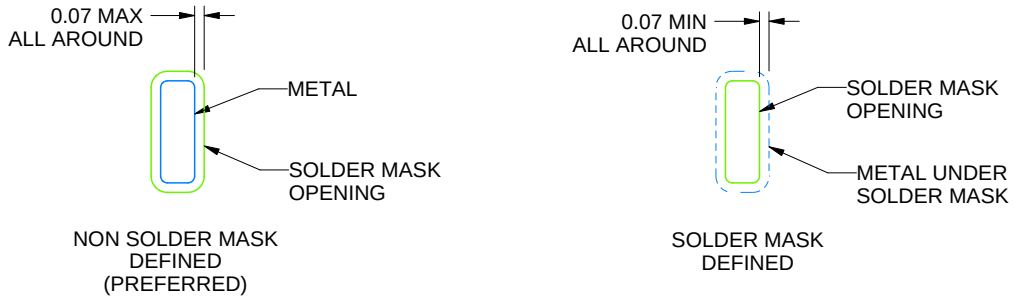


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:15X

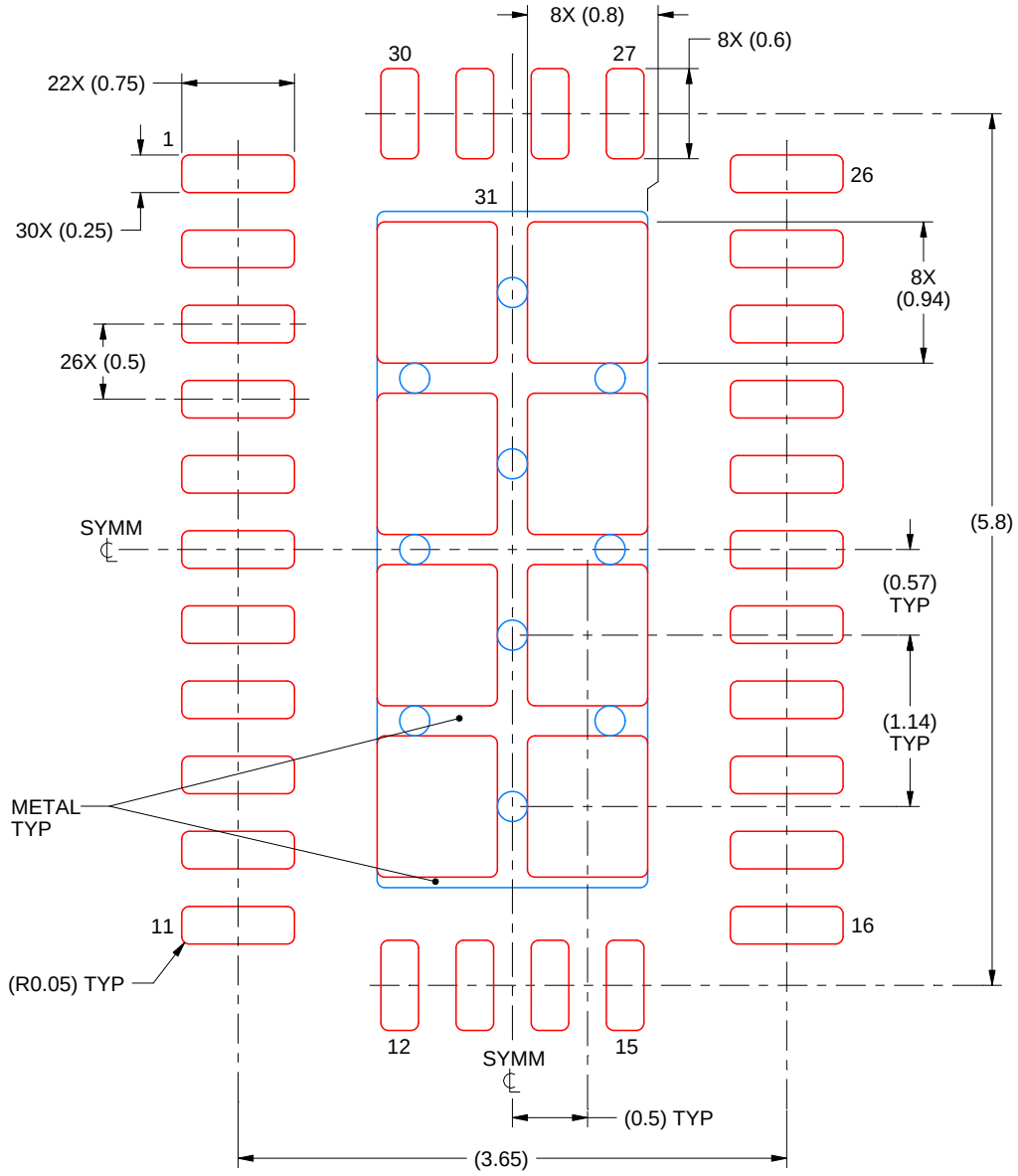


SOLDER MASK DETAILS

4227136/A 10/2021

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 31:
74.3% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

4227136/A 10/2021

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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最終更新日：2025 年 10 月