TEXAS INSTRUMENTS
LMG2610
JAJSLV7A – OCTOBER 2022 – REVISED DECEMBER 2022

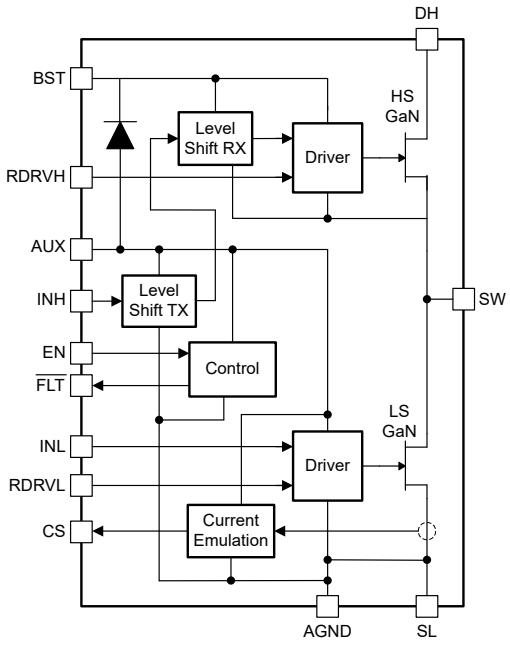
LMG2610 アクティブ・クランプ用 650V GaN ハーフブリッジを内蔵したフライバック・コンバータ

1 特長

- 650V GaN パワー FET ハーフブリッジ
- 170mΩ ローサイドおよび 248mΩ ハイサイド GaN FET
- 伝搬遅延が小さく、ターンオン・スルーレート制御を調整可能な内蔵ゲート・ドライバ
- 広い帯域幅で高精度の電流検出エミュレーション
- ローサイド / ハイサイド・ゲート・ドライブ・インターロック
- ハイサイド・ゲート・ドライブ信号レベル・シフタ
- スマート・スイッチ付きブートストラップ・ダイオード機能
- ハイサイドの起動:8µs 未満
- ローサイド / ハイサイドのサイクルごとの過電流保護
- $\overline{\text{FLT}}$ ピン通知付きの過熱保護
- AUX アイドル静止電流:240µA
- AUX スタンバイ静止電流:50µA
- BST アイドル静止電流:60µA
- 電源および入力ロジック・ピン最大電圧:26V
- デュアル・サーマル・パッド付き 9mm x 7mm QFN パッケージ

2 アプリケーション

- アクティブ・クランプ・フライバック・パワー・コンバータ
- AC/DC アダプタおよびチャージャ
- AC/DC USB 壁コンセント電源
- AC/DC 補助電源



概略ブロック図

3 概要

LMG2610 は、スイッチ・モード電源アプリケーションの 75W 未満のアクティブ・クランプ・フライバック (ACF) コンバータに適した 650V GaN パワー FET ハーフブリッジです。LMG2610 は、ハーフブリッジ・パワー FET、ゲート・ドライバ、ブートストラップ・ダイオード、ハイサイド・ゲート・ドライブ・レベル・シフタを 9mm x 7mm の QFN パッケージに統合することで、設計の簡素化、部品点数の低減、基板面積の低減を実現しています。

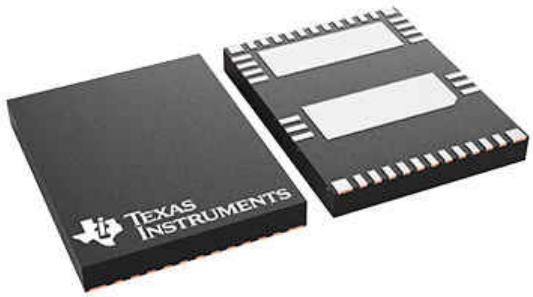
GaN FET の非対称の抵抗値は、ACF の動作条件に合わせて最適化されています。プログラマブルなターンオン・スルーレートにより、EMI とリンギングを制御できます。ローサイド電流検出エミュレーションにより、従来の電流検出抵抗方式よりも消費電力を低減でき、またローサイドのサーマル・パッドを冷却用 PCB 電源グランドに接続できます。

ハイサイド・ゲート・ドライブ信号レベル・シフタにより、外付けソリューションに見られるノイズとバースト・モード電力消費の問題を解消できます。スマート・スイッチ付き GaN ブートストラップ FET を使うと、ダイオードの順方向電圧降下がなく、ハイサイド電源を過充電せず、逆方向回復電荷がありません。

LMG2610 は、小さい静止電流と高速な起動時間によって、コンバータの軽負荷効率要件とバースト・モード動作に対応しています。保護機能には、FET ターンオン・インターロック、低電圧誤動作防止 (UVLO)、サイクル単位の電流制限、過熱シャットダウンが含まれます。

製品情報

部品番号	パッケージ (1)	本体サイズ (公称)
LMG2610	QFN	9.00mm × 7.00mm



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4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision * (October 2022) to Revision A (December 2022)	Page
• データシートのステータスを「事前情報」から「量産データ」に変更	1

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5 Pin Configuration and Functions

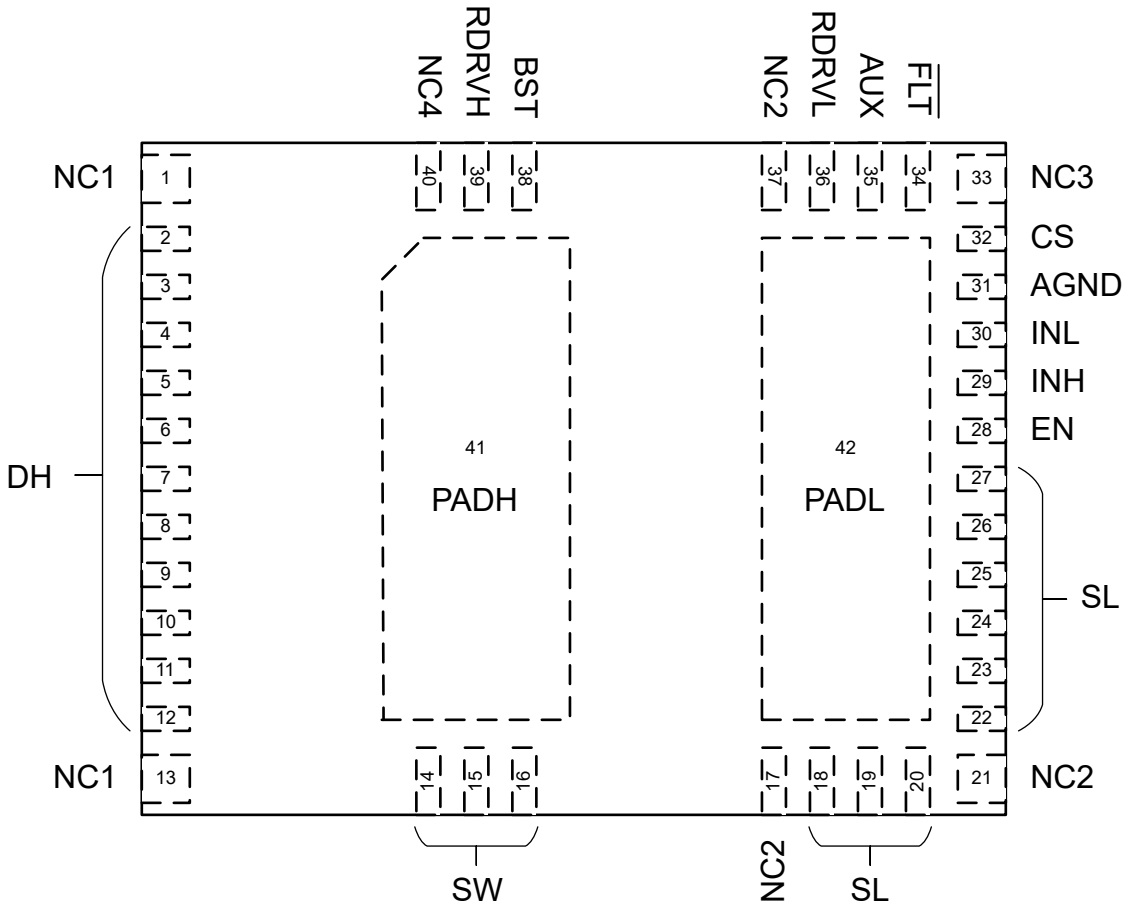


図 5-1. RRG Package, 40-Pin VQFN (Top View)

表 5-1. Pin Functions

PIN		TYPE[1]	DESCRIPTION
NAME	NO.		
NC1	1, 13	NC	Used to anchor QFN package to PCB. Pins must be soldered to PCB landing pads. The PCB landing pads are non-solder mask defined pads and must not be physically connected to any other metal on the PCB. Internally connected to DH.
DH	2-12	P	High-side GaN FET drain. Internally connected to NC1.
SW	14-16	P	GaN FET half-bridge switch node between the high-side GaN FET source and low-side GaN FET drain. Internally connected to PADH.
NC2	17, 21, 37	NC	Used to anchor QFN package to PCB. Pins must be soldered to PCB landing pads. The PCB landing pads are non-solder mask defined pads and must not be physically connected to any other metal on the PCB. Internally connected to AGND, SL, and PADL.
SL	18-20, 22-27	P	Low-side GaN FET source. Internally connected to AGND, PADL, and NC2.
EN	28	I	Enable. Used to toggle between active and standby modes. The standby mode has reduced quiescent current to support converter light load efficiency targets. There is a forward biased ESD diode from EN to AUX so avoid driving EN higher than AUX.
INH	29	I	High-side gate-drive control input. Referenced to AGND. Signal is level shifted internally to the high-side GaN FET driver. There is a forward biased ESD diode from INH to AUX so avoid driving INH higher than AUX.
INL	30	I	Low-side gate-drive control input. Referenced to AGND. There is a forward biased ESD diode from INL to AUX so avoid driving INL higher than AUX.
AGND	31	GND	Low-side analog ground. Internally connected to SL, PADL, and NC2.
CS	32	O	Current-sense emulation output. Outputs 1 ma/A scaled replica of the low-side GaN FET current. Feed output current into a resistor to create a current sense voltage signal. Reference the resistor to the power supply controller IC local ground. This function replaces the external current-sense resistor that is used in series with the low-side FET.
NC3	33	NC	Used to anchor QFN package to PCB. Pin must be soldered to a PCB landing pad. The PCB landing pad is non-solder mask defined pad and must not be physically connected to any other metal on the PCB. Pin not connected internally.
$\overline{FLT}$	34	O	Active-low fault output. Open-drain output that asserts during an over-temperature shut down.
AUX	35	P	Auxiliary voltage rail. Low-side supply voltage. Connect a local bypass capacitor between AUX and AGND.
RDRVL	36	I	Low-side drive strength control resistor. Set a resistance between RDRVL and AGND to program the low-side GaN FET turn-on slew rate.
BST	38	P	Bootstrap voltage rail. High-side supply voltage. The bootstrap diode function between AUX and BST is internally provided. Connect an appropriately sized bootstrap capacitor between BST and SW. Recommend to make the SW connection using NC4 as a pass through connection to PADH (PADH = SW) as explained in the NC4 description.
RDRVH	39	I	High-side drive strength control resistor. Set a resistance between RDRVH and SW to program the high-side GaN FET turn-on slew rate. Recommend to make the SW connection using NC4 as a pass through connection to PADH (PADH = SW) as explained in the NC4 description.
NC4	40	NC	Pin is not functional. Pin is high impedance and referenced to SW. Recommend to connect pin to PADH (PADH = SW) to use as convenient connection for the BST bypass capacitor and the RDRVH resistor. See the example board layout in the *Layout Example* section.
PADH	41	TP	High-side thermal pad. Internally connected to SW. All the SW current can be conducted with PADH (PADH = SW).
PADL	42	TP	Low-side thermal pad. Internally connected to SL, AGND, and NC2. All the SL current can be conducted with PADL (PADL = SL).

(1) I = Input, O = Output, G = Ground, P = Power, NC = No Connect, TP = Thermal Pad.

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6 Specifications

6.1 Absolute Maximum Ratings

Unless otherwise noted: voltages are respect to AGND(1)

			MIN	MAX	UNIT
$V_{DS(ls)}$	Low-side drain-source (SW to SL) voltage, FET off			650	V
$V_{DS(surge)(ls)}$	Low-side drain-source (SW to SL) voltage, surge condition, FET off (2)			720	V
$V_{DS(tr)(surge)(ls)}$	Low-side drain-source (SW to SL) transient ringing peak voltage, surge condition, FET off (2)			800	V
$V_{DS(hs)}$	High-side drain source (DH to SW) voltage, FET off			650	V
$V_{DS(surge)(hs)}$	High-side drain-source (DH to SW) voltage, surge condition, FET off (2)			720	V
$V_{DS(tr)(surge)(hs)}$	High-side drain-source (DH to SW) transient ringing peak voltage, surge condition, FET off (2)			800	V
	Pin voltage	AUX	–0.3	30	V
		EN, INL, INH, $\overline{FLT}$	–0.3	V_{AUX} + 0.3	V
		CS	–0.3	5.5	V
		RDRVL	–0.3	4	V
	Pin voltage to SW	BST	–0.3	30	V
		RDRVH	–0.3	4	V
$I_{D(peak)(ls)}$	Low-side drain (SW to SL) peak current, FET on		–6.4	Internally limited	A
$I_{S(peak)(ls)}$	Low-side source (SL to SW) peak current, FET off			6.4	A
$I_{D(peak)(hs)}$	High-side drain (DH to SW) peak current, FET on		–4	Internally limited	A
$I_{S(peak)(hs)}$	High-side source (SW to DH) peak current, FET off			4	A
	Positive sink current	CS		10	mA
		$\overline{FLT}$ (while asserted)		Internally limited	mA
T_J	Operating junction temperature		–40	150	°C
T_{stg}	Storage temperature		–65	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) See GaN Power FET Switching Capability for more information on the GaN FET switching capability.

6.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	Pins1 through 16, Pins 38 through 40	±1000	V
			Pins 17 through 37	±2000	V
		Charged device model (CDM), per ANSI/ESDA/JEDEC JS-002(2)		±500	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

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6.3 Recommended Operating Conditions

Unless otherwise noted: voltages are respect to AGND

			MIN	NOM	MAX	UNIT
	Supply voltage	AUX	10		26	V
	Supply voltage to SW	BST	7.5		26	V
	Input voltage	EN, INL, INH	0		V_{AUX}	V
	Pull-up voltage on open-drain output	$\overline{FLT}$	0		V_{AUX}	V
V_{IH}	High-level input voltage	EN, INL, INH	2.5			V
V_{IL}	Low-level input voltage				0.6	V
$I_{D(peak)(ls)}$	Low-side drain (SW to SL) peak current, FET on		–3.2		5.4	A
$I_{D(peak)(hs)}$	High-side drain (DH to SW) peak current, FET on		–2		3	A
C_{AUX}	AUX to AGND capacitance from external bypass capacitor		3 x C_{BST}			µF
C_{BST_SW}	BST to SW capacitance from external bypass capacitor		0.010			µF
R_{RDRVL}	RDRVL to AGND resistance from external slew-rate control resistor to configure below low-side slew rate settings					
	slew rate setting 0 (slowest)		90	120	open	kΩ
	slew rate setting 1		42.5	47	51.5	kΩ
	slew rate setting 2		20	22	24	kΩ
	slew rate setting 3 (fastest)		0	5.6	11	kΩ
R_{RDRVH_SW}	RDRVH to SW resistance from external slew-rate control resistor to configure below high-side slew rate settings					
	slew rate setting 0 (slowest)		90	120	open	kΩ
	slew rate setting 1		42.5	47	51.5	kΩ
	slew rate setting 2		20	22	24	kΩ
	slew rate setting 3 (fastest)		0	5.6	11	kΩ

6.4 Thermal Information

THERMAL METRIC[1]		LMG2610 RRG (VQFN) 40 Pins	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	25.3	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	1.22	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

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6.5 Electrical Characteristics

1) Symbol definitions: $V_{DS(ls)}$ = SW to SL voltage; $I_{DS(ls)}$ = SW to SL current; $V_{DS(hs)}$ = DH to SW voltage; $I_{D(hs)}$ = DH to SW current; 2) Unless otherwise noted: voltage, resistance, and capacitance are respect to AGND; -40 °C ≤ T_J ≤ 125 °C; 10 ≤ V_{AUX} ≤ 26; 7.5 ≤ V_{BST_SW} ≤ 26; V_{EN} = 5 V; V_{INL} = 0 V; V_{INH} = 0 V; R_{RDRVL} = 0 Ω; R_{RDRVH_SW} = 0 Ω; R_{CS} = 100 Ω

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
LOW-SIDE GAN POWER FET						
$R_{DS(on)(ls)}$	Drain-source (SW to SL) on resistance	V_{INL} = 5 V, $I_{D(ls)}$ = 3 A, T_J = 25°C		170		mΩ
		V_{INL} = 5 V, $I_{D(ls)}$ = 3 A, T_J = 125°C		325		
$V_{SD(ls)}$	Source-drain (SL to SW) third-quadrant voltage	SL to SW current = 0.1 A		-1.9		V
		SL to SW current = 1 A		-2.6		
$I_{DSS(ls)}$	Drain (SW to SL) leakage current	$V_{DS(hs)}$ = 0 V, $V_{DS(ls)}$ = 650 V, T_J = 25 °C		2		μA
		$V_{DS(hs)}$ = 0 V, $V_{DS(ls)}$ = 650 V, T_J = 125 °C		10		
$Q_{OSS(ls)}$	Output (SW to SL) charge	$V_{DS(hs)}$ = 0 V, $V_{DS(ls)}$ = 400 V		19.7		nC
$C_{OSS(ls)}$	Output (SW to SL) capacitance			22		pF
$E_{OSS(ls)}$	Output (SW to SL) capacitance stored energy			2.32		μJ
$C_{OSS,er(ls)}$	Energy related effective output (SW to SL) capacitance			29		pF
$C_{OSS,tr(ls)}$	Time related effective output (SW to SL) capacitance	$V_{DS(hs)}$ = 0 V, $V_{DS(ls)}$ = 0 V to 400 V		49.2		pF
$Q_{RR(ls)}$	Reverse recovery charge			0		nC
HIGH-SIDE GAN POWER FET						
$R_{DS(on)(hs)}$	Drain-source (DH to SW) on resistance	V_{INH} = 5 V, $I_{D(hs)}$ = 1.75 A, T_J = 25°C		248		mΩ
		V_{INH} = 5 V, $I_{D(hs)}$ = 1.75 A, T_J = 125°C		470		
$V_{SD(hs)}$	Source-drain (SW to DH) third-quadrant voltage	SW to DH current = 0.1 A		-2		V
		SW to DH current = 1 A		-2.7		
$I_{DSS(hs)}$	Drain (DH to SW) leakage current	$V_{DS(ls)}$ = 0 V, $V_{DS(hs)}$ = 650 V, T_J = 25 °C		1.4		μA
		$V_{DS(ls)}$ = 0 V, $V_{DS(hs)}$ = 650 V, T_J = 125 °C		7		
$Q_{OSS(hs)}$	Output (DH to SW) charge	$V_{DS(ls)}$ = 0 V, $V_{DS(hs)}$ = 400 V		15.51		nC
$C_{OSS(hs)}$	Output (DH to SW) capacitance			22.4		pF
$E_{OSS(hs)}$	Output (DH to SW) capacitance stored energy			2.15		μJ
$C_{OSS,er(hs)}$	Energy related effective output (DH to SW) capacitance			26.9		pF
$C_{OSS,tr(hs)}$	Time related effective output (DH to SW) capacitance	$V_{DS(ls)}$ = 0 V, $V_{DS(hs)}$ = 0 V to 400 V		38.78		pF
$Q_{RR(hs)}$	Reverse recovery charge			0		nC
LOW-SIDE OVERCURRENT PROTECTION						
$I_{T(OC)(ls)}$	Overcurrent fault – threshold current		5.4	5.9	6.4	A
HIGH-SIDE OVERCURRENT PROTECTION						
$I_{T(OC)(hs)}$	Overcurrent fault – threshold current		3	3.5	4	A
BOOTSTRAP RECTIFIER						
$R_{DS(on)}$	AUX to BST on resistance	V_{INL} = 5 V, V_{AUX_BST} = 1 V, T_J = 25°C		8		Ω
		V_{INL} = 5 V, V_{AUX_BST} = 1 V, T_J = 125°C		14		
	AUX to BST current limit	V_{INL} = 5 V, V_{AUX_BST} = 7 V	210	240	270	mA
	BST to AUX reverse current blocking threshold	V_{INL} = 5 V		15		mA

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1) Symbol definitions: $V_{DS(ls)}$ = SW to SL voltage; $I_{DS(ls)}$ = SW to SL current; $V_{DS(hs)}$ = DH to SW voltage; $I_{D(hs)}$ = DH to SW current; 2) Unless otherwise noted: voltage, resistance, and capacitance are respect to AGND; -40 °C ≤ T_J ≤ 125 °C; 10 ≤ V_{AUX} ≤ 26; 7.5 ≤ V_{BST_SW} ≤ 26; V_{EN} = 5 V; V_{INL} = 0 V; V_{INH} = 0 V; R_{RDRVL} = 0 Ω; R_{RDRVH_SW} = 0 Ω; R_{CS} = 100 Ω

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
CS						
	Current sense gain ($I_{CS(src)}$ / $I_{D(LS)}$)	V_{INL} = 5 V, 0 A ≤ $I_{D(ls)}$ < $I_{T(OC)(ls)}$, 0 V ≤ V_{CS} ≤ 2 V		1		mA/A
	Current sense input offset current	V_{INL} = 5 V, 0 A ≤ $I_{D(ls)}$ < $I_{T(OC)(ls)}$, 0 V ≤ V_{CS} ≤ 2 V	–50		50	mA
	Initial held output after overcurrent fault occurs while INL remains high	V_{INL} = 5 V, 0 V ≤ V_{CS} ≤ 2 V			7	mA
$I_{CS(src)(OC)(final)}$	Final held output after overcurrent fault occurs while INL remains high	V_{INL} = 5 V, 0 V ≤ V_{CS} ≤ 2 V	10	12	15.5	mA
	Output clamp voltage	V_{INL} = 5 V, $I_{D(ls)}$ = 5 A, CS sinking 5 mA from external source		2.5		V
EN, INL, INH						
V_{IT+}	Positive-going input threshold voltage		1.7		2.45	V
$V_{IT–}$	Negative-going input threshold voltage		0.7		1.3	V
	Input threshold voltage hysteresis			1		V
	Pull-down resistance	0 V ≤ V_{PIN} ≤ 3 V	200	400	600	kΩ
	Pull-down current	V_{AUX} = 26 V; 10 V ≤ V_{PIN} ≤ 26 V		10		µA
OVER-TEMPERATURE PROTECTION						
	Temperature fault – postive-going threshold temperature			150		°C
	Temperature fault – negative-going threshold temperature			130		°C
	Temperature fault – threshold temperature hysteresis			20		°C
$\overline{FLT}$						
	Low-level output voltage	$\overline{FLT}$ sinking 1mA while asserted			200	mV
	Off-state current	$V_{\overline{FLT}}$ = V_{AUX} while de-asserted			1	µA
AUX						
$V_{AUX,T+(UVLO)}$	UVLO – positive-going threshold voltage		8.9	9.3	9.7	V
	UVLO – negative-going threshold voltage		8.6	9.0	9.4	V
	UVLO – threshold voltage hysteresis			250		mV
	Standby quiescent current	V_{EN} = 0 V		50	80	µA
	Quiescent current			250	370	µA
		V_{INL} = 5 V, $I_{D(ls)}$ = 0 A		1370		µA
	Operating current	V_{INL} = 0 V or 5 V, $V_{DS(ls)}$ = 0 V, f_{INL} = 500 kHz, $I_{D(ls)}$ = 0 A		3.1		mA
BST						
$V_{BST_SW,T+(UVLO)}$	V_{BST_SW} UVLO for FET to turn on – positive-going threshold voltage		6.7	7	7.3	V
	V_{BST_SW} UVLO for FET to stay on– negative-going threshold voltage		4.8	5.1	5.4	V
	Quiescent current			65	100	µA
		V_{INH} = 5 V		330		
	Operating current	V_{INH} = 0 V or 5 V, $V_{DS(hs)}$ = 0 V; f_{INH} = 500 kHz		1.2		mA

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6.6 Switching Characteristics

1) Symbol definitions: $V_{DS(ls)}$ = SW to SL voltage; $I_{DS(ls)}$ = SW to SL current; $V_{DS(hs)}$ = DH to SW voltage; $I_{D(hs)}$ = DH to SW current; 2) Unless otherwise noted: voltage, resistance, and capacitance are respect to AGND; -40 °C ≤ T_J ≤ 125 °C; 10 ≤ V_{AUX} ≤ 26; 7.5 ≤ V_{BST_SW} ≤ 26; V_{EN} = 5 V; V_{INL} = 0 V; V_{INH} = 0 V; R_{RDRVL} = 0 Ω; R_{RDRVH_SW} = 0 Ω; R_{CS} = 100 Ω

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
LOW-SIDE GAN POWER FET						
$t_{d(on)(Idrain)(ls)}$	Drain current turn-on delay time	From V_{INL} > $V_{INL,IT+}$ to $I_{D(ls)}$ > 50 mA, V_{BUS} = 400 V, L_{HB} current = 2 A, at below low-side slew rate settings, see GaN Power FET Switching Parameters				
		slew rate setting 0 (slowest)		68		ns
		slew rate setting 1		40		
		slew rate setting 2		35		
		slew rate setting 3 (fastest)		34		
$t_{d(on)(ls)}$	Turn-on delay time	From V_{INL} > $V_{INL,IT+}$ to $V_{DS(ls)}$ < 320 V, V_{BUS} = 400 V, L_{HB} current = 2 A, at below low-side slew rate settings, see GaN Power FET Switching Parameters				
		slew rate setting 0 (slowest)		91		ns
		slew rate setting 1		50		
		slew rate setting 2		43		
		slew rate setting 3 (fastest)		37		
$t_{r(on)(ls)}$	Turn-on rise time	From $V_{DS(ls)}$ < 320 V to $V_{DS(ls)}$ < 80 V, V_{BUS} = 400 V, L_{HB} current = 2 A, at below low-side slew rate settings, see GaN Power FET Switching Parameters				
		slew rate setting 0 (slowest)		14.9		ns
		slew rate setting 1		5.6		
		slew rate setting 2		3.8		
		slew rate setting 3 (fastest)		1.9		
$t_{d(off)(ls)}$	Turn-off delay time	From V_{INL} < $V_{INL,IT-}$ to $V_{DS(ls)}$ > 80 V, V_{BUS} = 400 V, L_{HB} current = 2 A, (independent of slew rate setting), see GaN Power FET Switching Parameters		43		ns
$t_{f(off)(ls)}$	Turn-off fall time	From $V_{DS(ls)}$ > 80 V to $V_{DS(ls)}$ > 320 V, V_{BUS} = 400 V, L_{HB} current = 2 A, (independent of slew rate setting), see GaN Power FET Switching Parameters		12.5		ns
	Turn-on slew rate	From $V_{DS(ls)}$ < 250 V to $V_{DS(ls)}$ < 150 V, T_J = 25 °C, V_{BUS} = 400 V, L_{HB} current = 2 A, at below low-side slew rate settings, see GaN Power FET Switching Parameters				
		slew rate setting 0 (slowest)		20		V/ns
		slew rate setting 1		50		
		slew rate setting 2		70		
		slew rate setting 3 (fastest)		140		

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1) Symbol definitions: $V_{DS(ls)}$ = SW to SL voltage; $I_{DS(ls)}$ = SW to SL current; $V_{DS(hs)}$ = DH to SW voltage; $I_{D(hs)}$ = DH to SW current; 2) Unless otherwise noted: voltage, resistance, and capacitance are respect to AGND; -40 °C ≤ T_J ≤ 125 °C; 10 ≤ V_{AUX} ≤ 26; 7.5 ≤ V_{BST_SW} ≤ 26; V_{EN} = 5 V; V_{INL} = 0 V; V_{INH} = 0 V; R_{RDRVL} = 0 Ω; R_{RDRVH_SW} = 0 Ω; R_{CS} = 100 Ω

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
HIGH-SIDE GAN POWER FET						
$t_{d(on)(Idrain)(hs)}$	Drain current turn-on delay time	From V_{INH} > $V_{INH,IT+}$ to $I_{D(hs)}$ > 50 mA, V_{BUS} = 400 V, L_{HB} current = 2 A, at below high-side slew rate settings, see GaN Power FET Switching Parameters				
		slew rate setting 0 (slowest)		60		ns
		slew rate setting 1		34		
		slew rate setting 2		31		
		slew rate setting 3 (fastest)		28		
$t_{d(on)(hs)}$	Turn-on delay time	From V_{INH} > $V_{INH,IT+}$ to $V_{DS(hs)}$ < 320 V, V_{BUS} = 400 V, L_{HB} current = 2 A, at below high-side slew rate settings, see GaN Power FET Switching Parameters				
		slew rate setting 0 (slowest)		86		ns
		slew rate setting 1		46		
		slew rate setting 2		39		
		slew rate setting 3 (fastest)		32		
$t_{r(on)(hs)}$	Turn-on rise time	From $V_{DS(hs)}$ < 320 V to $V_{DS(hs)}$ < 80 V, V_{BUS} = 400 V, L_{HB} current = 2 A, at below high-side slew rate settings, see GaN Power FET Switching Parameters				
		slew rate setting 0 (slowest)		13.1		ns
		slew rate setting 1		4.7		
		slew rate setting 2		3.2		
		slew rate setting 3 (fastest)		1.7		
$t_{d(off)(hs)}$	Turn-off delay time	From V_{INH} < $V_{INH,IT-}$ to $V_{DS(hs)}$ > 80 V, V_{BUS} = 400 V, L_{HB} current = 2 A, (independent of slew rate setting), see GaN Power FET Switching Parameters		37		ns
$t_{f(off)(hs)}$	Turn-off fall time	From $V_{DS(hs)}$ > 80 V to $V_{DS(hs)}$ > 320 V, V_{BUS} = 400 V, L_{HB} current = 2 A, (independent of slew rate setting), see GaN Power FET Switching Parameters		12.5		ns
	Turn-on slew rate	From $V_{DS(hs)}$ < 250 V to $V_{DS(hs)}$ < 150 V, T_J = 25 ℃, V_{BUS} = 400 V, L_{HB} current = 2 A, at below high-side slew rate settings, see GaN Power FET Switching Parameters				
		slew rate setting 0 (slowest)		20		V/ns
		slew rate setting 1		65		
		slew rate setting 2		90		
		slew rate setting 3 (fastest)		165		

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1) Symbol definitions: $V_{DS(ls)}$ = SW to SL voltage; $I_{DS(ls)}$ = SW to SL current; $V_{DS(hs)}$ = DH to SW voltage; $I_{D(hs)}$ = DH to SW current; 2) Unless otherwise noted: voltage, resistance, and capacitance are respect to AGND; -40 °C ≤ T_J ≤ 125 °C; 10 ≤ V_{AUX} ≤ 26; 7.5 ≤ V_{BST_SW} ≤ 26; V_{EN} = 5 V; V_{INL} = 0 V; V_{INH} = 0 V; R_{RDRVL} = 0 Ω; R_{RDRVH_SW} = 0 Ω; R_{CS} = 100 Ω

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
CS						
	Settling time	From I_{CS} > 0.1*$I_{CS(src)(final)}$ to I_{CS} < 0.9*$I_{CS(src)(final)}$, Low-side enabled into a 2 A load, 0 V ≤ V_{CS} ≤ 2 V,			35	ns
EN						
	EN wake-up time	V_{INL} = 5 V, From V_{EN} > V_{IT+} to $I_{D(ls)}$ > 10 mA		1		µs
BST						
	Start-up time from deep BST to SW discharge	From V_{BST_SW} ≥ $V_{BST_SW,T+(UVLO)}$ to high-side reacts to INH rising edge with V_{BST_SW} rising from 0 V to 10 V in 1 µs		5		µs
	Start-up time from shallow BST to SW discharge	From V_{BST_SW} ≥ $V_{BST_SW,T+(UVLO)}$ to high-side reacts to INH rising edge with V_{BST_SW} rising from 5 V to 10 V in 0.5 µs		2		µs

6.7 Typical Characteristics

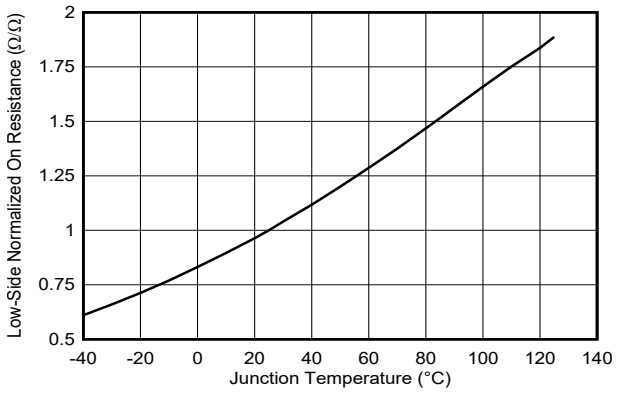


図 6-1. Low-Side Normalized On-Resistance vs Junction Temperature

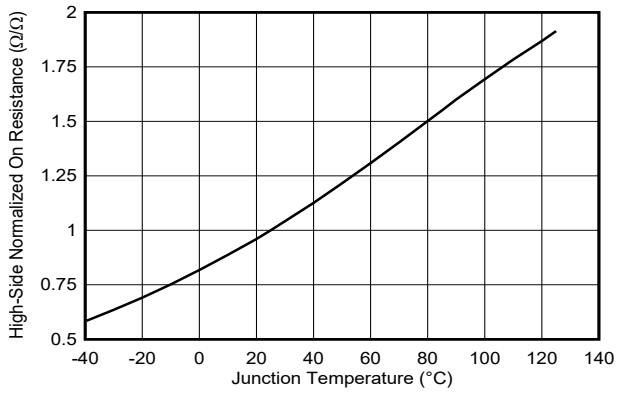


図 6-2. High-Side Normalized On-Resistance vs Junction Temperature

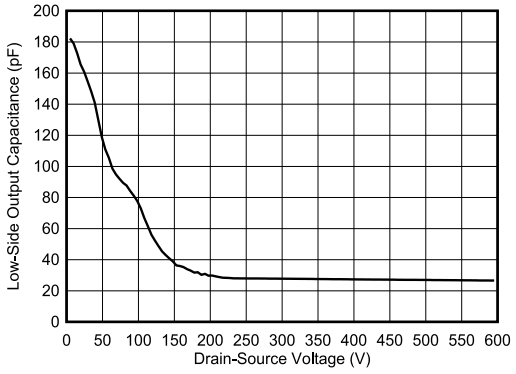


図 6-3. Low-Side Output Capacitance vs Drain-Source Voltage

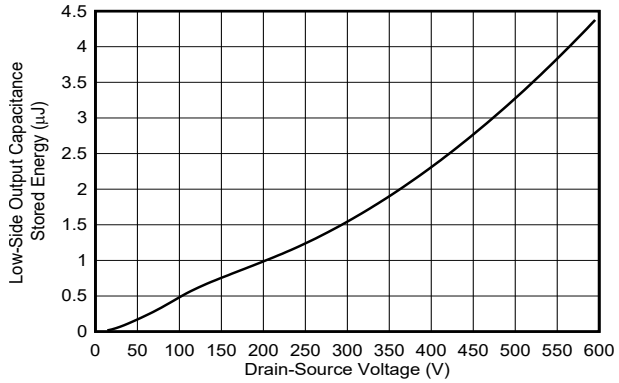


図 6-4. Low-Side Output Capacitance Stored Energy vs Drain-Source Voltage

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6.7 Typical Characteristics (continued)

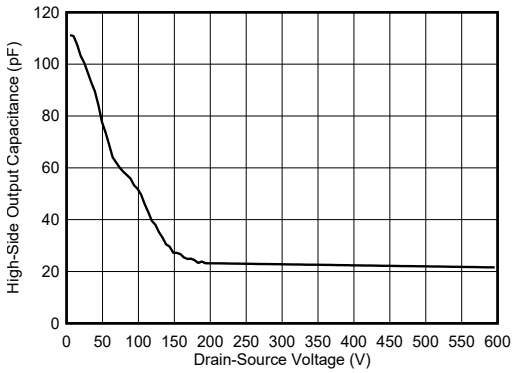


図 6-5. High-Side Output Capacitance vs Drain-Source Voltage

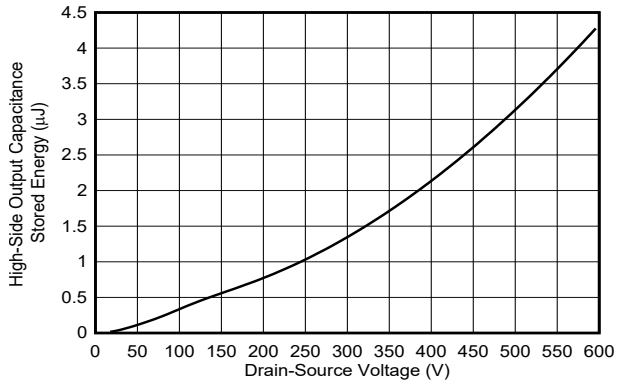


図 6-6. High-Side Output Capacitance Stored Energy vs Drain-Source Voltage

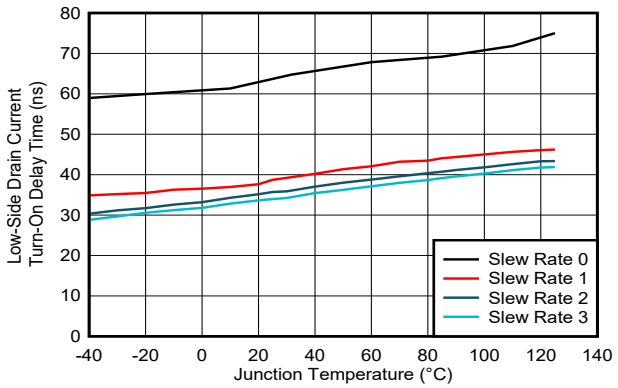


図 6-7. Low-Side Drain Current Turn-On Delay Time vs Junction Temperature

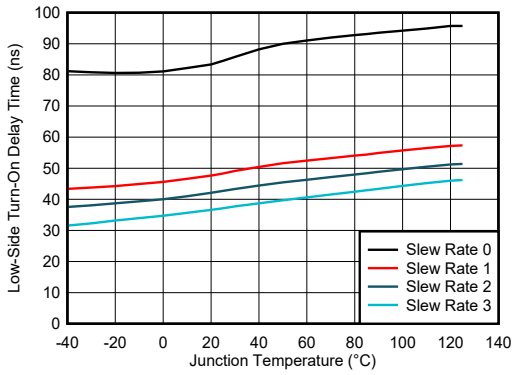


図 6-8. Low-Side Turn-On Delay Time vs Junction Temperature

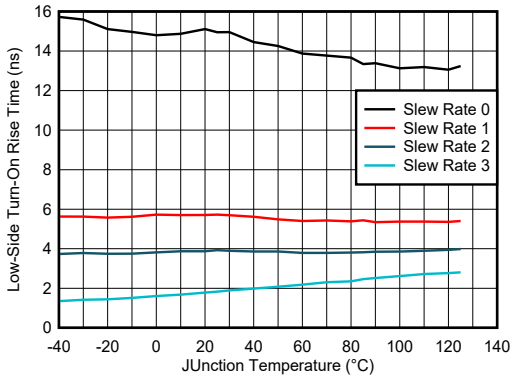


図 6-9. Low-Side Turn-On Rise Time vs Junction Temperature

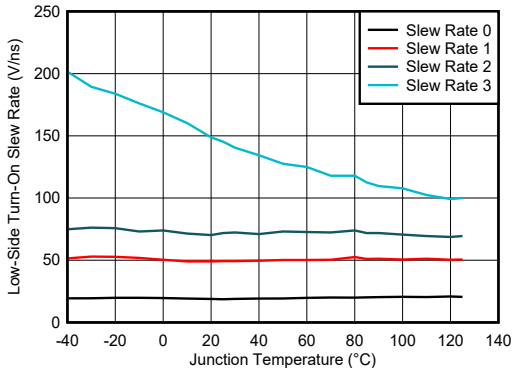


図 6-10. Low-Side Turn-On Slew Rate vs Junction Temperature

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6.7 Typical Characteristics (continued)

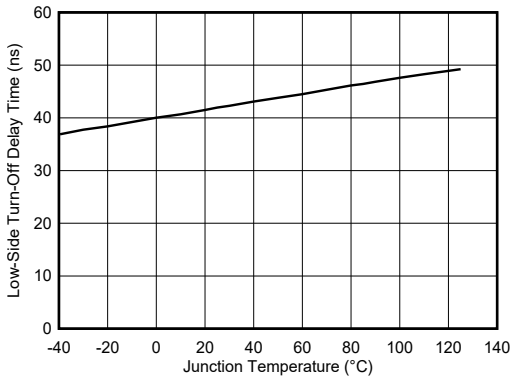


図 6-11. Low-Side Turn-Off Delay Time vs Junction Temperature

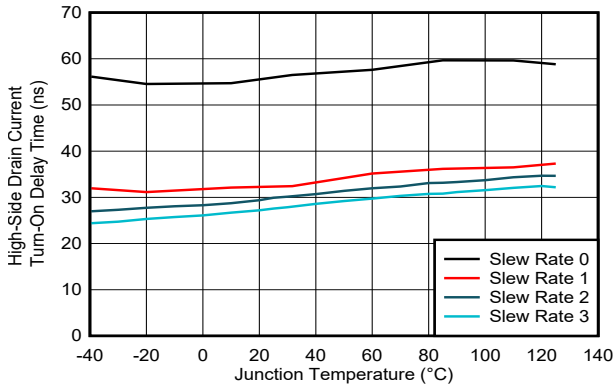


図 6-12. High-Side Drain Current Turn-On Delay Time vs Junction Temperature

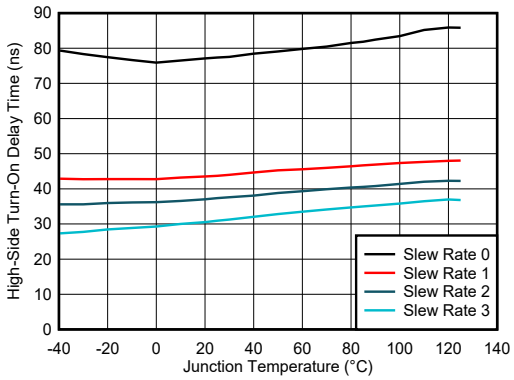


図 6-13. High-Side Turn-On Delay Time vs Junction Temperature

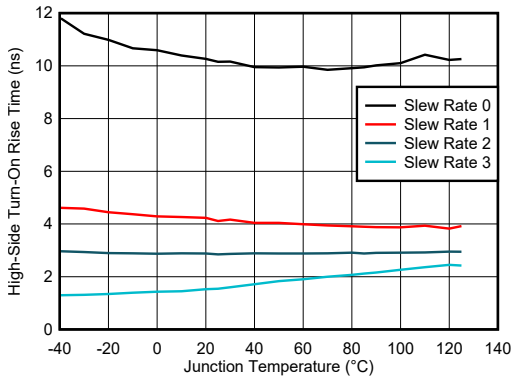


図 6-14. High-Side Turn-On Rise Time vs Junction Temperature

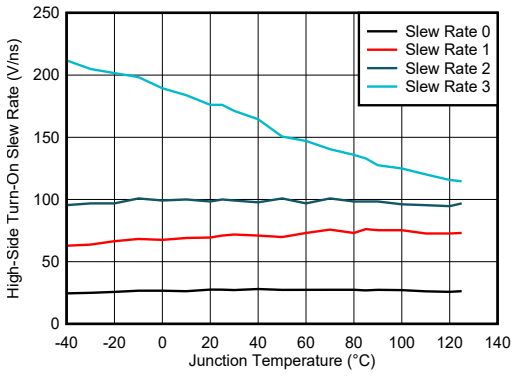


図 6-15. High-Side Turn-On Slew Rate vs Junction Temperature

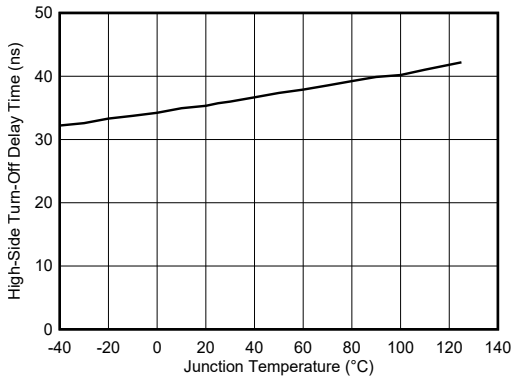


図 6-16. High-Side Turn-Off Delay Time vs Junction Temperature

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6.7 Typical Characteristics (continued)

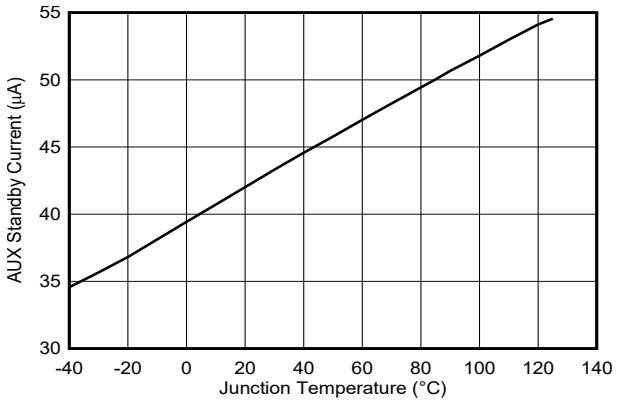
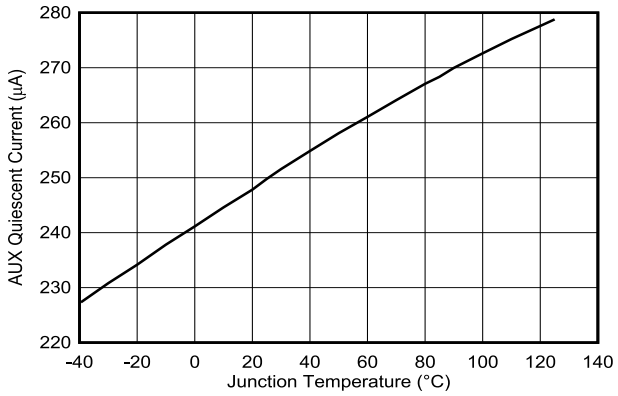
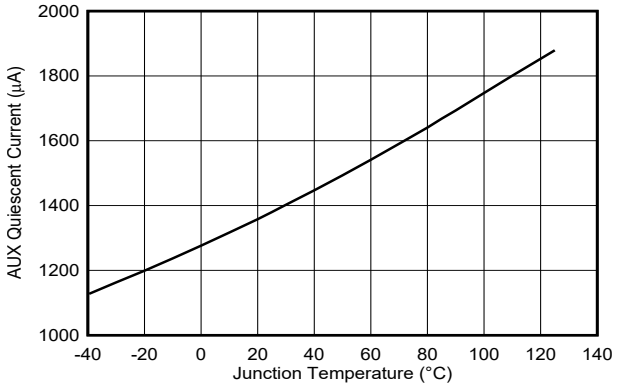


図 6-17. AUX Standby Current vs Junction Temperature



INL = 0 V

図 6-18. AUX Quiescent Current vs Junction Temperature



INL = 5 V

図 6-19. AUX Quiescent Current vs Junction Temperature

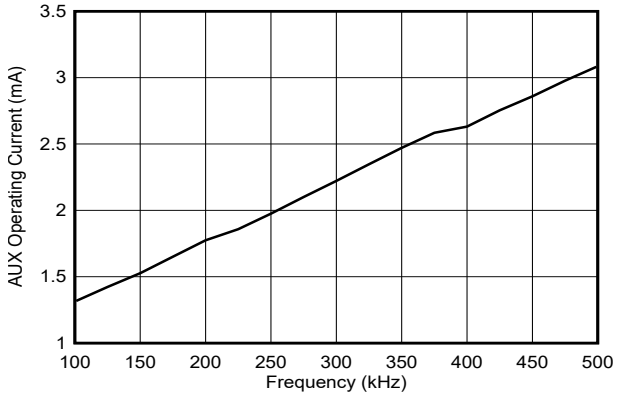
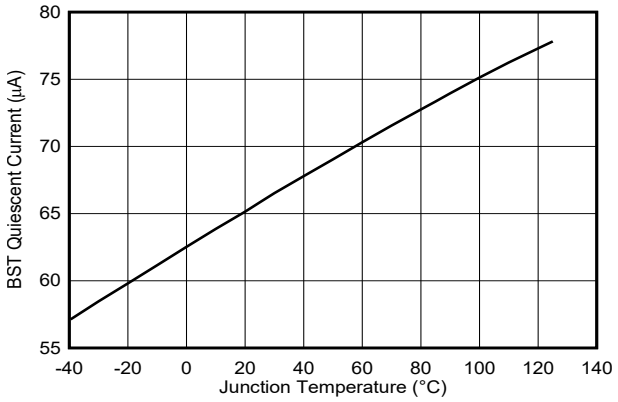
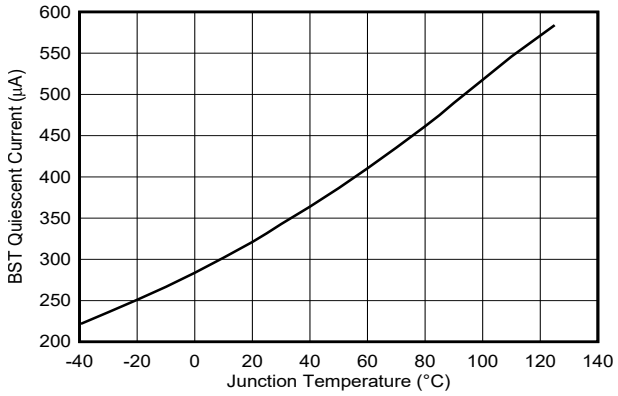


図 6-20. AUX Operating Current vs Frequency



INH = 0 V

図 6-21. BST Quiescent Current vs Junction Temperature



INH = 5 V

図 6-22. BST Quiescent Current vs Junction Temperature

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6.7 Typical Characteristics (continued)

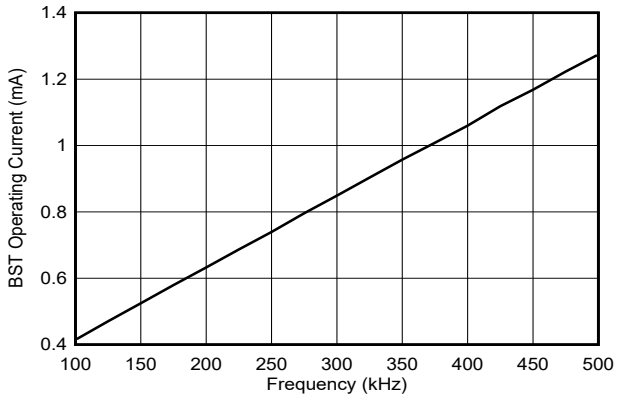


図 6-23. BST Operating Current vs Junction Temperature

7 Parameter Measurement Information

7.1 GaN Power FET Switching Parameters

図 7-1 shows the circuit used to measure the GaN power FET switching parameters. The circuit is operated as a double-pulse tester. Consult external references for double-pulse tester details. The circuit is placed in the boost configuration to measure the low-side GaN switching parameters. The circuit is placed in the buck configuration to measure the high-side GaN switching parameters. The GaN FET not being measured in each configuration (high-side in the boost and low-side in the buck) acts as the double-pulse tester diode and circulates the inductor current in the off-state, third-quadrant conduction mode. 表 7-1 shows the details for each configuration.

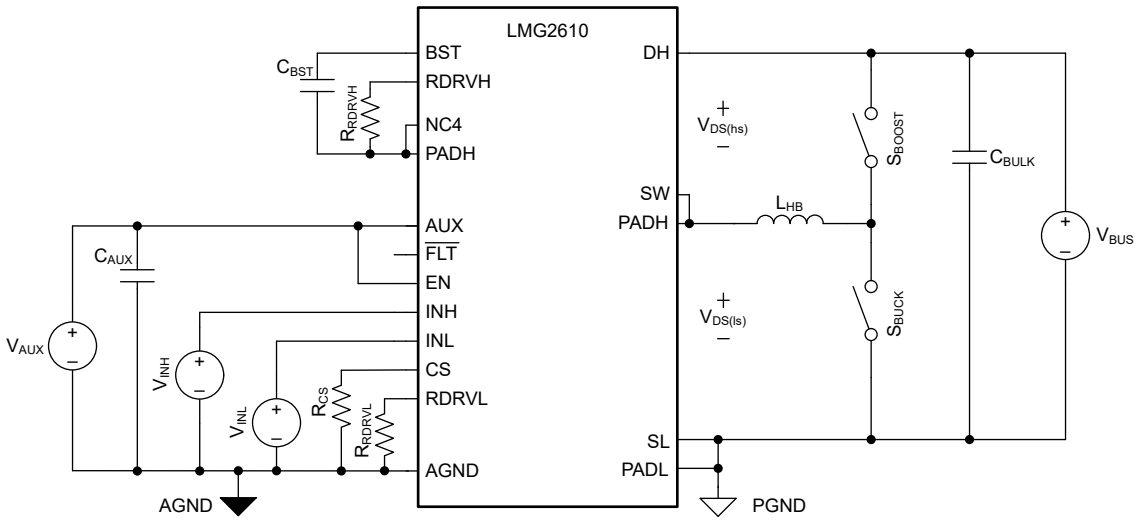


図 7-1. GaN Power FET Switching Parameters Test Circuit

表 7-1. GaN Power FET Switching Parameters Test Circuit Configuration Details

Configuration	GaN FET Under Test	GaN FET Acting as Diode	S_{BOOST}	S_{BUCK}	V_{INL}	V_{INH}
Boost	Low-side	High-side	Closed	Open	Double-pulse waveform	0 V
Buck	High-side	Low-side	Open	Closed	0 V	Double-pulse waveform

図 7-2 shows the GaN power FET switching parameters.

The GaN power FET turn-on transition has three timing components: drain-current turn-on delay time, turn-on delay time, and turn-on rise time. Note that the turn-on rise time is the same as the V_{DS} 80% to 20% fall time. All three turn-on timing components are a function of the RDRVx pin setting.

The GaN power FET turn-off transition has two timing components: turn-off delay time, and turn-off fall time. Note that the turn-off fall time is the same as the V_{DS} 20% to 80% rise time. The turn-off timing components are independent of the RDRVx pin setting, but heavily dependent on the L_{HB} current.

The turn-on slew rate is measured over a smaller voltage delta (100 V) compared to the turn-on rise time voltage delta (240 V) to obtain a faster slew rate which is useful for EMI design. The RDRVx pin is used to program the slew rate.

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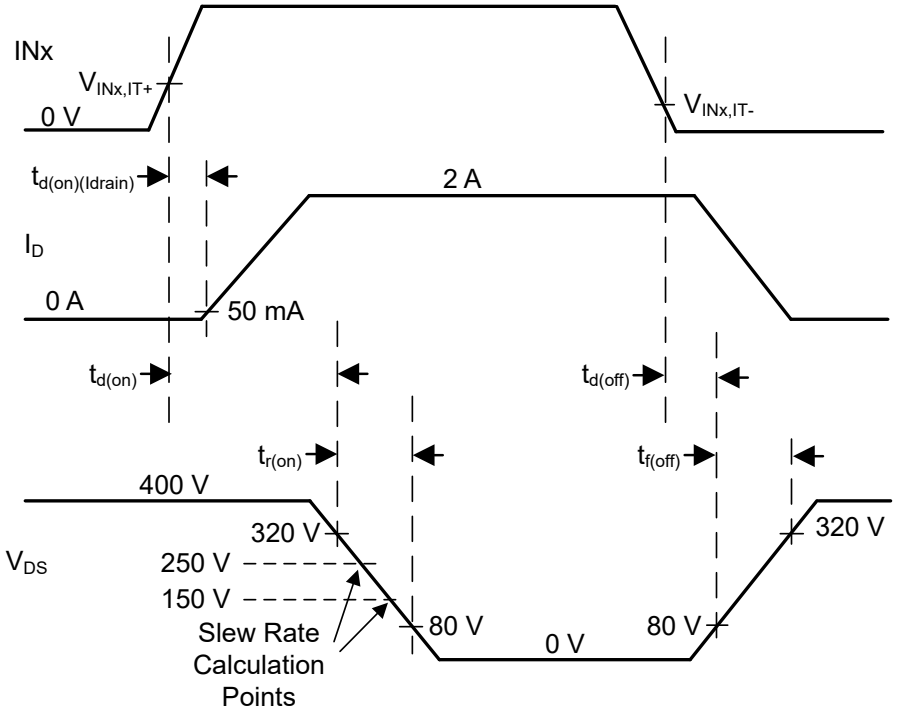


図 7-2. GaN Power FET Switching Parameters

8 Detailed Description

8.1 Overview

The LMG2610 is a highly-integrated 650-V GaN power-FET half bridge intended for use in active-clamp flyback (ACF) converters. The LMG2610 combines the half-bridge power FETs, gate drivers, low-side current-sense emulation function, high-side gate-drive level shifter, and bootstrap diode function in a 9-mm by 7-mm QFN package.

The 650-V rated GaN power FETs support the large transformer turns ratios needed to minimize the secondary-side synchronous-rectifier voltage requirements in flyback converter applications. The GaN half-bridge low output-capacitive charge reduces both the time and energy needed for ACF zero-voltage switching (ZVS) and is the key characteristic needed to create small, efficient power converters.

The GaN half-bridge consists of a 170-mΩ low-side FET and a 248-mΩ high-side FET. The asymmetric GaN half-bridge FET sizes are a good utilization of total GaN FET size for ACF operating conditions.

The LMG2610 internal gate drivers regulate the drive voltage for optimum GaN power-FET on-resistance. Internal drivers also reduce total gate inductance and GaN FET common-source inductance for improved switching performance, including common-mode transient immunity (CMTI). The low-side / high-side GaN FET turn-on slew rates can be individually programmed to one of four discrete settings for design flexibility with respect to power loss, switching-induced ringing, and EMI.

Current-sense emulation places a scaled replica of the low-side drain current on the output of the CS pin. The CS pin is terminated with a resistor to AGND to create the current-sense input signal to the external power supply controller. This CS pin resistor replaces the traditional current-sense resistor, placed in series with the low-side GaN FET source, at significant power and space savings. Furthermore, with no current-sense resistor in series with the GaN source, the low-side GaN FET thermal pad can be connected directly to the PCB power ground. This thermal pad connection both improves system thermal performance and provides additional device routing flexibility since full device current can be conducted through the thermal pads.

The high-side gate-drive level-shifter reduces the capacitive coupling of the sensitive high-side gate drive path for lower noise susceptibility and better CMTI compared to external solutions where the signal path has a much larger PCB footprint. The level shifter also has minimal impact on device quiescent current and no impact on device start-up time compared to external solutions with worse quiescent current and start up performance.

The bootstrap diode function between AUX and BST is implemented with a smart-switched GaN bootstrap FET. The switched GaN bootstrap FET allows more complete charging of the BST-to-SW capacitor since the on-state GaN bootstrap FET does not have the forward voltage drop of a traditional bootstrap diode. The smart-switched GaN bootstrap FET also avoids the traditional bootstrap diode problem of BST-to-SW capacitor overcharging due to off-state third-quadrant current flow in the low-side half-bridge GaN power FET. Finally, the bootstrap function has more efficient switching due to low capacitance and no reverse-recovery charge compared to the traditional bootstrap diode.

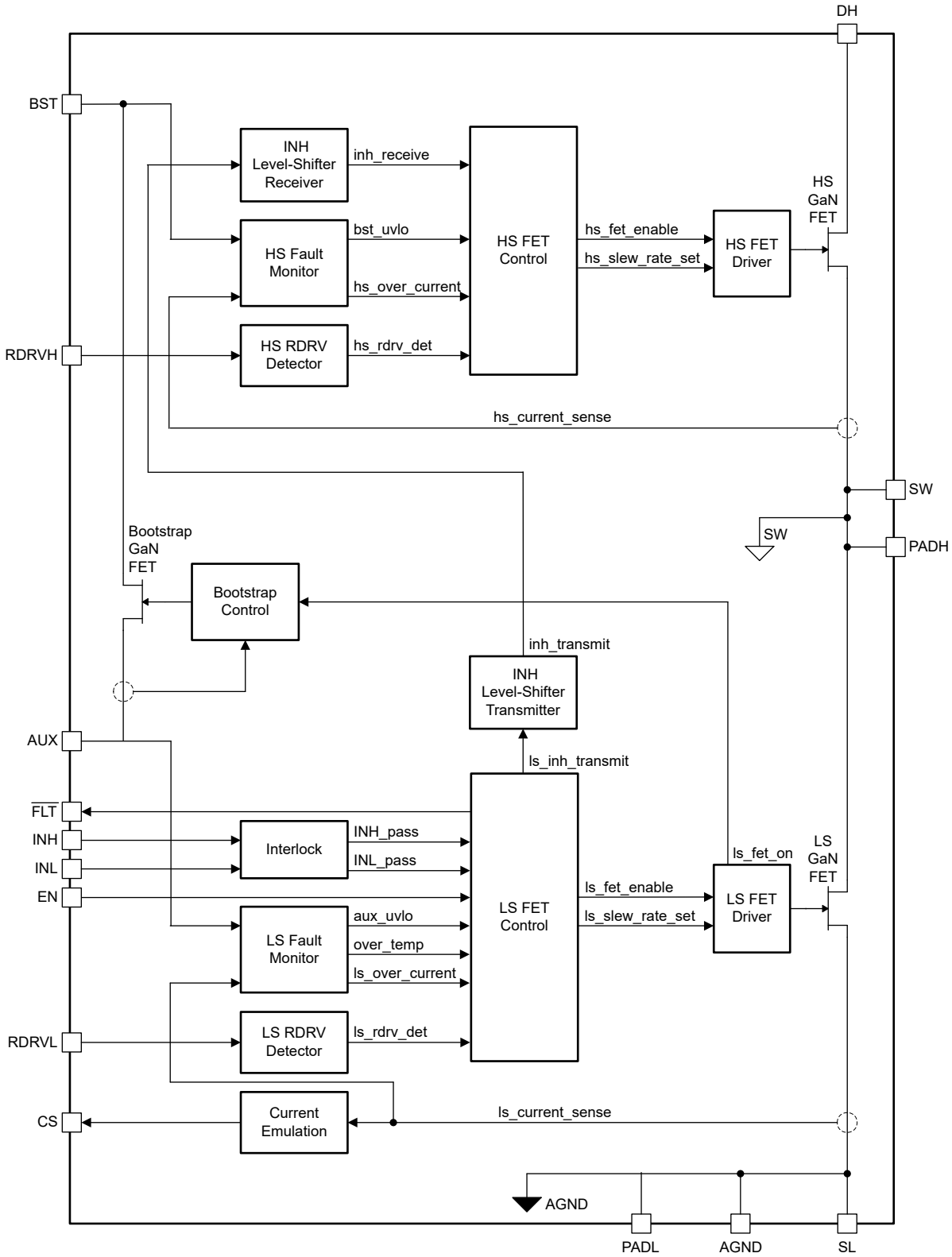
The AUX input supply wide voltage range is compatible with the corresponding wide range supply rail created by power supply controllers. The BST input supply range is even wider on the low end to account for capacitive droop in between bootstrap recharge cycles. Low AUX / BST idle quiescent currents and fast BST start-up time support converter burst-mode operation critical for meeting government light-load efficiency mandates. Further AUX quiescent current reduction is obtained by placing the device in standby mode with the EN pin.

The INL, INH, and EN control pins have high input impedance, low input threshold voltage and maximum input voltage equal to the AUX voltage. This allows the pins to support both low voltage and high voltage input signals and be driven with low-power outputs.

The LMG2610 protection features are low-side / high-side under-voltage lockout (UVLO), low-side / high-side input gate-drive interlock, low-side / high-side cycle-by-cycle current limit, and over-temperature shut down. The UVLO features also help achieve well-behaved converter operation. The over-temperature shut down is reported on the open drain $\overline{\text{FLT}}$ output.

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8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 GaN Power FET Switching Capability

Due to the silicon FET's long reign as the dominant power-switch technology, many designers are unaware that the nameplate drain-source voltage cannot be used as an equivalent point to compare devices across technologies. The nameplate drain-source voltage of a silicon FET is set by the avalanche breakdown voltage. The nameplate drain-source voltage of a GaN FET is set by the long term compliance to data sheet specifications.

Exceeding the nameplate drain-source voltage of a silicon FET can lead to immediate and permanent damage. Meanwhile, the breakdown voltage of a GaN FET is much higher than the nameplate drain-source voltage. For example, the breakdown drain-source voltage of the LMG2610 GaN power FET is more than 800 V which allows the LMG2610 to operate at conditions beyond an identically nameplate rated silicon FET.

The LMG2610 GaN power FET switching capability is explained with the assistance of 図 8-1. The figure shows the drain-source voltage versus time for the LMG2610 GaN power FET for four distinct switch cycles in a switching application. No claim is made about the switching frequency or duty cycle. The first two cycles show normal operation and the second two cycles show operation during a rare input voltage surge. The LMG2610 GaN power FETs are intended to be turned on in either zero-voltage switching (ZVS) or discontinuous-conduction mode (DCM) switching conditions.

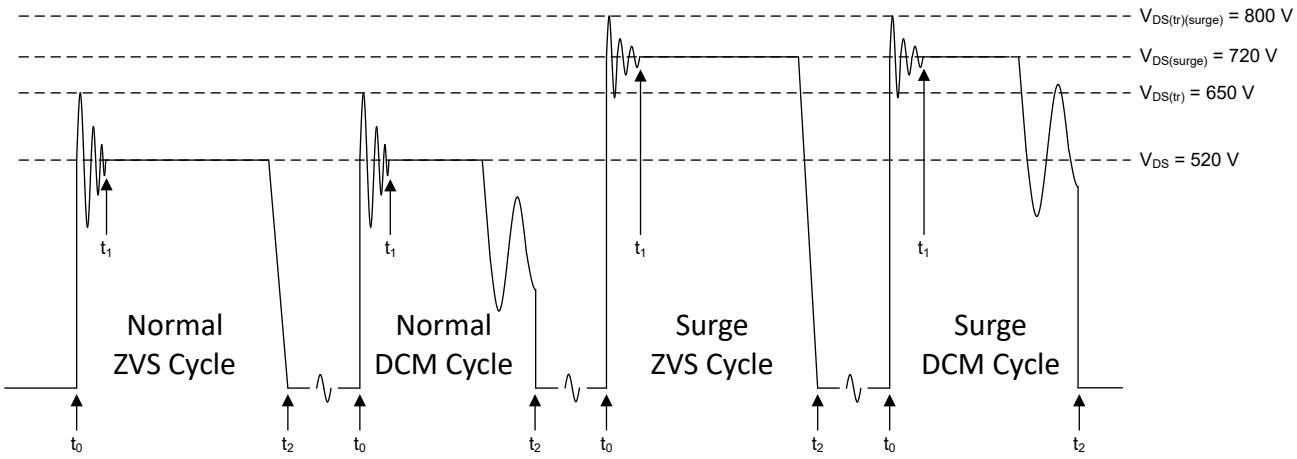


図 8-1. GaN Power FET Switching Capability

Each cycle starts before t_0 with the FET in the on state. At t_0 the GaN FET turns off and parasitic elements cause the drain-source voltage to ring at a high frequency. The high frequency ringing has damped out by t_1. Between t_1 and t_2 the FET drain-source voltage is set by the characteristic response of the switching application. The characteristic is shown as a flat line (plateau), but other responses are possible. At t_2 the GaN FET is turned on. For normal operation, the transient ring voltage is limited to 650 V and the plateau voltage is limited to 520 V. For rare surge events, the transient ring voltage is limited to 800 V and the plateau voltage is limited to 720 V.

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8.3.2 Turn-On Slew-Rate Control

The turn-on slew rate of both the low-side and high-side GaN power FETs are individually programmed to one of four discrete settings. The low-side slew rate is programmed by the resistance between the RDRVL and AGND pins. The high-side slew rate is programmed by the resistance between the RDRVH and SW pins. The low-side slew-rate setting is determined one time during AUX power up when the AUX voltage goes above the *AUX Power-On Reset* voltage. The high-side slew-rate setting is determined one time during BST-to-SW power up when the BST-to-SW voltage goes above the *BST Power-On Reset* voltage. The slew-rate setting determination time is not specified but is around 0.4 us.

表 8-1 shows the recommended typical resistance programming value for the four slew rate settings and the typical turn-on slew rate at each setting. As noted in the table, an open-circuit connection is acceptable for programming slew-rate setting 0 and a short-circuit connection (RDRVL shorted to AGND for the low-side turn-on slew rate) (RDRVH shorted to SW for the high-side turn-on slew rate) is acceptable for programming slew-rate setting 3.

表 8-1. Slew-Rate Setting

Turn-On Slew Rate Setting	Recommended Typical Programming Resistance (kΩ)	Typical LS / HS Turn-On Slew Rate (V/ns)	Comment
0	120	20 / 20	Open-circuit connection for programming resistance is acceptable.
1	47	50 / 65	
2	22	70 / 90	
3	5.6	140 / 165	Short-circuit connection for programming resistance (RDRVL shorted to AGND for low-side slew rate) (RDRVH shorted to SW for high-side slew rate) is acceptable.

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8.3.3 Current-Sense Emulation

The current-sense emulation function creates a scaled replica of the low-side GaN power FET positive drain current at the output of the CS pin. The current-sense emulation gain, G_{CSE}, is 1 mA output from the CS pin, I_{CS} for every 1 A passing into the drain of the low-side GaN power FET, I_D.

$$G_{CSE} = I_{CS} / I_D = 1\ mA / 1\ A = 0.001 \quad (1)$$

The CS pin is terminated with a resistor to AGND, R_{CS}, to create the current-sense voltage input signal to the external power supply controller.

R_{CS} is determined by solving for the traditional current-sense design resistance, $R_{CS(trad)}$, and multiplying by the inverse of G_{CSE}. The traditional current-sense design creates the current-sense voltage, $V_{CS(trad)}$, by passing the low-side GaN power FET drain current, I_D, through $R_{CS(trad)}$. The LMG2610 creates the current-sense voltage, V_{CS}, by passing the CS pin output current, I_{CS}, through R_{CS}. The current-sense voltage must be the same for both designs.

$$V_{CS} = I_{CS} * R_{CS} = V_{CS(trad)} = I_D * R_{CS(trad)} \quad (2)$$

$$R_{CS} = I_D / I_{CS} * R_{CS(trad)} = 1 / G_{CSE} * R_{CS(trad)} \quad (3)$$

$$R_{CS} = 1000 * R_{CS(trad)} \quad (4)$$

The CS pin is clamped internally to a typical 2.5 V. The clamp protects vulnerable power-supply controller current-sense input pins from over voltage if, for example, the current sense resistor on the CS pin were to become disconnected.

図 8-2 shows the current-sense emulation operation. In both cycles, the CS pin current emulates the low-side GaN power-FET drain current while the low-side FET is enabled. The first cycle shows normal operation where the controller turns off the low-side GaN power FET when the controller current-sense input threshold is tripped. The second cycle shows a fault situation where the LMG2610 *Over-Current Protection* turns off the low-side GaN power FET before the controller current-sense input threshold is tripped. In this second cycle, the LMG2610 avoids a hung controller INL pulse by generating a fast-ramping artificial current-sense emulation signal to trip the controller current-sense input threshold. The artificial signal persists until the INL pin goes to logic-low which indicates the controller is back in control of switch operation.

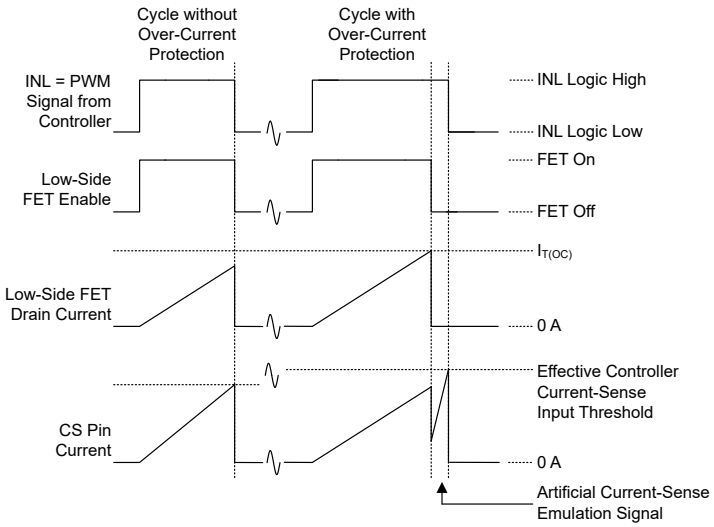


図 8-2. Current-Sense Emulation Operation

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8.3.4 Bootstrap Diode Function

The internal bootstrap diode function is implemented with a smart-switched GaN bootstrap FET. The GaN bootstrap FET blocks current in both directions between AUX and BST when The GaN bootstrap FET is turned off.

The bootstrap diode function is active when the low-side GaN power FET is turned on and inactive when the low-side GaN power FET is turned off. The GaN bootstrap FET is held off in the bootstrap diode inactive phase. The GaN bootstrap FET is turned on a single time at the beginning of the bootstrap active phase and is controlled as an ideal diode with diode current flowing from AUX to BST to charge the BST-to-SW capacitor. If a small reverse current from BST to AUX is detected after the GaN bootstrap FET is turned on, the GaN bootstrap FET is turned off for the remainder of the bootstrap active phase.

The bootstrap diode function implements a current limit to protect the GaN bootstrap FET when the BST-to-SW capacitor is significantly discharged at the beginning of the bootstrap active phase. If there is no current limit situation during the GaN bootstrap FET turn on, or if the bootstrap function drops out of current limit as the BST-to-SW capacitor charges, the current limit function is disabled for the remainder of the GaN bootstrap FET turn-on time. The current limit function is disabled to save quiescent current.

8.3.5 Input Control Pins (EN, INL, INH)

The EN pin is used to toggle the device between the active and standby modes described in *Device Functional Modes*.

The INL pin is used to turn the low-side GaN power FET on and off.

The INH pin is used to turn the high-side GaN power FET on and off.

The input control pins have a typical 1-V input-voltage-threshold hysteresis for noise immunity. The pins also have a typical 400 kΩ pull-down resistance to protect against floating inputs. The 400 kΩ saturates for typical input voltages above 4 V to limit the maximum input pull-down current to a typical 10 uA.

The INL turn-on action is impacted by the following conditions 1) *Standby Mode*, 2) *AUX UVLO*, 3) INH in control of *Interlock*, 4) Low-Side *Over-Current Protection*, and 5) *Over-Temperature Protection*.

The INH turn-on action is impacted by the following conditions 1) *Standby Mode*, 2) *AUX UVLO*, 3) INL in control of *Interlock*, 4) High-Side *Over-Current Protection*, and 5) *Over-Temperature Protection*.

The *Standby Mode*, *AUX UVLO*, and *Over-Temperature Protection* are the universal INL / INH blocking conditions. These conditions hold both GaN half-bridge power FETs off independent of INL and INH. 図 8-3 shows the Universal Blocking Condition Operation. Note that the high-side FET does not turn on at transistion #4. INH only turns on the high-side FET if there is no universal blocking condition when INH goes to logic high. This avoids an incomplete high-side FET turn-on period which can create undesired spike voltages in the converter.

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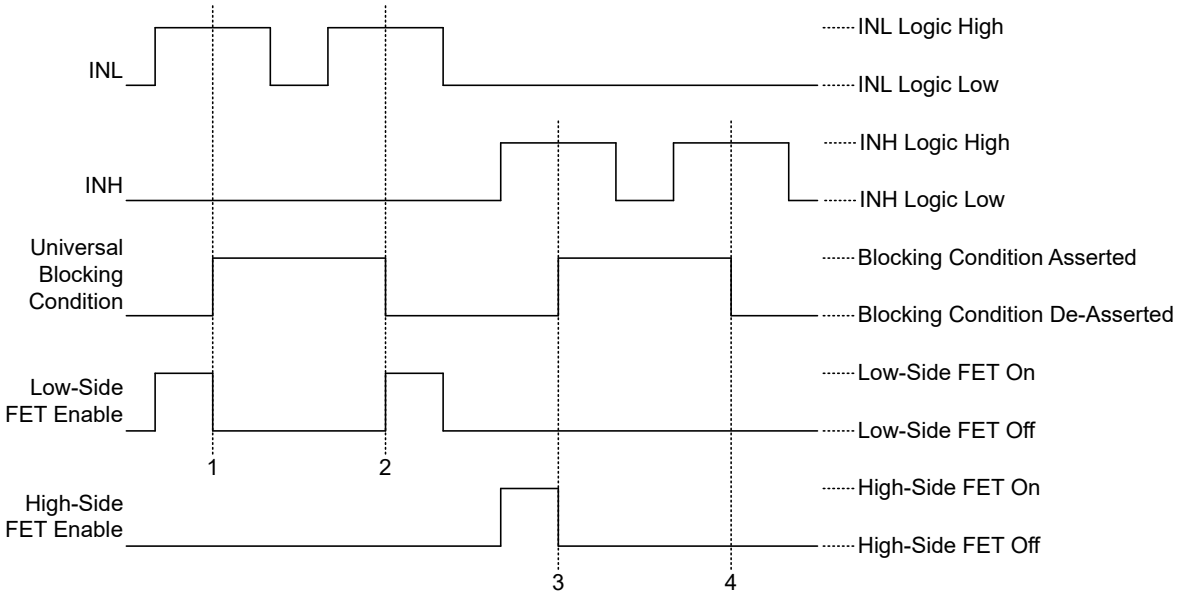


図 8-3. Universal INL / INH Blocking Condition Operation

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8.3.6 INL - INH Interlock

The interlock function keeps the low-side and high-side GaN power FETs from being simultaneously turned on when the INL and INH pins are both logic-high. Either the INL or the INH pin gains control of the interlock if it is logic high when the other pin is logic low. Once the INL or INH pin gains control of the interlock, it retains control as long as it remains logic high. Only the INL or INH pin in control of the interlock passes a logic-high signal through the interlock.

The interlock is disabled if any of the universal INL / INH blocking conditions defined in *Input Control Pins* are asserted. When the interlock is disabled, the interlock outputs are held at logic low. If both INL and INH are logic-high when the interlock is enabled, the INL takes priority, gains control of the interlock, and passes the INL logic-high signal through the interlock.

8.3.7 AUX Supply Pin

The AUX pin is the input supply for the low-side internal circuits and is the power source to charge the BST-to-SW capacitor through the internal bootstrap diode function.

8.3.7.1 AUX Power-On Reset

The AUX Power-On Reset disables all low-side functionality if the AUX voltage is below the AUX Power-On Reset voltage. The AUX Power-On Reset voltage is not specified but is around 5 V. The AUX Power-On Reset initates the one-time determination of the low-side slew-rate setting programmed on the RDRVL pin if the AUX voltage goes above the AUX Power-On Reset voltage. The AUX Power-On Reset enables the over-temperature protection function if the AUX voltage is above the AUX Power-On Reset voltage.

8.3.7.2 AUX Under-Voltage Lockout (UVLO)

The AUX UVLO holds off both the low-side and high-side GaN power FETs if the AUX voltage is below the AUX UVLO voltage. The AUX UVLO voltage is set higher than the BST UVLO voltage so the high-side GaN power FET can be operated when the low-side GaN power FET is operating. The voltage separation between the AUX UVLO voltage and BST UVLO voltage accounts for operating conditions where the bootstrap charging of the BST-to-SW capacitor from the AUX supply is incomplete. The AUX UVLO voltage hysteresis prevents on-off chatter near the UVLO voltage trip point.

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8.3.8 BST Supply Pin

The BST pin is the input supply for the high-side internal circuits. The BST pin and corresponding high-side circuits are referenced to the SW pin. The BST pin is powered by the low-side AUX Supply pin through the internal bootstrap diode function. The bootstrap function is inactive when the low-side GaN FET is off and the BST pin must rely on an external BST-to-SW capacitor for the BST power source.

Designing the BST-to-SW capacitance is a trade-off between high-side charge-up time and hold-up time. The BST-to-SW external capacitance is recommended to be a ceramic capacitor that is at least 10 nF over operating conditions.

8.3.8.1 BST Power-On Reset

The BST Power-On Reset voltage is with respect to the SW pin. The BST Power-On Reset disables all high-side functionality if the BST-to-SW voltage is below the BST Power-On Reset voltage. The BST Power-On Reset voltage is not specified but is around 5 V. The BST Power-On Reset initiates the one-time determination of the high-side slew-rate setting programmed on the RDRVH pin if the BST-to-SW voltage goes above the BST Power-On Reset voltage.

8.3.8.2 BST Under-Voltage Lockout (UVLO)

The BST UVLO voltage is with respect to the SW pin. The BST UVLO only controls the high-side GaN power FET. The BST UVLO does not control the low-side GaN power FET. The BST UVLO consists of two separate UVLO functions to create a two-level BST UVLO. The upper BST UVLO is called the BST Turn-On UVLO and only controls if the high-side GaN power FET is turned on. The lower BST UVLO is called the BST Turn-Off UVLO and only controls if the high-side GaN power FET is turned off after the high-side GaN power FET is turned on. The operation of the two-level UVLO is not the same as a single UVLO with wide hysteresis.

図 8-4 shows the BST UVLO operation. The BST Turn-On UVLO prevents the high-side GaN power FET from turning on at a INH logic-high rising edge if the BST-to-SW voltage is below the BST Turn-On UVLO voltage - INH pulses #1, #2, and #5. After the high-side GaN power FET is successfully turned-on, the BST Turn-On UVLO is ignored and the BST Turn-Off UVLO output is watched for the remainder of the INH logic-high pulse - INH pulses #3, #4, and #6. The BST Turn-Off UVLO turns off the high-side GaN power FET for the remainder of the INH logic-high pulse if the BST-to-SW voltage falls below the BST Turn-Off UVLO voltage - INH pulse #6.

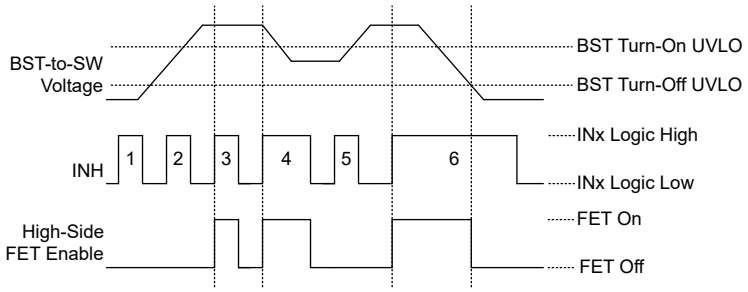


図 8-4. BST UVLO Operation

The effective voltage hysteresis of the two-level BST UVLO is the difference between the upper and lower BST UVLO voltages. A single-level BST UVLO can be implemented with the same hysteresis but allows subsequent high-side GaN power FET turn on anywhere in the hysteresis range. The two-level UVLO design prevents any turn on in the hysteresis range. A single-level BST UVLO would allow INH pulse #5 to turn on the high-side GaN power FET.

The two-level BST UVLO allows a wide hysteresis while making sure the BST-to-SW capacitor is adequately charged at the beginning of every INH pulse. The wide hysteresis allows a smaller BST-to-SW capacitor to be used which is useful for faster high-side start-up time. The adequate capacitor charge at the beginning of the INH pulse helps make sure the high-side GaN power FET is not turned-off early in the INH pulse which can create undesired spike voltages in the converter.

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8.3.9 Over-Current Protection

The LMG2610 implements cycle-by-cycle over-current protection for both half-bridge GaN power FETs. 図 8-5 shows the cycle-by-cycle over-current operation. Every INx logic-high cycle turns on the GaN power FET. If the GaN power FET drain current exceeds the over-current threshold current, the over-current protection turns off the GaN power FET for the remainder of the INx logic-high duration.

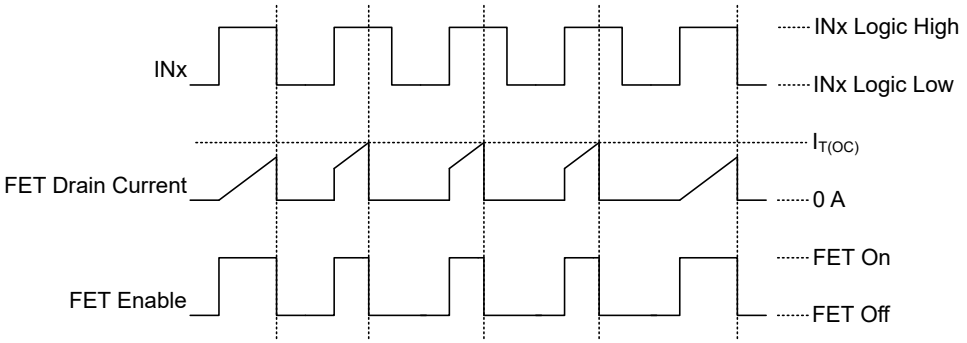


図 8-5. Cycle-by-Cycle Over-Current Protection Operation

An over-current protection event is not reported on the $\overline{FLT}$ pin. Cycle-by-cycle over-current protection minimizes system disruption because the event is not reported and because the protection allows the GaN power FET to turn on every INx cycle.

The low-side / high-side over-current protection threshold currents are set to different levels corresponding to the different GaN power FET sizes. As described in *Current-Sense Emulation*, an artificial CS pin current is produced after the low-side GaN power FET is turned off by the low-side over-current protection, to prevent the controller from entering a hung state.

8.3.10 Over-Temperature Protection

The over-temperature protection holds off both the low-side and high-side GaN power FETs if the LMG2610 temperature is above the over-temperature shut-down temperature. The over-temperature shut-down hysteresis avoids erratic thermal cycling. An over-temperature fault is reported on the $\overline{FLT}$ pin when the over-temperature protection is asserted. This is the only fault event reported on the $\overline{FLT}$ pin. The over-temperature protection is enabled when the AUX voltage is above the *AUX Power-On Reset* voltage. The low AUX Power-On Reset voltage helps the over-temperature protection remain operational when the AUX rail droops during the cool-down phase.

8.3.11 Fault Reporting

The LMG2610 only reports an over-temperature fault. An over-temperature fault is reported on the $\overline{FLT}$ pin when the *Over-Temperature Protection* function is asserted. The $\overline{FLT}$ pin is an active low open-drain output so the pin pulls low when there is an over-temperature fault.

8.4 Device Functional Modes

The LMG2610 has two modes of operation controlled by the EN pin. The device is in Active mode when the EN is logic high and in Standby mode when the EN pin is logic low. In active mode, the half-bridge GaN power FETs are controlled by the INL and INH pins. In Standby mode, the INL and INH pins are ignored, the half-bridge GaN power FETs are held off, and the AUX quiescent current is reduced to the AUX standby quiescent current.

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9 Application and Implementation

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Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

The LMG2610 is a GaN power-FET half bridge intended for use in off-line active-clamp flyback (ACF) converters. The LMG2610 provides plug-and-play simplicity since it integrates the half-bridge FETs, FET gate drivers, high-side gate-drive level shifter, bootstrap diode function, and current-sense emulation in a single package. The typical application example shows the LMG2610 pairing seamlessly with the Texas Instruments UCC28782 ACF controller to create a high-power-density, high-efficiency, 65-W, USB-PD charger.

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9.2 Typical Application

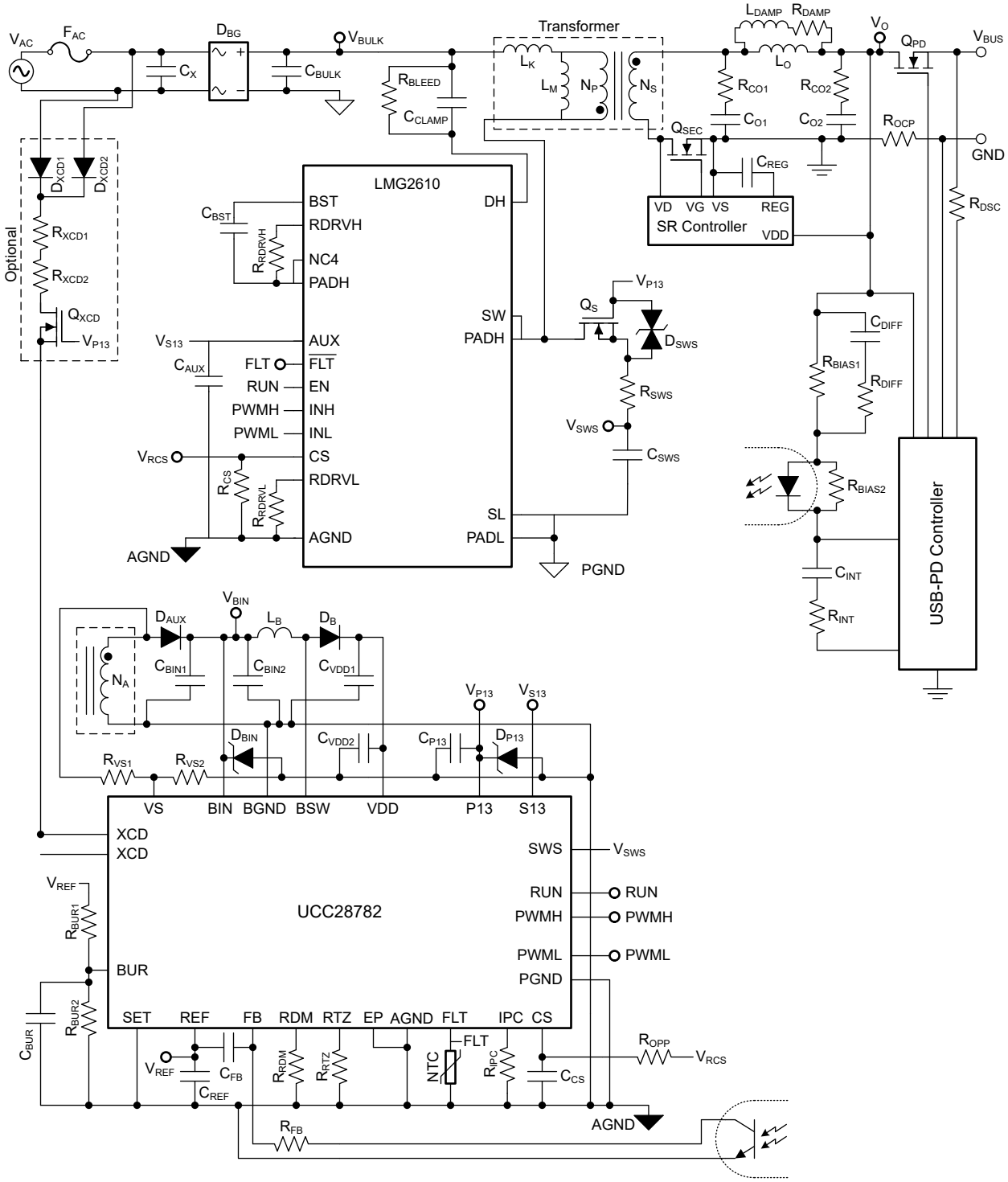


図 9-1. 65-W USB-PD Charger Application

9.2.1 Design Requirements

表 9-1. Electrical Performance Specifications

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT CHARACTERISTICS						
V_{IN}	Input line voltage (RMS)		90	115 / 230	264	V
f_{LINE}	Input line frequency		47	50 / 60	63	Hz
P_{STBY}	Input power at no-load, V_O = 5 V	V_{IN} = 230 V_{RMS}, I_O = 0 A		55	70	mW
		V_{IN} = 115 V_{RMS}, I_O = 0 A		45	70	mW
$P_{0.25W}$	Input power at 0.25-W load, V_O = 20 V	V_{IN} = 230 V_{RMS}, P_O = 250 mW		399	470	mW
		V_{IN} = 115 V_{RMS}, P_O = 250 mW		359	470	mW
OUTPUT CHARACTERISTICS						
V_O	Output voltage, 20-V setting	V_{IN} = 90 to 264 V_{RMS}, I_O = 0 A to 3.25 A		19.95		V
	Output voltage, 15-V setting	V_{IN} = 90 to 264 V_{RMS}, I_O = 0 A to 3 A		15.06		
	Output voltage, 9-V setting	V_{IN} = 90 to 264 V_{RMS}, I_O = 0 A to 3 A		9.05		
	Output voltage, 5-V setting	V_{IN} = 90 to 264 V_{RMS}, I_O = 0 A to 3 A		5.05		
$I_{O(FL)}$	Full-load rated output current, 20-V setting	V_{IN} = 90 to 264 V_{RMS}, V_O = 20 V		3.25		A
$I_{O(FL2)}$	Full-load rated output current, 15-V, 9-V, 5-V settings	V_{IN} = 90 to 264 V_{RMS}, V_O = 15 V, 9 V, 5 V		3.00		A
V_{O_pp}	Output ripple voltage, peak to peak 20-V setting	V_{IN} = 90 to 264 V_{RMS}, I_O = 0 A to 3.25 A		150	600	mVpp
	Output ripple voltage, peak to peak 15-V setting	V_{IN} = 90 to 264 V_{RMS}, I_O = 0 A to 3 A		150	450	
	Output ripple voltage, peak to peak 9-V setting	V_{IN} = 90 to 264 V_{RMS}, I_O = 0 A to 3 A		150	300	
	Output ripple voltage, peak to peak 5-V setting	V_{IN} = 90 to 264 V_{RMS}, I_O = 0 A to 3 A		150	200	
$P_{O(OPP)}$	Over-power protection threshold	V_{IN} = 90 to 264 V_{RMS}		70		W
t_{OPP}	Over-power protection duration	V_{IN} = 90 to 264 V_{RMS}, P_O > $P_{O(OPP)}$		160		ms
ΔV_O	Output voltage deviation during step-load transient	V_O = 20 V, I_O step between 0 A to $I_{O(FL)}$ at 100 Hz		-604 / +340	±1000	mVpp
SYSTEM CHARACTERISTICS						
η_{FL_20}	Full-load efficiency, V_O = 20 V	V_{IN} = 230 V_{RMS}, I_O = 3.25 A	94%	94.2%		
		V_{IN} = 115 V_{RMS}, I_O = 3.25 A	94%	94.2%		
		V_{IN} = 90 V_{RMS}, I_O = 3.25 A	93%	93.3%		
η_{avg_20}	4-point average efficiency(1), V_O = 20 V	V_{IN} = 230 V_{RMS}	89%	93.4%		
		V_{IN} = 115 V_{RMS}	89%	92.4%		
$\eta_{10\%_20}$	Efficiency at 10% load, V_O = 20 V	V_{IN} = 230 V_{RMS}, I_O = 10% of $I_{O(FL)}$	79%	83.8%		
		V_{IN} = 115 V_{RMS}, I_O = 10% of $I_{O(FL)}$	79%	89.0%		
T_{AMB}	Ambient operating temperature range	V_{IN} = 90 to 264 V_{RMS}, V_O = 20 V, I_O = 0 to 3.25 A		25°C		

(1) Average efficiency of four load points, I_O = 100%, 75%, 50%, and 25% of $I_{O(FL)}$.

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9.2.2 Detailed Design Procedure

The 65-W USB-PD Charger Application is adapted from the typical application found in the *UCC28782 High-Density Active-Clamp Flyback Controller* data sheet. The UCC28782 data sheet detailed design procedure is not repeated here. Refer to the UCC28782 data sheet for the details in designing the active-clamp flyback primary-side power stage and in using the UCC28782 controller. This detailed design procedure focuses on the specifics of using the LMG2610 in the application.

9.2.2.1 Turn-On Slew-Rate Design

The LMG2610 turn-on slew rates are programmed as discussed in *Turn-On Slew-Rate Control*. In normal active-clamp flyback (ACF) operation the high-side power switch operates at zero-voltage switching (ZVS), so the high-side turn-on time does not affect the switch node slew rate. Therefore, the high-side GaN power FET is programmed to turn on as fast as possible to minimize high-side GaN power-FET third-quadrant losses. The fastest high-side turn-on time is programmed by setting

$$R_{DRVH} < 5.6\ k\Omega \quad (5)$$

In normal ACF operation, the low-side power switch operates at both ZVS and non-ZVS valley switching depending on the load condition. The valley switching occurs at zero transformer current. Therefore, the low-side is programmed to turn on as slow as possible to minimize EMI and circuit ringing with no additional switching loss penalty. The slowest low-side turn-on time is programmed by setting

$$R_{DRVL} > 120\ k\Omega \quad (6)$$

9.2.2.2 Current-Sense Design

The *UCC28782 High-Density Active-Clamp Flyback Controller* data sheet shows the calculation for a traditional current sense resistor, $R_{CS(UCC28782)}$, in series with the low-side power switch current. R_{CS} is calculated with 式 4

$$R_{CS} = 1000 * R_{CS(UCC28782)} \quad (7)$$

The $R_{OPP(UCC2872)}$ determination in the *UCC28782 High-Density Active-Clamp Flyback Controller* data sheet assumes the current sense resistor is very small. R_{OPP} is adjusted to account for the significant R_{CS} value.

$$R_{OPP} = R_{OPP(UCC2872)} - R_{CS} \quad (8)$$

9.3 Power Supply Recommendations

The LMG2610 operates from a single input supply connected to the AUX pin. The BST pin is powered internally by the AUX pin. The LMG2610 is intended to be operated from the same supply managed and used by the power supply controller. The wide recommended AUX voltage range of 10 V to 26 V overlaps common-controller supply-pin turn-on and UVLO voltage limits.

The BST-to-SW external capacitance is recommended to be a ceramic capacitor that is at least 10 nF over operating conditions.

The AUX external capacitance is recommended to be a ceramic capacitor that is at least three-times larger than the BST-to-SW capacitance over operating conditions.

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9.4 Layout

9.4.1 Layout Guidelines

9.4.1.1 Solder-Joint Stress Relief

Large QFN packages can experience high solder-joint stress. Several best practices are recommended to provide solder-joint stress relief. First, the instructions for the NC1, NC2, and NC3 anchor pins found in 表 5-1 must be followed. Second, all the board solder pads must be non-solder-mask defined (NSMD) as shown in the land pattern example in the *Mechanical Data*. Finally, any board trace connected to an NSMD pad must be less than 2/3 the width of the pad on the pad side where it is connected. The trace must maintain this 2/3 width limit for as long as it is not covered by solder mask. After the trace is under solder mask, there are no limits on the trace dimensions. All these recommendations are followed in the *Layout Example*.

9.4.1.2 Signal-Ground Connection

Design the power supply with separate signal and power grounds that only connect in one location. Connect the LMG2610 AGND pin to signal ground. Connect the LMG2610 SL pin and PADL thermal pad to power ground. The LMG2610 serves as the single connection point between the signal and power grounds since the AGND pin, SL pin, and PADL thermal pad are connected internally. Do not connect the signal and power grounds anywhere else on the board except as recommended in the next sentence. To facillitate board debug with the LMG2610 not installed, connect the AGND pad to the PADL thermal pad as shown in the *Layout Example*.

9.4.1.3 CS Pin Signal

As seen with 式 4, the current-sense signal impedance is three orders of magnitude higher than a traditional current-sense signal. This higher impedance has implications for current-sense signal noise susceptibility. Minimize routing the current-sense signal near any noisy traces. Place the current-sense resistor and any filtering capacitors at the far end of the trace next to the controller current-sense input pin.

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9.4.2 Layout Example

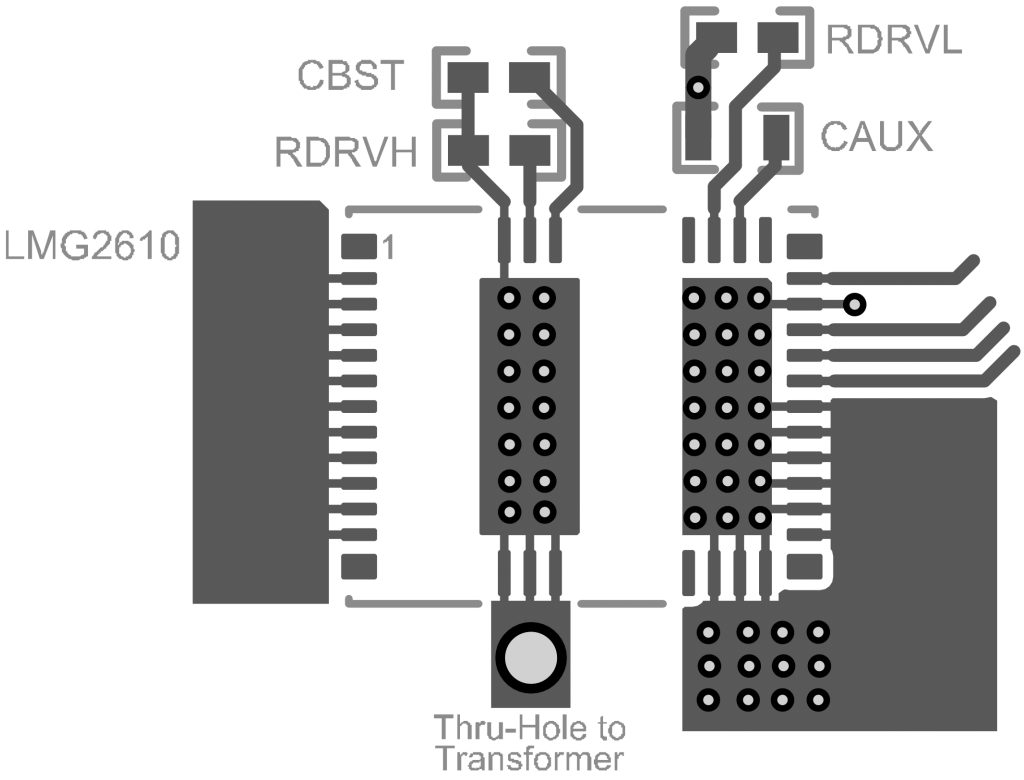


図 9-2. PCB Top Layer (First Layer)

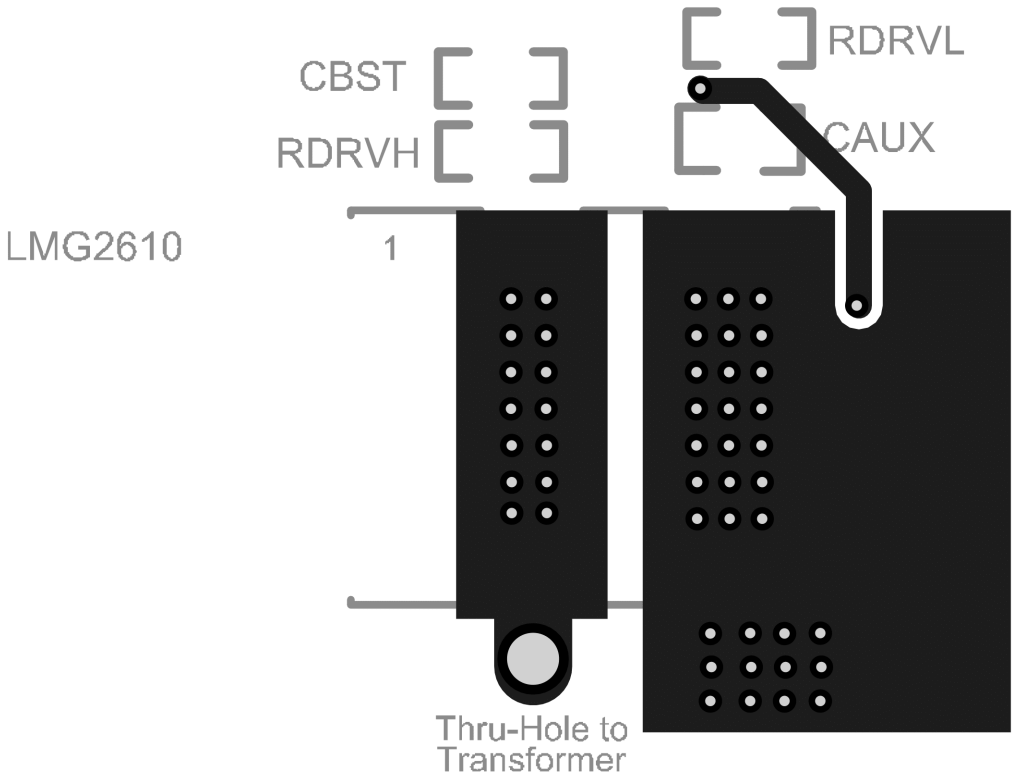


図 9-3. PCB Inner Layer (Second Layer)

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10 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

10.1 Documentation Support

10.1.1 Related Documentation

The LMG2610 Active-Clamp Flyback Power Stage Design Calculator is an Excel-based calculation tool for LMG2610 design.

Using the UCC28782EVM-030 65-W USB-C PD High-Density Active-Clamp Flyback Converter is a User Guide for the EVM

10.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

10.3 サポート・リソース

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10.4 Trademarks

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10.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

10.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

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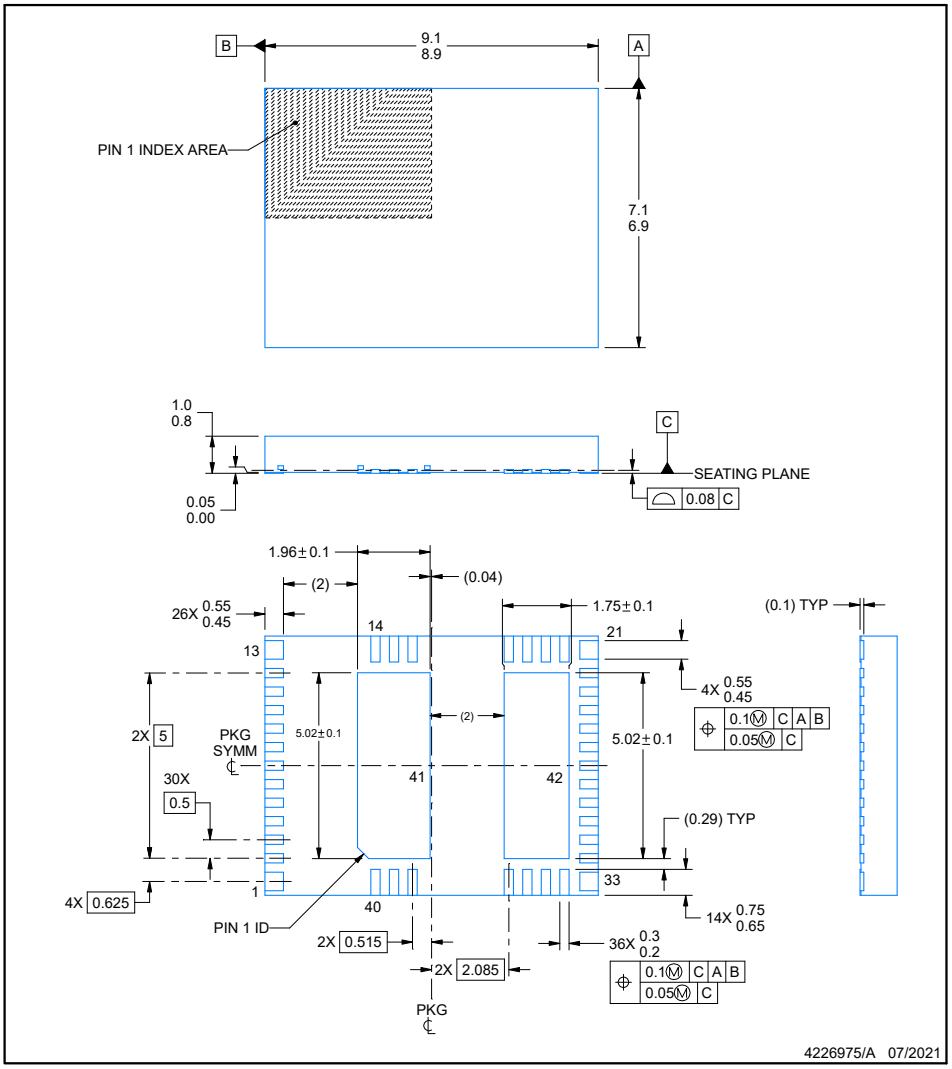
11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGE OUTLINE

RRG0040A-C01 **VQFN - 1.0 mm max height**

PLASTIC QUAD FLATPACK - NO LEAD



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

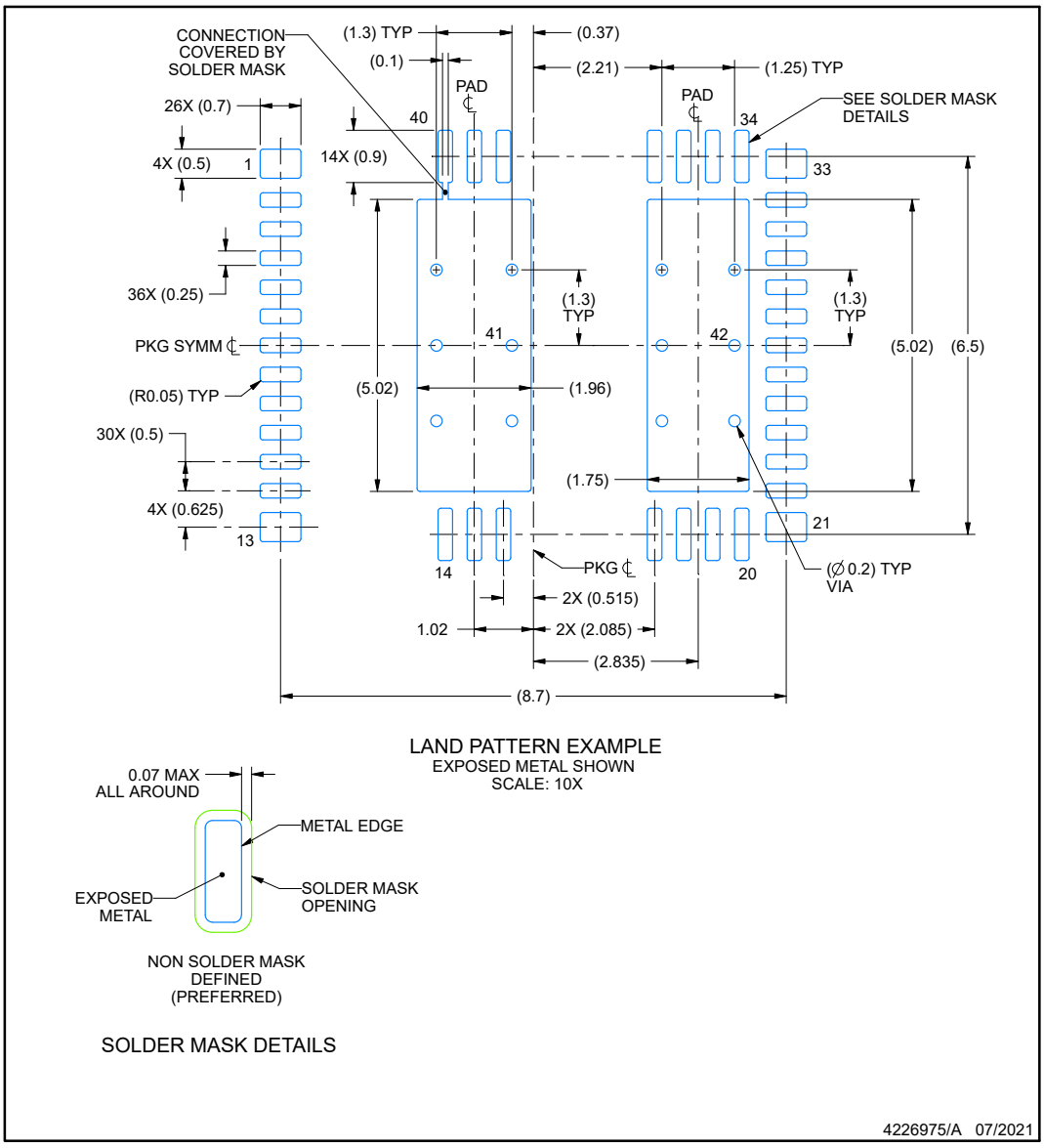
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EXAMPLE BOARD LAYOUT

RRG0040A-C01

VQFN - 1.0 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES: (continued)

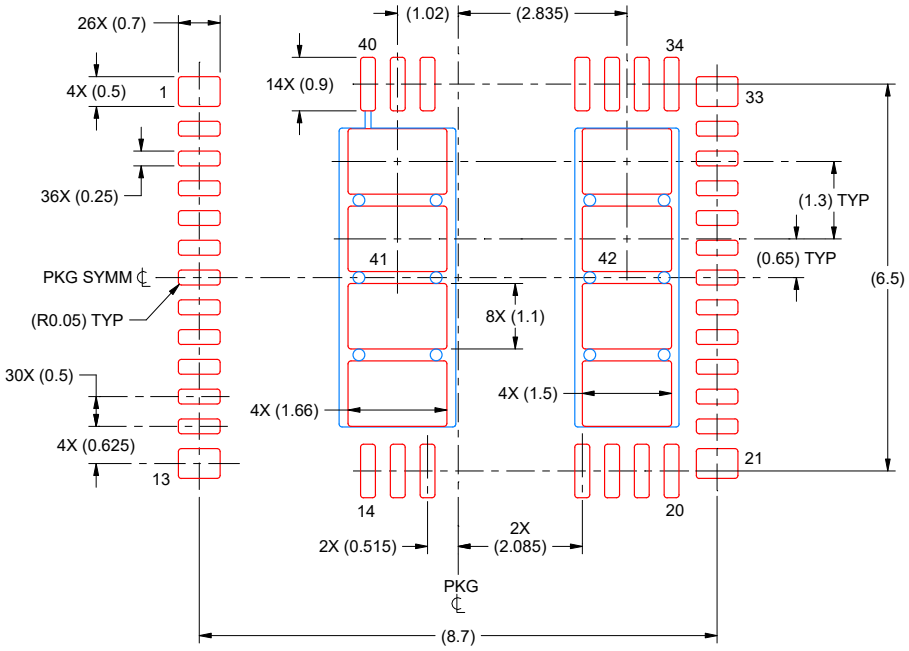
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If some or all are implemented, recommended via locations are shown.

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EXAMPLE STENCIL DESIGN

RRG0040A-C01 — **VQFN - 1.0 mm max height**

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 10X

PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
EXPOSED PAD 41: 74%
EXPOSED PAD 42: 75%

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LMG2610RRGR	Active	Production	VQFN (RRG) | 40	2000 | LARGE T&R	ROHS Exempt	NIPDAU	Level-3-260C-168HRS	-40 to 150	LMG2610 NNNNC
LMG2610RRGR.A	Active	Production	VQFN (RRG) | 40	2000 | LARGE T&R	ROHS Exempt	NIPDAU	Level-3-260C-168HRS	-40 to 150	LMG2610 NNNNC
LMG2610RRGT	Active	Production	VQFN (RRG) | 40	250 | SMALL T&R	ROHS Exempt	NIPDAU	Level-3-260C-168 HR	-40 to 150	LMG2610 NNNNC
LMG2610RRGT.A	Active	Production	VQFN (RRG) | 40	250 | SMALL T&R	ROHS Exempt	NIPDAU	Level-3-260C-168 HR	-40 to 150	LMG2610 NNNNC

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

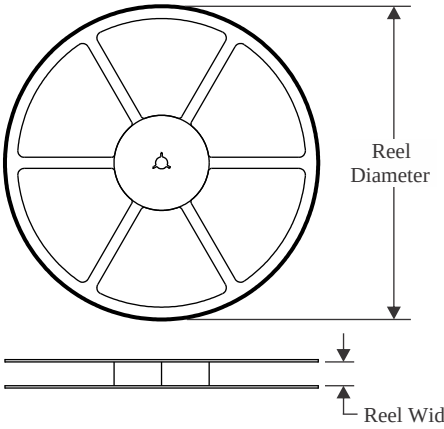
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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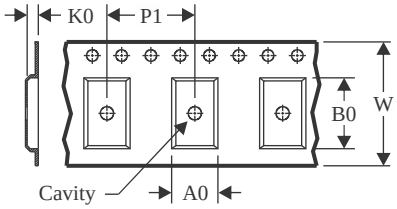
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TAPE AND REEL INFORMATION

REEL DIMENSIONS

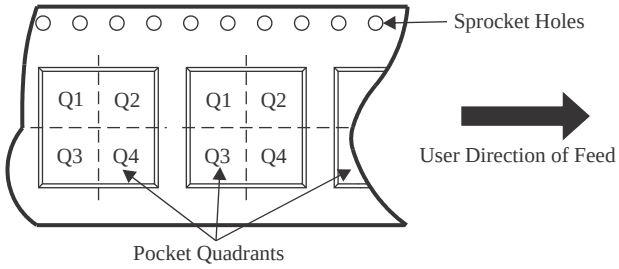


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

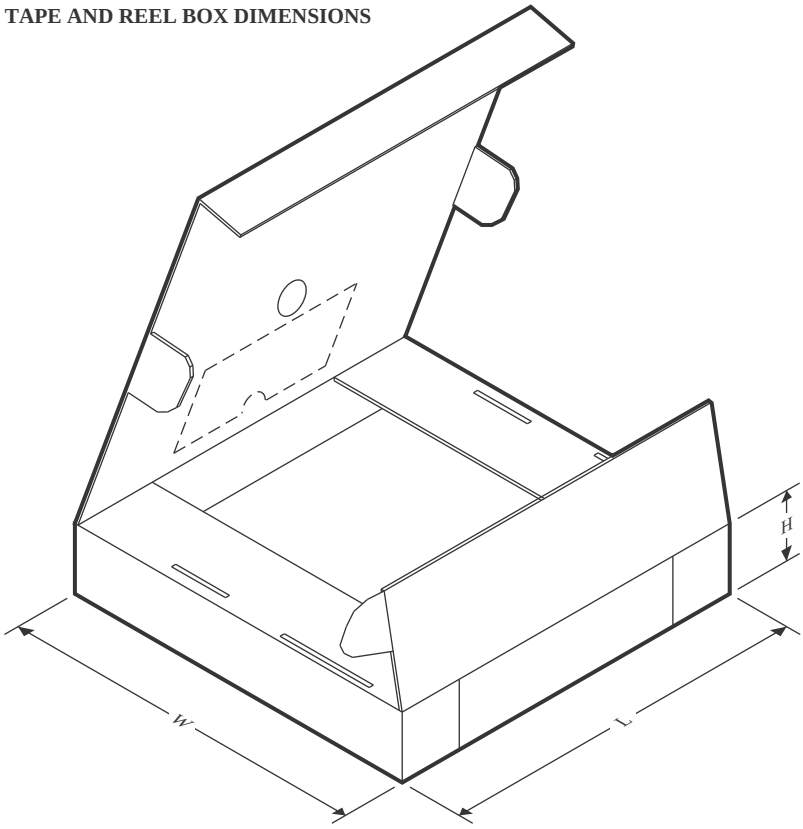
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMG2610RRGR	VQFN	RRG	40	2000	330.0	16.4	9.3	7.3	1.2	12.0	16.0	Q1
LMG2610RRGT	VQFN	RRG	40	250	180.0	16.4	9.3	7.3	1.2	12.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMG2610RRGR	VQFN	RRG	40	2000	367.0	367.0	38.0
LMG2610RRGT	VQFN	RRG	40	250	213.0	191.0	55.0

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