LMH2832 完全差動デュアル、1.1GHz、デジタル可変ゲイン・アンプ

1 特長

- 2チャネルで独立に SPI™制御されるDVGA
- 5V単一電源
- -3dB帯域幅: 1.1GHz (最大ゲイン)
- フラット帯域幅応答: 300MHz
- チャネル間ゲイン・マッチング: ±0.05dB
- チャネル間位相マッチング: ±0.1°
- ゲイン
  - 30dB～–9dB
  - 1dBステップ、±0.2dB
- 出力の3次インターセプト・ポイント(OIP3)
  - 300MHzで43dBm
  - 200MHzで51dBm
- ノイズ値(NF)
  - 300MHzで6.5dB (最大ゲイン)、Z_{IN} = 150Ω
- 可変消費電力
  - チャネルごとに90mA～108mA
- パワーセービングおよびパワーダウン機能
  - チャネルごとにI_Q < 4.5 mA
  - パワーダウン・ピンとSPIでプログラム可能
- 300MHzでの入力リターン・ロス
  - 17dB (R_S = 150Ω)

2 アプリケーション

- DOCSIS 3.1 CMTSアップストリーム直接サンプリング受信機
- CATVモデム信号スケーリング
- プログラマブル・ゲインのIFアンプ
- 汎用RF、IFゲイン・ステージ
- ADCドライバ

3 概要

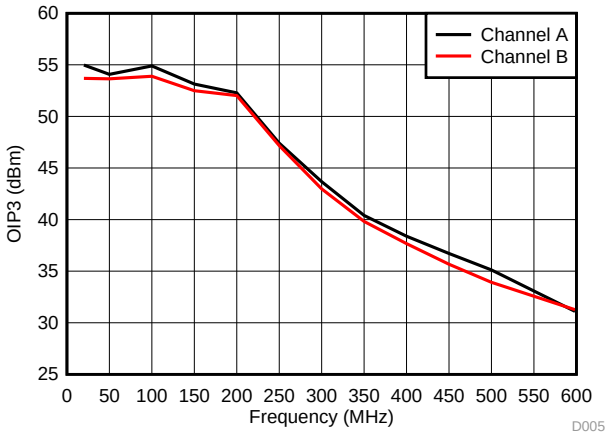
LMH2832は直線性が高い2チャネルのデジタル可変ゲイン・アンプ(DVGA)で、高速信号チェーンおよびデータ収集システム用です。LMH2832は高い帯域幅、低い歪み、低いノイズを実現するよう最適化されているため、2チャネル、14ビットのA/Dコンバータ(ADC)ドライバに理想的です。このデバイスは、1つの固定ゲイン・ブロックと、1つの可変アッテネータで構成され、合計ゲインは30dB、最大減衰は39dBです。ゲインの範囲は30dB～-9dBで、1dBステップで設定でき、ゲイン精度は±0.2dBです。入力インピーダンスは1:3Ωまたは1:2Ω比率のバランを使用して、それぞれ50Ωまたは75Ωに簡単にマッチングできます。LMH2832は汎用ADCを駆動するよう設計されており、ケーブル上データ・サービス・インターフェイス仕様(DOCSIS) 3.0の32直交振幅変調(QAM)キャリア、およびDOCSIS 3.1の広帯域直交周波数分割多重化(OFDM)システムの両方の要件も満たしています。LMH2832は非常に優れたNF (6.5dB)と直線性を持ち、DOCSISの仕様内で動作するよう設計されています。パワーダウン状態での静止電流はチャネルごとに5mA未満で、動作時の標準消費電流はチャネルごとに105mAです。

製品情報(1)

型番	パッケージ	本体サイズ(公称)
LMH2832	VQFN (40)	6.00mm×6.00mm

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。

出力の3次インターセプト・ポイント(OIP3)特性



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4 改訂履歴

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

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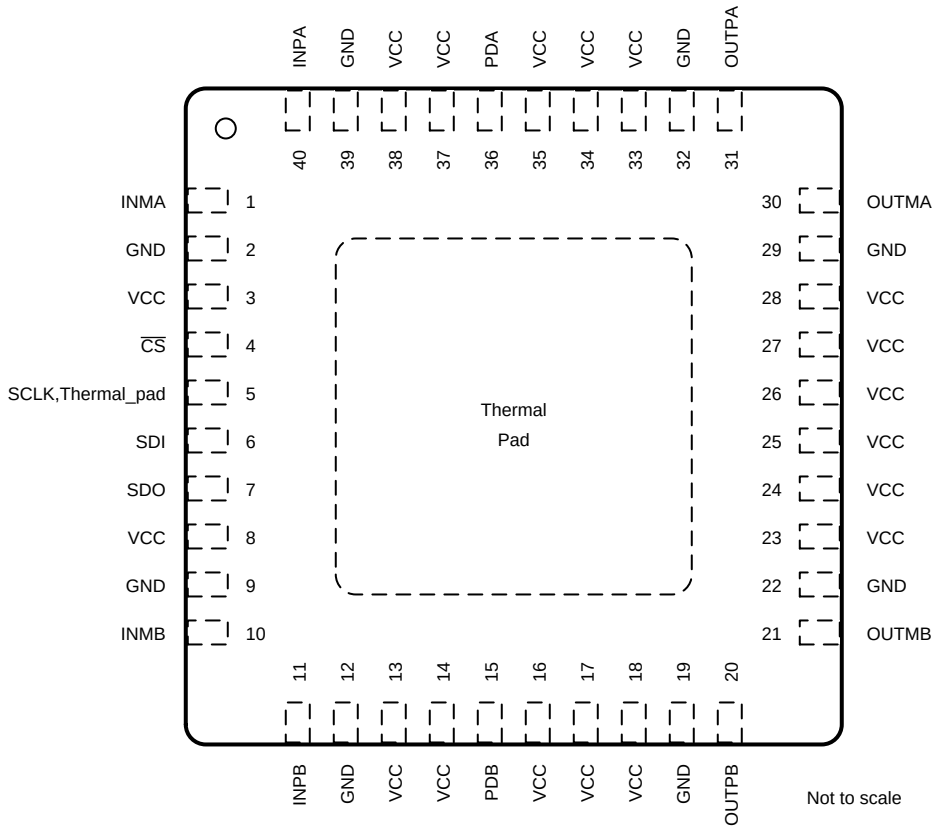
5 Device Comparison Table

Table 1. DVGA Device Comparison

DEVICE	MAX GAIN, BW	DISTORTION	NOISE FIGURE
LMH6401	26 dB, 4.5 GHz	43-dBm OIP3 at 200 MHz, –80-dBc HD3 at 200 MHz	7.7 dB
LHM6517	22 dB, 1.2 GHz	43-dBm OIP3 at 200 MHz, –74-dBc HD3 at 200 MHz	5.5 dB
LMH6521	26 dB, 1.2 GHz	49-dBm OIP3 at 200 MHz, –84-dBc HD3 at 200 MHz	7.3 dB
LMH6881	26 dB, 2.4 GHz	42-dBm OIP3 at 200 MHz, –76-dBc HD3 at 200 MHz	9.7 dB

6 Pin Configuration and Functions

RHA Package
40-Pin VQFN
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
$\overline{CS}$	4	I	Serial interface enable, active low
GND	2, 9, 12, 19, 22, 29, 32, 39	I	Analog ground
INMA	1	I	Negative differential input, channel A
INMB	10	I	Negative differential input, channel B
INPA	40	I	Positive differential input, channel A
INPB	11	I	Positive differential input, channel B
OUTMA	30	O	Negative differential output, channel A
OUTMB	21	O	Negative differential output, channel B
OUTPA	31	O	Positive differential output, channel A
OUTPB	20	O	Positive differential output, channel B
PDB	15	I	Power-down control, channel B (logic high = power-down)
PDA	36	I	Power-down control, channel A (logic high = power-down)
SCLK	5	I	Serial interface clock input
SDI	6	I	Serial interface data input
SDO	7	O	Serial interface data output
VCC	3, 8, 13, 14, 16, 17, 18, 23, 24, 25, 26, 27, 28, 33, 34, 35, 37, 38	I	Analog voltage supply
Thermal pad		—	Connected to ground

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7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[1]

		MIN	MAX	UNIT
Power supply		–0.5	5.5	V
Input applied to analog inputs	INPA, INMA, INPB, INMB	–0.5	5.5	V
Voltage applied to input pins		–0.5	5.5	V
Digital input/output voltage range		–0.3	2	V
Operating junction temperature, T_J			125	°C
Storage temperature, T_{stg}		–40	125	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001[1]	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101[2]	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_S	Power-supply voltage	4.75	5	5.25	V
	Specified operating temperature range	–40		85	°C

7.4 Thermal Information

THERMAL METRIC[1]		LMH2832 RHA (VQFN) 40 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	29.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	20.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	6.6	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.3	°C/W
ψ_{JB}	Junction-to-board characterization parameter	6.5	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	2.3	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report (SPRA953).

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7.5 Electrical Characteristics

at T_A = 25°C, V_{S+} = 5 V, R_i = 75 Ω, R_L = 150 Ω, maximum gain (1:2-Ω ratio transformer plus 30-dB DVGA gain), f = 5 MHz to 300 MHz, V_O converted to single-ended (SE) measurement with a transformer, and default current setting (unless otherwise noted); upon power-up, gain is set to mid-range

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT	TEST LEVEL(1)
AC PERFORMANCE							
LSBW	Large-signal, –3-dB bandwidth	G = 30 dB, V_O = 2 V_{PP}		1140		MHz	C
		G = 0 dB, V_O = 2 V_{PP}		2350			C
BW	Bandwidth for 0.1-dB flatness			300		MHz	C
HD2	Second-order harmonic distortion	f = 100 MHz, V_O = 2 V_{PP}		–88		dBc	C
		f = 200 MHz, V_O = 2 V_{PP}		–76			C
		f = 300 MHz, V_O = 2 V_{PP}		–63			C
		f = 450 MHz, V_O = 2 V_{PP}		–58			C
HD3	Third-order harmonic distortion	f = 100 MHz, V_O = 2 V_{PP}		–94		dBc	C
		f = 200 MHz, V_O = 2 V_{PP}		–90			C
		f = 300 MHz, V_O = 2 V_{PP}		–81			C
		f = 450 MHz, V_O = 2 V_{PP}		–75			C
IMD3	Third-order intermodulation distortion	f = 100 MHz, tone spacing = 2 MHz, P_{OUT}(2) = 0 dBm per tone		–106		dBc	C
		f = 200 MHz, tone spacing = 2 MHz		–102			C
		f = 300 MHz, tone spacing = 2 MHz		–86			C
OIP3	Output third-order intercept point	f = 100 MHz, tone spacing = 2 MHz, P_{OUT} = 0 dBm per tone		53		dBm	C
		f = 200 MHz, tone spacing = 2 MHz, P_{OUT} = 0 dBm per tone		51			C
		f = 300 MHz, tone spacing = 2 MHz, P_{OUT} = 0 dBm per tone		43			C
P1dB	1-dB compression point	f = 100 MHz, R_L = 150 Ω		16		dBm	C
		f = 200 MHz, R_L = 150 Ω		16			C
		f = 300 MHz, R_L = 150 Ω		16.5			C
NF	Noise figure	R_i = 150 Ω, f = 300 MHz, max gain		6.5		dB	C
	Output-referred voltage noise	f = 300 MHz, max gain		47.7		nV/√Hz	C
S11	Input return loss	f = 300 MHz		17		dB	C
S22	Reverse Isolation	Including input transformer, f < 300 MHz		53		dB	C
	Channel-to-channel crosstalk	f = 300 MHz, channel A to B		–77		dB	C
		f = 300 MHz, channel B to A		–81			
	Channel-to-channel phase matching	f = 200 MHz		±0.1		°	C
	Channel-to-channel gain matching	f = 200 MHz		±0.05		dB	C
GAIN PARAMETERS							
	Maximum voltage gain	f = dc, gain code = 00h	29.5	30	30.5	dB	A
	Minimum voltage gain	f = dc, gain code = 27h	–9.5	–9	–8.5	dB	A
	Gain range			39		dB	C
	Gain step size	Between any two adjacent gain settings	0.75	1	1.25	dB	A
E_G	Gain error	For any gain value	–0.5	0	0.5	dB	A
	Cumulative gain error	Referenced to max gain	–1		1	dB	A
	Gain step transition time			6		ns	C

(1) Test levels: (A) 100% tested at 25°C. Overtemperature limits by characterization and simulation. (B) Limits set by characterization and simulation. (C) Typical value only for information.
(2) P_{OUT} is the signal tone power at the output of the device.

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Electrical Characteristics (continued)

at T_A = 25°C, V_{S+} = 5 V, R_i = 75 Ω, R_L = 150 Ω, maximum gain (1:2-Ω ratio transformer plus 30-dB DVGA gain), f = 5 MHz to 300 MHz, V_O converted to single-ended (SE) measurement with a transformer, and default current setting (unless otherwise noted); upon power-up, gain is set to mid-range

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT	TEST LEVEL (1)
ANALOG INPUT CHARACTERISTICS							
z_{in}	Input resistance	f = dc, differential	135	150	165	Ω	A
C_{in}	Input capacitance	Differential		0.6		pF	C
	Single-ended input resistance	f = dc	67.5	75	82.5	Ω	A
	Single-ended input capacitance			1.2		pF	C
V_{ICM}	Input common-mode voltage	Internally biased to mid-supply	–0.2		0.2	V	A
V_{IL}	Low-level input voltage range	Differential gain shift < 1 dB		(V_{S-}) + 1.5		V	C
V_{IH}	High-level input voltage range	Differential gain shift < 1 dB		(V_{S+}) – 1.5		V	C
ANALOG OUTPUT CHARACTERISTICS							
z_o	Output resistance	Differential		20		Ω	C
V_{OL}	Low-level output voltage range	V_S = 5 V, GND = 0 V		1.15	1.25	V	A
V_{OH}	High-level output voltage range	V_S = 5 V, GND = 0 V	3.75	3.85		V	A
V_{OM}	Maximum output voltage swing	T_A = 25°C	5	5.4		V	A
		T_A = –40°C to +85°C		5.4	6.4		B
CMRR	Common-mode rejection ratio			56		dB	C
POWER SUPPLY							
V_S	Supply voltage		4.75	5.0	5.25	V	A
I_Q	Quiescent current per channel	Default current, default bias setting	102	105	108	mA	A
		Min current, lowest power setting		90			C
		Max current, highest bias setting		108			C
±PSRR	Power-supply rejection ratio (3)	Gain = 30 dB		–48		dB	C
POWER-DOWN (4)							
	Power-down quiescent current (per channel)	T_A = 25°C		2.5	6	mA	A
		T_A = –40°C to +85°C			6.5		B
	Power-down bias current		–2	–1		µA	A
	Turn-on time delay	Time to V_O = 90% of final value, gain = 0 dB, V_I = 2 V		55		ns	C
	Turn-off time delay	Time to V_O = 10% of original value, gain = 0 dB, V_I = 2 V		110		ns	C
	Forward isolation in PD mode	f = 300 MHz		–67		dB	C
DIGITAL INPUTS/OUTPUTS							
V_{IH}	High-level input voltage		1.4		2	V	A
V_{IL}	Low-level input voltage		–0.3		0.8	V	A
V_{OH}	High-level output voltage	I_{OH} = –100 µA	1.65			V	A
		I_{OH} = –2 mA	1.55				A
V_{OL}	Low-level output voltage	I_{OL} = 100 µA			0.1	V	A
		I_{OL} = 2 mA			0.2		A

(3) PSRR is defined with respect to a differential output.
(4) The device power-down function can be controlled by the PDx pins or by the power-down register accessible from the SPI interface.

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7.6 Timing Requirements: SPI

		MIN	TYP	MAX	UNIT
f_{S_C}	SCLK frequency (1)	0	25	50	MHz
t_{PH}	SCLK pulse duration, high		10		ns
t_{PL}	SCLK pulse duration, low		10		ns
t_{SU}	SDI setup		3		ns
t_H	SDO hold		3		ns
t_{IZ}	SDO tri-state		3		ns
t_{ODZ}	SDO driven to tri-state (2)	0	10	20	ns
t_{OZD}	SDO tri-state to driven	0	2	5	ns
t_{OD}	SDO output delay (2)	0	10	12	ns
t_{CSS}	$\overline{CS}$ setup (3)	3	5		ns
t_{CSH}	$\overline{CS}$ hold		3		ns
t_{IAG}	Inter-access gap		20		ns

(1) Tested on the automated test equipment (ATE) only up to 25 MHz.
(2) Referenced to the negative edge of SCLK.
(3) Referenced to the positive edge of SCLK.

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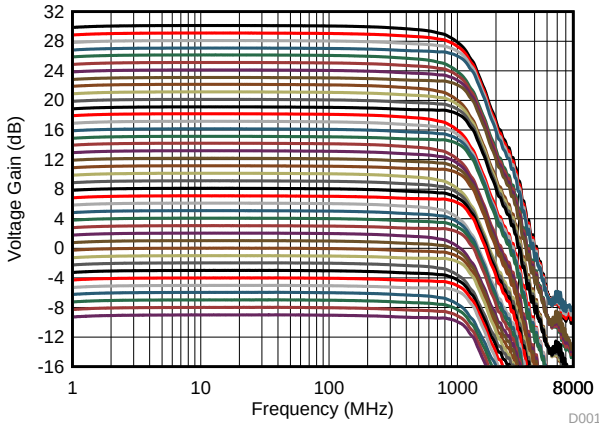
7.7 Typical Characteristics

at T_A = 25°C, V_{S+} = 5 V, R_i = 75 Ω, R_L = 150 Ω, maximum gain (1:2-Ω ratio transformer plus 30-dB DVGA gain), f = 5 MHz to 300 MHz, V_O converted to single-ended (SE) measurement with transformer, and default current setting (unless otherwise noted); upon power-up, gain is set to mid-range



V_O = 2 V_{PP}

Figure 1. Voltage Gain vs Frequency (1-dB Gain Steps)

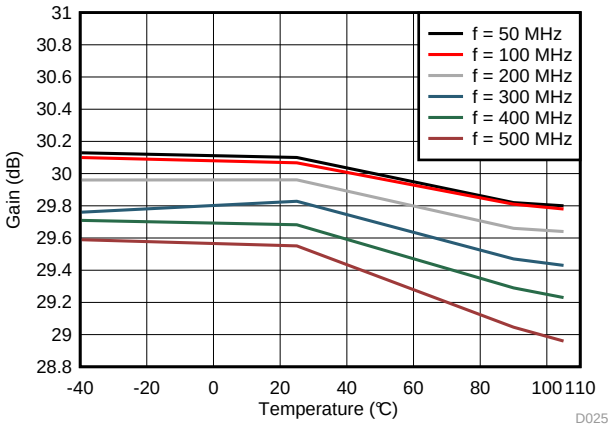
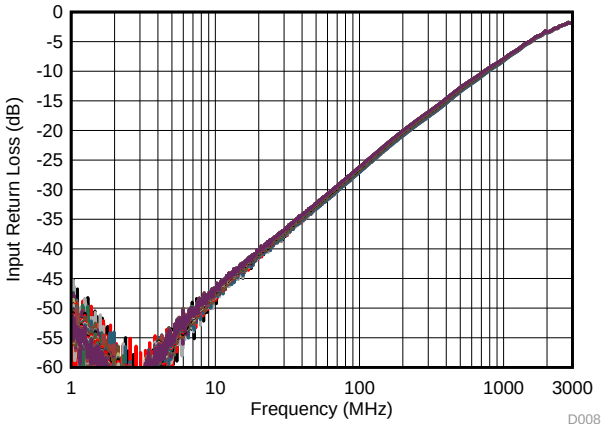
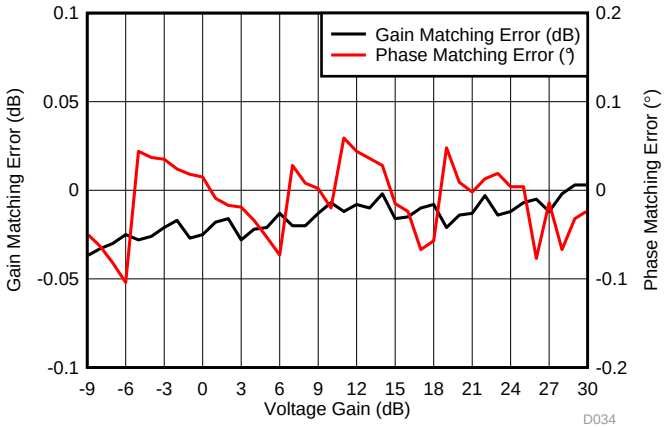


Figure 2. Gain Flatness vs Temperature



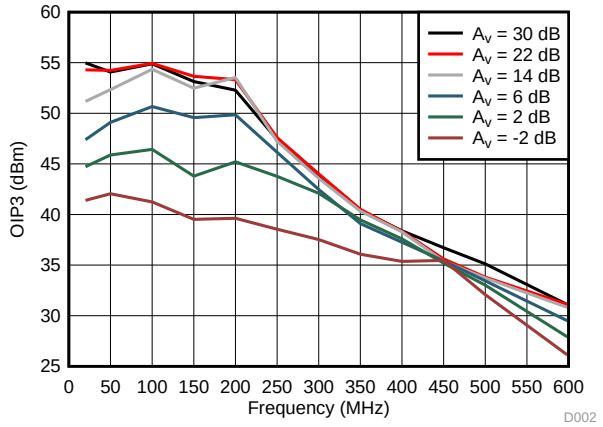
Differential input impedance (Z_{IN}) = 150 Ω, all gain settings

Figure 3. Input Return Loss vs Frequency



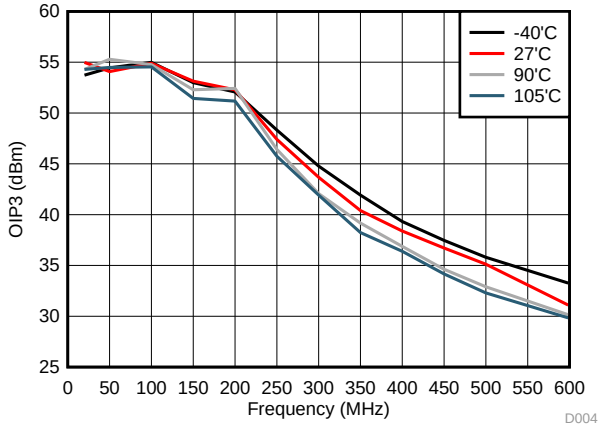
f = 200 MHz

Figure 4. Channel-to-Channel Mismatch Error



P_{OUT} = 0 dBm per tone

Figure 5. OIP3 vs Frequency and Voltage Gain



P_{OUT} = 0 dBm per tone

Figure 6. OIP3 vs Frequency and Temperature

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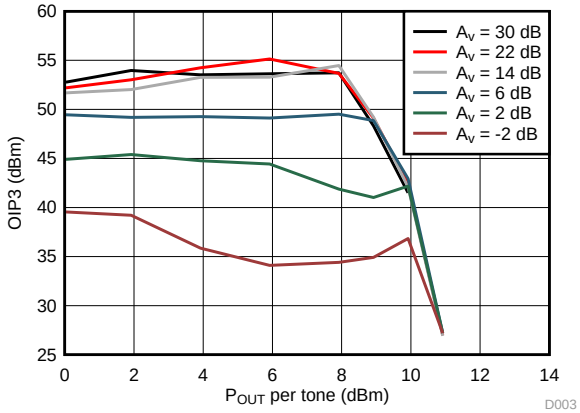
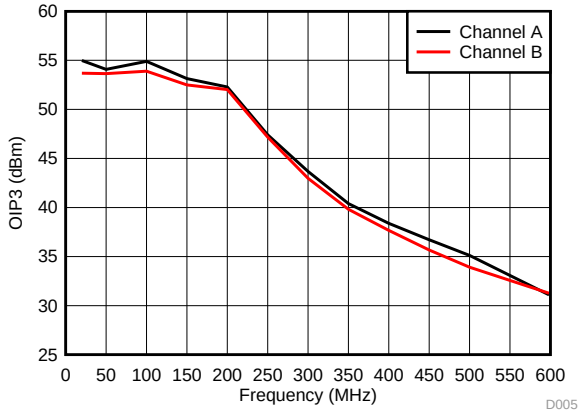
Typical Characteristics (continued)

at T_A = 25°C, V_{S+} = 5 V, R_i = 75 Ω, R_L = 150 Ω, maximum gain (1:2-Ω ratio transformer plus 30-dB DVGA gain), f = 5 MHz to 300 MHz, V_O converted to single-ended (SE) measurement with transformer, and default current setting (unless otherwise noted); upon power-up, gain is set to mid-range



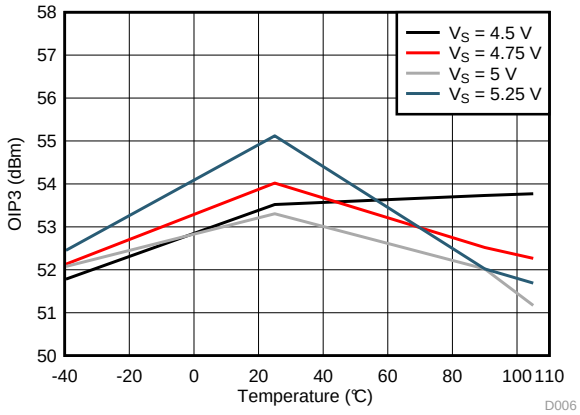
f = 200 MHz

Figure 7. OIP3 vs Output Power



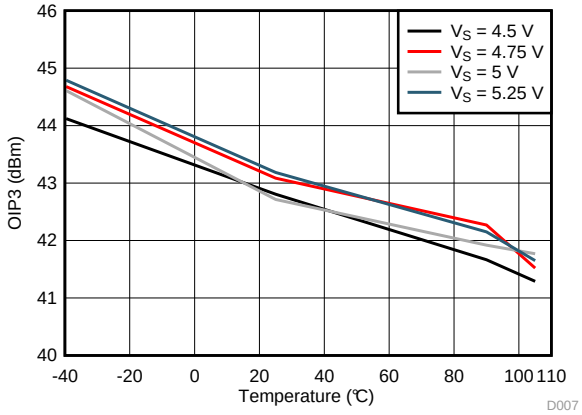
P_{OUT} = 0 dBm per tone

Figure 8. OIP3 Channel Comparison



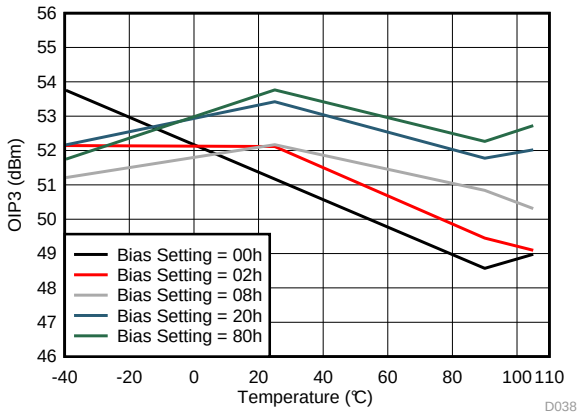
P_{OUT} = 0 dBm per tone

Figure 9. OIP3 vs Temperature and Supply Voltage (f = 200 MHz)



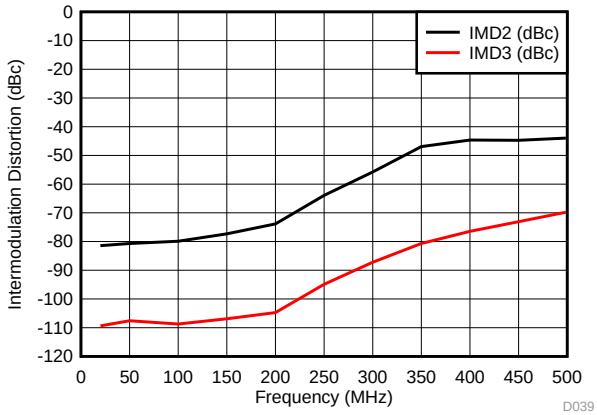
P_{OUT} = 0 dBm per tone

Figure 10. OIP3 vs Temperature and Supply Voltage (f = 300 MHz)



P_{OUT} = 0 dBm per tone

Figure 11. OIP3 vs Temperature and Bias Setting (f = 200 MHz)



P_{OUT} = 0 dBm per tone

Figure 12. Intermodulation Distortion vs Frequency

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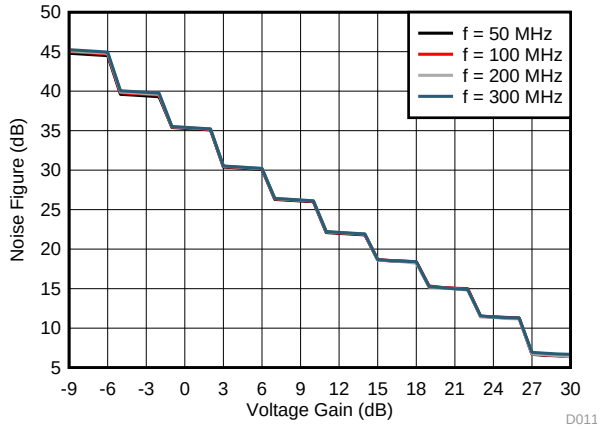
Typical Characteristics (continued)

at T_A = 25°C, V_{S+} = 5 V, R_i = 75 Ω, R_L = 150 Ω, maximum gain (1:2-Ω ratio transformer plus 30-dB DVGA gain), f = 5 MHz to 300 MHz, V_O converted to single-ended (SE) measurement with transformer, and default current setting (unless otherwise noted); upon power-up, gain is set to mid-range



Z_{IN} = 150 Ω

Figure 13. Noise Figure vs Voltage Gain

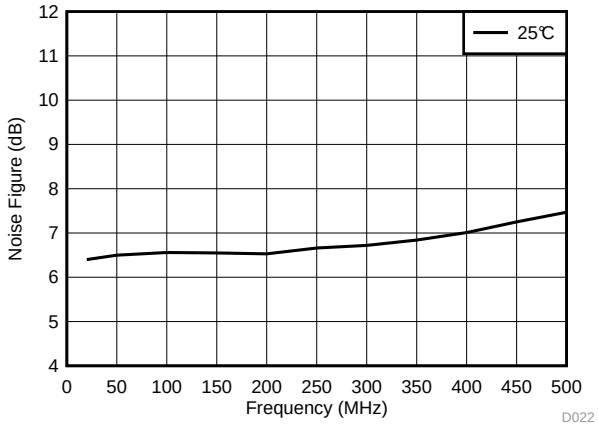
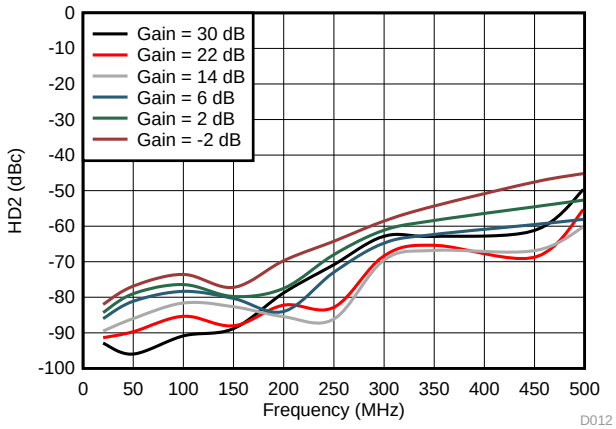
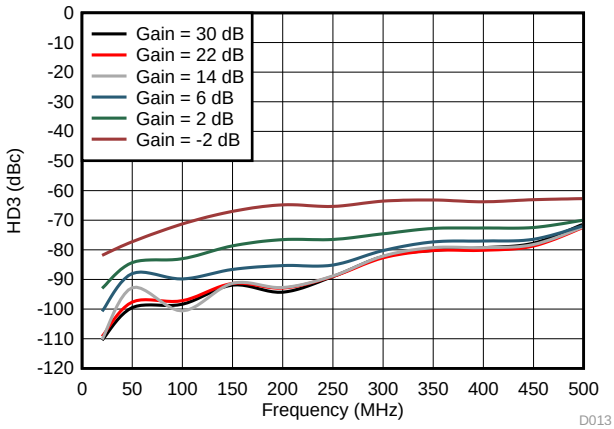


Figure 14. Noise Figure vs Frequency



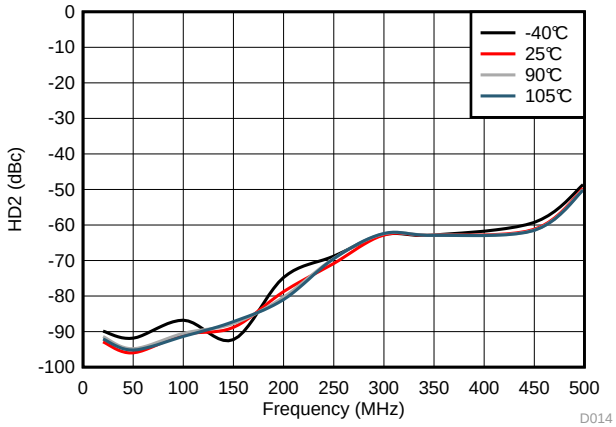
V_O = 2 V_{PP}

Figure 15. HD2 vs Frequency and Gain Settings



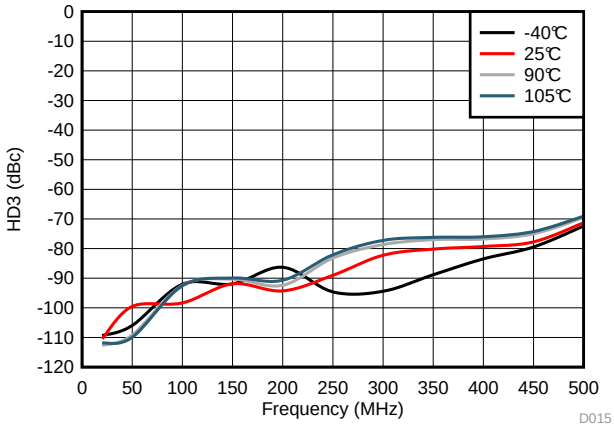
V_O = 2 V_{PP}

Figure 16. HD3 vs Frequency and Gain Settings



V_O = 2 V_{PP}

Figure 17. HD2 vs Frequency and Temperature



V_O = 2 V_{PP}

Figure 18. HD3 vs Frequency and Temperature

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Typical Characteristics (continued)

at T_A = 25°C, V_{S+} = 5 V, R_i = 75 Ω, R_L = 150 Ω, maximum gain (1:2-Ω ratio transformer plus 30-dB DVGA gain), f = 5 MHz to 300 MHz, V_O converted to single-ended (SE) measurement with transformer, and default current setting (unless otherwise noted); upon power-up, gain is set to mid-range

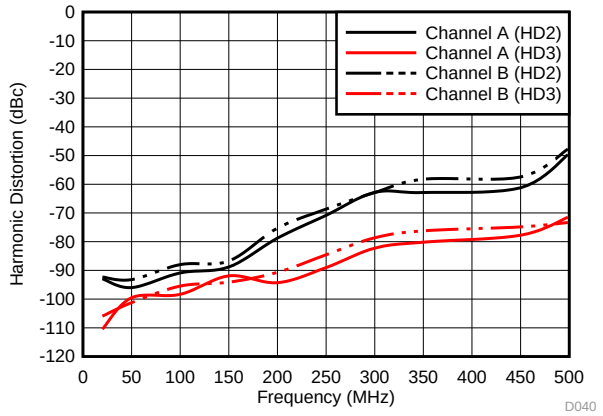

Figure 19. Harmonic Distortion Between Channels

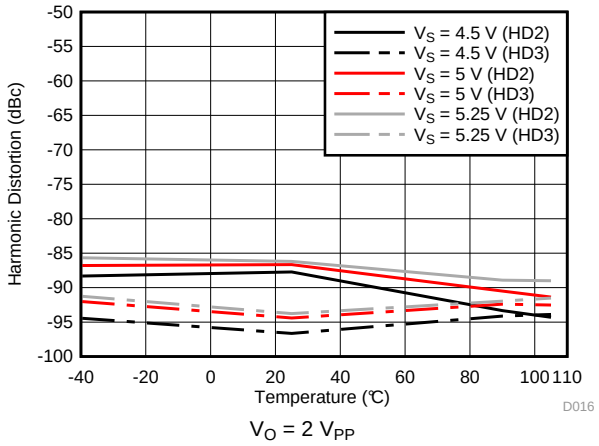

Figure 20. Harmonic Distortion vs Temperature and Supply Voltage (100 MHz)

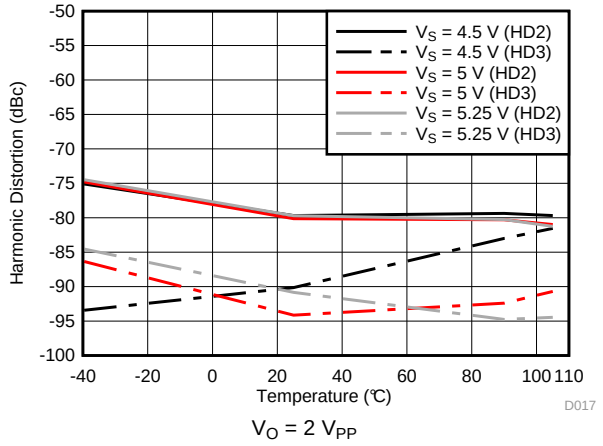

Figure 21. Harmonic Distortion vs Temperature and Supply Voltage (200 MHz)

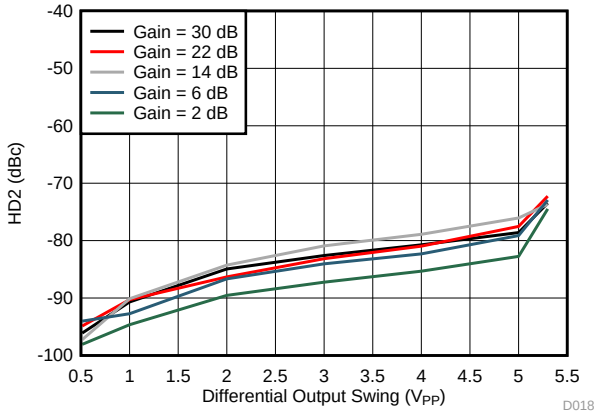

Figure 22. HD2 vs Differential Output Swing (100 MHz)

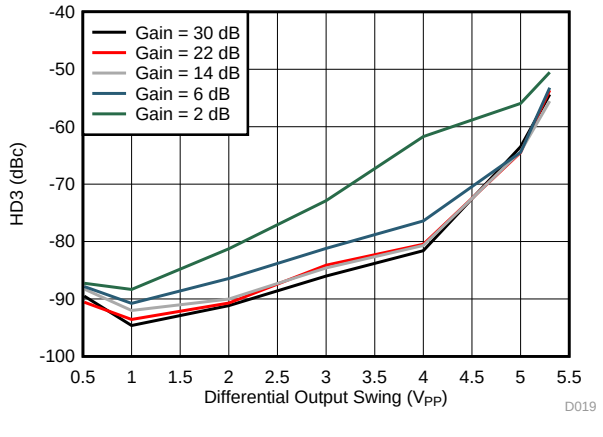

Figure 23. HD3 vs Differential Output Swing (100 MHz)

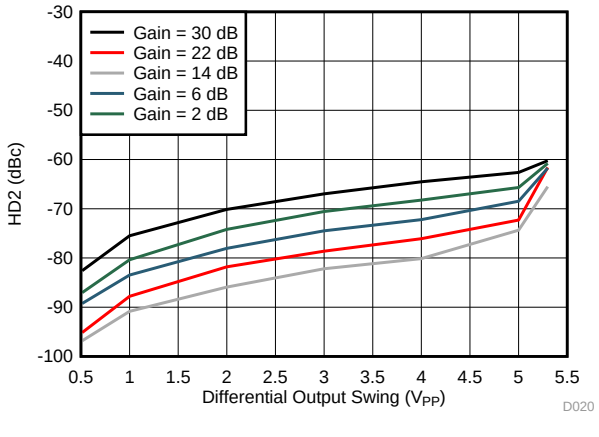

Figure 24. HD2 vs Differential Output Swing (200 MHz)

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Typical Characteristics (continued)

at T_A = 25°C, V_{S+} = 5 V, R_i = 75 Ω, R_L = 150 Ω, maximum gain (1:2-Ω ratio transformer plus 30-dB DVGA gain), f = 5 MHz to 300 MHz, V_O converted to single-ended (SE) measurement with transformer, and default current setting (unless otherwise noted); upon power-up, gain is set to mid-range

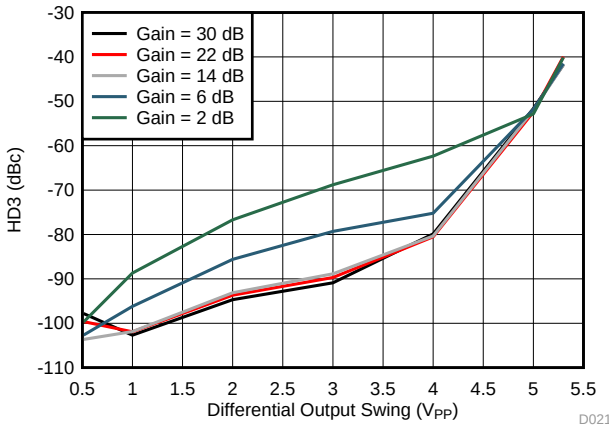

Figure 25. HD3 vs Differential Output Swing (200 MHz)

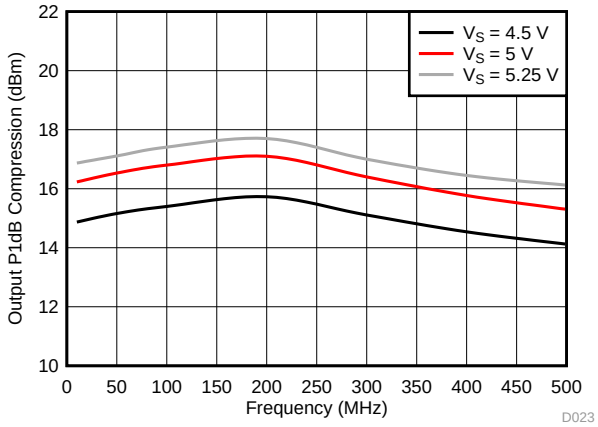

Figure 26. Output P1dB Compression vs Frequency

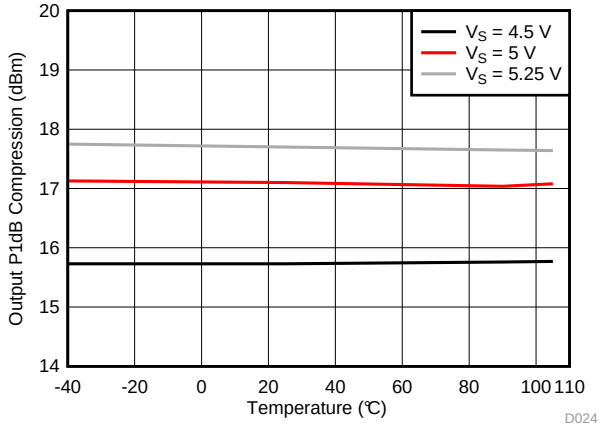

Figure 27. Output P1dB Compression vs Temperature

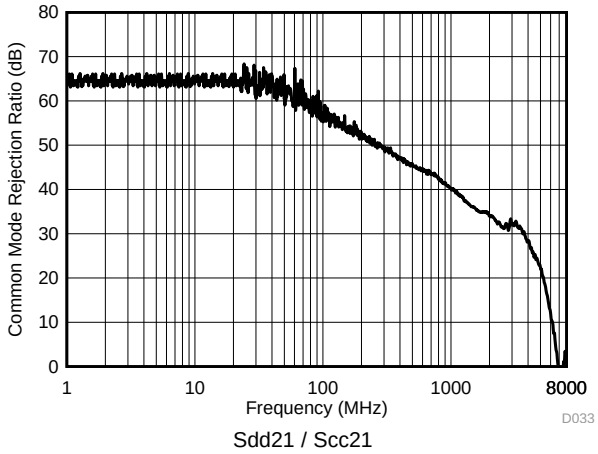

Figure 28. CMRR vs Frequency

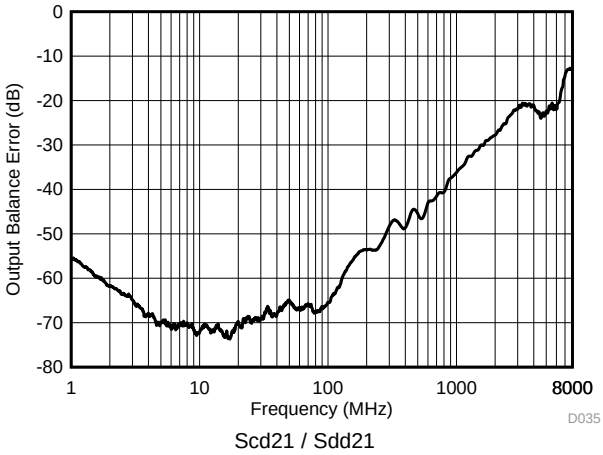

Figure 29. Output Balance Error vs Frequency

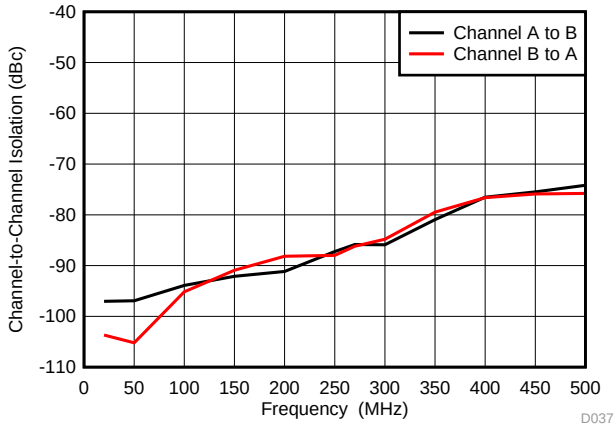

Figure 30. Channel-to-Channel Isolation vs Frequency

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Typical Characteristics (continued)

at T_A = 25°C, V_{S+} = 5 V, R_i = 75 Ω, R_L = 150 Ω, maximum gain (1:2-Ω ratio transformer plus 30-dB DVGA gain), f = 5 MHz to 300 MHz, V_O converted to single-ended (SE) measurement with transformer, and default current setting (unless otherwise noted); upon power-up, gain is set to mid-range

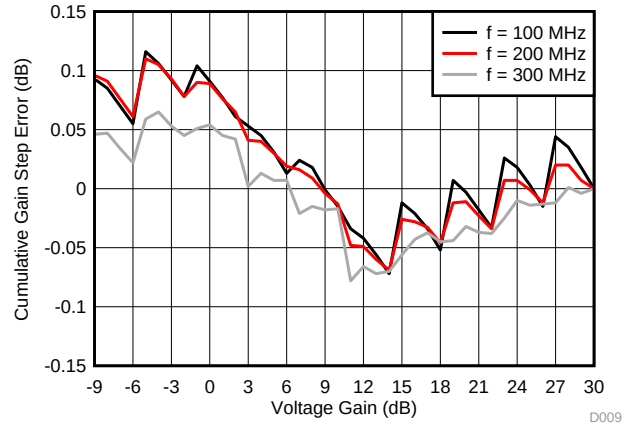

Figure 31. Cumulative Gain Step Error vs Voltage Gain

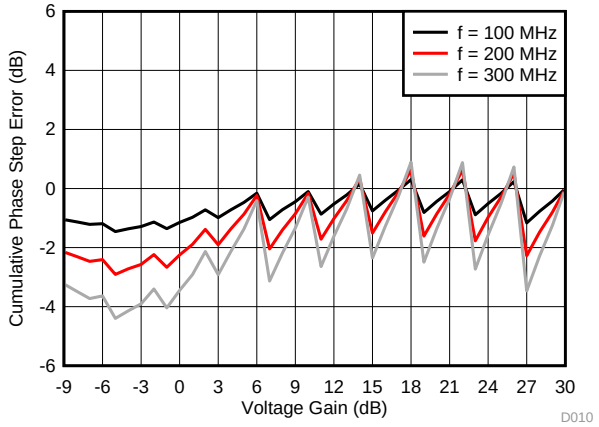

Figure 32. Cumulative Phase Step Error vs Voltage Gain

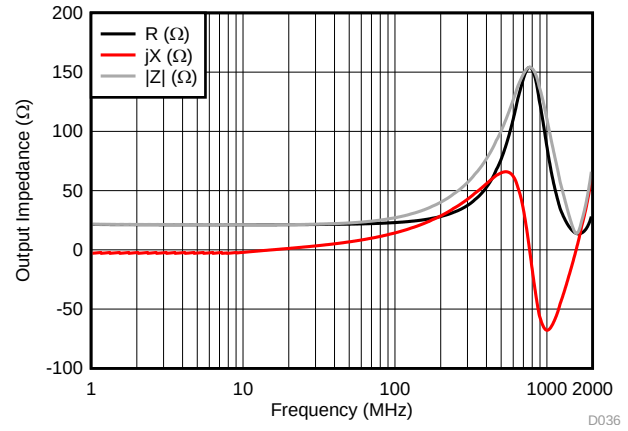

Figure 33. Output Impedance vs Frequency

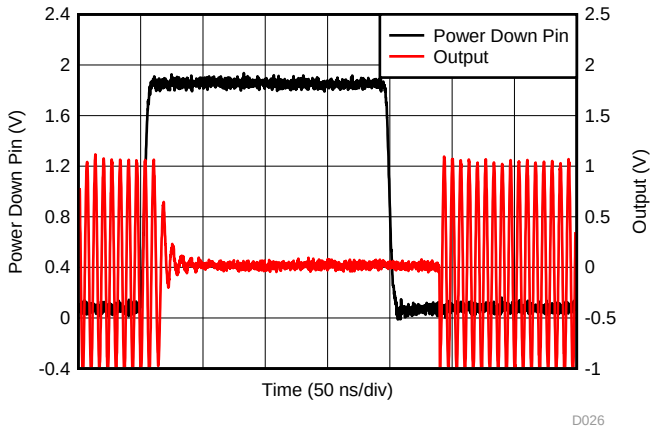

Figure 34. Power-Down Transition Response

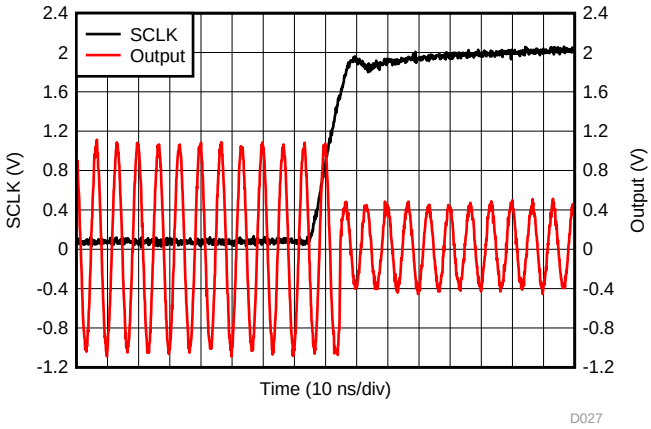

Figure 35. Gain Switching Response (A_V = 30 dB to 22 dB)

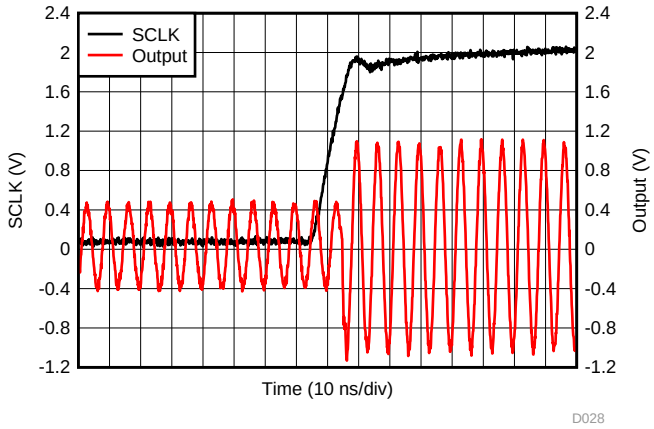

Figure 36. Gain Switching Response (A_V = 22 dB to 30 dB)

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Typical Characteristics (continued)

at T_A = 25°C, V_{S+} = 5 V, R_i = 75 Ω, R_L = 150 Ω, maximum gain (1:2-Ω ratio transformer plus 30-dB DVGA gain), f = 5 MHz to 300 MHz, V_O converted to single-ended (SE) measurement with transformer, and default current setting (unless otherwise noted); upon power-up, gain is set to mid-range

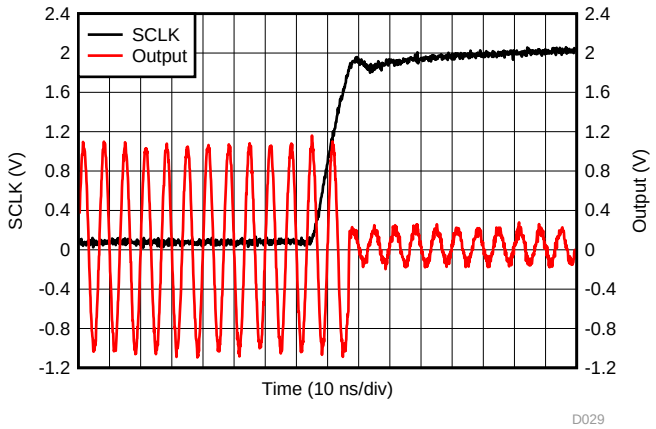

Figure 37. Gain Switching Response (A_V = 30 dB to 14 dB)

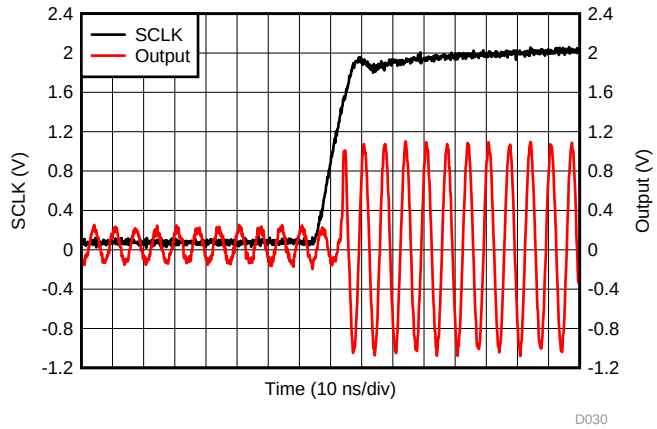

Figure 38. Gain Switching Response (A_V = 14 dB to 30 dB)

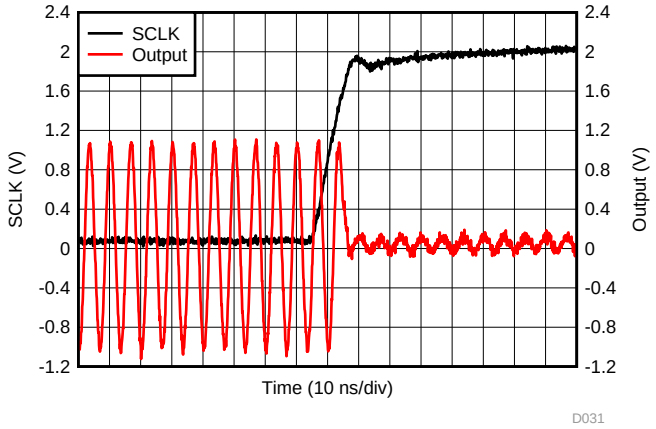

Figure 39. Gain Switching Response (A_V = 30 dB to 6 dB)

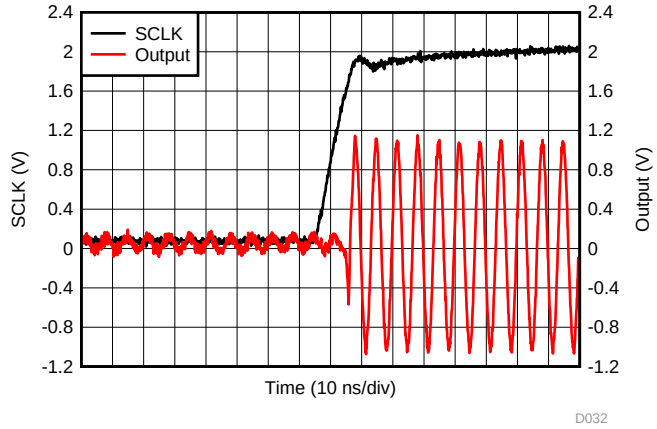

Figure 40. Gain Switching Response (A_V = 6 dB to 30 dB)

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8 Parameter Measurement Information

8.1 Setup Diagrams

Figure 41 to Figure 44 illustrate various test setup diagrams using the LMH2832 evaluation module (EVM).

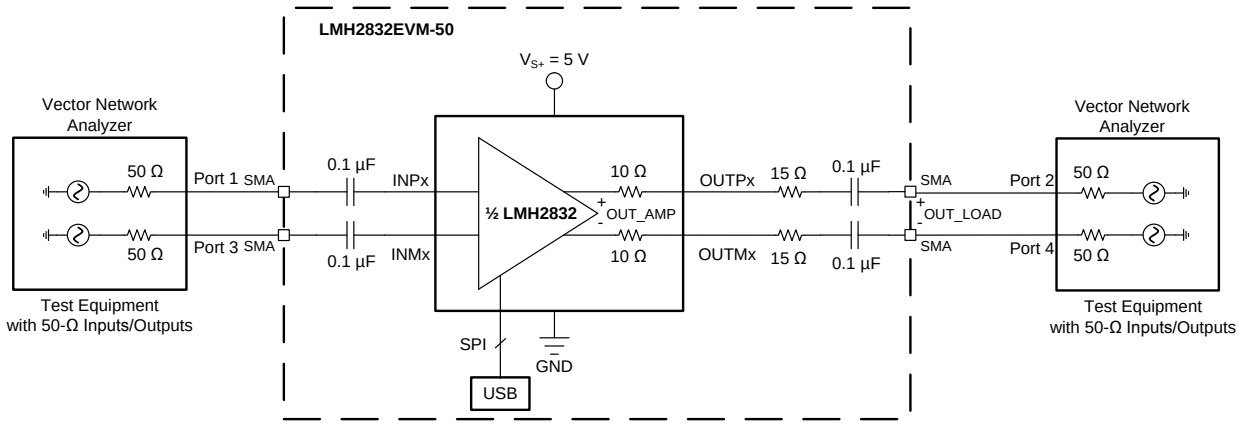

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Figure 41. Frequency Response Differential Test Setup

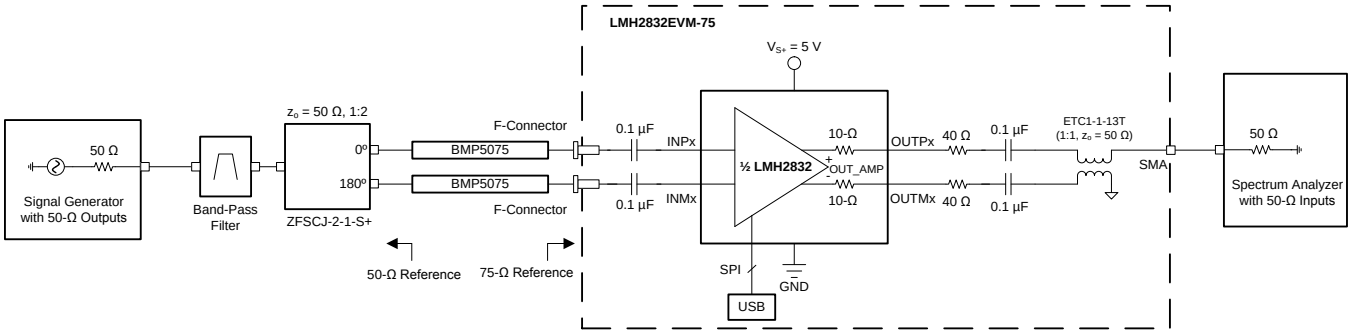

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Figure 42. Single-Tone Harmonic Distortion Test Setup

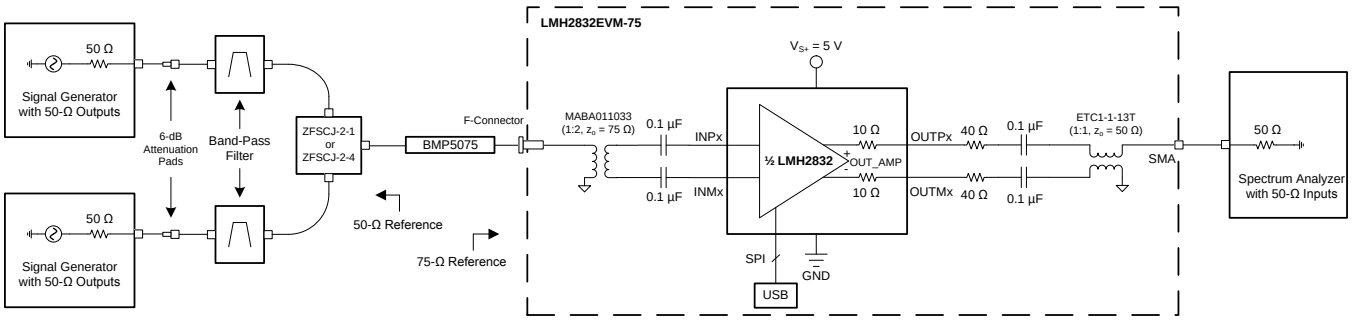

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Figure 43. Two-Tone Linearity Test Setup (OIP3, OIP2)

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Setup Diagrams (continued)

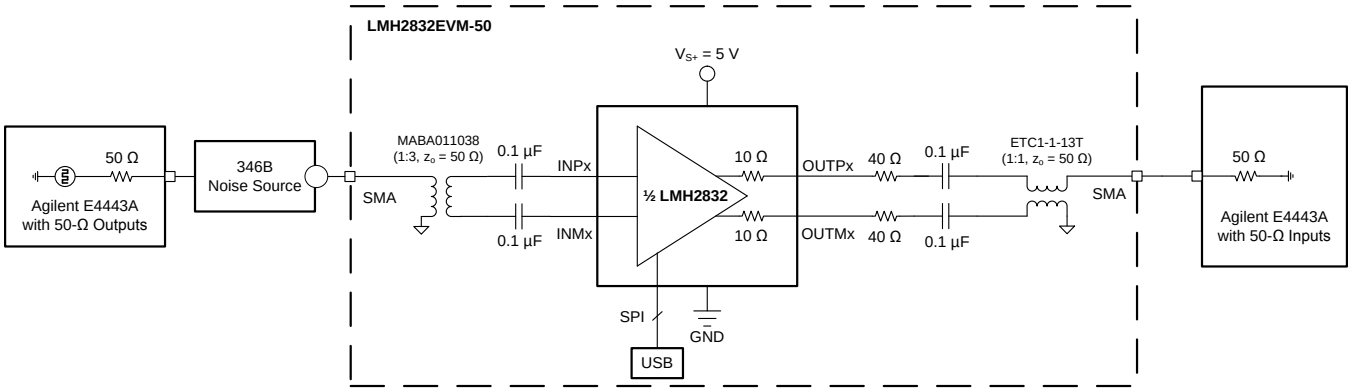

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Figure 44. Noise Figure Test Setup

8.2 ATE Testing and DC Measurements

All production testing and dc parameters are measured on automated test equipment (ATE) capable of dc measurements only. Some measurements (such as voltage gain) are referenced to the output of the internal amplifier and do not include losses attributed to the on-chip output resistors. The *Electrical Characteristics* values specify these conditions. When the measurement is referred to the amplifier output, the output resistors are not included in the measurement. If the measurement is referred to the device pins, then the output resistor loss is included in the measurement.

8.3 Frequency Response

This test is done by running an S-parameter sweep on a 4-port differential network analyzer using the standard EVM with no baluns; see Figure 41. The inputs and outputs of the EVM are connected to the network analyzer using 75-Ω coaxial cables with the input ports set to a characteristic impedance of 75 Ω, and the output ports set to a characteristic impedance of 50 Ω.

The frequency response test with capacitive load is done by soldering the capacitor across the LMH2832 output pins. In this configuration, the on-chip, 10-Ω resistors on each output leg isolate the capacitive load from the amplifier output pins.

8.4 Distortion

The standard EVM is used for measuring both the single-tone harmonic distortion and two-tone intermodulation distortion; see Figure 42 and Figure 43, respectively. The distortion is measured with differential input signals to the LMH2832. In order to interface with 50-Ω, single-ended test equipment, 50-Ω to 75-Ω impedance matching pads followed by external baluns (1:2, z_o = 75 Ω) are required between the EVM output ports and the test equipment. These baluns are used to combine two single tones in the two-tone test plots as well as to convert the single-ended input to differential output for harmonic distortion tests. The use of 6-dB attenuator pads on both the inputs and outputs is recommended to provide a balanced match between the external balun and the EVM.

8.5 Noise Figure

This test is done by matching the input of the LMH2832 to a 50-Ω noise source using a 50-Ω to 75-Ω impedance transformation pad followed by a 1:2 balun (Figure 44), with the noise figure being referred to the input impedance (R_S = 150 Ω). As noted in Figure 44, a Keysight Technologies™ E4443A with NF features is used for the testing.

8.6 Pulse Response, Slew Rate, and Overdrive Recovery

For time-domain measurements, the standard EVM is driven through an impedance transformation pad and a balun again to convert a single-ended output from the test equipment to the differential inputs of the LMH2832. The differential outputs are directly connected to the oscilloscope inputs, with the differential signal response calculated using trace math from the two separate oscilloscope inputs.

8.7 Power-Down

The standard EVM is used for this test by completely removing the shorting block on jumper JPD. A high-speed, 50-Ω pulse generator is used to drive the PDx pin that toggles the output signal on or off depending upon the PDx pin voltage.

8.8 Crosstalk, Gain Matching, and Phase Matching

The standard EVM is used for these tests with both channels enabled. For gain and phase matching, the responses of both channels are measured on a network analyzer and the gain and phase values are compared. For crosstalk, a single channel is driven with a signal on the network analyzer when the other channel is measured.

8.9 Output Measurement Reference Points

The LMH2832 has two on-chip, 10-Ω output resistors on each channel. When matching the output to a 100-Ω load, the evaluation module (EVM) uses an external 40-Ω resistor on each output leg to complete the output matching. The inclusion of on-chip output resistors creates two potential reference points for measuring the output voltage. The first reference point is at the internal amplifier output (OUT_AMP), and the second reference point is at the externally-matched 100-Ω load (OUT_LOAD). The measurements in the *Electrical Characteristics* table and in the *Typical Characteristics* section are referred to the (OUT_AMP) reference point unless otherwise specified. The conversion between reference points is a straightforward correction of 3 dB for power and 6 dB for voltage, as shown in Equation 1 and Equation 2. The measurements are referenced to OUT_AMP when not specified.

$$\text{VOUT_LOAD} = (\text{VOUT_AMP} - 6\ \text{dB}) \quad (1)$$

$$\text{POUT_LOAD} = (\text{POUT_AMP} - 3\ \text{dB}) \quad (2)$$

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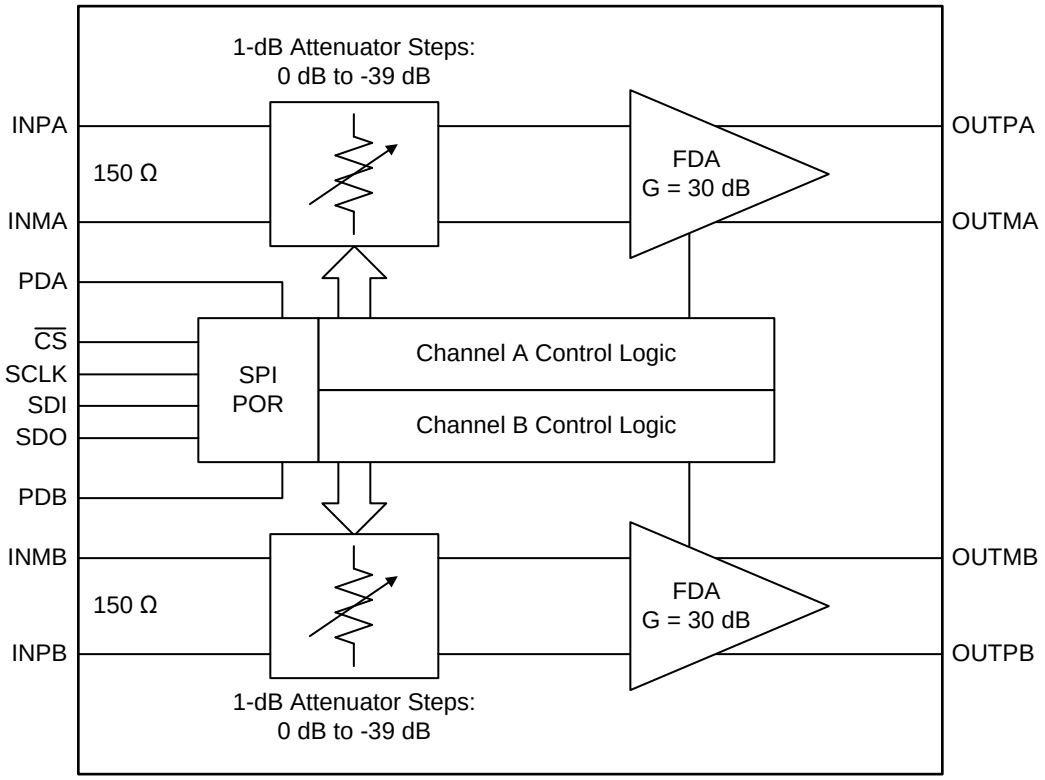
9 Detailed Description

9.1 Overview

Each channel of the LMH2832 consists of an input attenuator block followed by a fully differential amplifier that has a gain of 30 dB. The attenuator has a range of 0 dB to –39 dB in 1-dB steps that is controlled by an SPI interface. The two channels can be controlled independently using the digital interface including power-down and bias settings. A separate analog power-down pin (PDA, PDB) is also included for each channel so that the device can bet set to a low-power state without waiting for a serial write to a register. The internal registers also include a power-on-reset (POR) that ensures the device starts in a known state after the power is reset.

9.2 Functional Block Diagram



9.3 Feature Description

9.3.1 Analog Input Characteristics

The LMH2832 is a dual-channel device with two identical channels (A and B) that each have differential input pins (INP and INM) that denote the positive and negative inputs, respectively. The inputs are expected to be ac-coupled only, typically through a transformer or capacitor. The amplifier self-biases the input common-mode to mid-supply for the maximum input voltage range. The inputs of the LMH2832 can only be driven differentially. For single-ended input source applications, use a balun or fully differential amplifier (such as the LMH3401 or LMH5401) that can convert single-ended to differential signals before the LMH2832.

Feature Description (continued)

At maximum gain, the digital attenuator is set to 0 dB of attenuation, causing the input signal to be much larger than the output signal and forcing the maximum output voltage swing to be limited by the outputs of the device. However at minimum gain, the maximum voltage swing is limited by the inputs of the device because the attenuator causes the output voltage to be 9 dB lower than the input voltage. In minimum gain, the input voltage limits against the electrostatic discharge (ESD) devices before the output reaches the maximum swing limits. For linear operation, the input voltage must be kept within the maximum input voltage ratings described in the *Electrical Characteristics* table.

The input impedance of the LMH2832 is set by internal termination resistors to a nominal value of 150 Ω, differential. Process variations result in a range of values, as described in the *Electrical Characteristics* table. The input impedance is also affected by device parasitic effects at higher frequencies that cause the impedance to shift away from the nominal value.

9.3.2 Analog Output Characteristics

The LMH2832 has series, 10-Ω, on-chip resistors on each output to provide isolation from board parasitics that can cause instability. When designing a filter following the LMH2832, the filter source impedance calculation must include the two 10-Ω, on-chip resistors. Table 2 shows the calculated external source impedance values required for various matched filter loads.

Table 2. Output Resistor Values for Matched Loads

MATCHED FILTER IMPEDANCE (Ω)	EXTERNAL SERIES RESISTOR PER OUTPUT (Ω)
100	80
150	130
200	180
300	280

9.3.3 Driving Low Insertion-Loss Filters

When driving high-speed ADCs, a filter is commonly driven with a matched impedance to the ADC. This impedance is matched by the amplifier by setting the combination of the output resistors to the same impedance as the ADC inputs. Impedance matching is often done to minimize any transmission reflections caused by the physical signal path. The drawback to using a matched impedance is that a voltage swing is required from the amplifier outputs that is twice the desired ADC input voltage swing, which can cause output voltage limitation issues.

To avoid using a matched impedance, a low insertion loss filter can be driven where there is little to no resistance added at the amplifier outputs. The amplifier outputs then only must swing to the value of the ADC full-scale input voltage, thus eliminating most of the potential amplifier output headroom issues. The requirements of this technique are that the amplifier must be able to provide enough current to the load of the ADC and that the path between the amplifier outputs and ADC inputs must be minimized to prevent any reflections.

9.3.4 Input Impedance Matching

The LMH2832 has a differential input impedance of 150 Ω that can be easily matched to single-ended, 50-Ω or 75-Ω systems using baluns. For a single-ended, 50-Ω input, a 1:3-Ω ratio balun can be used to create a 150-Ω differential source impedance to the device with a balun gain of 4.8 dB. For a single-ended, 75-Ω input, a 1:2-Ω ratio balun creates a 150-Ω differential source impedance to the device with a voltage gain of 3 dB.

9.3.5 Power-On Reset (POR)

The LMH2832 has a built-in, power-on-reset (POR) that sets the device registers to their default state (see the *Register Maps* section) on power-up. Note that the LMH2832 register information is lost when power is removed. When power is reapplied, the POR ensures that the device enters a default state. Power glitches (of sufficient duration) can also initiate the POR and return the device to a default state.

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9.4 Device Functional Modes

9.4.1 Power-Down (PD)

The device supports power-down control using an external power-down (PDx) pin or by writing a logic high to bit 6 of SPI register 2h (see the *Register Maps* section). The external PDx pins are active high; when left floating, the device defaults to an on condition resulting from the internal pulldown resistors that cause a logic low on the PDx pins. The device PDx thresholds are noted in the *Electrical Characteristics* table. The device consumes approximately 7 mA in power-down mode. Note that the SPI register contents are preserved in power-down mode.

9.4.2 Gain Control

The LMH2832 gain can be controlled from 30-dB gain (0-dB attenuation) to –9-dB gain in 1-dB steps by digitally programming the SPI register 2h; see the *Register Maps* section for more details.

9.5 Programming

9.5.1 Details of the Serial Interface

The LMH2832 has a set of internal registers that can be accessed by the serial interface formed by the $\overline{CS}$ (serial interface enable), SCLK (serial interface clock), SDI (serial interface input data), and SDO (serial interface read-back data) pins. Serially shifting bits into the device is enabled when $\overline{CS}$ is low. SDI serial data are latched at every SCLK rising edge when $\overline{CS}$ is active (low). The serial data are loaded into the register at every 16th SCLK rising edge when $\overline{CS}$ is low. When the word length exceeds a multiple of 16 bits, the excess bits are ignored. Data can be loaded in multiples of 16-bit words within a single active $\overline{CS}$ pulse. The first eight bits form the register address and the remaining eight bits are the register data. The interface can function with SCLK frequencies from 25 MHz down to very low speeds (of a few hertz) and also with a non-50% SCLK duty cycle. A summary of the LMH2832 SPI protocol is:

1. SPI-1.1 interface
2. Independent channel A, B attenuation programming (6-bit gain control)
3. SPI register contents are preserved in power-down mode
4. SPI-controlled power modes (3-bit control for eight options to step down the power)
5. Powered for the main 5-V power supply
6. 1.8-V logic

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Programming (continued)

9.5.2 Timing Diagrams

Figure 45 and Figure 46 show timing diagrams for the SPI write and read bus cycles, respectively. Figure 47 shows an example timing diagram for a streaming write cycle and Figure 48 shows an example timing diagram for a streaming read cycle. Figure 49, Figure 50, Figure 51, and Figure 52 illustrate timing diagrams and requirements for the clock, data input, data output, and chip select, respectively. See the *Timing Requirements: SPI* table for SPI timing requirements.

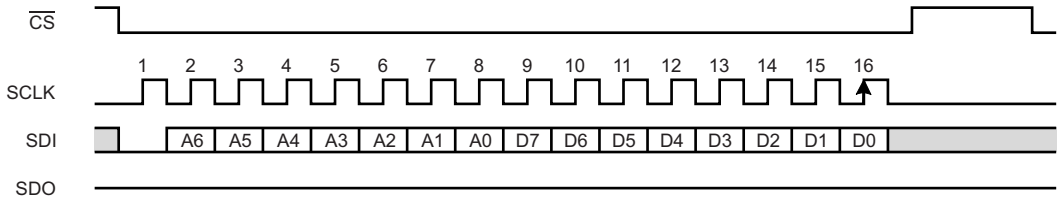

Figure 45. SPI Write Bus Cycle Timing Diagram

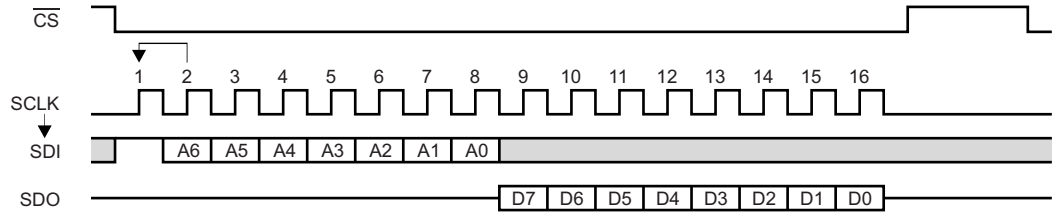

Figure 46. SPI Read Bus Cycle Timing Diagram

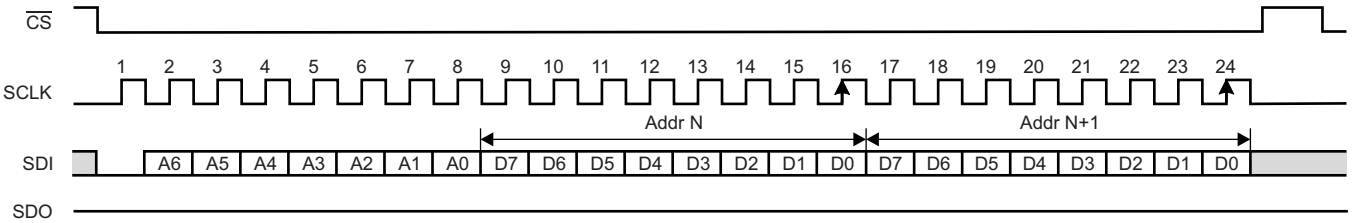

Figure 47. SPI Streaming Write Example Timing Diagram

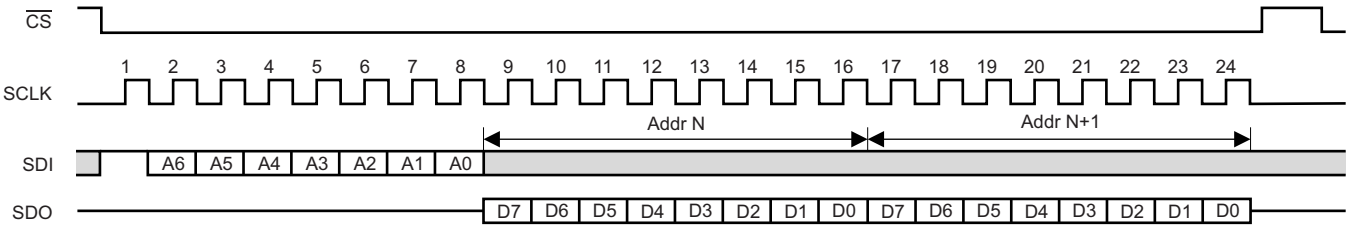

Figure 48. SPI Streaming Read Example Timing Diagram

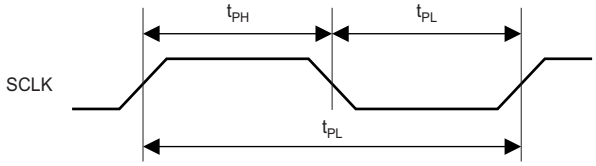

Figure 49. SPI Clock Timing Diagram

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Programming (continued)

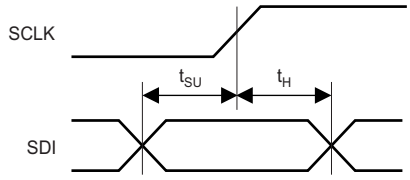

Figure 50. SPI Data Input Timing Diagram

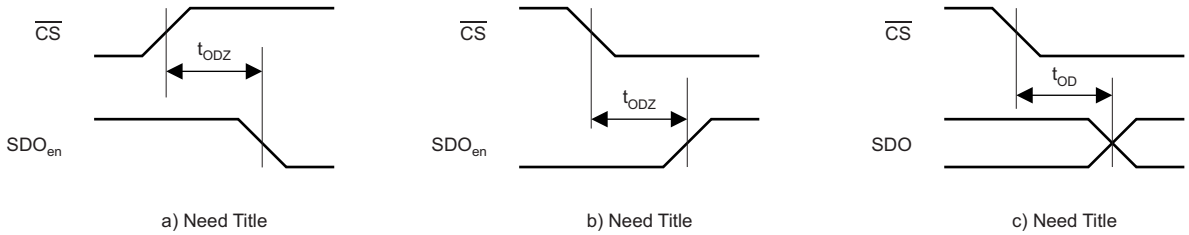

Figure 51. SPI Data Output Timing Diagrams

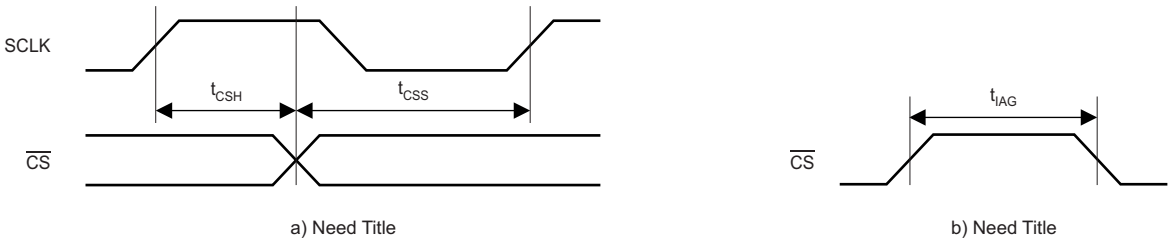

Figure 52. SPI Chip Select Timing Diagrams

9.6 Register Maps

Table 3 shows the SPI registers for the LMH2832.

Table 3. SPI Register Map

ADDRESS (A[6:0])	R/W	DEFAULT (Hex)	REGISTER NAME	REGISTER DATA							
				7	6	5	4	3	2	1	0
0	R	B3	Revision ID	1	0	1	1	0	0	1	1
1	R	23	Product ID	0	0	1	0	0	0	1	1
2	R/W	00	SW reset	Reserved			Reset B	Reserved			Reset A
3	R/W	00	Power-down	Reserved			PD B	Reserved			PD A
4	R/W	20	Channel A RW0, bias control	Channel A RW0							
5	R/W	14	Channel A RW1, attenuator control	Channel A RW1							
6	R/W	20	Channel B RW0, bias control	Channel B RW0							
7	R/W	14	Channel B RW1, attenuator control	Channel B RW1							
8-127	R	00	Reserved	0	0	0	0	0	0	0	0

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9.6.1 Register Descriptions

Exercising the SW reset function returns all registers to the default values of the respective channel.

9.6.1.1 SW Reset Register (address = 2)

Figure 53. SW Reset Register

7	6	5	4	3	2	1	0
Reserved			Reset B	Reserved			Reset A
R-0h			R/W-0h	R-0h			R/W-0h

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 4. SW Reset Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	Reserved	R	0h	Reserved.
4	Reset B	R/W	0h	This bit is a self-clearing bit. 0 = No action 1 = Reset
3-1	Reserved	R	0h	Reserved.
0	Reset A	R/W	0h	This bit is a self-clearing bit. 0 = No action 1 = Reset

9.6.2 Power-Down Control Register (address = 3)

Figure 54. Power-Down Control Register

7	6	5	4	3	2	1	0
Reserved			PD B	Reserved			PD A
R-0h			R/W-0h	R-0h			R/W-0h

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 5. Power-Down Control Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	Reserved	R	0h	Reserved.
4	PD B	R/W	0h	0 = Active 1 = PD
3-1	Reserved	R	0h	Reserved.
0	PD A	R/W	0h	0 = Active 1 = PD

9.6.3 Channel A RW0 Register (address = 4)

Figure 55. Channel A RW0 Register

7	6	5	4	3	2	1	0
Channel A RW0							
R/W-0h							

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 6. Channel A RW0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	Channel A RW0	R/W	0h	These bits drive the output CHA_RW0[7:0] and are reset by a device reset or Reset A. Table 10 lists controls for this register.

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9.6.4 Channel A RW1 Register (address = 5)

Figure 56. Channel A RW1 Register

7	6	5	4	3	2	1	0
Channel A RW1							
R/W-0h							

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 7. Channel A RW1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	Channel A RW1	R/W	0h	These bits drive the output CHA_RW1[7:0] and are reset by a device reset or Reset A. Table 11 lists controls for this register.

9.6.5 Channel B RW0 Register (address = 6)

Figure 57. Channel B RW0 Register

7	6	5	4	3	2	1	0
Channel B RW0							
R/W-0h							

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 8. Channel B RW0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	Channel B RW0	R/W	0h	These bits drive the output CHB_RW0[7:0] and are reset by a device reset or Reset B. Table 10 lists controls for this register.

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9.6.6 Channel B RW1 Register (address = 7)

Figure 58. Channel B RW1 Register

7	6	5	4	3	2	1	0
Channel B RW1							
R/W-0h							

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 9. Channel B RW1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	Channel B RW1	R/W	0h	These bits drive the output CHB_RW1[7:0] and are reset by a device reset or Reset B. Table 11 lists controls for this register.

Table 10. Bias Control Register Bit Settings (Channels A, B)(1)

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	1
0	0	0	0	0	0	1	X
0	0	0	0	0	1	X	X
0	0	0	0	1	X	X	X
0	0	0	1	X	X	X	X
0	0	1	X	X	X	X	X
0	1	X	X	X	X	X	X
1	X	X	X	X	X	X	X

(1) Default value: 001xxxxx. Highest power: 1xxxxxxx. Lower power: 00000000.

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Table 11. Attenuator Control Register Bit Settings (Channels A, B)[(1)]

7	6	5	4	3	2	1	0
Reserved, always read 0		0	0	0	0	0	0
Reserved, always read 0		0	0	0	0	0	1
Reserved, always read 0		0	0	0	0	1	0
Reserved, always read 0		0	0	0	0	1	1
Reserved, always read 0		0	0	0	1	0	0
Reserved, always read 0		0	0	0	1	0	1
Reserved, always read 0		0	0	0	1	1	0
Reserved, always read 0		0	0	0	1	1	1
Reserved, always read 0		0	0	1	0	0	0
Reserved, always read 0		0	0	1	0	0	1
Reserved, always read 0		0	0	1	0	1	0
Reserved, always read 0		0	0	1	0	1	1
Reserved, always read 0		0	0	1	1	0	0
Reserved, always read 0		0	0	1	1	0	1
Reserved, always read 0		0	0	1	1	1	0
Reserved, always read 0		0	0	1	1	1	1
Reserved, always read 0		0	1	0	0	0	0
Reserved, always read 0		0	1	0	0	0	1
Reserved, always read 0		0	1	0	0	1	0
Reserved, always read 0		0	1	0	0	1	1
Reserved, always read 0		0	1	0	1	0	0
Reserved, always read 0		0	1	0	1	0	1
Reserved, always read 0		0	1	0	1	1	0
Reserved, always read 0		0	1	0	1	1	1
Reserved, always read 0		0	1	1	0	0	0
Reserved, always read 0		0	1	1	0	0	1
Reserved, always read 0		0	1	1	0	1	0
Reserved, always read 0		0	1	1	0	1	1
Reserved, always read 0		0	1	1	1	0	0
Reserved, always read 0		0	1	1	1	0	1
Reserved, always read 0		0	1	1	1	1	0
Reserved, always read 0		0	1	1	1	1	1
Reserved, always read 0		1	0	0	0	0	0
Reserved, always read 0		1	0	0	0	0	1
Reserved, always read 0		1	0	0	0	1	0
Reserved, always read 0		1	0	0	0	1	1
Reserved, always read 0		1	0	0	1	0	0
Reserved, always read 0		1	0	0	1	0	1
Reserved, always read 0		1	0	0	1	1	0
Reserved, always read 0		1	0	0	1	1	1

(1) Default attenuation setting: xx001011. Maximum attenuation (lowest gain setting): xx100111. Minimum attenuation (highest gain setting): xx000000.

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10 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

The LMH2832 is designed as a general-purpose, analog-to-digital converter (ADC) driver that also meets the performance requirements for DOCSIS 3.X upstream CMTS solutions. This section describes various requirements and considerations for using the LMH2832 and also some design examples.

10.1.1 Driving ADCs

When the amplifier is driving an ADC, the key points to consider for implementation are the signal-to-noise ratio (SNR), spurious-free dynamic range (SFDR), and ADC input considerations, as described in this section.

A typical application of the LMH2832 involves driving a wideband, 14-bit ADC (such as the ADS54J40), as shown in Figure 59. The LMH2832 can drive the full Nyquist bandwidth of ADCs with sampling rates up to 900 MSPS. If the front-end bandwidth of the ADC is more than 450 MHz, then use a simple noise filter to improve SNR. Otherwise, the ADC can be connected directly to the amplifier output pins with appropriate matching resistors to limit the full-scale input of the ADC. Note that the LMH2832 inputs must be driven differentially using a balun or fully differential amplifiers (FDAs). For dc-coupled applications, an FDA (such as the LMH3401 or LMH5401) that can convert a single-ended input to a differential output with low distortion is preferred.

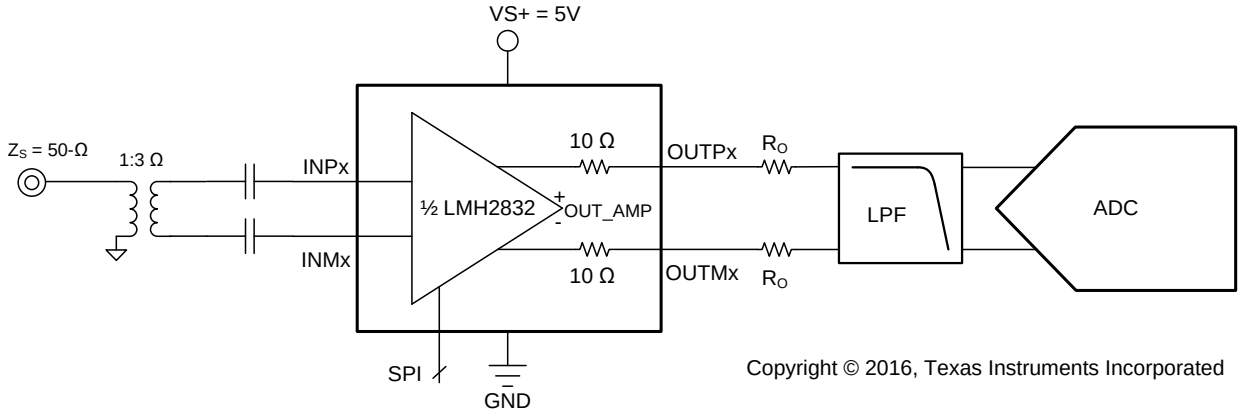

Figure 59. ADC Driver with a 50-Ω Source

Application Information (continued)

10.1.1.1 SNR Considerations

When using the LMH2832 with a filter, the signal-to-noise ratio (SNR) of the amplifier and filter can be calculated from the amplitude of the signal and the bandwidth of the filter. The noise from the amplifier is band-limited by the filter with the equivalent brick-wall filter bandwidth. The amplifier and filter noise can be calculated using Equation 3:

$$SNR_{AMP+FILTER} = 10 \cdot \log\left(\frac{V^2_O}{e^2_{FILTEROUT}}\right) = 20 \cdot \log\left(\frac{V_O}{e_{FILTEROUT}}\right)$$

where:

- $e_{FILTEROUT} = e_{NAMPOUT} \cdot \sqrt{ENB}$
- $e_{NAMPOUT}$ = the output noise density of the LMH2832 (50.4 nV/$\sqrt{Hz}$) at A_V = 30 dB
- ENB = the brick-wall equivalent noise bandwidth of the filter
- V_O = the amplifier output signal (3)

For example, with a first-order (N = 1) band-pass or low-pass filter with a 1000-MHz cutoff, ENB is 1.57 • f_{-3dB} = 1.57 • 1000 MHz = 1570 MHz. For second-order (N = 2) filters, ENB is 1.22 • f_{-3dB}. When the filter order increases, ENB approaches f_{-3dB} (N = 3 → ENB = 1.15 • f_{-3dB}; N = 4 → ENB = 1.13 • f_{-3dB}). Both V_O and $e_{FILTEROUT}$ are in RMS voltages. For example, with a 2-V_{PP} (0.707 V_{RMS}) output signal and a 300-MHz, first-order, low-pass filter, the SNR of the amplifier and filter is 56 dB with $e_{FILTEROUT}$ = 50.4 nV/$\sqrt{Hz}$ • $\sqrt{471\ MHz}$ = 1.09 mV_{RMS}.

The SNR of the amplifier, filter, and ADC sum in RMS fashion, as shown in Equation 4 (SNR values in dB):

$$SNR_{SYSTEM} = -20 \cdot \log\left(\sqrt{10^{\frac{-SNR_{AMP+FILTER}}{10}} + 10^{\frac{-SNR_{ADC}}{10}}}\right) \quad (4)$$

This formula shows that if the SNR of the amplifier and filter equals the SNR of the ADC, then the combined SNR is 3 dB lower (worse). Thus, for minimal degradation (< 1 dB) on the ADC SNR, the SNR of the amplifier and filter must be 10 dB greater than the ADC SNR. The combined SNR calculated in this manner is usually accurate to within ±1 dB of the actual implementation.

10.1.1.2 SFDR Considerations

The SFDR of the amplifier is usually set by the second- or third-order harmonic distortion for single-tone inputs, and by the second-order or third-order intermodulation distortion for two-tone inputs. Harmonics and second-order intermodulation distortion can be filtered to some degree, but third-order intermodulation spurs cannot be filtered. The ADC generates the same distortion products as the amplifier, but also generates additional spurs (not harmonically related to the input signal) as a result of sampling and clock feed through.

When the spurs from the amplifier and filter are known, each individual spur can be directly added to the same spur from the ADC, as shown in Equation 5, to estimate the combined spur (spur amplitudes in dBc):

$$HDx_{SYSTEM} = -20 \cdot \log\left(10^{\frac{-HDx_{AMP+FILTER}}{20}} + 10^{\frac{-HDx_{ADC}}{20}}\right) \quad (5)$$

This calculation assumes that the spurs are in phase, but usually provides a good estimate of the final combined distortion.

For example, if the spur of the amplifier and filter equals the spur of the ADC, then the combined spur is 6 dB higher. To minimize the amplifier contribution (< 1 dB) to the overall system distortion, the spur from the amplifier and filter must be approximately 15 dB lower in amplitude than that of the converter. The combined spur calculated in this manner is usually accurate to within ±6 dB of the actual implementation; however, higher variations can be detected as a result of phase shift in the filter, especially in second-order harmonic performance.

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Application Information (continued)

This worst-case spur calculation assumes that the amplifier and filter spur of interest is in phase with the corresponding spur in the ADC, such that the two spur amplitudes can be added linearly. There are two phase-shift mechanisms that cause the measured distortion performance of the amplifier-ADC chain to deviate from the expected performance calculated using Equation 5; one mechanism is the common-mode phase shift and the other is the differential phase shift.

Common-mode phase shift is the phase shift detected equally in both branches of the differential signal path including the filter. Common-mode phase shift nullifies the basic assumption that the amplifier, filter, and ADC spur sources are in phase. This phase shift can lead to better performance than predicted when the spurs become phase shifted, and there is the potential for cancellation when the phase shift reaches 180°. However, there is a significant challenge in designing an amplifier-ADC interface circuit to take advantage of a common-mode phase shift for cancellation: the phase characteristics of the ADC spur sources are unknown, thus the necessary phase shift in the filter and signal path for cancellation is also unknown.

Differential phase shift is the difference in the phase response between the two branches of the differential filter signal path. Differential phase shift in the filter is a result of mismatched components caused by nominal tolerances and can severely degrade the even harmonic distortion of the amplifier-ADC chain. This effect has the same result as mismatched path lengths for the two differential traces, and causes more phase shift in one path than the other. Ideally, the phase responses over frequency through the two sides of a differential signal path are identical, such that even harmonics remain optimally out of phase and cancel when the signal is taken differentially. However, if one side has more phase shift than the other, then the even harmonic cancellation is not as effective.

Single-order, resistor-capacitor (RC) filters cause very little differential phase shift with nominal tolerances of 5% or less, but higher-order, inductor-capacitor (LC) filters are very sensitive to component mismatch. For instance, a third-order Butterworth band-pass filter with a 100-MHz center frequency and a 20-MHz bandwidth displays as much as 20° of differential phase imbalance in a SPICE Monte Carlo analysis with 2% component tolerances. Therefore, although a prototype may work, production variance is unacceptable. For ac-coupled or dc-coupled applications where a transformer or balun cannot be used, using first- or second-order filters is recommended to minimize the effect of differential phase shift.

10.1.1.3 ADC Input Common-Mode Voltage Considerations (AC-Coupled Input)

When interfacing to an ADC, the input common-mode voltage range of the ADC must be taken into account for proper operation. In an ac-coupled application between the amplifier and the ADC, the input common-mode voltage bias of the ADC can be accomplished in different ways. Some ADCs use internal bias networks such that the analog inputs are automatically biased to the required input common-mode voltage if the inputs are ac-coupled with capacitors (or if the filter between the amplifier and ADC is a band-pass filter). Other ADCs supply the required input common-mode voltage from a reference voltage output pin (often termed CM or V_{CM}). With these ADCs, the ac-coupled input signal can be re-biased to the input common-mode voltage by connecting resistors from each input to the CM output of the ADC, as shown in Figure 60. AC coupling provides dc common-mode isolation between the amplifier and the ADC; thus, the output common-mode voltage of the amplifier is a *don't care* for the ADC.

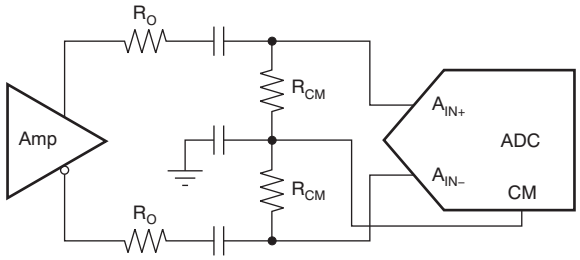

Figure 60. Biasing AC-Coupled ADC Inputs Using the ADC CM Output

Application Information (continued)

10.1.1.4 ADC Input Common-Mode Voltage Considerations (DC-Coupled Input)

The LMH2832 is designed to primarily be used in ac-coupled applications only. However, the LMH2832 can be dc-coupled if certain strict conditions are met. The LMH2832 has an internal common-mode bias equal to the mid-supply voltage, so any dc coupling on the input or output must have a common-mode voltage that is also set to mid-supply. To dc couple to an ADC input, the mid-supply voltage of the LMH2832 must be centered around the ADC input common-mode. This common-mode matching can be accomplished by shifting the supplies to center the mid-supply voltage around the ADC input common-mode voltage. However, shifting the supplies also changes the ground reference for the digital inputs, which then likely requires a voltage-shifted interface as well. The LMH2832 is not recommended to be operated as dc-coupled unless absolutely necessary.

10.2 Typical Applications

10.2.1 DOCSIS 3.X Driver

The LMH2832 is designed to perform best when driving differential input ADCs in high-speed applications. Figure 61 shows an example diagram of the LMH2832 driving an ADC with a fifth-order, low-pass filter for a 75-Ω impedance, data over cable service interface specification (DOCSIS) 3.X upstream receiver return path application. The primary interface between the amplifier and the ADC is usually an antialiasing filter to suppress high-frequency harmonics that otherwise alias back into the ADC FFT spectrum. Filters range from single-order real RC poles to higher-order, resistor-inductor-capacitor (RLC) filters, depending on the application requirements. Series output resistors (R_O) help isolate the amplifier from any capacitive load presented by the filter, and can also be used to create a matched impedance to drive transmission lines.

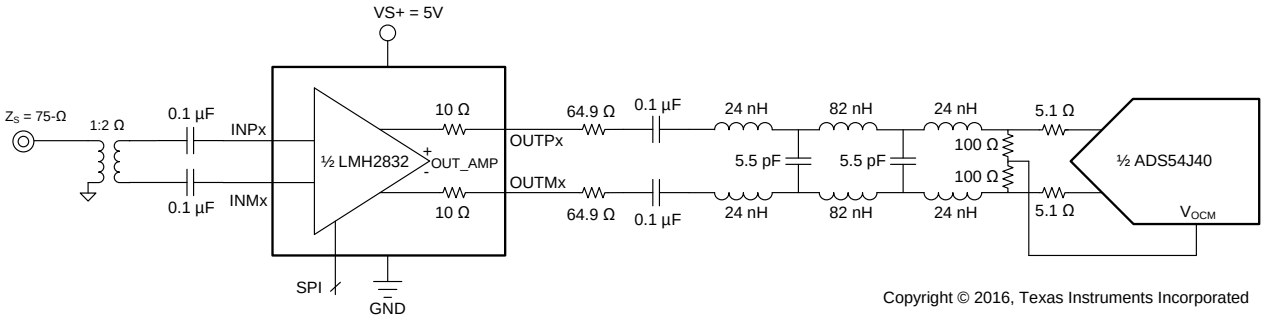

Figure 61. DOCSIS 3.X Driver with the ADS54J40 and a 300-MHz, 4th-Order, Butterworth, Low-Pass Filter

10.2.1.1 Design Requirements

Table 12 shows example design requirements for the LMH2832 in an upstream receiver application.

Table 12. Example Design Requirements

SPECIFICATION	DESIGN REQUIREMENTS
Supply voltage	4.75 to 5.25 V
Usable input frequency range	300 MHz
System voltage gain and range	33-dB voltage gain with 30-dB range
Source impedance	75 Ω, single-ended
Signal path SNR at 175 MHz (measured at ADC)	> 50 dBFS

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10.2.1.2 Detailed Design Procedure

To begin the design process, make sure that none of the following design parameters exceed the limits listed in the *Electrical Characteristics* table, such as:

- Supply voltage
- Temperature range
- Input voltage range across gain
- Output current requirements
- Digital I/O voltages and currents

10.2.1.2.1 Source Resistance Matching

Standard DOCSIS systems use a characteristic single-ended impedance of 75 Ω that must be properly matched to the 150-Ω differential impedance of the LMH2832. The circuit in Figure 61 uses a transformer with a 1:2-Ω ratio to convert the signal from single-ended to differential, and also to match the differential impedance. The transformer also adds a signal gain of approximately 3 dB to the system with some insertion loss depending on the chosen transformer.

10.2.1.2.2 Output Impedance Matching

For the circuit in Figure 61, the output impedance is matched to a 150-Ω characteristic impedance filter to maximize the performance of the LMH2832. On the amplifier output side, the output impedance is matched to 150 Ω by including a 65-Ω series resistor on each output. Combined with the internal 10-Ω resistors on each output, the total differential impedance becomes 150 Ω. The ADS54J40 has an input impedance of approximately 600 Ω that is reduced to 150 Ω by using two 5-Ω series input resistors in parallel with two 100-Ω series resistors. The 5-Ω series resistors are included to isolate the input capacitance of the ADC so that the response of the filter is not affected. With both the amplifier and ADC impedances matched, any transmission line effects of the connection are minimized.

If the ADC is physically located close enough to the amplifier, a matched impedance may not be needed; see *Driving Low Insertion-Loss Filters* section for more information on driving non-matched filters.

10.2.1.2.3 Voltage Headroom Considerations

Because of the series resistors included on both the amplifier outputs and ADC inputs, the amplifier must drive a voltage that is significantly higher than the ADC full-scale input. For the circuit in Figure 61, the ADS54J40 full-scale input voltage is 1.9 V_{PP}, so the required voltage at the amplifier output pins is 3.6 V_{PP}. This voltage is less than the specified output voltage of 5 V_{PP} for the LMH2832, thus system performance is not limited. If the required output voltage is higher than what the amplifier can support, then the matched resistance value can be reduced. However, this reduction can have performance implications because more current output is required from the amplifier.

The input voltage swing can be larger than the output voltage swing because the LMH2832 can operate as an attenuator. To maintain the full-scale voltage of the ADS54J40 input in this application, the amplifier cannot attenuate more than 1 dB from input to output; otherwise, the maximum input voltage swing is exceeded. If the amplifier must be operated with more attenuation, then the output voltage must be reduced.

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10.2.1.3 Application Curve

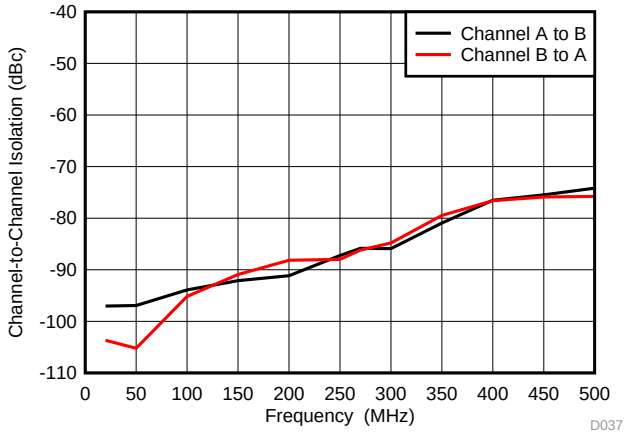

Figure 62. Amplifier Dual Channel Isolation Presented to ADC Interface

10.2.2 IQ Receiver

The LMH2832 is a dual-channel device; therefore, the device has excellent gain and phase matching between channels A and B. This matching makes the LMH2832 an excellent choice for systems that require two matched channels (such as an IQ demodulation receiver), as shown in Figure 63. For an IQ system, both the gain and phase must match for the real and imaginary channel. When using two single-channel amplifiers, the matching characteristics are subject to process lot and packaging variations for two individual devices, and there is often no way to make sure that the amplifiers match without testing each amplifier. However, the dual-channel architecture of the LMH2832 allows for much tighter gain and phase matching with minimal crosstalk effects. For more matching information, see the *Electrical Characteristics* table.

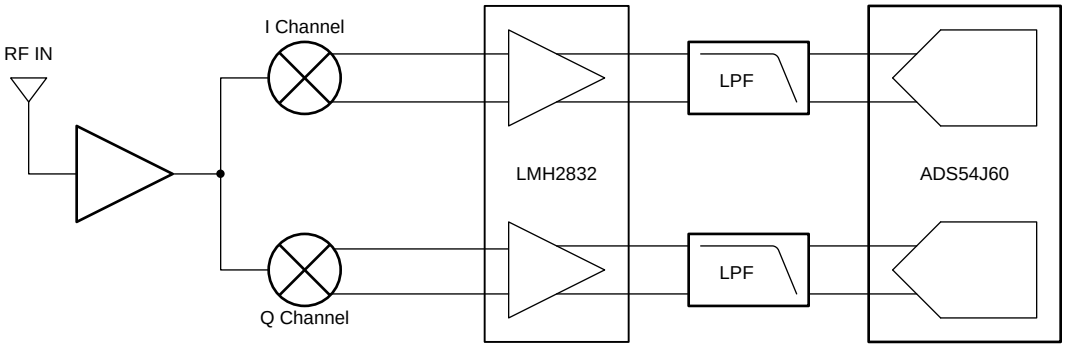

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Figure 63. IQ Receiver Block Diagram

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10.3 Do's and Don'ts

10.3.1 Do:

- Include a thermal analysis at the beginning of the project
- Use well-terminated transmission lines for all signals
- Maintain symmetrical input and output trace layouts
- Use solid metal layers for the power supplies
- Keep signal lines as straight as possible

10.3.2 Don't:

- Use a lower power-supply voltage than necessary
- Forget about the common-mode response of filters and transmission lines
- Rout digital line traces close to the analog signals and supply line traces

11 Power Supply Recommendations

The LMH2832 is designed to be used with a single supply with a range of 4.75 V to 5.25 V. The ideal supply voltage is a 5.0-V total single-ended supply. If the supply is reduced to the minimum voltage, then the maximum input and output voltage range is reduced by 0.25 V.

11.1 Split Supplies

Ideally, the LMH2832 uses a single-ended, 5-V supply, but the device can be operated on a split supply if necessary. However, the digital logic is referenced to the GND pins, meaning that the logic reference shifts with the GND supply if connected to a negative voltage and must be accounted for in the logic connections. In general, the LMH2832 is not suggested to be operated with a split-supply configuration.

11.2 Supply Decoupling

Power-supply decoupling is critical to high-frequency performance. Onboard bypass capacitors are used on the LMH2832EVM; however, the most important component of the supply bypassing is provided by the printed circuit board (PCB). As illustrated in Figure 64, there are multiple vias connecting the LMH2832 power planes to the power-supply traces. These vias connect the internal power planes to the LMH2832. Both V_{CC} and GND must be connected to the internal power planes with several square centimeters of continuous plane in the immediate vicinity of the amplifier. The capacitance between these power planes provides the bulk of the high-frequency bypassing for the LMH2832.

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12 Layout

12.1 Layout Guidelines

With a small bandwidth greater than 1 GHz, layout for the LMH2832 is critical and nothing can be neglected. In order to simplify board design, the LMH2832 has on-chip resistors that reduce the affect of off-chip capacitance. For this reason, make sure that the ground layer below the LMH2832 is not cut. The recommendation to not cut the ground plane under the amplifier input and output pins is different than many other high-speed amplifiers, but the reason is that parasitic inductance is more harmful to the LMH2832 performance than parasitic capacitance. By leaving the ground layer under the device intact, parasitic inductance of the output and power traces is minimized. The DUT portion of the evaluation board layout is shown in Figure 64.

The EVM uses long-edge capacitors for the decoupling capacitors, which reduces series resistance and increases the resonant frequency. Vias are also placed to the power planes before the bypass capacitors. Although not evident in the top layer, two vias are used at the capacitor in addition to the two vias underneath the device.

The output-matching resistors are 0402 size and are placed very close to the amplifier output pins, which reduces both parasitic inductance and capacitance. The use of 0603 output-matching resistors produces a measurable decrease in bandwidth.

When the signal is on a 50-Ω or 75-Ω controlled impedance transmission line, the layout then becomes much less critical. The transition from the 50-Ω or 75-Ω transmission line to the amplifier pins is the most critical area.

12.2 Layout Example

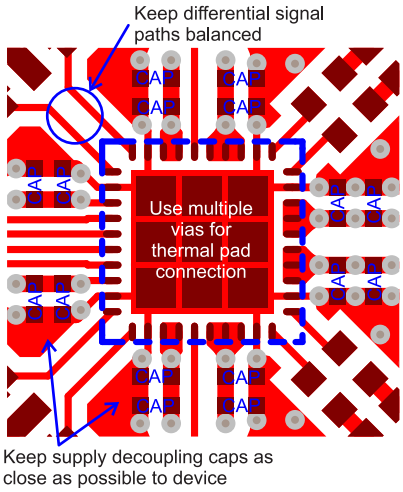

Figure 64. Layout Example

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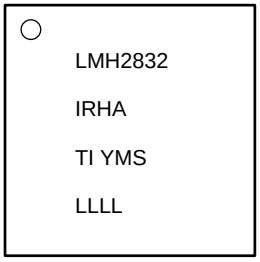
13 デバイスおよびドキュメントのサポート

13.1 デバイス・サポート

13.1.1 デバイスの項目表記



Legend:
○ = Pin 1 Designator
LMH2832 = Device Name
TI = Texas Instruments
YM = Year Month Date Code
S = Assembly Site Code
LLLL = Assembly Lot Code

図 65. デバイスのマーキング情報

13.2 ドキュメントのサポート

13.2.1 関連資料

関連資料については、以下を参照してください。

- *『ADS54J40 2チャネル、14ビット、1.0GSPS A/Dコンバータ』データシート*(SBAS714)
- *『LMH3401 7GHz、超広帯域、固定ゲイン、完全差動アンプ』データシート*(SBOS695)
- *『LMH5401 8GHz、低ノイズ、低消費電力、完全差動アンプ』データシート*(SBOS710)
- *『LMH6521 高パフォーマンス、2チャネルDVGA』データシート*(SNOSB47)
- *『LMH3404 2チャネル、7GHz、低ノイズ、低消費電力、完全差動アンプ』データシート*(SBOS739)
- *『LMH3402 2チャネル、ゲイン選択可能、7GHz、低ノイズ、低消費電力、完全差動アンプ』データシート*(SBOS744)
- *『LMH2832EVM-50評価モジュール』ユーザー・ガイド*(SLOU454)
- *『LMH2832EVM-75評価モジュール』ユーザー・ガイド*(SLOU438)
- 『LMH2832 TINA-TIリファレンス・デザイン』(SBOMA21)
- 『LMH2832 TINA-TI Spiceモデル』(SBOMA22)

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13.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LMH2832IRHAR	Active	Production	VQFN (RHA) | 40	2500 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	LMH2832 IRHA
LMH2832IRHAR.A	Active	Production	VQFN (RHA) | 40	2500 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	LMH2832 IRHA
LMH2832IRHARG4	Active	Production	VQFN (RHA) | 40	2500 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	LMH2832 IRHA
LMH2832IRHARG4.A	Active	Production	VQFN (RHA) | 40	2500 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	LMH2832 IRHA
LMH2832IRHAT	Active	Production	VQFN (RHA) | 40	250 | SMALL T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	LMH2832 IRHA
LMH2832IRHAT.A	Active	Production	VQFN (RHA) | 40	250 | SMALL T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	LMH2832 IRHA

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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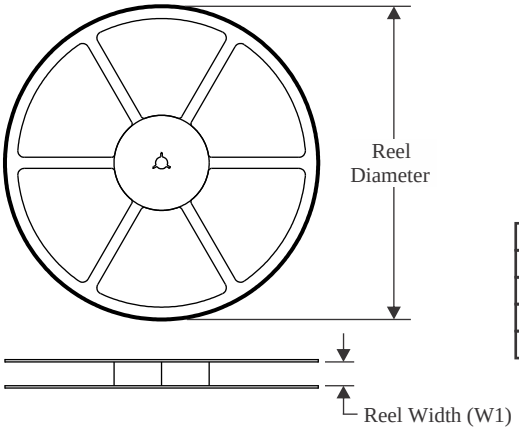
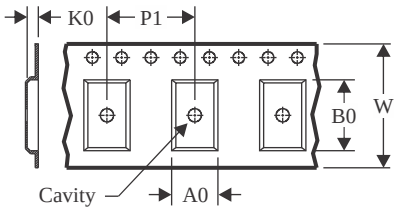
TAPE AND REEL INFORMATION

REEL DIMENSIONS

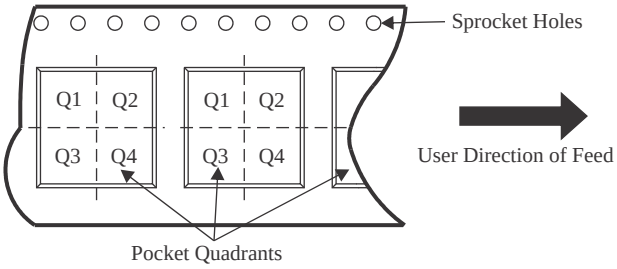


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

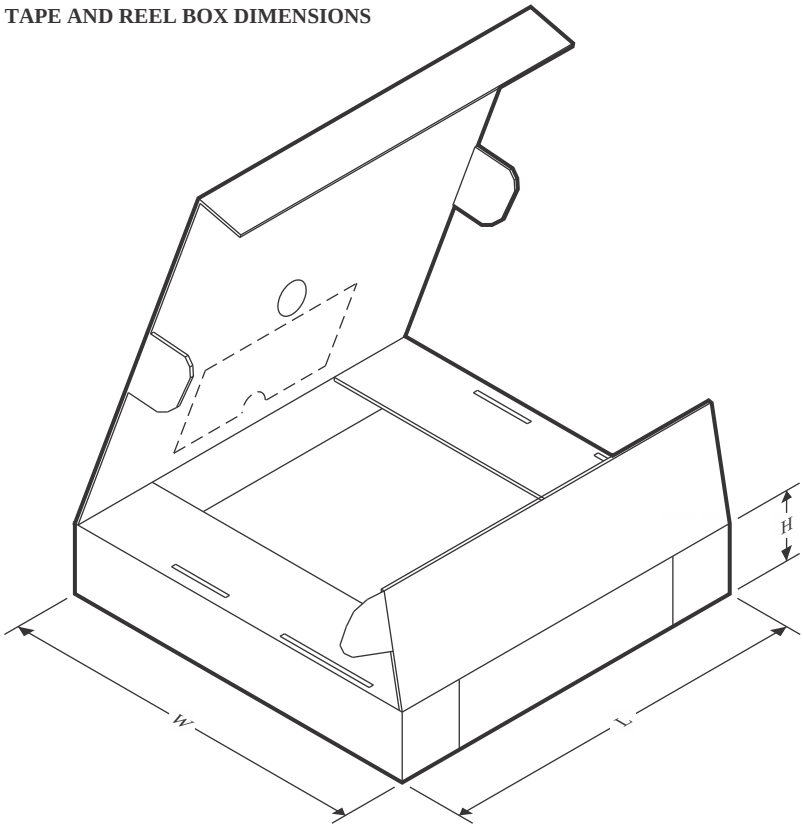
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMH2832IRHAR	VQFN	RHA	40	2500	330.0	16.4	6.3	6.3	1.1	12.0	16.0	Q2
LMH2832IRHARG4	VQFN	RHA	40	2500	330.0	16.4	6.3	6.3	1.1	12.0	16.0	Q2
LMH2832IRHAT	VQFN	RHA	40	250	180.0	16.4	6.3	6.3	1.1	12.0	16.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMH2832IRHAR	VQFN	RHA	40	2500	367.0	367.0	38.0
LMH2832IRHARG4	VQFN	RHA	40	2500	367.0	367.0	38.0
LMH2832IRHAT	VQFN	RHA	40	250	210.0	185.0	35.0

GENERIC PACKAGE VIEW

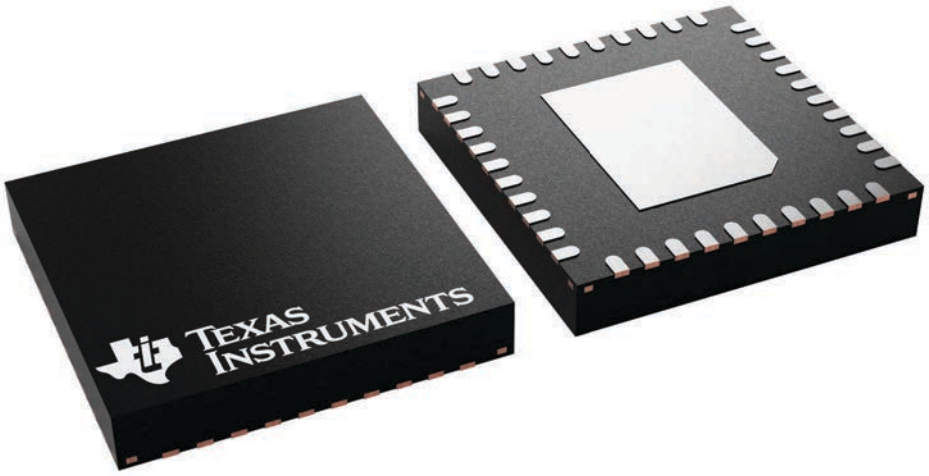
RHA 40

VQFN - 1 mm max height

6 x 6, 0.5 mm pitch

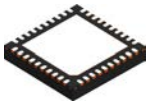
PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4225870/A

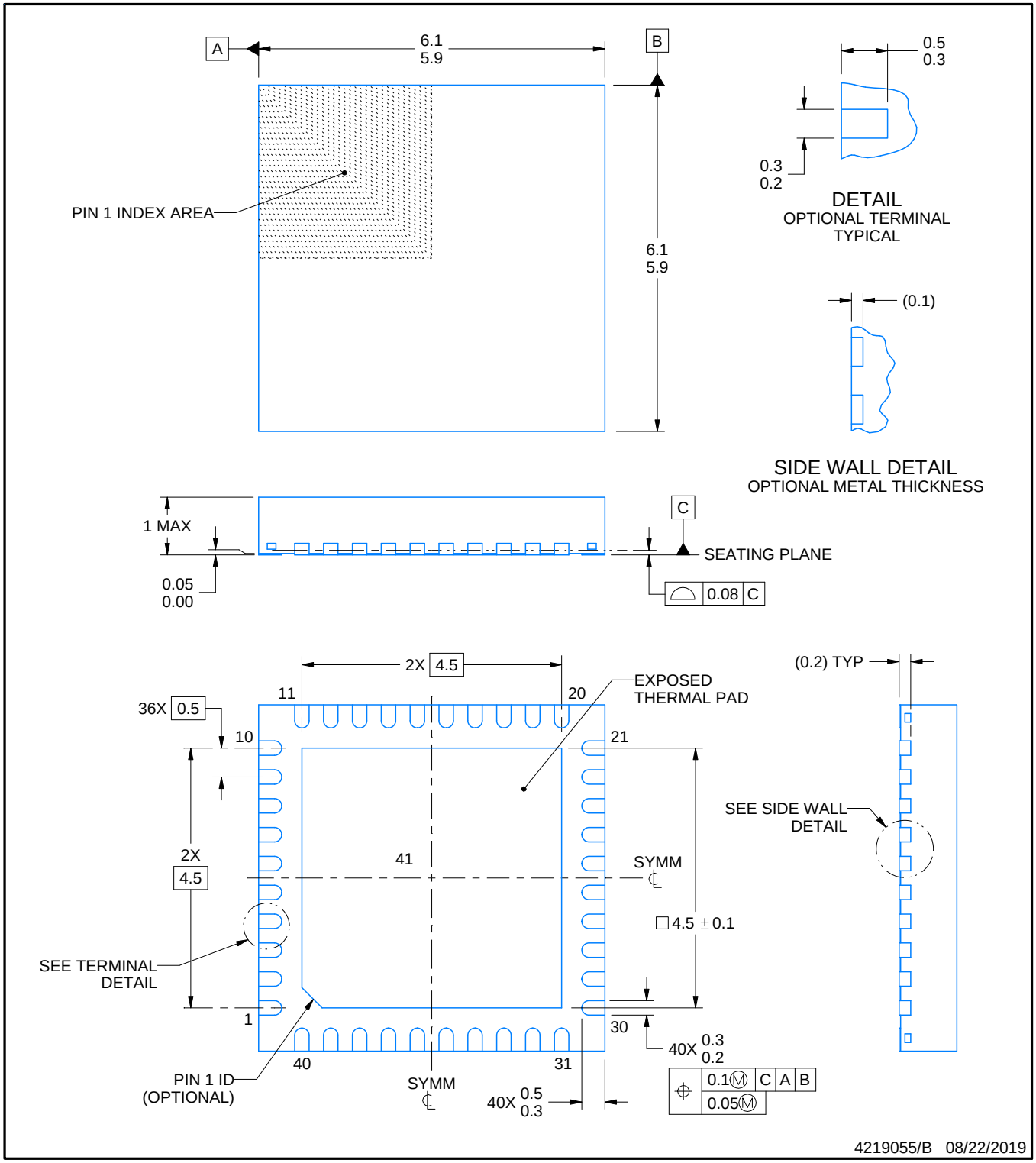
RHA0040H



PACKAGE OUTLINE

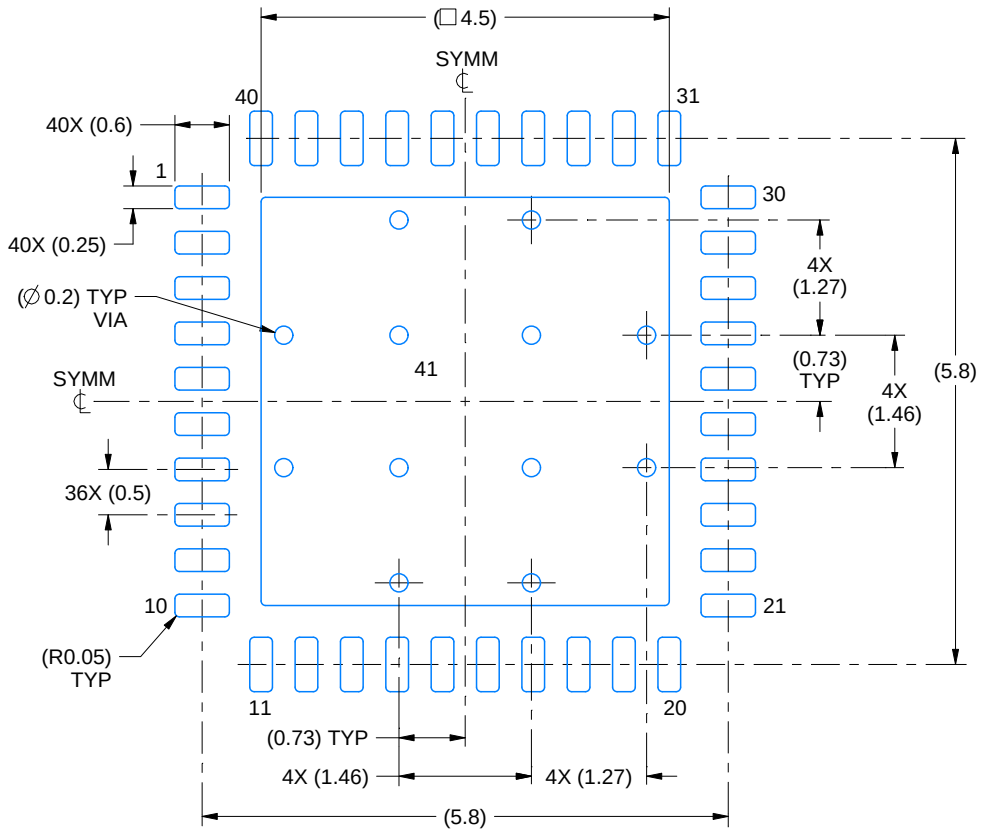
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

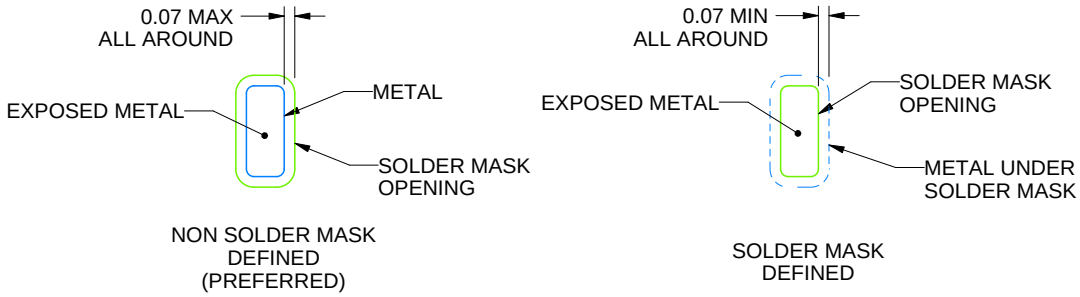


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:12X

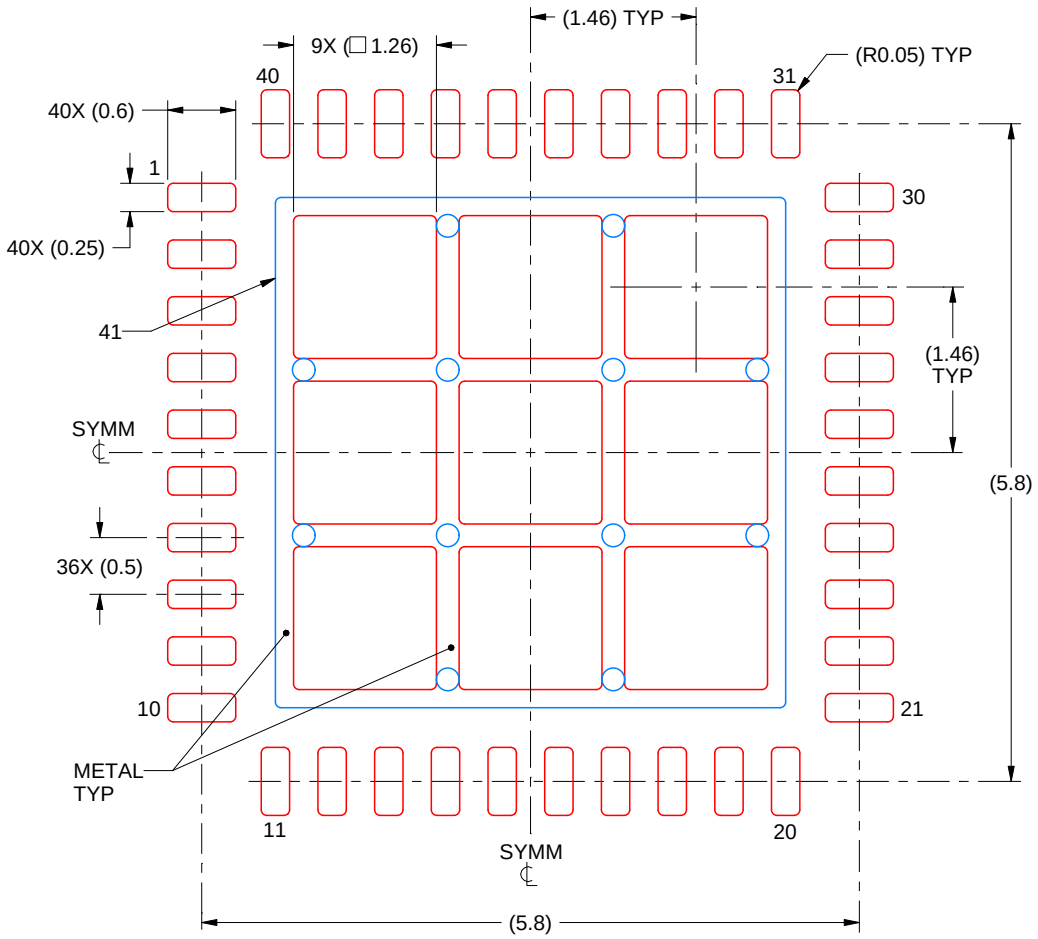


SOLDER MASK DETAILS

4219055/B 08/22/2019

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 41:
70% PRINTED SOLDER COVERAGE BY AREA
SCALE:15X

4219055/B 08/22/2019

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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最終更新日：2025 年 10 月