LMH34400 240MHz、シングルエンド、トランスインピーダンス・アンプ、クランプ内蔵

1 特長

- 内蔵ゲイン:40kΩ
- 性能、C_{PD} = 1pF:
  - 帯域幅:240MHz
  - 入力換算ノイズ:50nA$_{RMS}$
  - 立ち上がり / 立ち下がり時間:1.5ns
- 環境光キャンセル機能内蔵
- 100mA 保護クランプ内蔵
- 静止電流:20mA
- ローパワー・モード電流:1.5mA
- 温度範囲:–40℃～+125℃

2 アプリケーション

- 機械式スキャン LIDAR
- ソリッド・ステート・スキャン LIDAR
- レーザー距離計
- 光学 ToF 位置センサ
- ドローン・ビジョン
- 産業用ロボットの LIDAR
- 移動型ロボットの LIDAR
- 掃除ロボットの LIDAR

3 概要

LMH34400 は、LIDAR (光検出と測距) アプリケーションとレーザー距離測定システムのための、産業用でクラス最小の固定ゲイン、シングルエンド・トランスインピーダンス・アンプです。LMH34400 は、出力スイング 1.0V$_{PP}$ を実現し、入力換算ノイズは 50nA$_{RMS}$ です。

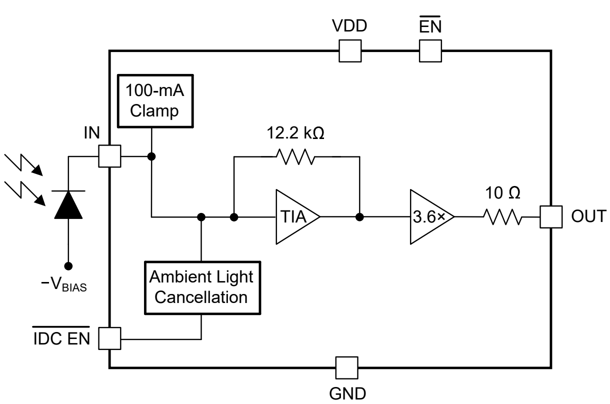
LMH34400 は、過負荷入力状態からアンプを保護し迅速にデバイスを回復させることができる 100mA のクランプを内蔵しています。LMH34400 は、フォトダイオードとアンプとの AC 結合の代わりに使用できる環境光キャンセル (ALC) 回路も内蔵しているため、基板面積とシステム・コストを削減できます。測定する周波数信号が 400kHz 未満の場合は、ALC ループをディセーブルにします。

アンプを使用していないときに電力を節約するために、LMH34400 は $\overline{EN}$ ピンを使用して低消費電力モードに設定できます。この機能により、$\overline{EN}$ 制御ピンをマルチプレクサ選択機能として使用し、複数の LMH34400 アンプを受信信号チェーンの次の段の入力に多重化できます。LMH34400 は、シングルエンド出力を提供し、時間 / デジタル・コンバータ (TDC) ベースの LIDAR システムと組み合わせて使用するために最適化されています。

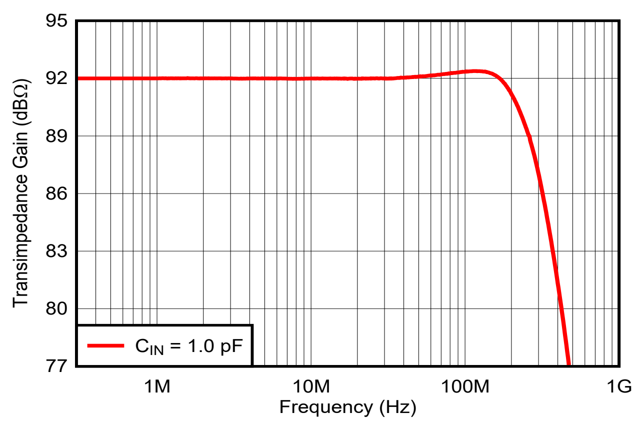
パッケージ情報

部品番号	パッケージ (1)	パッケージ・サイズ (2)
LMH34400	DRL (SOT5X3、6)	1.6mm × 1.6mm

(1) 詳細については、セクション 10 を参照してください。
(2) パッケージ・サイズ (長さ×幅) は公称値であり、該当する場合はピンも含まれます。



概略ブロック図



トランスインピーダンス帯域幅と周波数との関係

Table of Contents

4 Pin Configuration and Functions

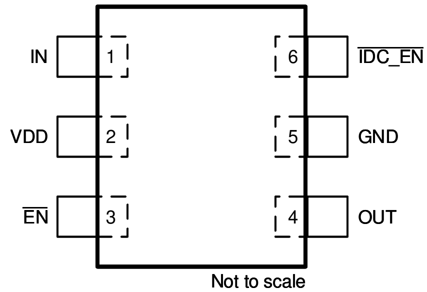


図 4-1. DRL Package, 6-Pin SOT5X3 (Top View)

表 4-1. Pin Functions

PIN		TYPE[1]	DESCRIPTION
NAME	**NO.**		
$\overline{\text{EN}}$	3	I	Device enable pin. $\overline{\text{EN}}$ = logic low = normal operation (default)[2]; $\overline{\text{EN}}$ = logic high = low-power mode.
GND	5	I	Amplifier ground
$\overline{\text{IDC\_EN}}$	6	I	Ambient light cancellation loop enable. $\overline{\text{IDC\_EN}}$ = logic low = enable dc cancellation (default)[2]; $\overline{\text{IDC\_EN}}$ = logic high = disable dc cancellation.
IN	1	I	Transimpedance amplifier input
OUT	4	O	Amplifier output
VDD	2	I	Positive power supply

(1) I = input, O = output
(2) TI recommends driving a digital pin with a low-impedance source rather than leaving the pin floating because fast-moving transients can couple into the pin and inadvertently change the logic level.

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[1]

		MIN	MAX	UNIT
V_{DD}	Total supply voltage		3.65	V
	Voltage at output pin	0	V_{DD}	V
	Voltage at logic pins	–0.25	V_{DD}	V
I_{IN}	Continuous current into IN		25	mA
I_{OUT}	Continuous output current		35	mA
T_J	Junction temperature		150	°C
T_A	Operating free-air temperature	–40	125	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins[1]	±1000	V
		Charged device model (CDM), per ANSI/ESDA/JEDEC JS-002, all pins[2]	±250	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{DD}	Total supply voltage	3	3.3	3.45	V
T_A	Operating free-air temperature	–40		125	°C

5.4 Thermal Information

THERMAL METRIC[1]		LMH34400 DRL (SOT-563) 6 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	201.2	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	101.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	83.2	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	5.4	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	82.4	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

5.5 Electrical Characteristics

at V_{DD} = 3.3 V, C_{PD} (1) = 1 pF, $\overline{EN}$ = 0 V, $\overline{IDC\_EN}$ = 3.3 V, R_L = 100 Ω (Output is AC-coupled for AC performance parameters; for DC performance parameters load is referenced to 1V), and T_A = 25℃ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
AC PERFORMANCE						
SSBW	Small-signal bandwidth	V_{OUT} = 100 mV_{PP}		240		MHz
LSBW	Large-signal bandwidth	V_{OUT} = 1 V_{PP}		240		MHz
t_R, t_F	Rise and fall time	V_{OUT} = 100 mV_{PP}, pulse duration = 10 ns		1.5		ns
	Slew rate (2)	V_{OUT} = 1 V_{PP}, pulse duration = 10 ns		470		V/µs
	Overload recovery time (1% settling)	I_{IN} = 10 mA, pulse duration = 10 ns		18		ns
	Overload pulse extension (3)	I_{IN} = 10 mA, pulse duration = 10 ns		3		ns
e_N	Output noise density	f = 10 MHz		94		nV/√Hz
i_N	Integrated input-referred noise	f = DC to 250 MHz		50		nA_{RMS}
Z_{OUT}	Closed-loop output impedance	f = 50 MHz		10		Ω
DC PERFORMANCE						
Z_{21}	Small-signal transimpedance gain (4)		33	40	46	kΩ
V_O	Default output voltage	I_{IN} = 0 µA	0.93	1	1.07	V
$\Delta V_O/\Delta T_A$	Output voltage drift			±20		µV/°C
INPUT PERFORMANCE						
R_{IN}	Input Resistance		50	100	150	Ω
V_{IN}	Default input bias voltage	Input pin floating	2.44	2.5	2.55	V
$\Delta V_{IN}/\Delta T_A$	Default input bias voltage drift	Input pin floating		1.1		mV/°C
I_{IN}	DC input current range	Z_{21} < 3-dB degradation from I_{IN} = 5 µA	27	34		µA
OUTPUT PERFORMANCE						
V_{OH}	Output voltage swing (high) (5)		2.05	2.3		V
		T_A = –40°C to 125°C		2.3		V
V_{OL}	Output voltage swing (low) (6)			0.4	0.6	V
		T_A = –40°C to 125°C		0.45		V
I_{OUT}	Linear output drive (source)	I_{IN} = 15 µA, R_L = 25 Ω	16	19	22	mA
		T_A = –40°C, I_{IN} = 15 µA, R_L = 25 Ω		19		mA
		T_A = 125°C, I_{IN} = 15 µA, R_L = 25 Ω		19		mA
I_{SC}	Output short-circuit current (7)			85		mA
Z_{OUT}	DC output impedance (amplifier enabled)		7	10	13	Ω
AMBIENT LIGHT CANCELLATION PERFORMANCE ($\overline{IDC\_EN}$ = 0 V) (8)						
	Settling time	I_{IN} = 0 µA → 100 µA		6		µs
		I_{IN} = 100 µA → 0 µA		35		µs
	Ambient light current cancellation range	Output offset shift from I_{DC} = 5 µA < ±10 mV	2	3		mA
POWER SUPPLY						
I_Q	Quiescent current		16	20	24	mA
		T_A = 125°C		22.5		mA
		T_A = –40°C		18		mA

5.5 Electrical Characteristics (続き)

at V_{DD} = 3.3 V, C_{PD} [(1)] = 1 pF, $\overline{EN}$ = 0 V, $\overline{IDC\_EN}$ = 3.3 V, R_L = 100 Ω (Output is AC-coupled for AC performance parameters; for DC performance parameters load is referenced to 1V), and T_A = 25℃ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SHUTDOWN						
I_Q	Disabled quiescent current ($\overline{EN}$ = V_{DD})		1.2	1.5	1.7	mA
		T_A = –40°C		1.4		mA
		T_A = 125°C		1.6		mA
	$\overline{EN}$ and $\overline{IDC\_EN}$ pins input bias current			65	90	µA

(1) Input capacitance of photodiode.
(2) Average of rising and falling slew rate.
(3) Pulse duration extension measured at 50% of pulse height of square wave.
(4) Gain measured at the amplifier output pin when driving a 100-Ω resistive load. At higher resistor loads the gain increases.
(5) Photodiode anode biased to a negative voltage
(6) Photodiode cathode biased to a positive voltage
(7) Device cannot withstand continuous short-circuit.
(8) Enabling the ambient light cancellation loop adds noise to the system.

5.6 Electrical Characteristics: Logic Threshold and Switching Characteristics

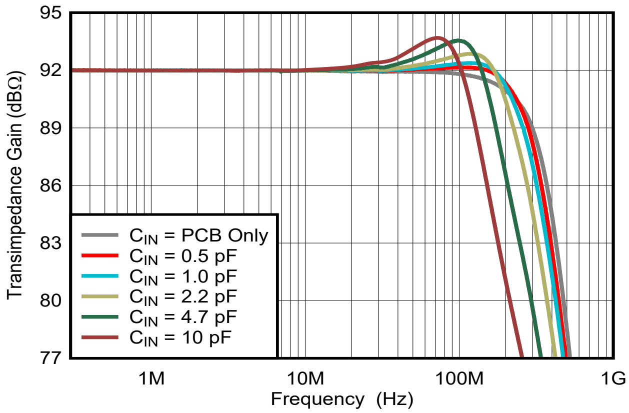
at V_{DD} = 3.3 V, C_{PD} [(1)] = 1 pF, $\overline{EN}$ = 0 V, $\overline{IDC\_EN}$ = 3.3 V, R_L = 100 Ω (Output is AC-coupled for AC performance parameters; for DC performance parameters load is referenced to 1V), and T_A = 25℃ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
LOGIC THRESHOLD PERFORMANCE						
	$\overline{EN}$ control threshold voltage	Amplifier disabled above this voltage		1.6	2	V
		Amplifier enabled below this voltage	0.8	1.2		V
	$\overline{IDC\_EN}$ control threshold voltage	Ambient light cancellation loop disabled above this voltage		1.6	2	V
		Ambient light cancellation loop enabled below this voltage	0.8	1.2		V
$\overline{EN}$ CONTROL TRANSIENT PERFORMANCE						
	Enable transition-time (1% settling)	Ambient loop disabled, f_{IN} = 25 MHz, V_{OUT} = 1 V_{PP}, I_{DC} = 0 µA		200		ns
	Disable transition-time (1% settling)	Ambient loop disabled, f_{IN} = 25 MHz, V_{OUT} = 1 V_{PP}, I_{DC} = 0 µA		3.5		ns
	Enable transition-time (1% settling)	Ambient loop enabled, f_{IN} = 25 MHz, V_{OUT} = 1 V_{PP}, I_{DC} = 100 µA		10		µs
	Disable transition-time (1% settling)	Ambient loop enabled, f_{IN} = 25 MHz, V_{OUT} = 1 V_{PP}, I_{DC} = 100 µA		3.5		ns

(1) Input capacitance of photodiode.

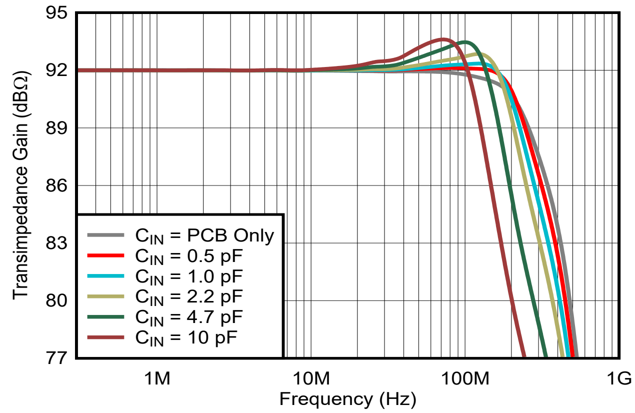
5.7 Typical Characteristics

at V_{DD} = 3.3 V, C_{PD} = 1 pF, $\overline{EN}$ = 0 V (enabled), $\overline{IDC\_EN}$ = 3.3 V (disabled), R_L = 100 Ω, and T_A = 25°C (unless otherwise noted)



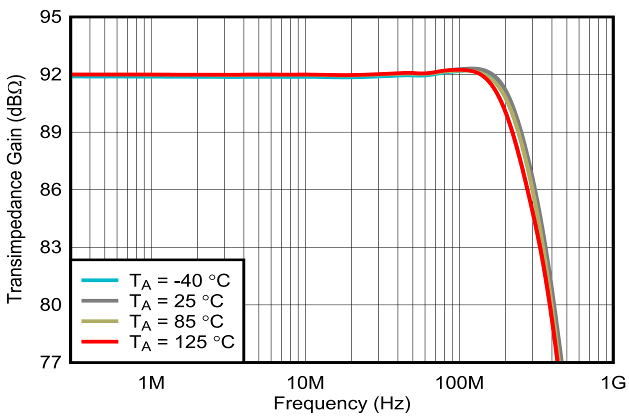
V_{OUT} = 100 mV_{PP}

図 5-1. Small-Signal Response vs Input Capacitance



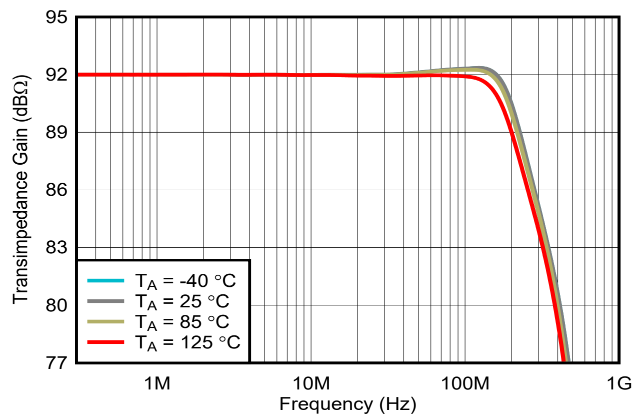
V_{OUT} = 1 V_{PP}

図 5-2. Large-Signal Response vs Input Capacitance



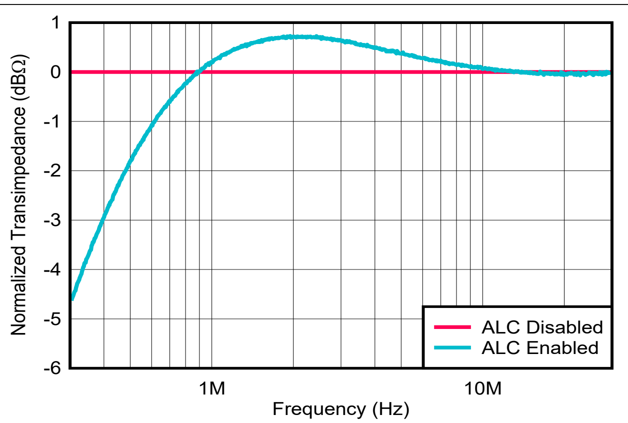
V_{OUT} = 100 mV_{PP}

図 5-3. Small-Signal Response vs Ambient Temperature



V_{OUT} = 1 V_{PP}

図 5-4. Large-Signal Response vs Ambient Temperature



I_{DC_IN} = 100 µA

図 5-5. Low-side Frequency Response vs Ambient Light Cancellation

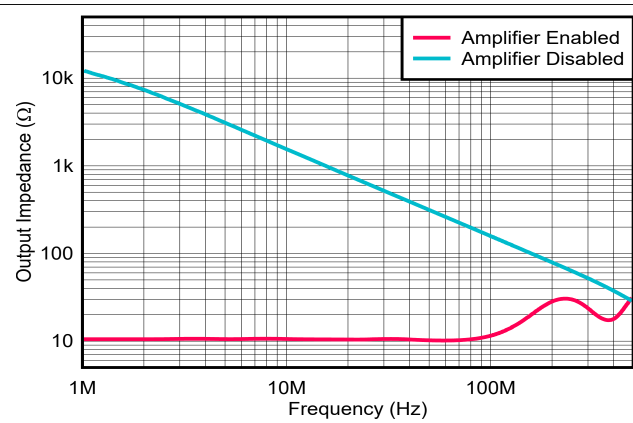


図 5-6. Closed-Loop Output Impedance vs Frequency

5.7 Typical Characteristics (continued)

at V_{DD} = 3.3 V, C_{PD} = 1 pF, $\overline{EN}$ = 0 V (enabled), $\overline{IDC\_EN}$ = 3.3 V (disabled), R_L = 100 Ω, and T_A = 25°C (unless otherwise noted)

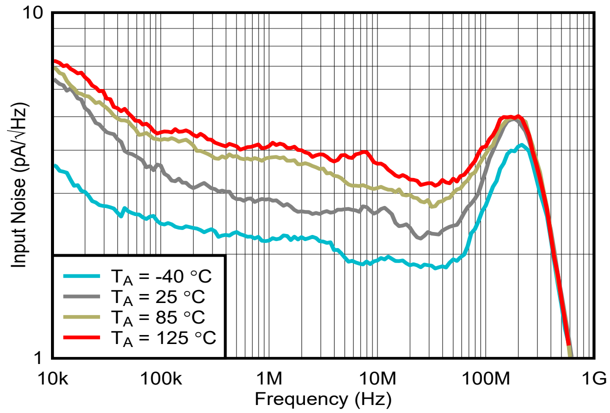


図 5-7. Input Noise Density vs Ambient Temperature

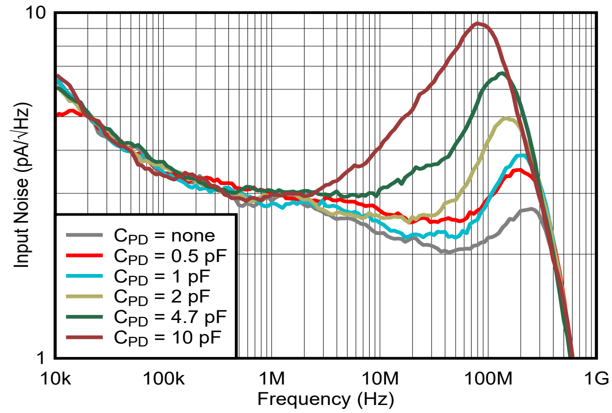
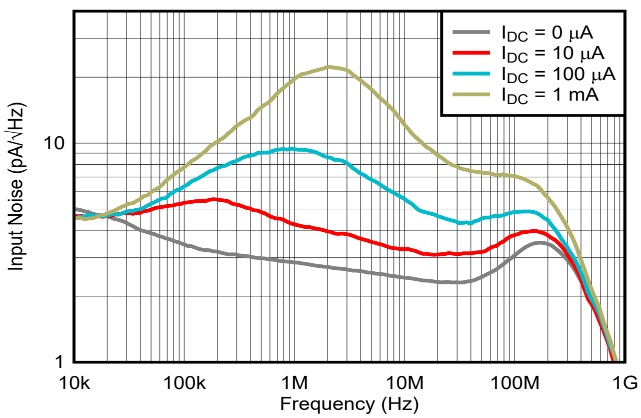


図 5-8. Input Noise Density vs Input Capacitance



$\overline{IDC\_EN}$ = 0 V

図 5-9. Input Noise Density vs Ambient Light DC Current

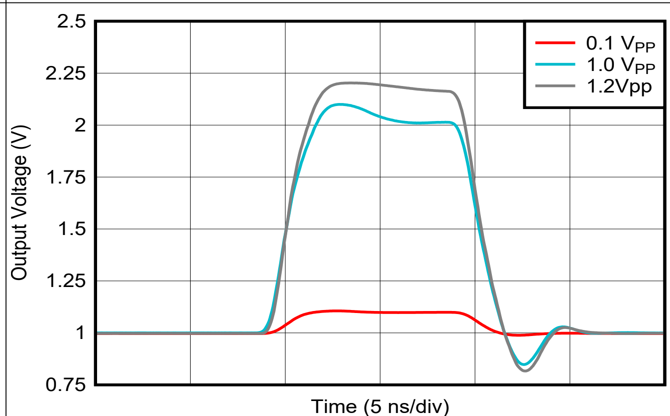


図 5-10. Pulse Response vs Output Swing

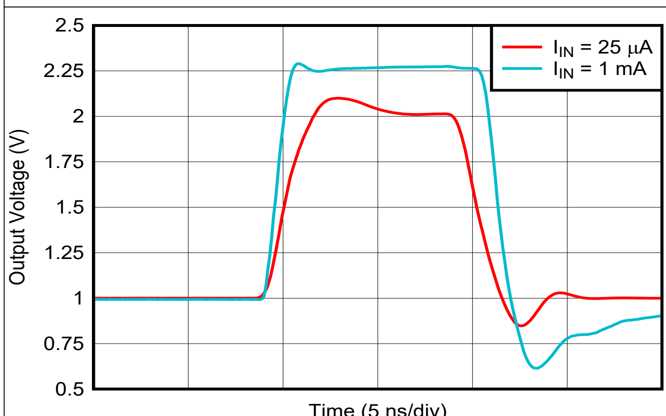


図 5-11. Overloaded Pulse Response

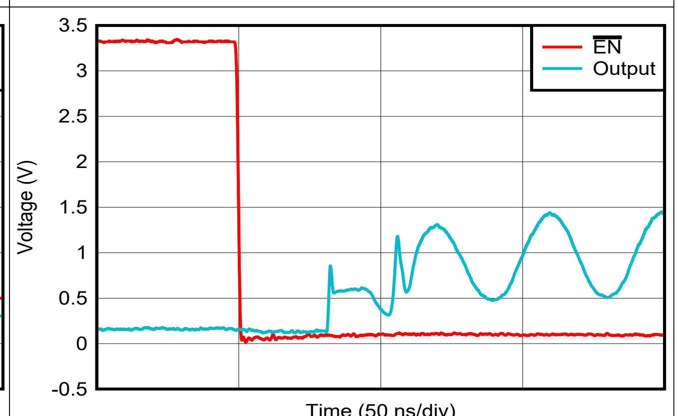


図 5-12. Turn-On Time

5.7 Typical Characteristics (continued)

at V_{DD} = 3.3 V, C_{PD} = 1 pF, $\overline{EN}$ = 0 V (enabled), $\overline{IDC\_EN}$ = 3.3 V (disabled), R_L = 100 Ω, and T_A = 25°C (unless otherwise noted)

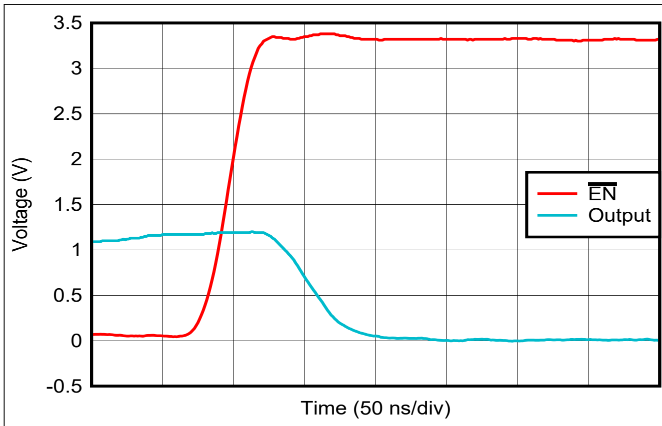
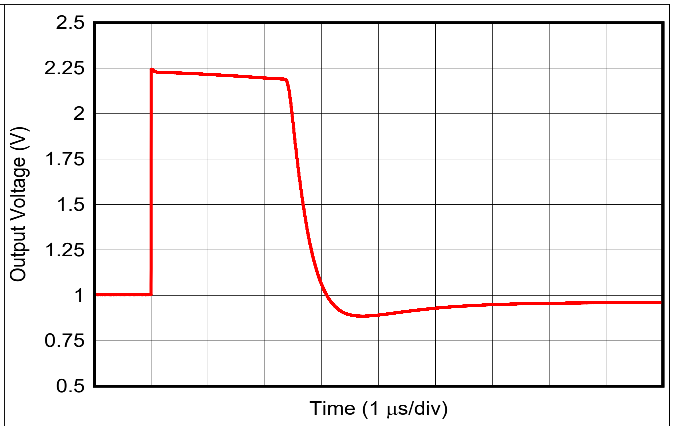
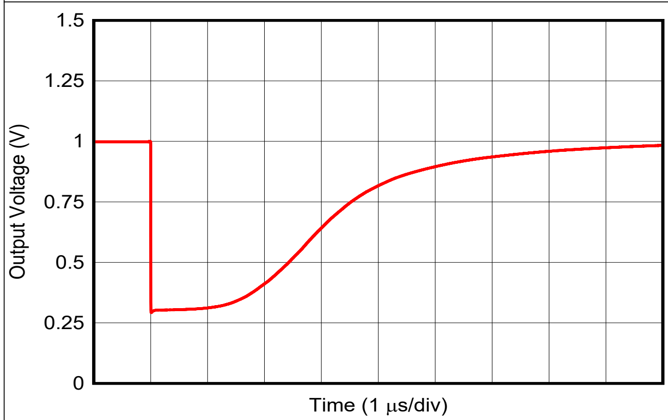


図 5-13. Turn-Off Time



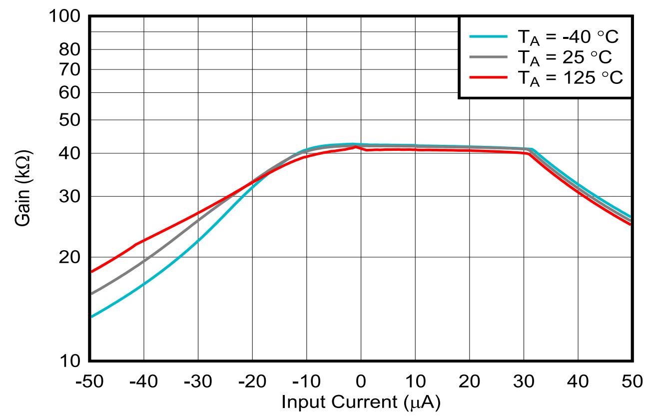
I_{DC_IN} = 0 µA → 100 µA

図 5-14. Ambient Loop Cancellation Settling Time



I_{DC_IN} = 100 µA → 0 µA

図 5-15. Ambient Loop Cancellation Settling Time



Positive current is sinking current into the photodiode cathode

図 5-16. Transimpedance Gain vs Input Current

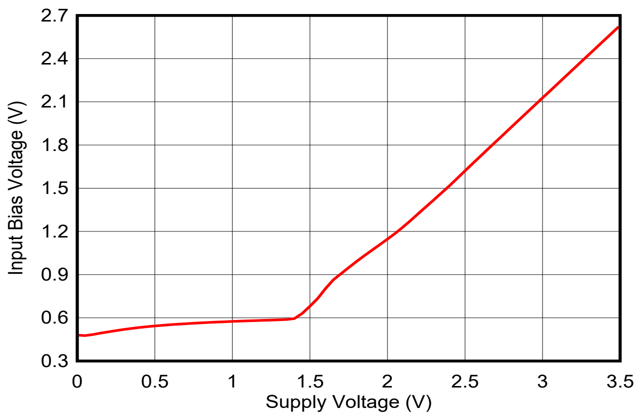


図 5-17. Input Bias Voltage vs Supply Voltage

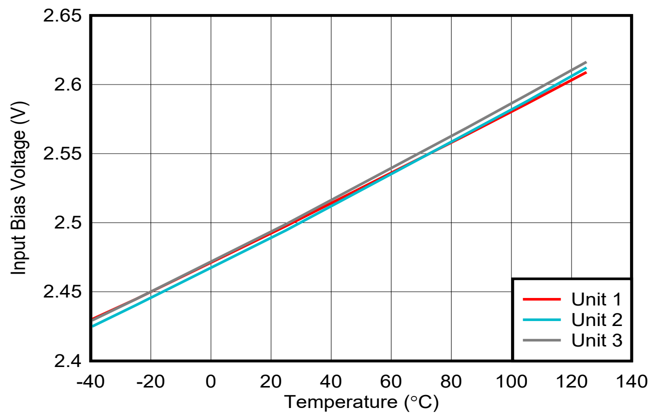


図 5-18. Input Bias Voltage vs Ambient Temperature

5.7 Typical Characteristics (continued)

at V_{DD} = 3.3 V, C_{PD} = 1 pF, $\overline{EN}$ = 0 V (enabled), $\overline{IDC\_EN}$ = 3.3 V (disabled), R_L = 100 Ω, and T_A = 25°C (unless otherwise noted)

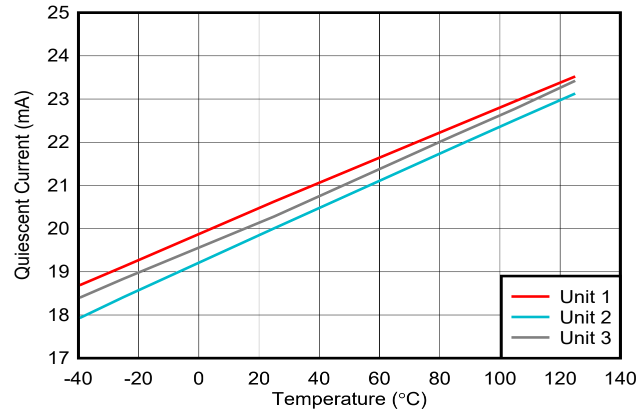


図 5-19. Quiescent Current vs Ambient Temperature

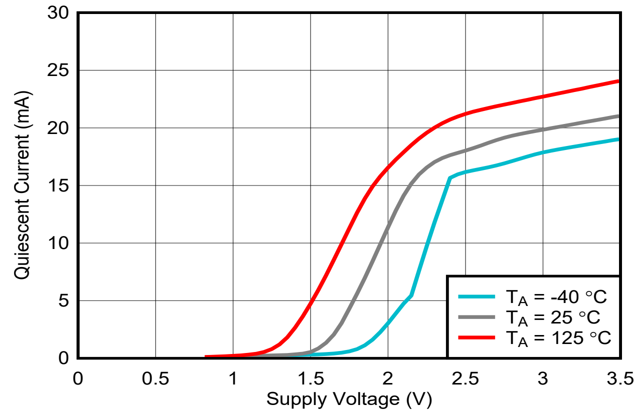


図 5-20. Quiescent Current vs Supply Voltage

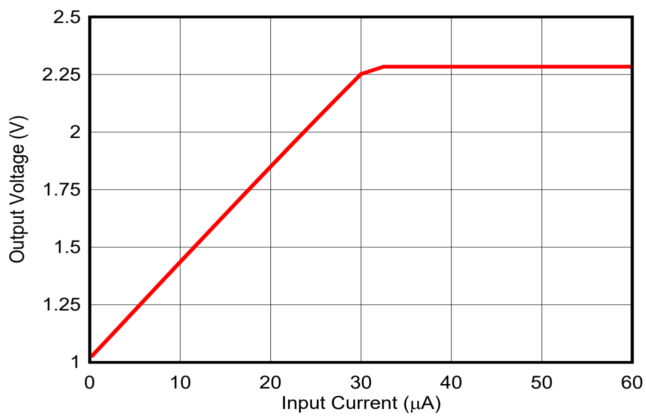


図 5-21. Output Voltage vs Input Current

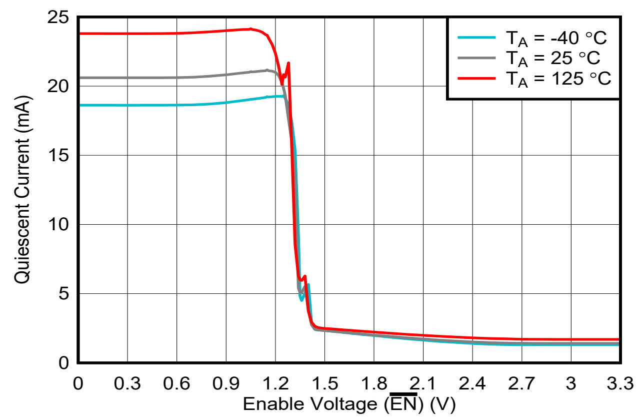
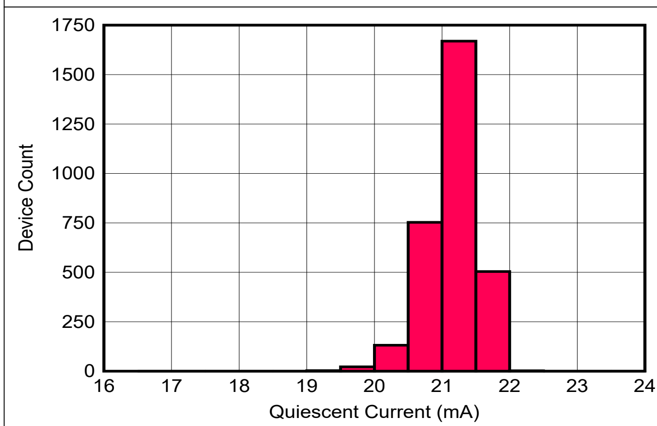
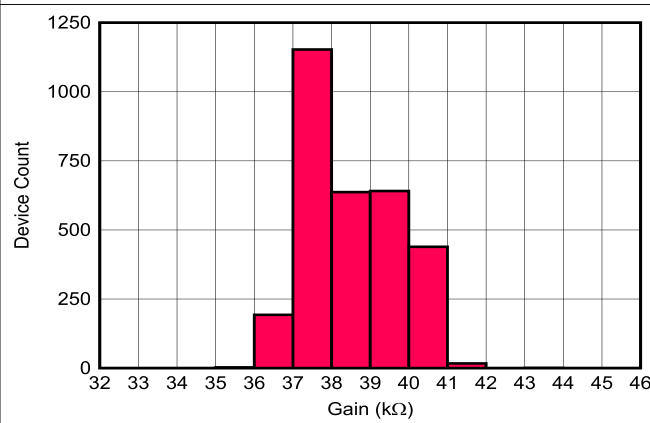


図 5-22. Logic Threshold vs Ambient Temperature



μ = 21.1 mA, σ = 0.38 mA

図 5-23. Quiescent Current Distribution

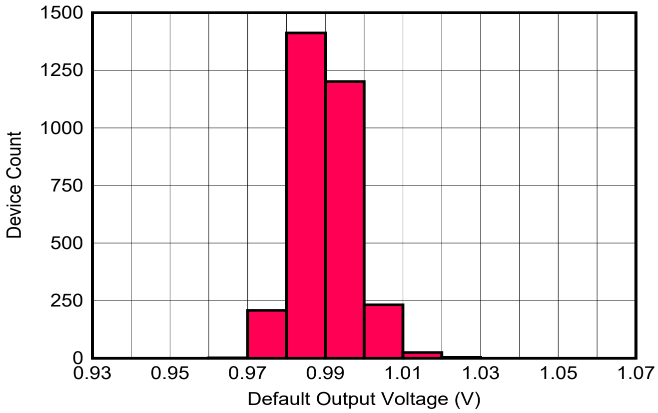


μ = 38.5 kΩ, σ = 1.2 kΩ

図 5-24. Transimpedance Gain Distribution

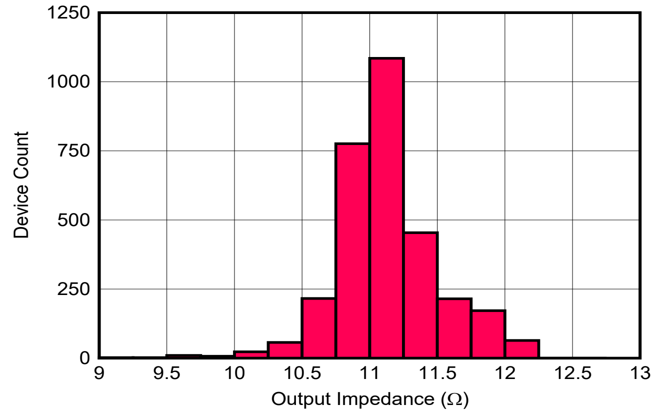
5.7 Typical Characteristics (continued)

at V_{DD} = 3.3 V, C_{PD} = 1 pF, $\overline{EN}$ = 0 V (enabled), $\overline{IDC\_EN}$ = 3.3 V (disabled), R_L = 100 Ω, and T_A = 25°C (unless otherwise noted)



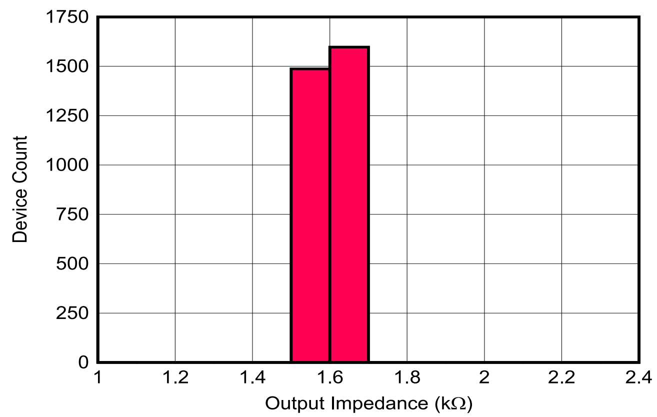
μ = 0.99 V, σ = 0.0073 V

図 5-25. Default Output Voltage Distribution



μ = 11 Ω, σ = 0.38 Ω, device enabled

図 5-26. Output Impedance (Z_{OUT}) Distribution



μ = 1.6 kΩ, σ = 0.013 kΩ, device disabled

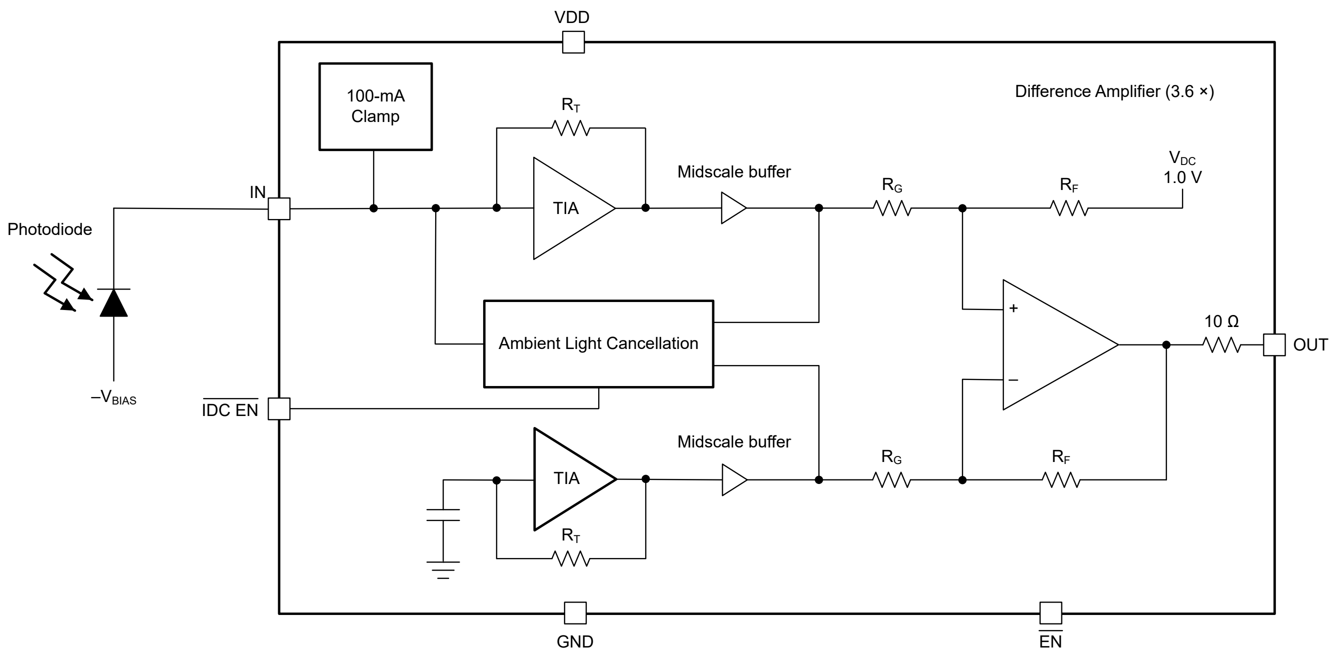
図 5-27. Output Impedance (Z_{OUT}) Distribution

6 Detailed Description

6.1 Overview

The LMH34400 is a single-channel, single-ended output, high-speed transimpedance amplifier (TIA) and features several integrated functions geared towards light detection and ranging (LIDAR) and pulsed time-of-flight (ToF) systems. The LMH34400 is designed to work with photodiode (PD) anodes that are biased to a negative voltage and cathodes that are tied to the amplifier input; therefore, the amplifier sources the photocurrent. The LMH34400 is offered in a space-saving 1.6-mm × 1.6-mm, 6-pin SOT5X3 package and is rated over a temperature range from –40°C to +125°C.

6.2 Functional Block Diagram



6.3 Feature Description

6.3.1 Clamping and Input Protection

The LMH34400 is designed to work with photodiode (PD) configurations that can source or sink current; the LMH34400, however, is optimized for a sinking current configuration. It is assumed that the LMH34400 device is being used with a PD that is configured with its cathode tied to the amplifier input and the anode tied to a negative supply voltage, unless stated otherwise.

The LMH34400 features two internal clamps, a fast recovery clamp and a soft clamp. The fast recovery clamp is the active clamp when the photodiode is sinking a photocurrent. The soft clamp is the active clamp when the photodiode is sourcing a photocurrent.

Stray reflections from nearby objects with high reflectivity can produce large output current pulses from the PD. The linear input range of the LMH34400 is approximately 30 µA. Input currents in excess of the linear current range cause the internal nodes of the amplifier to saturate, which increases the amplifier recovery time. The end result is a broadening of the output pulse leading to blind zones in the system. To protect against this condition, the LMH34400 features an integrated clamp that absorbs and diverts the excess current to the positive supply (V_{DD}) when the amplifier detects its nodes entering a saturated condition. The integrated clamp minimizes the pulse extension to less than a few nanoseconds for input pulses up to 100 mA. When the amplifier is in low-power mode, the clamp circuitry is still active, thereby protecting the TIA input.

6.3.2 ESD Protection

All LMH34400 IO pins excluding (VDD and GND) have an internal electrostatic discharge (ESD) protection diode to the positive and negative supply rails to protect the amplifier from ESD events.

6.3.3 Single-Ended Output Stage

The output stage of the LMH34400 has a 10-Ω series resistor on its output to isolate the amplifier output stage transistors from the package bond-wire inductance and printed circuit board (PCB) capacitance. The net gain of the LMH34400 (TIA + output stage) is 40 kΩ when driving an external 100-Ω resistor. When the external load resistor is increased above 100 Ω, the effective gain from the IN pin to the output pin increases. Consequently, when the external load resistor is decreased to less than 100 Ω, the effective gain from the IN pin to the output pin decreases as a result of the larger voltage drop across the internal 10-Ω resistor. When there is no load resistor connected to the output pin, the effective TIA gain is 44 kΩ. The output voltage of the LMH34400 is set to a fixed value of 1.0 V when there is no current flowing into the amplifier. The output swings above and below 1.0 V when the photodiode sinks and sources current, respectively.

6.4 Device Functional Modes

6.4.1 Ambient Light Cancellation Mode

The LMH34400 has an integrated DC cancellation loop that can used to cancel any voltage offsets resulting from ambient light. The DC cancellation loop is enabled by setting $\overline{\text{IDC\_EN}}$ low. Incident ambient light on a photodiode produces a DC current resulting in an offset voltage at the output of the TIA stage. If the photodiode produces a DC output current resulting from ambient light, then the output of the level-shift buffer stage is offset from the reference voltage VREF. The ALC loop detects this offset and produces an opposing DC current to compensate for the differential offset voltage at its input. The loop has a high-pass cutoff frequency of 400 kHz. The ambient light cancellation loop is disabled when the amplifier is placed in low-power mode.

The shot noise current introduced by the DC cancellation loop increases the overall amplifier noise. So, if the ambient light level is negligible, then disable the loop to improve SNR. The cancellation loop helps save PCB space and system costs by eliminating the need for external AC coupling passive components. Additionally, the extra trace inductance and PCB capacitance introduced by using external AC coupling components degrades the LMH34400 dynamic performance.

6.4.2 Power-Down Mode (Multiplexer Mode)

The LMH34400 can be placed in low-power mode by setting $\overline{EN}$ high, which helps in saving system power. Enabling low-power mode puts the outputs of the internal amplifiers in the LMH34400 in a high-impedance state.

図 6-1 shows how this device feature can further save board space and cost by eliminating the need for a discrete high-speed multiplexer, if a system consists of several photodiode and amplifier channels multiplexed to single time-of-flight detector circuit. The disabled channel outputs are not an ideal open circuit; therefore, as the number of multiplexed channels increases, the disabled channels begin to load the enabled channel. An additional isolation resistor helps to reduce the impact of reflections from disabled channels. Multiplexing more than four channels in parallel degrades the performance of the enabled channel.

When the amplifier is in low-power mode, the clamp circuitry is still active thereby protecting the TIA input. The ambient light cancellation loop is disabled when the amplifier is placed in power-down mode. When the LMH34400 device is brought out of power-down operation, the ambient light cancellation loop requires several time constants to settle. The time constant is based on the 400-kHz cutoff frequency of the loop.

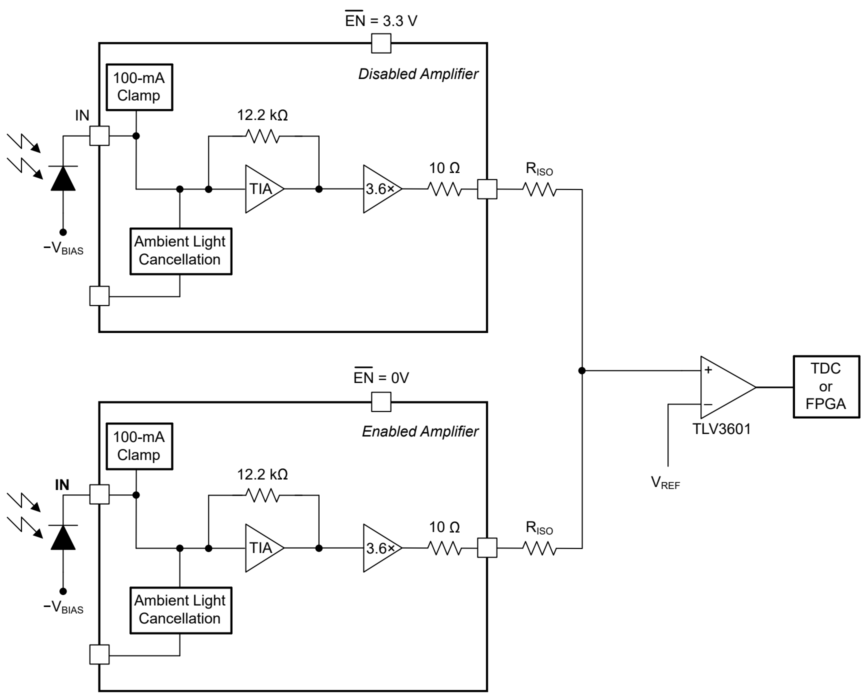


図 6-1. Configuring Two LMH34400 Devices in Multiplexer Mode

7 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

7.1 Application Information

The high gain and single-ended output of the LMH34400 is designed to be used in connection with a time-to-digital converter (TDC) for a time-of-flight (ToF) based receiver in a LIDAR system. The TDC function can be implemented using a stand-alone TDC or using a FPGA. ToF receive circuits that use TDC are significantly less expensive and consume considerably less power when compared to an analog-to-digital converter (ADC) based solution. The output of the LMH34400 presents an analog representation of the returned light pulse. Common practice uses a time-discriminator circuit before the TDC to precisely use a deterministic portion of the returned waveform to stop the TDC. The most straightforward method to accomplish this action is called leading-edge discrimination. This method uses a high-speed comparator with a low propagation delay to stop the TDC when the waveform crosses a chosen incoming light amplitude value.

In many applications, the amplitude of the returned pulse can vary considerably as a result of the difference in target reflectivity or simply the light source spreading out to a target moving to longer distances. For this reason, choose a comparator with low dispersion. If the dispersion is high, then the amplitude variation in the returned signal is converted to a variation in the timing signal presented to the TDC. This behavior is known as a *walk error*. 図 7-1 shows the LMH34400 connected to the TLV3601 high-speed comparator. In this configuration, an incoming optical pulse sources current out of the amplifier input pin and delivers a proportional voltage pulse to the comparator input. The amplifier output has 1.0-V dc with no input current; therefore, set the reference voltage of the comparator to a level greater than 1.0 V. For example, to have the comparator change states when the input is greater than 10 µA, then set the V_{REF} voltage to 1.0 V + (40 kΩ × 10 µA) = 1.4 V.

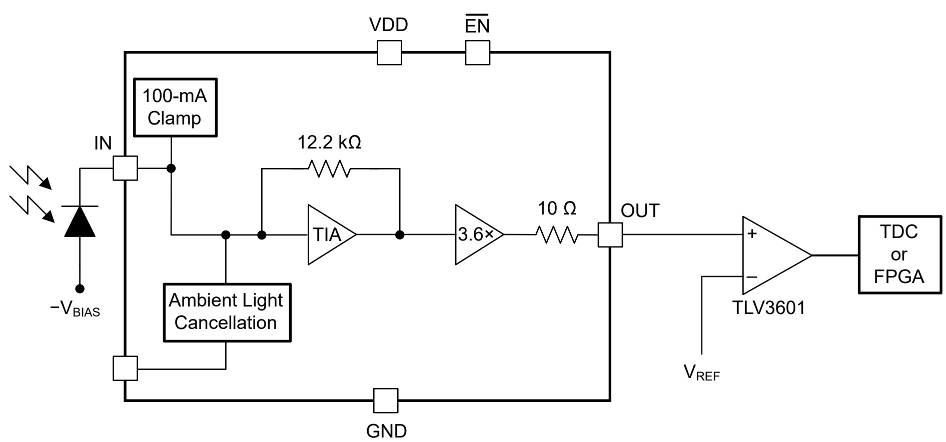


図 7-1. LMH34400 to Interface to Comparator and TDC

7.2 Typical Applications

7.2.1 LMH34400 Test Circuit

図 7-2 shows the circuit used to test the LMH34400 with a voltage source.

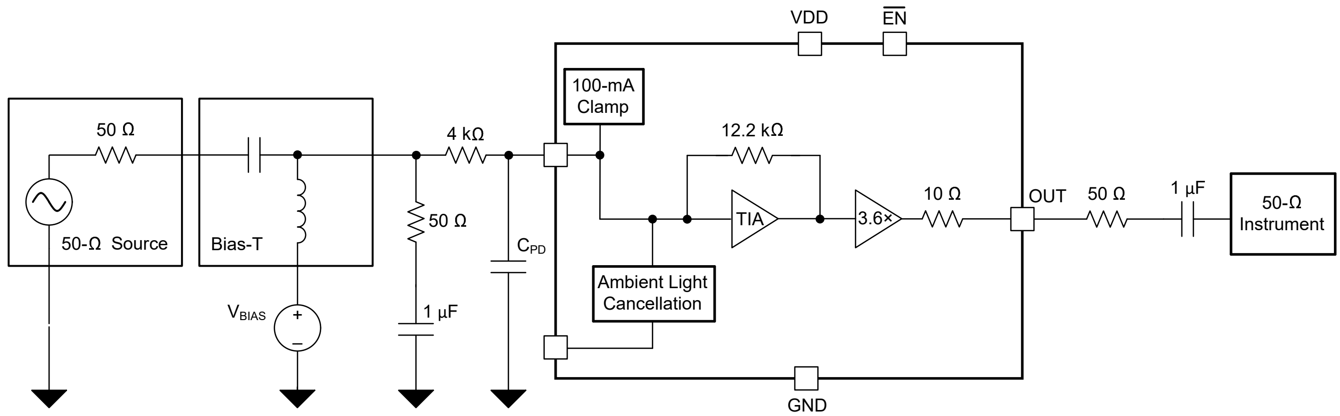


図 7-2. LMH34400 Test Circuit

7.2.1.1 Design Requirements

The objective is to design a low-noise, wideband output transimpedance amplifier. The design requirements are as follows:

- Amplifier supply voltage: 3.3 V
- Transimpedance gain: 40 kΩ
- Photodiode capacitance: C_{PD} = 1 pF
- Target bandwidth: 240 MHz
- Integrated input-referred noise: 50 nA_{RMS} (noise bandwidth = 250 MHz)

7.2.1.2 Detailed Design Procedure

図 7-2 shows the LMH34400 test circuit used to evaluate various bandwidth without using an optical input signal. The voltage source is dc biased close to the input bias voltage of the LMH34400 (approximately 2.5 V). The LMH34400 internal design is optimized to only source current out of the input pin (pin 1). When testing the LMH34400 with a network analyzer or other ac source, control the dc bias such that the sum of the input ac and dc components does not result in a sourcing current into the amplifier input.

In the configuration shown in 図 7-2, there is a 50-Ω series resistor that helps with any reflection into the observing instrument. The instrument can be any 50-Ω impedance input device such as a vector network analyzer (VNA) or oscilloscope. This setup creates a voltage divider on the output and reduces the TIA amplitude by a factor of two. Make sure to consider this factor when interpreting the measured results.

The bandwidth of a transimpedance amplifier strongly depends on the capacitance of the photodiode (C_{PD}) that is connected to the input pin of the amplifier. The larger the capacitance, the lower the closed-loop bandwidth. 図 7-3 shows when the C_{PD} that is connected to the LMH34400 is between 0 pF and 10 pF.

While bandwidth is inversely proportional to the photodiode capacitance, the input-referred current noise and photodiode capacitance are directly proportional. To measure the output noise, use the same circuit in 図 7-2 with a simple modification. In this case, remove all components on the input pin except C_{PD}. 図 7-4 shows the impact of the input-referred noise density as the C_{PD} is varied from 0 pF to 10 pF. As the capacitance increases, the amplitude and breadth of the high-frequency noise increases significantly.

図 7-5 shows the impact of an increasing photodiode capacitance on these two parameters in one plot. In this plot, the integrated input-referred noise is calculated over a fixed range of dc to 250 MHz. Both the small-signal bandwidth and integrated input-referred noise trend toward poorer performance as the capacitance increases. For the highest level of performance, minimize the photodiode capacitance. As the photodiode capacitance is proportional to the photodiode light-capturing area, the final value chosen is a compromise of several system variables and differs between applications.

7.2.1.3 Application Curves

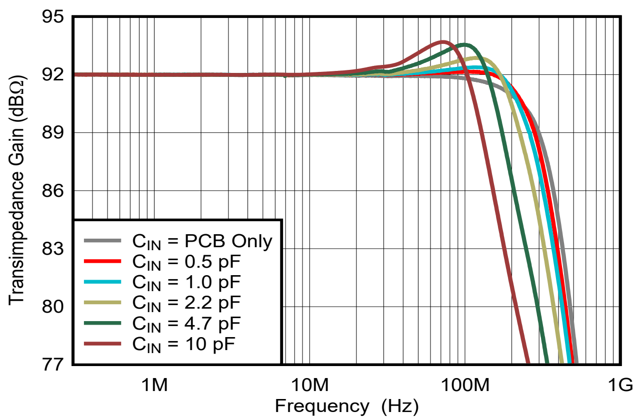


図 7-3. Small-Signal Response vs Input Capacitance

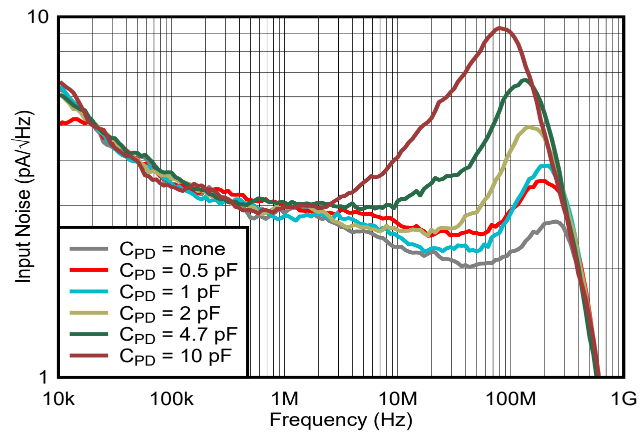


図 7-4. Input Noise Density vs Input Capacitance

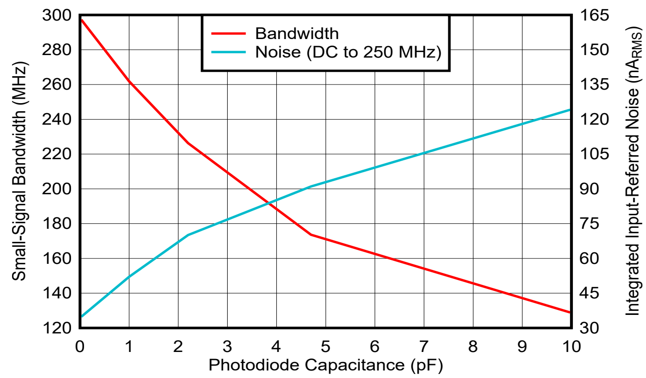


図 7-5. Bandwidth and Noise vs Input Capacitance

7.2.2 LMH34400 Signal Chain With Comparator

A common application for the LMH34400 is as a transimpedance front-end driving a comparator that can connect to a time-to-digital converter to calculate distances from pulse-based time-of-flight (ToF) measurements. 図 7-6 shows the test circuit using a commercially available photodiode with 1 pF of pin capacitance and a 2-GHz cutoff frequency. Select a photodiode with a cutoff frequency far greater than the LMH34400 bandwidth. The photodiode is connected to the LMH34400, which then drives the TLV3601 comparator. Choose a comparator with low input overdrive dispersion to reduce walk error.

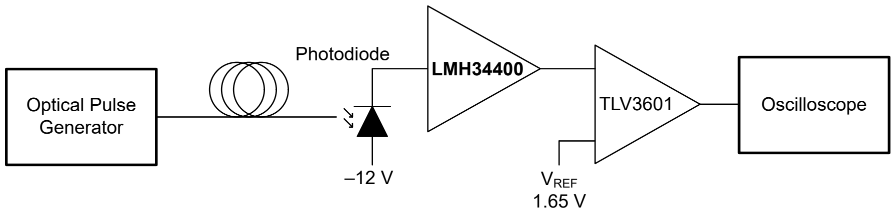


図 7-6. LMH34400 Signal Chain With Comparator

7.2.2.1 Design Requirements

The objective is to design a transimpedance front-end that can receive a 10 ns wide pulse, amplify the pulse through the LMH34400, and then drive the output through a comparator. The design requirements are as follows:

- Supply voltage 3.3 V
- Photodiode capacitance 1 pF
- Pulse width 10 ns
- Input current pulse edge rate 1 ns
- Input peak current 25 µA

7.2.2.2 Detailed Design Procedure

The circuit in 図 7-6 shows a photodiode anode connected to the LMH34400 that is followed by a comparator. To create the 10-ns, 25-µA input-current pulses, choose a photodiode with low input capacitance and minimal biasing requirements that allows for easy optical coupling through fiber. Given the 40-kΩ gain from the LMH34400, the expected output voltage with a 25-µA input current is a 1-V peak signal. With input-pulse edge rates of 1 ns, the LMH34400 is expected to produce slower pulse edges because the input slew rate is higher than the capabilities of the device. To increase the edge rates of the LMH34400 output signal, the TLV3601 comparator is added after the LMH34400 because the TLV3601 has a rise and fall time of 750 ps.

For a simple time-of-flight application, the output of the comparator can be connected to a time-to-digital converter (TDC) to perform a simple distance calculation. Using this method, the distance is calculated by measuring the time between outgoing and incoming pulse edges and multiplying by two. In the signal chain, the LMH34400 provides the initial signal amplification and conversion to a voltage. Then, the TLV3601 further increases the output amplitude, as well as provides a clean, fast edge to a following time-to-digital converter.

In the circuit design, the interface between the LMH34400 and the TLV3601 does not require any additional biasing or level shifting, because the LMH34400 default output bias interfaces easily with the comparator. Additionally, this 1-V bias level allows for setting the threshold voltage to half of the supply voltage, which keeps the threshold voltage as close as possible to the center of the comparator bias range. However, this threshold can be set at any value greater than 1 V to adjust for the dynamic-range requirements of the application. In this realization, the output of the TLV3601 is connected to a 50-Ω series output resistance to properly interface with 50-Ω terminated test equipment.

7.2.2.3 Application Curves

図 7-7 through 図 7-9 show the control signal input, LMH34400 output, and TLV3601 output, respectively, with a 10-ns wide, 1-ns edge rate input current pulse. The figures show the ability of the LMH34400 to convert a small 25-μA input signal to a 1-V output, and then use the TLV3601 to increase the edge rate and amplitude of the received pulse. Also, the shape of this output pulse stays approximately constant over a large range of optical input power levels. In this specific case, be aware that the output swing of the TLV3601 is limited because the TLV3601 is driving a matched 100-Ω load to interface with the test equipment.

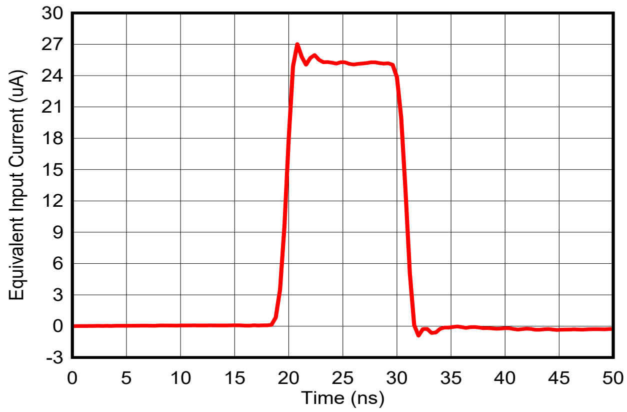


図 7-7. Equivalent Input Current Signal to LMH34400

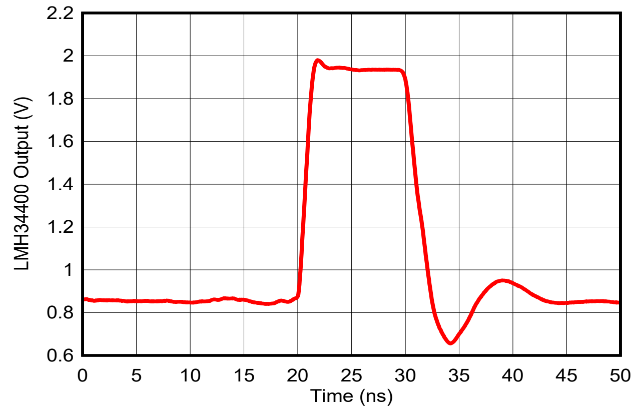


図 7-8. LMH34400 Output Voltage

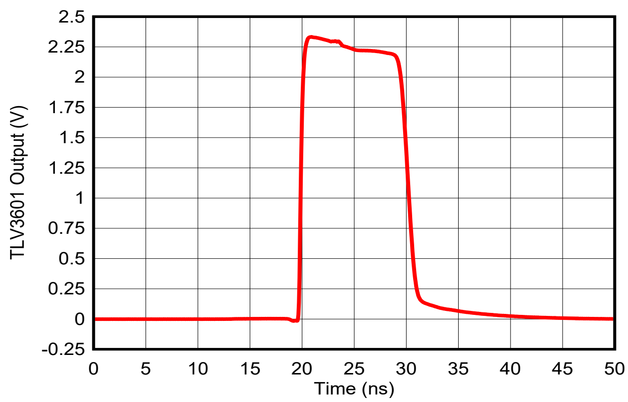


図 7-9. TLV3601 Output Voltage Driving 100-Ω Load

7.3 Power Supply Recommendations

The LMH34400 operates on a single 3.3-V power supply. A low power-supply source impedance must be maintained across frequency; therefore, use multiple bypass capacitors in parallel. Place the bypass capacitors as close as possible to the supply pin, and place the smallest capacitor on the same side of the PCB as the LMH34400. Preferably, also place the larger-valued bypass capacitors on the same side of the PCB. However, the capacitors can be positioned on the opposite side of the PCB using multiple vias if layout space is overly constrained.

7.4 Layout

7.4.1 Layout Guidelines

Achieving desired performance with a high-frequency amplifier such as the LMH34400 requires careful attention to board layout parasitics and external component types. Recommendations that optimize performance include:

- **Minimize parasitic capacitance from the signal I/O pins to ac ground.** Parasitic capacitance on the output pins can cause instability whereas parasitic capacitance on the input pin reduces the amplifier bandwidth. To reduce unwanted capacitance, cut out the power and ground traces under the signal input and output pins. Otherwise, ground and power planes must be unbroken elsewhere on the board.
- **Minimize the distance from the power-supply pins to high-frequency bypass capacitors.** Use high quality, 100-pF to 0.1-µF, C0G and NPO-type decoupling capacitors with voltage ratings at least three times greater than the amplifiers maximum power supplies. Place the smallest-value capacitors on the same side as the DUT. If possible, use low equivalent series impedance capacitors to further reduce the parasitic impedance. If space constraints force the larger value bypass capacitors to be placed on the opposite side of the PCB, then use multiple vias on the supply and ground side of the capacitors. This configuration provides is a low-impedance path to the amplifiers power-supply pins across the amplifiers gain bandwidth specification. Avoid narrow power and ground traces to minimize inductance between the pins and the decoupling capacitors. Use larger (2.2-µF to 6.8-µF) decoupling capacitors that are effective at lower frequency on the supply pins. Place these decoupling capacitors further from the device.

7.4.2 Layout Example

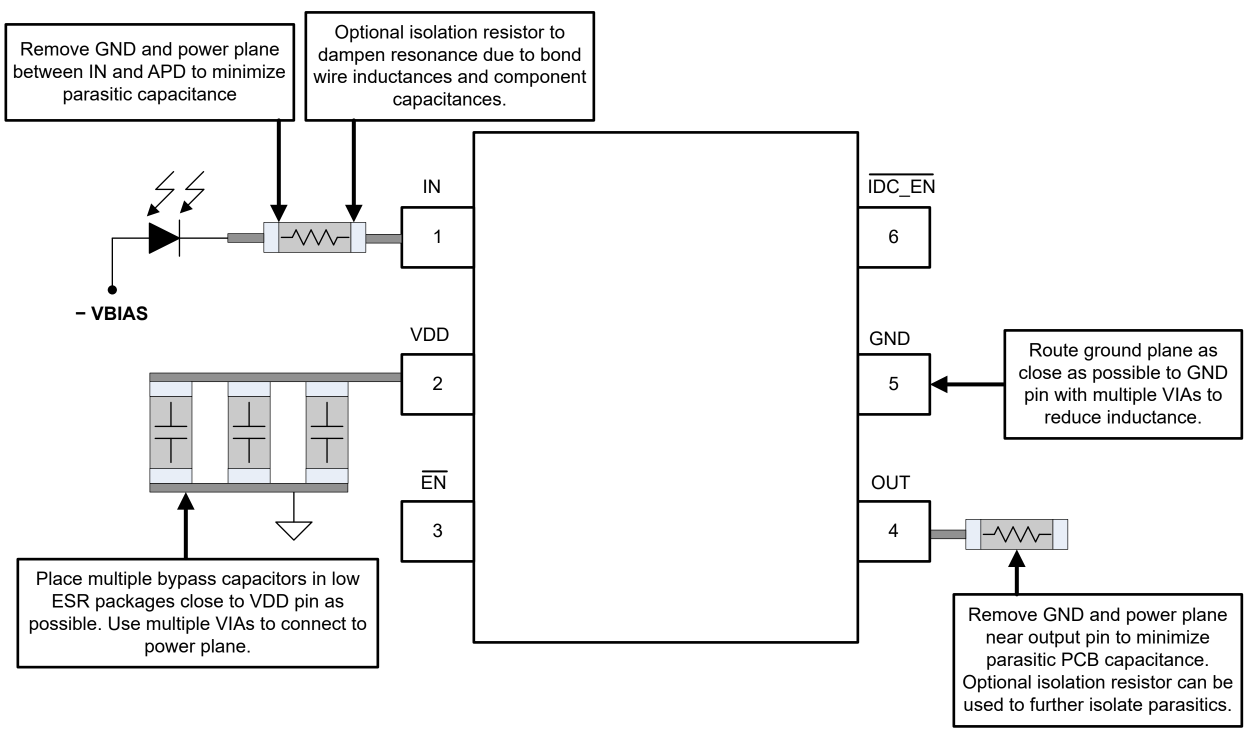


図 7-10. Layout Recommendation

8 Device and Documentation Support

8.1 Device Support

8.1.1 Development Support

- Texas Instruments, *LIDAR-Pulsed Time-of-Flight Reference Design Using High-Speed Data Converters* design guide
- Texas Instruments, *LIDAR Pulsed Time of Flight Reference Design* design guide
- Texas Instruments, *Optical Front-End System Reference Design* design guide

8.2 Documentation Support

8.2.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *LMH34400DRL Evaluation Module* user's guide
- Texas Instruments, *What You Need To Know About Transimpedance Amplifiers – Part 1* blog
- Texas Instruments, *What You Need To Know About Transimpedance Amplifiers – Part 2* blog
- Texas Instruments, *Training Video: How to Design Transimpedance Amplifier Circuits*
- Texas Instruments, *Training Video: High-Speed Transimpedance Amplifier Design Flow*
- Texas Instruments, *Training Video: How to Convert a TINA-TI Model into a Generic SPICE Model*
- Texas Instruments, *Transimpedance Considerations for High-Speed Amplifiers* application report

8.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

8.4 サポート・リソース

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ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

8.7 用語集

テキサス・インスツルメンツ用語集	この用語集には、用語や略語の一覧および定義が記載されています。

9 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision B (March 2023) to Revision C (October 2023) **Page**

- 本体サイズの列をパッケージ・サイズに変更、パッケージ名を SOT563 から SOT5X3 に変更、幅を 1.2mm から 1.6mm に変更、「パッケージ情報」表に注 2 を追加 1
- Updated package name and dimensions in *Overview* section.......... 12
- Changed referenced comparator from TLV3801 to TLV3601 in the *Application Information* and *Power-Down Mode (Multiplexer Mode)* sections.......... 15
- Updated Figure 7-8, *LMH34400 Output Voltage* 19

Changes from Revision A (August 2022) to Revision B (March 2023) **Page**

- Added the *Typical Application*, *Design Requirements*, and *Detailed Design Procedure* sections.......... 18

Changes from Revision * (March 2022) to Revision A (August 2022) **Page**

- データシートのステータスを以下のように変更:「事前情報」から *「量産データ」* 1

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LMH34400IDRLR	Active	Production	SOT-5X3 (DRL) | 6	4000 | LARGE T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	1M5
LMH34400IDRLR.B	Active	Production	SOT-5X3 (DRL) | 6	4000 | LARGE T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	1M5

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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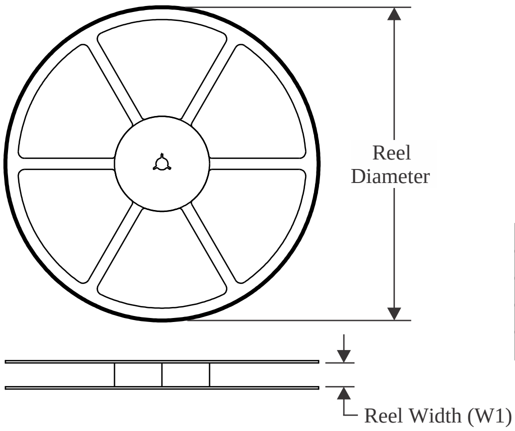
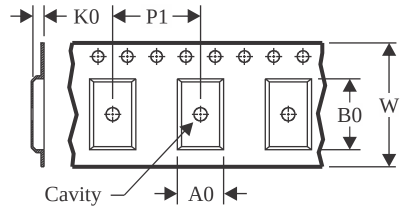
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

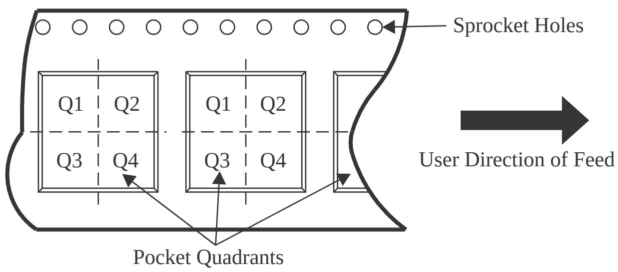


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

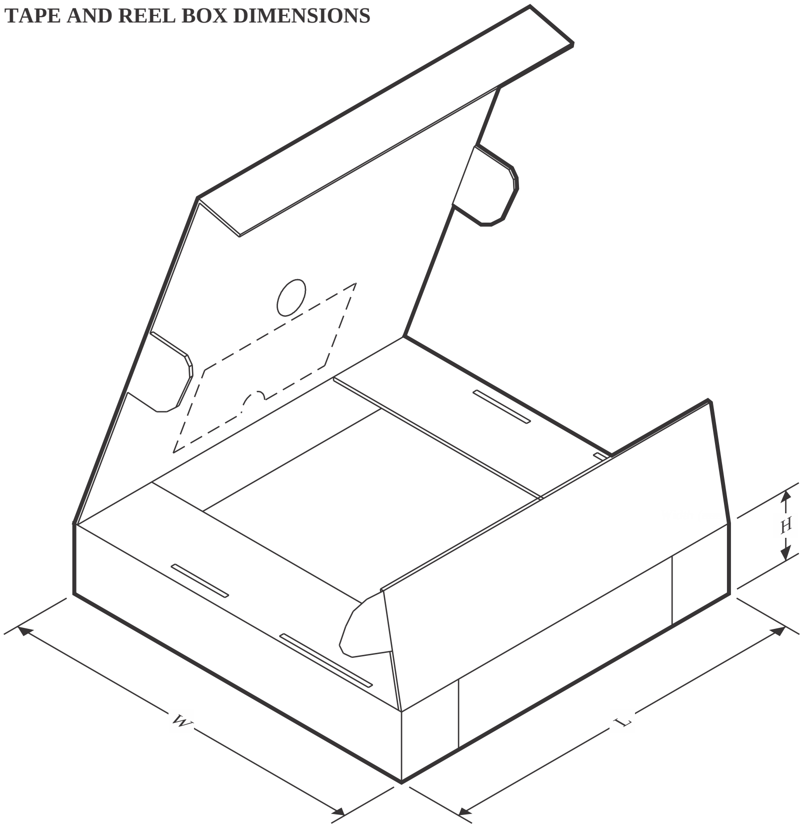
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

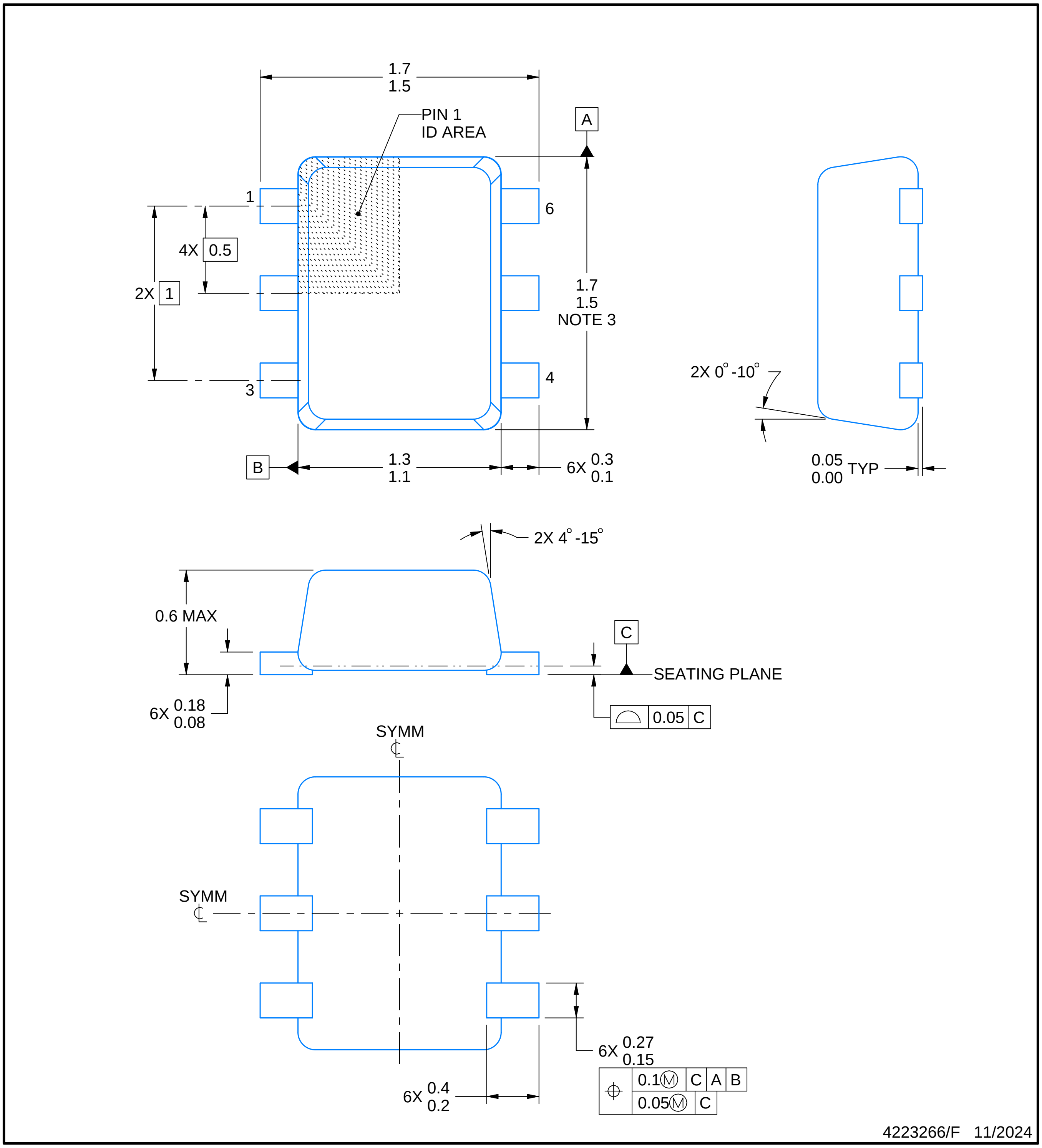
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMH34400IDRLR	SOT-5X3	DRL	6	4000	180.0	8.4	1.98	1.78	0.69	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



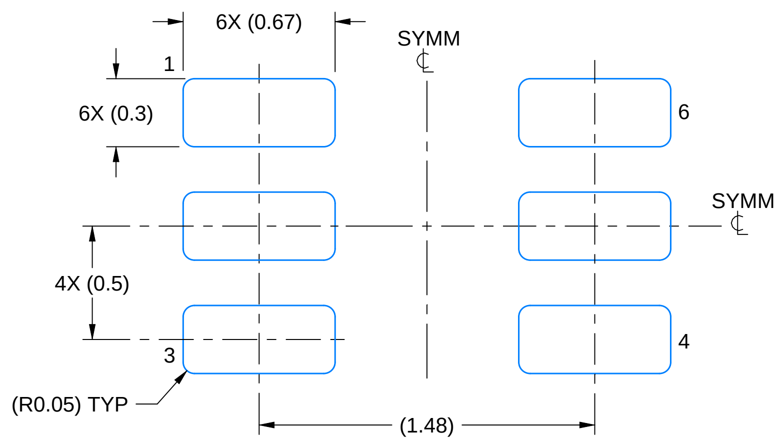
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMH34400IDRLR	SOT-5X3	DRL	6	4000	202.0	201.0	28.0

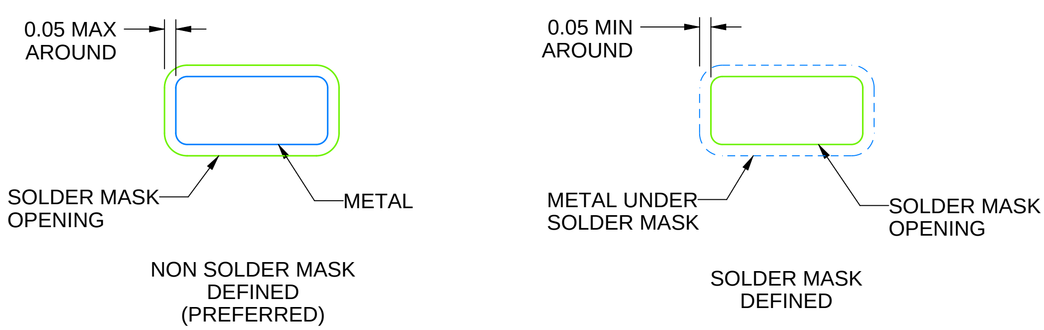


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-293 Variation UAAD



LAND PATTERN EXAMPLE
SCALE:30X

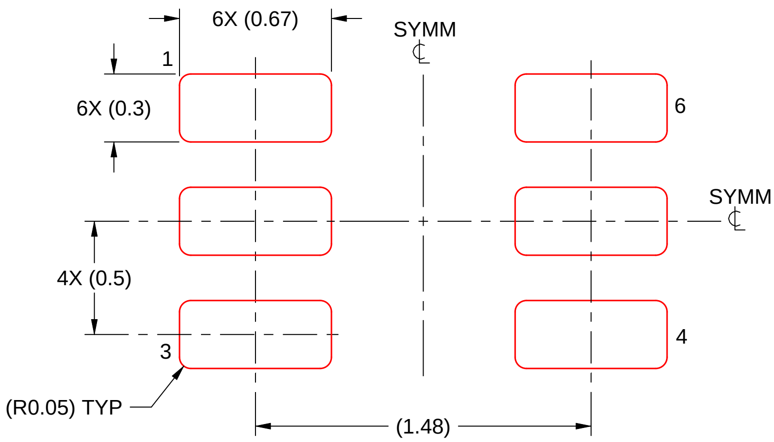


SOLDERMASK DETAILS

4223266/F 11/2024

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
7. Land pattern design aligns to IPC-610, Bottom Termination Component (BTC) solder joint inspection criteria.



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:30X

4223266/F 11/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

重要なお知らせと免責事項