LMH5401 8GHz、低ノイズ、低消費電力の完全差動アンプ

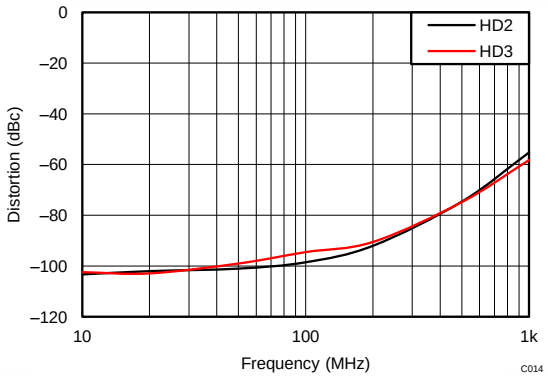
1 特長

- ゲイン帯域幅積(GBP): 8GHz
- 優れた直線性:
  DC～2GHz、G＝12dB
- スルーレート: 17,500V/µs
- HD2/HD3歪みが小さい
  ($1V_{PP}$、200Ω、DE-DE、G＝12dB):
  - 100MHz: HD2で－104dBc、HD3で－96dBc
  - 200MHz: HD2で－95dBc、HD3で－92dBc
  - 500MHz: HD2で－80dBc、HD3で－77dBc
  - 1GHz: HD2で－64dBc、HD3で－58dBc
- IMD2/IMD3歪みが小さい
  ($2V_{PP}$、200Ω、DE-DE、G＝12dB):
  - 200MHz: IMD2で－96dBc、IMD3で－95dBc
  - 500MHz: IMD2で－80dBc、IMD3で－83dBc
  - 1GHz: IMD2で－70dBc、IMD3で－63dBc
- 入力電圧ノイズ: 1.25nV/√Hz
- 入力電流ノイズ: 3.5pA/√Hz
- シングルとデュアルの電源による動作をサポート
- 消費電力: 55mA
- パワーダウン機能

2 アプリケーション

- GSPS ADCドライバ
- 高速データ収集用ADCドライバ
- 1GBPS Ethernet over Microwave用ADCドライバ
- DACバッファ
- IF、RF、ベースバンド・ゲイン・ブロック
- SAWフィルタ・バッファおよびドライバ
- DCから2GHzまでのバランの代替
- レベル・シフタ

歪みと周波数との関係
(G＝12dB、SE-DE、R_L＝200Ω、V_{PP}＝2V)



3 概要

LMH5401は、無線周波数(RF)や中間周波数(IF)のアプリケーション、または高速なDC結合の時間領域アプリケーションに対して最適化された、極めて高性能な差動アンプです。アナログ/デジタル・コンバータ(ADC)の駆動時に、シングルエンドから差動への(SE-DE)変換を要するDCまたはAC結合アプリケーションに最適であり、SE-DEまたは差動-差動(DE-DE)モードでの動作時に生じる2次/3次歪みを非常に小さく抑えることができます。

LMH5401は、SE-DEシステムとDE-DEシステムのいずれにも最適化されており、DC～2GHzというかつてない使用可能帯域幅を実現しています。LMH5401を使用すれば、試験/測定機器やブロードバンド通信、高速データ収集などの幅広いアプリケーションにおいて、外部バランなしで信号チェーンのSE-DE変換が可能になります。

同相基準入力ピンを使用して、アンプの出力同相をADCの入力要件に合わせることができるほか、3.3V～5Vの電源を選択可能で、必要であればデュアル電源での動作にも対応します。またパワーダウン機能を利用して、消費電力を削減することも可能です。

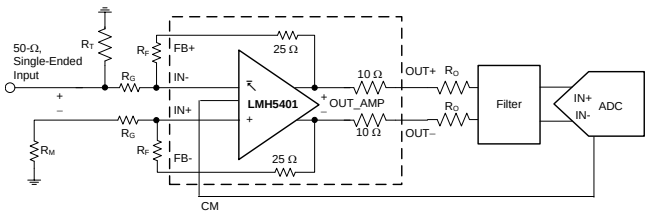
5V電源を使用した場合には、275mWという非常に低い消費電力で優れた性能を提供します。高性能を実現するLMH5401は、テキサス・インスツルメンツの先進的な相補型BiCMOSプロセスで製造され、省スペース型のUQFN-14パッケージで供給されます。

製品情報(1)

型番	パッケージ	本体サイズ
LMH5401	UQFN (14)	2.50mm×2.50mm

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。

ADC12J4000を駆動するLMH5401



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4 改訂履歴

Revision C (October 2017) から **Revision D** に変更 **Page**

- Added table note to *Pin Functions* table to distinguish pin types ... 4
- Changed GND and PD pin descriptions in *Pin Functions* table ... 4
- Changed VOUT_AMP value from 2 V_{PP} to 1 V_{PP} in condition statement of *HD2 and HD3* curve ... 15
- Changed VOUT_AMP value from 2 V_{PP} to 1 V_{PP} in condition statement of *HD2 and HD3 Differential* curve ... 16
- Changed VOUT_AMP value from 2 V_{PP} to 1 V_{PP} in condition statement of *HD2 and HD3 vs Output Voltage* curve ... 16
- Changed VOUT_AMP value from 2 V_{PP} to 1 V_{PP} in condition statement of *HD2 and HD3 vs Input Common-Mode Voltage* curve ... 16
- Changed VOUT_AMP value from 2 V_{PP} to 1 V_{PP} in condition statement of *HD2 and HD3 vs Output Common-Mode Voltage* curve ... 16
- Corrected and deleted note from *Functional Block Diagram* ... 24
- Added *Power Down and Ground Pins* subsection to *Feature Description* section ... 25

Revision B (January 2015) から **Revision C** に変更 **Page**

- Added Input, V_{IO}, I_{IB}, and I_{IO} parameters to 5-V *Electrical Characteristics* table ... 6
- Changed R_T and R_{G2} values in first row of Table 2 ... 21
- Changed *Functional Block Diagram* graphic ... 24
- Changed *Device Comparison Table* to be a separate sub-section within *Feature Description* section ... 30
- Added *Driving Unmatched Loads For Lower Loss* section ... 36

- Changed *8 MHz* to *8 GHz* in first sentence of *Layout Guidelines* section 45

Revision A (October 2014) から Revision B に変更 **Page**

- 「概要」セクションの第1文に*DC結合*を追加 1
- 「概要」セクションの第2段落第2文を変更 1
- Updated ESD Ratings table to current standards 5
- Changed AC Performance, *IMD3* and *IMD2* parameter test conditions in 5-V Electrical Characteristics table 6
- Changed Input, V_{ICL} parameter maximum specification in 5-V Electrical Characteristics table 6
- Changed Input, V_{ICL} parameter maximum specification in 3.3-V Electrical Characteristics table 8
- Changed Output, V_{OCRH} parameter test condition from *Output voltage range low* to T_A = *–40°C to 85°C* in 3.3-V Electrical Characteristics table 9
- Changed Typical Characteristics curves: updated color scheme, grammatical edits throughout curves 10
- Added *Large-Signal* to title of Figure 2, Figure 4, and Figure 6 10
- Added *Large-Signal* to title of Figure 8 10
- Changed *Differential-Ended* to *Differential* in title of Figure 11 10
- Added *Large-Signal* to titles of Figure 30, Figure 32, and Figure 34 15
- Added *Large-Signal* to title of Figure 36 15
- Changed correction to reduction in second paragraph of *Output Reference Points* section 20
- Changed header for last column in Table 1 21
- ChangedFigure 56 through Figure 59: modifications to figures, added A_V = *4 V/V* to titles 22
- Deleted last sentence from first paragraph of the *Fully-Differential Amplifier* section 25
- Changed *1.2 V* to *the specified minimum voltage* in the third paragraph of the *Fully-Differential Amplifier* section 25
- Added sixth sentence stating the feedback path must always be DC-coupled to the *AC-Coupled Signal Path Considerations* section 25
- Added A_V = *4 V/V* to title of Figure 62 30
- Deleted example from the *Operation with a Single Supply* section 31
- Added *Stability* section 32
- Changed *15 dB* to *19 dB* in third paragraph of *SFDR Considerations* section 38
- Added Figure 75 to the *Active Balun* section 42

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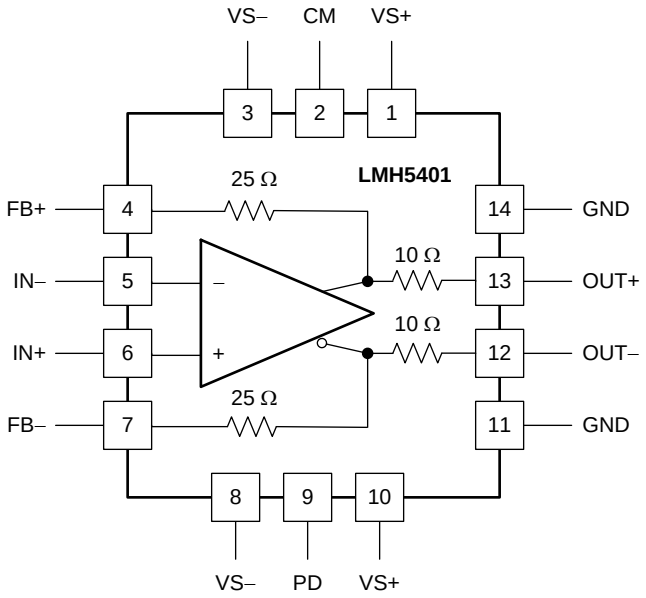
- Changed Output Common-Mode Control Pin, V_{CM} *voltage range low* and *high* parameter typical specifications in 5-V Electrical Characteristics 7
- Changed Output Common-Mode Control Pin, V_{CM} *voltage range low* and *high* parameter specifications in 3.3-V Electrical Characteristics table 9

5 Pin Configuration and Functions

RMS Package
14-Pin UQFN
Top View



Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
CM	2	I	Input pin to set amplifier output common-mode voltage
FB–	7	O	Negative output feedback component connection
FB+	4	O	Positive output feedback component connection
GND	11, 14	P	Power down ground. See Power Down and Ground Pins
IN–	5	I	Negative input pin
IN+	6	I	Positive input pin
OUT–	12	O	Negative output pin
OUT+	13	O	Positive output pin
PD	9	I	Power-down (logic 1 = power down). See Power Down and Ground Pins
VS–	3, 8	P	Negative supply voltage
VS+	1, 10	P	Positive supply voltage

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

	MIN	MAX	UNIT
Power supply		5.5	V
Input voltage range	(VS–) – 0.7	(VS+) + 0.7	V
Input current		10	mA
Output current (sourcing or sinking) OUT+, OUT–		100	mA
Continuous power dissipation	See *Thermal Information* table		
Maximum junction temperature, T_J		150	°C
Maximum junction temperature, continuous operation, long-term reliability		125	°C
Operating free-air temperature, T_A	–40	85	°C
Storage temperature, T_{stg}	–40	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±3500	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	NOM	MAX	UNIT
Supply voltage (V_S = VS+ – VS–)	3.15	5	5.25	V
Operating junction temperature, T_J	–40		125	°C
Ambient operating air temperature, T_A	–40	25	85	°C

6.4 Thermal Information

THERMAL METRIC(1)		LMH5401 RMS (UQFN) 14 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	101	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	51	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	61	°C/W
ψ_{JT}	Junction-to-top characterization parameter	4.2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	61	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics: V_S = 5 V

at T_A = 25°C, VS+ = 2.5 V, VS– = –2.5 V, V_{CM} = 0 V, R_L = 200-Ω differential, G = 12 dB (4 V/V), single-ended input, differential output, and R_S = 50 Ω, (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT	TEST LEVEL(2)
AC PERFORMANCE							
GBP	Gain bandwidth product	G = 30 dB (32 V/V)		8		GHz	C
SSBW	Small-signal, –3-dB bandwidth	V_O = 200 mV_{PP}		6.2		GHz	C
LSBW	Large-signal, –3-dB bandwidth	V_O = 2 V_{PP}		4.8		GHz	C
	Bandwidth for 0.1-dB flatness	V_O = 2 V_{PP}		800		MHz	C
SR	Slew rate	2-V step		17500		V/µs	C
	Rise and fall time	1-V step, 10% to 90%		80		ps	C
	Overdrive recovery	Overdrive = ±0.5 V		300		ps	C
	Output balance error	f = 1 GHz		47		dBc	C
z_o	Output impedance	At DC, differential	16	20	24	Ω	A
	0.1% settling time	2 V, R_L = 200 Ω		1		ns	C
HD2	Second-order harmonic distortion	f = 100 MHz, V_O = 2 V_{PP}		–99		dBc	C
		f = 200 MHz, V_O = 2 V_{PP}		–92		dBc	C
		f = 500 MHz, V_O = 2 V_{PP}		–75		dBc	C
		f = 1 GHz, V_O = 2 V_{PP}		–56		dBc	C
HD3	Third-order harmonic distortion	f = 100 MHz, V_O = 2 V_{PP}		–94		dBc	C
		f = 200 MHz, V_O = 2 V_{PP}		–90		dBc	C
		f = 500 MHz, V_O = 2 V_{PP}		–75		dBc	C
		f = 1 GHz, V_O = 2 V_{PP}		–58		dBc	C
IMD3	Third-order intermodulation	f = 100 MHz, V_O = 1 V_{PP} per tone		–95		dBc	C
		f = 200 MHz, V_O = 1 V_{PP} per tone		–91		dBc	C
		f = 500 MHz, V_O = 1 V_{PP} per tone		–75		dBc	C
		f = 1 GHz, V_O = 1 V_{PP} per tone		–60		dBc	C
IMD2	Second-order intermodulation	f = 100 MHz, V_O = 1 V_{PP} per tone		–95		dBc	C
		f = 200 MHz, V_O = 1 V_{PP} per tone		–89		dBc	C
		f = 500 MHz, V_O = 1 V_{PP} per tone		–71		dBc	C
		f = 1 GHz, V_O = 1 V_{PP} per tone		–52		dBc	C
NOISE PERFORMANCE							
e_n	Input voltage noise density			1.25		nV/√Hz	C
i_n	Input noise current			3.5		pA/√Hz	C
NF	Noise figure	R_S = 50 Ω, SE-DE, 200 MHz (see Figure 59)		9.6		dB	C
INPUT							
V_{OS}	Input offset voltage			±0.5	±5	mV	A
I_B	Input bias current			70	150	µA	A
I_{OS}	Input offset current			±1	±10	µA	A
	Differential resistance	Open-loop		4600		Ω	C
V_{ICL}	Input common-mode low voltage			VS–	(VS–) + 0.41	V	A
V_{ICH}	Input common-mode high voltage		(VS+) – 1.41	(VS+) – 1.2		V	A
CMRR	Common-mode rejection ratio	Differential, 1-V_{PP} input shift, DC		72		dBc	C

(1) The input resistance and corresponding gain are obtained with the external resistance added.
(2) Test levels: (A) 100% tested at 25°C. Overtemperature limits by characterization and simulation. (B) Limits set by characterization and simulation. (C) Typical value only for information.

Electrical Characteristics: V_S = 5 V (continued)

at T_A = 25°C, VS+ = 2.5 V, VS– = –2.5 V, V_{CM} = 0 V, R_L = 200-Ω differential, G = 12 dB (4 V/V), single-ended input, differential output, and R_S = 50 Ω, (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT	TEST LEVEL(2)
OUTPUT								
V_{OCRH}	Output voltage range, high	Measured single-ended	T_A = 25°C	(VS+) – 1.3	(VS+) – 1.1		V	A
			T_A = –40°C to +85°C		(VS+) – 1.2		V	C
V_{OCRL}	Output voltage range, low	Measured single-ended	T_A = 25°C	(VS–) + 1.3	(VS–) + 1.1		V	A
			T_A = –40°C to +85°C		(VS–) + 1.2		V	C
V_{OD}	Differential output voltage swing	Differential			5.8		V_{PP}	C
I_{OD}	Differential output current	V_O = 0 V(3)		40	50		mA	A
POWER SUPPLY								
V_S	Supply voltage			3.15		5.25	V	A
PSRR	Power-supply rejection ratio	VS–		–50	–80		dB	A
		VS+		–60	–82		dB	A
I_Q	Quiescent current	Power down = 0		50	55	62	mA	A
		Power down = 1		1	3	6	mA	A
OUTPUT COMMON-MODE CONTROL PIN (V_{CM})								
SSBW	Small-signal bandwidth	V_{OCM} = 100 mV_{PP}			1.2		GHz	C
	V_{CM} slew rate	V_{OCM} = 500 mV_{PP}			2900		V/µs	C
	V_{CM} voltage range low	Differential gain shift < 1 dB			(VS–) + 1.4	(VS–) + 2	V	A
	V_{CM} voltage range high	Differential gain shift < 1 dB		(VS+) – 2	(VS+) – 1.4		V	A
	V_{CM} gain	V_{CM} = 0 V		0.98	1	1.01	V/V	A
	V_{OCM} output common-mode offset from V_{CM} input voltage	V_{CM} = 0 V			–27		mV	C
V_{OCM}	Common-mode offset voltage	Output-referred			0.4		mV	A
POWER DOWN (PD PIN)								
V_T	Enable or disable voltage threshold	Device powers on below 0.8 V Device powers down above 1.2 V		0.9	1.1	1.2	V	A
	Power down quiescent current			1	3	6	mA	A
	Power down bias current	Power down = 2.5 V			10	±100	µA	C
	Turnon time delay	Time to V_O = 90% of final value			10		ns	C
	Turnoff time delay	Time to V_O = 10% of original value			10		ns	C

(3) This test shorts the outputs to ground (midsupply) then sources or sinks 60 mA and measures the deviation from the initial condition.

6.6 Electrical Characteristics: V_S = 3.3 V

at T_A = 25°C, VS+ = 1.65 V, VS– = –1.65 V, V_{CM} = 0 V, R_L = 200-Ω differential, G = 12 dB (4 V/V), single-ended input and differential output, and input and output referenced to midsupply, (unless otherwise noted.) Measured using an EVM as discussed in the *Parameter Measurement Information* section.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT	TEST LEVEL(1)
AC PERFORMANCE							
GBP	Gain bandwidth product	G = 30 dB (32 V/V)		8		MHz	C
SSBW	Small-signal, –3-dB bandwidth	V_O = 200 mV_{PP}		6		GHz	C
LSBW	Large-signal, –3-dB bandwidth	V_O = 2 V_{PP}		4.4		GHz	C
	Bandwidth for 0.1-dB flatness	V_O = 2 V_{PP}		700		MHz	C
SR	Slew rate	2-V step		17500		V/µs	C
	Rise and fall time	1-V step, 10% to 90%		90		ps	C
	Overdrive recovery	Overdrive = ±0.5 V		400		ps	C
	Output balance error	f = 1 GHz		47		dBc	C
z_o	Output impedance	At DC	16	20	24	Ω	A
	0.1% settling time	2 V, R_L = 200 Ω		1		ns	C
HD2	Second-order harmonic distortion	f = 100 MHz, V_O = 1 V_{PP}		–100		dBc	C
		f = 200 MHz, V_O = 1 V_{PP}		–94		dBc	C
		f = 500 MHz, V_O = 1 V_{PP}		–78.5		dBc	C
		f = 1 GHz, V_O = 1 V_{PP}		–58		dBc	C
HD3	Third-order harmonic distortion	f = 100 MHz, V_O = 1 V_{PP}		–86		dBc	C
		f = 200 MHz, V_O = 1 V_{PP}		–78		dBc	C
		f = 500 MHz, V_O = 1 V_{PP}		–64		dBc	C
		f = 1 GHz, V_O = 1 V_{PP}		–52		dBc	C
IMD2	Second-order intermodulation distortion	f = 100 MHz, V_O = 0.5 V_{PP} per tone		–95		dBc	C
		f = 200 MHz, V_O = 0.5 V_{PP} per tone		–95		dBc	C
		f = 500 MHz, V_O = 0.5 V_{PP} per tone		–81		dBc	C
		f = 1 GHz, V_O = 0.5 V_{PP} per tone		–66		dBc	C
IMD3	Third-order intermodulation distortion	f = 100 MHz, V_O = 0.5 V_{PP} per tone		–101		dBc	C
		f = 200 MHz, V_O = 0.5 V_{PP} per tone		–95		dBc	C
		f = 500 MHz, V_O = 0.5 V_{PP} per tone		–82		dBc	C
		f = 1 GHz, V_O = 0.5 V_{PP} per tone		–66		dBc	C
NOISE PERFORMANCE							
e_n	Input voltage noise density			1.25		nV/√Hz	C
i_n	Input noise current			3.5		pA/√Hz	C
NF	Noise figure	R_S = 50 Ω, SE-DE, G = 12 dB, 200 MHz		9.6		dB	C
INPUT							
Z_{id}	Differential impedance			4600		Ω	C
V_{ICL}	Input common-mode low voltage			(VS–)	(VS–) + 0.41	V	A
V_{ICH}	Input common-mode high voltage		(VS+) – 1.41	(VS+) – 1.2		V	A
CMRR	Common-mode rejection ratio	Differential, 1-V_{PP} input shift, DC		–72		dBc	C

(1) Test levels: (A) 100% tested at 25°C. Overtemperature limits by characterization and simulation. (B) Limits set by characterization and simulation. (C) Typical value only for information.

Electrical Characteristics: V_S = 3.3 V (continued)

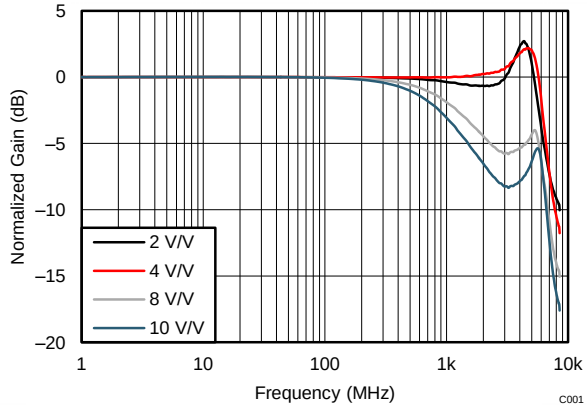
at T_A = 25°C, VS+ = 1.65 V, VS– = –1.65 V, V_{CM} = 0 V, R_L = 200-Ω differential, G = 12 dB (4 V/V), single-ended input and differential output, and input and output referenced to midsupply, (unless otherwise noted.) Measured using an EVM as discussed in the *Parameter Measurement Information* section.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT	TEST LEVEL (1)
OUTPUT								
V_{OCRH}	Output voltage range, high	Measured single-ended	T_A = 25°C	(VS+) – 1.3	(VS+) – 1.1		V	A
			T_A = –40°C to +85°C		(VS+) – 1.2		V	C
V_{OCRL}	Output voltage range, low	Measured single-ended	T_A = 25°C	(VS–) + 1.3	(VS–) + 1.1		V	A
			T_A = –40°C to +85°C		(VS–) + 1.2		V	C
V_{OD}	Differential output voltage swing	Differential			2.8		V_{PP}	C
I_{OD}	Differential output current	V_O = 0 V (2)		30	40		mA	A
POWER SUPPLY								
V_S	Supply voltage			3.15		5.25	V	A
PSRR	Power-supply rejection ratio	VS–		–50	–80		dB	A
		VS+		–60	–84		dB	A
I_Q	Quiescent current	Power down = 0		49	54	62	mA	A
		Power down = 1		1	1.6	5	mA	A
OUTPUT COMMON-MODE CONTROL PIN (V_{CM})								
SSBW	Small-signal bandwidth	V_{OCM} = 200 mV_{PP}			3		GHz	C
	V_{CM} voltage range low	Differential gain shift < 1 dB			(VS–) + 1.35	(VS–) + 1.55	V	A
	V_{CM} voltage range high	Differential gain shift < 1 dB		(VS+) – 1.55	(VS+) – 1.35		V	A
	V_{CM} gain	V_{CM} = 0 V		0.98	1	1.01	V/V	A
	V_{OCM} output common-mode offset from V_{CM} input voltage	V_{CM} = 0 V			–27		mV	C
V_{OCM}	Common-mode offset voltage	Output-referred			0.4		mV	A
POWER DOWN (PD PIN)								
V_T	Enable or disable voltage threshold	Device powers on below 0.8 V, device powers down above 1.2 V		0.9	1.1	1.2	V	A
	Power down quiescent current			1	3	6	mA	A
	Power down bias current	Power down = 2.5 V			10	±100	µA	C
	Turnon time delay	Time to V_O = 90% of final value			10		ns	C
	Turnoff time delay	Time to V_O = 10% of original value			10		ns	C

(2) This test shorts the outputs to ground (midsupply) then sources or sinks 60 mA and measures the deviation from the initial condition.

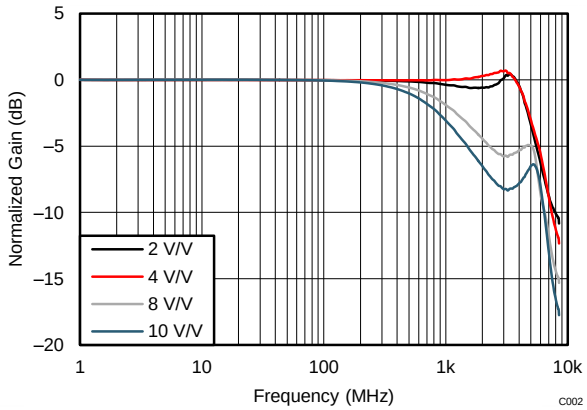
6.7 Typical Characteristics: 5 V

at T_A = 25°C, split supplies, V_{CM} = 0 V, R_L = 200-Ω differential (R_O = 40 Ω each), G = 12 dB (4 V/V), single-ended input and differential output, and input and output pins referenced to midsupply, (unless otherwise noted.) Measured using an EVM as discussed in the *Parameter Measurement Information* section (see Figure 56 to Figure 59).



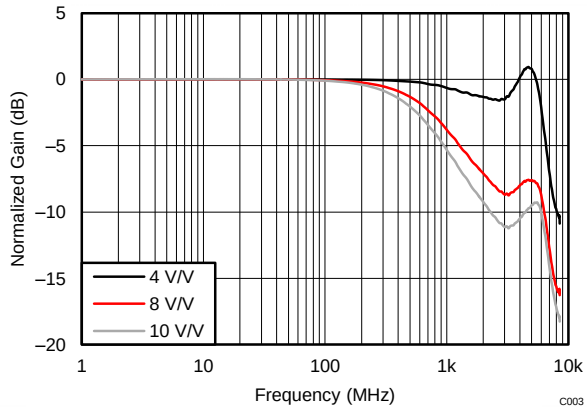
V_S = ±2.5 V, VOUT_AMP = 0.2 V_{PP}, R_L = 200 Ω

Figure 1. Small-Signal Frequency Response vs Gain



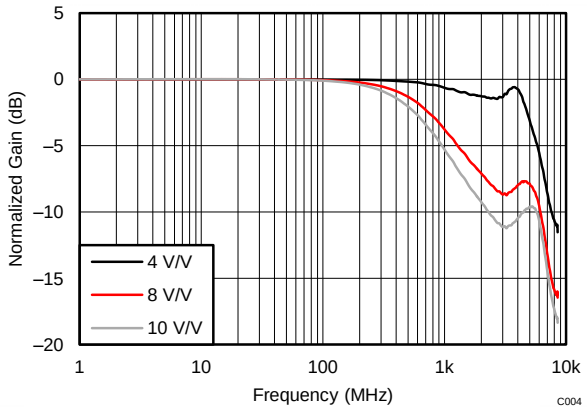
VOUT_AMP = 2 V_{PP}, R_L = 200 Ω

Figure 2. Large-Signal Frequency Response vs Gain



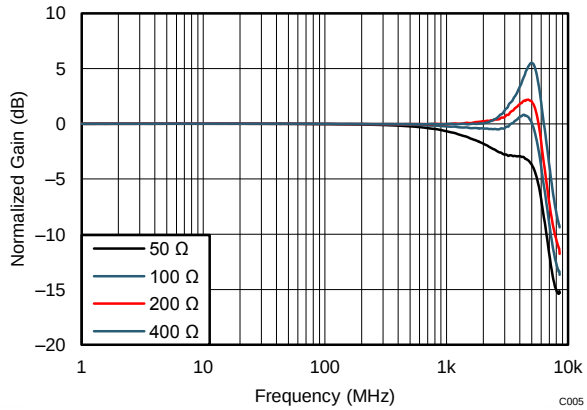
VOUT_AMP = 0.2 V_{PP}, R_L = 200 Ω

Figure 3. Differential Input Small-Signal Frequency Response vs Gain



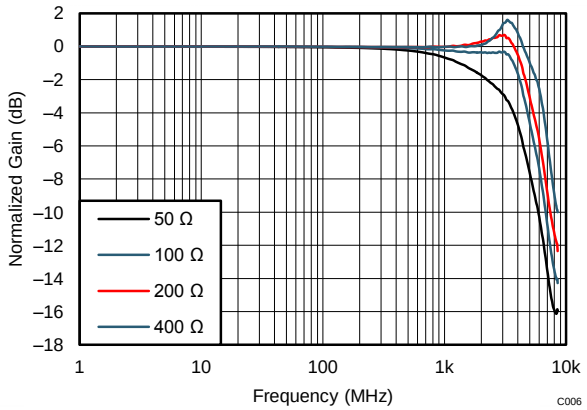
VOUT_AMP = 2 V_{PP}, R_L = 200 Ω

Figure 4. Differential Input Large-Signal Frequency Response vs Gain



V_S = ±2.5 V, VOUT_AMP = 2 V_{PP}, G = 12 dB, SE-DE

Figure 5. Small-Signal Frequency Response vs Load

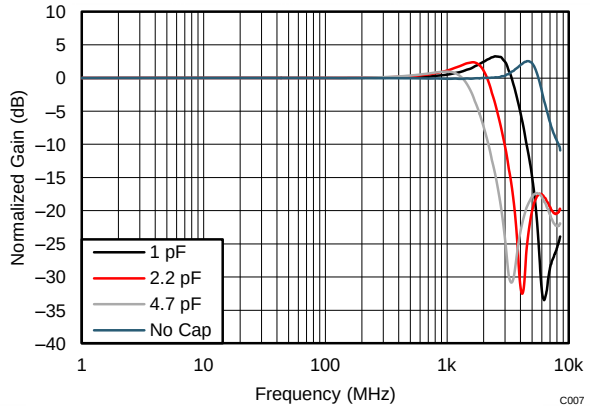


V_S = ±2.5 V, VOUT_AMP = 2 V_{PP}, G = 12 dB, SE-DE

Figure 6. Large-Signal Frequency Response vs Load

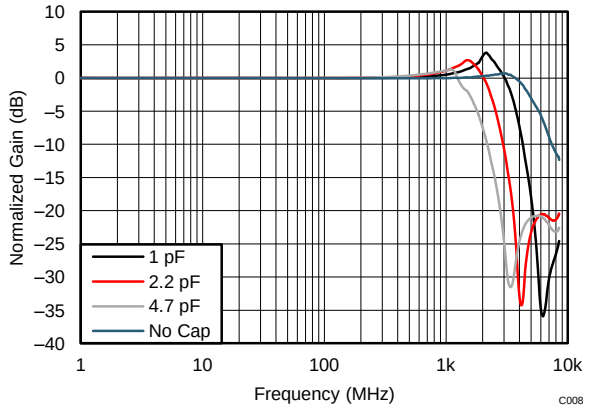
Typical Characteristics: 5 V (continued)

at T_A = 25°C, split supplies, V_{CM} = 0 V, R_L = 200-Ω differential (R_O = 40 Ω each), G = 12 dB (4 V/V), single-ended input and differential output, and input and output pins referenced to midsupply, (unless otherwise noted.) Measured using an EVM as discussed in the *Parameter Measurement Information* section (see Figure 56 to Figure 59).



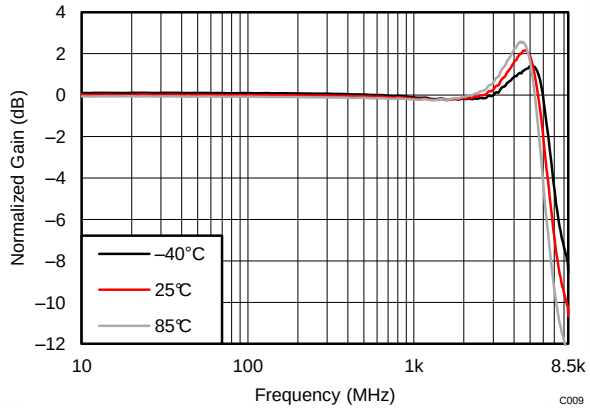
V_S = ±2.5 V, VOUT_AMP = 0.2 V_{PP}, capacitance at DUT output pins, G = 12 dB, SE-DE

Figure 7. Small-Signal Frequency Response vs Capacitive Load



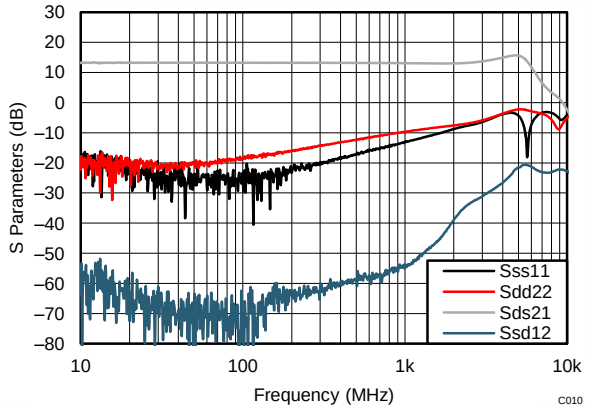
V_S = ±2.5 V, VOUT_AMP = 2 V_{PP}, capacitance at DUT output pins, G = 12 dB, SE-DE

Figure 8. Large-Signal Frequency Response vs Capacitive Load



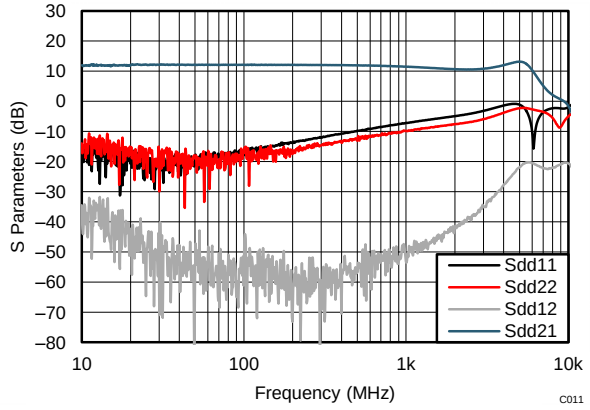
V_S = ±2.5 V, VOUT_AMP = 2 V_{PP}, G = 12 dB, SE-DE

Figure 9. Bandwidth vs Temperature



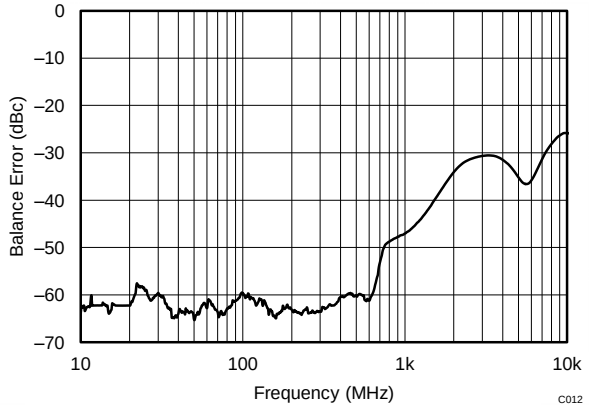
V_S = ±2.5 V, VOUT_AMP = 200 mV_{PP}, ±2.5-V supply

Figure 10. S-Parameters Single-Ended Input



V_S = ±2.5 V, VOUT_AMP = 200 mV_{PP}

Figure 11. S-Parameters Differential Input (±2.5-V Supply)

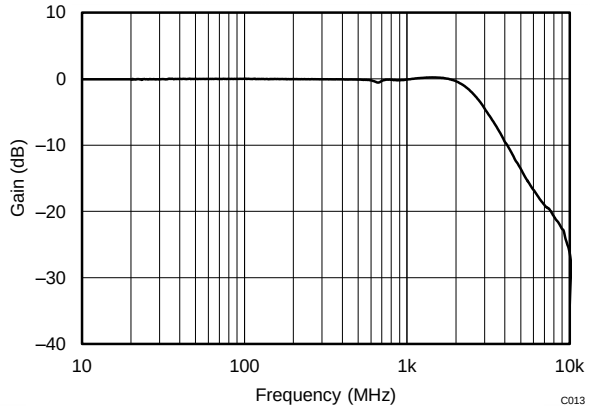


V_S = ±2.5 V, VOUT_AMP = 200 mV_{PP}

Figure 12. Balance Error

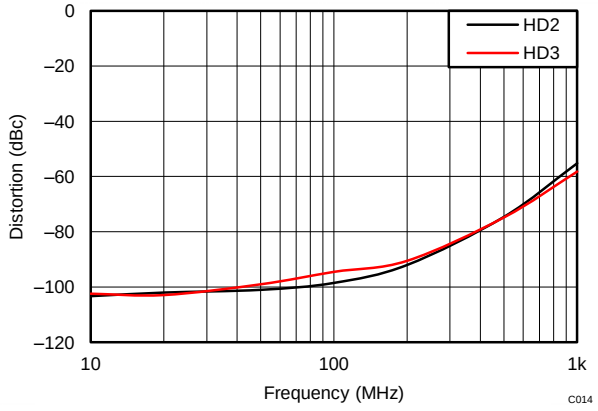
Typical Characteristics: 5 V (continued)

at T_A = 25°C, split supplies, V_{CM} = 0 V, R_L = 200-Ω differential (R_O = 40 Ω each), G = 12 dB (4 V/V), single-ended input and differential output, and input and output pins referenced to midsupply, (unless otherwise noted.) Measured using an EVM as discussed in the *Parameter Measurement Information* section (see Figure 56 to Figure 59).



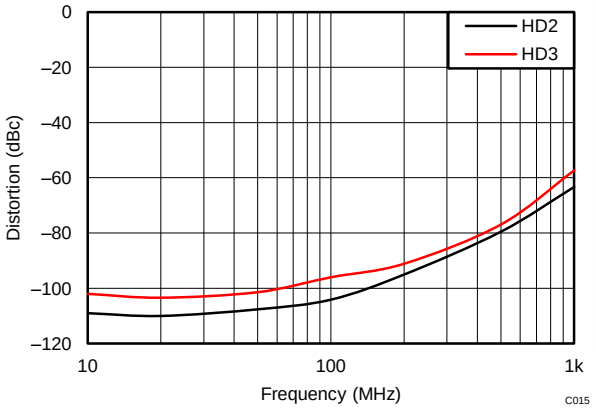
V_S = ±2.5 V, VOUT_AMP = 200 mV_{PP}

Figure 13. Common-Mode Frequency Response



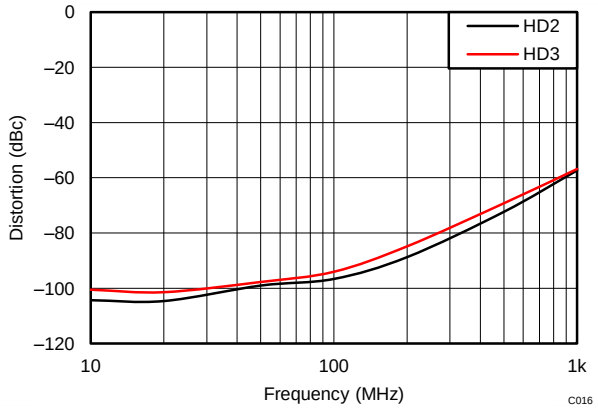
V_S = ±2.5 V, VOUT_AMP = 2 V_{PP}, SE-DE, R_L = 200 Ω

Figure 14. HD2 and HD3 vs Frequency



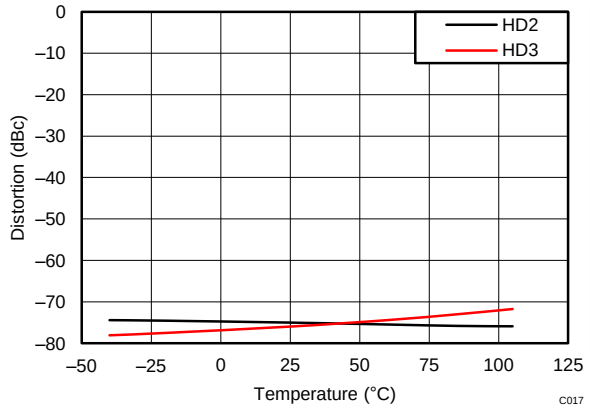
V_S = ±2.5 V, VOUT_AMP = 2 V_{PP}
(Differential to Differential, R_L = 200 Ω)

Figure 15. HD2 and HD3 vs Frequency



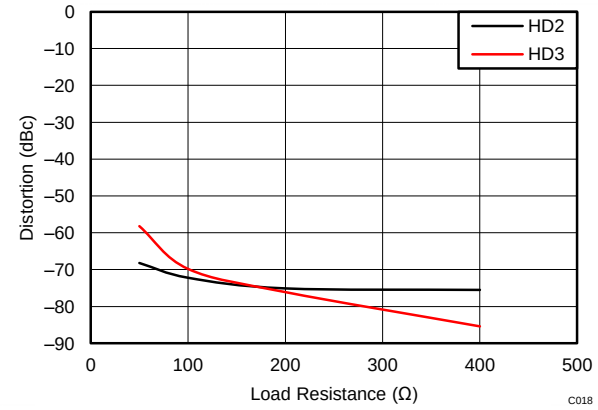
V_S = ±2.5 V, VOUT_AMP = 2 V_{PP}, (SE-DE, R_L = 100 Ω)

Figure 16. HD2 and HD3 vs Frequency



V_S = ±2.5 V, VOUT_AMP = 2 V_{PP}, R_L = 200 Ω, f = 500 MHz

Figure 17. HD2 and HD3 vs Temperature

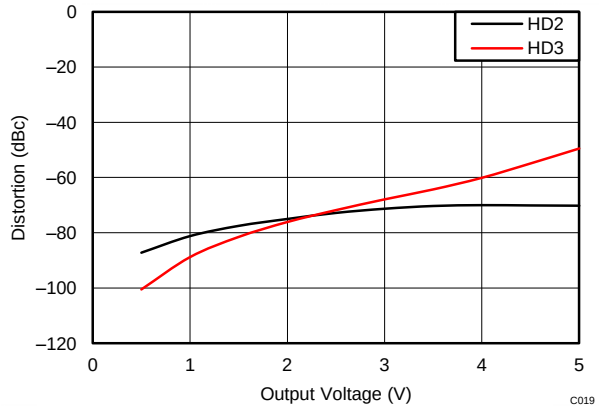


V_S = ±2.5 V, VOUT_AMP = 2 V_{PP}, f = 500 MHz

Figure 18. HD2 and HD3 vs Load Resistance

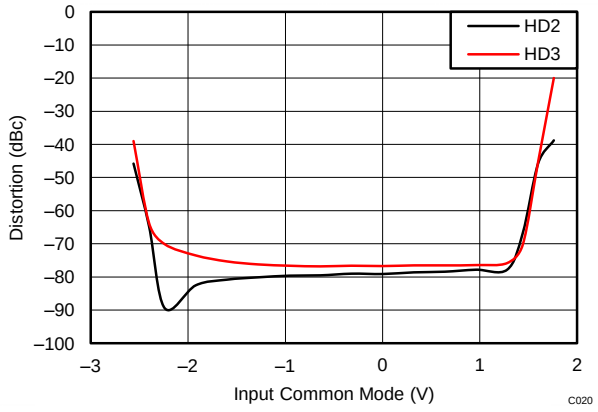
Typical Characteristics: 5 V (continued)

at T_A = 25°C, split supplies, V_{CM} = 0 V, R_L = 200-Ω differential (R_O = 40 Ω each), G = 12 dB (4 V/V), single-ended input and differential output, and input and output pins referenced to midsupply, (unless otherwise noted.) Measured using an EVM as discussed in the *Parameter Measurement Information* section (see Figure 56 to Figure 59).



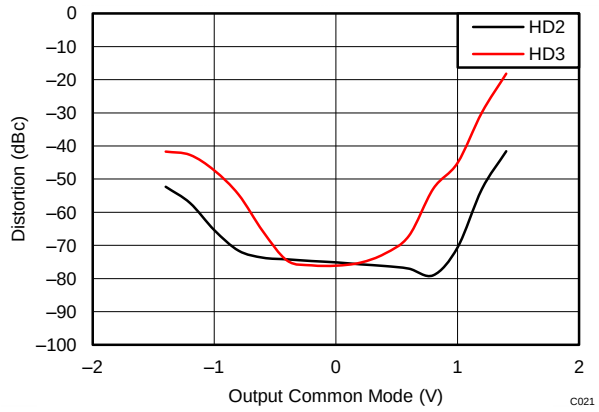
V_S = ±2.5 V, f = 500 MHz

Figure 19. HD2 and HD3 vs Output Voltage



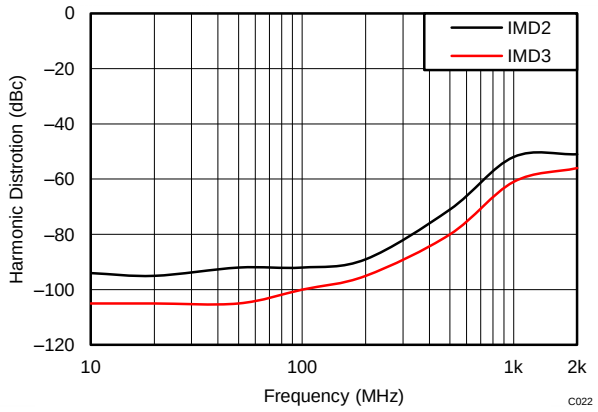
V_S = ±2.5 V, VOUT_AMP = 2 V_{PP}, f = 500 MHz

Figure 20. HD2 and HD3 vs Input Common-Mode Voltage



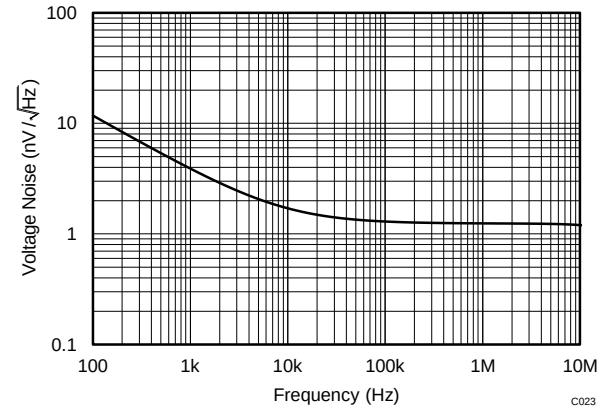
V_S = ±2.5 V, f = 500 MHz , VOUT_AMP = 2 V_{PP}

Figure 21. HD2 and HD3 vs Output Common-Mode Voltage



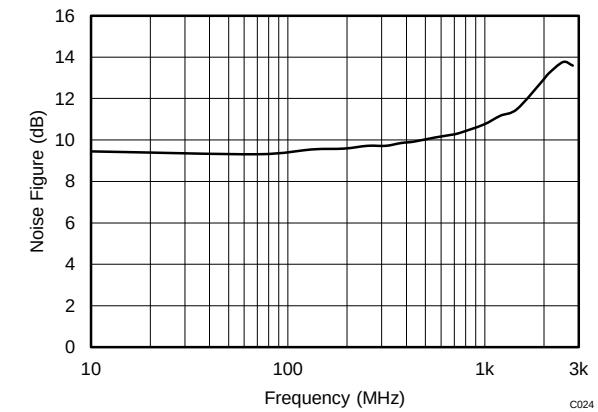
V_S = ±2.5 V, VOUT_AMP = 1 V_{PP} per tone

Figure 22. Intermodulation vs Frequency



V_S = ±2.5 V

Figure 23. Input-Referred Voltage Noise

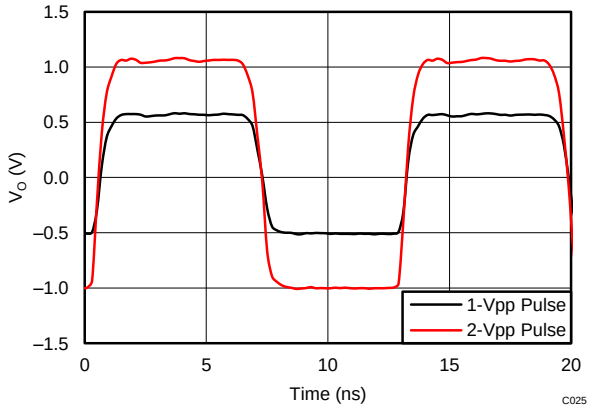


V_S = ±2.5 V

Figure 24. Noise Figure vs Frequency

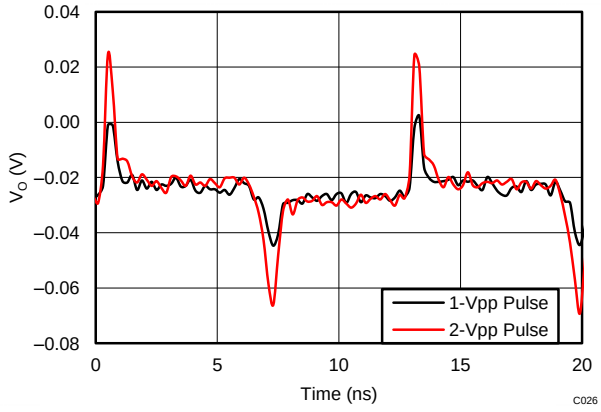
Typical Characteristics: 5 V (continued)

at T_A = 25°C, split supplies, V_{CM} = 0 V, R_L = 200-Ω differential (R_O = 40 Ω each), G = 12 dB (4 V/V), single-ended input and differential output, and input and output pins referenced to midsupply, (unless otherwise noted.) Measured using an EVM as discussed in the *Parameter Measurement Information* section (see Figure 56 to Figure 59).



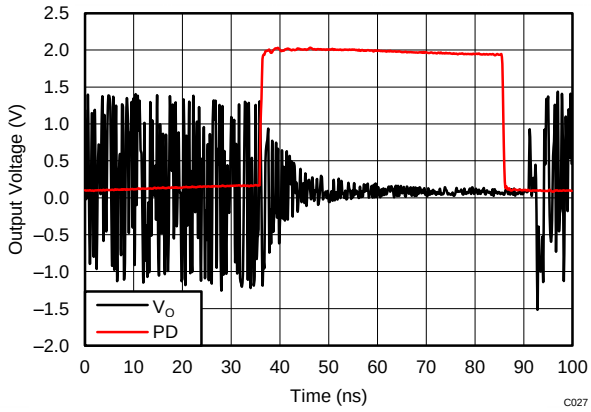
V_S = ±2.5 V, VOUT_AMP

Figure 25. Pulse Response for Various V_O



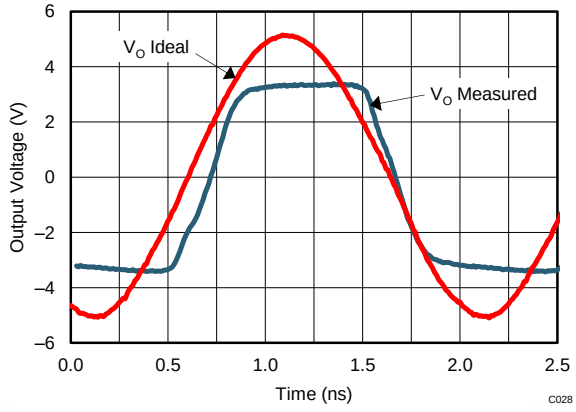
V_S = ±2.5 V, VOUT_AMP, V_{CM} = (V_{O+} + $V_{O–}$) / 2

Figure 26. Pulse Response Common-Mode for Various V_O



V_S = ±2.5 V

Figure 27. Power-Down Timing

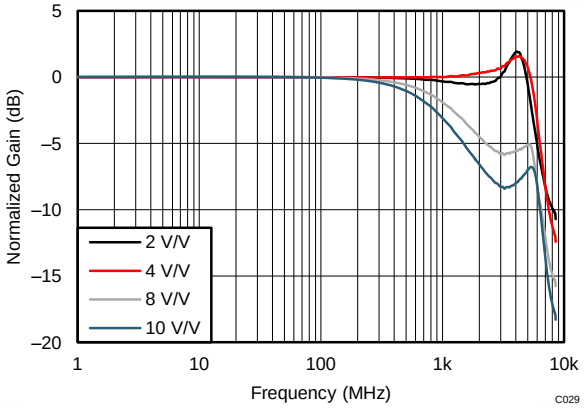


V_S = ±2.5 V

Figure 28. Overdrive Recovery

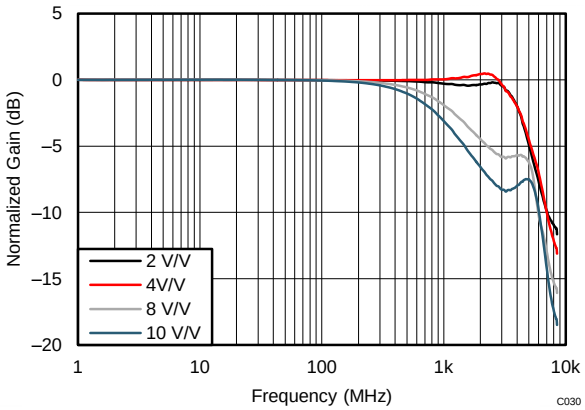
6.8 Typical Characteristics: 3.3 V

at T_A = 25°C, split supplies, V_{CM} = 0 V, R_L = 200-Ω differential (R_O = 40 Ω each), G = 12 dB, single-ended input and differential output, and input and output pins referenced to midsupply, (unless otherwise noted). Measured using an EVM as discussed in the *Parameter Measurement Information* section (see Figure 56 to Figure 59).



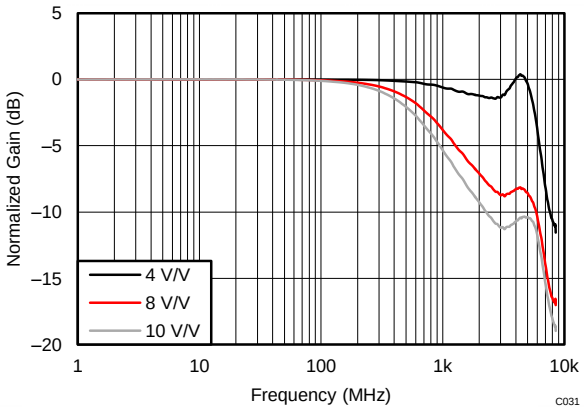
V_S = ±1.65 V, VOUT_AMP = 0.2 V_{PP}, R_L = 200 Ω

Figure 29. Small-Signal Frequency Response vs Gain



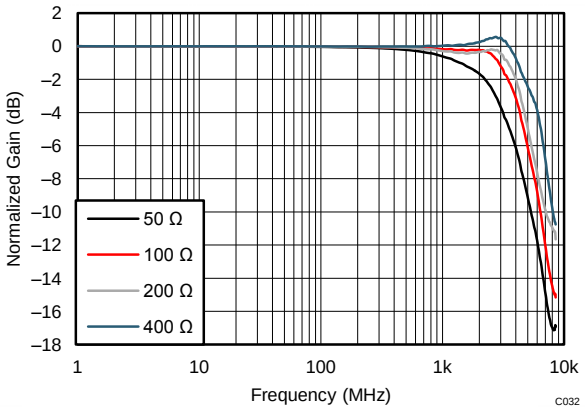
V_S = ±1.65 V, VOUT_AMP = 2 V_{PP}, R_L = 200 Ω

Figure 30. Large-Signal Frequency Response vs Gain



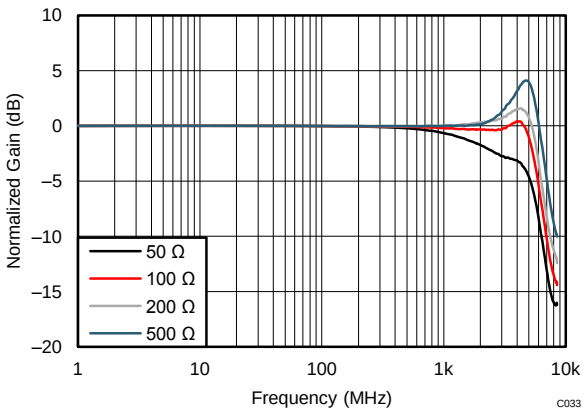
V_S = ±1.65 V, VOUT_AMP = 0.2 V_{PP}, G = 12 dB

Figure 31. Small-Signal Frequency Response vs R_L



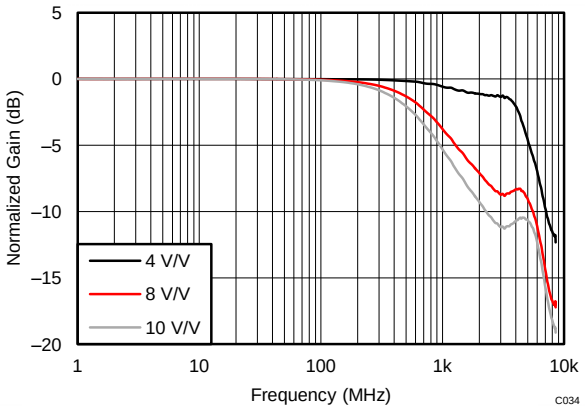
V_S = ±1.65 V, VOUT_AMP = 2 V_{PP}, G = 12 dB

Figure 32. Large-Signal Frequency Response vs R_L



V_S = ±1.65 V, VOUT_AMP = 0.2 V_{PP}, G = 12 dB

Figure 33. Small-Signal Differential Input Frequency Response vs R_L

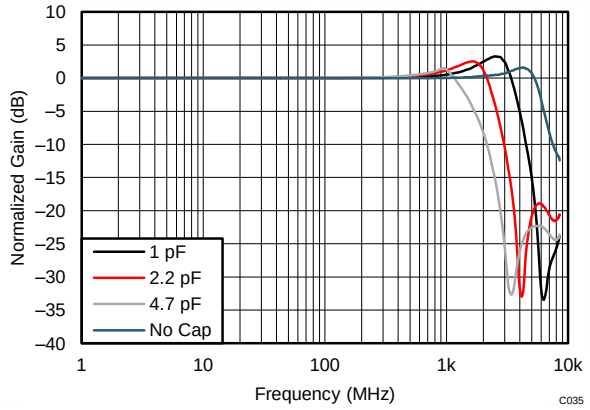


V_S = ±1.65 V, VOUT_AMP = 2 V_{PP}

Figure 34. Large-Signal Differential Input Frequency Response vs R_L

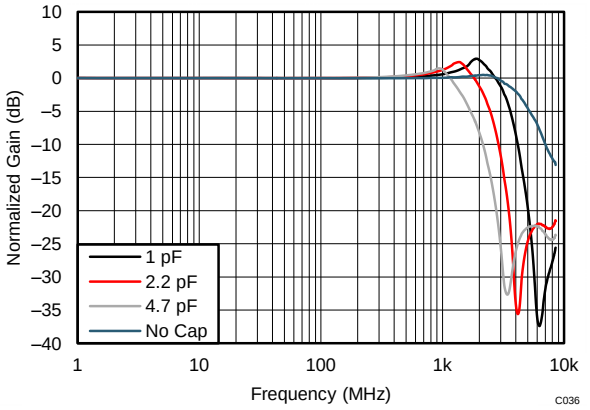
Typical Characteristics: 3.3 V (continued)

at T_A = 25°C, split supplies, V_{CM} = 0 V, R_L = 200-Ω differential (R_O = 40 Ω each), G = 12 dB, single-ended input and differential output, and input and output pins referenced to midsupply, (unless otherwise noted). Measured using an EVM as discussed in the *Parameter Measurement Information* section (see Figure 56 to Figure 59).



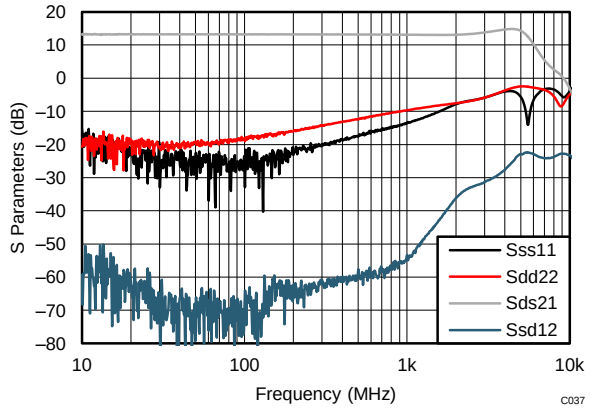
V_S = ±1.65 V, VOUT_AMP = 2 V_{PP}, capacitance at DUT output pins,

Figure 35. Small-Signal Frequency Response with Capacitive Load



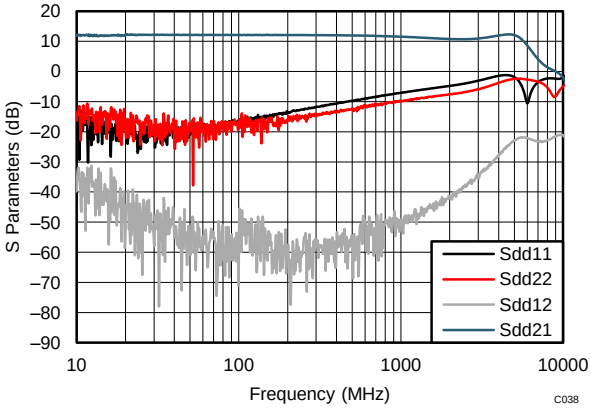
V_S = ±1.65 V, VOUT_AMP = 2 V_{PP}, capacitance at DUT output pins

Figure 36. Large-Signal Frequency Response with Capacitive Load



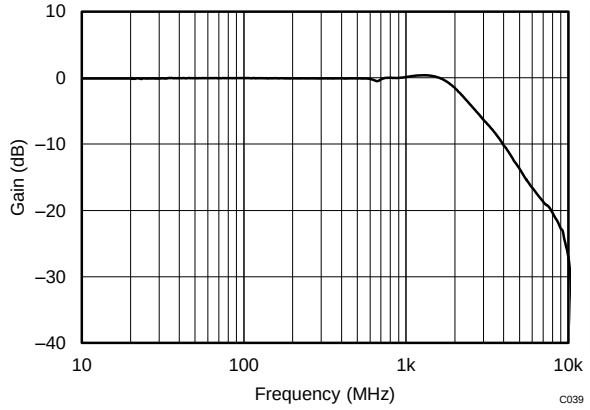
V_S = ±1.65 V, VOUT_AMP = 200 mV_{PP}

Figure 37. Single-Ended Input, S-Parameters



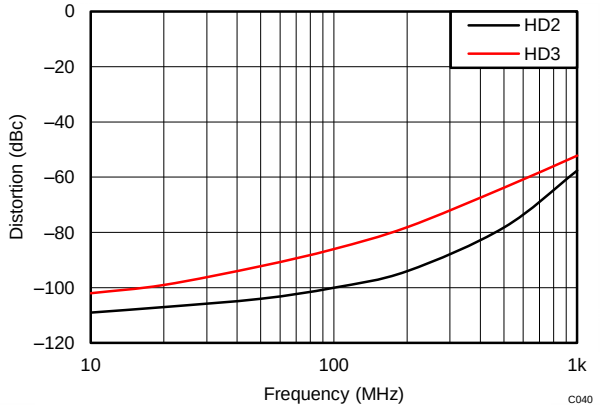
V_S = ±1.65 V, VOUT_AMP = 200 mV_{PP}

Figure 38. Differential Input, S-Parameters



V_S = ±1.65 V, VOUT_AMP = 200 mV_{PP}

Figure 39. Common-Mode Frequency Response

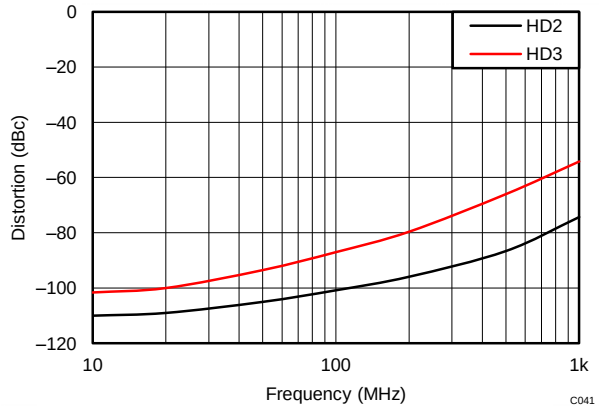


V_S = ±1.65 V, VOUT_AMP = 1 V_{PP}, R_L = 200 Ω, G = 12 dB, single-ended input

Figure 40. HD2 and HD3

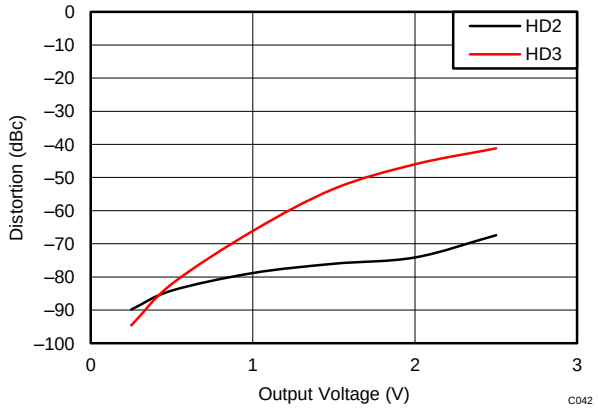
Typical Characteristics: 3.3 V (continued)

at T_A = 25°C, split supplies, V_{CM} = 0 V, R_L = 200-Ω differential (R_O = 40 Ω each), G = 12 dB, single-ended input and differential output, and input and output pins referenced to midsupply, (unless otherwise noted). Measured using an EVM as discussed in the *Parameter Measurement Information* section (see Figure 56 to Figure 59).



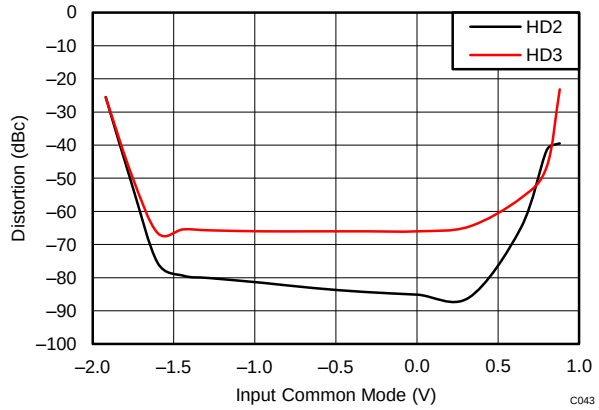
V_S = ±1.65 V, VOUT_AMP = 1 V_{PP}, R_L = 200 Ω, G = 12 dB, differential input

Figure 41. HD2 and HD3 Differential



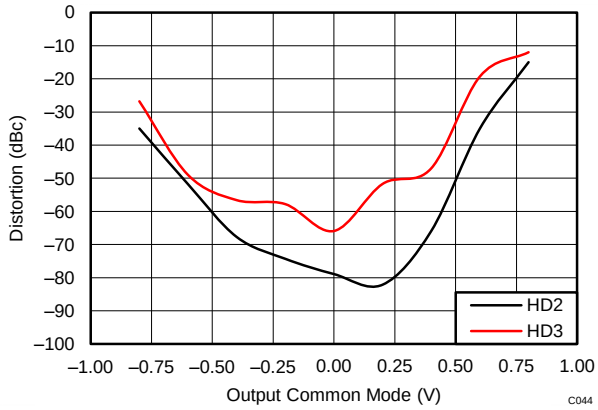
V_S = ±1.65, VOUT_AMP = 1 V_{PP}, f = 500 MHz, R_L = 200 Ω, G = 12 dB

Figure 42. HD2 and HD3 vs Output Voltage



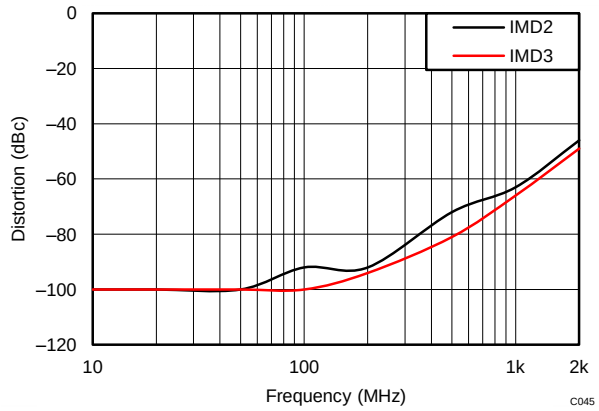
V_S = ±1.65 V, VOUT_AMP = 1 V_{PP}, f = 500 MHz, R_L = 200 Ω, G = 12 dB

Figure 43. HD2 and HD3 vs Input Common-Mode Voltage



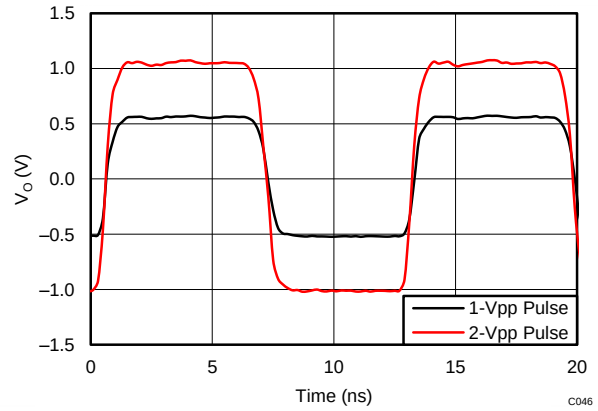
V_S = ±1.65 V, VOUT_AMP = 1 V_{PP}, f = 500 MHz, R_L = 200 Ω, G = 12 dB

Figure 44. HD2 and HD3 vs Output Common-Mode Voltage



V_S = ±1.65 V, VOUT_AMP = 0.5 V_{PP} per tone, R_L = 200 Ω, G = 12 dB

Figure 45. Intermodulation Distortion vs Frequency

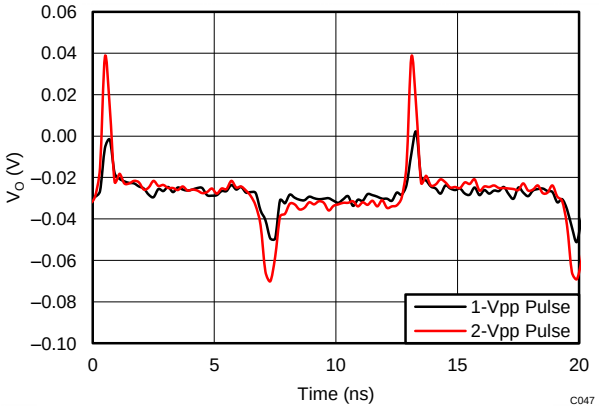


V_S = ±1.65 V, VOUT_AMP

Figure 46. Pulse Response for Various V_O

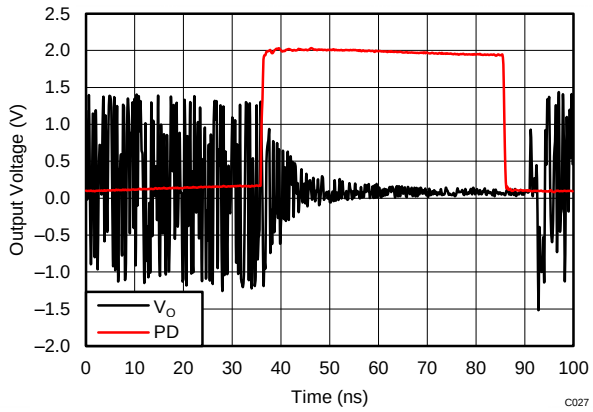
Typical Characteristics: 3.3 V (continued)

at T_A = 25°C, split supplies, V_{CM} = 0 V, R_L = 200-Ω differential (R_O = 40 Ω each), G = 12 dB, single-ended input and differential output, and input and output pins referenced to midsupply, (unless otherwise noted). Measured using an EVM as discussed in the *Parameter Measurement Information* section (see Figure 56 to Figure 59).



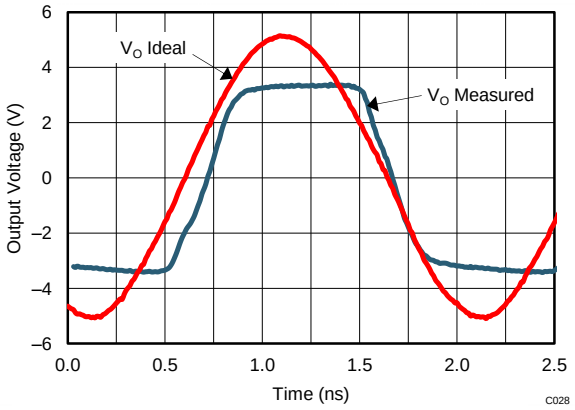
V_S = ±1.65 V, VOUT_AMP, V_{CM} = (V_{O+} + $V_{O–}$) / 2

Figure 47. Pulse Response Common-Mode



V_S = ±2.5 V

Figure 48. Power-Down Timing

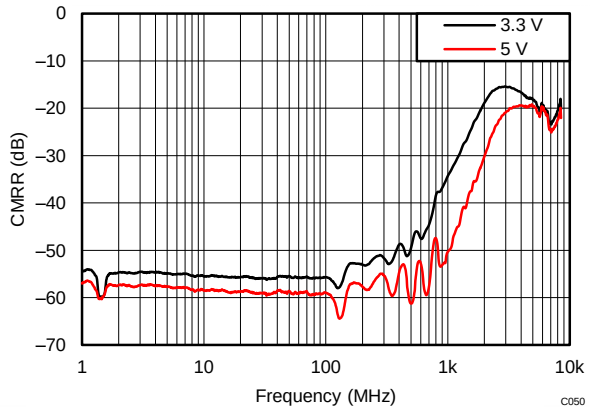


V_S = ±2.5 V

Figure 49. Overdrive Recovery

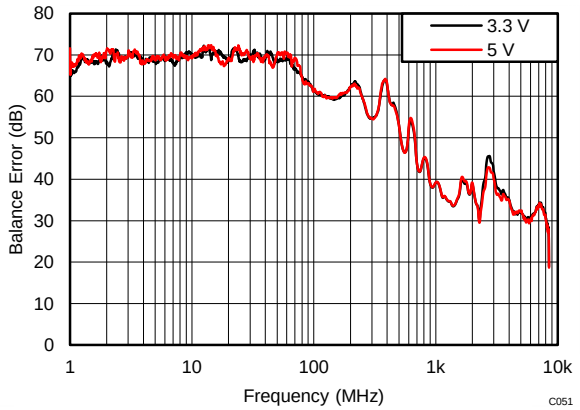
6.9 Typical Characteristics: 3.3-V to 5-V Supply Range

at T_A = 25°C, split supplies, V_{CM} = 0 V, R_L = 200-Ω differential (R_O = 40 Ω each), G = 12 dB, single-ended input and differential output, and input and output pins referenced to midsupply, (unless otherwise noted). Measured using an EVM as discussed in the *Parameter Measurement Information* section (see Figure 56 to Figure 59).



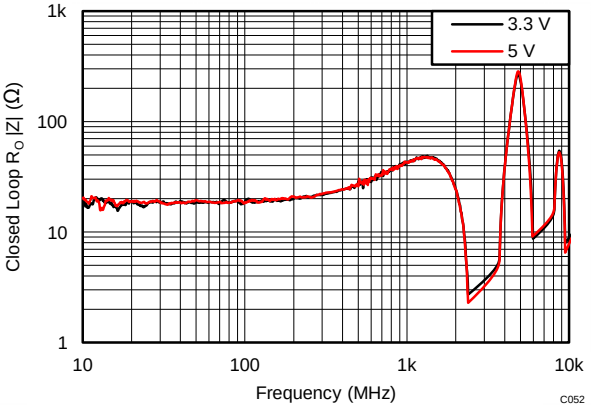
Differential input, differential output, (Sdc21)

Figure 50. CMRR



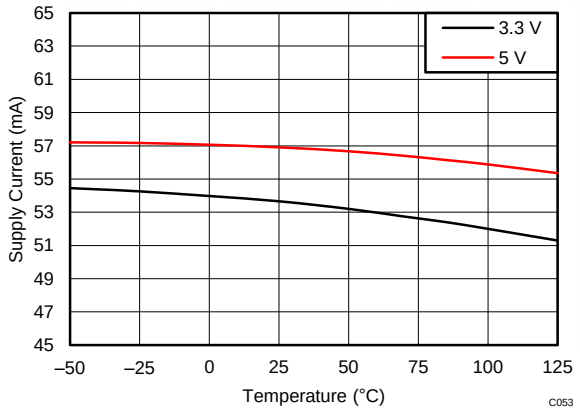
Differential input, differential output

Figure 51. Balance Error



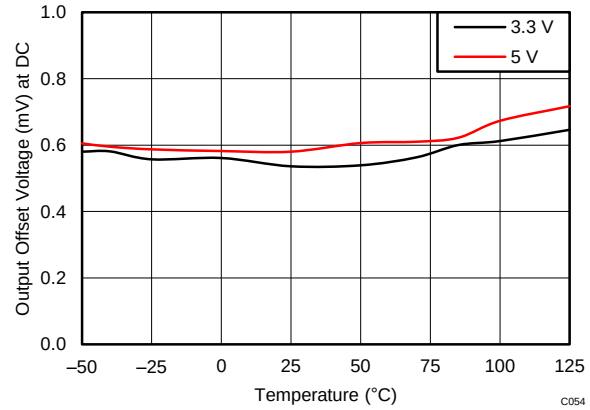
Differential output impedance, response includes board parasitics

Figure 52. Differential Output Impedance vs Frequency



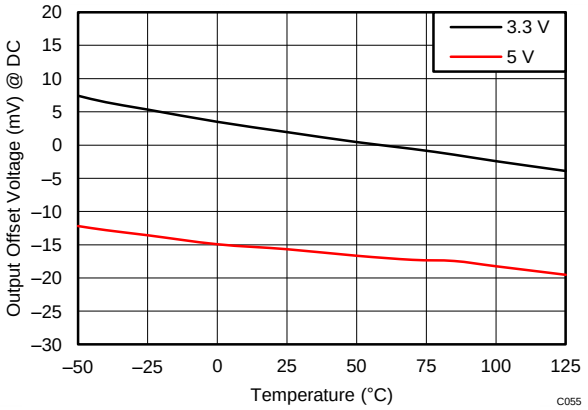
V_S = ±2.5 V

Figure 53. Supply Current vs Temperature



At DC

Figure 54. Differential Offset Voltage vs Temperature



At DC

Figure 55. Common-Mode Offset Voltage vs Temperature

7 Parameter Measurement Information

7.1 Output Reference Points

The LMH5401 is a fully-differential amplifier (FDA) configurable with external resistors for noise gain greater than 2 V/V or 6 dB (GBP = 8 GHz). For most of this document, data is collected for G = 12 dB for single-ended-to-differential (SE-DE) and differential-to-differential (DE-DE) conversions in the diagrams shown in the *Test Schematics* section. When matching the output to a 100-Ω load, the evaluation module (EVM) uses external 40-Ω resistors to complete the output matching. Having on-chip output resistors creates two potential reference points for measuring the output voltage. The amplifier output pins create one output reference point (OUT_AMP). The other output reference point is the point at the matched 100-Ω load (OUT_LOAD). These points are shown in Figure 56 to Figure 59; see the *Test Schematics* section.

Most measurements in the *Electrical Characteristics* tables and in the *Typical Characteristics* sections are measured with reference to the OUT_AMP reference point. The conversion between reference points is a straightforward reduction of 3 dB for power and 6 dB for voltage, as shown in Equation 1. The measurements are referenced to OUT_AMP when not specified.

$$\text{VOUT\_LOAD} = (\text{VOUT\_AMP} - 6\ \text{dB}) \text{ and } \text{POUT\_LOAD} = (\text{POUT\_AMP} - 3\ \text{dB}) \quad (1)$$

7.2 ATE Testing and DC Measurements

All production testing and ensured DC parameters are measured on automated test equipment capable of DC measurements only. Measurements such as output current sourcing and sinking are made in reference to the device output pins. Some measurements (such as voltage gain) reference the output of the internal amplifier and do not include losses attributed to the on-chip output resistors. The *Electrical Characteristics* table conditions specify these conditions. When the measurement refers to the amplifier output, then the output resistors are not included in the measurement. If the measurement refers to the device pins, then the output resistor loss is included in the measurement.

7.3 Frequency Response

This test is run with single-ended inputs and differential inputs.

For tests with single-ended inputs, the standard EVM is used with no changes; see Figure 56. To provide a matched input, the unused input requires a broadband 50-Ω termination to connect. When using a four-port network analyzer, the unused input can be terminated with a broadband load, or can connect to the unused input on the four-port analyzer. The network analyzer provides proper termination. A network analyzer connects to the input and output of the EVM with 50-Ω coaxial cables and measures the forward transfer function (s21). The input signal frequency is swept with the signal level set for the required output amplitude.

The LMH5401 is fully symmetrical. Either input (IN+ or IN–) can be used for single-ended inputs. The unused input must be terminated. R_F, R_{G1}, and R_{G2} determine the gain. R_T and R_M enable matching to the source resistance. See the *Test Schematics* section for more information on setting these resistors per gain and source impedance requirements. Bandwidth is dependant on gain settings because this device is a voltage feedback amplifier. With a GBP of 8 GHz, the approximate bandwidth is calculated for a specific application requirement, as shown in Equation 2. Figure 57 shows a test schematic for differential input and output.

$$\text{GBP (Hz)} = \text{BW (Hz)} \times \text{Noise Gain} \quad (2)$$

Frequency Response (continued)

For tests with differential inputs, the same setup for single-ended inputs is used except all four connectors are connected to a network analyzer port. Measurements are made in true differential mode on the Rohde & Schwarz® network analyzer or in calculated differential mode. In each case, the differential inputs are each driven with a 50-Ω source. Table 1 and Table 2 lists the resistor values used in frequency response sweeps.

Table 1. Differential Input/Output

A_V (V/V)	R_{G1}, R_{G2} (Ω)	R_F (TOTAL / EXTERNAL, Ω)	R_T (Ω)
2	100	199 / 174	100
4	49.9	199 / 174	N/A
6	49.9	300 / 274	N/A
8	49.9	400 / 375	N/A
10	49.9	500 / 475	N/A

Table 2. SE Input

A_V (V/V)	R_{G1} (Ω)	R_T (Ω)	R_{G2} (Ω)	R_F (TOTAL / EXTERNAL, Ω)
2	90.9	76.8	121	200 / 175
4	22.6	357	66.5	152 / 127
8	12.1	1100	60.4	250 / 225
10	9.76	1580	57.6	300 / 275

7.4 S-Parameters

The standard EVM is used for all s-parameter measurements. All four ports are used or are terminated with 50 Ω; see the *Frequency Response* section.

7.5 Frequency Response with Capacitive Load

The standard EVM is used and the capacitive load is soldered to the inside pads of the 40-Ω matching resistors (on the DUT side). In this configuration, the on-chip, 10-Ω resistors isolate the capacitive load from the amplifier output pins. The test schematic for capacitive load measurements is shown in Figure 58.

7.6 Distortion

The standard EVM is used for measuring single-tone harmonic distortion and two-tone intermodulation distortion. All distortion is measured with single-ended input signals; see Figure 59. To interface with single-ended test equipment, external baluns are required between the EVM output ports and the test equipment. The *Typical Characteristics* plots are created with Marki™ baluns, model number BAL-0010. These baluns combine two tones in the two-tone test plots. For distortion measurements, the same termination must be used on both input pins. When a filter is used on the driven input port, the same filter and a broadband load terminate the other input. When the signal source is a broadband controlled impedance, only a broadband-controlled impedance is required to terminate the unused input.

7.7 Noise Figure

The standard EVM is used with a single-ended input matched to 50-Ω and the Marki balun on the output similar to the harmonic distortion test setup.

7.8 Pulse Response, Slew Rate, and Overdrive Recovery

The standard EVM is used for time-domain measurements. The input is single-ended with the differential outputs routed directly to the oscilloscope inputs. The differential signal response is calculated from the two separate oscilloscope inputs (Figure 25 to Figure 46). In addition, the common-mode response is captured in this configuration.

7.9 Power Down

The standard EVM is used with the shorting block on jumper JPD removed completely. A high-speed, 50-Ω pulse generator drives the PD pin when the output signal is measured by viewing the output signal (such as a 250-MHz sine-wave input).

7.10 V_{CM} Frequency Response

The standard EVM is used with R_{CM+} and $R_{CM–}$ removed and a new resistor installed at R_{TCM} = 49.9 Ω. The 49.9-Ω resistor is placed at C17 on the EVM schematic. A network analyzer is connected to the V_{CM} input of the EVM and the EVM outputs are connected to the network analyzer with 50-Ω coaxial cables. Set the network analyzer analysis settings to single-ended input and differential output. Measure the output common-mode with respect to the single-ended input (Scs21). The input signal frequency is swept with the signal level set for 100 mV (–16 dBm). Note that the common-mode control circuit gain is one.

7.11 Test Schematics

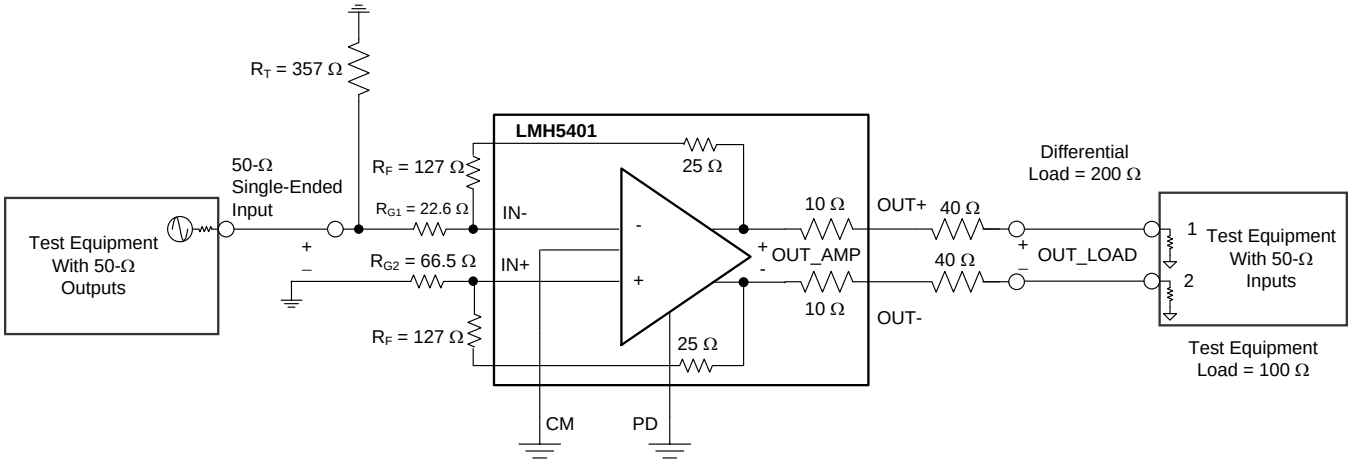


Figure 56. Test Schematic: Single-Ended Input, Differential Output, A_V = 4 V/V

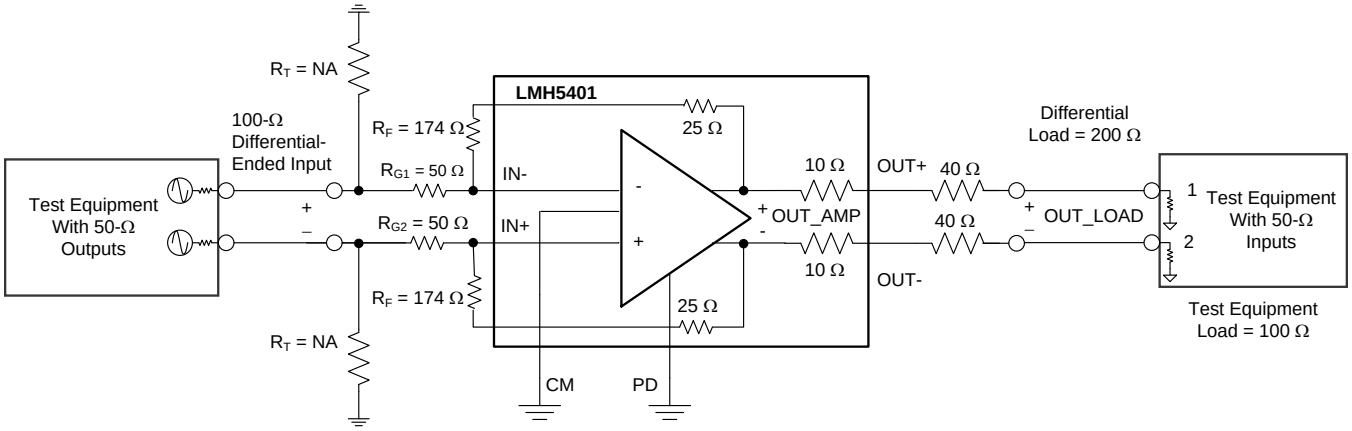


Figure 57. Test Schematic: Differential Input, Differential Output, A_V = 4 V/V

Test Schematics (continued)

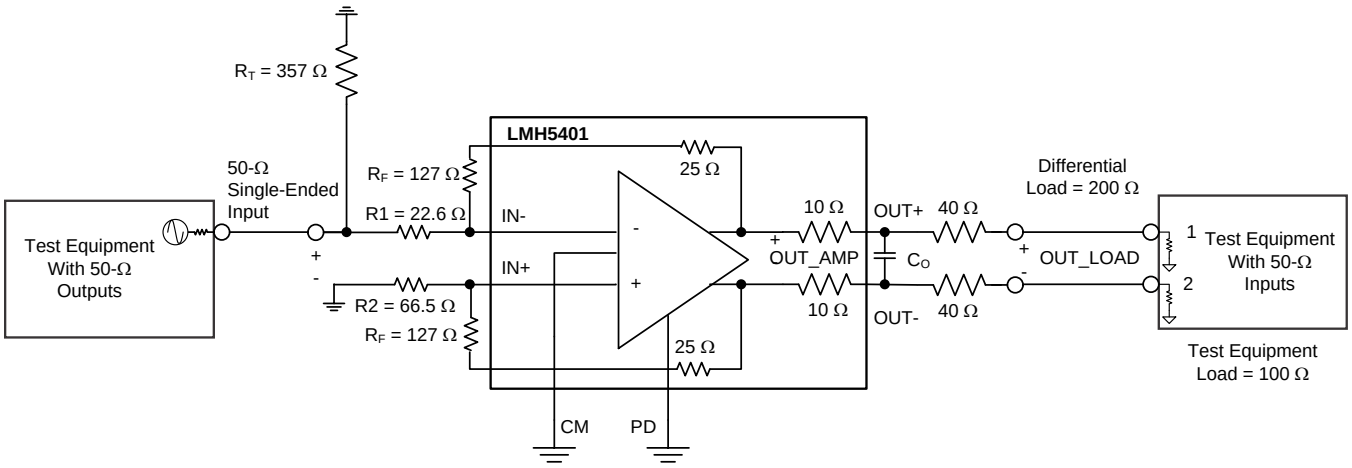


Figure 58. Test Schematic: Capacitive Load, A_V = 4 V/V

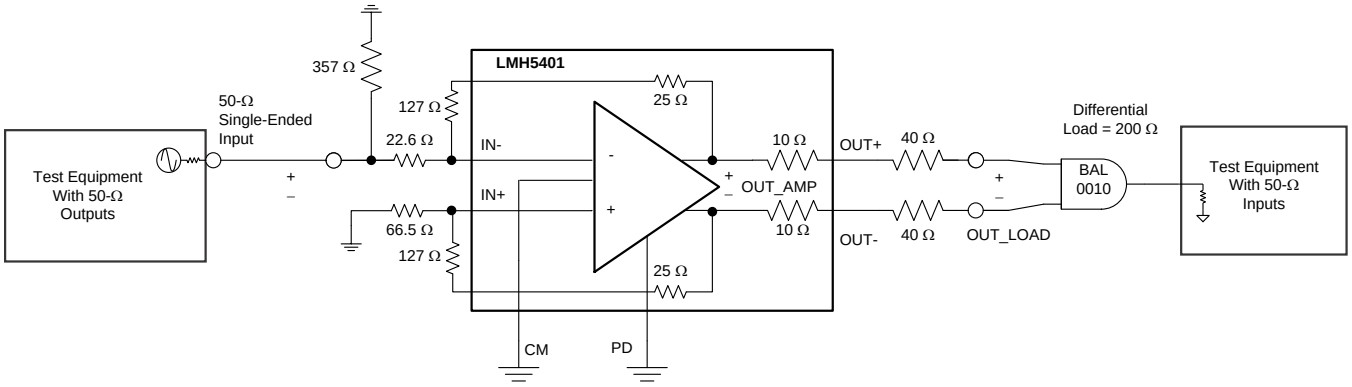


Figure 59. Test Schematic for Noise Figure and Single-Ended Harmonic Distortion, A_V = 4 V/V

8 Detailed Description

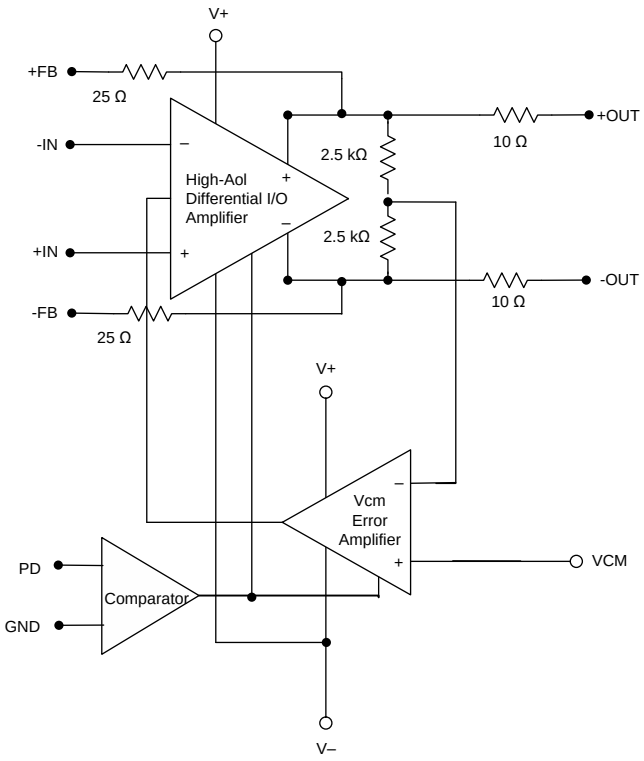
8.1 Overview

The LMH5401 is a very high-performance, differential amplifier optimized for radio frequency (RF) and intermediate frequency (IF) or high-speed, time-domain applications for wide bandwidth applications as the GBP is 8 GHz. The device is designed for DC- or AC-coupled applications that may require a single-ended-to-differential (SE-DE) conversion when driving an analog-to-digital converter (ADC). The required external feedback (R_F) and gain set (R_G) resistors configure the gain of the device. For the EVM the standard gain is set to G = 12 dB (for DE and SE conversions) with R_F = 127 Ω and R_G = 22.6 Ω.

A common-mode reference input pin aligns the amplifier output common-mode with the ADC input requirements. Power supplies between 3.3 V and 5 V are selected and dual-supply operation is supported when required by the application. A power-down feature is available for power savings.

The LMH5401 offers two on-chip termination resistors, one for each output with values of 10 Ω each. For most load conditions the 10-Ω resistors are a partial termination. Consequently, external termination resistors are required in most applications. See Table 4 for some common load values and the matching resistors.

8.2 Functional Block Diagram



V– and GND are isolated.

8.3 Feature Description

The LMH5401 includes the following features:

- Fully-differential amplifier
- Flexible gain configurations using external resistors
- Output common-mode control
- Single- or split-supply operation
- Gain bandwidth product (GBP) of 8 GHz
- Linear bandwidth of 2 GHz (G = 12 dB)
- Power down

8.3.1 Fully-Differential Amplifier

The LMH5401 is a voltage feedback (VFA)-based fully-differential amplifier (FDA) offering a GBP of 8 GHz with flexible gain options using external resistors. The core differential amplifier is a slightly decompensated voltage feedback design with a high slew rate and best-in-class linearity up to 2 GHz for G = 12 dB (SE-DE, DE-DE).

As with all FDA devices, the output average voltage (common-mode) is controlled by a separate common-mode loop. The target for this output average is set by the V_{CM} input pin. The V_{OCM} range extends from 1.1 V below the midsupply voltage to 1.1 V above the midsupply voltage when using a 5-V supply. Note that on a 3.3-V supply the output common-mode range is quite small. For applications using a 3.3-V supply voltage, the output common-mode must remain very close to the midsupply voltage.

The input common-mode voltage offers more flexibility than the output common-mode voltage. The input common-mode range extends from the negative rail to approximately 1 V above the midsupply voltage when powered with a 5-V supply.

8.3.1.1 Power Down and Ground Pins

A power-down pin is included. This pin is referenced to the GND pins with a threshold voltage of approximately 1 V. Setting the PD pin voltage to more than the specified minimum voltage turns the device off, which places the LMH5401 into a very low quiescent current state. Note that when disabled, the signal path is still present through the passive external resistors. Input signals applied to a disabled LMH5401 device still appear at the outputs at some level through this passive resistor path, as with any disabled FDA device. The power-down pin is biased to the logic-low state with a 50-kΩ internal resistor.

8.3.2 Operations for Single-Ended to Differential Signals

One of the most useful features supported by the FDA device is a simple conversion from a single-ended input to a differential output centered on a user-controlled, common-mode level. Although the output side is relatively straightforward, the device input pins move in a common-mode sense with the input signal. This feature increases the apparent input impedance to be greater than the R_G value. However, this feature can cause input clipping if this common-mode signal moves beyond the input range. This input active impedance issue applies to AC- and DC-coupled designs, and requires somewhat more complex solutions for the resistors to account for this active impedance, as shown in this section.

8.3.2.1 AC-Coupled Signal Path Considerations for Single-Ended Input to Differential Output Conversion

When the signal path is AC coupled, the DC biasing for the LMH5401 becomes a relatively simple task. In all designs, start by defining the output common-mode voltage. The AC-coupling issue can be separated for the input and output sides of an FDA design. The input can be AC-coupled and the output DC coupled, or the output can be AC-coupled and the input DC-coupled, or they can both be AC-coupled. One situation where the output can be DC-coupled (for an AC-coupled input), is when driving directly into an ADC where the V_{OCM} control voltage uses the ADC common-mode reference to directly bias the FDA output common-mode to the required ADC input common-mode. The feedback path must always be DC-coupled. In any case, the design starts by setting the desired V_{OCM}. When an AC-coupled path follows the output pins, the best linearity is achieved by operating V_{OCM} at midsupply. The V_{OCM} voltage must be within the linear range for the common-mode loop, as specified in the headroom specifications. If the output path is AC-coupled, letting the V_{OCM} control pin float is usually preferred to obtain a midsupply default V_{OCM} bias with no external elements. To limit noise, place a 0.1-µF decoupling capacitor on the V_{OCM} pin to ground. After V_{OCM} is defined, check the target output voltage swing to ensure that the V_{OCM} positive or negative output swing on each side does not clip into the supplies. If the

Feature Description (continued)

desired output differential swing is defined as V_{OPP}, divide by 4 to obtain the $\pm V_P$ swing around V_{OCM} at each of the two output pins (each pin operates 180° out of phase with the other). Check that $V_{OCM} \pm V_P$ does not exceed the output swing of this device. Going to the device input pins side, because both the source and balancing resistor on the non-signal input side are DC blocked (see Figure 61), no common-mode current flows from the output common-mode voltage, thus setting the input common-mode equal to the output common-mode voltage. This input headroom sets a limit for higher V_{OCM} voltages. The minimum headroom for the input pins to the positive supply overrides the headroom limit for the output V_{OCM} because the input V_{ICM} is the output V_{OCM} for AC-coupled sources. The input signal moves this input V_{ICM} around the DC bias point, as shown in the *Resistor Design Equations for Single-to-Differential Applications* subsection of the *Fully-Differential Amplifier* section.

8.3.2.2 DC-Coupled Input Signal Path Considerations for SE-DE Conversions

The output considerations remain the same as for the AC-coupled design. The input can be DC-coupled when the output is AC-coupled. A DC-coupled input with an AC-coupled output can have some advantages to move the input V_{ICM} down if the source is ground referenced. When the source is DC-coupled into the LMH5401 (as shown in Figure 60), both sides of the input circuit must be DC coupled to retain differential balance. Normally, the non-signal input side has an R_G element biased to an expected source midrange value. Providing this midscale reference provides a balanced differential swing around V_{OCM} at the outputs. Often, R_{G2} is grounded for DC-coupled, bipolar-input applications. This configuration provides a balanced differential output if the source swings around ground. If the source swings from ground to some positive voltage, grounding R_{G2} results in a unipolar output differential swing from both outputs at V_{OCM} (when the input is at ground) to one polarity of swing. Biasing R_{G2} to an expected midpoint for the input signal creates a differential output swing around V_{OCM}. One significant consideration for a DC-coupled input is that V_{OCM} sets up a common-mode bias current from the output back through R_F and R_G to the source on both sides of the feedback. Without input-balancing networks, the source must sink or source this DC current. After the input signal range and biasing on the other R_G element is set, check that the voltage divider from V_{OCM} to V_I through R_F and R_G (and possibly R_S) establishes an input V_{ICM} at the device input pins that is in range.

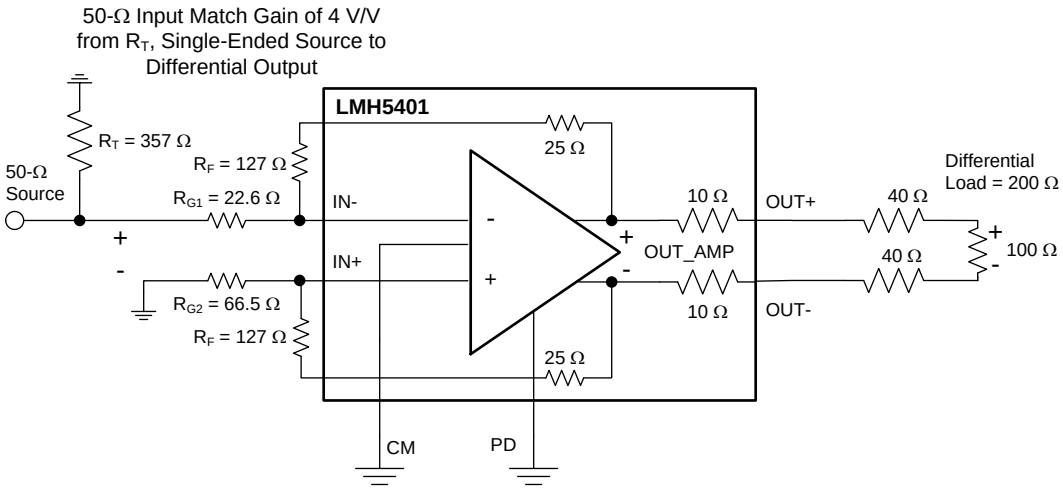


Figure 60. DC-Coupled, Single-Ended-to-Differential, Gain of 4 V/V

8.3.2.3 Resistor Design Equations for Single-to-Differential Applications

Being familiar with the FDA resistor selection criteria is still important because the LMH5401 gain is configured through external resistors. The design equations for setting the resistors around an FDA to convert from a single-ended input signal to a differential output can be approached in several ways. In this section, several critical assumptions are made to simplify the results:

- The feedback resistors are selected first and are set to be equal on the two sides of the device.
- The DC and AC impedances from the summing junctions back to the signal source and ground (or a bias voltage on the non-signal input side) are set equal to retain the feedback divider balance on each side of the FDA.

Feature Description (continued)

Both of these assumptions are typical and are aimed to deliver the best dynamic range through the FDA signal path.

After the feedback resistor values are selected, the aim is to solve for R_T (a termination resistor to ground on the signal input side), R_{G1} (the input gain resistor for the signal path), and R_{G2} (the matching gain resistor on the non-signal input side); see Figure 61. This example uses the LMH5401, which is an external resistor FDA. The same resistor solutions can be applied to AC- or DC-coupled paths. Adding blocking capacitors in the input-signal chain is a simple option. Adding these blocking capacitors after the R_T element (see Figure 61) has the advantage of removing any DC currents in the feedback path from the output V_{OCM} to ground.

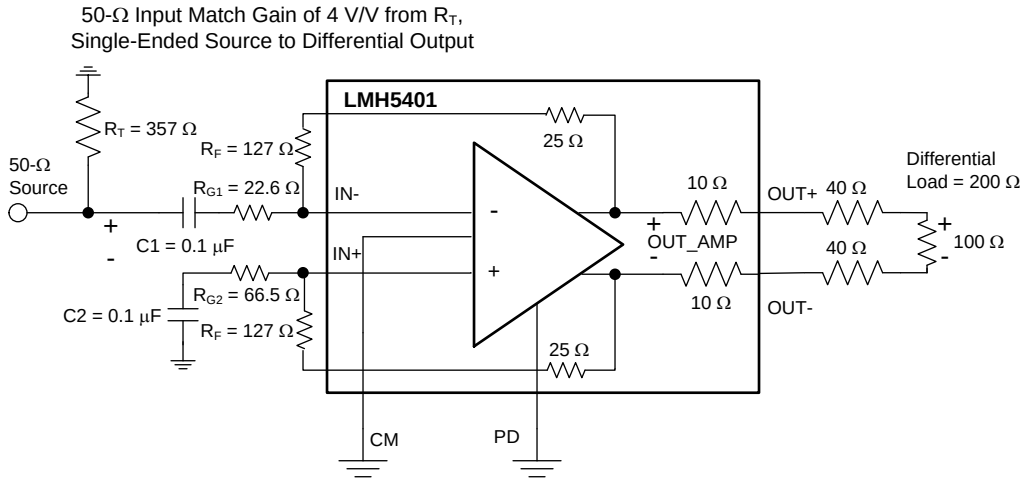


Figure 61. AC-Coupled, Single-Ended Source to a Differential Gain of a 4-V/V

Most FDA amplifiers use external resistors and have complete flexibility in the selected R_F. However, the LMH5401 has small on-chip feedback resistors that are fixed at 25 Ω. The equations used in this section apply with an additional 25 Ω to add to the external R_F resistors.

After the feedback resistor values are selected, solve for R_T (a termination resistor to ground on the signal input side), R_{G1} (the input gain resistor for the signal path), and R_{G2} (the matching gain resistor on the non-signal input side). The same resistor solutions are applied to AC- or DC-coupled paths. Adding blocking capacitors in the input-signal chain is a simple option. Adding these blocking capacitors after the R_T element has the advantage of removing any DC currents in the feedback path from the output V_{OCM} to ground.

Earlier approaches to the solutions for R_T and R_{G1} (when the input must be matched to a source impedance, R_S) follow an iterative approach. This complexity arises from the active input impedance at the R_{G1} input. When the FDA converts a single-ended signal to a differential signal, the common-mode input voltage at the FDA inputs must move with the input signal to generate the inverted output signal as a current in the R_{G2} element. A more recent solution is shown as Equation 3, where a quadratic in R_T is solved for an exact required value. This quadratic emerges from the simultaneous solution for a matched input impedance and target gain. The only required inputs are:

1. The selected R_F value.
2. The target voltage gain (A_V) from the input of R_T to the differential output voltage.
3. The desired input impedance at the junction of R_T and R_{G1} to match R_S.

Solving this quadratic for R_T starts the solution sequence, as shown in Equation 3:

$$R_T^2 - R_T \frac{2R_S\left(2R_F + \frac{R_S}{2}A_V^2\right)}{2R_F\left(2 + A_V\right) - R_S A_V(4 + A_V)} - \frac{2R_F R_S^2 A_V}{2R_F\left(2 + A_V\right) - R_S A_V\left(4 + A_V\right)} = 0 \quad (3)$$

Feature Description (continued)

Because this equation is a quadratic, there are limits to the range of solutions. Specifically, after R_F and R_S are selected, there is physically a maximum gain beyond which Equation 3 starts to solve for negative R_T values (if input matching is a requirement). With R_F selected, use Equation 4 to verify that the maximum gain is greater than the desired gain.

$$Av_{max} = \left(\frac{R_F}{R_S} - 2\right) \bullet \left[1 + \sqrt{1 + \frac{4\frac{R_F}{R_S}}{\left(\frac{R_F}{R_S} - 2\right)^2}}\right] \quad (4)$$

Feature Description (continued)

If the achievable A_{Vmax} is less than desired, increase the R_F value. After R_T is derived from Equation 3, the R_{G1} element is shown in Equation 5:

$$R_{G1} = \frac{2\frac{R_F}{A_V} - R_S}{1 + \frac{R_S}{R_T}} \tag{5}$$

Then, the simplest approach is to use a single $R_{G2} = R_T \parallel R_S + R_{G1}$ on the non-signal input side. Often, this approach is shown as the separate R_{G1} and R_S elements. This approach can provide a better divider match on the two feedback paths, but a single R_{G2} is often acceptable. A direct solution for R_{G2} is shown as Equation 6:

$$R_{G2} = \frac{2\frac{R_F}{A_V}}{1 + \frac{R_S}{R_T}} \tag{6}$$

This design proceeds from a target input impedance matched to R_S, signal gain A_V, and a selected R_F value. The nominal R_F value selected for the LMH5401 characterization is 152 Ω ($R_{FExternal}$ + $R_{FInternal}$, where $R_{FInternal}$ is always 25 Ω). As discussed previously, this resistance is on-chip and cannot be changed. See Table 1 and Table 2 in the *Frequency Response* section, which lists the value of resistors used for characterization in this document.

8.3.2.4 Input Impedance Calculations

The designs so far have included a source impedance (R_S) that must be matched by R_T and R_{G1}. The total impedance with respect to the input at R_{G1} for the circuit of Figure 60 is the parallel combination of R_T to ground and ZA (active impedance) presented by the amplifier input at R_{G1}. That expression (assuming R_{G2} is set to obtain a differential divider balance) is shown in Equation 7:

$$ZA = R_{G1}\frac{\left(1 + \frac{R_{G1}}{R_{G2}}\right)\left(1 + \frac{R_F}{R_{G1}}\right)}{2 + \frac{R_F}{R_{G2}}} \tag{7}$$

For designs that do not require impedance matching (but instead come from the low-impedance output of another amplifier, for instance), $R_{G1} = R_{G2}$ is the single-to-differential design used without R_T to ground. Setting $R_{G1} = R_{G2} = R_G$ in Equation 7 shows the input impedance of a simple input FDA driving from a low-impedance, single-ended source to a differential output.

8.3.3 Differential-to-Differential Signals

The LMH5401 can amplify differential input signals to differential output signals. In many ways, this method is a much simpler way to operate the FDA from a design equations perspective. Again, assuming the two sides of the circuit are balanced with equal R_F and R_G elements, the differential input impedance is the sum of the two R_G elements to a differential inverting summing junction. In these designs, the input common-mode voltage at the summing junctions does not move with the signal, but must be DC biased in the allowable range for the input pins with consideration given to the voltage headroom required to each supply. Slightly different considerations apply to ac- or DC-coupled, differential-in to differential-out designs, as shown in this section.

Feature Description (continued)

8.3.3.1 AC-Coupled, Differential-Input to Differential-Output Design Issues

When using the LMH5401 with an AC-coupled differential source, the input can be coupled in through two blocking capacitors. An optional input differential termination resistor (R_M) can be included to allow the input R_G resistors to be scaled up while still delivering lower differential input impedance to the source. In Figure 62, the R_G elements sum to show a 200-Ω differential impedance and the R_M element combines in parallel to give a net 100-Ω, AC, differential impedance to the source. Again, the design proceeds by selecting the R_F element values, then the R_G to set the differential gain, then an R_M element (if required) to achieve a target input impedance. Alternatively, the R_M element can be eliminated, the R_G elements set to the desired input impedance, and R_F set to the get the differential gain (= R_F / R_G). The DC biasing in Figure 62 is simple. The output V_{OCM} is set by the input control voltage and, because there is no DC current path for the output common-mode voltage, that DC bias sets the input pins common-mode operating points.

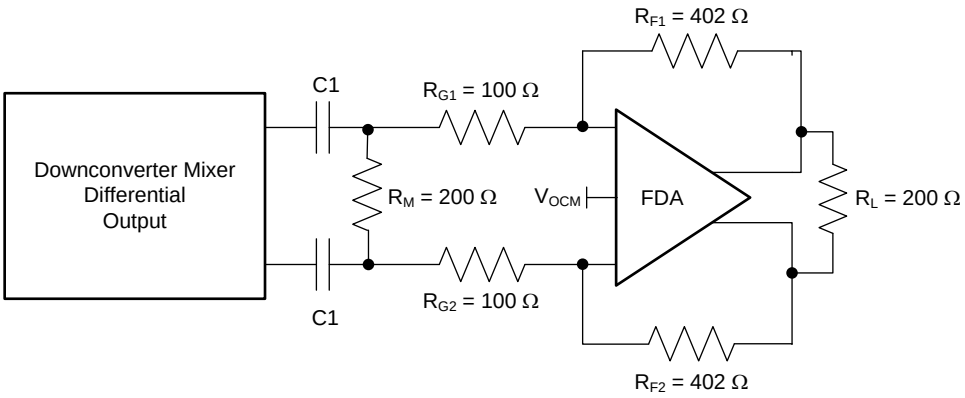


Figure 62. Downconverting Mixer AC-Coupled to the LMH5401 (A_V = 4 V/V)

8.3.3.2 DC-Coupled, Differential-Input to Differential-Output Design Issues

Operating the LMH5401 with a DC-coupled input source simply requires that the input pins stay in range of the DC common-mode operating voltage. Only R_G values that are equal to the differential input impedance and that set the correct R_F values for the gain desired are required.

8.3.4 Output Common-Mode Voltage

The CM input controls the output common-mode voltage. CM has no internal biasing network and must be driven by an external source or resistor divider network to the positive power supply. The CM input impedance is very high and bias current is not critical. The CM input has no internal reference and must be driven from an external source. Using a bypass capacitor is required. A capacitor value of 0.01 µF is recommended. For best harmonic distortion, maintain the CM input within ±1 V of the midsupply voltage using a 5-V supply and within ±0.5 V when using a 3.3-V supply. The CM input voltage can operate outside this range if a lower output swing is used or distortion degradation is allowed. For more information, see Figure 21 and Figure 22.

8.3.5 LMH5401 Comparison

Table 3 lists several fully differential amplifiers with similar applications to the LMH5401.

Table 3. Device Family Comparison

DEVICE	BW (A_V = 12 dB)	DISTORTION	NOISE (nV/√Hz)
LMH3401	7 GHz, G = 16 dB	–79-dBc HD2, –77-dBc HD3 at 500 MHz	1.4
LMH6554	1.6 GHz	–79-dBc HD2, –70-dBc HD3 at 250 MHz	0.9
LMH6552	0.8 GHz	–74-dBc HD2, –84-dBc HD3 at 70 MHz	1.1

8.4 Device Functional Modes

8.4.1 Operation With a Split Supply

The LMH5401 operates using split supplies. One of the most common supply configurations is ±2.5 V. In this case, VS+ is connected to 2.5 V, VS– is connected to –2.5 V, and the GND pins are connected to the system ground. As with any device, the LMH5401 is impervious to what the levels are named in the system. In essence, using split supplies is simply a level shift of the power pins by –2.5 V. If everything else is level-shifted by the same amount, the device does not detect any difference. With a ±2.5-V power supply, the CM range is 0 V ±1 V; the input has a slightly larger range of –2.5 V to 1 V. This design has certain advantages in systems where signals are referenced to ground, and as shown in the *ADC Input Common-Mode Voltage Considerations : DC-Coupled Input* section, for driving ADCs with low input common-mode voltage requirements in DC-coupled applications. With the GND pin connected to the system ground, the power-down threshold is 1.2 V, which is compatible with most logic levels from 1.5-V CMOS to 2.5-V CMOS.

As noted previously, the absolute supply voltage values are not critical. For example, using a 4-V VS+ and a –1-V VS– still results in a 5-V supply condition. As long as the input and output common-mode voltages remain in the optimum range, the amplifier can operate on any supply voltages from 3.3 V to 5.25 V. When considering using supply voltages near the 3.3-V total supply, take care to ensure that the amplifier performance is adequate. Setting appropriate common-mode voltages for large-signal swing conditions becomes difficult when the supply voltage is below 4 V.

8.4.2 Operation With a Single Supply

As with split supplies, the LMH5401 can operate from single-supply voltages from 3.3 V to 5.25 V. Single-supply operation is most appropriate when the signal path is AC-coupled and the input and output common-mode voltages are set to midsupply by the CM pin and are preserved by coupling capacitors on the input and output.

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

9.1.1 Stability

Two types of gain are associated with amplifiers: noise and signal gain. Noise gain (NG) is what is used to best determine the stability of an amplifier. The noise gain is the inverse of the voltage divider from the outputs back to the differential inputs. This gain is calculated by NG = (R_F / R_{IN}) + 1. For the LMH5401, NG values greater than three creates a stable circuit independent on how the signal gain is set. In Figure 63, for optimal performance choose R_F within the values noted in this document (see the *Parameter Measurement Information* section for further information). Using too large of a resistance in the feedback path adds noise and can possibly have a negative affect on bandwidth, depending on the parasitic capacitance of the board; too low of a resistance can load the output, thus affecting distortion performance. When low gain stability is required, alter the noise gain by adding a *dummy* resistor (that is, R_T in the differential configuration of Figure 63). By manipulating the noise gain with this addition, the amplifier can be stabilized without affecting signal gain. Evaluate the system at lower signal gains (G less than or equal to 2) if SNR can be tolerated with the higher noise gain configuration. In Figure 63, R_S and R_T in parallel combination affects the noise gain of the amplifier. R_G and R_F are the main gain-setting resistors and the addition of R_T adjusts the noise gain for stability. Much of this stability can be simulated using the LMH5401 TINA model, depending on the amplifier configuration. The example in Figure 63 (listed in row 1 of Table 1) uses the LMH5401, a signal gain of two , and a noise gain of five.

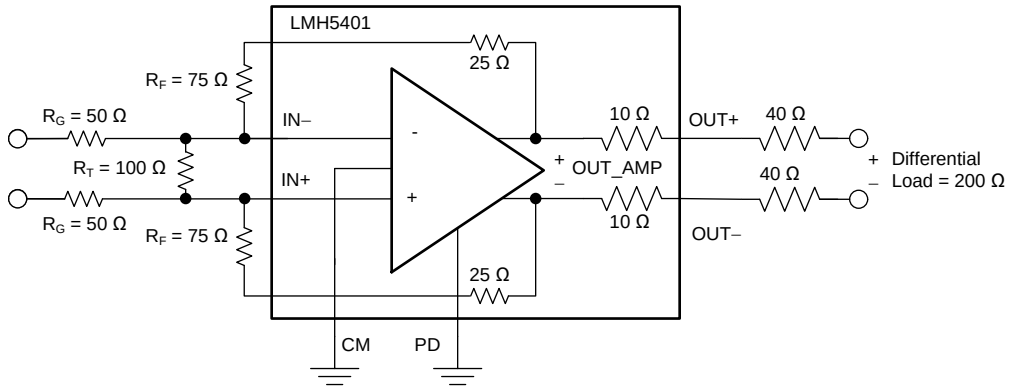


Figure 63. Differential Stability

9.1.2 Input and Output Headroom Considerations

The starting point for most designs is to assign an output common-mode voltage. For AC-coupled signal paths, this starting point is often the default midsupply voltage to retain the most available output swing around the output operating point, which is centered with V_{CM} equal to the midsupply point. For DC-coupled designs, set this voltage considering the required minimum headroom to the supplies listed in the *Electrical Characteristics* tables for V_{CM} control. From that target output, V_{CM}, the next step is to verify that the desired output differential V_{PP} stays within the supplies. For any desired differential output voltage (V_{OPP}) check the maximum possible signal swing for each output pin. Make sure that each pin can swing to the voltage required by the application.

Application Information (continued)

For instance, when driving the ADC12D1800RF with a 1.25-V common-mode and 0.8-V_{PP} input swing, the maximum output swing is set by the negative-going signal from 1.25 V to 0.2 V. The negative swing of the signal is right at the edge of the output swing capability of the LMH5401. To set the output common-mode to an acceptable range, a negative power supply of at least –1 V is recommended. The designed negative supply voltage is the ADC V_{CM} – 2.5 V for the negative supply and the ADC V_{CM} + 2.5 V for the input swing. To use the existing supply rails, deviating from the designed voltage may be required.

With the output headroom confirmed, the input junctions must stay within the operating range. Because the input range extends approximately to the negative supply voltage, input range limitations only appear when approaching the positive supply where a maximum 1.5-V headroom is required.

The input pins operate at voltages set by the external circuit design, the required output (V_{OCM}), and the input signal characteristics. The operating voltage of the input pins depends on the external circuit design. With a differential input, the input pins operate at a fixed input V_{ICM}, and the differential input signal does not influence this common-mode operating voltage.

AC-coupled differential input designs have a V_{ICM} equal to the output V_{OCM}. DC-coupled differential input designs must check the voltage divider from the source V_{CM} to the LMH5401 CM setting. That result solves to an input V_{ICM} within the specified range. If the source V_{CM} can vary over some voltage range, the validation calculations must include this variation.

9.1.3 Noise Analysis

The first step in the output noise analysis is to reduce the application circuit to the simplest form with equal feedback and gain setting elements to ground (as shown in Figure 64) and considering FAD and resistor noise terms.

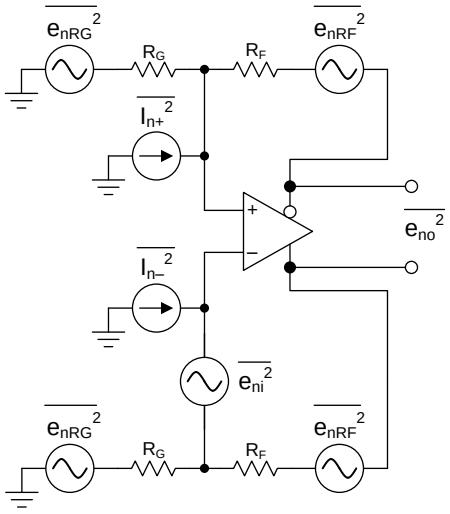


Figure 64. FDA Noise-Analysis Circuit

Figure 64 shows the noise powers for each term. When the R_F and R_G terms are matched on each side, the total differential output noise is the root sum of squares (RSS) of these separate terms. Using NG (noise gain) ≡ 1 + R_F / R_G, the total output noise is shown in Equation 8. Each resistor noise term is a 4-k*T*R power.

$$e_{no} = \sqrt{(e_{ni}NG)^2 + 2(i_nR_F)^2 + 2(4kTR_FNG)} \quad (8)$$

Application Information (continued)

The first term is the differential input spot noise times the noise gain. The second term is the input current noise terms times the feedback resistor (and because there are two terms, the power is two times one of the terms). The last term is the output noise resulting from the R_F and R_G resistors (again times two) for the output noise power of each side added together. Using the exact values for a 50-Ω, matched, single-ended to differential gain, sweep with 127 Ω (plus an internal 25 Ω) and the intrinsic noise e_{ni} = 1.25 nV and i_n = 3.5 pA for the LMH5401, which gives an output spot noise from Equation 8. Then, dividing by the signal gain set through internal resistors (A_V), gives the input-referred, spot-noise voltage (e_i) of 1.35 nV/√Hz. Note that for the LMH5401 the current noise is an insignificant noise contributor because of the low value of R_F.

9.1.4 Noise Figure

Noise figure (NF) is a helpful measurement in an RF system design. The basis of this calculation is to define how much thermal noise the system (or even on the component) adds to this input signal. All systems are assumed to have a starting thermal noise power of –174 dBm/√Hz at room temperature calculated from $P_{(dBW)}$ = 10 × log (kTB), where T is temperature in Kelvin (290k), B is bandwidth in Hertz (1 Hz), and k is Boltzmann's constant 1.38 × $10^{–23}$ (J / K). Whenever an element is placed in a system, additional noise is added beyond the thermal noise floor. The noise factor (NF) helps calculate the noise figure and is the ratio between the input SNR and the output SNR. Input SNR includes the noise contribution from the resistive part of the source impedance, Z_S. NF is relative to the source impedance used in the measurement or calculation because capacitors and inductors are known to be noiseless. Equation 9 calculates NF:

$$NF = 10 \log (e_{no}^2 / en_{Zs}) \quad (9)$$

where

- $e_{n(Zs)}$ is the thermal noise of the source resistance and equal to 4 kTR_S $(GD_T)^2$,
- G is the voltage gain of the amplifier.

From Equation 10, NF is approximately equal to 10 dB which is the just above the actual value of 9.6 dB measured on the bench at 200 MHz when referenced to 50 Ω and as shown in Figure 59.

$$D_T = \frac{R_T}{R_S + R_T} \quad (10)$$

For thermal noise calculations with different source resistances, Equation 11 can be used to calculate the NF change with a new source resistance. For example, Equation 9 uses a source resistance of 50 Ω. By using a source of 100 Ω, the new noise figure calculation (Equation 11) yields an NF of 6.6 dB, which provides a 3-dB improvement that results from the increase in Z_S.

$$e_{n(Zs)} = kTRs \quad (11)$$

9.1.5 Thermal Considerations

The LMH5401 is packaged in a space-saving UQFN package that has a thermal coefficient ($R_{\theta JA}$) of 101°C/W. Limit the total power dissipation to keep the device junction temperature below 150°C for instantaneous power and below 125°C for continuous power.

9.2 Typical Application

The LMH5401 is designed as a single-ended-to-differential (SE-DE) and differential-to-differential (DE-DE) gain block configured with external resistors and gain-stable single-ended to differential for NG ≥ 2 V/V . The LMH5401 has no low-end frequency cutoff and has 8-GHz gain product bandwidth. The LMH5401 is a substitute for a balun transformer in many applications.

The R_O resistors serve to match the filter impedance to the 20-Ω amplifier differential output impedance. If no filter is used, these resistors may not be required if the ADC is located very close to the LMH5401. If there is a transmission line between the LMH5401 and the ADC, then the R_O resistors must be sized to match the transmission line impedance. A typical application driving an ADC is shown in Figure 65.

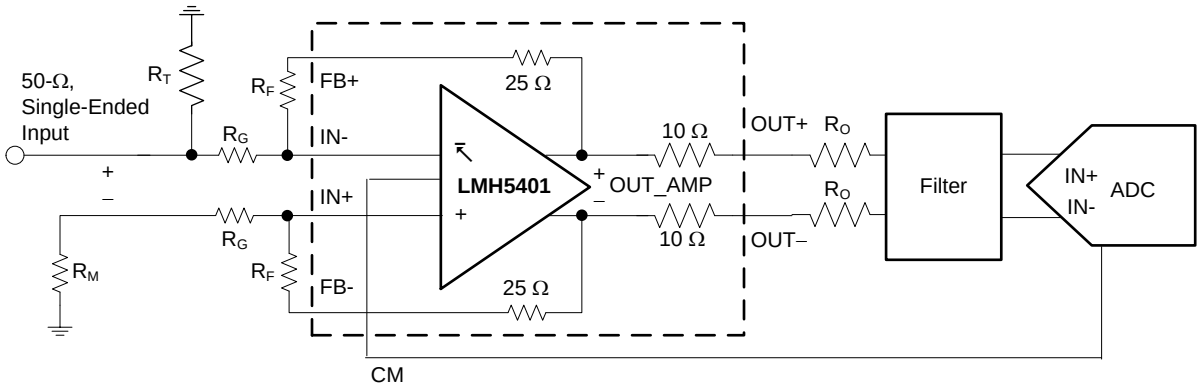


Figure 65. Single-Ended Input ADC Driver

9.2.1 Design Requirements

The main design requirements are to keep the amplifier input and output common-mode voltages compatible with the ADC requirements and the amplifier requirements. Using split power supplies may be required.

Typical Application (continued)

9.2.2 Detailed Design Procedure

9.2.2.1 Driving Matched Loads

The LMH5401 has on-chip output resistors, however, for most load conditions additional resistance must be added to the output to match a desired load. Table 4 lists the matching resistors for some common load conditions.

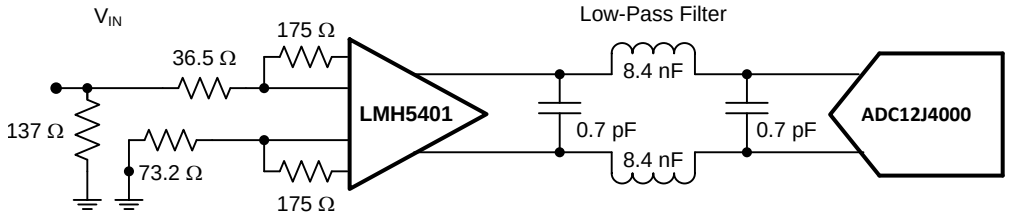
Table 4. Load Component Values(1)

LOAD (R_L)	R_{O+} AND R_{O-} FOR A MATCHED TERMINATION	TOTAL LOAD RESISTANCE AT AMPLIFIER OUTPUT	TERMINATION LOSS
50 Ω	15 Ω	100 Ω	6 dB
100 Ω	40 Ω	200 Ω	6 dB
200 Ω	90 Ω	400 Ω	6 dB
400 Ω	190 Ω	800 Ω	6 dB
1 kΩ	490 Ω	2000 Ω	6 dB

(1) The total load includes termination resistors.

9.2.2.2 Driving Unmatched Loads For Lower Loss

When the LMH5401 and the load can be placed very close together, back-terminated transmission lines are not required. In this case, the 6-dB loss can be reduced significantly. One example is shown in Figure 66.



NOTE: Amplifier gain = 12 dB and net gain to ADC = 10.5 dB.

Figure 66. Low-Loss ADC

9.2.2.3 Driving Capacitive Loads

With high-speed signal paths, capacitive loading is highly detrimental to the signal path, as shown in Figure 67. Designers must make every effort to reduce parasitic loading on the amplifier output pins. The device on-chip resistors are included to isolate the parasitic capacitance associated with the package and the PCB pads that the device is soldered to. The LMH5401 is stable with most capacitive loads ≤ 10 pF; however, bandwidth suffers with capacitive loading on the output.

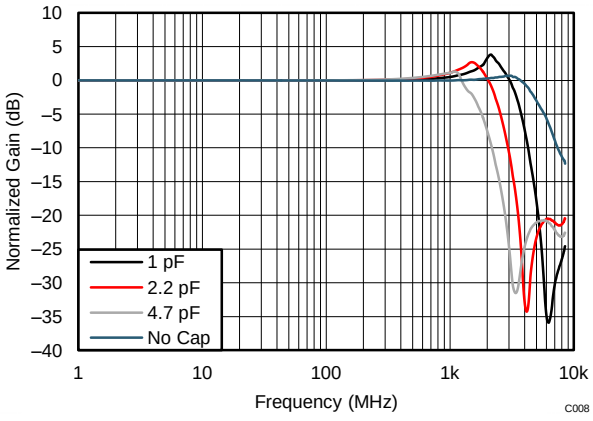


Figure 67. Frequency Response with Capacitive Load

9.2.2.4 Driving ADCs

The LMH5401 is designed and optimized for the highest performance to drive differential input ADCs. Figure 68 shows a generic block diagram of the LMH5401 driving an ADC. The primary interface circuit between the amplifier and the ADC is usually a filter of some type for antialias purposes, and provides a means to bias the signal to the input common-mode voltage required by the ADC. Filters range from single-order real RC poles to higher-order LC filters, depending on the requirements of the application. Output resistors (R_O) are shown on the amplifier outputs to isolate the amplifier from any capacitive loading presented by the filter.

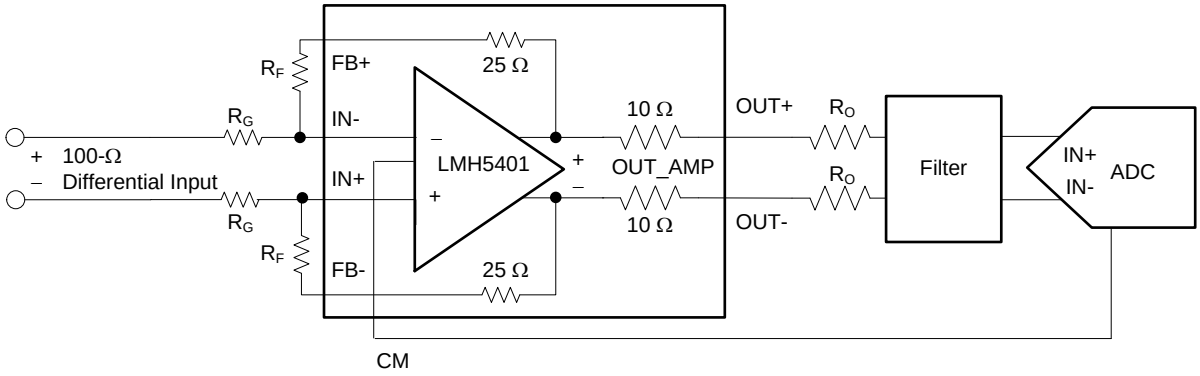


Figure 68. Differential ADC Driver Block Diagram

The key points to consider for implementation are the SNR, SFDR, and ADC input considerations, as shown in this section.

9.2.2.4.1 SNR Considerations

The signal-to-noise ratio (SNR) of the amplifier and filter can be calculated from the amplitude of the signal and the bandwidth of the filter. The noise from the amplifier is band-limited by the filter with the equivalent brick-wall filter bandwidth. The amplifier and filter noise can be calculated using Equation 12:

$$SNR_{AMP+FILTER} = 10 \times \log\left(\frac{V^2_O}{e^2_{FILTEROUT}}\right) = 20 \times \log\left(\frac{V_O}{e_{FILTEROUT}}\right)$$

where:

- $e_{FILTEROUT} = e_{NAMPOUT} \times \sqrt{ENB}$,
- $e_{NAMPOUT}$ = the output noise density of the LMH5401,
- ENB = the brick-wall equivalent noise bandwidth of the filter, and
- V_O = the amplifier output signal. (12)

For example, with a first-order (N = 1) band-pass or low-pass filter with a 30-MHz cutoff, the ENB is 1.57 × $f_{–3dB}$ = 1.57 × 30 MHz = 47.1 MHz. For second-order (N = 2) filters, the ENB is 1.22 × $f_{–3dB}$. When filter order increases, the ENB approaches $f_{–3dB}$ (N = 3 → ENB = 1.15 × $f_{–3dB}$; N = 4 → ENB = 1.13 × $f_{–3dB}$). Both V_O and $e_{FILTEROUT}$ are in RMS voltages. For example, with a 2-V_{PP} (0.707 V_{RMS}) output signal and a 30-MHz first-order filter, the SNR of the amplifier and filter is 70.7 dB with $e_{FILTEROUT}$ = 5.81 nV/√Hz × √47.1 MHz = 39.9 μV_{RMS}.

The SNR of the amplifier, filter, and ADC sum in RMS fashion is as shown in Equation 13 (SNR values in dB):

$$SNR_{SYSTEM} = -20 \times \log\left(\sqrt{10^{\frac{-SNR_{AMP+FILTER}}{10}} + 10^{\frac{-SNR_{ADC}}{10}}}\right) \quad (13)$$

This formula shows that if the SNR of the amplifier and filter equals the SNR of the ADC, the combined SNR is 3 dB lower (worse). Thus, for minimal degradation (< 1 dB) on the ADC SNR, the SNR of the amplifier and filter must be ≥ 10 dB greater than the ADC SNR. The combined SNR calculated in this manner is usually accurate to within ±1 dB of the actual implementation.

9.2.2.4.2 SFDR Considerations

The SFDR of the amplifier is usually set by the second-order or third-order harmonic distortion for single-tone inputs, and by the second-order or third-order intermodulation distortion for two-tone inputs. Harmonics and second-order intermodulation distortion can be filtered to some degree, but third-order intermodulation spurs cannot be filtered. The ADC generates the same distortion products as the amplifier, but as a result of the sampling and clock feedthrough, additional spurs (not linearly related to the input signal) are included.

When the spurs from the amplifier and filter are known, each individual spur can be directly added to the same spur from the ADC, as shown in Equation 14, to estimate the combined spur (spur amplitudes in dBc):

$$HDx_{SYSTEM} = -20 \times \log\left(10^{\frac{-HDx_{AMP+FILTER}}{20}} + 10^{\frac{-HDx_{ADC}}{20}}\right) \quad (14)$$

This calculation assumes the spurs are in phase, but usually provides a good estimate of the final combined distortion.

For example, if the spur of the amplifier and filter equals the spur of the ADC, then the combined spur is 6 dB higher. To minimize the amplifier contribution (< 1 dB) to the overall system distortion, the spur from the amplifier and filter must be approximately 19 dB lower in amplitude than that of the converter. The combined spur calculated in this manner is usually accurate to within ±6 dB of the actual implementation; however, higher variations can be detected as a result of phase shift in the filter, especially in second-order harmonic performance.

This worst-case spur calculation assumes that the amplifier and filter spur of interest is in phase with the corresponding spur in the ADC, such that the two spur amplitudes can be added linearly. There are two phase-shift mechanisms that cause the measured distortion performance of the amplifier-ADC chain to deviate from the expected performance calculated using Equation 14: common-mode phase shift and differential phase shift.

Common-mode phase shift is the phase shift detected equally in both branches of the differential signal path including the filter. Common-mode phase shift nullifies the basic assumption that the amplifier, filter, and ADC spur sources are in phase. This phase shift can lead to better performance than predicted when the spurs become phase shifted, and there is the potential for cancellation when the phase shift reaches 180°. However, a significant challenge exists in designing an amplifier-ADC interface circuit to take advantage of a common-mode phase shift for cancellation: the phase characteristic of the ADC spur sources are unknown, thus the necessary phase shift in the filter and signal path for cancellation is also unknown.

Differential phase shift is the difference in the phase response between the two branches of the differential filter signal path. Differential phase shift in the filter as a result of mismatched components caused by nominal tolerance can severely degrade the even-order distortion of the amplifier-ADC chain. This effect has the same result as mismatched path lengths for the two differential traces, and causes more phase shift in one path than the other. Ideally, the phase response over frequency through the two sides of a differential signal path are identical, such that even-order harmonics remain optimally out of phase and cancel when the signal is taken differentially. However, if one side has more phase shift than the other, then the even-order harmonic cancellation is not as effective.

Single-order RC filters cause very little differential phase shift with nominal tolerances of 5% or less, but higher-order LC filters are very sensitive to component mismatch. For instance, a third-order Butterworth band-pass filter with a 100-MHz center frequency and a 20-MHz bandwidth creates as much as 20° of differential phase imbalance in a SPICE Monte Carlo analysis with 2% component tolerances. Therefore, although a prototype may work, production variance is unacceptable. In ac-coupled applications that require second- and higher-order filters between the LMH5401 and the ADC, a transformer or balun is recommended at the ADC input to restore the phase balance. For DC-coupled applications where a transformer or balun at the ADC input cannot be used, using first- or second-order filters is recommended to minimize the effect of differential phase shift because of the component tolerance.

9.2.2.4.3 ADC Input Common-Mode Voltage Considerations : AC-Coupled Input

The input common-mode voltage range of the ADC must be respected for proper operation. In an AC-coupled application between the amplifier and the ADC, the input common-mode voltage bias of the ADC is accomplished in different ways depending on the ADC. Some ADCs use internal bias networks such that the analog inputs are automatically biased to the required input common-mode voltage if the inputs are AC-coupled with capacitors (or if the filter between the amplifier and ADC is a band-pass filter). Other ADCs supply the required input common-mode voltage from a reference voltage output pin (often called CM or V_{CM}). With these ADCs, the AC-coupled input signal can be re-biased to the input common-mode voltage by connecting resistors from each input to the CM output of the ADC, as Figure 69 shows. However, the signal is attenuated because of the voltage divider created by R_{CM} and R_O.

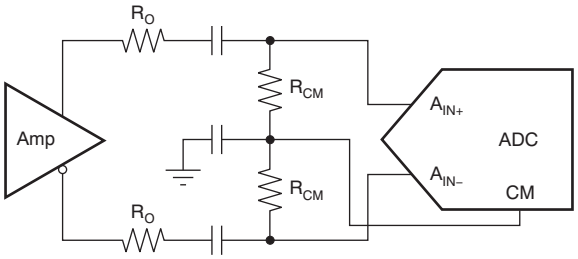


Figure 69. Biasing AC-Coupled ADC Inputs Using the ADC CM Output

The signal can be re-biased when ac coupling; thus, the output common-mode voltage of the amplifier is a *don't care* for the ADC.

9.2.2.4.4 ADC Input Common-Mode Voltage Considerations : DC-Coupled Input

DC-coupled applications vary in complexity and requirements, depending on the ADC. One typical requirement is resolving the mismatch between the common-mode voltage of the driving amplifier and the ADC. Devices such as the ADS5424 require a nominal 2.4-V input common-mode, whereas other devices such as the ADS5485 require a nominal 3.1-V input common-mode; still others such as the ADS6149 and the ADS4149 require 1.5 V and
0.95 V, respectively. As shown in Figure 70, a resistor network can be used to perform a common-mode level shift. This resistor network consists of the amplifier series output resistors and pull-up or pull-down resistors to a reference voltage. This resistor network introduces signal attenuation that may prevent the use of the full-scale input range of the ADC. ADCs with an input common-mode closer to the typical 2.5-V LMH5401 output common-mode are easier to DC-couple, and require little or no level shifting.

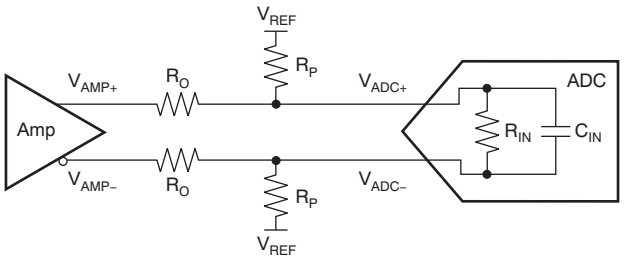


Figure 70. Resistor Network to DC Level-Shift Common-Mode Voltage

For common-mode analysis of the circuit in Figure 70, assume that $V_{AMP\pm} = V_{CM}$ and $V_{ADC\pm} = V_{CM}$ (the specification for the ADC input common-mode voltage). V_{REF} is chosen to be a voltage within the system higher than V_{CM} (such as the ADC or amplifier analog supply) or ground, depending on whether the voltage must be pulled up or down, respectively; R_O is chosen to be a reasonable value, such as 24.9 Ω. With these known values, R_P can be found by using Equation 15:

$$R_P = R_O \left(\frac{V_{ADC} - V_{REF}}{V_{AMP} - V_{ADC}} \right) \quad (15)$$

Shifting the common-mode voltage with the resistor network comes at the expense of signal attenuation. Modeling the ADC input as the parallel combination of a resistance (R_{IN}) and capacitance (C_{IN}) using values taken from the ADC data sheet, the approximate differential input impedance (Z_{IN}) for the ADC can be calculated at the signal frequency. The effect of C_{IN} on the overall calculation of gain is typically minimal and can be ignored for simplicity (that is, $Z_{IN} = R_{IN}$). The ADC input impedance creates a divider with the resistor network; the gain (attenuation) for this divider can be calculated by Equation 16:

$$GAIN = \left(\frac{2R_P \parallel Z_{IN}}{2R_O + 2R_P \parallel Z_{IN}} \right) \quad (16)$$

With ADCs that have internal resistors that bias the ADC input to the ADC input common-mode voltage, the effective R_{IN} is equal to twice the value of the bias resistor. For example, the ADS5485 has a 1-kΩ resistor tying each input to the ADC V_{CM}; therefore, the effective differential R_{IN} is 2 kΩ.

The introduction of the R_P resistors modifies the effective load that must be driven by the amplifier. Equation 17 shows the effective load created when using the R_P resistors.

$$R_L = 2R_O + 2R_P \parallel Z_{IN} \quad (17)$$

The R_P resistors function in parallel to the ADC input such that the effective load (output current) at the amplifier output is increased. Higher current loads limit the LMH5401 differential output swing.

By using the gain and knowing the full-scale input of the ADC ($V_{ADC\ FS}$), the required amplitude to drive the ADC with the network can be calculated using Equation 18:

$$V_{AMP\ PP} = \frac{V_{ADC\ FS}}{GAIN} \quad (18)$$

As with any design, testing is recommended to validate whether the specific design goals are met.

9.2.2.5 GSPS ADC Driver

The LMH5401 can drive the full Nyquist bandwidth of ADCs with sampling rates up to 4 GSPS, as shown in Figure 71. If the front-end bandwidth of the ADC is more than 2 GHz, use a simple noise filter to improve SNR. Otherwise, the ADC can be connected directly to the amplifier output pins. Matching resistors may not be required, however allow space for matching resistors on the preliminary design.

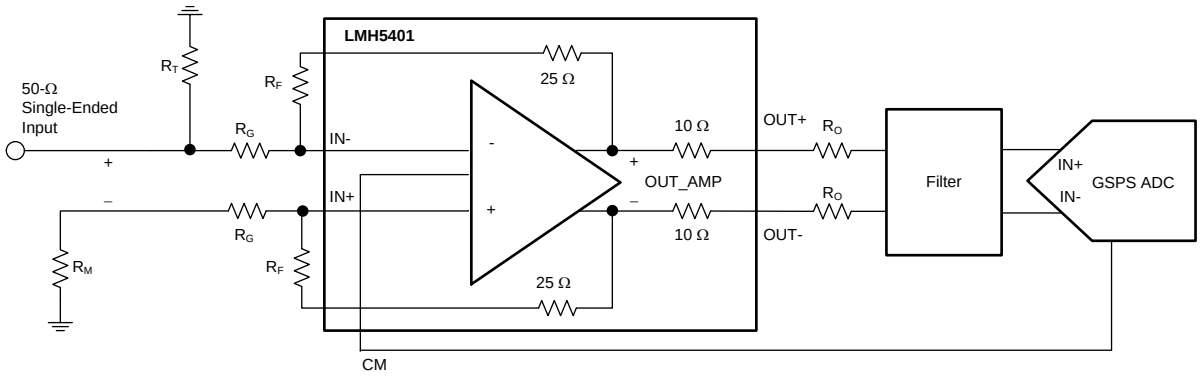


Figure 71. GSPS ADC Driver

9.2.2.6 Common-Mode Voltage Correction

The LMH5401 can set the output common-mode voltage to within a typical value of ±30 mV. If greater accuracy is desired, a simple circuit can improve this accuracy by an order of magnitude. A precision, low-power operational amplifier is used to sense the error in the output common-mode of the LMH5401 and corrects the error by adjusting the voltage at the CM pin. In Figure 72, the precision of the op amp replaces the less accurate precision of the LMH5401 common-mode control circuit while still using the LMH5401 common-mode control circuit speed. The op amp in this circuit must have better than a 1-mV input-referred offset voltage and low noise. Otherwise the specifications are not very critical because the LMH5401 is responsible for the entire differential signal path.

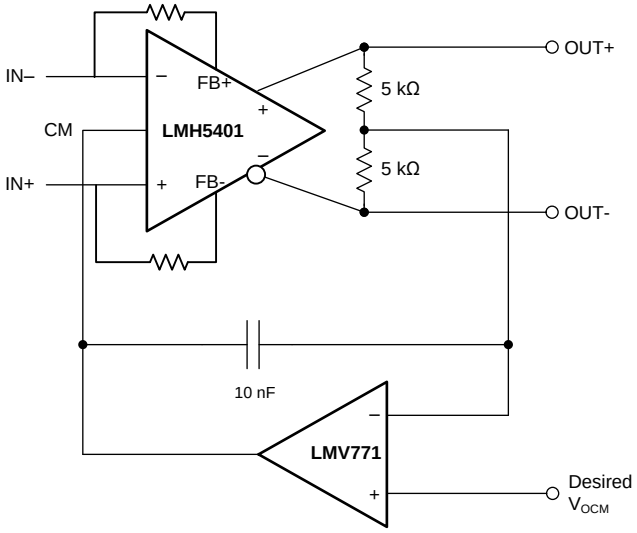


Figure 72. Common-Mode Correction Circuit

9.2.2.7 Active Balun

The LMH5401 is designed to convert single-ended signals to a differential output with high bandwidth and linearity, as shown in Figure 73. The LMH5401 can support DC coupling as well as AC coupling. The LMH5401 is smaller than any balun with low-frequency response and has balance errors that are excellent over a wide frequency range. As shown in Figure 74, the LMH5401 balance error is better than –40 dBc up to 1 GHz when used with a 5-V supply. Figure 75 plots the input return loss. The s-parameters demonstrate the performance of the configuration, which is comparable (or even better) to a balun.

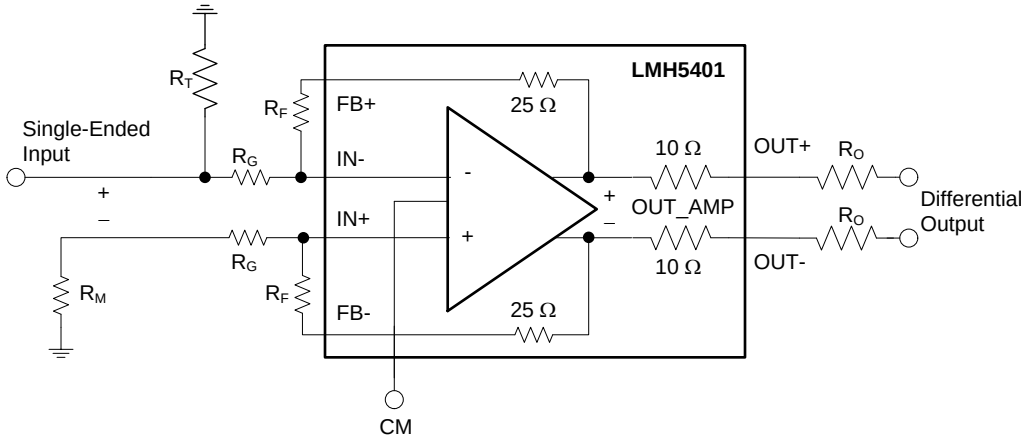


Figure 73. Active Balun

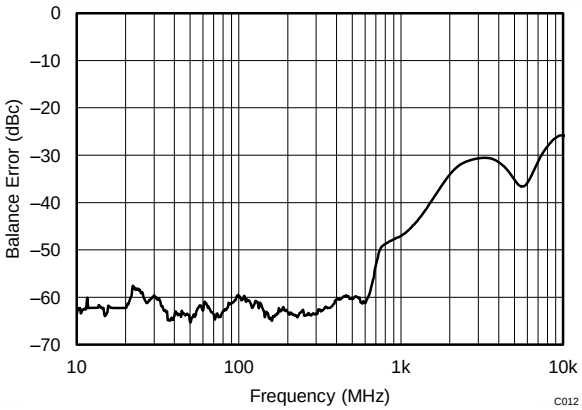


Figure 74. Balance Error

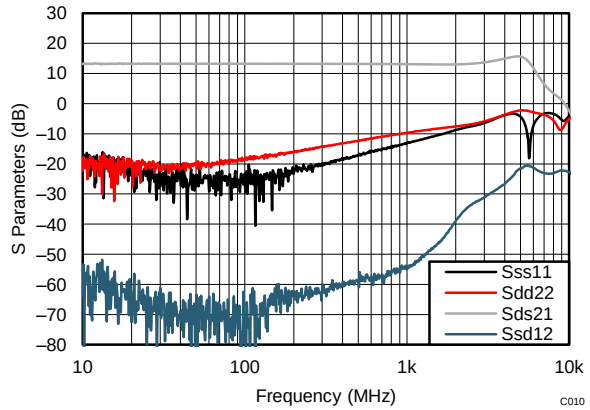


Figure 75. Input Return Loss

9.2.3 Application Curves

The LMH5401 has on-chip series output resistors to facilitate board layout. These resistors provide the LMH5401 extra phase margin in most applications. When the amplifier is used to drive a terminated transmission line or a controlled impedance filter, extra resistance is required to match the transmission line of the filter. In these applications, there is a 6 dB loss of gain. When the LMH5401 is used to drive loads that are not back-terminated there is a loss in gain resulting from the on-chip resistors. Figure 76 shows that loss for different load conditions. In most cases the loads are between 50 Ω and 200 Ω, where the on-chip resistor losses are 1.6 dB and 0.42 dB, respectively. Figure 77 shows the net gain realized by the amplifier for a large range of load resistances when the LMH5401 is configured for 16-dB gain.

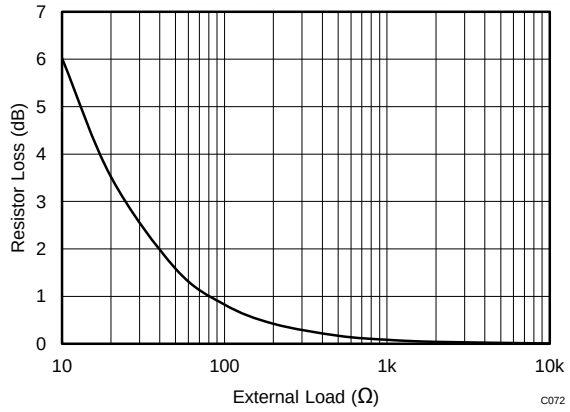


Figure 76. Gain Loss Resulting from On-Chip Output Resistors

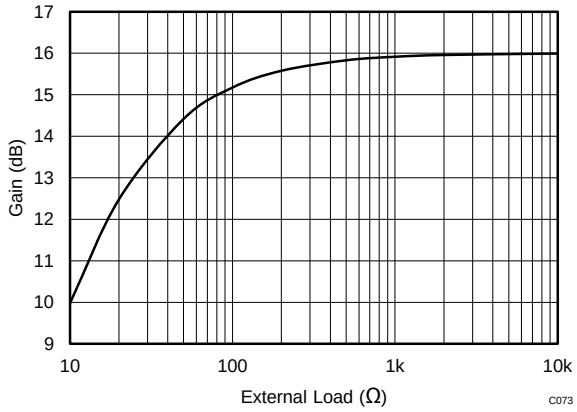


Figure 77. Net Gain versus Load Resistance

9.3 Do's and Don'ts

9.3.1 Do:

- Include a thermal design at the beginning of the project.
- Use well-terminated transmission lines for all signals.
- Use solid metal layers for the power supplies.
- Keep signal lines as straight as possible.
- Use split supplies where required.

9.3.2 Don't:

- Use a lower supply voltage than necessary.
- Use thin metal traces to supply power.
- Forget about the common-mode response of filters and transmission lines.

10 Power Supply Recommendations

The LMH5401 can be used with either split or single-ended power supplies. The ideal supply voltage is a 5-V total supply, split around the desired common-mode of the output signal swing. For example, if the LMH5401 is used to drive an ADC with a 1-V input common mode, then the designed supply voltages are 3.5 V and –1.5 V. The GND pin can then be connected to the system ground and the PD pin is ground referenced.

10.1 Supply Voltage

Using a 5-V power supply gives the best balance of performance and power dissipation. If power dissipation is a critical design criteria, a power supply as low as 3.3 V (±1.65) can be used. When using a lower power supply, the input common-mode and output swing capabilities are drastically reduced. Take care to study the common-mode voltages required before deciding on a lower-voltage power supply. In most cases, the extra performance achieved with 5-V supplies is worth the power.

10.2 Single-Supply

Single-supply voltages from 3.3 V to 5 V are supported. When using a single supply check both the input and output common-mode voltages that are required by the system.

10.3 Split-Supply

In general, split-supplies allow the most flexibility in system design. To operate as split-supply, apply the positive supply voltage to VS+, the negative supply voltage to VS–, and the ground reference to GND. Note that supply voltages are not required to be symmetrical. Provided the total supply voltage is between 3.3 V and 5.25 V, any combination of positive and negative supply voltages is acceptable. This feature is often used when the output common-mode voltage must be set to a particular value. For best performance, the power-supply voltages are symmetrical around the desired output common-mode voltage. The input common-mode voltage range is much more flexible than the output.

10.4 Supply Decoupling

Power-supply decoupling is critical to high-frequency performance. Onboard bypass capacitors are used on the LMH5401EVM; however, the most important component of the supply bypassing is provided by the PCB. As shown in Figure 78, there are multiple vias connecting the LMH5401 power planes to the power-supply traces. These vias connect the internal power planes to the LMH5401. VS+ and VS– must be connected to the internal power planes with several square centimeters of continuous plane in the immediate vicinity of the amplifier. The capacitance between these power planes provides the bulk of the high-frequency bypassing for the LMH5401.

11 Layout

11.1 Layout Guidelines

With a GBP of 8 GHz, layout for the LMH5401 is critical and nothing can be neglected. To simplify board design, the LMH5401 has on-chip resistors that reduce the effect of off-chip capacitance. For this reason, TI does not recommend cutting the ground layer below the LMH5401. The recommendation to not cut the ground plane under the amplifier input and output pins is different than many other high-speed amplifiers, but parasitic inductance is more harmful to the LMH5401 performance than parasitic capacitance. By leaving the ground layer under the device intact, parasitic inductance of the output and power traces is minimized. The DUT portion of the evaluation board layout is shown in Figure 78 and Figure 79.

The EVM uses long-edge capacitors for the decoupling capacitors, which reduces series resistance and increases the resonant frequency. Vias are also placed to the power planes before the bypass capacitors. Although not evident in the top layer, two vias are used at the capacitor in addition to the two vias underneath the device.

The output matching resistors are 0402 size and are placed very close to the amplifier output pins, which reduces parasitic inductance and capacitance. The use of 0603 output matching resistors produces a measurable decrease in bandwidth.

When the signal is on a 50-Ω controlled impedance transmission line, the layout then becomes much less critical. The transition from the 50-Ω transmission line to the amplifier pins is the most critical area.

The CM pin requires a bypass capacitor. Place this capacitor near the device. See *LMH5401EVM Evaluation Module* for more details on board layout and design.

11.2 Layout Example

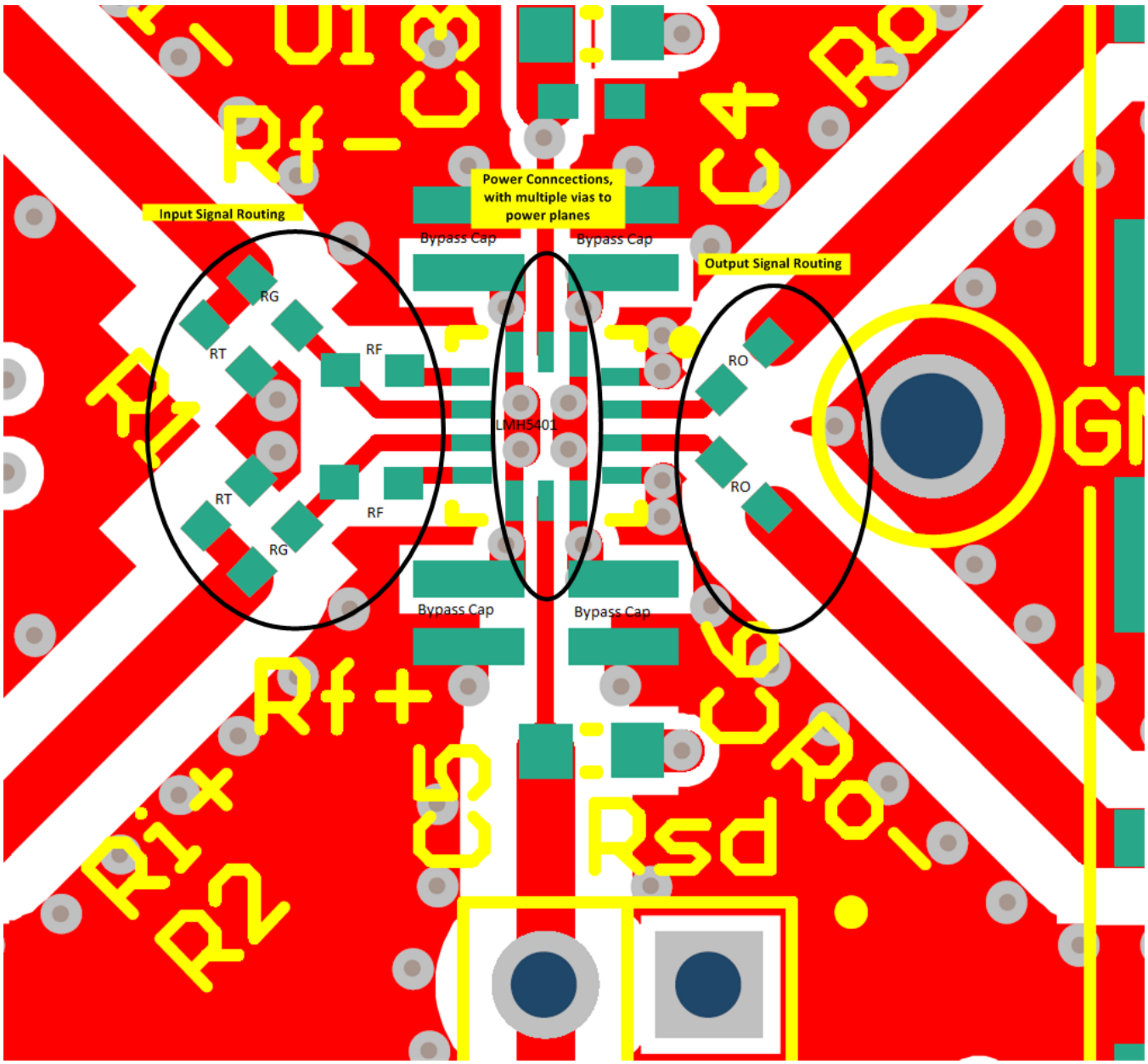


Figure 78. Layout Example

Layout Example (continued)

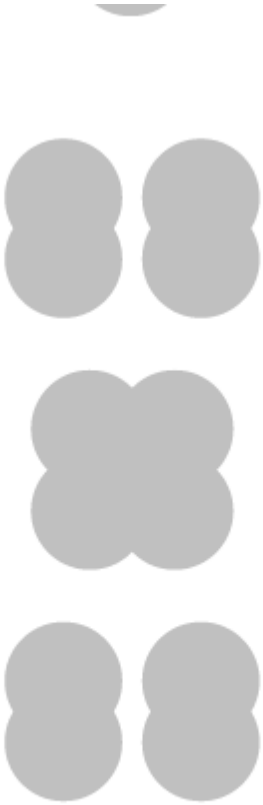


Figure 79. EVM Layout Ground Layer Showing Solid Ground Plane

12 デバイスおよびドキュメントのサポート

12.1 デバイス・サポート

12.1.1 デバイスの項目表記

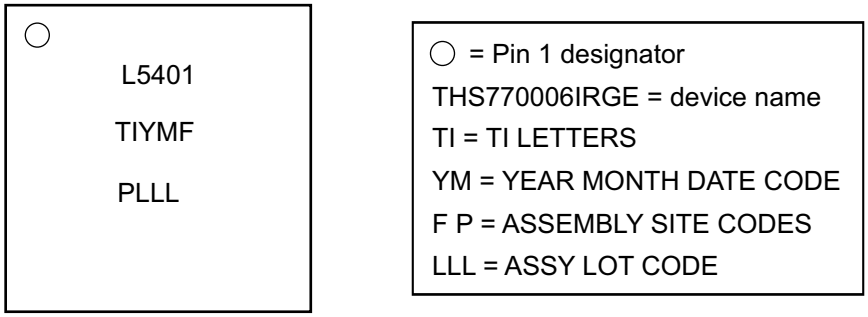


図 80. デバイスのマーキング情報

12.2 ドキュメントのサポート

12.2.1 関連資料

関連資料については、以下を参照してください。

- テキサス・インスツルメンツ、*『LMH3401 7GHz、超広帯域、固定ゲイン、完全差動アンプ』*
- テキサス・インスツルメンツ、*『LMH6554 2.8GHz、超高直線性完全差動アンプ』*
- テキサス・インスツルメンツ、*『LMH6552 1.5GHz完全差動アンプ』*
- テキサス・インスツルメンツ、*『ADC12D1800RF 12ビット、シングル3.6GSPS RFサンプリングADC』*
- テキサス・インスツルメンツ、*『ADS5424 14ビット、105MSPSアナログ/デジタル・コンバータ』*
- テキサス・インスツルメンツ、*『ADS548x 16ビット、170/200MSPSアナログ/デジタル・コンバータ』*
- テキサス・インスツルメンツ、*『ADS614x、ADS612x 14/12ビット、250/210MSPS ADC、DDR LVDSおよび並列CMOS出力対応』*
- テキサス・インスツルメンツ、*『ADS412x、ADS414x 12/14ビット、160/250MSPS、超低消費電力ADC』*
- テキサス・インスツルメンツ、*『LMH5401EVM評価モジュール』*
- テキサス・インスツルメンツ、*『AN-2188 アンプとADCの間: 通信システムにおけるフィルタ損失の管理』*
- テキサス・インスツルメンツ、*『AN-2235 LMH6517/21/22および他の高速IF/RF帰還型アンプの基板設計』*
- テキサス・インスツルメンツ、*『LMH5401 TINAマクロモデル』*

12.3 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、ti.comのデバイス製品フォルダを開いてください。右上の隅にある「*通知を受け取る*」をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

12.4 コミュニティ・リソース

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

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設計サポート ***TIの設計サポート*** 役に立つE2Eフォーラムや、設計サポート・ツールをすばやく見つけることができます。技術サポート用の連絡先情報も参照できます。

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静電気放電はわずかな性能の低下から完全なデバイスの故障に至るまで、様々な損傷を与えます。高精度の集積回路は、損傷に対して敏感であり、極めてわずかなパラメータの変化により、デバイスに規定された仕様に適合しなくなる場合があります。

12.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。この情報は、そのデバイスについて利用可能な最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LMH5401IRMSR	Active	Production	UQFN (RMS) | 14	3000 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 85	L5401
LMH5401IRMSR.A	Active	Production	UQFN (RMS) | 14	3000 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 85	L5401
LMH5401IRMST	Active	Production	UQFN (RMS) | 14	250 | SMALL T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 85	L5401
LMH5401IRMST.A	Active	Production	UQFN (RMS) | 14	250 | SMALL T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 85	L5401

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

OTHER QUALIFIED VERSIONS OF LMH5401 :

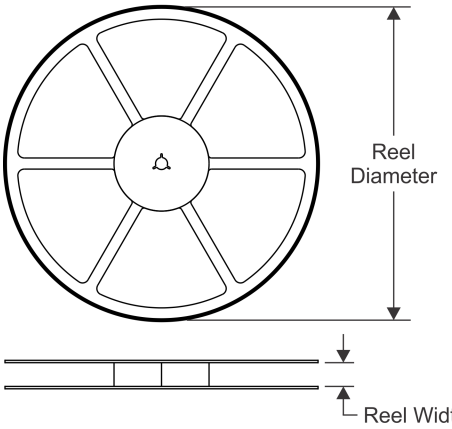
- Space : LMH5401-SP

NOTE: Qualified Version Definitions:

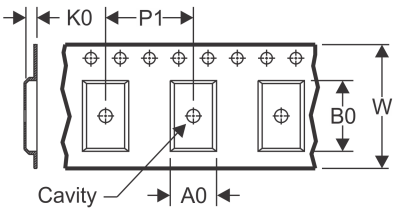
- Space - Radiation tolerant, ceramic packaging and qualified for use in Space-based application

TAPE AND REEL INFORMATION

REEL DIMENSIONS

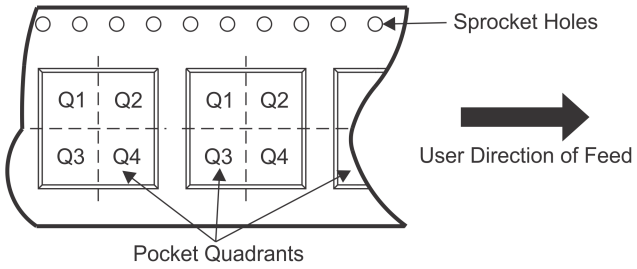


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

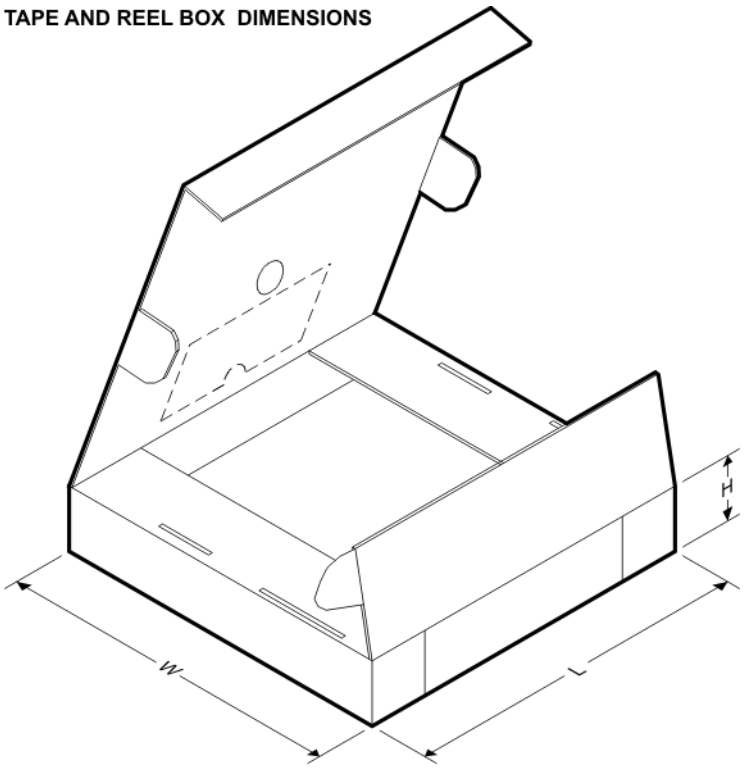
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

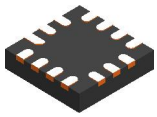
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMH5401IRMSR	UQFN	RMS	14	3000	180.0	9.5	2.7	2.7	0.7	4.0	8.0	Q2
LMH5401IRMST	UQFN	RMS	14	250	180.0	9.5	2.7	2.7	0.7	4.0	8.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

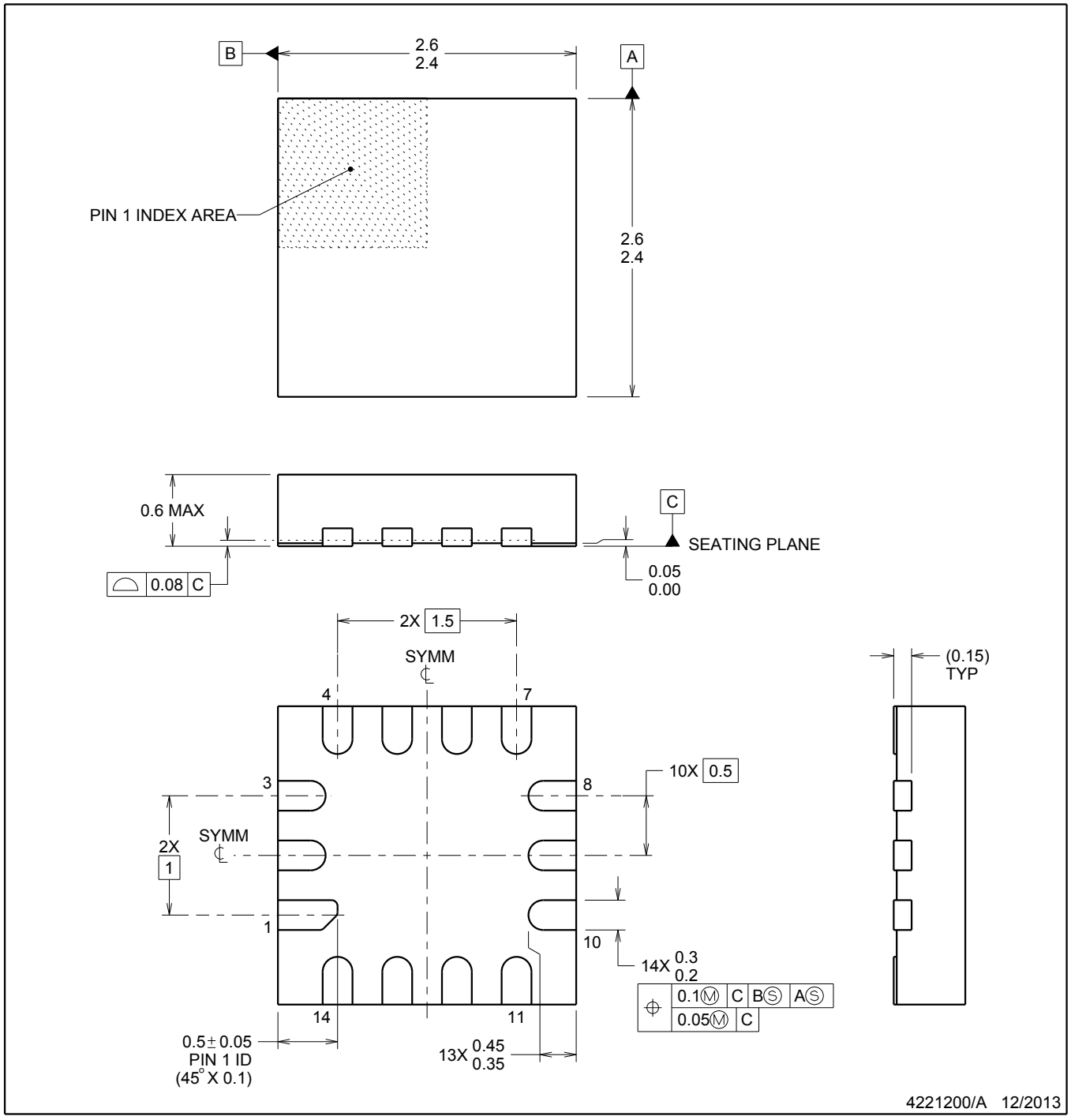
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMH5401IRMSR	UQFN	RMS	14	3000	205.0	200.0	30.0
LMH5401IRMST	UQFN	RMS	14	250	205.0	200.0	30.0



RMS0014A

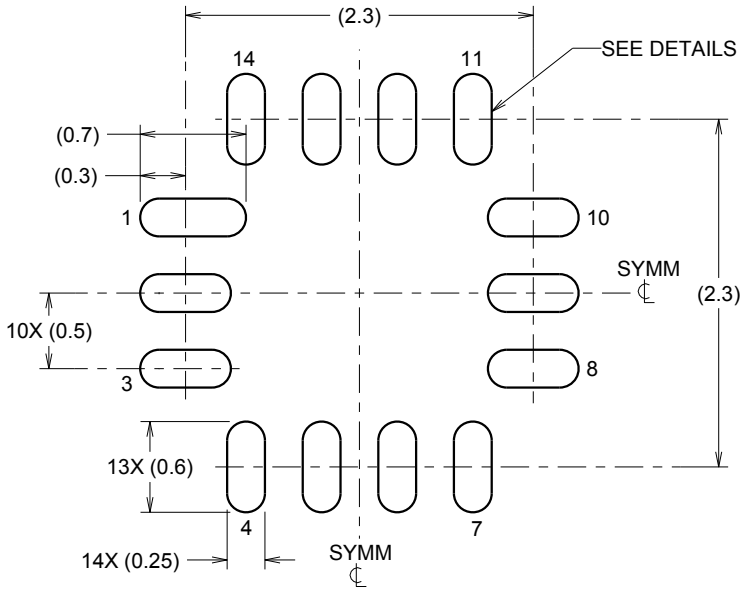
UQFN - 0.6 mm max height

UQFN

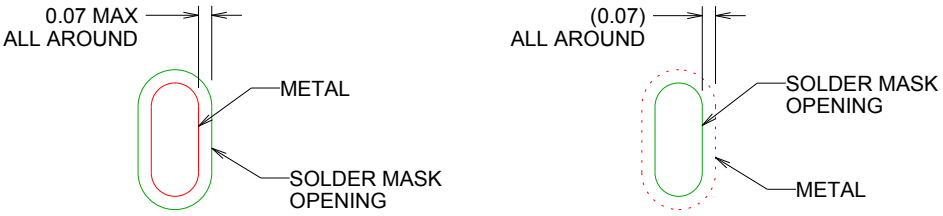


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:20X



NON SOLDER MASK
DEFINED
(PREFERRED)

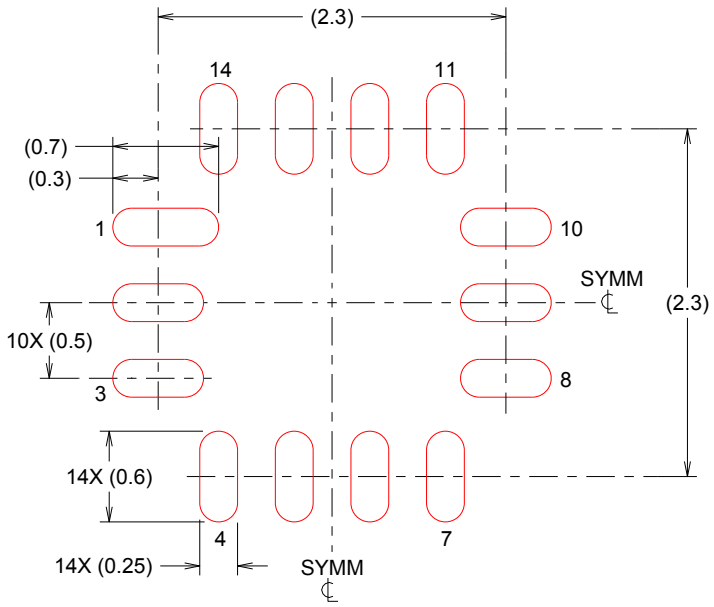
SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4221200/A 12/2013

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see QFN/SON PCB application report in literature No. SLUA271 (www.ti.com/lit/slua271).



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:20X

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NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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最終更新日：2025 年 10 月