TEXAS INSTRUMENTS
LMK04832-SP
JAJSJN4C – MAY 2020 – REVISED NOVEMBER 2022

LMK04832-SP 宇宙グレード、超低ノイズ、JESD204B 対応、デュアル・ループ・クロック・ジッタ・クリーナ

1 特長

- SMD #5962R1723701VXC
  - 総照射線量耐性:100krad (ELDRS フリー)
  - SEL 耐性 > 120MeV × cm^2/mg
  - SEFI 耐性 > 120MeV × cm^2/mg
- 最高クロック出力周波数:3255 MHz
- マルチモード:デュアル PLL、シングル PLL、クロック・ディストリビューション
- 6GHz の外付け VCO または分配入力
- 超低ノイズ (2500MHz 時):
  - 54fs RMS ジッタ (12kHz～20MHz)
  - 64fs RMS ジッタ (100Hz～20MHz)
  - -157.6dBc/Hz のノイズ・フロア
- 超低ノイズ (3200MHz 時):
  - 61fs RMS ジッタ (12kHz～20MHz)
  - 67fs RMS ジッタ (100Hz～100MHz)
  - -156.5dBc/Hz のノイズ・フロア
- PLL2
  - PLL FOM: －230dBc/Hz
  - PLL 1/f: －128dBc/Hz
  - 位相検出速度:最高 320MHz
  - 2 つの VCO を内蔵:2440～2600MHz および 2945～3255MHz
- 最大 14 個の差動デバイス・クロック
  - CML、LVPECL、LCPECL、HSDS、LVDS、2xLVCMOS プログラマブル出力
- 最大 1 個のバッファ付き VCXO/XO 出力
  - LVPECL、LVDS、2xLVCMOS をプログラム可能
- 1-1023 の CLKout 分周器
- 1-8191 の SYSREF 分周器
- SYSREF クロックの 25ps ステップ・アナログ遅延
- デバイス・クロックおよび SYSREF のデジタル遅延および動的デジタル遅延
- PLL1 によるホールドオーバー・モード
- PLL1 または PLL2 による 0 遅延
- 周囲温度範囲:-55℃～125℃

2 アプリケーション

- 通信ペイロード
- レーダー画像処理ペイロード
- コマンドとデータの取り扱い

3 概要

LMK04832-SP は、高水準の性能を誇る、JEDEC JESD204B に準拠した航空宇宙アプリケーション向けクロック・コンディショナーです。

PLL2 からの 14 のクロック出力を構成して、7 つの JESD204B コンバータ、あるいはデバイス・クロックおよび SYSREF クロックを使用するその他のロジック・デバイスを駆動できます。DC および AC 結合により SYSREF を生成することが可能です。JESD204B アプリケーションに限らず、従来のクロッキング・システム向けに 14 の出力をそれぞれ高性能出力として個別に構成できます。

LMK04832-SP は、SYSREF の生成またはリクロッキングの有無にかかわらず、デュアル PLL、シングル PLL、またはクロック分配モードで動作するように構成できます。PLL2 は内蔵 VCO でも外付け VCO でも動作します。

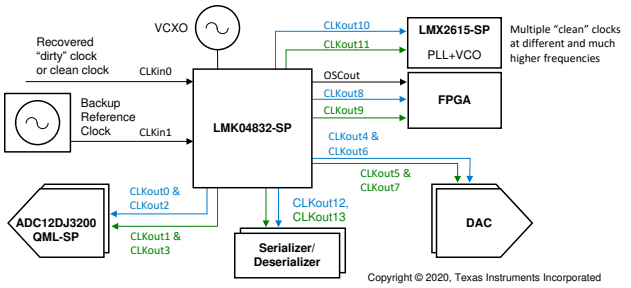
高性能である上に、電力と性能のトレードオフ、デュアル VCO、動的デジタル遅延、ホールドオーバーといった機能を備えた LMK04832-SP は、柔軟性のある高性能クロック・ツリーを提供できます。

LMK04832-SP は 10.9mm × 10.9mm の 64 ピン CFP パッケージで供給されます。

パッケージ情報

部品番号	種類	パッケージ(1)
SN0064HBE	メカニカル・サンプル(2)	非導電性タイ・バー付き 64 ピン・セラミック (HBE0064B)
LMK04832W/EM	エンジニアリング・サンプル(3)	
5962R1723701VXC	放射線耐性強化の保証	

(1) 利用可能なパッケージについては、このデータシートの末尾にある注文情報を参照してください。
(2) これらのユニットはパッケージのみで、ダイが含まれていません。評価のみを目的としています
(3) これらのユニットは製造や飛行には適していません。これらはエンジニアリング評価のみを目的としています。



概略回路図

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4 Revision History

Changes from Revision B (December 2020) to Revision C (November 2022)	Page
• 「製品情報」表を「パッケージ情報」に変更	1
• Updated セクション 6.1 to include cold sparing considerations ratings	6
• Updated セクション 6.6 to include t_{CHW} information	6
• Changed 図 6-1 to include t_{CHW} in diagram	12
• Changed 図 8-3 to include one-shot feature	20
• Changed 表 8-4	29
• Moved the *Power Supply Recommendations* and *Layout* sections to the *Application and Implementation* section	89
• Added *Cold Sparing Considerations* section	89
• Explained the damage prevention details to unpowered device when cold sparing is used	90

Changes from Revision A (August 2020) to Revision B (December 2020)	Page
• デバイスのステータスを「事前情報」から「量産データ」に変更	1

Changes from Revision * (March 2017) to Revision A (August 2020)	Page
• 文書全体の表、図、相互参照の採番方法を更新	1
• Added *Layout* section	91

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5 Pin Configuration and Functions

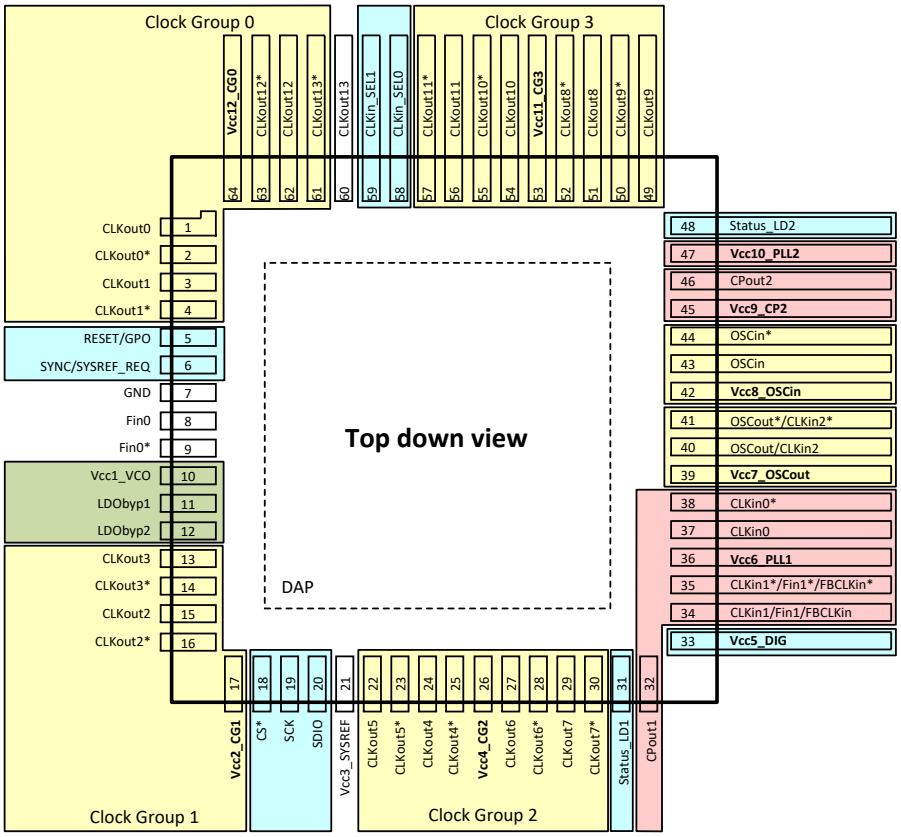


図 5-1. HBD CFP Package 64-Pin CFP Top View

表 5-1. Pin Functions

PIN		I/O	TYPE	DESCRIPTION
NO.	NAME			
1	CLKout0	O	Programmable	Clock output 0. For JESD204B systems suggest Device Clock.(2) Programmable formats: CML, LVPECL, LCPECL, or LVDS.
2	CLKout0*			
3	CLKout1	O	Programmable	Clock output 1. For JESD204B systems suggest SYSREF Clock.(2) Programmable formats: CML, LVPECL, LCPECL, LVDS, or 2xLVCMOS.
4	CLKout1*			
5	RESET/GPO	I	CMOS	Device reset input or GPO
6	SYNC/ SYSREF_REQ	I	CMOS	Synchronization input or SYSREF_REQ for requesting continuous SYSREF.
7	GND	–	GND	This pin should be grounded.
8, 9	Fin0/Fin0*	I	ANLG	High-speed input for external VCO or clock distribution. Supports /2 for frequency greater than 3250 MHz.
10	Vcc1_VCO	–	PWR	Power supply for VCO and clock distribution.
11	LDObyp1	–	ANLG	LDO Bypass, bypassed to ground with 10-µF capacitor.
12	LDObyp2	–	ANLG	LDO Bypass, bypassed to ground with a 0.1-µF capacitor.
13	CLKout3	O	Programmable	Clock output 3. For JESD204B systems suggest SYSREF Clock.(2) Programmable formats: CML, LVPECL, LCPECL, LVDS, or 2xLVCMOS.
14	CLKout3*			
15	CLKout2	O	Programmable	Clock output 2. For JESD204B systems suggest Device Clock.(2) Programmable formats: CML, LVPECL, LCPECL, or LVDS.
16	CLKout2*			
17	Vcc2_CG1	–	PWR	Power supply for clock outputs 2 and 3.

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表 5-1. Pin Functions (continued)

PIN		I/O	TYPE	DESCRIPTION
NO.	NAME			
18	CS*	I	CMOS	Chip Select
19	SCK	I	CMOS	SPI Clock
20	SDIO	I/O	CMOS	SPI Data
21	Vcc3_SYSREF	–	PWR	Power supply for SYSREF divider and SYNC.
22	CLKout5	O	Programmable	Clock output 5. For JESD204B systems suggest SYSREF Clock.(2) Programmable formats: CML, LVPECL, LCPECL, LVDS, or 2xLVCMOS.
23	CLKout5*			
24	CLKout4	O	Programmable	Clock output 4. For JESD204B systems suggest Device Clock.(2) Programmable formats: CML, LVPECL, LCPECL, or LVDS.
25	CLKout4*			
26	Vcc4_CG2	–	PWR	Power supply for clock outputs 4, 5, 6 and 7.
27	CLKout6	O	Programmable	Clock output 6. For JESD204B systems suggest Device Clock.(2) Programmable formats: CML, LVPECL, LCPECL, or LVDS.
28	CLKout6*			
29	CLKout7	O	Programmable	Clock output 7. For JESD204B systems suggest SYSREF Clock.(2) Programmable formats: CML, LVPECL, LCPECL, LVDS, or 2xLVCMOS.
30	CLKout7*			
31	Status_LD1	I/O	Programmable	Programmable status pin.
32	CPout1	O	ANLG	Charge pump 1 output.
33	Vcc5_DIG	–	PWR	Power supply for the digital circuitry.
34	CLKin1	I	ANLG	Reference Clock Input Port 1 for PLL1.
	FBCLKin			Feedback input for external clock feedback input (0–delay mode).
	Fin1			External VCO Input or clock distribution input.
35	CLKin1*	I	ANLG	Reference Clock Input Port 1 for PLL1.
	FBCLKin*			Feedback input for external clock feedback input (0–delay mode).
	Fin1*			External VCO Input or clock distribution input.
36	Vcc6_PLL1	–	PWR	Power supply for PLL1, charge pump 1, holdover DAC
37	CLKin0	I	ANLG	Reference Clock Input Port 0 for PLL1.
38	CLKin0*			
39	Vcc7_OSCout	–	PWR	Power supply for OSCout port.
40	OSCout	I/O	Programmable	Buffered output of OSCin port.
	CLKin2			Reference Clock Input Port 2 for PLL1.
41	OSCout*	I/O	Programmable	Buffered output of OSCin port.
	CLKin2*			Reference Clock Input Port 2 for PLL1.
42	Vcc8_OSCin	–	PWR	Power supply for OSCin
43	OSCin	I	ANLG	Feedback to PLL1 and reference input to PLL2. AC-coupled.
44	OSCin*			
45	Vcc9_CP2	–	PWR	Power supply for PLL2 Charge Pump.
46	CPout2	O	ANLG	Charge pump 2 output.
47	Vcc10_PLL2	–	PWR	Power supply for PLL2.
48	Status_LD2	I/O	Programmable	Programmable status pin.
49	CLKout9	O	Programmable	Clock output 9. For JESD204B systems suggest SYSREF Clock.(2) Programmable formats: CML, LVPECL, LCPECL, LVDS, or 2xLVCMOS.
50	CLKout9*			
51	CLKout8	O	Programmable	Clock output 8. For JESD204B systems suggest Device Clock.(2) Programmable formats: CML, LVPECL, LCPECL, LVDS, or 2xLVCMOS.
52	CLKout8*			
53	Vcc11_CG3	–	PWR	Power supply for clock outputs 8, 9, 10, and 11.
54	CLKout10	O	Programmable	Clock output 10. For JESD204B systems suggest Device Clock.(2) Programmable formats: CML, LVPECL, LCPECL, LVDS, or 2xLVCMOS.
55	CLKout10*			

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表 5-1. Pin Functions (continued)

PIN		I/O	TYPE	DESCRIPTION
NO.	NAME			
56	CLKout11	O	Programmable	Clock output 11. For JESD204B systems suggest SYSREF Clock.(2) Programmable formats: CML, LVPECL, LCPECL, LVDS, or 2xLVCMOS.
57	CLKout11*			
58	CLKin_SEL0	I/O	Programmable	Programmable status pin.
59	CLKin_SEL1	I/O	Programmable	Programmable status pin.
60	CLKout13	O	Programmable	Clock output 13. For JESD204B systems suggest SYSREF Clock.(2) Programmable formats: CML, LVPECL, LCPECL, LVDS, or 2xLVCMOS.
61	CLKout13*			
62	CLKout12	O	Programmable	Clock output 12. For JESD204B systems suggest Device Clock.(2) Programmable formats: CML, LVPECL, LCPECL, or LVDS.
63	CLKout12*			
64	Vcc12_CG0	–	PWR	Power supply for clock outputs 0, 1, 12, and 13.
DAP	DAP	–	GND	DIE ATTACH PAD, connect to GND.(1)

(1) The metal lid is internally grounded and attached to the DAP.
(2) Actual best allocation of device clocks and SYSREF depends upon frequency planning to group common frequencies.

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6 Specifications

6.1 絶対最大定格

自由気流での動作温度範囲内 (特に記述のない限り)(1)

記号	パラメータ	最小値	最大値	単位
V_{DD}、V_{DD_A}	電源電圧	-0.3	3.6	V
V_{IN}	入力電圧(2)	-0.3	V_{DD} + 0.3	V
I_{IN}	差動入力電流 (CLKinX/X*、OSCin/OSCin*、Fin)		5	mA
T_J	接合部温度		150	℃
T_{stg}	保存温度	-65	150	℃
	電源オフ時の CLKin0 および SYNC ピンへの最大電流(3)		7	mA
	電源なしのレシーバから外部入力への最大累積露光		10	時間

(1) 絶対最大定格の範囲外の動作は、デバイスの永続的な損傷の原因となる可能性があります。「絶対最大定格」は、このデータシートの「推奨動作条件」に示された値を超える状態で本製品が正常に動作することを暗黙的に示すものではありません。「絶対最大定格」の範囲内であっても「推奨動作条件」の範囲外で使用した場合、本デバイスは完全に機能するとは限らず、このことが本デバイスの信頼性、機能、性能に影響を及ぼし、本デバイスの寿命を縮める可能性があります。

(2) デバイスが電源オフ状態のとき、クロック入力ピン (CLKinX/FinX および OSCin) は最大 ±400mV の AC 結合信号を受け入れます。AC 結合時の電源なしデバイス入力の絶対制限値は、ピンの ±5mA (RMS) 電流制限によって決定されます。AC 結合クロック入力の ±5mA (RMS) 電流制限は、動作接合部温度全体にわたって、許容される動作周波数全体で 0.01µF の容量を使用して ±400mV の信号を結合することで達成されます。より小さな AC カップリング・コンデンサを使用する場合や、入力ピンの RMS 電流を制限するより小さな入力周波数を使用する場合は、より大きな信号を許容できる場合があります。

(3) LMK04832-SP は、外部電源のトランスミッタが短時間 (デバイスの最大 10 時間の寿命)、電源の入っていないレシーバに信号を送信しても、性能の低下を示しません。特性評価は、最大 VDD、125℃ の接合部温度、および電源オフ時の CLKin0 および SYNC ピンへの最大電流を使用して実施しました。

6.2 ESD 定格

記号	パラメータ	条件	値	単位
$V_{(ESD)}$	静電気放電	人体モデル (HBM)、ANSI/ESDA/JEDEC JS-001 に準拠、すべてのピン(1)	±2000	V
		デバイス帯電モデル (CDM)、ANSI/ESDA/JEDEC JS-002 準拠、すべてのピン(2)	±250	

(1) JEDEC のドキュメント JEP155 には、500V HBM であれば標準的な ESD 制御プロセスで安全な製造が可能であると記載されています。
(2) JEDEC のドキュメント JEP157 には、250V CDM であれば標準的な ESD 制御プロセスで安全な製造が可能であると記載されています。

6.3 推奨動作条件

ケースでの温度範囲内 (特に記述のない限り)

記号	パラメータ	最小値	公称値	最大値	単位
V_{DD}	IO 電源電圧	3.135	3.3	3.465	V
V_{DD_A}	コア電源電圧	3.135	3.3	3.465	V
T_A	周囲温度	-55		125	℃

6.4 熱に関する情報

記号	熱評価基準(1)	LMK04832-SP HBD (CFP) 64 ピン	単位
$R_{\theta JA}$	接合部から周囲への熱抵抗	21.8	℃/W
$R_{\theta JC(top)}$	接合部からケース (上面) への熱抵抗	6.7	℃/W
$R_{\theta JB}$	接合部から基板への熱抵抗	7.4	℃/W
Ψ_{JT}	接合部から上部への特性評価パラメータ	1.3	℃/W

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記号	熱評価基準(1)	LMK04832-SP HBD (CFP) 64 ピン	単位
Ψ_{JB}	接合部から基板への特性評価パラメータ	7.1	℃/W
$R_{\theta JC(bot)}$	接合部からケース (底面) への熱抵抗	0.5	℃/W

(1) 従来および最新の熱評価基準の詳細については、『半導体および IC パッケージの熱評価基準』アプリケーション・レポートを参照してください。

6.5 電気的特性

VDD、VDD_A = 3.3V±5%、-55℃≤TA≤125℃。標準値は、VDD = VDD_A = 3.3V、25℃ のときです (特に記述のない限り)。

記号	パラメータ	テスト条件		最小値	代表値	最大値	単位
消費電流							
I_{CC}	パワーダウン電源電流	デバイスの電源がオフになります			3.3	5	mA
	電源電流(1)	PLL1 は外部 VCXO にロックされ、PLL2 は内部 VCO にロックされます	バイパスに 4 個の CML 32mA クロック、3 個の LVDS クロック/12 LCPECL として 4 個の SYSREF LVDS として 3 個の SYSREF		1010		
			バイパスに 4 個の CML 32mA クロック、3 個の LVDS クロック/12 LCPECL (LOW 状態) として 4 個の SYSREF LVDS (LOW 状態) として 3 個の SYSREF		780		
			バイパスに 4 個の CML 32mA クロック 3 個の LVDS クロック/12 7 個の SYSREF 出力がパワーダウン		675		
CLKin 仕様							
f_{CLKinX}	LOS 回路	LOS_EN = 1		0.001		125	MHz
	PLL1	CLKinX-TYPE=1 (MOS)	AC 結合入力	0.001		250	
		CLKinX-TYPE=0 (バイポーラ)	AC 結合入力	0.001		750	
	PLL2	CLKinX_TYPE=0 (バイポーラ)	AC 結合入力	0.001		500	
	0 遅延	外部フィードバックによる 0 遅延 (CLKin1)	AC 結合入力	0.001		750	
	分配モード	CLKin1/Fin1 ピンのみ	AC 結合入力	0.001		3250	
スルー CLKin	入力スルーレート(2)			0.15	0.5		V/ns
$V_{CLKinX/Fin1}$	シングルエンド・クロック入力電圧	AC 結合入力ピン、GND 結合 AC 相補ピン		0.5		2.4	Vpp
V_{ID}CLKinX/Fin1	差動クロック入力電圧(3)	AC 結合		0.125		1.55	|V|
V_{SS}CLKinX/Fin1				0.25		3.1	Vpp
|VCLKinX-offset|	CLKinX/CLKinX* 間の DC オフセット電圧、各ピンは AC 結合	CLKin0/1/2 (バイポーラ)			0		|mV|
		CLKin0/1 (MOS)			55		
		CLKin2 (MOS)			20		
VCLKinVIH	高入力電圧	V_{CLKin}-V_{IH}	DC 結合入力	2		Vcc	V

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6.5 電気的特性 (continued)

VDD、VDD_A = 3.3V±5%、-55℃≤TA≤125℃。標準値は、VDD = VDD_A = 3.3V、25℃ のときです (特に記述のない限り)。

記号	パラメータ	テスト条件		最小値	代表値	最大値	単位
VCLKinVIL	低入力電圧	V_{CLKin}-V_{IL}	DC 結合入力	0		0.4	V
FIN0 入力ピン							
f_{Fin0}	外部入力周波数	AC 結合スルーレート > 150V/us	FIN0_DIV2_EN=1	1		3250	MHz
f_{Fin0}			FIN0_DIV2_EN=2	1		6400	MHz
V_{ID}Fin0	差動入力電圧	AC 結合		0.125		1.55	Vpp
V_{SS}Fin0				0.25		3.1	Vpp
PLL 1 仕様							
f_{PD1}	位相検出器周波数					40	MHz
PN10kHz	PLL 正規化 1/f ノイズ(4)	PLL1_CP_GAIN = 350µA			-117		dBc/Hz
		PLL1_CP_GAIN = 1550µA			-118		
PN FOM	PLL 性能指数(5)	PLL1_CP_GAIN = 350µA			-221.5		
		PLL1_CP_GAIN = 1550µA			-223		
I_{CPOUT1}	チャージ・ポンプの電流(6)	VCPout=Vcc/2 (0～15 で動作することをお客様に伝えるための注)	PLL1_CP_GAIN=0		50		µA
			PLL1_CP_GAIN=1		150		
			PLL1_CP_GAIN=2		250		
			PLL1_CP_GAIN=4		450		
			PLL1_CP_GAIN=8		850		
I_{CPout1}%MIS	チャージ・ポンプのシンク / ソースのミスマッチ	V_{CPout1} = VCC/2、T = 25℃	V_{CPout1} = VCC/2、T = 25℃		1	10	%
$I_{CPout1}V_{TUNE}$	チャージ・ポンプ電流変動の大きさとチャージ・ポンプ電圧との関係	0.5V < V_{CPout1} < V_{CC} - 0.5V T_A = 25℃	0.5V < V_{CPout1} < V_{CC} - 0.5V T_A = 25℃		4	10	%
I_{CPout1}% 温度	チャージ・ポンプ電流と温度変動との関係				4	10	%
I_{CPOUT1}TRI	チャージ・ポンプの TRI_STATE リーク電流					10	nA
OSCin 入力							
f_{OSCin}	EN_PLL2_REF_2X=0			0.001		500	MHz
	EN_PLL2_REF_2X=1			0.001		320	
スルー $_{OSCin}$	入力スルーレート			0.15	0.5		V/ns
V_{OSCin}	OSCin または OSCin* の入力電圧	AC 結合、シングルエンド、GND 結合 AC 未使用ピン		0.2		2.4	Vpp
V_{ID}OSCin	差動電圧スイング(3)	AC 結合		0.2		1.55	|V|
V_{SS}OSCin				0.4		3.1	Vpp
V_{CLKinX}Offset	CLKinX/CLKinX* 間の DC オフセット電圧、各ピンは AC 結合				20		mV
PLL 2 仕様							
f_{PD}	位相検出器周波数					320	MHz
PN10kHz	PLL 正規化 1/f ノイズ(4)	PLL2_CP_GAIN = 1600µA			-123		dBc/Hz
		PLL2_CP_GAIN = 3200µA			-128		
PN FOM	PLL 性能指数(5)	PLL2_CP_GAIN = 1600µA			-226.5		
		PLL2_CP_GAIN = 3200µA			-230		
I_{CPOUT}	チャージ・ポンプ電流の大きさ(6)	VCPout=VCC/2	PLL2_CP_GAIN=2		1600		µA
			PLL2_CP_GAIN=3		3200		
I_{CPout1}%MIS	チャージ・ポンプのシンク / ソースのミスマッチ	V_{CPout1} = VCC/2、T = 25℃	V_{CPout1} = VCC/2、T = 25℃		1	10	%

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6.5 電気的特性 (continued)

VDD、VDD_A = 3.3V±5%、-55℃≤TA≤125℃。標準値は、VDD = VDD_A = 3.3V、25℃ のときです (特に記述のない限り)。

記号	パラメータ	テスト条件		最小値	代表値	最大値	単位
$I_{CPout1}V_{TUNE}$	チャージ・ポンプ電流変動の大きさとチャージ・ポンプ電圧との関係	0.5V < V_{CPout1} < V_{CC} - 0.5V T_A = 25℃	0.5V < V_{CPout1} < V_{CC} - 0.5V T_A = 25℃		4	10	%
I_{CPout1}% 温度	チャージ・ポンプ電流と温度変動との関係				4	10	%
I_{CPOUT1}TRI	チャージ・ポンプの TRI_STATE リーク電流					10	nA
内蔵 VCO 仕様							
f_{VCO}	VCO 周波数範囲		VCO0	2440			MHz
			VCO1			3255	
K_{VCO}	VCO チューニング感度		VCO0		8～11		MHz/V
			VCO1		17～23		
$\|\Delta T_{CL}\|$	連続ロックで許容される温度ドリフト(7)		VCO0			150	℃
	連続ロックで許容される温度ドリフト(7)		VCO1			180	℃
L (f) VCO	開ループ VCO 位相ノイズ	VCO0 (2500MHz)	10kHz		-88.4		dBc/Hz
			100kHz		-117		
			800kHz		-137.5		
			1MHz		-139.7		
			10MHz		-152.6		
		VCO0 (2590 MHz)	10kHz		-85.7		
			100kHz		-115.8		
			800 kHz		-137		
			1MHz		-138.6		
			10MHz		-151.8		
L (f) VCO	開ループ VCO 位相ノイズ	VCO1 (2700MHz)	10kHz		-82.6		dBc/Hz
			100kHz		-112.3		
			800 kHz		-134.9		
			1MHz		-137.2		
			10MHz		-151.1		
		VCO1 (3200 MHz)	10kHz		-81		
			100kHz		-110.4		
			800 kHz		-134.3		
			1MHz		-135.6		
			10MHz		-149.3		
出力クロックのスキューとタイミング							
SKEWCLKinX	出力スキューへの出力	同じペアのデバイス・クロックと同じ形式			50		ps
		偶数から偶数、または奇数から奇数へ、同じ形式			50		
		偶数クロックから奇数クロックへ			50		
ディストリビューション・モードでの Fin ピンからの追加ジッタ (注 6)							
L (f) CLKout	分周なしの追加ジッタ、ディストリビューション・モード	245.76MHz の出力周波数、12k～20MHz の積分帯域幅	LVCMOS		50		fs
			LVDS		50		
			LVPECL		40		
			LCPECL		35		
			HSDS		40		
			CML		35		

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6.5 電気的特性 (continued)

VDD、VDD_A = 3.3V±5%、-55℃≤TA≤125℃。標準値は、VDD = VDD_A = 3.3V、25℃ のときです (特に記述のない限り)。

記号	パラメータ	テスト条件		最小値	代表値	最大値	単位
LVCMOS 出力							
$f)_{CLKout}$	周波数		5pF 負荷			250	MHz
$L(f)_{CLKout}$	ノイズ・フロア	245.76 MHz	20MHz オフセット		-160		dBc/Hz
V_{OH}	出力 HIGH 電圧	1mA 負荷		Vcc-0.1			V
V_{OL}	出力 LOW 電圧	1mA 負荷				0.1	V
I_{OH}	出力 HIGH 電流	FD=1.65V			-28		mA
I_{OL}	出力 LOW 電流	Vd=1.65V			28		mA
デューティ	出力デューティ・サイクル				50		%
LVDS クロック出力							
L (f) CLKout	ノイズ・フロア	245.76MHz 出力	20MHz オフセット		-159.5		dBc/Hz
T_R/T_F	立ち上がり / 立ち下がり時間:20%～80%				175		ps
V_{OD}	差動出力電圧	DC 測定、AC 結合からレシーバ入力 R_L = 100Ω 差動			400		mV
ΔV_{OD}	相補出力状態での V_{OD} の変更			-60		60	mV
V_{OS}	出力オフセット電圧			1.125	1.25	1.375	V
ΔV_{OS}	相補出力状態での VOS の変更					35	mV
$I_{SA}I_{SB}$	短絡回路出力電流			-24		24	mA
LCPECL クロック出力							
L (f) CLKout	ノイズフロア	245.76MHz 出力	20MHz オフセット		-162.5		dBc/Hz
T_R/T_F	立ち上がり / 立ち下がり時間:20%～80%				135		ps
V_{OH}	出力 HIGH 電圧	50Ω、0.5V での DC 測定			1.4		V
V_{OL}	出力 LOW 電圧				0.6		V
V_{OD}	差動出力電圧	50Ω、0.5V での DC 測定			870		mV
LVPECL クロック出力							
L (f) CLKout	ノイズフロア	245.76MHz 出力、LVPECL 2.0V	20MHz オフセット		-163		dBc/Hz
T_R/T_F	立ち上がり / 立ち下がり時間:20%～80%				135		ps
V_{OH}	出力 HIGH 電圧	DC 測定終端:50Ω、Vcc-2V	LVPECL 1.6V		Vcc-1		V
			LVPECL 2.0 V		Vcc-1		
V_{OL}	出力 LOW 電圧		LVPECL 1.6 V		Vcc-1.8		V
			LVPECL 2.0 V		Vcc-2		
V_{OD}	差動出力電圧	2.5GHz、Em = 120Ω から GND へ、R_L = AC 結合の 100Ω	LVPECL 1.6 V		0.8		V
			LVPECL 2.0 V		1		
HSDS クロック出力							
L (f) CLKout	ノイズフロア	245.76MHz 出力	20MHz オフセット		-162		dBc/Hz
T_R/T_F	立ち上がり / 立ち下がり時間:20%～80%				170		ps
V_{OH}	出力 HIGH 電圧	50Ω、0.5V での DC 測定	HSDS 6mA		Vcc-0.9		V
			HSDS 8 mA		Vcc-0.95		
V_{OL}	出力 LOW 電圧		HSDS 6 mA		Vcc-1.5		V
			HSDS 8 mA		Vcc-1.7		

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6.5 電気的特性 (continued)

VDD、VDD_A = 3.3V±5%、-55℃≤TA≤125℃。標準値は、VDD = VDD_A = 3.3V、25℃ のときです (特に記述のない限り)。

記号	パラメータ	テスト条件		最小値	代表値	最大値	単位
V_{OD}	出力電圧	50Ω、0.5V での DC 測定	HSDS 6mA		0.6		V
			HSDS 8 mA		0.75		
ΔV_{OD}	相補出力状態での VOS の変更		HSDS 6 mA	-80		80	mV
			HSDS 8 mA	-115		115	
CML 出力							
L (f) CLKout	ノイズフロア	20MHz オフセット			-163		dBc/Hz
T_R/T_F	立ち上がり / 立ち下がり時間:20%～80%	CML 16 mA			120		ps
		CML 24 mA			125		
		CML 32 mA			135		
V_{OH}	出力 HIGH 電圧	VCC、DC 測定まで 50Ω のプルアップ抵抗			Vcc		V
V_{OL}	出力 LOW 電圧	VCC、DC 測定まで 50Ω のプルアップ抵抗	CML 16 mA		Vcc-0.84		V
			CML 24 mA		Vcc-1.26		
			CML 32 mA		Vcc-1.66		
V_{OD}	出力電圧	VCC、DC 測定まで 50Ω のプルアップ抵抗	CML 16 mA		840		mV
			CML 24 mA		1260		
			CML 32 mA		1660		
		VCC、DC 測定まで 50Ω のプルアップ抵抗、R_L = AC 結合 100Ω、250MHz	CML 16 mA		550		mV
			CML 24 mA		815		
			CML 32 mA		1070		
デジタル出力 (CLKin_SELX、STATUS_LDX、および RESET/GPO、SDIO)							
V_{OH}	出力 HIGH 電圧			Vcc-0.4			V
V_{OL}	出力 LOW 電圧					0.4	V
デジタル入力							
V_{IH}	High レベル入力電圧			1.2			V
V_{IL}	Low レベル入力電圧					0.5	V
I_{IH}	High レベル入力電流	CLKinX_SEL、RESET/GPO、SYNC、SCK、SDIO、CS*		10		80	uA
		SYNC	$V_{IH} = V_{CC}$			25	
I_{IL}	Low レベル入力電流	CLKinX_SEL、RESET/GPO、SYNC、SCK、SDIO、CS*		-5		5	µA
I_{IL}	Low レベル入力電流	SYNC	V_{IL} = 0V	-5		5	

(1) TICS Pro ツールを使用して、特定の構成に対応する Icc を計算します
(2) デバイスは最低 0.15V/ns のスルーレートで動作しますが、最高の位相ノイズ性能を得るために、0.5V/ns 以上のスルーレートを推奨します。
(3) VID および VOD 電圧の定義については、「差動電圧測定の用語」を参照してください。
(4) PLL の帯域内位相ノイズのモデル化に関する仕様は、1/f フリッカー・ノイズである LPLL_flicker(f) です。このノイズは、キャリアの近くで支配的な役割をします。フリッカー・ノイズは 10dB/decade のスロープです。PN10kHz は、10kHz のオフセットと 1Ghz のキャリア周波数に正規化されています。PN10kHz = LPLL_flicker(10kHz) - 20log (Fout/1GHz)。ここで、LPLL_flicker(f) は、全ノイズ L (f) に影響を与えるフリッカー・ノイズのみの 1 次側帯域位相ノイズです。LPLL_flicker(f) を測定するには、キャリアに近い 10dB/decade スロープにすることが重要です。このノイズ源を位相ノイズの合計 L (f) から絶縁するには、高い比較周波数とクリーンな水晶振動子が重要です。低消費電力またはノイズの多いソースを使用する場合、リファレンス発振器の性能によって LPLL_flicker(f) をマスクできます。PLL の帯域内位相ノイズの合計性能は、LPLL_flicker(f) と LPLL_flat (f) の合計です。
(5) PLL の帯域内位相ノイズをモデル化する仕様。PLL の正規化された位相ノイズの寄与である LPLL_flat (f) は、次のように定義されます。PN1Hz = LPLL_flat (f) - 20log (N) - 10log (fPDX)。LPLL_flat (f) はオフセット周波数 f で 1 Hz の帯域幅で測定される 1 次側バンド位相ノイズであり、fPDX はシンセサイザの位相検出器周波数です。LPLL_flat (f) は、合計ノイズ L (f) に寄与します。
(6) このパラメータは、電気的仕様に示されているよりも多くの状態にプログラム可能です

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(7) 連続ロックの最大許容温度ドリフトとは、0x168 レジスタが PLL2_FCAL_DIS = 0 で最後にプログラムされた時点での値から、どちらの方向にも温度がドリフトできる範囲であり、引き続きロック状態を維持していることを意味します。0X168 レジスタを同じ値にプログラムする動作により、周波数キャリブレーション・ルーチンがアクティブになります。これは、部品が全周波数範囲で動作することを意味しますが、温度が連続ロックの最大許容ドリフトを超えてドリフトした場合、適切なレジスタをリロードしてロック状態を維持する必要があります。このパラメータは間接的にテストされます。

6.6 タイミング要件

VDD、VDD_A = 3.3V±5%、-55℃≤TA≤125℃。標準値は、VDD = VDD_A = 3.3V、25℃ のときです (特に記述のない限り)。

記号	パラメータ	最小値	公称値	最大値	単位
タイミング要件					
td_S	SDI エッジから SCK 立ち上がりエッジまでのセットアップ時間	40			ns
td_H	SDI エッジから SCK 立ち上がりエッジまでのホールド時間	20			ns
t_{SCK}	SCK の周期	400			ns
t_{HIGH}	SCK の高幅	120			ns
t_{LOW}	SCK の低幅	120			ns
t_{CS}	SCK 立ち上がりエッジまでの CS* 立ち下がりエッジのセットアップ時間	40			ns
t_{CH}	SCK 立ち上がりエッジからの CS* 立ち上がりエッジのホールド時間	40			ns
t_{CHW}	CS* の高幅時間	120			ns
t_{DV}	SCK 立ち下がりエッジから有効な読み戻しデータへ			120	ns

6.7 Timing Diagram

Register programming information on the SDIO pin is clocked into a shift register on each rising edge of the SCK signal. On the rising edge of the CS* signal, the register is sent from the shift register to the register addressed. A slew rate of at least 30 V/µs is recommended for these signals. After programming is complete the CS* signal should be returned to a high state. If the SCK or SDIO lines are toggled while the VCO is in lock, as is sometimes the case when these lines are shared with other parts, the phase noise may be degraded during this programming.

4-wire mode read back has same timing as SDIO pin.

R/W bit = 0 is for SPI write. R/W bit = 1 is for SPI read.

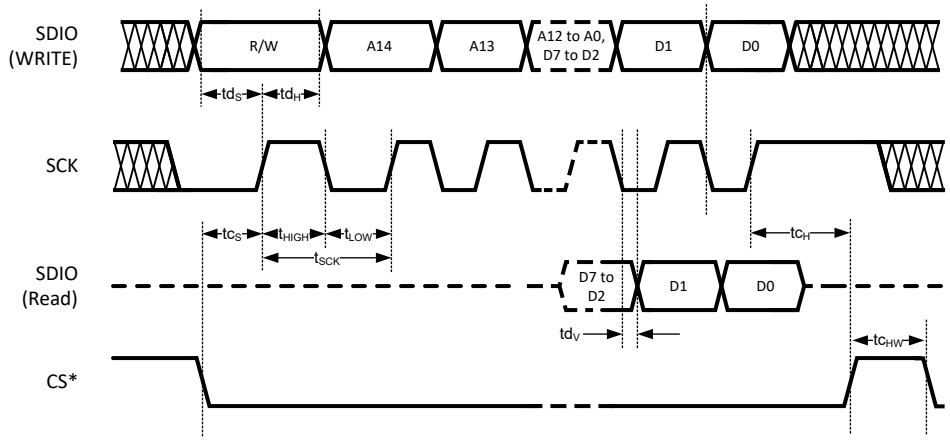
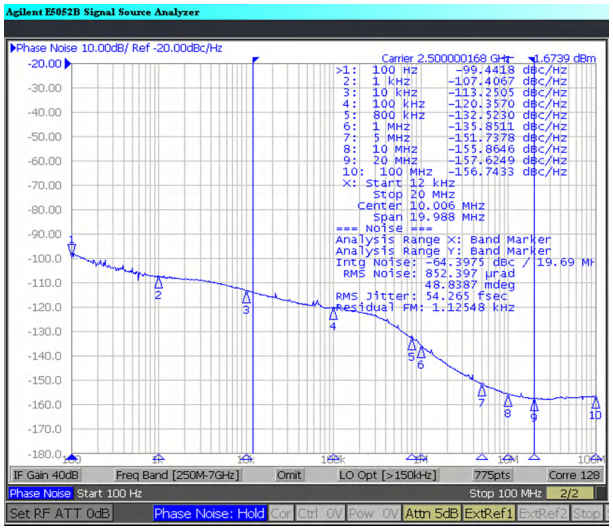


図 6-1. SPI Timing Diagram

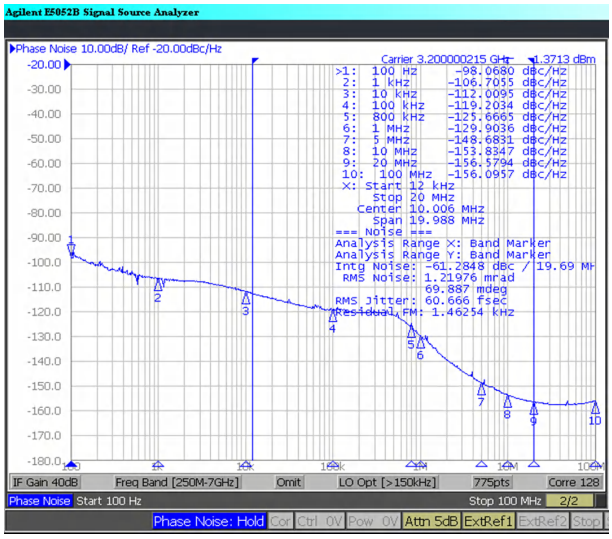
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6.8 代表的特性



100Hz～100MHz のジッタ = 63.6fs rms。
出力は、68nH～20Ω の DC バイアスで CML 32mA として CLKout4 です。
その他の設定は、CLKout4_5_IDL = 1 および CLKout4_5_BYP = 1 です。
PLL2 ループ・フィルタ R2 = 470Ω、C2 = 150nF、チャージ・ポンプ = 3200µA。
リファレンスは、Prodyn BIB-100G Balun から OSCin へのオプション SMAB-B711 を備えた R&S SMA100B 信号ジェネレータです。

図 6-2. 312.5MHz の OSCin / 位相検出器周波数で、2500MHz での VCO1 性能を発揮する PLL2



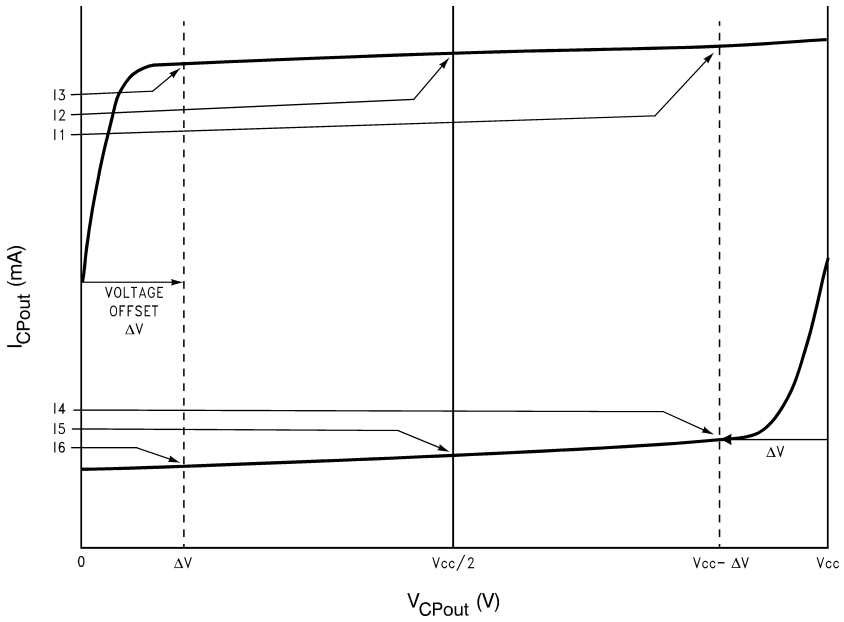
100Hz～100MHz のジッタ = 67fs rms。
出力は、68nH～20Ω の DC バイアスで CML 32mA として CLKout4 です。
その他の設定は、CLKout4_5_IDL = 1 および CLKout4_5_BYP = 1 です。
PLL2 ループ・フィルタ R2 = 470Ω、C2 = 150nF、チャージ・ポンプ = 3200µA。
リファレンスは、Prodyn BIB-100G Balun から OSCin へのオプション SMAB-B711 を備えた R&S SMA100B 信号ジェネレータです。

図 6-3. 3200MHz で VCO1 性能を発揮する PLL2、320MHz の OSCin / 位相検出器周波数

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7 Parameter Measurement Information

7.1 Charge Pump Current Specification Definitions



I1 = Charge Pump Sink Current at $V_{CPout} = V_{CC} - \Delta V$
I2 = Charge Pump Sink Current at $V_{CPout} = V_{CC}/2$
I3 = Charge Pump Sink Current at $V_{CPout} = \Delta V$
I4 = Charge Pump Source Current at $V_{CPout} = V_{CC} - \Delta V$
I5 = Charge Pump Source Current at $V_{CPout} = V_{CC}/2$
I6 = Charge Pump Source Current at $V_{CPout} = \Delta V$
ΔV = Voltage offset from the positive and negative supply rails. Defined to be 0.5 V for this device.

7.1.1 Charge Pump Output Current Magnitude Variation vs Charge Pump Output Voltage

$$I_{CPout}\ Vs\ V_{CPout} = \frac{|I1| - |I3|}{|I1| + |I3|} \times 100\%$$

$$= \frac{|I4| - |I6|}{|I4| + |I6|} \times 100\%$$

7.1.2 Charge Pump Sink Current vs Charge Pump Output Source Current Mismatch

$$I_{CPout}\ Sink\ Vs\ I_{CPout}\ Source = \frac{|I2| - |I5|}{|I2| + |I5|} \times 100\%$$

7.1.3 Charge Pump Output Current Magnitude Variation vs Ambient Temperature

$$I_{CPout}\ Vs\ T_A = \frac{|I_2|\Big|_{T_A} - |I_2|\Big|_{T_A = 25°C}}{|I_2|\Big|_{T_A = 25°C}} \times 100\%$$

$$= \frac{|I_5|\Big|_{T_A} - |I_5|\Big|_{T_A = 25°C}}{|I_5|\Big|_{T_A = 25°C}} \times 100\%$$

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7.2 Differential Voltage Measurement Terminology

The differential voltage of a differential signal can be described by two different definitions causing confusion when reading data sheets or communicating with other engineers. This section will address the measurement and description of a differential signal so that the reader will be able to understand and distinguish between the two different definitions when used.

The first definition used to describe a differential signal is the absolute value of the voltage potential between the inverting and noninverting signal. The symbol for this first measurement is typically V_{ID} or V_{OD} depending on if an input or output voltage is being described.

The second definition used to describe a differential signal is to measure the potential of the noninverting signal with respect to the inverting signal. The symbol for this second measurement is V_{SS} and is a calculated parameter. Nowhere in the IC does this signal exist with respect to ground, it only exists in reference to its differential pair. V_{SS} can be measured directly by oscilloscopes with floating references, otherwise this value can be calculated as twice the value of V_{OD} as described in the first description.

図 7-1 illustrates the two different definitions side-by-side for inputs and 図 7-2 illustrates the two different definitions side-by-side for outputs. The V_{ID} and V_{OD} definitions show V_A and V_B DC levels that the noninverting and inverting signals toggle between with respect to ground. V_{SS} input and output definitions show that if the inverting signal is considered the voltage potential reference, the noninverting signal voltage potential is now increasing and decreasing above and below the noninverting reference. Thus the peak-to-peak voltage of the differential signal can be measured.

V_{ID} and V_{OD} are often defined as volts (V) and V_{SS} is often defined as volts peak-to-peak (V_{PP}).

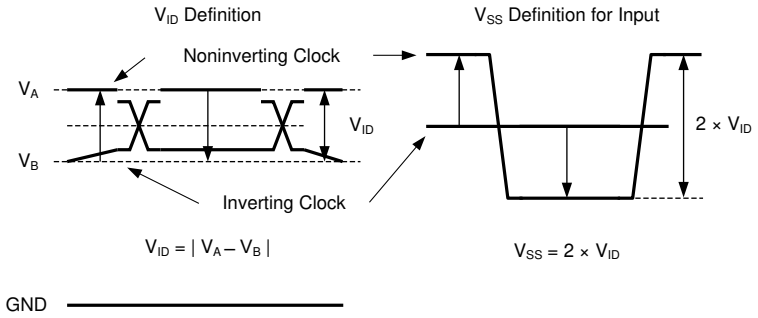


図 7-1. Two Different Definitions for Differential Input Signals

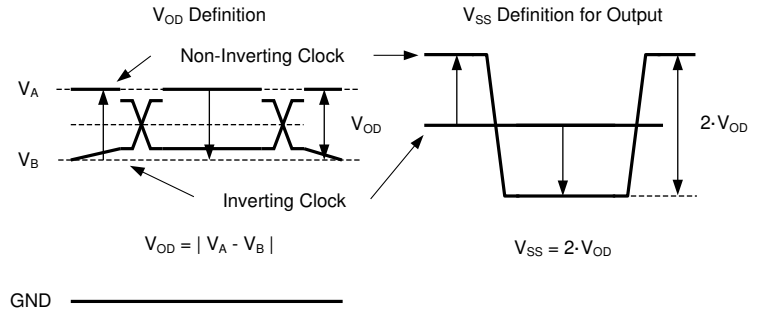


図 7-2. Two Different Definitions for Differential Output Signals

Refer to application note *AN-912 Common Data Transmission Parameters and their Definitions* (SNLA036) for more information.

8 Detailed Description

8.1 Overview

The LMK04832-SP device is very flexible to meet many application requirements. Use cases include dual loop, dual loop 0-delay nested, dual loop 0-delay cascaded, single loop, single loop 0-delay, and clock distribution.

The device may be used in JESD204B systems by providing a device clock and SYSREF to target devices, however traditional (non-JESD204B) systems are possible by programming pairs of outputs to share the clock divider or any mix of JESD204B and traditional.

8.1.1 Differences Between LMK04832-SP and LMK04832

The LMK04832-SP is very similar to the LMK04832 commercial device, but it does have a few differences.

表 8-1. LMK04832-SP vs. LMK04832

Attribute	LMK04832	LMK04832-SP
Radiation Hardened	No	Yes
Temperature	–40 ºC to +85 ºC	–55 ºC to +125 ºC
Package Size	9 × 9 mm^2	11 × 11 mm^2 (Disregarding Leads) 30 × 30 mm^2 (Including Leads)
Package Composition	Plastic	Ceramic
Pins 8/9	NC	Fin0/Fin0* Input
Pin 7	NC	GND
Programming Speed	5 MHz	2.5 MHz

8.1.1.1 Jitter Cleaning

The dual loop PLL architecture provides the lowest jitter performance over a wide range of output frequencies and phase noise integration bandwidths. The first stage PLL (PLL1) is driven by an external reference clock and uses an external VCXO to provide a frequency accurate, low phase noise reference clock for the second stage frequency multiplication PLL (PLL2).

PLL1 typically uses a narrow loop bandwidth (typically 10 Hz to 200 Hz) to retain the frequency accuracy of the reference clock input signal while at the same time suppressing the higher offset frequency phase noise that the reference clock may have accumulated along its path or from other circuits. This cleaned reference clock provides the reference input to PLL2.

The low phase noise reference provided to PLL2 allows PLL2 to operate with a wide loop bandwidth (typically 50 kHz to 200 kHz). The loop bandwidth for PLL2 is chosen to take advantage of the superior high offset frequency phase noise profile of the internal VCO and the good low offset frequency phase noise of the reference VCXO.

Ultra-low jitter is achieved by allowing the phase noise of the external VCXO to dominate the final output phase noise at low offset frequencies and the phase noise of the internal VCO to dominate the final output phase noise at high offset frequencies. This results in best overall phase noise and jitter performance.

8.1.1.2 JEDEC JESD204B Support

This device clocks up to 7 JESD204B targets using 7 device clocks and 7 SYSREF clocks and allows every clock output to be configured as a device clock or SYSREF clock.

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8.1.2 Clock Inputs

注

CLKin1 can be used as a reference for dual loop, single loop, or clock distribution mode, providing flexibility configuring the device for different operation modes from one clock input.

8.1.2.1 Inputs for PLL1

CLKin0, CLKin1, and CLKin2 are the three redundant inputs with their own PLL1 R dividers that can be used as a reference input to PLL1. The switching between these inputs can either be automatic or manual. For manual switching, CLKin_SEL0 and CLKin_SEL1 pins can be used for faster speed. These input pins are also shared for other functions.

- CLKin1 is shared for use as an external 0-delay feedback (FBCLKin), or for use with an external VCO (Fin).
- CLKin2 is shared for use as OSCout. To use CLKin2 as an input power down OSCout, see セクション 8.6.2.3.1.

8.1.2.2 Inputs for PLL2

In dual loop configurations, the PLL2 reference is from OSCin. However, in single PLL2 loop operation, it is also possible to use any of the three CLKins of PLL1 as a reference to PLL2.

8.1.2.3 Inputs When Using Clock Distribution Mode

For clock distribution mode, a reference signal is may be applied to the Fin0 or Fin1 pins. CLKin0 can be used to distribute a SYSREF signal through the device. In this use case, CLKin0 is re-clocked by CLKin1. The Fin0 pins are generally recommended over the Fin1 pins because they allow higher frequency, use a lower noise path, and cannot be used for other functions (like redundant input).

8.1.3 PLL1

PLL1 allows low offset jitter cleaning as well as the use of redundant inputs and frequency holdover.

8.1.3.1 Frequency Holdover

Frequency holdover keeps the clock outputs on frequency with minimum drift when the reference is lost until a valid reference clock signal is re-established. This can only be used if PLL1 is used.

8.1.3.2 External VCXO for PLL1

When PLL1 is used, an external VCXO is required. The close-in noise performance of this VCXO is critcal for good jitter cleaning performance. The LMK04832-SP also provides OSCout, which by power-on default is a buffered copy of the PLL1 feedback and PLL2 reference input at OSCin. This reference input is typically a low noise VCXO or XO. This output can be used to clock external devices such as microcontrollers, FPGAs, CPLDs, and so forth, before the LMK04832-SP is programmed.

- The OSCout buffer output type is programmable to LVDS, LVPECL, or LVCMOS.
- The VCXO buffered output can be synchronized to the VCO clock distribution outputs by using Cascaded 0-Delay Mode.

8.1.4 PLL2

8.1.4.1 Internal VCOs for PLL2

PLL2 has two internal VCOs. The output of the selected VCO is routed to the Clock Distribution Path. This same selection is also fed back to the PLL2 phase detector through a prescaler and N-divider.

8.1.4.2 External VCO Mode

An external VCO can be used with PLL2 with the input for the external VCO coming through Fin0 or Fin1, although Fin0 is generally preferred.

- Fin0/Fin0* input is generally recommended because it is lower noise, supports higher input frequency (up to 6 GHz if the div2 is used), and it leaves CLKin1 available for redundant inputs.

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Fin1/Fin1* inputs are generally NOT recommended, for the reasons stated above, although they can be used.

8.1.5 Clock Distribution

The LMK04832-SP features a total of 14 PLL2 clock outputs driven from the internal or external VCO.

All clock outputs have programmable output types. They can be programmed to CML, LVPECL, LVDS, HSDS, or LCPECL. All odd clock outputs plus CLKout8 and CLKout10 may be programmed to LVCMOS.

If OSCout is included in the total number of clock outputs the LMK04832-SP is able to distribute up to 15 differential clocks. OSCout may be a buffered version of OSCin, DCLKout6, DCLKout8, or SYSREF. Its output format is programmable to LVDS, LVPECL, or LVCMOS.

The following sections discuss specific features of the clock distribution channels that allow the user to control various aspects of the output clocks.

8.1.5.1 Clock Divider

There are 7 clock dividers. In a traditional clocking system each divider can drive two outputs. The divider range is 1 to 1023. Duty cycle correction may be enabled for the output. When the divider is used even clocks may not output CML.

In a JESD204B system, one clock output is a device clock driven from the clock divider and the other paired clock is from the SYSREF divider. For connectivity flexibility, either the even or odd clock output may be driven by the clock divider or be the SYSREF output.

8.1.5.2 High Performance Divider Bypass Mode

Even clock outputs (CLKoutX) of the LMK04832-SP may bypass the clock divider to achieve the best possible noise floor and output swing. In this mode, the only usable output format is CML.

8.1.5.3 SYSREF Clock Divider

The SYSREF divider supports a divide range of 8 to 8191 (even and odd). There is no duty cycle correction for the SYSREF divider. The SYSREF output may be routed to all clock outputs.

8.1.5.4 Device Clock Delay

The device clocks support digital delay for phase adjustment of the clock outputs.

The digital delay allows outputs to be delayed from 8 to 1023 VCO cycles. The delay step can be as small as half the period of the clock distribution path. For example, a 3.2-GHz VCO frequency results in 156.25-ps steps.

The digital delay value takes effect on the clock output phase after a SYNC event.

8.1.5.5 Dynamic Digital Delay

The device clock dividers support a dynamic digital delay feature which allows the clock to be delayed by one full device clock cycle. With a single programming, an adjustment of up to 255 one cycle delays may occur. When making a multi-step adjustment, the adjustments are periodically applied to reduce impact to the clock.

Dynamic phase adjustments of half a clock distribution cycle are possible by half step.

The SYSREF digital delay value is reused for dynamic digital delay. To achieve a one cycle delay program the SYSREF digital delay value to one greater than half the SYSREF divide value.

8.1.5.6 SYSREF Delay: Global and Local

The SYSREF divider includes a digital delay block which allows a global phase shift with respect to the device clocks.

Each clock output pair includes a local SYSREF analog and digital delay for unique phase adjustment of each SYSREF clock.

The local analog delay allows for approximately 21-ps steps. Turning-on analog delay adds an additional 124 ps of delay in the clock path. The digital delay step can be as small as half the period of the clock distribution path. For example, a 3.2-GHz VCO frequency results in 156.25-ps steps.

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The local digital delay and half step allows a SYSREF output to be delayed from 1.5 to 11 clock distribution path cycles.

8.1.5.7 Programmable Output Formats

All clock outputs can be programmed to an LVDS, HSDS, LVPECL, or LCPECL output type. Odd clock outputs in addition to CLKout8 and CLKout10 may also be programmed to LVCMOS. All odd clock outputs can also be programmed to CML. When in bypass mode the even clock output may only be CML.

The OSCout can be programmed to an LVDS, LVPECL, or LVCMOS output type.

Any HSDS output type can be programmed to 6-mA or 8-mA amplitude levels.

Any LVPECL output type can be programmed to 1600-mVpp or 2000-mVpp amplitude levels. The 2000-mVpp LVPECL output type is a Texas Instruments proprietary configuration that produces a 2000-mVpp differential swing for compatibility with many data converters and is also known as 2VPECL.

LCPECL allows for DC-coupling SYSREF to low voltage JESD204B targets.

8.1.5.8 Clock Output Synchronization

Using the SYNC input causes all active clock outputs to share a rising edge as programmed by fixed digital delay.

The SYNC event must occur for digital delay values to take effect.

8.1.6 0-Delay

Two types of 0-delay mode are supported.

1. Cascaded 0-delay
2. Nested 0-delay

Cascaded 0-delay mode establishes a fixed deterministic phase relationship of the phase of the PLL2 input clock (OSCin) to the phase of a clock selected by the feedback mux. The 0-delay feedback uses internal feedback from the CLKout6, CLKout8, or SYSREF. The 0-delay feedback can also be from an external feedback through the FBCLKin port. The FB_MUX selects the feedback source. Because OSCin has a fixed deterministic phase relationship to the feedback clock, OSCout will also have a fixed deterministic phase relationship to the feedback clock. In this mode, PLL1 input clock (CLKinX) also has a fixed deterministic phase relationship to PLL2 input clock (OSCin); this results in a fixed deterministic phase relationship between all clocks from CLKinX to the clock outputs.

Nested 0-delay mode establishes a fixed deterministic phase relationship of the phase of the PLL1 input clock (CLKinX) to the phase of a clock selected by the feedback mux. The 0-delay feedback uses internal feedback from the CLKout6, CLKout8, or SYSREF. The 0-delay feedback can also be from an external feedback through the FBCLKin port. The FB_MUX selects the feedback source.

Without using 0-delay mode, there will be n possible fixed phase relationships from clock input to clock output depending on the clock output divide value.

Using an external 0-delay feedback reduces the number of available clock inputs by one.

8.1.7 Status Pins

The status pins can be monitored for feedback or in some cases used for input depending upon device programming. For example:

- The CLKin_SEL0 pin may indicate the LOS (loss-of-signal) for CLKin0.
- The CLKin_SEL1 pin may be an input for selecting the active clock input.
- The Status_LD1 pin may indicate if the device is locked.
- The Status_LD2 pin may indicate if PLL2 is locked.

The status pins can be programmed to a variety of other outputs including PLL divider outputs, combined PLL lock detect signals, PLL1 Vtune railing, readback, and so forth. Refer to セクション 8.6 for more information.

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8.2 Functional Block Diagram

図 8-1 illustrates the high level LMK04832-SP block diagram.

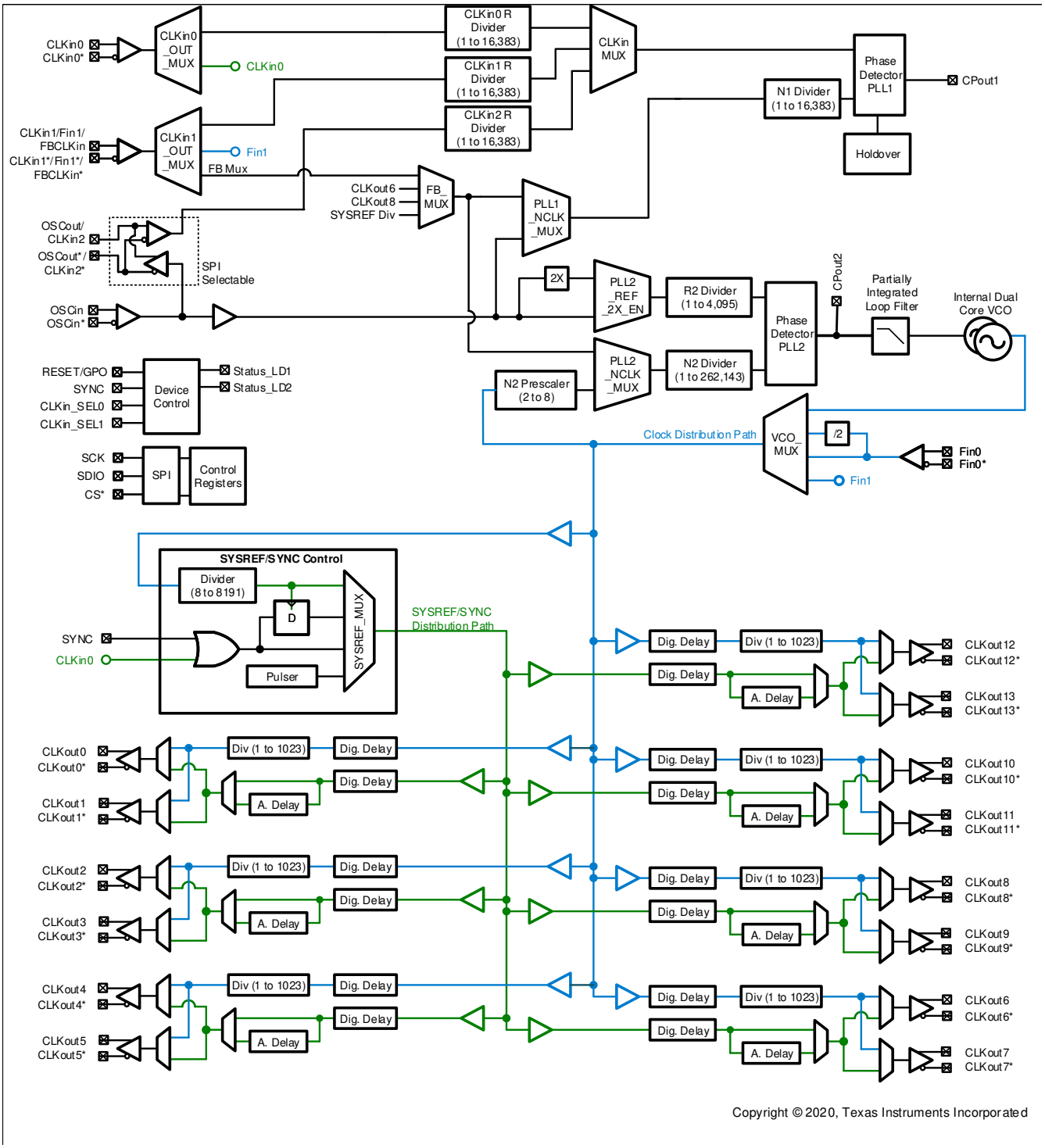
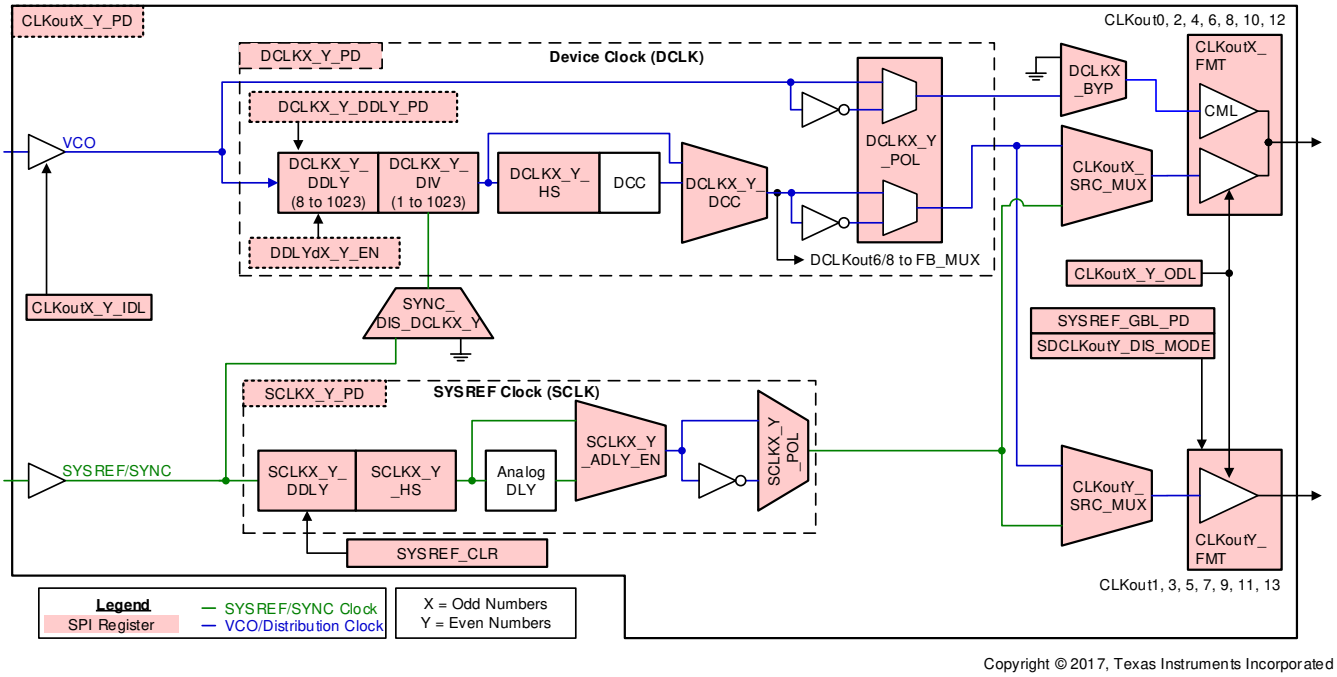


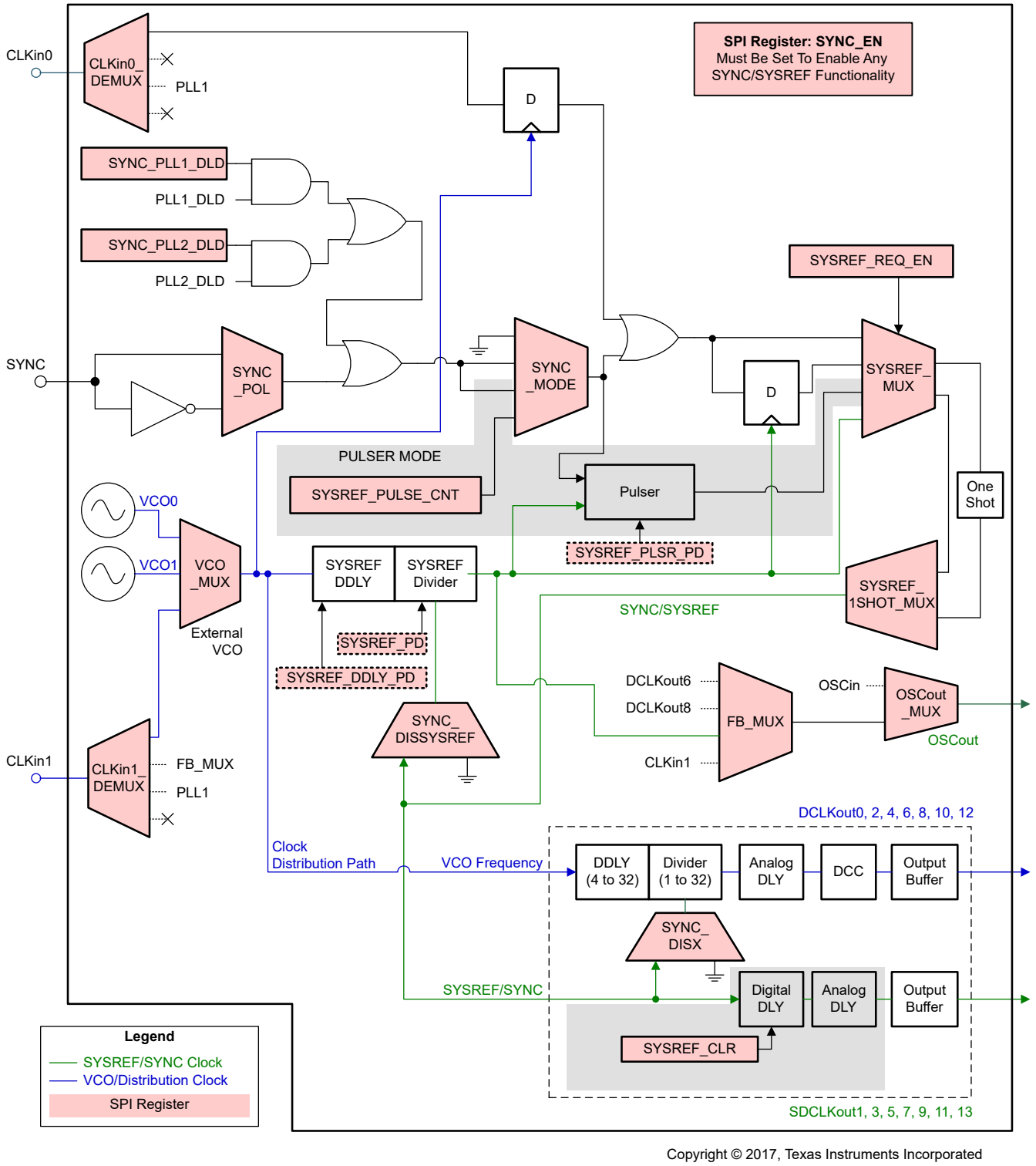
図 8-1. High Level LMK04832-SP Block Diagram

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図 8-2. Device and SYSREF Clock Output Block



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図 8-3. SYNC/SYSREF Clocking Paths

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8.3 Feature Description

8.3.1 Synchronizing PLL R Dividers

In some cases, it is necessary to synchronize PLL R dividers to enable determinism of clocks outputs to inputs. This typically is required when the fraction Total PLL N divide / Total PLL R divide does not reduce to N / 1.

8.3.1.1 PLL1 R Divider Synchronization

It is possible to use the CLKin0 or SYNC pin to synchronize the PLL1 R divider. In either case, the PLL1 R divider is armed for reset, then the rising sync edge arrives from either SYNC pin or CLKin0. After the PLL1 R divider is armed, PLL1 is unlocked until the synchronization edge arrives and allows the divider to operate and the PLL to lock. The procedure to synchronize PLL1 R is as follows:

1. Setup device for synchronizing PLL1 R:
   - PLL1R_SYNC_EN = 0x1
   - PLL1R_SYNC_SRC = 0x1 (SYNC pin) or 0x2 (CLKin0)
   - CLKin0_DEMUX = 0x2 (PLL1)
   - CLKin1_DEMUX = 0x2 (PLL1)
   - CLKin0_TYPE = 0x1 (MOS) for DC-coupled or CLKin0_TYPE = 0x0 (Bipolar) for AC-coupled
2. Arm PLL1 R divider for synchronization
   - PLL1R_RST = 1, then 0.
   - PLL1 is unlocked.
3. Send rising edge on SYNC pin or CLKin0.
   - PLL1 R divider is released from reset and PLL1 relocks.

It is necessary to meet a setup and hold time when CLKin0 or SYNC pin goes high to ensure deterministic reset of the PLL1 R divider.

The SYNC_POL bit has no effect on SYNC polarity for PLL1 R synchronization.

8.3.1.2 PLL2 R Divider Synchronization

The SYNC pin must be used to synchronized the PLL2 R divider. When PLL2R_SYNC_EN = 1, as long as the SYNC pin is held high, the PLL2 R divider is held in reset. When the SYNC pin is returned low, the divider is allowed to continue dividing. While PLL2R_SYNC_EN = 1 and SYNC pin is high PLL2 is unlocked.

It is necessary to meet a setup and hold time when SYNC pin goes low to ensure deterministic reset of the PLL2 R divider.

The SYNC_POL bit has no effect on SYNC polarity for PLL2 R synchronization.

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8.3.2 SYNC/SYSREF

The SYNC and SYSREF signals share the same SYNC/SYSREF Clock Distribution path. To properly use SYNC and/or SYSREF for JESD204B it is important to understand the SYNC/SYSREF system. 図 8-2 illustrates the detailed diagram of a clock output block with SYNC circuitry included. 図 8-3 illustrates the interconnects and highlights some important registers used in controlling the device for SYNC/SYSREF purposes.

To reset or synchronize a divider, the following conditions must be met:

1. SYNC_EN must be set. This ensures proper operation of the SYNC circuitry.
2. SYSREF_MUX and SYNC_MODE must be set to a proper combination to provide a valid SYNC/SYSREF signal.
   - If SYSREF block is being used, the SYSREF_PD bit must be clear.
   - If the SYSREF Pulser is being used, the SYSREF_PLSR_PD bit must be clear.
   - For each CLKoutX or CLKoutY being used for SYSREF, the respective SCLKX_Y_PD bit must be cleared.
3. DCLKX_Y_DDLY_PD and SYSREF_DDLY_PD bits must be clear to power up the digital delay circuitry used during SYNC to cause deterministic phase between the device clock dividers and the global SYSREF divider.
4. The SYNC_DISX bit must be clear to allow SYNC/SYSREF signal to divider circuit. The SYSREF_MUX register selects the SYNC source which resets the SYSREF/CLKoutX dividers provided the corresponding SYNC_DISX bit is clear.
5. Other bits which impact the operation of SYNC such as SYNC_1SHOT_EN may be set as desired.
6. After these dividers are synchronized, the DCLKX_Y_DDLY_PD and SYSREF_DDLY_PD bits may be set to save current. Clearing them to power up may disrupt the output clock phase.

表 8-2 illustrates the some possible combinations of SYSREF_MUX and SYNC_MODE.

表 8-2. Some Possible SYNC Configurations

NAME	SYNC_MODE	SYSREF_MUX	OTHER	DESCRIPTION
SYNC Disabled	0	0	CLKin0_DEMUX ≠ 0	No SYNC will occur.
Pin or SPI SYNC	1	0	CLKin0_DEMUX ≠ 0	Basic SYNC functionality, SYNC pin polarity is selected by SYNC_POL. To achieve SYNC through SPI, toggle the SYNC_POL bit.
Differential input SYNC	X	0 or 1	CLKin0_DEMUX = 0	Differential CLKin0 now operates as SYNC input.
JESD204B Pulser on pin transition.	2	2	SYSREF_PULSE_CNT sets pulse count	Produce SYSREF_PULSE_CNT programmed number of pulses on pin transition. SYNC_POL can be used to cause SYNC through SPI.
JESD204B Pulser on SPI programming.	3	2	SYSREF_PULSE_CNT sets pulse count	Programming SYSREF_PULSE_CNT register starts sending the number of pulses.
Re-clocked SYNC	1	1	SYSREF operational, SYSREF Divider as required for training frame size.	Allows precise SYNC for n-bit frame training patterns for non-JESD converters such as LM97600.
External SYSREF request	0	2	SYSREF_REQ_EN = 1 Pulser powered up	When SYNC pin is asserted, continuous SYSERF pulses occur. Turning on and off of the pulses is synchronized to prevent runt pulses from occurring on SYSREF.
Continuous SYSREF	X	3	SYSREF_PD = 0 SYSREF_DDLY_PD = 0 SYSREF_PLSR_PD = 1 (1)	Continuous SYSREF signal.

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表 8-2. Some Possible SYNC Configurations (continued)

NAME	SYNC_MODE	SYSREF_MUX	OTHER	DESCRIPTION
Re-clocked SYSREF distribution	0	0	SYSREF_DDLY_PD = 1 SYSREF_PLSR_PD = 1 SYSREF_PD = 1.	Fan-out of CLKin0 reclocked to the clock distribution path.

(1) SCLKX_Y_PD = 0 as required per SYSREF output. This applies to any SYNC or SYSREF output on SCLKX_Y when SCLKX_Y_MUX = 1 (SYSREF output)

注

Because the SYNC/SYSREF signal is reclocked by the Clock Distribution Path, an active clock must be present on the Clock Distribution Path (either from VCO or Fin0/Fin1 pins in distribution mode) for SYNC to take effect.

注

Any device clock divider or the SYSREF divider which does not have the SYNC_DISX bit or SYNC_DISSYSREF bit set will reset while SYNC/SYSREF Distribution Path is high. This is especially important for the SYSREF divider which has the ability to reset itself if the SYNC_DISSYSREF = 0! **Be sure to set SYNC_DISX/SYNC_DISSYSREF bits as required.**

注

While using Divide-by-2 or Divide-by-3 for DCLK_X_Y_DIV, SYNC procedure requires to first program Divide-by-4 and then back to Divide-by-2 or Divide-by-3 before doing SYNC.

8.3.3 JEDEC JESD204B

8.3.3.1 How to Enable SYSREF

表 8-3 summarizes the bits needed to make SYSREF functionality operational.

表 8-3. SYSREF Bits

REGISTER	FIELD	VALUE	DESCRIPTION
0x140	SYSREF_PD	0	Must be clear, power-up SYSREF circuitry including the SYSREF divider.
0x140	SYSREF_DDLY_PD	0	Must be clear to power-up digital delay circuitry. Must be powered up during initial SYNC to ensure deterministic timing to other clock dividers.
0x143	SYNC_EN	1	Must be set, enable SYNC.
0x143	SYSREF_CLR	1 → 0	Do not hold local SYSREF DDLY block in reset except at start. Anytime SYSREF_PD = 1 because of user programming or device RESET, it is necessary to set SYSREF_CLR for 15 VCO clock cycles to clear the local SYSREF digital delay. Once cleared, SYSREF_CLR must be cleared to allow SYSREF to operate.

Enabling JESD204B operation involves synchronizing all the clock dividers with the SYSREF divider, then configuring the actual SYSREF functionality.

8.3.3.1.1 Setup of SYSREF Example

The following procedure is a programming example for a system which is to operate with a 3000-MHz VCO frequency. Use CLKout0 and CLKout2 to drive converters at 1500 MHz. Use CLKout4 to drive an FPGA at 150 MHz. Synchronize the converters and FPGA using a two SYSREF pulses at 10 MHz.

1. **Program registers 0x000 to 0x555 (refer to セクション 8.5.1). Key to prepare for SYSREF operations:**
   a. Prepare for manual SYNC: SYNC_POL = 0, SYNC_MODE = 1, SYSREF_MUX = 0
   b. Setup output dividers as per example: DCLK0_1_DIV and DCLK2_3_DIV = 2 for frequency of 1500 MHz. DCLK4_5_DIV = 20 for frequency of 150 MHz.
   c. Setup output dividers as per example: SYSREF_DIV = 300 for 10-MHz SYSREF.

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d. Setup SYSREF: SYSREF_PD = 0, SYSREF_DDLY_PD = 0, DCLK0_1_DDLY_PD = 0, DCLK2_3_DDLY_PD = 0, DCLK4_5_DDLY_PD = 0, SYNC_EN = 1, SYSREF_PLSR_PD = 0, SYSREF_PULSE_CNT = 1 (2 pulses). SCLK0_1_PD = 0, SCLK2_3_PD = 0, SCLK4_5_PD = 0.
e. Clear Local SYSREF DDLY: SYSREF_CLR = 1.

2. **Establish deterministic phase relationships between SYSREF and Device Clock for JESD204B:**
   a. Set device clock and SYSREF divider digital delays: DCLK0_1_DDLY, DCLK2_3_DDLY, DCLK4_5_DDLY, and SYSREF_DDLY.
   b. Set device clock digital delay half steps: DCLK0_1_HS, DCLK2_3_HS, DCLK4_5_HS.
   c. Set SYSREF clock digital delay as required to achieve known phase relationships: SCLK0_1_DDLY, SCLK2_3_DDLY, and SCLK4_5_DDLY. If half step adjustments are required SCLK0_1_HS, SCLK2_3_HS, and SCLK4_5_HS.
   d. To allow SYNC to affect dividers: SYNC_DIS0 = 0, SYNC_DIS2 = 0, SYNC_DIS4 = 0, SYNC_DISSYSREF = 0.
   e. **Perform SYNC by toggling SYNC_POL = 1 then SYNC_POL = 0.**
3. Now that dividers are synchronized, **disable SYNC from resetting these dividers.** It is not desired for SYSREF to reset it's own divider or the dividers of the output clocks.
   a. Prevent SYNC (SYSREF) from affecting dividers: SYNC_DIS0 = 1, SYNC_DIS2 = 1, SYNC_DIS4 = 1, SYNC_DISSYSREF = 1.
4. **Release reset of local SYSREF digital delay.**
   a. SYSREF_CLR = 0. Note this bit needs to be set for only 15 clock distribution path clocks after SYSREF_PD = 0.
5. **Set SYSREF operation**.
   a. Allow pin SYNC event to start pulser: SYNC_MODE = 2.
   b. Select pulser as SYSREF signal: SYSREF_MUX = 2.
6. **Complete!** Now asserting the SYNC pin, or toggling SYNC_POL will result in a series of 2 SYSREF pulses.

8.3.3.1.2 SYSREF_CLR

The local digital delay of the SCLKX_Y_DDLY is implemented as a shift buffer. To ensure no unwanted pulses occur at this SYSREF output at start-up, when using SYSREF, requires clearing the buffers by setting SYSREF_CLR = 1 for 15 VCO clock cycles. After a reset, this bit is set, so it must be cleared before SYSREF output is used.

If the SYSREF pulser is used. It is also required to set SYSREF_CLR = 1 for 15 VCO clock cycles after the SYSREF pulser is powered up.

8.3.3.2 SYSREF Modes

8.3.3.2.1 SYSREF Pulser

This mode allows for the output of 1, 2, 4, or 8 SYSREF pulses for every SYNC pin event or SPI programming. This implements the gapped periodic functionality of the JEDEC JESD204B specification.

When in SYSREF Pulser mode, programming the field SYSREF_PULSE_CNT in register 0x13E will result in the pulser sending the programmed number of pulses.

8.3.3.2.2 Continuous SYSREF

This mode allows for continuous output of the SYSREF clock.

注

Continuous operation of SYSREF is not recommended due to crosstalk from the SYSREF clock to device clock. JESD204B is designed to operate with a single burst of pulses to initialize the system at start-up, after which it is theoretically not required to send another SYSREF because the system will continue to operate with deterministic phases.

8.3.3.2.3 SYSREF Request

This mode allows an external source to synchronously turn on or off a continuous stream of SYSREF pulses using the SYNC/SYSREF_REQ pin.

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Setup the mode by programming SYSREF_REQ_EN = 1 and SYSREF_MUX = 2 (Pulser). The pulser does not need to be powered for this mode of operation.

When the SYSREF_REQ pin is asserted, the SYSREF_MUX will synchronously be set to continuous mode providing continuous pulses at the SYSREF frequency until the SYSREF_REQ pin is unasserted and the final SYSREF pulse will complete sending synchronously.

8.3.4 Digital Delay

Digital (coarse) delay allows a group of outputs to be delayed by 8 to 1023 clock distribution path cycles. The delay step can be as small as half the period of the clock distribution path cycle by using the DCLKX_Y_HS bit. There are two different ways to use the digital delay:

1. Fixed digital delay
2. Dynamic digital delay

In both delay modes, the regular clock divider is substituted with an alternative divide value.

8.3.4.1 Fixed Digital Delay

Fixed digital delay value takes effect on the clock outputs after a SYNC event. As such, the outputs will be LOW for a while during the SYNC event. Applications that cannot accept clock breakup when adjusting digital delay during application run time should use dynamic digital delay to adjust phase.

8.3.4.1.1 Fixed Digital Delay Example

Assuming the device already has the following initial configurations, and the application should delay CLKout2 by one VCO cycle compared to CLKout0.

- VCO frequency = 2949.12 MHz
- CLKout0 = 368.64 MHz (DCLK0_1_DIV = 8, CLKout0_SRC_MUX = 0 (Device Clock))
- CLKout2 = 368.64 MHz (DCLK2_3_DIV = 8, CLKout2_SRC_MUX = 0 (Device Clock))

The following steps should be followed

1. Set DCLK0_1_DDLY = 8 and DCLK2_3_DDLY = 9. Static delay for each clock.
2. Set DCLK0_1_DDLY_PD = 0 and DCLK2_3_DDLY_PD = 0. Power up the digital delay circuit.
3. Set SYNC_DIS0 = 0 and SYNC_DIS2 = 0. Allow the outputs to be synchronized.
4. Perform SYNC by asserting, then unasserting SYNC. Either by using SYNC_POL bit or the SYNC pin.
5. Now that the SYNC is complete, to save power it is allowable to power down DCLK0_1_DDLY_PD = 1 and/or DCLK2_3_DDLY_PD = 1.
6. Set SYNC_DIS0 = 1 and SYNC_DIS2 = 1. Prevent the output from being synchronized, very important for steady-state operation when using JESD204B.

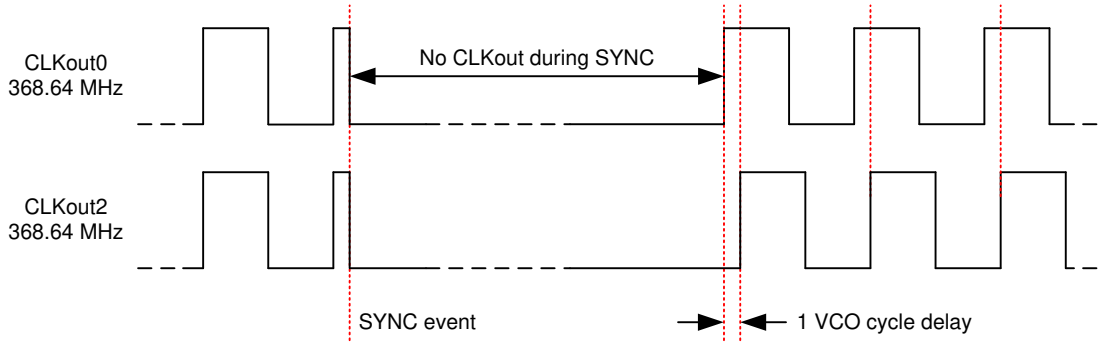


図 8-4. Fixed Digital Delay Example

8.3.4.2 Dynamic Digital Delay

Dynamic digital delay allows the phase of clocks to be changed with respect to each other with little impact to the clock signal.

For the device clock dividers this is accomplished by substituting the regular clock divider with an alternate divide value of one larger than the regular divider for one cycle. This substitution will occur a number of times equal to the value programmed into the DDLYd_STEP_CNT field for all outputs with DDLYdX_EN = 1.

For the SYSREF divider an alternate divide value will be substituted for the regular divide value. This substitution will occur a number of times equal to the value programmed into the DDLYd_STEP_CNT if DDLYd_SYSREF_EN = 1. To achieve one cycle delay as is done for the device clock dividers, set the SYSREF_DDLY value to one greater than SYSREF_DIV+SYSREF_DIV/2. For example, for a SYSREF divider of 100, to achieve 1 cycle delay, SYSREF_DIV = 100 + 50 + 1 = 151.

While using the Dynamic Digital Delay feature, CLKin_OVERRIDE must be set to 0.

- By programming a larger alternate divider (delay) value, the phase of the adjusted outputs are delayed with respect to the other clocks.
- By programming a smaller alternate divider (delay) value, the phase of the adjusted outputs are advanced with respect to the other clocks.

8.3.4.3 Single and Multiple Dynamic Digital Delay Example

In this example, two separate adjustments are made to the device clocks. In the first adjustment, a single delay of 1 VCO cycle occurs between CLKout2 and CLKout0. In the second adjustment, two delays of 1 VCO cycle occur between CLKout2 and CLKout0. At this point in the example, CLKout2 is delayed 3 VCO cycles behind CLKout0.

Assuming the device already has the following initial configurations:

- VCO frequency: 2949.12 MHz
- CLKout0 = 368.64 MHz, DCLK0_1_DIV = 8
- CLKout2 = 368.64 MHz, DCLK2_3_DIV = 8

The following steps illustrate the example above:

1. Set DCLK2_3_DDLY = 4. First part of delay for CLKout2.
2. Set DCLK2_3_DDLY_PD = 0. Enable the digital delay for CLKout2.
3. Set DDLYd0_EN = 0 and DDLYd2_EN = 1. Enable dynamic digital delay for CLKout2 but not CLKout0.
4. Set DDLYd_STEP_CNT = 1. This begins the **first adjustment.**

Before step 4, CLKout2 clock edge is aligned with CLKout0.

After step 4, CLKout2 counts nine clock distribution path cycles to the next rising edge, one greater than the divider value, effectively delaying CLKout2 by one VCO cycle with respect to CLKout0. ***This is the first adjustment.***

5. Set DDLYd_STEP_CNT = 2. This begins the **second adjustment.**

Before step 5, CLKout2 clock edge was delayed 1 clock distribution path cycle from DCLKout0.

After step 5, CLKout2 counts nine clock distribution path cycles twice, each time one greater than the divide value, effectively delaying CLKout2 by two clock distribution path cycles with respect to CLKout0. ***This is the second adjustment.***

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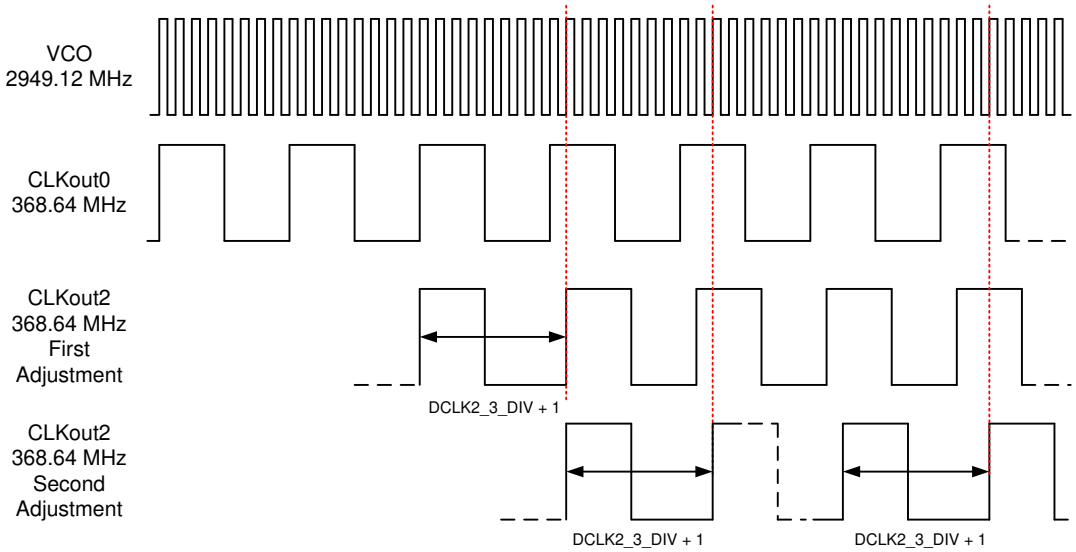


図 8-5. Single and Multiple Adjustment Dynamic Digital Delay Example

8.3.5 SYSREF to Device Clock Alignment

To ensure proper JESD204B operation, the timing relationship between the SYSREF and the Device clock must be adjusted for optimum setup and hold time as shown in 図 8-6. The global SYSREF digital delay (SYSREF_DDLY), local SYSREF digital delay (SCLKX_Y_DDLY), local SYSREF half step (SCLKX_Y_HS), and local SYSREF analog delay (SCLKX_Y_ADLY, SCLK2_3_ADLY_EN) can be adjusted to provide the required setup and hold time between SYSREF and Device Clock. It is also possible to adjust the device clock digital delay (DCLKX_Y_DDLY) and half step (DCLK0_1_HS, DCLK0_1_DCC) to adjust phase with respect to SYSREF.

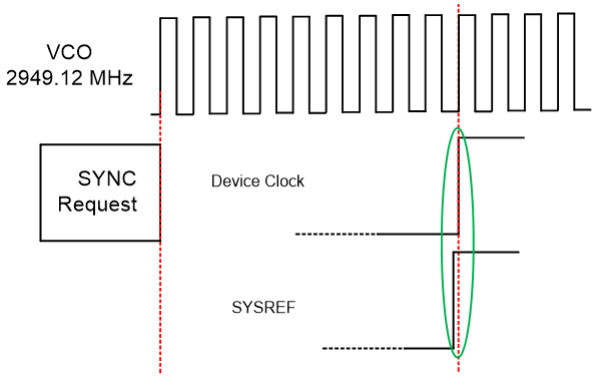


図 8-6. SYSREF to Device Clock Timing alignment

Depending on the DCLKout_X path settings, local SCLK_X_Y_DDLY might need adjustment factor. Following equation can be used to calculate the required Digital Delay Values to align SYSREF to the corresponding DCLKout:

$$SYSREF_DDLY = DCLKX_Y_DDLY - 1 + DCLK_DIV_ADJUST + DCLK_HS_ADJUST - SCLK_X_Y_DDLY \quad (1)$$

SYSREF_DDLY > 7; SCLK_X_Y_DDLY > 1.

表 8-4. DCLK_DIV_ADJUST

DCLKX_Y_DIV	DCLK_DIV_ADJUST
>6	0
6	–1

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表 8-4. DCLK_DIV_ADJUST (continued)

DCLKX_Y_DIV	DCLK_DIV_ADJUST
5	2
4	0
3 (1)	–2
2 (1)	–2

(1) Refer to the SYNC requirement セクション 8.3.2

表 8-5. DCLK_HS_ADJUST

DCLK & HS	DCLK_HS_ADJUST
0	0
1	1

For example: DCLKX_Y_DIV = 32, DCLKX_Y_DDLY = 10, DCC&HS = 1;

SYSREF_DDLY=10 – 1 + 0 + 1 – 2 = 8

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8.3.6 Input Clock Switching

Manual, pin select, and automatic are three different kinds clock input switching modes can be selected according to the combination of bits as illustrated in 図 8-7.

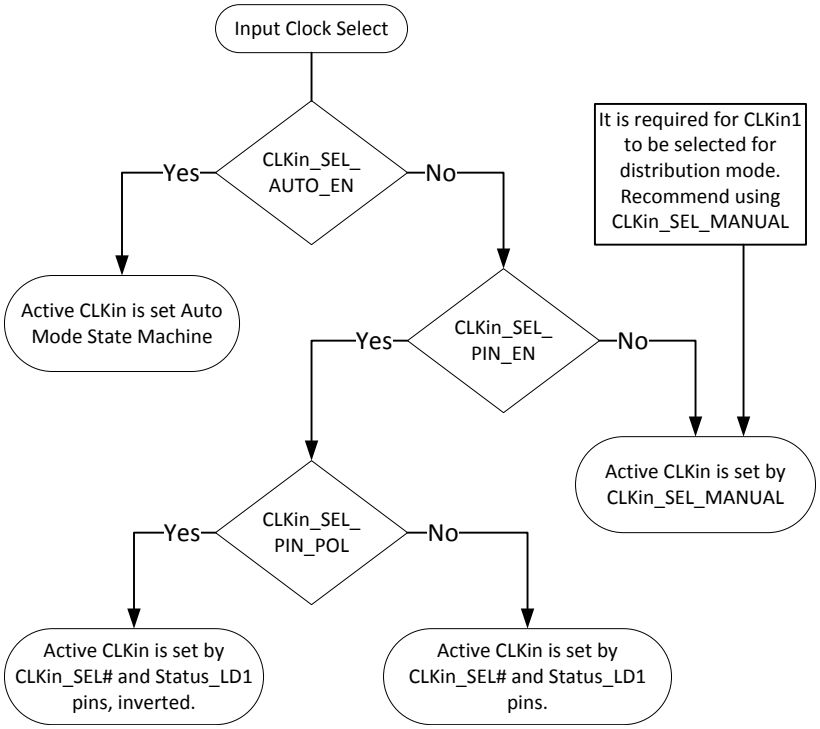


図 8-7. CLKinX Input Reference

The following sections provide information about how the active input clock is selected and what causes a switching event in the various clock input selection modes.

8.3.6.1 Input Clock Switching - Manual Mode

When CLKin_SEL_AUTO_EN = 0 and CLKin_SEL_PIN_EN = 0, the active CLKin is selected by CLKin_SEL_MANUAL. Programming a value of 0, 1, or 2 to CLKin_SEL_MANUAL causes CLKin0, CLKin1, or CLKin2, respectively, to be the selected active input clock. In this mode, the EN_CLKinX bits are overriden such that the CLKinX buffer operates even if CLKinX is disabled with EN_CLKinX = 0.

If holdover is entered in this mode by setting CLKin_SEL_MANUAL = 3, then the device will re-lock to the selected CLKin upon holdover exit.

8.3.6.2 Input Clock Switching - Pin Select Mode

When CLKin_SEL_AUTO_EN = 0 and CLKin_SEL_PIN_EN = 1, the active CLKin is selected by the CLKin_SEL# and Status_LD1 pins.

Configuring Pin Select Mode

The CLKin_SEL0_TYPE must be programmed to an input value for the CLKin_SEL0 pin to function as an input for pin select mode.

The CLKin_SEL1_TYPE must be programmed to an input value for the CLKin_SEL1 pin to function as an input for pin select mode.

The polarity of the clock input select pins can be inverted with the CLKin_SEL_PIN_POL bit.

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The pin select mode overrides the EN_CLKinX bits such that the CLKinX buffer operates even if CLKinX is disabled with EN_CLKinX = 0. To switch as fast as possible, keep the clock input buffers (that could be used to switch to) enabled (EN_CLKinX = 1).

8.3.6.3 Input Clock Switching - Automatic Mode

When CLKin_SEL_AUTO_EN = 1, LOS_EN = 1, and HOLDOVER_EXIT_MODE = 0 (Exit based on LOS), the active clock is selected in priority order with CLKin0 being the highest priority, CLKin1 second, and CLKin2 third.

For a clock input to be eligible to be switched to, it must be enabled using EN_CLKinX. The LOS_TIMEOUT should also be set to a frequency below the input frequency.

To ensure LOS is valid for AC-coupled inputs, the MOS mode must be set for the CLKin and no termination is allowed to be between the pins unless the pins are DC.blocked. For example, no 100-Ω termination across CLKin0 and CLKin0* pins on IC side of AC-coupling capacitors.

8.3.7 Digital Lock Detect

Both PLL1 and PLL2 support digital lock detect. Digital lock detect compares the phase between the reference path (R) and the feedback path (N) of the PLL. When the time error, which is phase error, between the two signals is less than a specified window size (ε) a lock detect count increments. When the lock detect count reaches a user specified value, PLL1_DLD_CNT or PLL2_DLD_CNT, lock detect is asserted true. Once digital lock detect is true, a single phase comparison outside the specified window will cause digital lock detect to be asserted false. This is illustrated in 図 8-8.

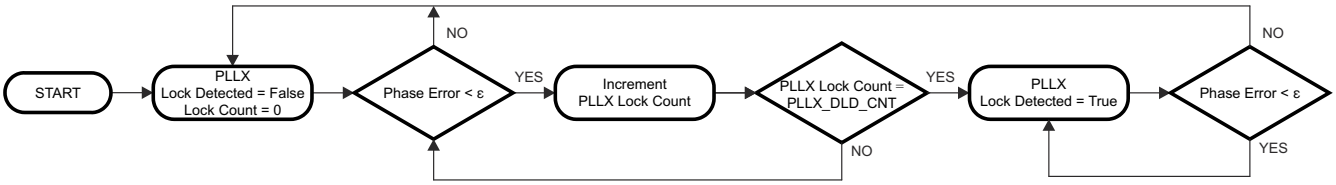


図 8-8. Digital Lock Detect Flowchart

This incremental lock detect count feature functions as a digital filter to ensure that lock detect is not asserted for only a brief time when the phases of R and N are within the specified tolerance for only a brief time during initial phase lock.

See セクション 9.1.2 for more detailed information on programming the registers to achieve a specified frequency accuracy in ppm with lock detect.

The digital lock detect signal can be monitored on the Status_LD1 or Status_LD2 pin. The pin may be programmed to output the status of lock detect for PLL1, PLL2, or both PLL1 and PLL2.

8.3.7.1 Calculating Digital Lock Detect Frequency Accuracy

See セクション 9.1.2 for more detailed information on programming the registers to achieve a specified frequency accuracy in ppm with lock detect.

The digital lock detect feature can also be used with holdover to automatically exit holdover mode. See セクション 8.3.8.3 for more information.

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8.3.8 Holdover

Holdover mode causes PLL2 to stay locked on frequency with minimal frequency drift when an input clock reference to PLL1 becomes invalid. While in holdover mode, the PLL1 charge pump is TRI-STATED and a fixed tuning voltage is set on CPout1 to operate PLL1 in open loop.

8.3.8.1 Enable Holdover

Program HOLDOVER_EN = 1 to enable holdover mode.

Holdover mode can be configured to set the CPout1 voltage upon holdover entry to a fixed user defined voltage (EN_MAN_DAC = 1) or a tracked voltage (EN_MAN_DAC = 0).

8.3.8.1.1 Fixed (Manual) CPout1 Holdover Mode

By programming MAN_DAC_EN = 1, then the MAN_DAC value will be set on the CPout1 pin during holdover.

The user can optionally enable CPout1 voltage tracking (TRACK_EN = 1), read back the tracked DAC value, then re-program MAN_DAC value to a user desired value based on information from previous DAC read backs. This allows the most user control over the holdover CPout1 voltage, but also requires more user intervention.

8.3.8.1.2 Tracked CPout1 Holdover Mode

By programming MAN_DAC_EN = 0 and TRACK_EN = 1, the tracked voltage of CPout1 is set on the CPout1 pin during holdover. When the DAC has acquired the current CPout1 voltage, the *DAC_Locked* signal is set, which may be observed on Status_LD1 or Status_LD2 pins by programming PLL1_LD_MUX or PLL2_LD_MUX, respectively.

Updates to the DAC value for the Tracked CPout1 sub-mode occurs at the rate of the PLL1 phase detector frequency divided by (DAC_CLK_MULT × DAC_CLK_CNTR).

The DAC update rate should be programmed for ≤ 100 kHz to ensure DAC holdover accuracy.

The ability to program slow DAC update rates, for example one DAC update per 4.08 seconds when using 1024-kHz PLL1 phase detector frequency with DAC_CLK_MULT = 16,384 and DAC_CLK_CNTR = 255, allows the device to *look-back* and set CPout1 at a previous *good* CPout1 tuning voltage values before the event which caused holdover to occur.

The current voltage of DAC value can be read back using RB_DAC_VALUE, see セクション 8.6.2.9.6.

8.3.8.2 During Holdover

PLL1 is run in open-loop mode.

- PLL1 charge pump is set to TRI-STATE.
- PLL1 DLD is unasserted.
- The HOLDOVER status is asserted
- During holdover, if PLL2 was locked prior to entry of holdover mode, PLL2 DLD continues to be asserted.
- CPout1 voltage is set to:
  - a voltage set in the MAN_DAC register (MAN_DAC_EN = 1).
  - a voltage determined to be the last valid CPout1 voltage (MAN_DAC_EN = 0).
- PLL1 attempts to lock with the active clock input.

The HOLDOVER status signal can be monitored on the Status_LD1 or Status_LD2 pin by programming the PLL1_DLD_MUX or PLL2_DLD_MUX register to *Holdover Status*.

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8.3.8.3 Exiting Holdover

Holdover mode can be exited in one of two ways.

- Manually, by programming the device from the host.
- Automatically, when the LOS signal unasserts for a clock that provides a valid input to PLL1.

8.3.8.4 Holdover Frequency Accuracy and DAC Performance

When in holdover mode, PLL1 runs in open loop and the DAC sets the CPout1 voltage. If *fixed CPout1* mode is used, then the output of the DAC is dependant upon the MAN_DAC register. If *tracked CPout1* mode is used, then the output of the DAC is approximately the same voltage at the CPout1 pin before holdover mode was entered. When using Tracked mode and MAN_DAC_EN = 1, the DAC value during holdover is loaded with the programmed value in MAN_DAC and not the tracked value.

When in Tracked CPout1 mode, the DAC has a worst-case tracking error of ±2 LSBs once PLL1 tuning voltage is acquired. The step size is approximately 3.2 mV, therefore the VCXO frequency error during holdover mode caused by the DAC tracking accuracy is ±6.4 mV × Kv, where Kv is the tuning sensitivity of the VCXO in use. Therefore, the accuracy of the system when in holdover mode in ppm is:

$$\text{Holdover accuracy (ppm)} = \frac{\pm 6.4\ \text{mV} \times \text{Kv} \times 1e6}{\text{VCXO Frequency}} \quad (2)$$

As an example, consider a system with a 19.2-MHz clock input, a 153.6-MHz VCXO with a Kv of 17 kHz/V. The accuracy of the system in holdover in ppm is:

$$\pm 0.71\ \text{ppm} = \pm 6.4\ \text{mV} \times 17\ \text{kHz/V} \times 1e6 / 153.6\ \text{MHz} \quad (3)$$

It is important to account for this frequency error when determining the allowable frequency error window to cause holdover mode to exit.

8.3.9 PLL2 Loop Filter

PLL2 has an integrated loop filter of C1i = 60 pF, R3 = 2400 Ω, C3 = 50 pF, R4 = 200 Ω and C4 = 10 pF as shown in 図 8-9. Loop filter components C1, C2, and R2 can be solved using TI software. See セクション 10.1 for more information.

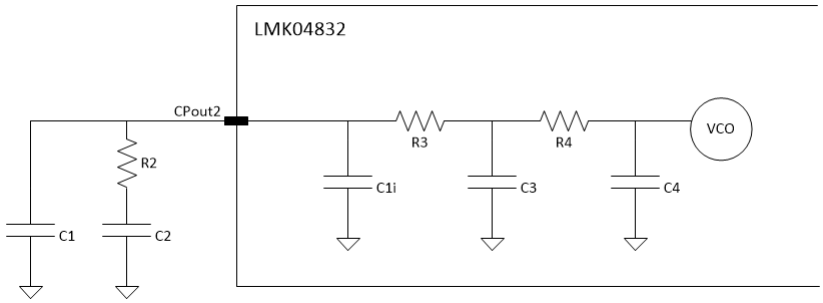


図 8-9. PLL2 On-Chip Loop Filter

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8.4 Device Functional Modes

The LMK04832-SP is a flexible device that can be configured for many different use cases. The following simplified block diagrams help show the user the different use cases of the device.

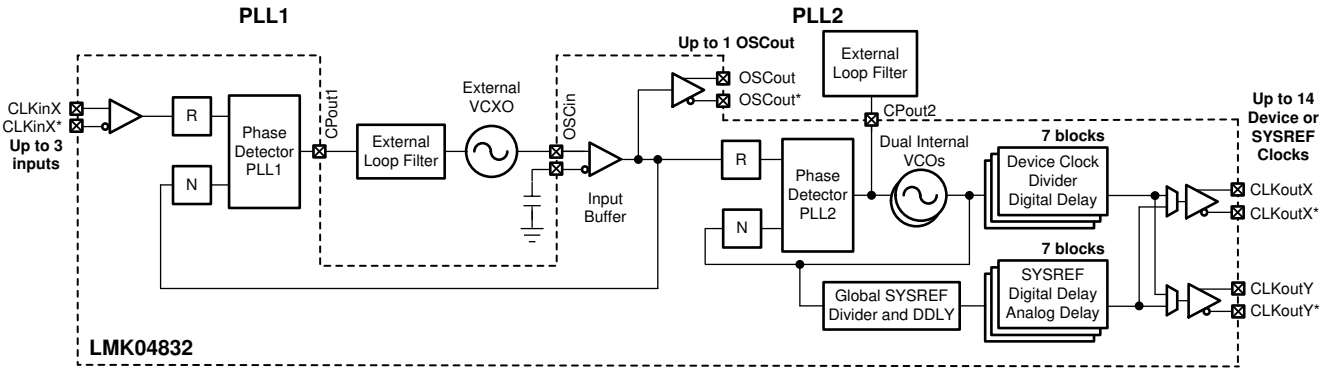
8.4.1 DUAL PLL

8.4.1.1 Dual Loop

図 8-10 illustrates the typical use case of dual loop mode. In dual loop mode, the reference to PLL1 is from CLKin0, CLKin1, or CLKin2. An external VCXO is used to provide feedback for the first PLL and a reference to the second PLL. This first PLL cleans the jitter with the VCXO by using a narrow loop bandwidth. The VCXO may be buffered through the OSCout port. The VCXO is used as the reference to PLL2 and may be doubled using the frequency doubler. The internal VCO drives up to seven divide/delay blocks which drive up to 14 clock outputs.

Hitless switching and holdover functionality are optionally available when the input reference clock is lost. Holdover works by forcing a DAC voltage to the tuning voltage of the VCXO.

It is also possible to use an external VCO in place of PLL2's internal VCO. In this case one less CLKin is available as a reference as CLKin1 is used for external input.



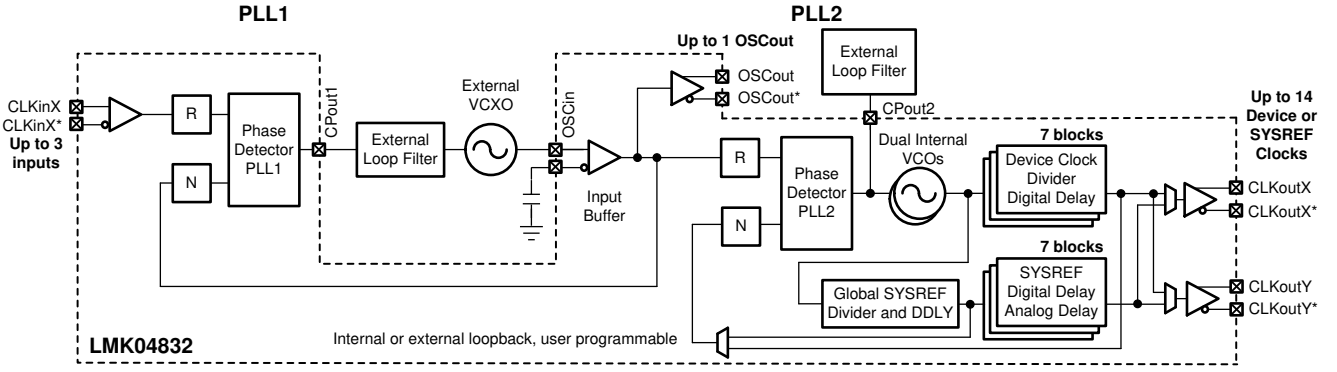
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図 8-10. Simplified Functional Block Diagram for Dual Loop Mode

8.4.1.2 Dual Loop With Cascaded 0-Delay

図 8-11 illustrates the use case of cascaded 0-delay dual loop mode. This configuration differs from dual loop mode 図 8-10 in that the feedback for PLL2 is driven by a clock output instead of the VCO output directly.

It is also possible to use an external VCO in place of the internal VCO of the PLL2, but one less CLKin is available as a reference and the external 0-delay feedback is not available.

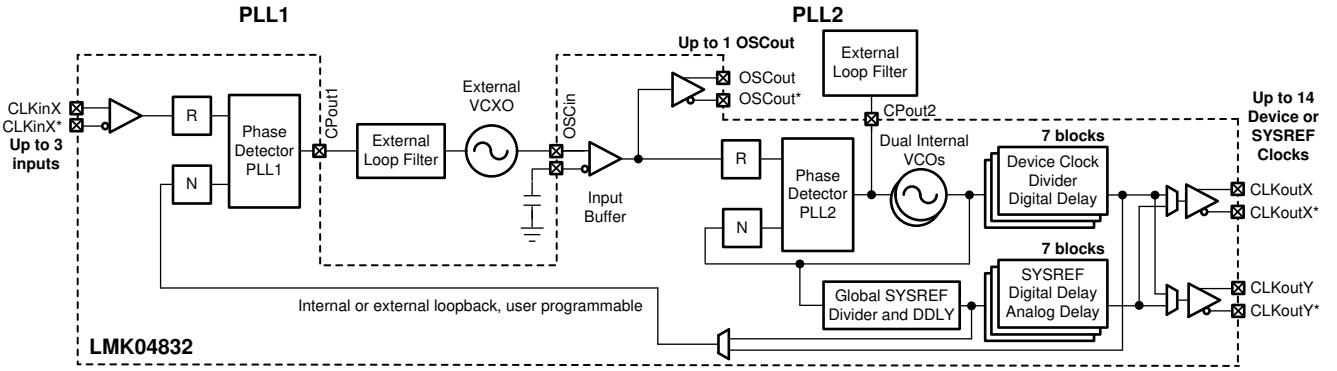


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図 8-11. Simplified Functional Block Diagram for Cascaded 0-Delay Dual Loop Mode

8.4.1.3 Dual Loop With Nested 0-Delay

図 8-12 illustrates the use case of nested 0-delay dual loop mode. This configuration is similar to the dual PLL in 図 8-10 except that the feedback to the first PLL is driven by a clock output. The PLL2 reference OSCin is not deterministic to the CLKin or feedback clock.



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図 8-12. Simplified Functional Block Diagram for Nested 0-Delay Dual Loop Mode

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8.4.2 Single PLL

8.4.2.1 PLL2 Single Loop

図 8-13 illustrates the use case of PLL2 single loop mode. When used with a high-frequency clean reference performance as good as dual loop mode may be achieved. Traditionally the OSCin is used as a reference to PLL2, but it is also possible to use CLKinX as a reference to PLL2.

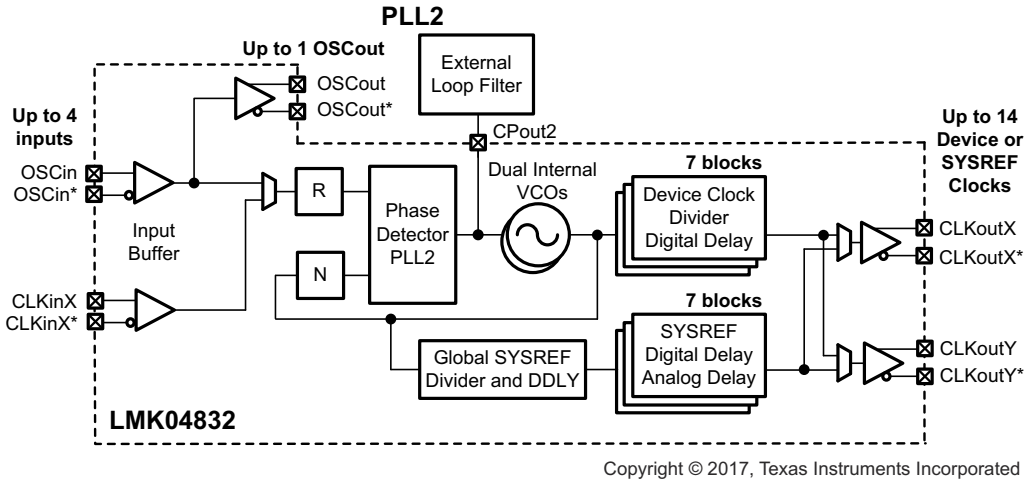


図 8-13. Simplified Functional Block Diagram for Single Loop Mode

8.4.2.2 PLL2 With External VCO

Adding an external VCO is possible using the Fin0/Fin1 input pins. The input may be single-ended or differential. At high frequency the input impedance to Fin0/Fin1 is low, a resistive pad is recommended for matching.

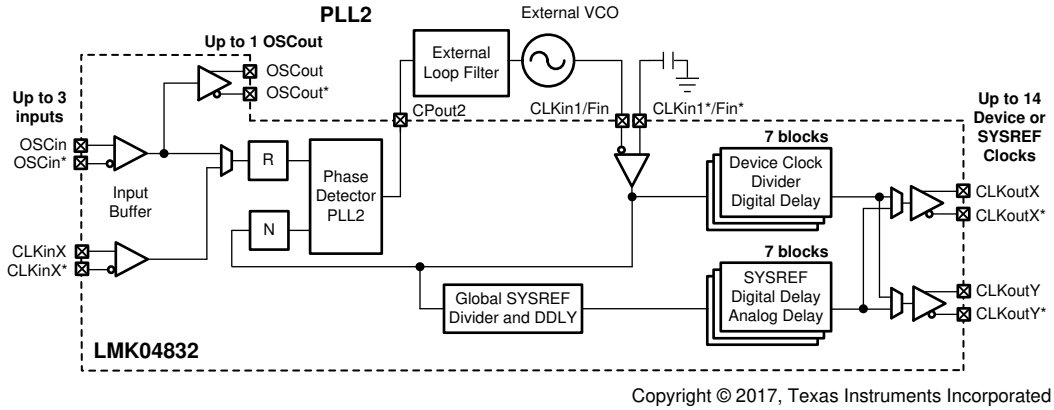
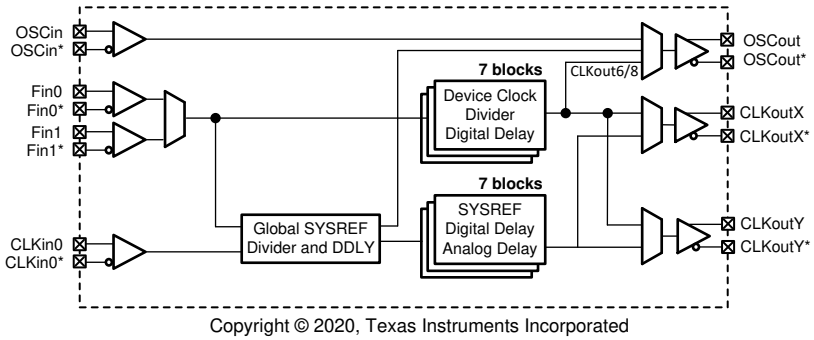


図 8-14. Simplified Functional Block Diagram for Single Loop Mode With External VCO

8.4.3 Distribution Mode

図 8-15 illustrates the use case of distribution mode. As in all the other use cases, OSCin to OSCout can be used as a buffer to OSCin or from clock distribution path through CLKout6, CLKout8, or the SYSREF divider.

At high frequency, the input impedance to Fin0/Fin1 is low and a resistive pad is recommended for matching.



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図 8-15. Simplified Functional Block Diagram for Distribution Mode

8.5 Programming

The LMK04832 device is programmed using 24-bit registers. Each register consists of a 1-bit command field (R/W), a 15-bit address field (A14 to A0) and a 8-bit data field (D7 to D0). The contents of each register is clocked in MSB first (R/W), and the LSB (D0) last. During programming, the CS* signal is held low. The serial data is clocked in on the rising edge of the SCK signal. After the LSB is clocked in, the CS* signal goes *high* to latch the contents into the shift register. TI recommends to program registers in numeric order (for example, 0x000 to 0x555 with exceptions noted in the セクション 8.5.1). Each register consists of one or more fields which control the device functionality. See the セクション 6.5 section and 図 6-1 for timing details.

8.5.1 Recommended Programming Sequence

Registers are generally programmed in numeric order with 0x000 being the first and 0x555 being the last register programmed. The recommended programming sequence from POR involves:

1. Program register 0x000 with RESET = 1.
2. Program defined registers from 0x000 to 0x165.
3. If PLL2 is used, program 0x173 with PLL2_PD and PLL2_PRE_PD clear to allow PLL2 to lock after PLL2_N is programmed.
4. Continue programming defined registers from 0x166 to 0x555.

注

When using the internal VCO, PLL2_N registers 0x166, 0x167, and 0x168 must be programmed after other PLL2 dividers are programed to ensure proper VCO frequency calibration. This is also true for PLL2_N_CAL registers 0x163, 0x164, 0x165 when PLL2_NCLK_MUX = 1. So if any divider such as PLL2_R is altered to change the VCO frequency, the VCO calibration must be run again by programming PLL2_N.

Power up PLL2 by setting PLL2_PRE_PD = 0 and PLL2_PD = 0 in register 0x173 before programming PLL2_N.

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8.6 Register Maps

8.6.1 Register Map for Device Programming

表 8-6 provides the register map for device programming. Any register can be read from the same data address it is written to.

表 8-6. Register Map

ADDRESS [14:0]	DATA[7:0]							
23:8	7	6	5	4	3	2	1	0
0x000	RESET	0	0	SPI_3WIRE_DIS	0	0	0	0
0x002	0	0	0	0	0	0	0	POWER DOWN
0x003	ID_DEVICE_TYPE							
0x004	ID_PROD[15:8]							
0x005	ID_PROD[7:0]							
0x006	ID_MASKREV							
0x00C	ID_VNDR[15:8]							
0x00D	ID_VNDR[7:0]							
0x100	DCLK0_1_DIV[7:0]							
0x101	DCLK0_1_DDLY[7:0]							
0x102	CLKout0_1_PD	CLKout0_1_ODL	CLKout0_1_IDL	DCLK0_1_DDLY_PD	DCLK0_1_DDLY[9:8]		DCLK0_1_DIV[9:8]	
0x103	0	1	CLKout0_SRC_MUX	DCLK0_1_PD	DCLK0_1_BYP	DCLK0_1_DCC	DCLK0_1_POL	DCLK0_1_HS
0x104	0	0	CLKout1_SRC_MUX	SCLK0_1_PD	SCLK0_1_DIS_MODE		SCLK0_1_POL	SCLK0_1_HS
0x105	0	0	SCLK0_1_ADLY_EN	SCLK0_1_ADLY				
0x106	0	0	0	0	SCLK0_1_DDLY			
0x107	CLKout1_FMT				CLKout0_FMT			
0x108	DCLK2_3_DIV[7:0]							
0x109	DCLK2_3_DDLY[7:0]							
0x10A	CLKout2_3_PD	CLKout2_3_ODL	CLKout2_3_IDL	DCLK2_3_DDLY_PD	DCLK2_3_DDLY[9:8]		DCLK2_3_DIV[9:8]	
0x10B	0	1	CLKout2_SRC_MUX	DCLK2_3_PD	DCLK2_3_BYP	DCLK2_3_DCC	DCLK2_3_POL	DCLK2_3_HS
0x10C	0	0	CLKout3_SRC_MUX	SCLK2_3_PD	SCLK2_3_DIS_MODE		SCLK2_3_POL	SCLK2_3_HS
0x10D	0	0	SCLK2_3_ADLY_EN	SCLK2_3_ADLY				
0x10E	0	0	0	0	SCLK2_3_DDLY			
0x10F	CLKout3_FMT				CLKout2_FMT			
0x110	DCLK4_5_DIV[7:0]							
0x111	DCLK4_5_DDLY[7:0]							
0x112	CLKout4_5_PD	CLKout4_5_ODL	CLKout4_5_IDL	DCLK4_5_DDLY_PD	DCLK4_5_DDLY[9:8]		DCLK4_5_DIV[9:8]	
0x113	0	1	CLKout4_SRC_MUX	DCLK4_5_PD	DCLK4_5_BYP	DCLK4_5_DCC	DCLK4_5_POL	DCLK4_5_HS
0x114	0	0	CLKout5_SRC_MUX	SCLK4_5_PD	SCLK4_5_DIS_MODE		SCLK4_5_POL	SCLK4_5_HS
0x115	0	0	SCLK4_5_ADLY_EN	SCLK4_5_ADLY				
0x116	0	0	0	0	SCLK4_5_DDLY			
0x117	CLKout5_FMT				CLKout4_FMT			
0x118	DCLK6_7_DIV[7:0]							

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表 8-6. Register Map (continued)

ADDRESS [14:0]	DATA[7:0]							
23:8	7	6	5	4	3	2	1	0
0x119	DCLK6_7_DDLY[7:0]							
0x11A	CLKout6_7_PD	CLKout6_7_ODL	CLKout6_7_IDL	DCLK6_7_DDLY_PD	DCLK6_7_DDLY[9:8]		DCLK6_7_DIV[9:8]	
0x11B	0	1	CLKout6_SRC_MUX	DCLK6_7_PD	DCLK6_7_BYP	DCLK6_7_DCC	DCLK6_7_POL	DCLK6_7_HS
0x11C	0	0	CLKout7_SRC_MUX	SCLK6_7_PD	SCLK6_7_DIS_MODE		SCLK6_7_POL	SCLK6_7_HS
0x11D	0	0	SCLK6_7_ADLY_EN	SCLK6_7_ADLY				
0x11E	0	0	0	0	SCLK6_7_DDLY			
0x11F	CLKout7_FMT				CLKout6_FMT			
0x120	DCLK8_9_DIV[7:0]							
0x121	DCLK8_9_DDLY[7:0]							
0x122	CLKout8_9_PD	CLKout8_9_ODL	CLKout8_9_IDL	DCLK8_9_DDLY_PD	DCLK8_9_DDLY[9:8]		DCLK8_9_DIV[9:8]	
0x123	0	1	CLKout8_SRC_MUX	DCLK8_9_PD	DCLK8_9_BYP	DCLK8_9_DCC	DCLK8_9_POL	DCLK8_9_HS
0x124	0	0	CLKout9_SRC_MUX	SCLK8_9_PD	SCLK8_9_DIS_MODE		SCLK8_9_POL	SCLK8_9_HS
0x125	0	0	SCLK8_9_ADLY_EN	SCLK8_9_ADLY				
0x126	0	0	0	0	SCLK8_9_DDLY			
0x127	CLKout9_FMT				CLKout8_FMT			
0x128	DCLK10_11_DIV[7:0]							
0x129	DCLK10_11_DDLY[7:0]							
0x12A	CLKout10_11_PD	CLKout10_11_ODL	CLKout10_11_IDL	DCLK10_11_DDLY_PD	DCLK10_11_DDLY[9:8]		DCLK10_11_DIV[9:8]	
0x12B	0	1	CLKout10_SRC_MUX	DCLK10_11_PD	DCLK10_11_BYP	DCLK10_11_DCC	DCLK10_11_POL	DCLK10_11_HS
0x12C	0	0	CLKout11_SRC_MUX	SCLK10_11_PD	SCLK10_11_DIS_MODE		SCLK10_11_POL	SCLK10_11_HS
0x12D	0	0	SCLK10_11_ADLY_EN	SCLK10_11_ADLY				
0x12E	0	0	0	0	SCLK10_11_DDLY			
0x12F	CLKout11_FMT				CLKout10_FMT			
0x130	DCLK12_13_DIV[7:0]							
0x131	DCLK12_13_DDLY[7:0]							
0x132	CLKout12_13_PD	CLKout12_13_ODL	CLKout12_13_IDL	DCLK12_13_DDLY_PD	DCLK12_13_DDLY[9:8]		DCLK12_13_DIV[9:8]	
0x133	0	1	CLKout12_SRC_MUX	DCLK12_13_PD	DCLK12_13_BYP	DCLK12_13_DCC	DCLK12_13_POL	DCLK12_13_HS
0x134	0	0	CLKout13_SRC_MUX	SCLK12_13_PD	SCLK12_13_DIS_MODE		SCLK12_13_POL	SCLK12_13_HS
0x135	0	0	SCLK12_13_ADLY_EN	SCLK12_13_ADLY				
0x136	0	0	0	0	SCLK12_13_DDLY			
0x137	CLKout13_FMT				CLKout12_FMT			
0x138	0	VCO_MUX		OSCout_MUX	OSCout_FMT			
0x139	0	0	0	SYSREF_REQ_EN	SYNC_BYPASS	0	SYSREF_MUX	
0x13A	0	0	0	SYSREF_DIV[12:8]				
0x13B	SYSREF_DIV[7:0]							
0x13C	0	0	0	SYSREF_DDLY[12:8]				
0x13D	SYSREF_DDLY[7:0]							

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表 8-6. Register Map (continued)

ADDRESS [14:0]	DATA[7:0]							
23:8	7	6	5	4	3	2	1	0
0x13E	0	0	0	0	0	SYSREF_PULSE_CNT		
0x13F	PLL2_RCLK_MUX	0	PLL2_NCLK_MUX	PLL1_NCLK_MUX		FB_MUX		FB_MUX_EN
0x140	PLL1_PD	VCO_LDO_PD	VCO_PD	OSCin_PD	SYSREF_GBL_PD	SYSREF_PD	SYSREF_DDLY_PD	SYSREF_PLSR_PD
0x141	DDLYd_SYSREF_EN	DDLYd12_EN	DDLYd10_EN	DDLYd8_EN	DDLYd6_EN	DDLYd4_EN	DDLYd2_EN	DDLYd0_EN
0x142	DDLYd_STEP_CNT							
0x143	SYSREF_CLR	SYNC_1SHOT_EN	SYNC_POL	SYNC_EN	SYNC_PLL2_DLD	SYNC_PLL1_DLD	SYNC_MODE	
0x144	SYNC_DISSYSREF	SYNC_DIS12	SYNC_DIS10	SYNC_DIS8	SYNC_DIS6	SYNC_DIS4	SYNC_DIS2	SYNC_DIS0
0x145	2	PLL1R_SYNC_EN	PLL1R_SYNC_SRC		PLL2R_SYNC_EN	FIN0_DIV2_EN	FIN0_INPUT_TYPE	
0x146	CLKin_SEL_PIN_EN	CLKin_SEL_PIN_POL	CLKin2_EN	CLKin1_EN	CLKin0_EN	CLKin2_TYPE	CLKin1_TYPE	CLKin0_TYPE
0x147	CLKin_SEL_AUTO_REVERT_EN	CLKin_SEL_AUTO_EN	CLKin_SEL_MANUAL		CLKin1_DEMUX		CLKin0_DEMUX	
0x148	0	0	CLKin_SEL0_MUX			CLKin_SEL0_TYPE		
0x149	0	SDIO_RDBK_TYPE	CLKin_SEL1_MUX			CLKin_SEL1_TYPE		
0x14A	0	0	RESET_MUX			RESET_TYPE		
0x14B	LOS_TIMEOUT		LOS_EN	TRACK_EN	HOLDOVER_FORCE	MAN_DAC_EN	MAN_DAC[9:8]	
0x14C	MAN_DAC[7:0]							
0x14D	0	0	DAC_TRIP_LOW					
0x14E	DAC_CLK_MULT		DAC_TRIP_HIGH					
0x14F	DAC_CLK_CNTR							
0x150	0	CLKin_OVERRIDE	HOLDOVER_EXIT_MODE	HOLDOVER_PLL1_DET	LOS_EXTERNAL_INPUT	HOLDOVER_VTUNE_DET	CLKin_SWITCH_CP_TRI	HOLDOVER_EN
0x151	0	0	HOLDOVER_DLD_CNT[13:8]					
0x152	HOLDOVER_DLD_CNT[7:0]							
0x153	0	0	CLKin0_R[13:8]					
0x154	CLKin0_R[7:0]							
0x155	0	0	CLKin1_R[13:8]					
0x156	CLKin1_R[7:0]							
0x157	0	0	CLKin2_R[13:8]					
0x158	CLKin2_R[7:0]							
0x159	0	0	PLL1_N[13:8]					
0x15A	PLL1_N[7:0]							
0x15B	PLL1_WND_SIZE		PLL1_CP_TRI	PLL1_CP_POL	PLL1_CP_GAIN			
0x15C	0	0	PLL1_DLD_CNT[13:8]					
0x15D	PLL1_DLD_CNT[7:0]							
0x15E	0	0	0	HOLDOVER_EXIT_NADJ				
0x15F	PLL1_LD_MUX					PLL1_LD_TYPE		
0x160	0	0	0	0	PLL2_R			
0x161	PLL2_R							
0x162	PLL2_P			0	OSCin_FREQ		PLL2_XTAL_EN	PLL2_REF_2X_EN
0x163	0	0	0	0	0	0	PLL2_N_CAL[17:16]	
0x164	PLL2_N_CAL[15:8]							

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表 8-6. Register Map (continued)

ADDRESS [14:0]	DATA[7:0]							
23:8	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
0x165	PLL2_N_CAL[7:0]							
0x166	0	0	0	0	0	0	PLL2_N[17:16]	
0x167	PLL2_N[15:8]							
0x168	PLL2_N[7:0]							
0x169	0	PLL2_WND_SIZE		PLL2_CP_GAIN		PLL2_CP_POL	PLL2_CP_TRI	PLL2_DLD_EN
0x16A	0	0	PLL2_DLD_CNT[13:8]					
0x16B	PLL2_DLD_CNT[7:0]							
0x16C	0	0	0	0	0	0	0	0
0x173	0	PLL2_PRE_PD	PLL2_PD	FIN0_PD	0	0	0	0
0x177			PLL1R_RST					
0x182	0	0	0	0	0	0	CLR_PLL1_LD_LOST	CLR_PLL2_LD_LOST
0x183	0	0	0	0	RB_PLL1_DLD_LOST	RB_PLL1_DLD	RB_PLL2_DLD_LOST	RB_PLL2_DLD
0x184	RB_DAC_VALUE[9:8]		RB_CLKin2_SEL	RB_CLKin1_SEL	RB_CLKin0_SEL	RB_CLKin2_LOS	RB_CLKin1_LOS	RB_CLKin0_LOS
0x185	RB_DAC_VALUE[7:0]							
0x188	0	X	RB_HOLDOVER	X	RB_DAC_RAIL	RB_DAC_HIGH	RB_DAC_LOW	RB_DAC_LOCKED
0x555	SPI_LOCK							

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8.6.2 Device Register Descriptions

The following section details the fields of each register, the Power-On-Reset Defaults, and specific descriptions of each bit.

In some cases similar fields are located in multiple registers. In this case specific outputs may be designated as X or Y. In these cases, the X represents even numbers from 0 to 12 and the Y represents odd numbers from 1 to 13. In the case where X and Y are both used in a bit name, then Y = X + 1.

8.6.2.1 System Functions

8.6.2.1.1 RESET, SPI_3WIRE_DIS

This register contains the RESET function and the ability to turn off 3-wire SPI mode. To use a 4-wire SPI mode, selecting SPI Read back in one of the output MUX settings. For example CLKin0_SEL_MUX or RESET_MUX. It is possible to have 3-wire and 4-wire readback at the same time.

表 8-7. Register 0x000

BIT	NAME	POR DEFAULT	DESCRIPTION
7	RESET	0	0: Normal operation 1: Reset (automatically cleared)
6:5	NA	0	Reserved
4	SPI_3WIRE_DIS	0	Disable 3-wire SPI mode. 0: 3 Wire Mode enabled 1: 3 Wire Mode disabled
3:0	NA	NA	Reserved

8.6.2.1.2 POWERDOWN

This register contains the POWERDOWN function.

表 8-8. Register 0x002

BIT	NAME	POR DEFAULT	DESCRIPTION
7:1	NA	0	Reserved
0	POWERDOWN	0	0: Normal operation 1: Power down device.

8.6.2.1.3 ID_DEVICE_TYPE

This register contains the product device type. This is read only register.

表 8-9. Register 0x003

BIT	NAME	POR DEFAULT	DESCRIPTION
7:0	ID_DEVICE_TYPE	6	PLL product device type.

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8.6.2.1.4 ID_PROD

These registers contain the product identifier. This is a read only register.

表 8-10. ID_PROD Field Registers

MSB	LSB
0x004[7:0] / ID_PROD[15:8]	0x005[7:0] / ID_PROD[7:0]

表 8-11. Registers 0x004 and 0x005

REGISTER	BIT	FIELD NAME	POR DEFAULT	DESCRIPTION
0x004	7:0	ID_PROD[15:8]	209 (0xD1)	MSB of the product identifier.
0x005	7:0	ID_PROD[7:0]	99 (0x63)	LSB of the product identifier.

8.6.2.1.5 ID_MASKREV

This register contains the IC version identifier. This is a read only register.

表 8-12. Register 0x006

BIT	NAME	POR DEFAULT	DESCRIPTION
7:0	ID_MASKREV	112 (0x70)	IC version identifier

8.6.2.1.6 ID_VNDR

These registers contain the vendor identifier. This is a read only register.

表 8-13. ID_VNDR Field Registers

MSB	LSB
0x00C[7:0] / ID_VNDR[15:8]	0x00D[7:0] / ID_VNDR[7:0]

表 8-14. Registers 0x00C, 0x00D

REGISTER	BIT	NAME	POR DEFAULT	DESCRIPTION
0x00C	7:0	ID_VNDR[15:8]	81 (0x51)	MSB of the vendor identifier.
0x00D	7:0	ID_VNDR[7:0]	4 (0x04)	LSB of the vendor identifier.

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8.6.2.2 (0x100 - 0x138) Device Clock and SYSREF Clock Output Controls

8.6.2.2.1 DCLKX_Y_DIV

The device clock divider can drive up to two outputs, an even (X) and an odd (Y) clock output. Divide is a 10 bit number and split across two registers.

表 8-15. DCLKX_Y_DIV Field Registers

MSB	LSB
0x0102[1:0] = DCLK0_1_DIV[9:8]	0x100[7:0] = DCLK0_1_DIV[7:0]
0x010A[1:0] = DCLK2_3_DIV[9:8]	0x108[7:0] = DCLK2_3_DIV[7:0]
0x0112[1:0] = DCLK4_5_DIV[9:8]	0x110[7:0] = DCLK4_5_DIV[7:0]
0x011A[1:0] = DCLK6_7_DIV[9:8]	0x118[7:0] = DCLK6_7_DIV[7:0]
0x0122[1:0] = DCLK8_9_DIV[9:8]	0x120[7:0] = DCLK8_9_DIV[7:0]
0x012A[1:0] = DCLK10_11_DIV[9:8]	0x128[7:0] = DCLK10_11_DIV[7:0]
0x0132[1:0] = DCLK12_13_DIV[9:8]	0x130[7:0] = DCLK12_13_DIV[7:0]

表 8-16. Registers 0x100, 0x108, 0x110, 0x118, 0x120, 0x128, and 0x130 0x102, 0x10A, 0x112, 0x11A, 0x122, 0x12A, 0x132

REGISTER	BIT	NAME	POR DEFAULT	DESCRIPTION	
0x102, 0x10A, 0x112, 0x11A, 0x122, 0x12A, 0x132	1:0	DCLKX_Y_DIV[9:8]	X_Y = 0_1 → 2 X_Y = 2_3 → 4 X_Y = 4_5 → 8 X_Y = 6_7 → 8 X_Y = 8_9 → 8 X_Y = 10_11 → 8 X_Y = 12_13 → 2	DCLKX_Y_DIV sets the divide value for the clock output, the divide may be even or odd. Both even or odd divides output a 50% duty cycle clock if duty cycle correction (DCC) is enabled.	
0x100, 0x108, 0x110, 0x118, 0x120, 0x128, and 0x130	7:0	DCLKX_Y_DIV[7:0]		**Field Value**	**Divider Value**
				0 (0x00)	Reserved
				1 (0x01)	1 (1)
				2 (0x02)	2
				...	...
				1022 (0x3FE)	1022
				1023 (0x3FF)	1023

(1) Duty cycle correction must also be enabled, DCLKX_Y_DCC = 1.

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8.6.2.2.2 DCLKX_Y_DDLY

This register controls the digital delay for the device clock outputs.

表 8-17. DCLKX_Y_DDLY Field Registers

MSB	LSB
0x0102[2:3] = DCLK0_1_DDLY[9:8]	0x101[7:0] = DCLK0_1_DDLY[7:0]
0x010A[2:3] = DCLK2_3_DDLY[9:8]	0x109[7:0] = DCLK2_3_DDLY[7:0]
0x0112[2:3] = DCLK4_5_DDLY[9:8]	0x111[7:0] = DCLK4_5_DDLY[7:0]
0x011A[2:3] = DCLK6_7_DDLY[9:8]	0x119[7:0] = DCLK6_7_DDLY[7:0]
0x0122[2:3] = DCLK8_9_DDLY[9:8]	0x121[7:0] = DCLK8_9_DDLY[7:0]
0x012A[2:3] = DCLK10_11_DDLY[9:8]	0x129[7:0] = DCLK10_11_DDLY[7:0]
0x0132[2:3] = DCLK12_13_DDLY[9:8]	0x131[7:0] = DCLK12_13_DDLY[7:0]

表 8-18. Registers 0x101, 0x109, 0x111, 0x119, 0x121, 0x129, 0x131 0x102, 0x10A, 0x112, 0x11A, 0x122, 0x12A, 0x132

REGISTER	BIT	NAME	POR DEFAULT	DESCRIPTION	
0x102, 0x10A, 0x112, 0x11A, 0x122, 0x12A, 0x132	2:3	DCLKX_Y_DDLY[9:8]	10 (0x0A)	Static digital delay which takes effect after a SYNC.	
				Field Value	**Delay Values**
				0 (0x00)	Reserved
				1 (0x01)	Reserved
				...	...
0x101, 0x109, 0x111, 0x119, 0x121, 0x129, 0x131	7:0	DCLKX_Y_DDLY[7:0]		7 (0x07)	Reserved
				8 (0x08)	8
				9 (0x09)	9
				...	...
				1022 (0x3FE)	1022
				1023 (0x3FF)	1023

Depending on the DCLK divide value, there may be an adjustment in phase delay required. 表 8-19 illustrate the impact of different divide values on the final digital delay.

表 8-19. Digital Delay Adjustment based on Divide Values

DIVIDE VALUE	DIGITAL DELAY ADJUSTMENT
2, 3	–2(1)
4, 7 to 1023	0
5	+2
6	+1

(1) Before SYNC, program divider to Divide-by-4, then back to Divide-by-2 or Divide-by-3 to ensure '-2' delay relationship.

For example, 表 8-20 illustrates a system with clock outputs having divide values /2,/4,/5 and /6 to share a common edge.

表 8-20. Digital Delay Adjustment Illustration

DIVIDE VALUE	PROGRAMMED DDLY	ACTUAL DDLY
2	13	11
4	11	11
5	8	11
6	10	11

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8.6.2.2.3 CLKoutX_Y_PD, CLKoutX_Y_ODL, CLKoutX_Y_IDL, DCLKX_Y_DDLY_PD, DCLKX_Y_DDLY[9:8], DCLKX_Y_DIV[9:8]

表 8-21. Registers 0x102, 0x10A, 0x112, 0x11A, 0x122, 0x12A, 0x132

BIT	NAME	POR DEFAULT	DESCRIPTION
7	CLKoutX_Y_PD	1	Power down the clock group defined by X and Y. 0: Enabled 1: Power down entire clock group including both CLKoutX and CLKoutY.
6	CLKoutX_Y_ODL	0	Sets output drive level for clocks. This has no impact for the even clock output in bypass mode. 0: Normal operation 1: Higher current consumption and lower noise floor.
5	CLKoutX_Y_IDL	0	Sets input drive level for clocks. 0: Normal operation 1: Higher current consumption and lower noise floor.
4	DCLKX_Y_DDLY_PD	0	Powerdown the device clock digital delay circuitry. 0: Enabled 1: Power down static digital delay for device clock divider.
3:2	DCLKX_Y_DDLY[9:8]	0	MSB of static digital delay, see セクション 8.6.2.2.2.
1:0	DCLKX_Y_DIV[9:8]	0	MSB of device clock divide value, see 表 8-16.

8.6.2.2.4 CLKoutX_SRC_MUX, CLKoutX_Y_PD, DCLKX_Y_BYP, DCLKX_Y_DCC, DCLKX_Y_POL, DCLKX_Y_HS

These registers control the analog delay properties for the device clocks.

表 8-22. Registers 0x103, 0x10B, 0x113, 0x11B, 0x123, 0x12B, 0x133

BIT	NAME	POR DEFAULT	DESCRIPTION
7	NA	0	Reserved
6	NA	1	Reserved
5	CLKoutX_SRC_MUX	0	Select CLKoutX clock source. Source must also be powered up. 0: Device Clock 1: SYSREF
4	CLKoutX_Y_PD	0	Power down the clock group defined by X and Y. 0: Enabled 1: Power down enter clock group X_Y.
3	DCLKX_BYP	0	Enable high performance bypass path for even clock outputs. 0: CLKoutX not in high performance bypass mode. CML is not valid for CLKoutX_FMT. 1: CLKoutX in high performance bypass mode. Only CML clock format is valid.
2	DCLKX_Y_DCC	0	Duty cycle correction for device clock divider. Required for half step. 0: No duty cycle correction. 1: Duty cycle correction enabled.
1	DCLKX_Y_POL	0	Invert polarity of device clock output. This also applies to CLKoutX in high performance bypass mode. Polarity invert is a method to get a half-step phase adjustment in high performance bypass mode or /1 divide value. 0: Normal polarity 1: Invert polarity
0	DCLKX_Y_HS	0	Sets the device clock half step value. Must be set to zero (0) for a divide of 1. No effect if DCLKX_Y_DCC = 0. 0: No phase adjustment 1: Adjust device clock phase –0.5 clock distribution path cycles.

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8.6.2.2.5 CLKoutY_SRC_MUX, SCLKX_Y_PD, SCLKX_Y_DIS_MODE, SCLKX_Y_POL, SCLKX_Y_HS

These registers set the half step for the device clock, the SYSREF output MUX, the SYSREF clock digital delay, and half step.

表 8-23. Registers 0x104, 0x10C, 0x114, 0x11C, 0x124, 0x12C, 0x134

BIT	NAME	POR DEFAULT	DESCRIPTION	
7:6	NA	0	Reserved	
5	CLKoutY_SRC_MUX	0	Select CLKoutX clock source. Source must also be powered up. 0: Device Clock 1: SYSREF	
4	SCLKX_Y_PD	1	Power down the SYSREF clock output circuitry. 0: SYSREF enabled 1: Power down SYSREF path for clock pair.	
3:2	SCLKX_Y_DIS_MODE	0	Set disable mode for clock outputs controlled by SYSREF. Some cases will assert when SYSREF_GBL_PD = 1.	
			Field Value	**Disable Mode**
			0 (0x00)	Active in normal operation
			1 (0x01)	If SYSREF_GBL_PD = 1, the output is a logic low, otherwise it is active.
			2 (0x02)	If SYSREF_GBL_PD = 1, the output is a nominal Vcm voltage for odd clock channels(1) and low for even clocks. Otherwise outputs are active.
			3 (0x03)	Output is a nominal Vcm voltage(1)
1	SCLKX_Y_POL	0	Sets the polarity of clock on SCLKX_Y when SYSREF clock output is selected with CLKoutX_MUX or CLKoutY_MUX. 0: Normal 1: Inverted	
0	SCLKX_Y_HS	0	Sets the local SYSREF clock half step value. 0: No phase adjustment 1: Adjust device SYSREF phase -0.5 clock distribution path cycles.	

(1) If LVPECL mode is used with emitter resistors to ground, the output Vcm will be approximately 0 V, each pin will be approximately 0 V. If CML mode is used with pullups to V_{CC}, the output V_{CM} will be approximately V_{CC} V, each pin will be approximately V_{CC} V.

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8.6.2.2.6 SCLKX_Y_ADLY_EN, SCLKX_Y_ADLY

These registers set the analog delay parameters for the SYSREF outputs.

表 8-24. Registers 0x105, 0x10D, 0x115, 0x11D, 0x125, 0x12D, 0x135

BIT	NAME	POR DEFAULT	DESCRIPTION	
7:6	NA	0	Reserved	
5	SCLKX_Y _ADLY_EN	0	Enables analog delay for the SYSREF output. 0: Disabled 1: Enabled	
4:0	SCLKX_Y _ADLY	0	SYSREF analog delay in approximately 21 ps steps. Selecting analog delay adds an additional 125 ps in propagation delay. Range is 125 ps to 608 ps.	
			Field Value	**Delay Value**
			0 (0x0)	125 ps
			1 (0x1)	146 ps (+21 ps from 0x00)
			2 (0x2)	167 ps (+42 ps from 0x00)
			3 (0x3)	188 ps (+63 ps from 0x00)
			...	...
			14 (0xE)	587 ps (+462 ps from 0x00)
			15 (0xF)	608 ps (+483 ps from 0x00)

8.6.2.2.7 SCLKX_Y_DDLY

表 8-25. Registers 0x106, 0x10E, 0x116, 0x11E, 0x126, 0x12E, 0x136

BIT	NAME	POR DEFAULT	DESCRIPTION
7:4	NA	0	Reserved
3:0	SCLKX_Y_DDLY	0	Set digital delay value for SYSREF clock (minimum 8)

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8.6.2.2.8 CLKoutY_FMT, CLKoutX_FMT

The difference in the tables is that some of the clock outputs have inverted CMOS polarity settings.

表 8-26. Registers 0x107 (CLKout0_1), 0x11F (CLKout6_7), 0x12F (CLKout10_11)

BIT	NAME	POR DEFAULT	DESCRIPTION		
7:4	CLKoutY_FMT	0	Set CLKoutY clock format		
			Field Value	**Output Format**	
			0 (0x00)	Powerdown	
			1 (0x01)	LVDS	
			2 (0x02)	HSDS 6 mA	
			3 (0x03)	HSDS 8 mA	
			4 (0x04)	LVPECL 1600 mV	
			5 (0x05)	LVPECL 2000 mV	
			6 (0x06)	LCPECL	
			7 (0x07)	CML 16 mA	
			8 (0x08)	CML 24 mA	
			9 (0x09)	CML 32 mA	
			10 (0x0A)	CMOS (Off/Inv)	
			11 (0x0B)	CMOS (Norm/Off)	
			12 (0x0C)	CMOS (Inv/Inv)	
			13 (0x0D)	CMOS (Inv/Norm)	
			14 (0x0E)	CMOS (Norm/Inv)	
			15 (0x0F)	CMOS (Norm/Norm)	
3:0	CLKoutX_FMT	0	Set CLKoutX clock format		
			Field Value	**Output Format DCLKX_BYP = 0**	**Output Format DCLKX_BYP = 1**
			0 (0x00)	Powerdown	Reserved
			1 (0x01)	LVDS	Reserved
			2 (0x02)	HSDS 6 mA	Reserved
			3 (0x03)	HSDS 8 mA	Reserved
			4 (0x04)	LVPECL 1600 mV	Reserved
			5 (0x05)	LVPECL 2000 mV	Reserved
			6 (0x06)	LCPECL	Reserved
			7 (0x07)	Reserved	CML 16 mA
			8 (0x08)	Reserved	CML 24 mA
			9 (0x09)	Reserved	CML 32 mA
			10 (0x0A)	CMOS (Off/Inv)(1)	Reserved
			11 (0x0B)	CMOS (Norm/Off)(1)	Reserved
			12 (0x0C)	CMOS (Inv/Inv)(1)	Reserved
			13 (0x0D)	CMOS (Inv/Norm)(1)	Reserved
			14 (0x0E)	CMOS (Norm/Inv)(1)	Reserved
			15 (0x0F)	CMOS (Norm/Norm)(1)	Reserved

(1) Only valid for CLKout10.

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表 8-27. Registers 0x10F (CLKout2_3), 0x117 (CLKout4_5), 0x127 (CLKout8_9), 0x137 (CLKout12_13)

BIT	NAME	POR DEFAULT	DESCRIPTION		
7:4	CLKoutY_FMT	0	Set CLKoutY clock format		
			Field Value	**Output Format**	
			0 (0x00)	Powerdown	
			1 (0x01)	LVDS	
			2 (0x02)	HSDS 6 mA	
			3 (0x03)	HSDS 8 mA	
			4 (0x04)	LVPECL 1600 mV	
			5 (0x05)	LVPECL 2000 mV	
			6 (0x06)	LCPECL	
			7 (0x07)	CML 16 mA	
			8 (0x08)	CML 24 mA	
			9 (0x09)	CML 32 mA	
			10 (0x0A)	CMOS (Off/Norm)	
			11 (0x0B)	CMOS (Inv/Off)	
			12 (0x0C)	CMOS (Norm/Norm)	
			13 (0x0D)	CMOS (Norm/Inv)	
			14 (0x0E)	CMOS (Inv/Norm)	
			15 (0x0F)	CMOS (Inv/Inv)	
3:0	CLKoutX_FMT	0	Set CLKoutX clock format		
			Field Value	**Output Format DCLKX_BYP = 0**	**Output Format DCLKX_BYP = 1**
			0 (0x00)	Powerdown	Reserved
			1 (0x01)	LVDS	Reserved
			2 (0x02)	HSDS 6 mA	Reserved
			3 (0x03)	HSDS 8 mA	Reserved
			4 (0x04)	LVPECL 1600 mV	Reserved
			5 (0x05)	LVPECL 2000 mV	Reserved
			6 (0x06)	LCPECL	Reserved
			7 (0x07)	Reserved	CML 16 mA
			8 (0x08)	Reserved	CML 24 mA
			9 (0x09)	Reserved	CML 32 mA
			10 (0x0A)	CMOS (Off/Norm)(1)	Reserved
			11 (0x0B)	CMOS (Inv/Off)(1)	Reserved
			12 (0x0C)	CMOS (Norm/Norm)(1)	Reserved
			13 (0x0D)	CMOS (Norm/Inv)(1)	Reserved
			14 (0x0E)	CMOS (Inv/Norm)(1)	Reserved
			15 (0x0F)	CMOS (Inv/Inv)(1)	Reserved

(1) Only valid for CLKout8.

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8.6.2.3 SYSREF, SYNC, and Device Config

8.6.2.3.1 VCO_MUX, OSCout_MUX, OSCout_FMT

表 8-28. Register 0x138

BIT	NAME	POR DEFAULT	DESCRIPTION	
7	NA	0	Reserved	
6:5	VCO_MUX	2	Selects clock distribution path source from VCO0, VCO1, or CLKin (external VCO)	
			Field Value	**VCO Selected**
			0 (0x00)	VCO 0
			1 (0x01)	VCO 1
			2 (0x02)	Fin1 / CLKin1 (external VCO)
			3 (0x03)	Fin0
4	OSCout_MUX	0	Select the source for OSCout: 0: Buffered OSCin 1: Feedback Mux	
3:0	OSCout_FMT	4	Selects the output format of OSCout. When powered down, these pins may be used as CLKin2.	
			Field Value	**OSCout Format**
			0 (0x00)	Power down (CLKin2)
			1 (0x01)	LVDS
			2 (0x02)	Reserved
			3 (0x03)	Reserved
			4 (0x04)	LVPECL 1600 mVpp
			5 (0x05)	LVPECL 2000 mVpp
			6 (0x06)	LVCMOS (Norm / Inv)
			7 (0x07)	LVCMOS (Inv / Norm)
			8 (0x08)	LVCMOS (Norm / Norm)
			9 (0x09)	LVCMOS (Inv / Inv)
			10 (0x0A)	LVCMOS (Off / Norm)
			11 (0x0B)	LVCMOS (Off / Inv)
			12 (0x0C)	LVCMOS (Norm / Off)
			13 (0x0D)	LVCMOS (Inv / Off)
			14 (0x0E)	LVCMOS (Off / Off)

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8.6.2.3.2 SYSREF_REQ_EN, SYNC_BYPASS, SYSREF_MUX

This register sets the source for the SYSREF outputs. Refer to 図 8-3 and セクション 8.3.2.

表 8-29. Register 0x139

BIT	NAME	POR DEFAULT	DESCRIPTION	
7:6	NA	0	Reserved	
5	NA	0	Reserved	
4	SYSREF_REQ_EN	0	Enables the SYNC/SYSREF_REQ pin to force the SYSREF_MUX = 3 for continuous pulses. When using this feature enable pulser and set SYSREF_MUX = 2 (Pulser).	
3	SYNC_BYPASS	0	Bypass SYNC polarity invert and other circuitry. 0: Normal 1: SYNC signal is bypassed	
2	NA	0	Reserved	
1:0	SYSREF_MUX	0	Selects the SYSREF source.	
			Field Value	**SYSREF Source**
			0 (0x00)	Normal SYNC
			1 (0x01)	Re-clocked
			2 (0x02)	SYSREF Pulser
			3 (0x03)	SYSREF Continuous

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8.6.2.3.3 SYSREF_DIV

These registers set the value of the SYSREF output divider.

表 8-30. SYSREF_DIV[12:0]

MSB	LSB
0x13A[4:0] = SYSREF_DIV[12:8]	0x13B[7:0] = SYSREF_DIV[7:0]

表 8-31. Registers 0x13A and 0x13B

REGISTER	BIT	NAME	POR DEFAULT	DESCRIPTION	
0x13A	7:5	NA	0	Reserved	
0x13A	4:0	SYSREF_DIV[12:8]	12	Divide value for the SYSREF outputs.	
				Field Value	**Divide Value**
				0 to 7 (0x00 to 0x07)	Reserved
				8 (0x08)	8
0x13B	7:0	SYSREF_DIV[7:0]	0	9 (0x09)	9
				...	...
				8190 (0x1FFE)	8190
				8191 (0X1FFF)	8191

8.6.2.3.4 SYSREF_DDLY

These registers set the delay of the SYSREF digital delay value.

表 8-32. SYSREF Digital Delay Register Configuration, SYSREF_DDLY[12:0]

MSB	LSB
0x13C[4:0] / SYSREF_DDLY[12:8]	0x13D[7:0] / SYSREF_DDLY[7:0]

表 8-33. Registers 0X13C and 0X13D

REGISTER	BIT	NAME	POR DEFAULT	DESCRIPTION	
0x13C	7:5	NA	0	Reserved	
0x13C	4:0	SYSREF_DDLY[12:8]	0	Sets the value of the SYSREF digital delay.	
				Field Value	**Delay Value**
				0x00 to 0x07	Reserved
				8 (0x08)	8
0x13D	7:0	SYSREF_DDLY[7:0]	8	9 (0x09)	9
				...	...
				8190 (0x1FFE)	8190
				8191 (0X1FFF)	8191

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8.6.2.3.5 SYSREF_PULSE_CNT

This register sets the number of SYSREF pulses if SYSREF is not in continuous mode. See セクション 8.6.2.3.2 for further description of SYSREF's outputs.

Programming the register causes the specified number of pulses to be output if "SYSREF Pulses" is selected by SYSREF_MUX and SYSREF functionality is powered up.

表 8-34. Register 0x13E

BIT	NAME	POR DEFAULT	DESCRIPTION	
7:2	NA	0	Reserved	
1:0	SYSREF_PULSE_CNT	3	Sets the number of SYSREF pulses generated when not in continuous mode. See セクション 8.6.2.3.2 for more information on SYSREF modes.	
			Field Value	**Number of Pulses**
			0 (0x00)	1 pulse
			1 (0x01)	2 pulses
			2 (0x02)	4 pulses
			3 (0x03)	8 pulses

8.6.2.3.6 PLL2_RCLK_MUX, PLL2_NCLK_MUX, PLL1_NCLK_MUX, FB_MUX, FB_MUX_EN

This register controls the feedback feature.

表 8-35. Register 0x13F

BIT	NAME	POR DEFAULT	DESCRIPTION	
7	PLL2_RCLK_MUX	0	Selects the source for PLL2 reference. 0: OSCin 1: Currently selected CLKin.	
6	NA	0	Reserved	
5	PLL2_NCLK_MUX	0	Selects the input to the PLL2 N Divider 0: PLL2 Prescaler 1: Feedback Mux	
4:3	PLL1_NCLK_MUX	0	Selects the input to the PLL1 N Divider. 0: OSCin 1: Feedback Mux 2: PLL2 Prescaler	
2:1	FB_MUX	0	When in 0-delay mode, the feedback mux selects the clock output to be fed back into the PLL1 N Divider.	
			Field Value	**Source**
			0 (0x00)	CLKout6
			1 (0x01)	CLKout8
			2 (0x02)	SYSREF Divider
			3 (0x03)	External
0	FB_MUX_EN	0	When using 0-delay, FB_MUX_EN must be set to 1 power up the feedback mux. 0: Feedback mux powered down 1: Feedback mux enabled	

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8.6.2.3.7 PLL1_PD, VCO_LDO_PD, VCO_PD, OSCin_PD, SYSREF_GBL_PD, SYSREF_PD, SYSREF_DDLY_PD, SYSREF_PLSR_PD

This register contains power down controls for OSCin and SYSREF functions.

表 8-36. Register 0x140

BIT	NAME	POR DEFAULT	DESCRIPTION
7	PLL1_PD	1	Power down PLL1 0: Normal operation 1: Power down
6	VCO_LDO_PD	1	Power down VCO_LDO 0: Normal operation 1: Power down
5	VCO_PD	1	Power down VCO 0: Normal operation 1: Power down
4	OSCin_PD	0	Power down the OSCin port. 0: Normal operation 1: Power down
3	SYSREF_GBL_PD	0	Power down individual SYSREF outputs depending on the setting of SCLKX_Y_DIS_MODE for each SYSREF output. SYSREF_GBL_PD allows many SYSREF outputs to be controlled through a single bit. 0: Normal operation 1: Activate Power down Mode
2	SYSREF_PD	0	Power down the SYSREF circuitry and divider. If powered down, SYSREF output mode cannot be used. SYNC cannot be provided either. 0: SYSREF can be used as programmed by individual SYSREF output registers. 1: Power down
1	SYSREF_DDLY_PD	0	Power down the SYSREF digital delay circuitry. 0: Normal operation, SYSREF digital delay may be used. Must be powered up during SYNC for deterministic phase relationship with other clocks. 1: Power down
0	SYSREF_PLSR_PD	0	Powerdown the SYSREF pulse generator. 0: Normal operation 1: Powerdown

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8.6.2.3.8 DDLYdSYSREF_EN, DDLYdX_EN

This register enables dynamic digital delay for enabled device clocks and SYSREF when DDLYd_STEP_CNT is programmed.

表 8-37. Register 0x141

BIT	NAME	POR DEFAULT	DESCRIPTION	
7	DDLYd _SYSREF_EN	0	Enables dynamic digital delay on SYSREF outputs	0: Disabled 1: Enabled
6	DDLYd12_EN	0	Enables dynamic digital delay on DCLKout12	
5	DDLYd10_EN	0	Enables dynamic digital delay on DCLKout10	
4	DDLYd8_EN	0	Enables dynamic digital delay on DCLKout8	
3	DDLYd6_EN	0	Enables dynamic digital delay on DCLKout6	
2	DDLYd4_EN	0	Enables dynamic digital delay on DCLKout4	
1	DDLYd2_EN	0	Enables dynamic digital delay on DCLKout2	
0	DDLYd0_EN	0	Enables dynamic digital delay on DCLKout0	

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8.6.2.3.9 DDLYd_STEP_CNT

This register sets the number of dynamic digital delay adjustments occur. Upon programming, the dynamic digital delay adjustment begins for each clock output with dynamic digital delay enabled. Dynamic digital delay can only be started by SPI.

Other registers must be set: SYNC_MODE = 3

表 8-38. Register 0x142

BIT	NAME	POR DEFAULT	DESCRIPTION	
7:0	DDLYd_STEP_CNT	0	Sets the number of dynamic digital delay adjustments that will occur.	
			Field Value	**Dynamic Digital Delay Adjustments**
			0 (0x00)	No Adjust
			1 (0x01)	1 step
			2 (0x02)	2 steps
			3 (0x03)	3 steps
			...	...
			254 (0xFE)	254 steps
			255 (0xFF)	255 steps

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8.6.2.3.10 SYSREF_CLR, SYNC_1SHOT_EN, SYNC_POL, SYNC_EN, SYNC_PLL2_DLD, SYNC_PLL1_DLD, SYNC_MODE

This register sets general SYNC parameters such as polarization, and mode. Refer to 図 8-3 for block diagram. Refer to 表 8-2 for using SYNC_MODE for specific SYNC use cases.

表 8-39. Register 0x143

BIT	NAME	POR DEFAULT	DESCRIPTION	
7	SYSREF_CLR	0	Except during SYSREF Setup Procedure (see セクション 8.3.2), this bit should always be programmed to 0. While this bit is set, extra current is used.	
6	SYNC_1SHOT_EN	0	SYNC one shot enables edge sensitive SYNC. 0: SYNC is level sensitive and outputs will be held in SYNC as long as SYNC is asserted. 1: SYNC is edge sensitive, outputs will be SYNCed on rising edge of SYNC. This results in the clock being held in SYNC for a minimum amount of time.	
5	SYNC_POL	0	Sets the polarity of the SYNC pin. 0: Normal 1: Inverted	
4	SYNC_EN	0	Enables the SYNC functionality. 0: Disabled 1: Enabled	
3	SYNC_PLL2_DLD	0	0: Off 1: Assert SYNC until PLL2 DLD = 1	
2	SYNC_PLL1_DLD	0	0: Off 1: Assert SYNC until PLL1 DLD = 1	
1:0	SYNC_MODE	1	Sets the method of generating a SYNC event.	
			Field Value	**SYNC Generation**
			0 (0x00)	Prevent SYNC Pin, SYNC_PLL1_DLD flag, or SYNC_PLL2_DLD flag from generating a SYNC event.
			1 (0x01)	SYNC event generated from SYNC pin or if enabled the SYNC_PLL1_DLD flag or SYNC_PLL2_DLD flag.
			2 (0x02)	For use with pulser - SYNC/SYSREF pulses are generated by pulser block via SYNC Pin or if enabled SYNC_PLL1_DLD flag or SYNC_PLL2_DLD flag.
			3 (0x03)	For use with pulser - SYNC/SYSREF pulses are generated by pulser block when programming register 0x13E (SYSREF_PULSE_CNT) is written to (see セクション 8.6.2.3.5).

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8.6.2.3.11 SYNC_DISSYSREF, SYNC_DISX

SYNC_DISX will prevent a clock output from being synchronized or interrupted by a SYNC event or when outputting SYSREF.

表 8-40. Register 0x144

BIT	NAME	POR DEFAULT	DESCRIPTION
7	SYNC_DISSYSREF	0	Prevent the SYSREF clocks from becoming synchronized during a SYNC event. If SYNC_DISSYSREF is enabled it will continue to operate normally during a SYNC event.
6	SYNC_DIS12	0	Prevent the device clock output from becoming synchronized during a SYNC event or SYSREF clock. If SYNC_DIS bit for a particular output is enabled then it will continue to operate normally during a SYNC event or SYSREF clock.
5	SYNC_DIS10	0	
4	SYNC_DIS8	0	
3	SYNC_DIS6	0	
2	SYNC_DIS4	0	
1	SYNC_DIS2	0	
0	SYNC_DIS0	0	

8.6.2.3.12 PLL1R_SYNC_EN, PLL1R_SYNC_SRC, PLL2R_SYNC_EN, FIN0_DIV2_EN, FIN0_INPUT_TYPE

These bits are used when synchronizing PLL1 and PLL2 R dividers. Refer to (TBD) for more information on the process to synchronize the PLL R dividers.

表 8-41. Register 0x145

BIT	NAME	POR DEFAULT	DESCRIPTION	
7	NA	0	Reserved	
6	PLL1R_SYNC_EN	0	Enable synchronization for PLL1 R divider 0: Not enabled 1: Enabled	
5:4	PLL1R_SYNC_SRC	0	Select the source for PLL1 R divider synchronization	
			Field Value	**Definition**
			0 (0x00)	Reserved
			1 (0x01)	SYNC Pin
			2 (0x02)	CLKin0
			3 (0x03)	Reserved
3	PLL2R_SYNC_EN	0	Enable synchronization for PLL2 R divider. Synchronization for PLL2 R always comes from the SYNC pin. 0: Not enabled 1: Enabled	
2	FIN0_DIV2_EN	0	Sets the input path to use or bypass the divide-by-2. 0: Bypassed (÷1) 1: Divided (÷2)	
1:0	FIN0_INPUT_TYPE	0	Program input type to hardware interface used.	
			Field Value	**Definition**
			0 (0x00)	Differential Input
			1 (0x01)	Single Ended Input (Fin0)
			2 (0x02)	Single Ended Input (Fin0*)
			3 (0x03)	Reserved

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8.6.2.4 (0x146 - 0x149) CLKin Control

8.6.2.4.1 CLKin_SEL_PIN_EN, CLKin_SEL_PIN_POL, CLKin2_EN, CLKin1_EN, CLKin0_EN, CLKin2_TYPE, CLKin1_TYPE, CLKin0_TYPE

This register has CLKin enable and type controls. See セクション 8.3.6 for more info on how clock input selection works.

表 8-42. Register 0x146

BIT	NAME	POR DEFAULT	DESCRIPTION	
7	CLKin_SEL_PIN_EN	0	Enables pin control according to 図 8-7.	
6	CLKin_SEL_PIN_POL	0	Inverts the CLKin polarity for use in pin select mode. 0: Active High 1: Active Low	
5	CLKin2_EN	0	Enable CLKin2 to be used during auto-switching. 0: Not enabled for auto mode 1: Enabled for auto clock switching mode	
4	CLKin1_EN	1	Enable CLKin1 to be used during auto-switching. 0: Not enabled for auto mode 1: Enabled for auto clock switching mode	
3	CLKin0_EN	1	Enable CLKin0 to be used during auto-switching. 0: Not enabled for auto mode 1: Enabled for auto clock switching mode	
2	CLKin2_TYPE	0	0: Bipolar 1: MOS	There are two buffer types for CLKin0, 1, and 2: bipolar and CMOS. Bipolar is recommended for differential inputs like LVDS or LVPECL. CMOS is recommended for DC-coupled single ended inputs. When using bipolar, CLKinX and CLKinX* must be AC-coupled. When using CMOS, CLKinX and CLKinX* may be AC or DC-coupled if the input signal is differential. If the input signal is single-ended the used input may be either AC or DC-coupled and the unused input must AC grounded.
1	CLKin1_TYPE	0		
0	CLKin0_TYPE	0		

8.6.2.4.2 CLKin_SEL_AUTO_REVERT_EN, CLKin_SEL_AUTO_EN, CLKin_SEL_MANUAL, CLKin1_DEMUX, CLKin0_DEMUX

表 8-43. Register 0x147

BIT	NAME	POR DEFAULT	DESCRIPTION	
7	CLKin_SEL_ AUTO_REVERT_EN	0	When in auto clock switching mode. If active clock is detected on higher priority clock, the clock input is immediately switched. Highest priority input is lowest numbered active clock input.	
6	CLKin_SEL_AUTO_EN	0	Enables pin control according to 図 8-7.	
5:4	CLKin_SEL_MANUAL	1	Selects the clock input when in manual mode according to 図 8-7.	
			Field Value	**Definition**
			0 (0x00)	CLKin0
			1 (0x01)	CLKin1
			2 (0x02)	CLKin2
			3 (0x03)	Holdover

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表 8-43. Register 0x147 (continued)

BIT	NAME	POR DEFAULT	DESCRIPTION	
3:2	CLKin1_DEMUX	0	Selects where the output of the CLKin1 buffer is directed.	
			Field Value	**CLKin1 Destination**
			0 (0x00)	Fin
			1 (0x01)	Feedback Mux (0-delay mode)
			2 (0x02)	PLL1
			3 (0x03)	Off
1:0	CLKin0_DEMUX	3	Selects where the output of the CLKin0 buffer is directed.	
			Field Value	**CLKin0 Destination**
			0 (0x00)	SYSREF Mux
			1 (0x01)	Reserved
			2 (0x02)	PLL1
			3 (0x03)	Off

8.6.2.4.3 CLKin_SEL0_MUX, CLKin_SEL0_TYPE

This register has CLKin_SEL0 controls.

表 8-44. Register 0x148

BIT	NAME	POR DEFAULT	DESCRIPTION		
7:6	NA	0	Reserved		
5:3	CLKin_SEL0_MUX	0	This set the output value of the CLKin_SEL0 pin. This register only applies if CLKin_SEL0_TYPE is set to an output mode		
			Field Value	**Output Format**	
			0 (0x00)	Logic Low	
			1 (0x01)	CLKin0 LOS	
			2 (0x02)	CLKin0 Selected	
			3 (0x03)	DAC Locked	
			4 (0x04)	DAC Low	
			5 (0x05)	DAC High	
			6 (0x06)	SPI Readback	
			7 (0x07)	Reserved	
2:0	CLKin_SEL0_TYPE	2	This sets the IO type of the CLKin_SEL0 pin.		
			Field Value	**Configuration**	**Function**
			0 (0x00)	Input	Input mode, see セクション 8.3.6.2 for description of input mode.
			1 (0x01)	Input with pullup resistor	
			2 (0x02)	Input with pulldown resistor	
			3 (0x03)	Output (push-pull)	Output modes; the CLKin_SEL0_MUX register for description of outputs.
			4 (0x04)	Output inverted (push-pull)	
			5 (0x05)	Reserved	
			6 (0x06)	Output (open-drain)	

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8.6.2.4.4 SDIO_RDBK_TYPE, CLKin_SEL1_MUX, CLKin_SEL1_TYPE

This register has CLKin_SEL1 controls and register readback SDIO pin type.

表 8-45. Register 0x149

BIT	NAME	POR DEFAULT	DESCRIPTION		
7	NA	0	Reserved		
6	SDIO_RDBK_TYPE	1	Sets the SDIO pin to open drain when during SPI readback in 3 wire mode. 0: Output, push-pull 1: Output, open drain.		
5:3	CLKin_SEL1_MUX	0	This set the output value of the CLKin_SEL1 pin. This register only applies if CLKin_SEL1_TYPE is set to an output mode.		
			Field Value	**Output Format**	
			0 (0x00)	Logic Low	
			1 (0x01)	CLKin1 LOS	
			2 (0x02)	CLKin1 Selected	
			3 (0x03)	DAC Locked	
			4 (0x04)	DAC Low	
			5 (0x05)	DAC High	
			6 (0x06)	SPI Readback	
			7 (0x07)	Reserved	
2:0	CLKin_SEL1_TYPE	2	This sets the IO type of the CLKin_SEL1 pin.		
			Field Value	**Configuration**	**Function**
			0 (0x00)	Input	Input mode, see セクション 8.3.6.2 for description of input mode.
			1 (0x01)	Input with pullup resistor	
			2 (0x02)	Input with pulldown resistor	
			3 (0x03)	Output (push-pull)	Output modes; see the CLKin_SEL1_MUX register for description of outputs.
			4 (0x04)	Output inverted (push-pull)	
			5 (0x05)	Reserved	
			6 (0x06)	Output (open-drain)	

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8.6.2.5 RESET_MUX, RESET_TYPE

This register contains control of the RESET pin.

表 8-46. Register 0x14A

BIT	NAME	POR DEFAULT	DESCRIPTION		
7:6	NA	0	Reserved		
5:3	RESET_MUX	0	This sets the output value of the RESET pin. This register only applies if RESET_TYPE is set to an output mode.		
			Field Value	**Output Format**	
			0 (0x00)	Logic Low	
			1 (0x01)	Reserved	
			2 (0x02)	CLKin2 Selected	
			3 (0x03)	DAC Locked	
			4 (0x04)	DAC Low	
			5 (0x05)	DAC High	
			6 (0x06)	SPI Readback	
2:0	RESET_TYPE	2	This sets the IO type of the RESET pin.		
			Field Value	**Configuration**	**Function**
			0 (0x00)	Input	Reset Mode Reset pin high = Reset
			1 (0x01)	Input with pullup resistor	
			2 (0x02)	Input with pulldown resistor	
			3 (0x03)	Output (push-pull)	Output modes; see the RESET_MUX register for description of outputs.
			4 (0x04)	Output inverted (push-pull)	
			5 (0x05)	Reserved	
			6 (0x06)	Output (open-drain)	

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8.6.2.6 (0x14B - 0x152) Holdover

8.6.2.6.1 LOS_TIMEOUT, LOS_EN, TRACK_EN, HOLDOVER_FORCE, MAN_DAC_EN, MAN_DAC[9:8]

This register contains the holdover functions.

表 8-47. Register 0x14B

BIT	NAME	POR DEFAULT	DESCRIPTION	
7:6	LOS_TIMEOUT	0	This controls the amount of time in which no activity on a CLKin forces a clock switch event.	
			Field Value	**Timeout**
			0 (0x00)	5 MHz typical
			1 (0x01)	25 MHz typical
			2 (0x02)	100 MHz typical
			3 (0x03)	200 MHz typical
5	LOS_EN	0	Enables the LOS (Loss-of-Signal) timeout control. Valid for MOS clock inputs. 0: Disabled 1: Enabled	
4	TRACK_EN	0	Enable the DAC to track the PLL1 tuning voltage, optionally for use in holdover mode. After device reset, tracking starts at DAC code = 512. Tracking can be used to monitor PLL1 voltage in any mode. 0: Disabled 1: Enabled, will only track when PLL1 is locked.	
3	HOLDOVER _FORCE	0	This bit forces holdover mode. When holdover mode is forced, if MAN_DAC_EN = 1, then the DAC will set the programmed MAN_DAC value. Otherwise the tracked DAC value will set the DAC voltage. 0: Disabled 1: Enabled.	
2	MAN_DAC_EN	1	This bit enables the manual DAC mode. 0: Automatic 1: Manual	
1:0	MAN_DAC[9:8]	2	See セクション 8.6.2.6.2 for more information on the MAN_DAC settings.	

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8.6.2.6.2 MAN_DAC

These registers set the value of the DAC in holdover mode when used manually.

表 8-48. MAN_DAC[9:0]

MSB	LSB
0x14B[1:0]	0x14C[7:0]

REGISTER	BIT	NAME	POR DEFAULT	DESCRIPTION	
0x14B	7:2			See セクション 8.6.2.6.1 for information on these bits.	
0x14B	1:0	MAN_DAC[9:8]	2	Sets the value of the manual DAC when in manual DAC mode.	
				Field Value	**DAC Value**
				0 (0x00)	0
				1 (0x01)	1
0x14C	7:0	MAN_DAC[7:0]	0	2 (0x02)	2
				...	...
				1022 (0x3FE)	1022
				1023 (0x3FF)	1023

8.6.2.6.3 DAC_TRIP_LOW

This register contains the high value at which holdover mode is entered.

表 8-49. Register 0x14D

BIT	NAME	POR DEFAULT	DESCRIPTION	
7:6	NA	0	Reserved	
5:0	DAC_TRIP_LOW	0	Voltage from GND at which holdover is entered if HOLDOVER_VTUNE_DET is enabled.	
			Field Value	**DAC Trip Value**
			0 (0x00)	1 x Vcc / 64
			1 (0x01)	2 x Vcc / 64
			2 (0x02)	3 x Vcc / 64
			3 (0x03)	4 x Vcc / 64
			...	...
			61 (0x17)	62 x Vcc / 64
			62 (0x18)	63 x Vcc / 64
			63 (0x19)	64 x Vcc / 64

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8.6.2.6.4 DAC_CLK_MULT, DAC_TRIP_HIGH

This register contains the multiplier for the DAC clock counter and the low value at which holdover mode is entered.

表 8-50. Register 0x14E

BIT	NAME	POR DEFAULT	DESCRIPTION	
7:6	DAC_CLK_MULT	0	This is the multiplier for the DAC_CLK_CNTR which sets the rate at which the DAC value is tracked.	
			Field Value	**DAC Multiplier Value**
			0 (0x00)	4
			1 (0x01)	64
			2 (0x02)	1024
			3 (0x03)	16384
5:0	DAC_TRIP_HIGH	0	Voltage from Vcc at which holdover is entered if HOLDOVER_VTUNE_DET is enabled.	
			Field Value	**DAC Trip Value**
			0 (0x00)	1 x Vcc / 64
			1 (0x01)	2 x Vcc / 64
			2 (0x02)	3 x Vcc / 64
			3 (0x03)	4 x Vcc / 64
			...	...
			61 (0x17)	62 x Vcc / 64
			62 (0x18)	63 x Vcc / 64
			63 (0x19)	64 x Vcc / 64

8.6.2.6.5 DAC_CLK_CNTR

This register contains the value of the DAC when in tracked mode.

表 8-51. Register 0x14F

BIT	NAME	POR DEFAULT	DESCRIPTION	
7:0	DAC_CLK_CNTR	127	This with DAC_CLK_MULT set the rate at which the DAC is updated. The update rate is = DAC_CLK_MULT * DAC_CLK_CNTR / PLL1 PDF	
			Field Value	**DAC Value**
			0 (0x00)	0
			1 (0x01)	1
			2 (0x02)	2
			3 (0x03)	3
			...	...
			253 (0xFD)	253
			254 (0xFE)	254
			255 (0xFF)	255

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8.6.2.6.6 CLKin_OVERRIDE, HOLDOVER_EXIT_MODE, HOLDOVER_PLL1_DET, LOS_EXTERNAL_INPUT, HOLDOVER_VTUNE_DET, CLKin_SWITCH_CP_TRI, HOLDOVER_EN

This register has controls for enabling clock in switch events.

表 8-52. Register 0x150

BIT	NAME	POR DEFAULT	DESCRIPTION
7	NA	0	Reserved
6	CLKin _OVERRIDE	0	When manual clock select is enabled, then CLKin_SEL_MANUAL = 0/1/2 selects a manual clock input. CLKin_OVERRIDE = 1 will force that clock input. CLKin_OVERRIDE = 1 is used with clock distribution mode for best performance. 0: Normal, no override. 1: Force select of only CLKin0/1/2 as specified by CLKin_SEL_MANUAL in manual mode. Dynamic digital delay will not operate.
5	HOLDOVER_ EXIT_MODE	0	0: Exit based on LOS status. If clock is active by LOS, then begin exit. 1: Exit based on PLL1 DLD. When the PLL1 phase detector confirming valid clock.
4	HOLDOVER _PLL1_DET	0	This enables the HOLDOVER when PLL1 lock detect signal transitions from high to low. 0: PLL1 DLD does not cause a clock switch event 1: PLL1 DLD causes a clock switch event
3	LOS_EXTERNAL_INPUT	0	Use external signals for LOS status instead of internal LOS circuitry. CLKin_SEL0 pin is used for CLKin0 LOS, CLKin_SEL1 pin is used for CLKin1 LOS, and Status_LD1 is used for CLKin2 LOS. For any of these pins to be valid, the corresponding _TYPE register must be programmed as an input. 0: Disabled 1: Enabled
2	HOLDOVER_ VTUNE_DET	0	Enables the DAC Vtune rail detector. When the DAC achieves a specified Vtune, if this bit is enabled, the current clock input is considered invalid and an input clock switch event is generated. 0: Disabled 1: Enabled
1	CLKin_SWITCH_CP_TRI	0	Enable clock switching with tri-stated charge pump. 0: Not enabled. 1: PLL1 charge pump tri-states during clock switching.
0	HOLDOVER_EN	0	Sets whether holdover mode is active or not. 0: Disabled 1: Enabled

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8.6.2.6.7 HOLDOVER_DLD_CNT

表 8-53. HOLDOVER_DLD_CNT[13:0]

MSB	LSB
0x151[5:0] / HOLDOVER_DLD_CNT[13:8]	0x152[7:0] / HOLDOVER_DLD_CNT[7:0]

This register has the number of valid clocks of PLL1 PDF before holdover is exited.

表 8-54. Registers 0x151 and 0x152

REGISTER	BIT	NAME	POR DEFAULT	DESCRIPTION	
0x151	7:6	NA	0	Reserved	
0x151	5:0	HOLDOVER _DLD_CNT[13:8]	2	The number of valid clocks of PLL1 PDF before holdover mode is exited.	
				Field Value	**Count Value**
				0 (0x00)	0
				1 (0x01)	1
0x152	7:0	HOLDOVER _DLD_CNT[7:0]	0	2 (0x02)	2
				...	...
				16382 (0x3FFE)	16382
				16383 (0x3FFF)	16383

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8.6.2.7 (0x153 - 0x15F) PLL1 Configuration

8.6.2.7.1 CLKin0_R

表 8-55. CLKin0_R[13:0]

MSB	LSB
0x153[5:0] / CLKin0_R[13:8]	0x154[7:0] / CLKin0_R[7:0]

These registers contain the value of the CLKin0 divider.

表 8-56. Registers 0x153 and 0x154

REGISTER	BIT	NAME	POR DEFAULT	DESCRIPTION	
0x153	7:6	NA	0	Reserved	
0x153	5:0	CLKin0_R[13:8]	0	The value of PLL1 N counter when CLKin0 is selected.	
				Field Value	**Divide Value**
				0 (0x00)	Reserved
				1 (0x01)	1
0x154	7:0	CLKin0_R[7:0]	120	2 (0x02)	2
				...	...
				16382 (0x3FFE)	16382
				16383 (0x3FFF)	16383

8.6.2.7.2 CLKin1_R

表 8-57. CLKin1_R[13:0]

MSB	LSB
0x155[5:0] / CLKin1_R[13:8]	0x156[7:0] / CLKin1_R[7:0]

These registers contain the value of the CLKin1 R divider.

表 8-58. Registers 0x155 and 0x156

REGISTER	BIT	NAME	POR DEFAULT	DESCRIPTION	
0x155	7:6	NA	0	Reserved	
0x155	5:0	CLKin1_R[13:8]	0	The value of PLL1 N counter when CLKin1 is selected.	
				Field Value	**Divide Value**
				0 (0x00)	Reserved
				1 (0x01)	1
0x156	7:0	CLKin1_R[7:0]	150	2 (0x02)	2
				...	...
				16382 (0x3FFE)	16382
				16383 (0x3FFF)	16383

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8.6.2.7.3 CLKin2_R

表 8-59. CLKin2_R[13:0]

MSB	LSB
0x157[5:0] / CLKin2_R[13:8]	0x158[7:0] / CLKin2_R[7:0]

表 8-60. Registers 0x157 and 0x158

REGISTER	BIT	NAME	POR DEFAULT	DESCRIPTION	
0x157	7:6	NA	0	Reserved	
0x157	5:0	CLKin2_R[13:8]	0	The value of PLL1 N counter when CLKin2 is selected.	
				Field Value	**Divide Value**
				0 (0x00)	Reserved
				1 (0x01)	1
0x158	7:0	CLKin2_R[7:0]	150	2 (0x02)	2
				...	...
				16382 (0x3FFE)	16382
				16383 (0x3FFF)	16383

8.6.2.7.4 PLL1_N

表 8-61. PLL1_N[13:0]

MSB	LSB
0x159[5:0] / PLL1_N[13:8]	0x15A[7:0] / PLL1_N[7:0]

These registers contain the N divider value for PLL1.

表 8-62. Registers 0x159 and 0x15A

REGISTER	BIT	NAME	POR DEFAULT	DESCRIPTION	
0x159	7:6	NA	0	Reserved	
0x159	5:0	PLL1_N[13:8]	0	The value of PLL1 N counter.	
				Field Value	**Divide Value**
				0 (0x00)	Not Valid
				1 (0x01)	1
0x15A	7:0	PLL1_N[7:0]	120	2 (0x02)	2
				...	...
				4,095 (0xFFF)	4,095

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8.6.2.7.5 PLL1_WND_SIZE, PLL1_CP_TRI, PLL1_CP_POL, PLL1_CP_GAIN

This register controls the PLL1 phase detector.

表 8-63. Register 0x15B

BIT	NAME	POR DEFAULT	DESCRIPTION	
7:6	PLL1_WND_SIZE	3	PLL1_WND_SIZE sets the window size used for digital lock detect for PLL1. If the phase error between the reference and feedback of PLL1 is less than specified time, then the PLL1 lock counter increments.	
			Field Value	**Definition**
			0 (0x00)	4 ns
			1 (0x01)	9 ns
			2 (0x02)	19 ns
			3 (0x03)	43 ns
5	PLL1_CP_TRI	0	This bit allows for the PLL1 charge pump output pin, CPout1, to be placed into TRI-STATE. 0: PLL1 CPout1 is active 1: PLL1 CPout1 is at TRI-STATE	
4	PLL1_CP_POL	1	PLL1_CP_POL sets the charge pump polarity for PLL1. Many VCXOs use positive slope. A positive slope VCXO increases output frequency with increasing voltage. A negative slope VCXO decreases output frequency with increasing voltage. 0: Negative Slope VCO/VCXO 1: Positive Slope VCO/VCXO	
3:0	PLL1_CP_GAIN	4	This bit programs the PLL1 charge pump output current level.	
			Field Value	**Gain**
			0 (0x00)	50 µA
			1 (0x01)	150 µA
			2 (0x02)	250 µA
			3 (0x03)	350 µA
			4 (0x04)	450 µA
			...	...
			14 (0x0E)	1450 µA
			15 (0x0F)	1550 µA

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8.6.2.7.6 PLL1_DLD_CNT

表 8-64. PLL1_DLD_CNT[13:0]

MSB	LSB
0x15C[5:0] / PLL1_DLD_CNT[13:8]	0x15D[7:0] / PLL1_DLD_CNT[7:0]

This register contains the value of the PLL1 DLD counter.

表 8-65. Registers 0x15C and 0x15D

REGISTER	BIT	NAME	POR DEFAULT	DESCRIPTION	
0x15C	7:6	NA	0	Reserved	
0x15C	5:0	PLL1_DLD _CNT[13:8]	32	The reference and feedback of PLL1 must be within the window of phase error as specified by PLL1_WND_SIZE for this many phase detector cycles before PLL1 digital lock detect is asserted.	
				Field Value	**Delay Value**
				0 (0x00)	Reserved
				1 (0x01)	1
0x15D	7:0	PLL1_DLD _CNT[7:0]	0	2 (0x02)	2
				3 (0x03)	3
				...	...
				16,382 (0x3FFE)	16,382
				16,383 (0x3FFF)	16,383

8.6.2.7.7 HOLDOVER_EXIT_NADJ

表 8-66. Register 0x15E

BIT	NAME	POR DEFAULT	DESCRIPTION
7:5	NA	0	Reserved
4:0	HOLDOVER_EXIT_NADJ	30	When holdover exists, PLL1 R counter and PLL1 N counter are reset. HOLDOVER_EXIT_NADJ is a 2s complement number which provides a relative timing offset between PLL1 R and PLL1 N divider.

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8.6.2.7.8 PLL1_LD_MUX, PLL1_LD_TYPE

This register configures the PLL1 LD pin.

表 8-67. Register 0x15F

BIT	NAME	POR DEFAULT	DESCRIPTION	
7:3	PLL1_LD_MUX	1	This sets the output value of the Status_LD1 pin.	
			Field Value	**MUX Value**
			0 (0x00)	Logic Low
			1 (0x01)	PLL1 DLD
			2 (0x02)	PLL2 DLD
			3 (0x03)	PLL1 & PLL2 DLD
			4 (0x04)	Holdover Status
			5 (0x05)	DAC Locked
			6 (0x06)	Reserved
			7 (0x07)	SPI Readback
			8 (0x08)	DAC Rail
			9 (0x09)	DAC Low
			10 (0x0A)	DAC High
			11 (0x0B)	PLL1_N
			12 (0x0C)	PLL1_N/2
			13 (0x0D)	PLL2_N
			14 (0x0E)	PLL2_N/2
			15 (0x0F)	PLL1_R
			16 (0x10)	PLL1_R/2
			17 (0x11)	PLL2_R(1)
			18 (0x12)	PLL2_R/2(1)
2:0	PLL1_LD_TYPE	6	Sets the IO type of the Status_LD1 pin.	
			Field Value	**TYPE**
			0 (0x00)	Input for External CLKin2 LOS
			1 (0x01)	Input for External CLKin2 LOS (pullup)
			2 (0x02)	Input for External CLKin2 LOS (pulldwn)
			3 (0x03)	Output (push-pull)
			4 (0x04)	Output inverted (push-pull)
			5 (0x05)	Reserved
			6 (0x06)	Output (open-drain)

(1) Only valid when PLL2_LD_MUX is not set to 2 (PLL2_DLD) or 3 (PLL1 & PLL2 DLD).

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8.6.2.8 (0x160 - 0x16E) PLL2 Configuration

8.6.2.8.1 PLL2_R

表 8-68. PLL2_R[11:0]

MSB	LSB
0x160[3:0] / PLL2_R[11:8]	0x161[7:0] / PLL2_R[7:0]

This register contains the value of the PLL2 R divider.

表 8-69. Registers 0x160 and 0x161

REGISTER	BIT	NAME	POR DEFAULT	DESCRIPTION	
0x160	7:4	NA	0	Reserved	
0x160	3:0	PLL2_R[11:8]	0	Valid values for the PLL2 R divider.	
				Field Value	**Divide Value**
				0 (0x00)	Not Valid
				1 (0x01)	1
0x161	7:0	PLL2_R[7:0]	2	2 (0x02)	2
				3 (0x03)	3
				...	...
				4,094 (0xFFE)	4,094
				4,095 (0xFFF)	4,095

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8.6.2.8.2 PLL2_P, OSCin_FREQ, PLL2_REF_2X_EN

This register sets other PLL2 functions.

表 8-70. Register 0x162

BIT	NAME	POR DEFAULT	DESCRIPTION	
7:5	PLL2_P	2	The PLL2 N Prescaler divides the output of the VCO as selected by Mode_MUX1 and is connected to the PLL2 N divider.	
			Field Value	**Value**
			0 (0x00)	8
			1 (0x01)	2
			2 (0x02)	2
			3 (0x03)	3
			4 (0x04)	4
			5 (0x05)	5
			6 (0x06)	6
			7 (0x07)	7
4:2	OSCin_FREQ	3	The frequency of the PLL2 reference input to the PLL2 Phase Detector (OSCin/OSCin* port) must be programmed in order to support proper operation of the frequency calibration routine which locks the internal VCO to the target frequency.	
			Field Value	**OSCin Frequency**
			0 (0x00)	0 to 63 MHz
			1 (0x01)	>63 MHz to 127 MHz
			2 (0x02)	>127 MHz to 255 MHz
			3 (0x03)	Reserved
			4 (0x04)	>255 MHz to 500 MHz
			5 (0x05) to 7(0x07)	Reserved
1	NA	0	Reserved	
0	PLL2_REF_2X_EN	1	Enabling the PLL2 reference frequency doubler allows for higher phase detector frequencies on PLL2 than would normally be allowed with the given VCXO frequency. Higher phase detector frequencies reduces the PLL2 N values which makes the design of wider loop bandwidth filters possible. 0: Doubler Disabled 1: Doubler Enabled	

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8.6.2.8.3 PLL2_N_CAL

PLL2_N_CAL[17:0]

PLL2 never uses 0-delay during frequency calibration. These registers contain the value of the PLL2 N divider used with PLL2 pre-scaler during calibration for cascaded 0-delay mode. Once calibration is complete, PLL2 will use PLL2_N value. Cascaded 0-delay mode occurs when PLL2_NCLK_MUX = 1.

表 8-71. PLL2_N_CAL[17:0]

MSB	—	LSB
0x163[1:0] / PLL2_N_CAL[17:16]	0x164[7:0] / PLL2_N_CAL[15:8]	0x165[7:0] / PLL2_N_CAL[7:0]

表 8-72. Registers 0x163, 0x164, and 0x165

REGISTER	BIT	NAME	POR DEFAULT	DESCRIPTION	
0x163	7:2	NA	0	Reserved	
0x163	1:0	PLL2_N _CAL[17:16]	0	**Field Value**	**Divide Value**
				0 (0x00)	Not Valid
0x164	7:0	PLL2_N_CAL[15:8]	0	1 (0x01)	1
				2 (0x02)	2
0x165	7:0	PLL2_N_CAL[7:0]	12	...	...
				262,143 (0x3FFFF)	262,143

8.6.2.8.4 PLL2_N

This register disables frequency calibration and sets the PLL2 N divider value. Programming register 0x168 starts a VCO calibration routine if PLL2_FCAL_DIS = 0.

表 8-73. PLL2_N[17:0]

MSB	—	LSB
0x166[1:0] / PLL2_N[17:16]	0x167[7:0] / PLL2_N[15:8]	0x168[7:0] / PLL2_N[7:0]

表 8-74. Registers 0x166, 0x167, and 0x168

REGISTER	BIT	NAME	POR DEFAULT	DESCRIPTION	
0x166	7:3	NA	0	Reserved	
0x166	1:0	PLL2_N[17:16]	0	**Field Value**	**Divide Value**
				0 (0x00)	Not Valid
0x167	7:0	PLL2_N[15:8]	0	1 (0x01)	1
				2 (0x02)	2
0x168	7:0	PLL2_N[7:0]	12	...	...
				262,143 (0x3FFFF)	262,143

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8.6.2.8.5 PLL2_WND_SIZE, PLL2_CP_GAIN, PLL2_CP_POL, PLL2_CP_TRI

This register controls the PLL2 phase detector.

表 8-75. Register 0x169

BIT	NAME	POR DEFAULT	DESCRIPTION
7	NA	0	Reserved
6:5	PLL2_WND_SIZE	2	PLL2_WND_SIZE sets the window size used for digital lock detect for PLL2. If the phase error between the reference and feedback of PLL2 is less than specified time, then the PLL2 lock counter increments. **Field Value** / **Maximum Phase Detector Frequency / Window Size** 0 (0x00) / Reserved 1 (0x01) / 320 MHz / 1 ns 2 (0x02) / 240 MHz / 1.8 ns 3 (0x03) / 160 MHz / 2.6 ns
4:3	PLL2_CP_GAIN	3	This bit programs the PLL2 charge pump output current level. The table below also illustrates the impact of the PLL2 TRISTATE bit in conjunction with PLL2_CP_GAIN. **Field Value** / **Definition** 0 (0x00) / Reserved 1 (0x01) / Reserved 2 (0x02) / 1600 µA 3 (0x03) / 3200 µA
2	PLL2_CP_POL	0	PLL2_CP_POL sets the charge pump polarity for PLL2. The internal VCO requires the negative charge pump polarity to be selected. Many VCOs use positive slope. A positive slope VCO increases output frequency with increasing voltage. A negative slope VCO decreases output frequency with increasing voltage. **Field Value** / **Description** 0 / Negative Slope VCO/VCXO 1 / Positive Slope VCO/VCXO
1	PLL2_CP_TRI	0	PLL2_CP_TRI TRI-STATEs the output of the PLL2 charge pump. 0: Disabled 1: TRI-STATE
0	PLL2_DLD_EN	0	PLL2 DLD circuitry is enabled when the PLL2 DLD is used to provide an output to a lock detect status pin. PLL2_DLD_EN allows enabling the PLL2 DLD circuitry without needing to provide PLL2 DLD to a status pin. This enables PLL2 DLD status to be read back using SPI while allowing the Status pins to be used for other purposes. 0: PLL2 DLD circuitry is on only of PLL2 DLD or PLL1 + PLL2 DLD signal is output from a Status_LD_MUX. 1: PLL2 DLD circuitry is forced on.

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8.6.2.8.6 PLL2_DLD_CNT

表 8-76. PLL2_DLD_CNT[13:0]

MSB	LSB
0x16A[5:0] / PLL2_DLD_CNT[13:8]	0x16B[7:0] / PLL2_DLD_CNT[7:0]

This register has the value of the PLL2 DLD counter.

表 8-77. Registers 0x16A and 0x16B

REGISTER	BIT	NAME	POR DEFAULT	DESCRIPTION	
0x16A	7	NA	0	Reserved	
0x16A	5:0	PLL2_DLD _CNT[13:8]	32	The reference and feedback of PLL2 must be within the window of phase error as specified by PLL2_WND_SIZE for PLL2_DLD_CNT cycles before PLL2 digital lock detect is asserted.	
				Field Value	**Divide Value**
				0 (0x00)	Not Valid
				1 (0x01)	1
0x16B	7:0	PLL2_DLD_CNT	0	2 (0x02)	2
				3 (0x03)	3
				...	...
				16,382 (0x3FFE)	16,382
				16,383 (0x3FFF)	16,383

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8.6.2.8.7 PLL2_LD_MUX, PLL2_LD_TYPE

This register sets the output value of the Status_LD2 pin.

表 8-78. Register 0x16E

BIT	NAME	POR DEFAULT	DESCRIPTION	
7:3	PLL2_LD_MUX	0	This sets the output value of the Status_LD2 pin.	
			Field Value	**MUX Value**
			0 (0x00)	Logic Low
			1 (0x01)	PLL1 DLD
			2 (0x02)	PLL2 DLD
			3 (0x03)	PLL1 & PLL2 DLD
			4 (0x04)	Holdover Status
			5 (0x05)	DAC Locked
			6 (0x06)	Reserved
			7 (0x07)	SPI Readback
			8 (0x08)	DAC Rail
			9 (0x09)	DAC Low
			10 (0x0A)	DAC High
			11 (0x0B)	PLL1_N
			12 (0x0C)	PLL1_N/2
			13 (0x0D)	PLL2_N
			14 (0x0E)	PLL2_N/2
			15 (0x0F)	PLL1_R
			16 (0x10)	PLL1_R/2
			17 (0x11)	PLL2_R(1)
			18 (0x12)	PLL2_R/2(1)
2:0	PLL2_LD_TYPE	6	Sets the IO type of the Status_LD2 pin.	
			Field Value	**TYPE**
			0 (0x00)	Reserved
			1 (0x01)	Reserved
			2 (0x02)	Reserved
			3 (0x03)	Output (push-pull)
			4 (0x04)	Output inverted (push-pull)
			5 (0x05)	Reserved
			6 (0x06)	Output (open drain)

(1) Only valid when PLL1_LD_MUX is not set to 2 (PLL2_DLD) or 3 (PLL1 & PLL2 DLD).

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8.6.2.9 (0x16F - 0x555) Misc Registers

8.6.2.9.1 PLL2_PRE_PD, PLL2_PD, FIN0_PD

表 8-79. Register 0x173

BIT	NAME	POR DEFAULT	DESCRIPTION
7	N/A	0	Reserved
6	PLL2_PRE_PD	1	Powerdown PLL2 prescaler 0: Normal Operation 1: Powerdown
5	PLL2_PD	1	Powerdown PLL2 0: Normal Operation 1: Powerdown
4	FIN0_PD	1	Powerdown Fin0 0: Normal Operation 1: Powerdown
3:0	N/A	0	Reserved

8.6.2.9.2 PLL1R_RST

Refer to セクション 8.3.1.1 for more information on synchronizing PLL1 R divider.

表 8-80. Register 0x177

BIT	NAME	POR DEFAULT	DESCRIPTION
7:6	NA	0	Reserved
5	PLL1R_RST	0	When set, PLL1 R divider will be held in reset. PLL1 will never lock with PLL1R_RST = 1. This bit is used in when synchronizing the PLL1 R divider. 0: PLL1 R divider normal operation. 1: PLL1 R divider held in reset.
4:0	NA	0	Reserved

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8.6.2.9.3 CLR_PLL1_LD_LOST, CLR_PLL2_LD_LOST

表 8-81. Register 0x182

BIT	NAME	POR DEFAULT	DESCRIPTION
7:2	NA	0	Reserved
1	CLR_PLL1_LD_LOST	0	To reset RB_PLL1_LD_LOST, write CLR_PLL1_LD_LOST with 1 and then 0. 0: RB_PLL1_LD_LOST will be set on next falling PLL1 DLD edge. 1: RB_PLL1_LD_LOST is held clear (0). User must clear this bit to allow RB_PLL1_LD_LOST to become set again.
0	CLR_PLL2_LD_LOST	0	To reset RB_PLL2_LD_LOST, write CLR_PLL2_LD_LOST with 1 and then 0. 0: RB_PLL2_LD_LOST will be set on next falling PLL2 DLD edge. 1: RB_PLL2_LD_LOST is held clear (0). User must clear this bit to allow RB_PLL2_LD_LOST to become set again.

8.6.2.9.4 RB_PLL1_LD_LOST, RB_PLL1_LD, RB_PLL2_LD_LOST, RB_PLL2_LD

For PLL2 DLD read back to be valid, either PLL2 DLD or PLL1 + PLL2 DLD signal must be output from the status pins, or PLL2_DLD_EN bit must be set = 1.

表 8-82. Register 0x183

BIT	NAME	POR DEFAULT	DESCRIPTION
7:4	N/A	0	Reserved
3	RB_PLL1_LD_LOST	0	This is set when PLL1 DLD edge falls. Does not set if cleared while PLL1 DLD is low.
2	RB_PLL1_LD	0	Read back 0: PLL1 DLD is low. Read back 1: PLL1 DLD is high.
1	RB_PLL2_LD_LOST	0	This is set when PLL2 DLD edge falls. Does not set if cleared while PLL2 DLD is low.
0	RB_PLL2_LD	0	PLL1_LD_MUX or PLL2_LD_MUX must select setting 2 (PLL2 DLD) for valid reading of this bit. Read back 0: PLL2 DLD is low. Read back 1: PLL2 DLD is high.

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8.6.2.9.5 RB_DAC_VALUE (MSB), RB_CLKinX_SEL, RB_CLKinX_LOS

This register provides read back access to CLKinX selection indicator and CLKinX LOS indicator. The 2 MSBs are shared with the RB_DAC_VALUE. See RB_DAC_VALUE section.

表 8-83. Register 0x184

BIT	NAME	POR DEFAULT	DESCRIPTION
7:6	RB_DAC_VALUE[9:8]		See RB_DAC_VALUE section.
5	RB_CLKin2_SEL		Read back 0: CLKin2 is not selected for input to PLL1. Read back 1: CLKin2 is selected for input to PLL1.
4	RB_CLKin1_SEL		Read back 0: CLKin1 is not selected for input to PLL1. Read back 1: CLKin1 is selected for input to PLL1.
3	RB_CLKin0_SEL		Read back 0: CLKin0 is not selected for input to PLL1. Read back 1: CLKin0 is selected for input to PLL1.
2	N/A		
1	RB_CLKin1_LOS		Read back 1: CLKin1 LOS is active. Read back 0: CLKin1 LOS is not active.
0	RB_CLKin0_LOS		Read back 1: CLKin0 LOS is active. Read back 0: CLKin0 LOS is not active.

8.6.2.9.6 RB_DAC_VALUE

Contains the value of the DAC for user readback.

表 8-84. RB_DAC_VALUE[9:0]

MSB	LSB
0x184 [7:6] / RB_DAC_VALUE[9:8]	0x185 [7:0] / RB_DAC_VALUE[7:0]

表 8-85. Registers 0x184 and 0x185

REGISTER	BIT	NAME	POR DEFAULT	
0x184	7:6	RB_DAC_ VALUE[9:8]	2	DAC value is 512 on power on reset, if PLL1 locks upon power-up the DAC value will change.
0x185	7:0	RB_DAC_ VALUE[7:0]	0	

8.6.2.9.7 RB_HOLDOVER

表 8-86. Register 0x188

BIT	NAME	POR DEFAULT	DESCRIPTION
7:5	N/A		Reserved
4	RB_HOLDOVER		Read back 0: Not in HOLDOVER. Read back 1: In HOLDOVER.
3:0	N/A		Reserved

8.6.2.9.8 SPI_LOCK

Prevents SPI registers from being written to, except for 0x555.

This register cannot be read back.

表 8-87. Register 0x555

BIT	NAME	POR DEFAULT	DESCRIPTION
7:0	SPI_LOCK	0	0: Registers unlocked. 1 to 255: Registers locked.

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9 Application and Implementation

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9.1 Application Information

To assist customers in frequency planning and design of loop filters, Texas Instruments provides Clock Architect and PLLatinum Sim and on ti.com.

9.1.1 Treatment of Unused Pins

Not all pins are needed for every application. In general, power down the unused feature in software. The unused pin may be left floating or grounded through a 1-kΩ resistor.

表 9-1. Treatment of Unused Pins

PINS	TREATMENT IF UNUSED
CLKoutX/CLKoutX*	1 kΩ to GND or float pin
RESET/GPO	1 kΩ to GND or float pin
SYNC/SYSREF_REQ	1 kΩ to GND or float pin
Fin0/Fin0*	1 kΩ to GND or float pin
Status_LD1,Status_LD2	1 kΩ to GND or float pin
CPout1/CPout2	1 kΩ to GND or float pin
OSCout/CLKin2	1 kΩ to GND or float pin
OSCout*/CLKin2*	1 kΩ to GND or float pin

9.1.2 Digital Lock Detect Frequency Accuracy

The digital lock detect circuit is used to determine PLL1 locked, PLL2 locked, and holdover exit events. A window size and lock count register are programmed to set a ppm frequency accuracy of reference to feedback signals of the PLL for each event to occur. When a PLL digital lock event occurs, the digital lock detect of the PLL is asserted true. When the holdover exit event occurs, the device will exit holdover mode when HOLDOVER_EXIT_MODE = 1 (Exit based on DLD).

表 9-2. Digital Lock Detect Related Fields

EVENT	PLL	WINDOW SIZE	LOCK COUNT
PLL1 Locked	PLL1	PLL1_WND_SIZE	PLL1_DLD_CNT
PLL2 Locked	PLL2	PLL2_WND_SIZE	PLL2_DLD_CNT
Holdover exit	PLL1	PLL1_WND_SIZE	HOLDOVER_DLD_CNT

For a digital lock detect event to occur, there must be a *lock count* number of phase detector cycles of PLLX during which the time and phase error of the PLLX_R reference and PLLX_N feedback signal edges are within the user programmable *window size*. Because there must be at least one *lock count* phase detector event before a lock event occurs, a minimum digital lock event time can be calculated as *lock count* / f_{PDX} where X = 1 for PLL1 or 2 for PLL2.

By using 式 4, values for a *lock count* and *window size* can be chosen to set the frequency accuracy required by the system in ppm before the digital lock detect event occurs:

$$\text{ppm} = \frac{1e6 \times \text{PLLX_WND_SIZE} \times f_{PDX}}{\text{PLLX_DLD_CNT}} \quad (4)$$

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The effect of the *lock count* value is that it shortens the effective lock window size by dividing the *window size* by *lock count*.

If at any time the PLLX_R reference and PLLX_N feedback signals are outside the time window set by *window size*, then the *lock count* value is reset to 0.

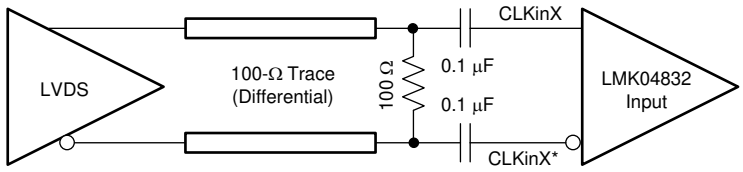
9.1.2.1 Minimum Lock Time Calculation Example

To calculate the minimum PLL2 *digital* lock time given a PLL2 phase detector frequency of 40 MHz and PLL2_DLD_CNT = 10,000. Then, the minimum lock time of PLL2 will be 10,000 / 40 MHz = 250 µs.

9.1.3 Driving CLKin AND OSCin Inputs

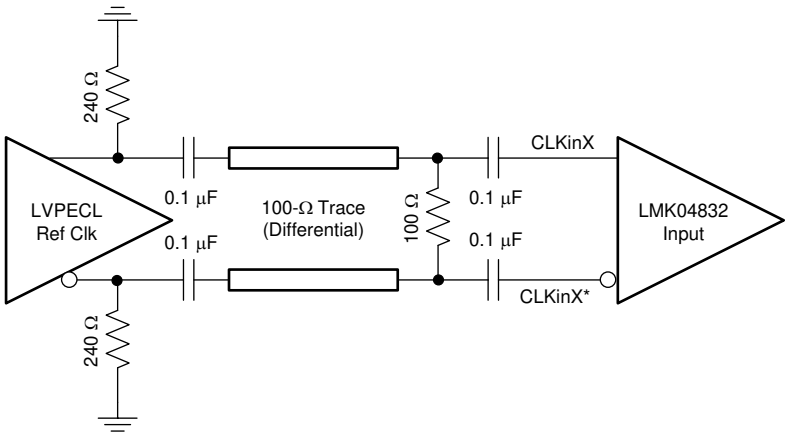
9.1.3.1 Driving CLKin and OSCin PINS With a Differential Source

CLKin and OSCin pins can be driven by differential signals. TI recommends setting the input mode to bipolar (CLKinX_BUF_TYPE = 0) when using differential reference clocks. The device internally biases the input pins so the differential interface should be AC-coupled. The recommended circuits for driving the CLKin pins with either LVDS or LVPECL are shown in 図 9-1 and 図 9-2.



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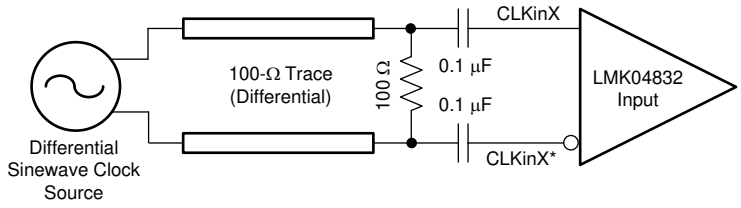
図 9-1. CLKinX/X* or OSCin Termination for an LVDS Reference Clock Source



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図 9-2. CLKinX/X* or OSCin Termination for an LVPECL Reference Clock Source

Finally, a reference clock source that produces a differential sine wave output can drive the CLKin pins using the following circuit. Note: the signal level must conform to the requirements for the CLKin pins listed in the セクション 6.5.



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図 9-3. CLKinX/X* or OSCin Termination for a Differential Sinewave Reference Clock Source

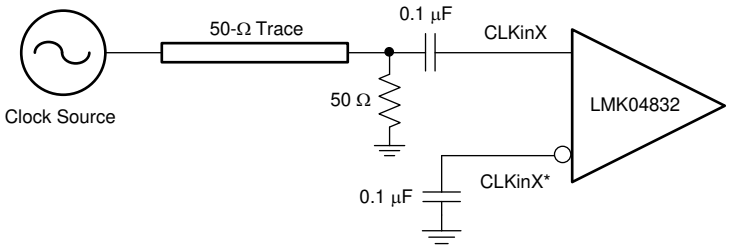
9.1.3.2 Driving CLKin Pins With a Single-Ended Source

The CLKin and OSCin pins can be driven using a single-ended reference clock source, for example, either a sine wave source or an LVCMOS/LVTTL source. CLKin supports both AC coupling or DC coupling. OSCin must use AC coupling. In the case of the sine wave source that is expecting a 50-Ω load, TI recommends using AC coupling as shown in 図 9-4 with a 50-Ω termination.

注

The signal level must conform to the requirements for the CLKin or OSCin pins listed in the セクション 6.5.

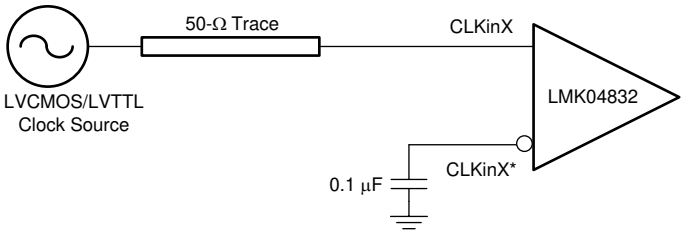
To support LOS functionality, CLKinX_BUF_TYPE must be set to MOS mode (CLKinX_BUF_TYPE = 1) when AC-coupled. When AC coupling, if the 100-Ω termination is placed on the IC side of the blocking capacitors, then the LOS functionality will not be valid.



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図 9-4. CLKinX/X* Single-Ended Termination

If the CLKin pins are being driven with a single-ended LVCMOS/LVTTL source, either DC coupling or AC coupling may be used. If DC coupling is used, the CLKinX_BUF_TYPE should be set to MOS buffer mode (CLKinX_BUF_TYPE = 1) and the voltage swing of the source must meet the specifications for DC -oupled, MOS-mode clock inputs given in the セクション 6.5. If AC coupling is used, the CLKinX_BUF_TYPE should be set to the bipolar buffer mode (CLKinX_BUF_TYPE = 0). The voltage swing at the input pins must meet the specifications for AC-coupled, bipolar mode clock inputs given in the セクション 6.5. In this case, some attenuation of the clock input level may be required. A simple resistive divider circuit before the AC-coupling capacitor is sufficient.



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図 9-5. DC-Coupled LVCMOS/LVTTL Reference Clock

9.1.4 OSCin Doubler for Best Phase Noise Performance

PLL2 OSCin input path includes an on-chip Frequency Doubler. To have the best phase noise performance, TI recommends to maximize the PLL2 phase detector frequency. For example, using 122.88-MHz VCXO, PLL2 phase detector frequency can be increased to 245.76 MHz by setting PLL2_REF_2X_EN. Doubler path is a high performance path for OSCin clock. For configuration where doubler cannot be used, TI recomends to use Doubler and PLL2_RDIV = 2. To have deterministic phase relationship between input clock and output clocks, 0-delay modes should be used (nested 0-delay mode for dual loop configuration instead of cascaded 0-delay mode).

9.1.5 Radiation Environments

9.1.5.1 Total Ionizing Dose

Radiation Hardness assured (RHA) products are those part numbers with a total ionizing dose (TID) level specified in the ordering information. Testing and qualification of these product is done on a wafer level according to MIL-STD-883, test method 1019. Wafer level TID data are available with lot shipments.

9.1.5.2 Single Event Effect

One time single event effect (SEE), including single event latch-up (SEL), single event functional interrupt (SEFI) and single event upset (SEU), testing was performed according to EIA/JEDEC Standard, EIA/JEDEC57. A test report is available upon request.

9.2 Typical Application

This design example highlights using the available tools to design loop filters and create programming map.

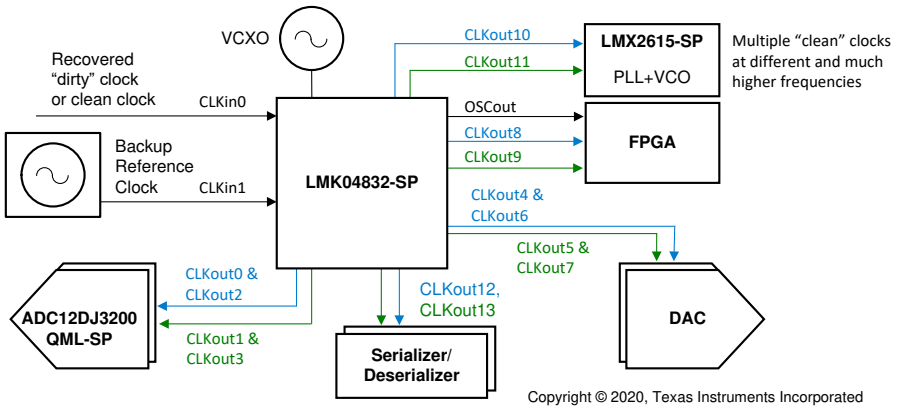


図 9-6. Typical Application

9.2.1 Design Requirements

Clocks outputs:

- 1x 245.76-MHz clock for JESD204B ADC, LVPECL.
  - This clock requires the best performance in this example.
- 2x 2949.12-MHz clock for JESD204B DAC, CML.
- 1x 122.88-MHz clock for JESD204B FPGA block, LVDS.
- 3x 10.24-MHz SYSREF for ADC (LVPECL), DAC (LVPECL), FPGA (LVDS).
- 2x 122.88-MHz clock for FPGA, LVDS.

For best performance, the highest possible phase detector frequency is used at PLL2. As such, a 122.88-MHz VCXO is used.

9.2.2 Detailed Design Procedure

注

This information is current as of the date of the release of this data sheet. Design tools receive continuous improvements to add features and improve model accuracy. Refer to the software instructions or training for latest features.

9.2.2.1 Device Selection

Enter the required frequencies into the tools. In this design, VCO0 and VCO1 both meet the design requirements. VCO0 offers a relatively improved VCO performance over VCO1. In this case, choose VCO0 for improved RMS jitter in the 12-kHz to 20-MHz integration range.

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9.2.2.1.1 Clock Architect

Under the advanced tab of the Clock Architect, filtering of specific parts can be done using regular expressions in the Part Filter box. [LMK04832.*] will filter for only the LMK04832 device (without brackets). More detailed filters can be given such as the entire part name LMK04832_VCO0 to force an LMK04832 using VCO0 solution if one is available.

9.2.2.2 Device Configuration and Simulation

The tools automatically configure the simulation to meet the input and output frequency requirements given, and make assumptions about other parameters to give some default simulations. However, the user may chose to make adjustments for more accurate simulations to their application. For example:

- Entering the VCO Gain of the external VCXO or possible external VCO used device.
- Adjust the charge pump current to help with loop filter component selection. Lower charge pump currents result in smaller components but may increase impacts of leakage and at the lowest values reduce PLL phase nosie performance.
- Clock Architect allows loading a custom phase noise plot for reference or VCXO block. Typically, a custom phase noise plot is entered for CLKin to match the reference phase noise to device; a phase noise plot for the VCXO can additionally be provided to match the performance of VCXO used. For improved accuracy in simulation and optimum loop filter design, be sure to load these custom noise profiles for use in application.
- PLLatinum Sim can also be used to design and simulate a loop filter.

9.2.2.3 Device Programming

Using the clock design tools configuration the TICS Pro software is manually updated with this information to meet the required application.

Frequency planning for assignment of outputs:

- To minimize crosstalk perform frequency planning / CLKout assignments to keep common frequencies on outputs close together.
- It is best to place common device clock output frequencies on outputs sharing the same V_{CC} group. For example, these outputs share Vcc4_CG2. Refer to セクション 5 to see the V_{CC} groupings the clock outputs.

In this example, the 245.76-MHz ADC output needs the best performance. CLKout2 provides the best noise floor / performance. The 245.76 MHz is placed on CLKout2 with 10.24-MHz SYSREF on CLKout3.

- For best performance the input and output drive level bits may be set. Best noise floor performance is achieved with CLKout2_3_IDL = 1 and CLKout2_3_ODL = 1.
- The CLKoutX_Y_ODL bit has no impact on even clock outputs in high performance bypass mode.

In this example, the 983.04-MHz DAC output is placed on CLKout4 and CLKout6 with 10.24-MHz SYSREF on paired CLKout5 and CLKout7 outputs.

- These outputs share Vcc4_CG2.

In this example, the 122.88-MHz FPGA JESD204B output is placed on CLKout10 with 10.24-MHz SYSREF on paired CLKout11 output.

Additionally, the 122.88-MHz FPGA non-JESD204B outputs are placed on CLKout8 and CLKout9.

- When frequency planning, consider PLL2 as a clock output at the phase detector frequency. As such, these 122.88-MHz outputs have been placed on the outputs close to the PLL2 and Charge Pump power supplies.

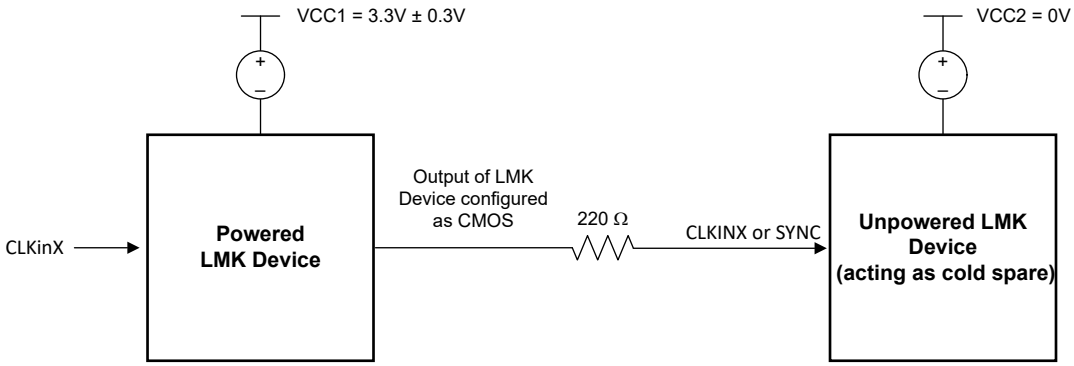
Once the device programming is completed as desired in the TICS Pro software, it is possible to export the register settings from the Register tab for use in application.

9.3 Power Supply Recommendations

9.3.1 Cold Sparing Considerations

図 9-7 below demonstrates how this part can be used for cold sparing

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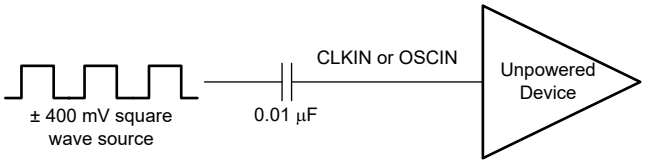
図 9-7. Cold Sparing Devices Setup

9.3.1.1 Damage Prevention Details to Unpowered Device

Setting two devices in a cold sparing setup leads to the unpowered device receiving DC-coupled LVCMOS pulses on the CLKIN0 or SYNC inputs periodically throughout the lifetime of the unpowered device. The cumulative lifetime limit for the unpowered device DC input current is 10 hours at maximum junction temperature. Also, the device can remain within specifications for much longer than this limit if the typical cold-spare junction temperature is lower than maximum junction temperature. However, by placing a 220-Ω in series between the output of the poweredde to the inputs of the unpowered devP, even when connected to a 3.3-V or 3.6-V powered system, DC pulses from the powered device do not damage the unpowered device. DC-coupling 3.3V or 3.6-V I/O can occur without the transmitter for the SYNC signal failing high and destroying the receiver, or any other circuitry within the unpowered device. Also, the 220-Ω resistor limits the current to about 7 mA, with less than 12 mW dissipated onto the unpowered device.

Additionally, if CLKIN is damaged or fails short in one of the CLKIN paths with the 220-Ω resistor in series to ground on the fault path, the current is limited. The initial damage won't short to the outputs of the transmitter powered device, and therefore, no damage occurs to the rest of the system. The inputs and outputs of each device have separate power supply pins that are not connected internally; therefore, if the unpowered device is powered, no issues can occur to the outputs, even if one of the inputs is damaged over the lifetime of the unpowered device.

When driving the CLKINx or OSCin inputs of an unpowered device, signal levels up to ± 400 mV can be AC-coupled through 0.01 µF across the operating frequency range. Under these constraints, the magnitude of the RMS currents injected into the CLKinX ESD structures is within acceptable power and current limits across the full junction temperature range and won't cause long-term degradation of function. Larger amplitudes, higher frequencies, or different coupling capacitors can be acceptable as long as the signal is AC-coupled and the unpowered current limit of 7 mA going into or coming out of the CLKIN or OSCIN pins is observed.



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図 9-8. AC-Coupled ± 400 mV Signal Inputted to Unpowered Device

9.3.2 Current Consumption

TI recommends using the TICS Pro software to calculate the current consumption estimate based on programmed configuration.

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9.4 Layout

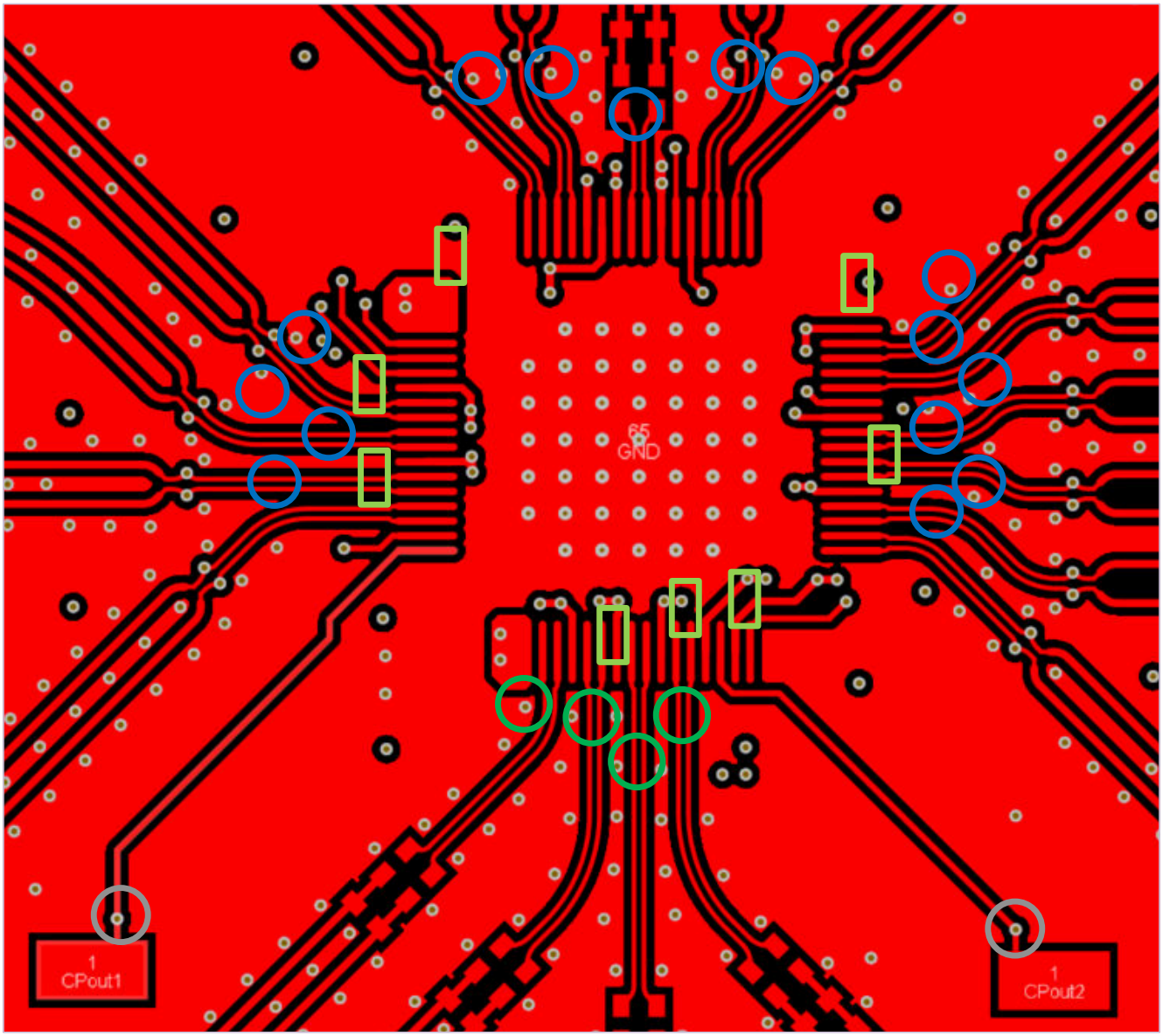
9.4.1 Layout Guidelines

9.4.1.1 Thermal Management

Power consumption of the LMK04832-SP can be high enough to require attention from thermal management. For reliability and performance reasons the die temperature should be limited to a maximum of 125°C. That is, as an estimate, T_A (ambient temperature) plus device power consumption times $R_{\theta JA}$ should not exceed 125°C.

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9.4.2 Layout Example



CLKouts/OSCouts - Differential signals should be routed tightly coupled to minimize PCB crosstalk.
For LVPECL/LCPECL/CML place components resistors close to IC.
OSCout shares pins with CLKin2 and is programmable for input or output.

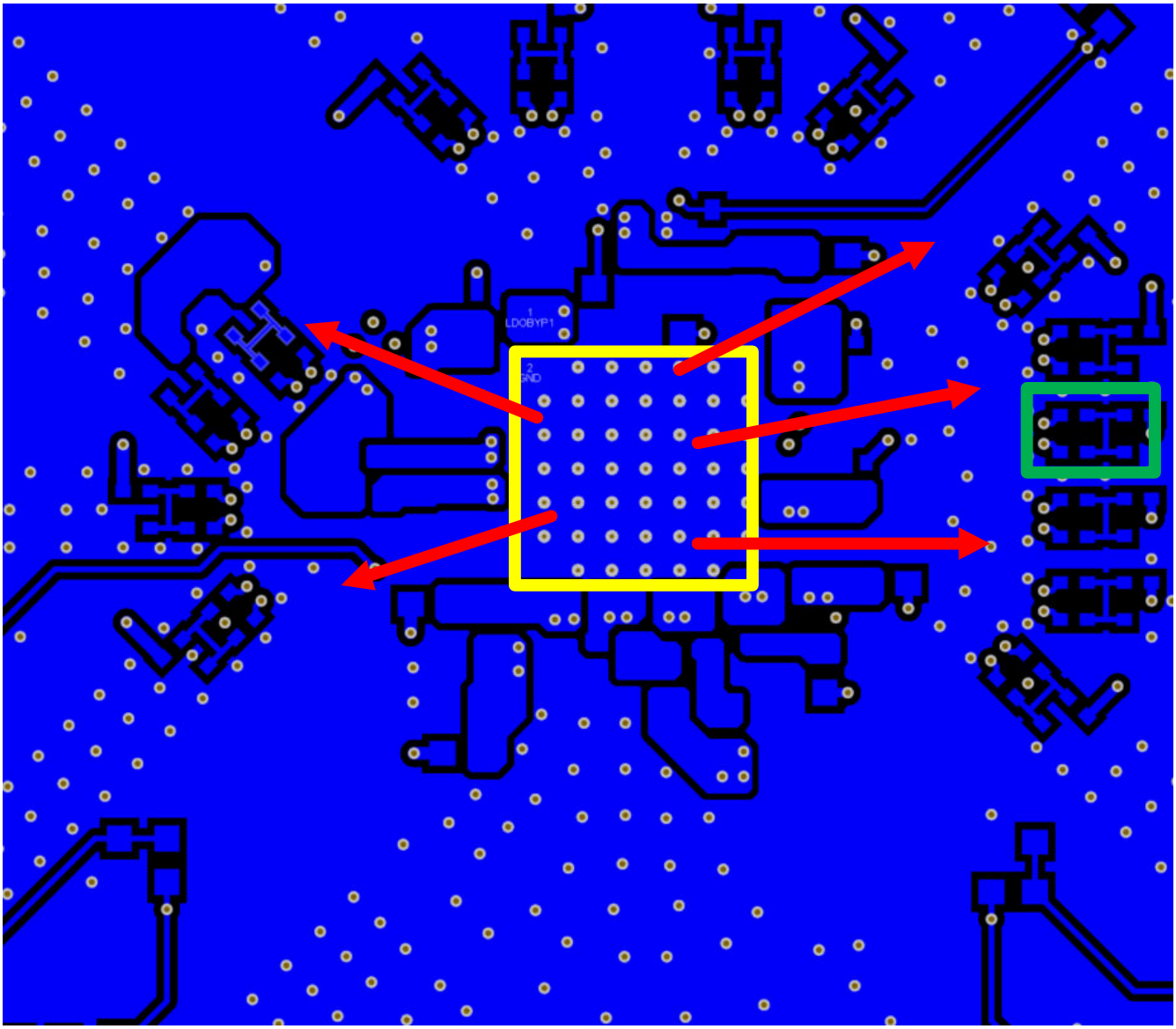
CLKin and OSCin - If differential input (preferred) route traces tightly coupled. If single ended, have at least 3-trace width (of CLKin/ OSCin trace) separation from other RF traces. Place terminations close to IC. CLKin2 and OSCout share pins and are programmable for input or output.

For CLKout Vccs in JESD204B application, Place the ferrite beads then a 1-µF capacitor. The 1-µF capacitor supports low-frequency SYSREF switching/turning on.
For CLKout Vccs in traditional applications, place a ferrite bead on top layer close to pins to choke high-frequency noise from the via.

Charge pump output - shorter traces are better. Place all resistors and caps close to the IC.

図 9-9. Top Layer

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Expose copper under the PCB to provide direct copper-to-air interface to dissipate heat.

A flexible termination / PCB layout for either CML requiring a pullup to Vcc or LVPECL/LCPECL requiring a pulldown to ground, or the H configuration for any other format as illustrated in layout above.

Provide areas of connect copper to allow heat to escape from directly below PCB. Do not let components block all thermal escape from the ground pad.

図 9-10. Bottom Layer

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10 Device and Documentation Support

10.1 Device Support

10.1.1 Development Support

10.1.1.1 Clock Architect

Part selection, loop filter design, simulation.

To run the online Clock Architect tool, go to www.ti.com/clockarchitect.

10.1.1.2 PLLatinum Sim

Supports loop filter design and simulation. All simulation is for a single loop, to perform dual loop simulations, the result of the first PLL sim must be loaded as a reference to the second PLL sim.

To download PLLatinum Sim tool, go to www.ti.com/tool/PLLATINUMSIM-SW

10.1.1.3 TICS Pro

EVM programming software. Can also be used to generate register map for programming and calculate current consumption estimate.

For TICS Pro, go to www.ti.com/tool/TICSPRO-SW

10.2 Documentation Support

10.2.1 Related Documentation

For releated documentation, see the following:

- *AN-912 Common Data Transmission Parameters and their Definitions* (SNLA036)

10.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

10.4 サポート・リソース

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10.5 Trademarks

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10.6 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

10.7 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

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11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This data is subject to change without notice and revision of this document.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
5962R1723701VXC	Active	Production	CFP (HBE) | 64	14 | TUBE	ROHS Exempt	NIAU	Level-1-NA-UNLIM	-55 to 125	5962R1723701VXC LMK04832-SP
5962R1723701VXC.A	Active	Production	CFP (HBE) | 64	14 | TUBE	ROHS Exempt	NIAU	Level-1-NA-UNLIM	-55 to 125	5962R1723701VXC LMK04832-SP
LMK04832W/EM	Active	Production	CFP (HBE) | 64	14 | TUBE	ROHS Exempt	NIAU	Level-1-NA-UNLIM	25 to 25	LMK04832W/EM EVAL ONLY
LMK04832W/EM.A	Active	Production	CFP (HBE) | 64	14 | TUBE	ROHS Exempt	NIAU	Level-1-NA-UNLIM	25 to 25	LMK04832W/EM EVAL ONLY
SN0064HBE	Active	Production	CFP (HBE) | 64	1 | TUBE	-	Call TI	Call TI	25 to 25	SN0064 ES MECHANICAL

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

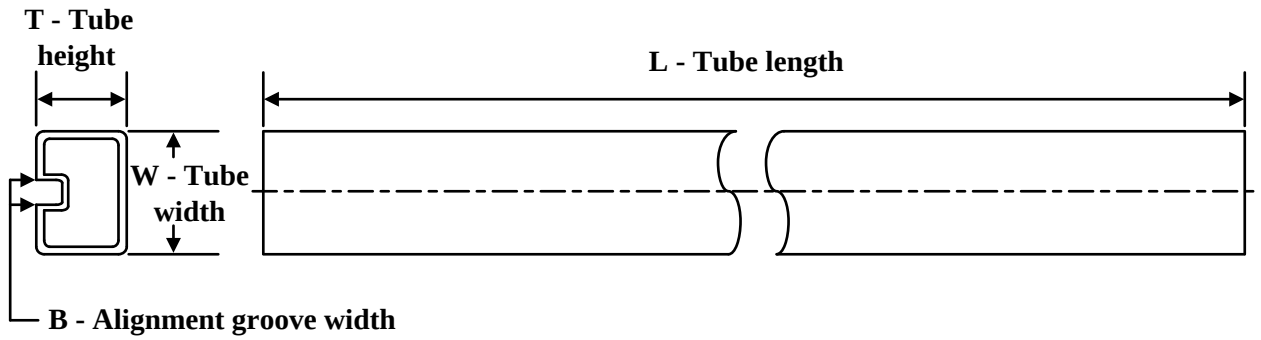
OTHER QUALIFIED VERSIONS OF LMK04832-SP :

- Catalog : LMK04832

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

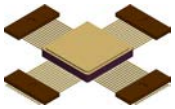
TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
5962R1723701VXC	HBE	CFP (HSL)	64	14	495	33	11176	16.51
5962R1723701VXC.A	HBE	CFP (HSL)	64	14	495	33	11176	16.51
LMK04832W/EM	HBE	CFP (HSL)	64	14	495	33	11176	16.51
LMK04832W/EM.A	HBE	CFP (HSL)	64	14	495	33	11176	16.51

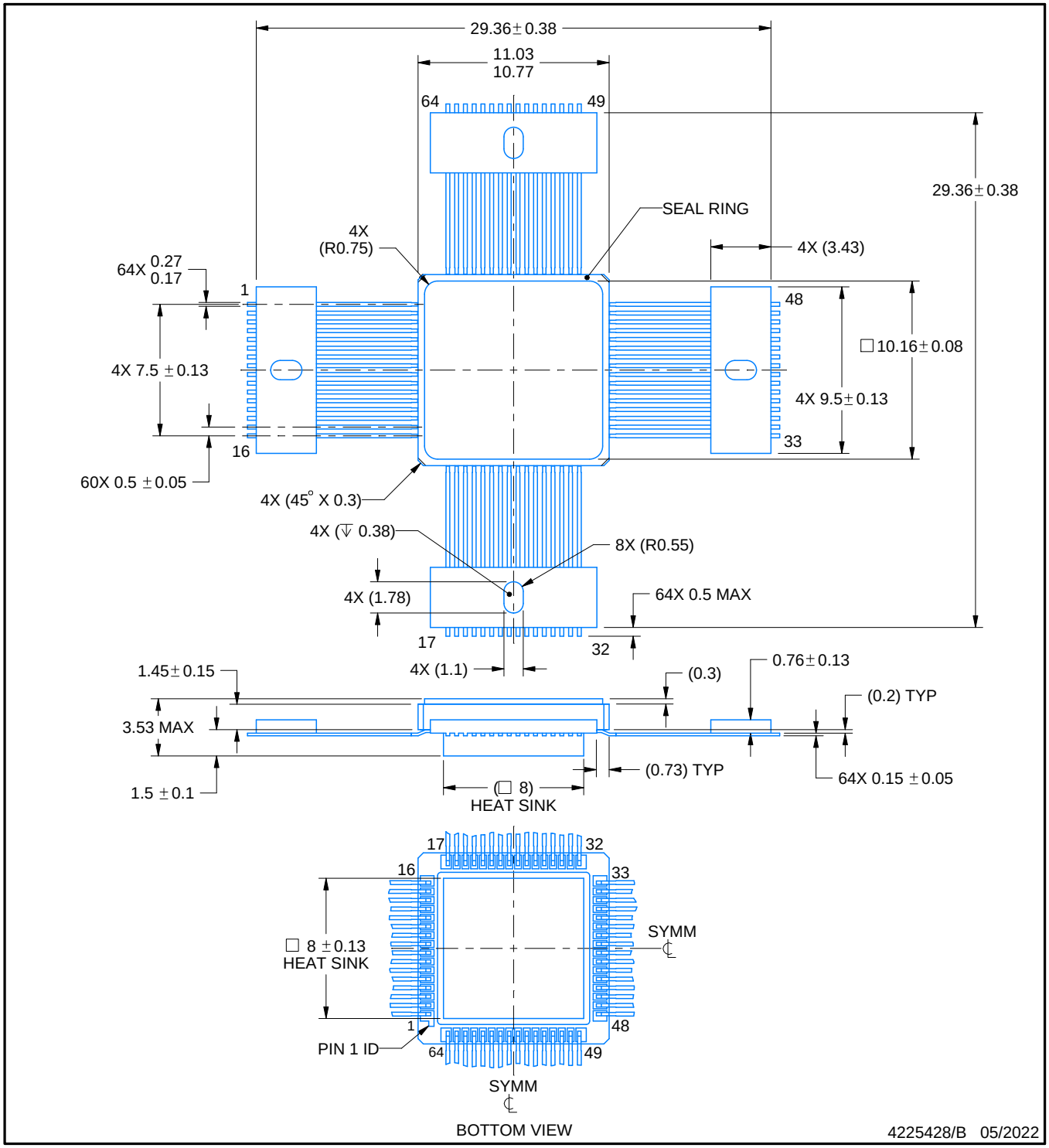
HBE0064B



PACKAGE OUTLINE

CFP - 3.53 mm max height

CERAMIC FLATPACK



NOTES:

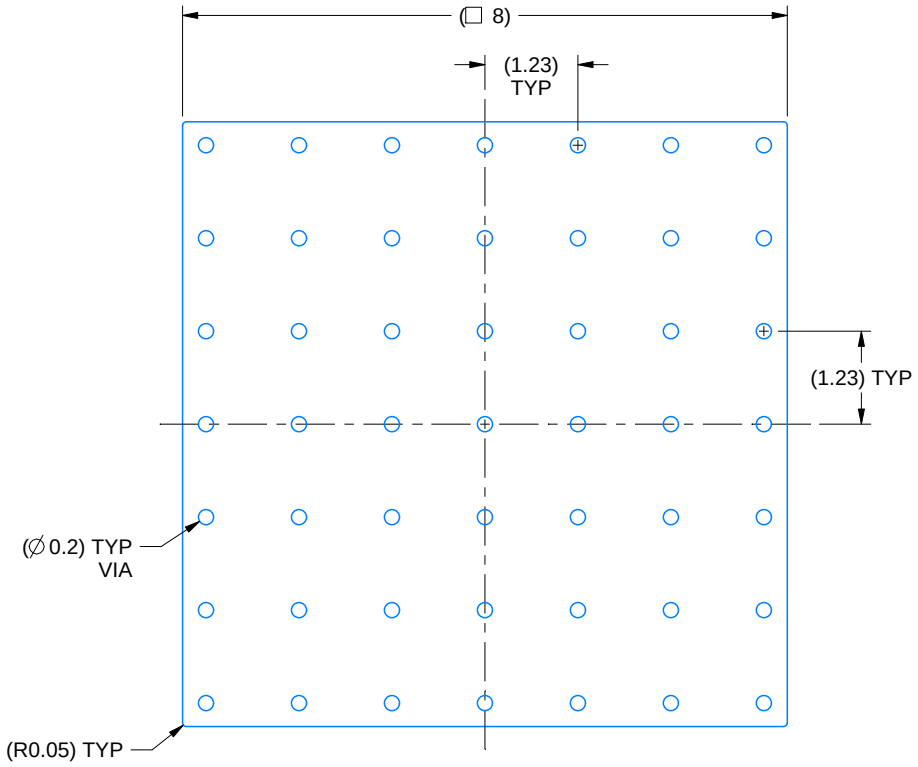
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package is hermetically sealed with a metal lid.
4. Ground pad to be electronic connected to heat sink and seal ring.
5. The leads are gold plated and can be solder dipped.

EXAMPLE BOARD LAYOUT

HBE0064B

CFP - 3.53 mm max height

CERAMIC FLATPACK



HEATSINK LAND PATTERN EXAMPLE
SCALE: 10X

4225428/B 05/2022

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