LMK61E2 EEPROM 内蔵、超低ジッタ プログラマブル発振器

1 特長

- 超低ノイズ、高性能
  - ジッタ:90fs RMS (標準値)、f_{OUT} > 100MHz
  - PSRR:-70dBc、堅牢な電源ノイズ耐性
- 柔軟な出力フォーマット、ユーザー選択可能
  - LVPECL:最大 1GHz
  - LVDS:最大 900MHz
  - HCSL:最大 400 MHz
- 合計周波数許容誤差:±50ppm
- システム レベルの特長
  - 周波数マージンニング:細/粗
  - EEPROM 内蔵:ユーザーが構成可能なデフォルト設定
- その他の特長
  - デバイス制御:I²C
  - 3.3V の動作電圧
  - 産業用温度範囲 (–40℃～+85℃)
  - 7mm × 5mm の 8 ピン パッケージ
  - WEBENCH® Power Designer により、LMK61E2 を使用するカスタム設計を作成

2 アプリケーション

- 水晶振動子、SAW、またはシリコン ベースの発振器に代わる高性能の代替品
- スイッチ、ルータ、ネットワーク ライン カード、ベースバンド ユニット (BBU)、サーバ、ストレージ / SAN
- 試験 / 測定機器
- 医療用画像処理
- FPGA、プロセッサ アタッチ

3 説明

LMK61E2 デバイスは、fractional-N 周波数シンセサイザと内蔵 VCO を備えた超低ジッタ PLLatinum™ プログラマブル発振器で、一般的に使用されるリファレンス クロックを生成します。出力は、LVPECL、LVDS、または HCSL として構成できます。

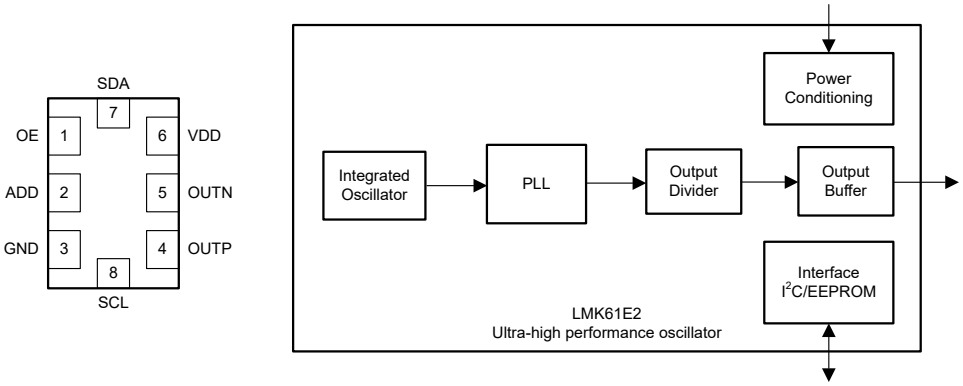
このデバイスは、156.25MHz LVPECL 出力を生成するよう工場出荷時にプログラムされたオンチップ EEPROM による自己スタートアップを備えています。デバイスのレジスタおよびオンチップ EEPROM 設定は、I²C 互換のシリアル インターフェイスにより完全にプログラム可能です。内蔵パワー コンディショニングは、優れた電源リップル除去 (PSRR) を提供し、電力供給ネットワークのコストと複雑さを低減します。このデバイスは、3.3V ± 5% の単電源で動作します。

このデバイスには、I²C シリアル インターフェイスによる細/粗周波数マージニング オプションが用意されており、標準のコンプライアンスおよびシステム タイミング マージン テストなど、システム設計検証テスト (DVT) をサポートします。

パッケージ情報

部品番号	デフォルト出力周波数 (MHz) とフォーマット	パッケージ (1)	パッケージ サイズ(2)
LMK61E2	156.25 LVPECL	SIA (QFM、8)	7.00mm × 5.00mm
LMK61E2BAA	156.25 LVDS		
LMK61E2BBA	125 LVDS		

(1) 詳細については、セクション 12 を参照してください。
(2) パッケージ サイズ (長さ × 幅) は公称値であり、該当する場合はピンを含みます。



ピン配置と単純なブロック図

このリソースの元の言語は英語です。翻訳は概要を便宜的に提供するもので、自動化ツール (機械翻訳) を使用していることがあり、TI では翻訳の正確性および妥当性につきましては一切保証いたしません。実際の設計などの前には、ti.com で必ず最新の英語版をご参照くださいますようお願いいたします。

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4 Pin Configuration and Functions

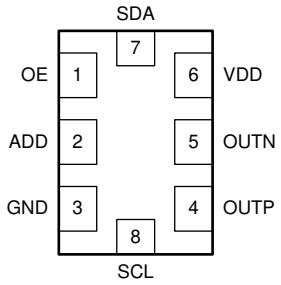


図 4-1. SIA Package 8-Pin QFM Top View

表 4-1. Pin Functions

PIN		Type	DESCRIPTION
NAME	NO.		
POWER			
GND	3	Ground	Device Ground.
VDD	6	Analog	3.3V Power Supply.
OUTPUT BLOCK			
OUTP, OUTN	4, 5	Universal	Differential Output Pair (LVPECL, LVDS or HCSL).
DIGITAL CONTROL / INTERFACES			
ADD	2	LVCMOS	When left open, LSB of I^2C target address is set to 01. When tied to VDD, LSB of I^2C target address is set to 10. When tied to GND, LSB of I^2C target address is set to 00.
OE	1	LVCMOS	Output Enable (internal pullup). When set to low, output pair is disabled and set at high impedance.
SCL	8	LVCMOS	I^2C Serial Clock (open-drain). Requires an external pullup resistor to VDD.
SDA	7	LVCMOS	I^2C Serial Data (bidirectional, open-drain). Requires an external pullup resistor to VDD.

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5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
VDD	Device supply voltage	–0.3	3.6	V
V_{IN}	Output voltage for logic inputs	–0.3	VDD + 0.3	V
V_{OUT}	Output voltage for clock outputs	–0.3	VDD + 0.3	V
T_J	Junction temperature		150	°C
T_{stg}	Storage temperature	–40	125	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±500	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
VDD	Device supply voltage	3.135	3.3	3.465	V
T_A	Ambient temperature	–40	25	85	°C
T_J	Junction temperature			125	°C
t_{RAMP}	VDD power-up ramp time	0.1		100	ms

5.4 Thermal Information

THERMAL METRIC(1)		LMK61E2 (2) (3) (4) QFM (SIA) 8 PINS			UNIT
		AIRFLOW (LFM) 0	AIRFLOW (LFM) 200	AIRFLOW (LFM) 400	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	54	44	41.2	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	34	n/a	N/A	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	36.7	n/a	N/A	°C/W
ψ_{JT}	Junction-to-top characterization parameter	11.2	16.9	21.9	°C/W
ψ_{JB}	Junction-to-board characterization parameter	36.7	37.8	38.9	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application note.
(2) The package thermal resistance is calculated on a 4-layer JEDEC board.
(3) Connected to GND with 3 thermal vias (0.3mm diameter).

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(4) ψ_{JB} (junction-to-board) is used when the main heat flow is from the junction to the GND pad. See the *Layout* section for more information on providing good system reliability and quality.

5.5 Electrical Characteristics - Power Supply

VDD = 3.3V ± 5%, T_A = –40°C to 85°C

PARAMETER		TEST CONDITIONS(1)	MIN	TYP	MAX	UNIT
IDD	Device current consumption	LVPECL(2)		162	208	mA
		LVDS		152	196	
		HCSL		155	196	
IDD-PD	Device current consumption when output is disabled	OE = GND		136		mA

(1) See *Parameter Measurement Information* for relevant test conditions.
(2) On-chip power dissipation must exclude 40mW, dissipated in the 150Ω termination resistors, from total power dissipation.

5.6 LVPECL Output Characteristics

VDD = 3.3V ± 5%, T_A = –40°C to 85°C

PARAMETER		TEST CONDITIONS(1)	MIN	TYP	MAX	UNIT
f_{OUT}	Output frequency(2)		10		1000	MHz
V_{OD}	Output voltage swing ($V_{OH} – V_{OL}$)(2)		700	800	1200	mV
$V_{OUT, DIFF, PP}$	Differential output peak-to-peak swing			2 × | V_{OD}|		V
V_{OS}	Output common-mode voltage			VDD – 1.55		V
t_R / t_F	Output rise/fall time (20% to 80%)(3)			120	200	ps
PN-Floor	Output phase noise floor (f_{OFFSET} > 10MHz)	156.25MHz		–165		dBc/Hz
ODC	Output duty cycle(3)		45%		55%	

(1) See *Parameter Measurement Information* for relevant test conditions.
(2) An output frequency over f_{OUT} maximum specification is possible, but output swing can be less than V_{OD} minimum specification.
(3) Verified by characterization.

5.7 LVDS Output Characteristics

VDD = 3.3V ± 5%, T_A = –40°C to 85°C

PARAMETER		TEST CONDITIONS(1)	MIN	TYP	MAX	UNIT
f_{OUT}	Output frequency(1)		10		900	MHz
V_{OD}	Output voltage swing ($V_{OH} – V_{OL}$)(1)		300	390	480	mV
$V_{OUT, DIFF, PP}$	Differential output peak-to-peak swing			2 × |V_{OD}|		V
V_{OS}	Output common-mode voltage			1.2		V
t_R / t_F	Output rise/fall time (20% to 80%)(2)			150	250	ps
PN-Floor	Output phase noise floor (f_{OFFSET} > 10MHz)	156.25MHz		–162		dBc/Hz
ODC	Output duty cycle(2)		45%		55%	
R_{OUT}	Differential output impedance			125		Ω

(1) An output frequency over f_{OUT} maximum specification is possible, but output swing can be less than V_{OD} minimum specification.
(2) Verified by characterization.

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5.8 HCSL Output Characteristics

VDD = 3.3V ± 5%, T_A = –40°C to 85°C

PARAMETER		TEST CONDITIONS(1)	MIN	TYP	MAX	UNIT
f_{OUT}	Output frequency		10		400	MHz
V_{OH}	Output high voltage		600		850	mV
V_{OL}	Output low voltage		–100		100	mV
V_{CROSS}	Absolute crossing voltage(2) (3)		250		475	mV
$V_{CROSS-DELTA}$	Variation of V_{CROSS} (2) (3)		0		140	mV
dV/dt	Slew rate(4)		0.8		2	V/ns
PN-Floor	Output phase noise floor (f_{OFFSET} > 10MHz)	100MHz		–164		dBc/Hz
ODC	Output duty cycle(4)		45%		55%	

(1) See *Parameter Measurement Information* for relevant test conditions.
(2) Measured from –150mV to +150mV on the differential waveform with the 300-mVpp measurement window centered on the differential zero crossing.
(3) Verified by design.
(4) Verified by characterization.

5.9 OE Input Characteristics

VDD = 3.3V ± 5%, T_A = –40°C to 85°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IH}	Input high voltage		1.4			V
V_{IL}	Input low voltage				0.6	V
I_{IH}	Input high current	V_{IH} = VDD	–40		40	µA
I_{IL}	Input low current	V_{IL} = GND	–40		40	µA
C_{IN}	Input capacitance			2		pF

5.10 ADD Input Characteristics

VDD = 3.3V ± 5%, T_A = –40°C to 85°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IH}	Input high voltage		1.4			V
V_{IL}	Input low voltage				0.4	V
I_{IH}	Input high current	V_{IH} = VDD	–40		40	µA
I_{IL}	Input low current	V_{IL} = GND	–40		40	µA
C_{IN}	Input capacitance			2		pF

5.11 Frequency Tolerance Characteristics (1)

VDD = 3.3V ± 5%, T_A = –40°C to 85°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_T	Total frequency tolerance	All output formats, frequency bands and device junction temperature up to 125°C; includes initial frequency tolerance, temperature and supply voltage variation, solder reflow and aging (10 years)	–50		50	ppm

(1) Verified by characterization.

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5.12 Power-On/Reset Characteristics (VDD)

VDD = 3.3V ± 5%, T_A = –40°C to 85°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{THRESH}	Threshold voltage(1)		2.72		2.95	V
V_{DROOP}	Allowable voltage droop(2)				0.1	V
$t_{STARTUP}$	Start-up time (1)	Time elapsed from VDD at 3.135V to output enabled			10	ms
t_{OE-EN}	Output enable time(2)	Time elapsed from OE at V_{IH} to output enabled			50	µs
t_{OE-DIS}	Output disable time(2)	Time elapsed from OE at V_{IL} to output disabled			50	µs

(1) Verified by characterization.
(2) Verified by design.

5.13 I²C-Compatible Interface Characteristics (SDA, SCL)

VDD = 3.3V ± 5%, T_A = –40°C to 85°C

PARAMETER		TEST CONDITIONS(1)	MIN	TYP(2)	MAX	UNIT
V_{IH}	Input high voltage		1.2			V
V_{IL}	Input low voltage				0.6	V
I_{IH}	Input leakage		–40		40	µA
C_{IN}	Input capacitance			2		pF
C_{OUT}	Input capacitance				400	pF
V_{OL}	Output low voltage	I_{OL} = 3mA			0.6	V
f_{SCL}	I²C clock rate		100		400	kHz
t_{SU_STA}	START condition setup time	SCL high before SDA low	0.6			µs
t_{H_STA}	START condition hold time	SCL low after SDA low	0.6			µs
t_{PH_SCL}	SCL pulse width high		0.6			µs
t_{PL_SCL}	SCL pulse width low		1.3			µs
t_{H_SDA}	SDA hold time	SDA valid after SCL low	0		0.9	µs
t_{SU_SDA}	SDA setup time		115			ns
t_{R_IN} / t_{F_IN}	SCL/SDA input rise and fall time				300	ns
t_{F_OUT}	SDA output fall time	C_{BUS} = 10pF to 400pF			250	ns
t_{SU_STOP}	STOP condition setup time		0.6			µs
t_{BUS}	Bus free time between STOP and START		1.3			µs

(1) Total capacitive load for each bus line ≤ 400pF.
(2) Verified by design.

5.14 PSRR Characteristics

VDD = 3.3V, T_A = 25°C, PLL bandwidth = 400kHz, VCO Frequency = 5GHz (Integer-N PLL), Output Divider = 32, Output Type = LVPECL/LVDS/HCSL

PARAMETER		TEST CONDITIONS(1)	MIN	TYP	MAX	UNIT
PSRR	Spurs induced by 50mV power supply ripple(2) (3) at 156.25MHz output, all output types	Sine wave at 50kHz		–70		dBc
		Sine wave at 100kHz		–70		
		Sine wave at 500kHz		–70		
		Sine wave at 1MHz		–70		

(1) See *Parameter Measurement Information* for relevant test conditions.
(2) Measured maximum spur level with 50mVpp sinusoidal signal between 50kHz and 1MHz applied on VDD pin

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(3) DJ_{SPUR} (ps, pk-pk) = [2 × 10(SPUR/20) / (π × f_{OUT})] × 1e6, where PSRR or SPUR in dBc and f_{OUT} in MHz.

5.15 Other Characteristics

VDD = 3.3V ± 5%, T_A = –40°C to 85°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{VCO}	VCO frequency range		4.6		5.6	GHz

5.16 PLL Clock Output Jitter Characteristics (1) (3)

VDD = 3.3V ± 5%, T_A = –40°C to 85°C

PARAMETER(3)		TEST CONDITIONS(1)	MIN	TYP	MAX	UNIT
RJ	RMS phase jitter(2) (12kHz – 20MHz) (1kHz – 5MHz)	f_{OUT} ≥ 100MHz, Integer-N PLL, All output types		100	200	fs RMS
RJ	RMS phase jitter(2) (12kHz – 20MHz) (1kHz – 5MHz)	f_{OUT} ≥ 100MHz, Fractional-N PLL, All output types		150	300	fs RMS

(1) See *Parameter Measurement Information* for relevant test conditions.
(2) Verified by characterization.
(3) Phase jitter measured with Agilent E5052 signal source analyzer using a differential-to-single ended converter (balun or buffer).

5.17 Typical 156.25MHz Output Phase Noise Characteristics (1) (2)

VDD = 3.3V, T_A = 25°C, PLL bandwidth = 400kHz, VCO Frequency = 5GHz, Integer-N PLL, Output Divider = 32, Output Type = LVPECL/LVDS/HCSL

PARAMETER		OUTPUT TYPE			UNIT
		LVPECL	LVDS	HCSL	
phn_{10k}	Phase noise at 10kHz offset	–143	–143	–143	dBc/Hz
Phn_{20k}	Phase noise at 20kHz offset	–143	–143	–143	dBc/Hz
phn_{100k}	Phase noise at 100kHz offset	–144	–144	–144	dBc/Hz
Phn_{200k}	Phase noise at 200kHz offset	–145	–145	–145	dBc/Hz
phn_{1M}	Phase noise at 1MHz offset	–150	–150	–150	dBc/Hz
phn_{2M}	Phase noise at 2MHz offset	–154	–154	–154	dBc/Hz
phn_{10M}	Phase noise at 10MHz offset	–165	–162	–164	dBc/Hz
phn_{20M}	Phase noise at 20MHz offset	–165	–162	–164	dBc/Hz

(1) See *Parameter Measurement Information* for relevant test conditions.
(2) Phase jitter measured with Agilent E5052 signal source analyzer using a differential-to-single ended converter (balun or buffer).

5.18 Typical 161.1328125 MHz Output Phase Noise Characteristics

VDD = 3.3V, T_A = 25°C, PLL bandwidth = 400kHz, VCO Frequency = 5.15625GHz, Fractional-N PLL, Output Divider = 32, Output Type = LVPECL/LVDS/HCSL

PARAMETER(1) (2)		OUTPUT TYPE			UNIT
		LVPECL	LVDS	HCSL	
phn_{10k}	Phase noise at 10kHz offset	–136	–136	–136	dBc/Hz
phn_{20k}	Phase noise at 20kHz offset	–136	–136	–136	dBc/Hz
phn_{100k}	Phase noise at 100kHz offset	–140	–140	–140	dBc/Hz
phn_{200k}	Phase noise at 200kHz offset	–141	–141	–141	dBc/Hz
phn_{1M}	Phase noise at 1MHz offset	–148	–148	–148	dBc/Hz
phn_{2M}	Phase noise at 2MHz offset	–156	–156	–156	dBc/Hz
phn_{10M}	Phase noise at 10MHz offset	–161	–159	–160	dBc/Hz

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VDD = 3.3V, T_A = 25°C, PLL bandwidth = 400kHz, VCO Frequency = 5.15625GHz, Fractional-N PLL, Output Divider = 32, Output Type = LVPECL/LVDS/HCSL

PARAMETER(1) (2)		OUTPUT TYPE			UNIT
		LVPECL	LVDS	HCSL	
phn_{20M}	Phase noise at 20MHz offset	–162	–160	–161	dBc/Hz

(1) See *Parameter Measurement Information* for relevant test conditions.
(2) Phase jitter measured with Agilent E5052 signal source analyzer using a differential-to-single ended converter (balun or buffer).

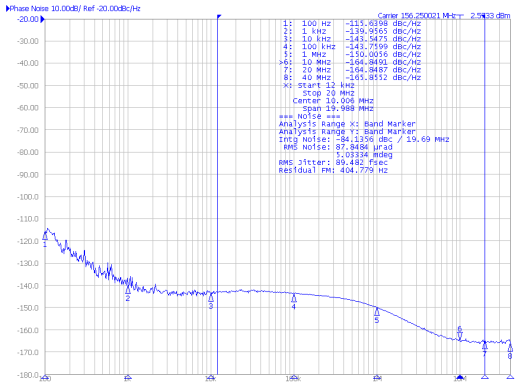
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5.19 Additional Reliability and Qualification

PARAMETER	CONDITION / TEST METHOD
Mechanical Shock	MIL-STD-202, Method 213
Mechanical Vibration	MIL-STD-202, Method 204
Moisture Sensitivity Level	J-STD-020, MSL3

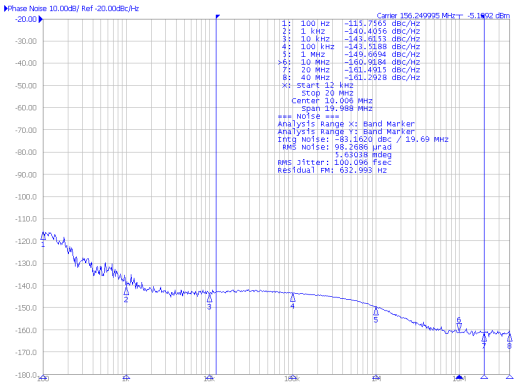
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5.20 Typical Characteristics



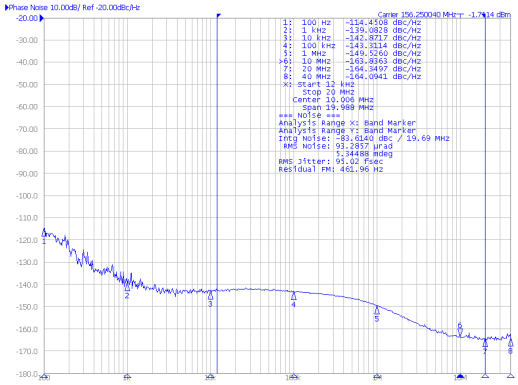
PLL Bandwidth = 400kHz
Integer-N PLL
VCO Frequency = 5GHz
Output Divider = 32

図 5-1. Closed-Loop Phase Noise of LVPECL Differential Output at 156.25MHz



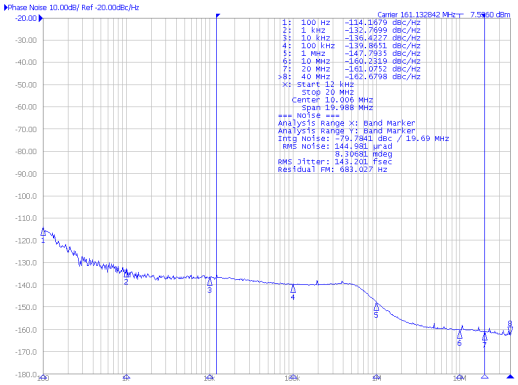
PLL Bandwidth = 400kHz
Integer-N PLL
VCO Frequency = 5GHz
Output Divider = 32

図 5-2. Closed-Loop Phase Noise of LVDS Differential Output at 156.25MHz



PLL Bandwidth = 400kHz
Integer-N PLL
VCO Frequency = 5GHz
Output Divider = 32

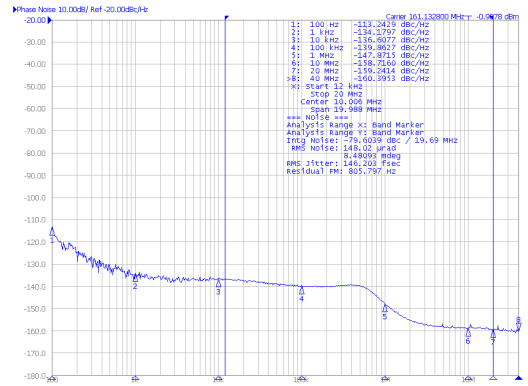
図 5-3. Closed-Loop Phase Noise of HCSL Differential Output at 156.25MHz



PLL Bandwidth = 400kHz
Fractional-N PLL
VCO Frequency = 5.15625GHz
Output Divider = 32

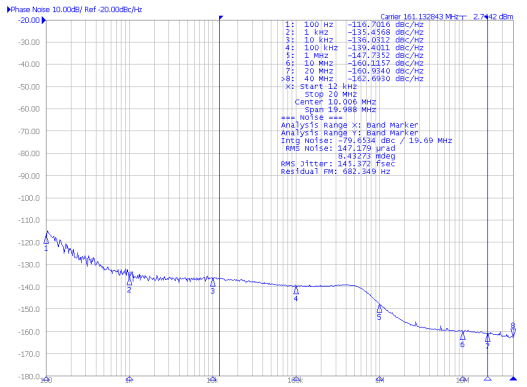
図 5-4. Closed-Loop Phase Noise of LVPECL Differential Output at 161.1328125MHz

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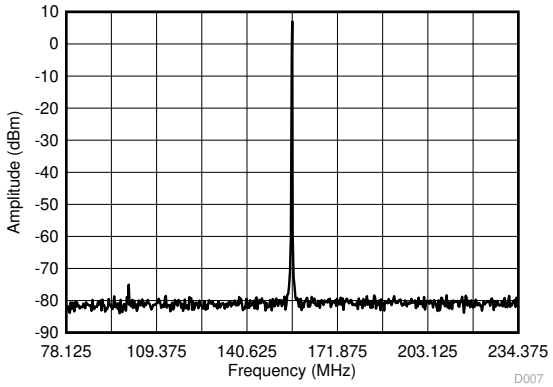
PLL Bandwidth = 400kHz
Fractional-N PLL
VCO Frequency = 5.15625GHz
Output Divider = 32

図 5-5. Closed-Loop Phase Noise of LVDS Differential Output at 161.1328125MHz



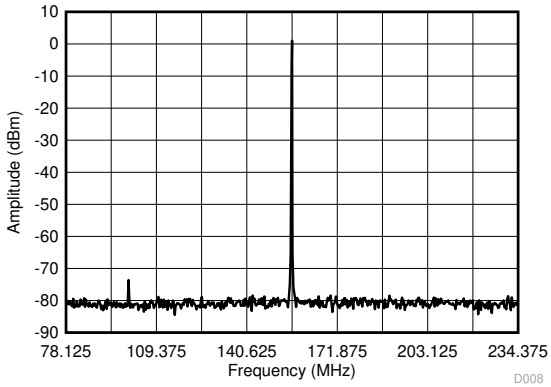
PLL Bandwidth = 400kHz
Fractional-N PLL
VCO Frequency = 5.15625GHz
Output Divider = 32

図 5-6. Closed-Loop Phase Noise of HCSL Differential Output at 161.1328125MHz



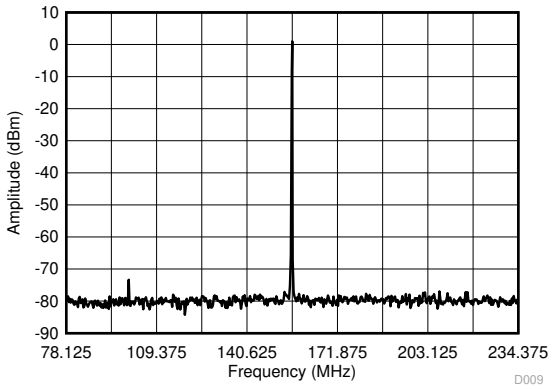
PLL Bandwidth = 400kHz
Integer-N PLL
VCO Frequency = 5GHz
Output Divider = 32

図 5-7. 156.25 ± 78.125MHz LVPECL Differential Output Spectrum



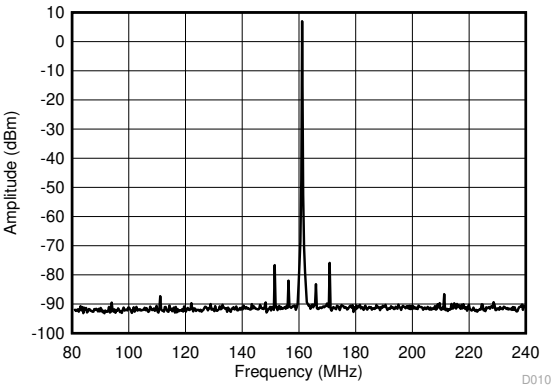
PLL Bandwidth = 400kHz
Integer-N PLL
VCO Frequency = 5GHz
Output Divider = 32

図 5-8. 156.25 ± 78.125MHz LVDS Differential Output Spectrum



PLL Bandwidth = 400kHz
Integer-N PLL
VCO Frequency = 5GHz
Output Divider = 32

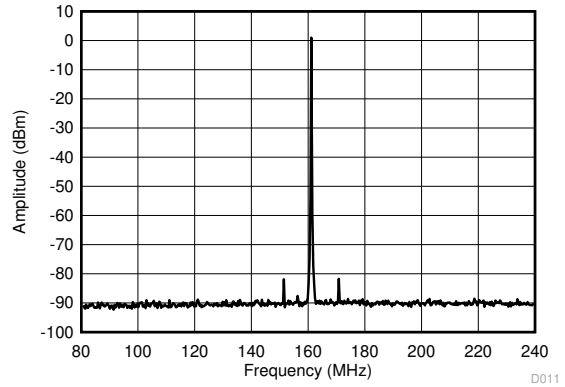
図 5-9. 156.25 ± 78.125MHz HCSL Differential Output Spectrum



PLL Bandwidth = 400kHz
Fractional-N PLL
VCO Frequency = 5.15625GHz
Output Divider = 32

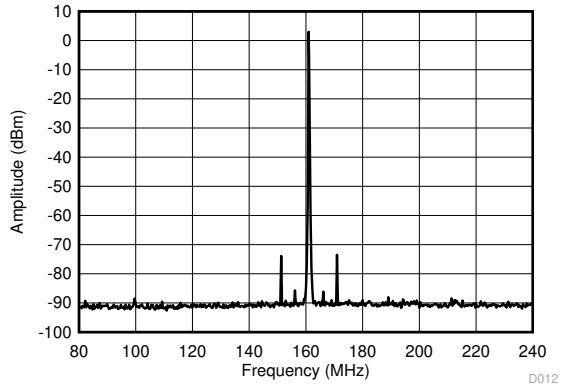
図 5-10. 161.1328125 ± 80.56640625MHz LVPECL Differential Output Spectrum

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PLL Bandwidth = 400kHz VCO Frequency = 5.15625GHz
Fractional-N PLL Output Divider = 32

図 5-11. 161.1328125 ± 80.56640625MHz LVDS Output Spectrum



PLL Bandwidth = 400kHz VCO Frequency = 5.15625GHz
Fractional-N PLL Output Divider = 32

図 5-12. 161.1328125 ± 80.56640625MHz HCSL Output Spectrum

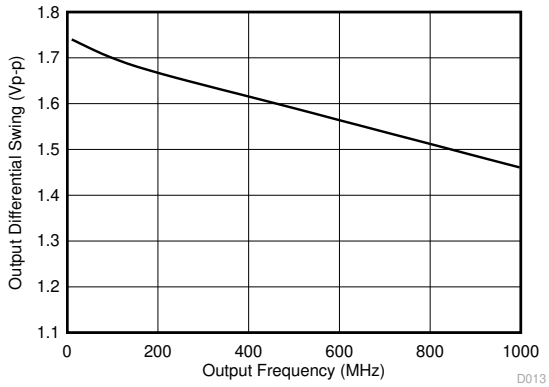


図 5-13. LVPECL Differential Output Swing vs Frequency

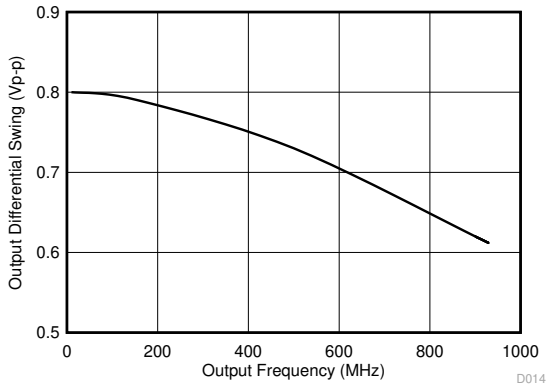


図 5-14. LVDS Differential Output Swing vs Frequency

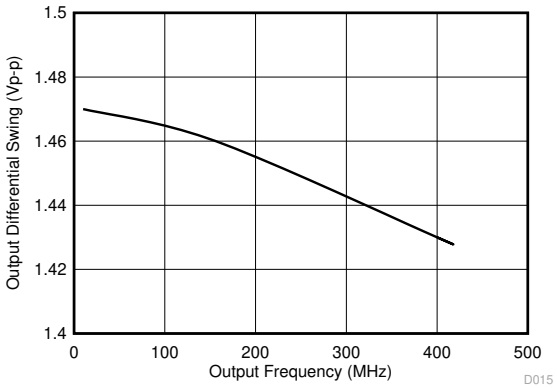


図 5-15. HCSL Differential Output Swing vs Frequency

6 Parameter Measurement Information

6.1 Device Output Configurations

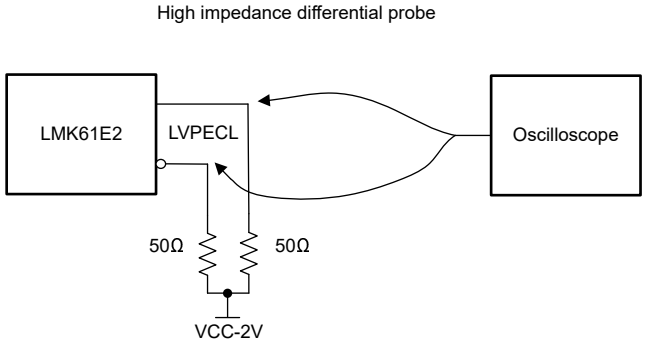


図 6-1. LVPECL Output DC Configuration During Device Test

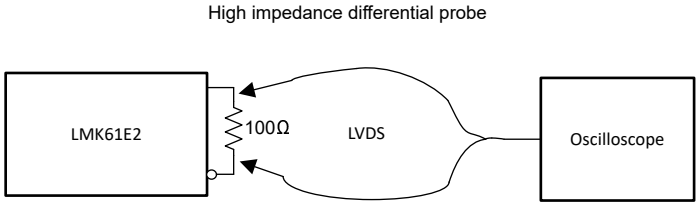


図 6-2. LVDS Output DC Configuration During Device Test

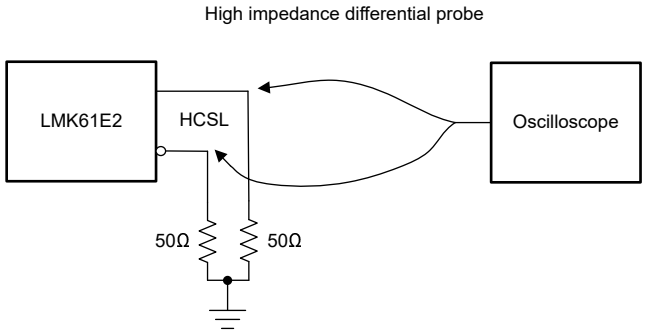


図 6-3. HCSL Output DC Configuration During Device Test

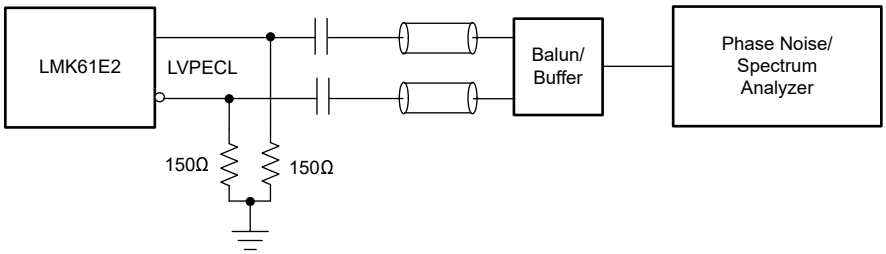


図 6-4. LVPECL Output AC Configuration During Device Test

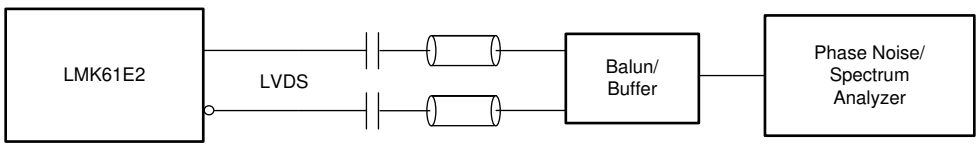


図 6-5. LVDS Output AC Configuration During Device Test

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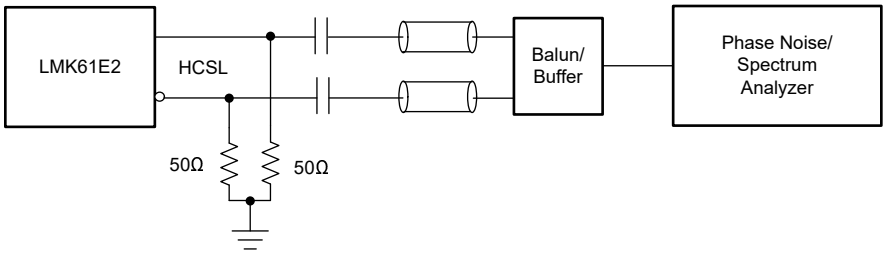


図 6-6. HCSL Output AC Configuration During Device Test

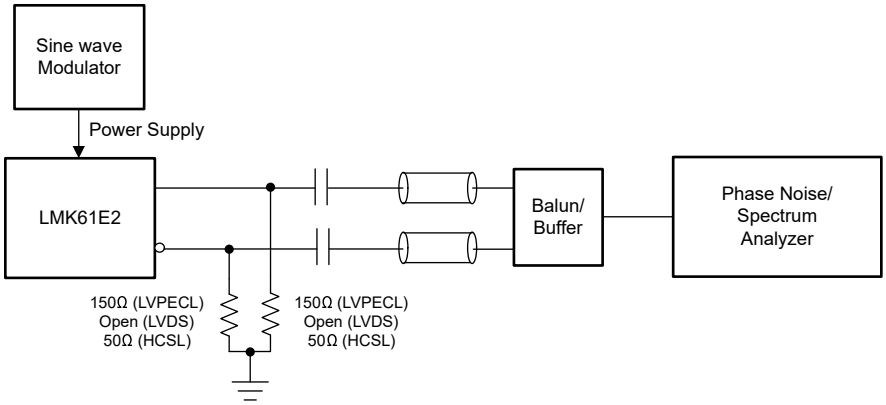


図 6-7. PSRR Test Setup

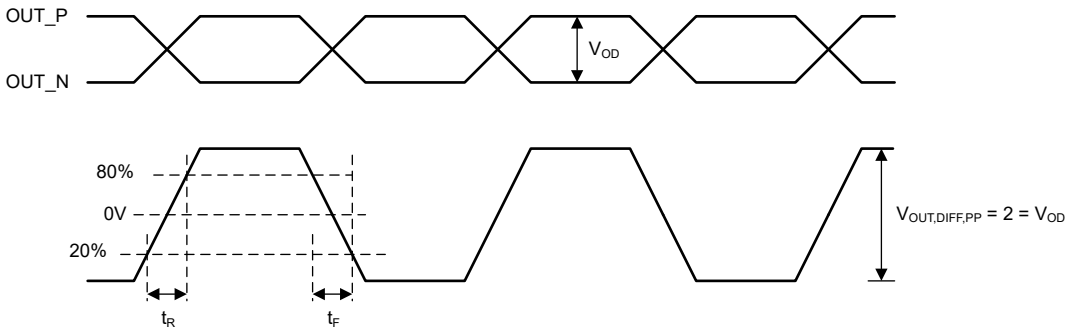


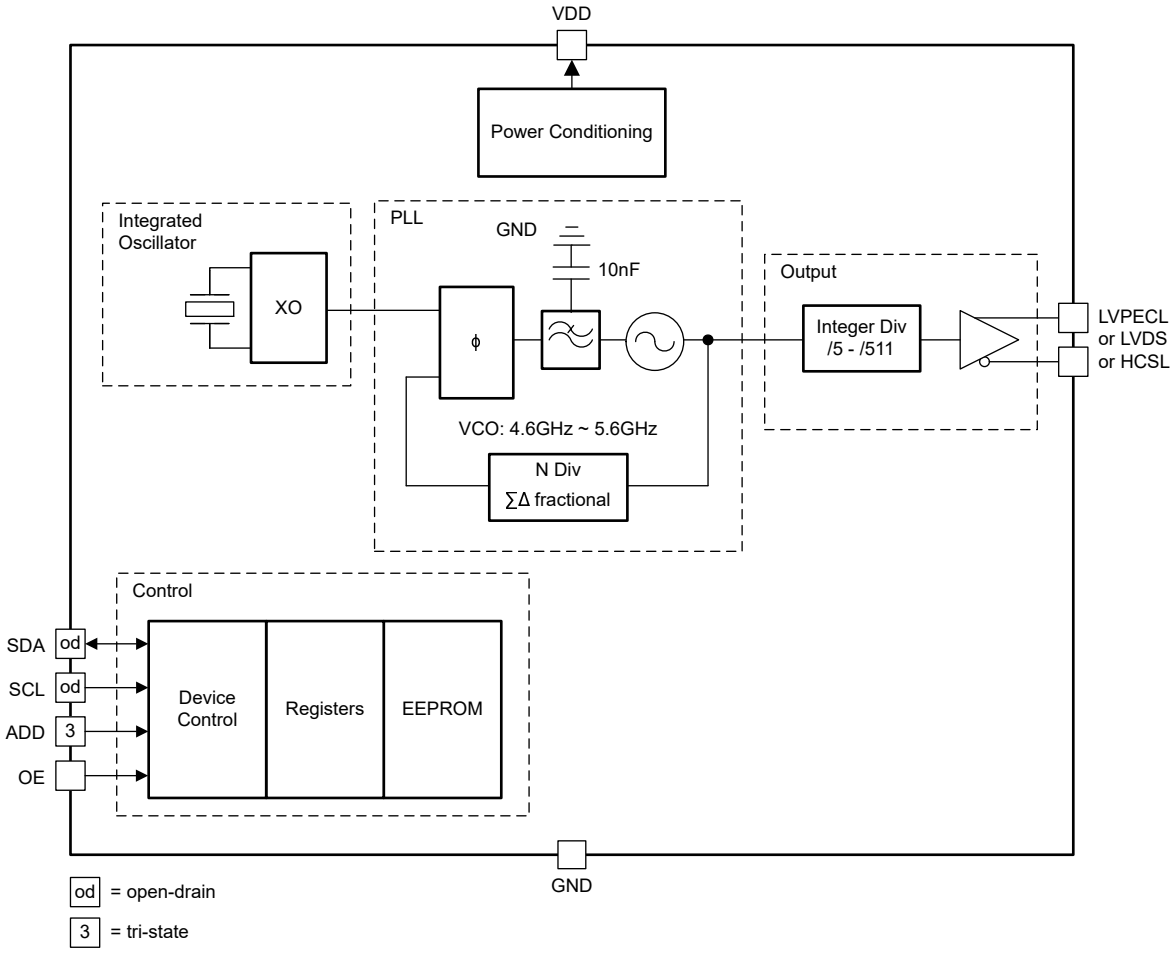
図 6-8. Differential Output Voltage and Rise/Fall Time

7 Detailed Description

7.1 Overview

The LMK61E2 is a programmable oscillator that generates commonly used reference clocks with less than 200-fs RMS maximum random jitter in integer PLL mode and less than 300-fs RMS maximum random jitter in fractional PLL mode.

7.2 Functional Block Diagram



注

Control blocks are compatible with 1.8, 2.5, or 3.3V I/O voltage levels.

7.3 Feature Description

7.3.1 Device Block-Level Description

The LMK61E2 comprises of an integrated oscillator that includes a 50MHz crystal, a fractional PLL with integrated VCO that supports a frequency range of 4.6GHz to 5.6GHz. The PLL block consists of a phase frequency detector (PFD), charge pump, integrated passive loop filter, a feedback divider that can support both integer and fractional values and a delta-sigma engine for noise suppression in fractional PLL mode. Completing the device is the combination of an integer output divider and a universal differential output buffer. The PLL is powered by on-chip low dropout (LDO) linear voltage regulators and the regulated supply network is partitioned such that the sensitive analog supplies are running from separate LDOs than the digital supplies which use dedicated LDO. The LDOs provide isolation to the PLL from any noise in the external power supply rail with a

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PSRR of better than –70 dBc at 50kHz to 1MHz ripple frequencies at 3.3V device supply. The device supports fine and coarse frequency margining by changing the settings of the integrated oscillator and the output divider respectively.

7.3.2 Device Configuration Control

The LMK61E2 supports I^2C programming interface where an I^2C host can update any device configuration after the device enables the host interface and the host writes a sequence that updates the device registers. Once the device configuration is set, the host can also write to the on-chip EEPROM for a new set of power-up defaults based on the configuration pin settings in the soft pin configuration mode.

7.3.3 Register File Reference Convention

図 7-1 shows the method that this document employs to refer to an individual register bit or a grouping of register bits. If a drawing or text references an individual bit the format is to specify the register number first and the bit number second. The LMK61E2 contains 38 registers that are 8 bits wide. The register addresses and the bit positions both begin with the number zero (0). A period separates the register address and bit address. The first bit in the register file is address 'R0.0' meaning that bit is located in Register 0 and is bit position 0. The last bit in the register file is address 'R72.7' referring to the 8th bit of register address 72 (the 73rd register in the device). 図 7-1 also lists specific bit positions as a number contained within a box. A box with the register address encloses the group of boxes that represent the bits relevant to the specific device circuitry in context.

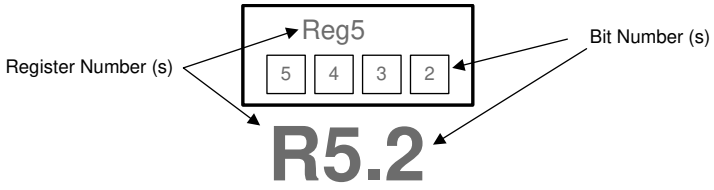


図 7-1. LMK61E2 Register Reference Format

7.3.4 Configuring the PLL

The PLL in LMK61E2 can be configured to accommodate various output frequencies either through I^2C programming interface or in the absence of programming, the PLL defaults stored in EEPROM is loaded on power up. The PLL can be configured by setting the Reference Doubler, Integrated PLL Loop Filter, Feedback Divider, and Output Divider.

For the PLL to operate in closed-loop mode, the following condition in 式 1 has to be met.

$$F_{VCO} = F_{REF} \times D \times [(INT + NUM/DEN)] \quad (1)$$

where

- F_{VCO}: PLL/VCO Frequency (4.6GHz to 5.6GHz)
- F_{REF}: 50MHz reference input
- D: PLL input frequency doubler, 1=Disabled, 2=Enabled
- INT: PLL feedback divider integer value (12 bits, 1 to 4095)
- NUM: PLL feedback divider fractional numerator value (22 bits, 0 to 4194303)
- DEN: PLL feedback divider fractional denominator value (22 bits, 1 to 4194303)

The output frequency is related to the VCO frequency as given in 式 2.

$$F_{OUT} = F_{VCO} / OUTDIV \quad (2)$$

where

- OUTDIV: Output divider value (9 bits, 5 to 511)

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7.3.5 Integrated Oscillator

The integrated oscillator in LMK61E2 features programmable load capacitances that can be set to either operate at exactly the nominal oscillation frequency or operate at a fixed frequency offset from the nominal oscillation frequency. This is done by programming R16 and R17. More details on frequency margining are provided in *Fine Frequency Margining*.

7.3.6 Reference Doubler

The reference path has a frequency doubler that can be enabled by programming R34.5 = 1. Enabling the doubler allows a higher comparison frequency for the PLL and results in a 3dB reduction in the in-band phase noise at the output of the LMK61E2. Enabling the doubler also results in higher reference and phase detector spurs which is minimized by enabling the higher order components (R3, C3) of the loop filter and programmed to appropriate values. Disabling the doubler results in higher in-band phase noise on the device output than when the doubler is enabled but the reference and phase detector spurs is lower on the device output than when the doubler is enabled.

7.3.7 Phase Frequency Detector

The Phase Frequency Detector (PFD) of the PLL takes inputs from the reference path and the feedback divider output and produces an output that is dependent on the phase and frequency difference between the two inputs. The input frequency of the PFD is 50MHz when reference doubler is disabled, or 100MHz when reference doubler is enabled.

7.3.8 Feedback Divider (N)

The N divider of the PLL includes fractional compensation and can achieve any fractional denominator (DEN) from 1 to 4,194,303. The integer portion, INT, is the whole part of the N divider value and the fractional portion, NUM / DEN, is the remaining fraction. INT, NUM, and DEN are programmed in R25, R26, R27, R28, R29, R30, R31, and R32. The total programmed N divider value, N, is determined by: N = INT + NUM / DEN. The output of the N divider sets the PFD frequency to the PLL and must equal 50MHz, when reference doubler is disabled, or 100MHz, when reference doubler is enabled.

7.3.9 Fractional Circuitry

The delta signal modulator is a key component of the fractional circuitry and is involved in noise shaping for better phase noise and spurs in the band of interest. The order of the delta sigma modulator is selectable between integer mode and third order, for fractional PLL mode, and can be programmed in R33[1-0]. Dithering can be programmed in R33[3-2] and must be disabled for integer PLL mode and set to weak for fractional PLL mode.

7.3.10 Charge Pump

The PLL has charge pump slices of 1.6mA, to be used when PLL is set to fractional mode, or 6.4mA, to be used when PLL is set to integer mode. These slices can be selected by programming R34[3-0]. When PLL is set to fractional mode, a phase shift needs to be introduced to maintain a linear response and verify consistent performance across operating conditions and a value of 0x2 must be programmed in R35[6-4]. When PLL is set to integer mode, a value of 0x0 must be programmed in R35[6-4].

7.3.11 Loop Filter

The LMK61E2 features a fully integrated loop filter for the PLL and supports programmable loop bandwidth from 100kHz to 1MHz. The loop filter components, R2, C1, R3, and C3 can be configured by programming R36, R37, R38, and R39 respectively. The LMK61E2 features a fixed value of C2 of 10nF. When PLL is configured in the fractional mode, R35.2 must be set to 1. When reference doubler is disabled for integer mode PLL, R35.2 must be set to 0 and R38[6-0] must be set to 0x00. When reference doubler is enabled for integer mode PLL, R35.2 must be set to 1 and R38 and R39 are written with the appropriate values. 図 7-2 shows the loop filter structure of the PLL. Set the PLL to best possible bandwidth to minimize output jitter. TI provides the WEBENCH® Clock Architect Tool that makes selecting the right loop filter components simple.

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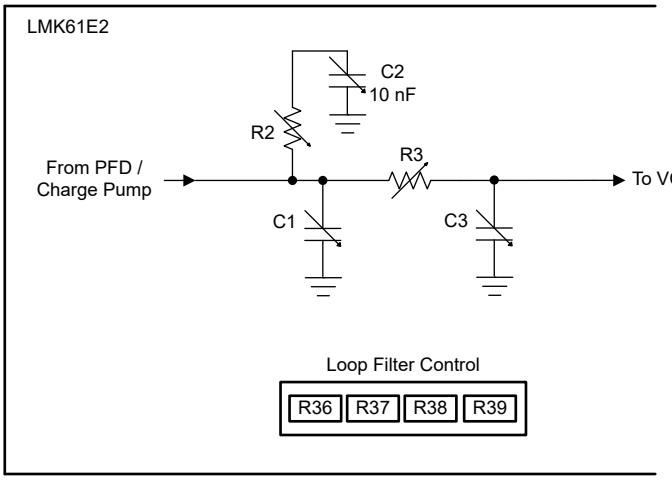


図 7-2. Loop Filter Structure of PLL

7.3.12 VCO Calibration

The PLL in LMK61E2 is comprised of LC VCO that is designed using high-Q monolithic inductors to oscillate between 4.6GHz and 5.6GHz and has low-phase noise characteristics. The VCO must be calibrated to verify that the clock outputs deliver optimal phase noise performance. Fundamentally, a VCO calibration establishes an optimal operating point within the tuning range of the VCO. Setting R72.1 to 1 causes a VCO recalibration and is necessary after device reconfiguration. VCO calibration automatically occurs on device power up.

7.3.13 High-Speed Output Divider

The high-speed output divider supports divide values of 5 to 511 and are programmed in R22 and R23. The output divider also supports coarse frequency margining that can initiate as low as a 5% change in the output frequency.

7.3.14 High-Speed Clock Output

The clock output can be configured as LVPECL, LVDS, or HCSL by programming R21[1-0]. Interfacing to LVPECL, LVDS, or HCSL receivers are done either with direct coupling or with AC-coupling capacitor as shown in 図 6-1 – 図 6-6.

The LVDS output structure has integrated 125Ω termination between each side (P and N) of the differential pair. The HCSL output structure is open drain and can be DC or AC coupled to HCSL receivers with appropriate termination scheme. The LVPECL output structure is an emitter follower requiring external termination.

7.3.15 Device Status

The PLL loss of lock and PLL calibration status can be monitored by reading R66[1-0]. These bits represent a logic-high interrupt output and are self-cleared once the readback is complete.

7.3.15.1 Loss of Lock

The PLL loss of lock detection circuit is a digital circuit that detects any frequency error, even a single cycle slip. Loss of lock can occur when an incorrect PLL configuration is programmed or the VCO has not been recalibrated.

7.4 Device Functional Modes

7.4.1 Interface and Control

The host (DSP, Microcontroller, FPGA, and so forth) configures and monitors the LMK61E2 through the I^2C port. The host reads and writes to a collection of control and status bits called the register map. The device blocks can be controlled and monitored through a specific grouping of bits located within the register file. The host controls and monitors certain device Wide critical parameters directly through register control and status bits. In the

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absence of the host, the LMK61E2 can be configured to operate from the on-chip EEPROM. The EEPROM array is automatically copied to the device registers upon power up. The user has the flexibility to rewrite the contents of EEPROM from the SRAM up to a 100 times.

Within the device registers, there are certain bits that have read or write access. Other bits are read-only (an attempt to write to a read-only bit does not change the state of the bit). Certain device registers and bits are reserved, meaning that the registers must not be changed from the default reset state. 図 7-3 shows interface and control blocks within LMK61E2 and the arrows refer to read access from and write access to the different embedded memories (EEPROM, SRAM).

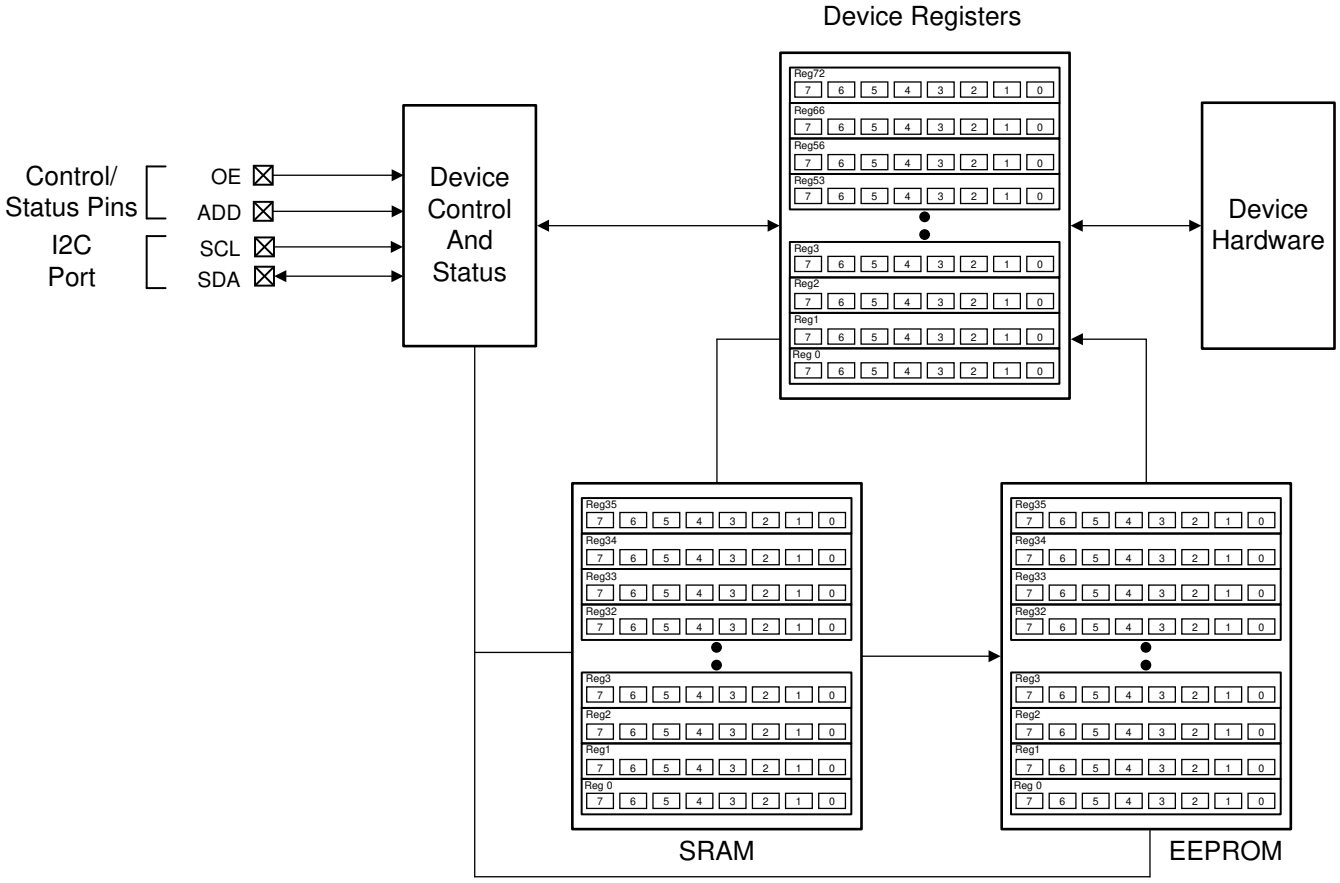


図 7-3. LMK61E2 Interface and Control Block

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7.5 Programming

7.5.1 I²C Serial Interface

The I²C port on the LMK61E2 works as a target device and supports both the 100kHz standard mode and 400kHz fast mode operations. Fast mode imposes a glitch tolerance requirement on the control signals. Therefore, the input receivers ignore pulses of less than 50ns duration. The I²C timing is given in *I²C-Compatible Interface Characteristics (SDA, SCL)*. The timing diagram is given in 図 7-4.

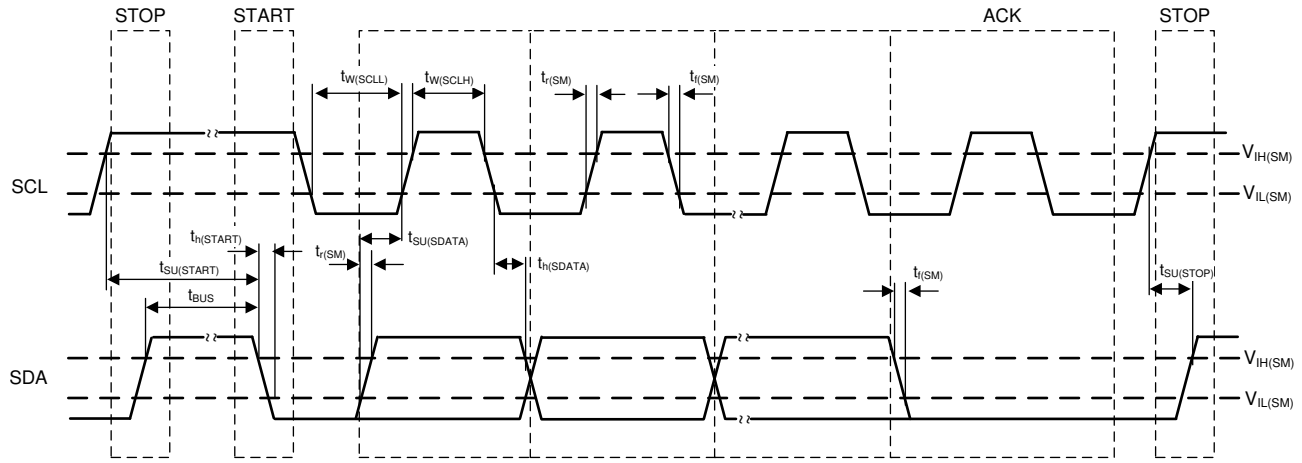


図 7-4. I²C Timing Diagram

In an I²C bus system, the LMK61E2 acts as a target device and is connected to the serial bus (data bus SDA and lock bus SCL). These are accessed using a 7-bit target address transmitted as part of an I²C packet. Only the device with a matching target address responds to subsequent I²C commands. In soft pin mode, the LMK61E2 allows up to three unique target devices to occupy the I²C bus based on the pin strapping of ADD (tied to VDD, GND, or left open). The device target address is 10110xx (the two LSBs are determined by the ADD pin).

During the data transfer through the I²C interface, one clock pulse is generated for each data bit transferred. The data on the SDA line must be stable during the high period of the clock. The high or low state of the data line can change only when the clock signal on the SCL line is low. The start data transfer condition is characterized by a high-to-low transition on the SDA line while SCL is high. The stop data transfer condition is characterized by a low-to-high transition on the SDA line while SCL is high. The start and stop conditions are always initiated by the controller. Every byte on the SDA line must be eight bits long. Each byte must be followed by an acknowledge bit and bytes are sent MSB first. The I²C register structure of the LMK61E2 is shown in 図 7-5.

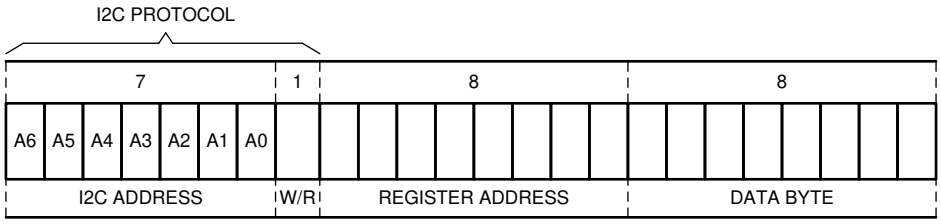


図 7-5. I²C Register Structure

The acknowledge bit (A) or non-acknowledge bit (A') is the 9th bit attached to any 8-bit data byte and is always generated by the receiver to inform the transmitter that the byte has been received (when A = 0) or not (when A' = 0). A = 0 is done by pulling the SDA line low during the 9th clock pulse and A' = 0 is done by leaving the SDA line high during the 9th clock pulse.

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The I2C controller initiates the data transfer by asserting a start condition which initiates a response from all target devices connected to the serial bus. Based on the 8-bit address byte sent by the controller over the SDA line (consisting of the 7-bit target address (MSB first) and an R/W' bit), the device whose address corresponds to the transmitted address responds by sending an acknowledge bit. All other devices on the bus remain idle while the selected device waits for data transfer with the controller.

After the data transfer has occurred, stop conditions are established. In write mode, the controller asserts a stop condition to end data transfer during the 10th clock pulse following the acknowledge bit for the last data byte from the target. In read mode, the controller receives the last data byte from the target but does not pull SDA low during the 9th clock pulse. This is known as a non-acknowledge bit. By receiving the non-acknowledge bit, the target knows the data transfer is finished and enters the idle mode. The controller then takes the data line low during the low period before the 10th clock pulse, and high during the 10th clock pulse to assert a stop condition. A generic transaction is shown in 図 7-6.

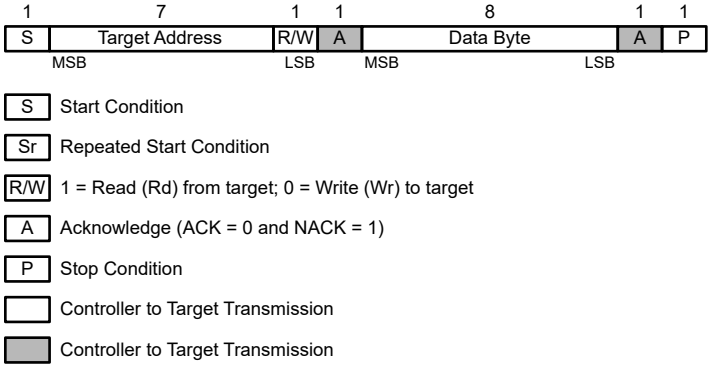


図 7-6. Generic Programming Sequence

The LMK61E2 I2C interface supports *Block Register Write/Read*, *Read/Write SRAM*, and *Read/Write EEPROM* operations. For *Block Register Write/Read* operations, the I2C controller can individually access addressed registers that are made of an 8-bit data byte. The offset of the indexed register is encoded in the register address, as described in 表 7-1.

表 7-1. Target Address Byte

DEVICE	A6	A5	A4	A3	A2	ADD pin	R/ $\overline{W}$
LMK61E2	1	0	1	1	0	0x0, 0x1 or 0x3	1/0

7.5.2 Block Register Write

The I2C *Block Register Write* transaction is illustrated in 図 7-7 and consists of the following sequence.

1. Controller issues a Start Condition.
2. Controller writes the 7-bit Target Address following by a Write bit.
3. Controller writes the 8-bit Register address as the CommandCode of the programming sequence.
4. Controller writes one or more data bytes each of which must be acknowledged by the target. The target increments the internal register address after each byte.
5. Controller issues a Stop Condition to terminate the transaction.

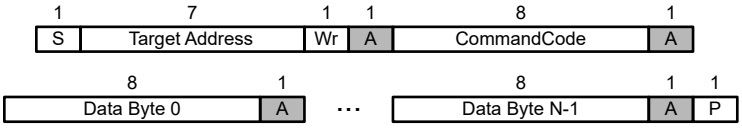


図 7-7. Block Register Write Programming Sequence

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7.5.3 Block Register Read

The I²C *Block Register Read* transaction is illustrated in 図 7-8 and consists of the following sequence.

1. Controller issues a Start Condition.
2. Controller writes the 7-bit Target Address followed by a Write bit.
3. Controller writes the 8-bit Register address as the CommandCode of the programming sequence.
4. Controller issues a Repeated Start Condition.
5. Controller writes the 7-bit Target Address following by a Read bit.
6. Target returns one or more data bytes as long as the Controller continues to acknowledge them. The target increments the internal register address after each byte.
7. Controller issues a Stop Condition to terminate the transaction.

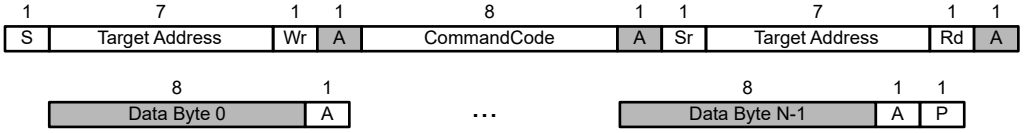


図 7-8. Block Register Read Programming Sequence

7.5.4 Write SRAM

The on-chip SRAM is a volatile, shadow memory array used to temporarily store register data, and is intended only for programming the non-Volatile EEPROM. The SRAM has the identical data format as the EEPROM map. The register configuration data can be transferred to the SRAM array through special memory access registers in the register map. To successfully program the SRAM, the complete base array and at least one page must be written. The following details the programming sequence to transfer the device registers into the SRAM.

1. Program the device registers to match a desired setting.
2. Write a 1 to R49.6. This verifies that the device registers are copied to the SRAM.

The SRAM can also be written with particular values according to the following programming sequence.

1. Write the SRAM address in R51.
2. Write the desired data byte in R53 in the same I²C transaction and this data byte is written to the address specified in the step above. Any additional access that is part of the same transaction cause the SRAM address to be incremented and a write takes place to the next SRAM address. Access to SRAM terminates at the end of current I²C transaction.

注

Incrementing SRAM addresses incorrectly is possible when 2 successive accesses are made to R51.

7.5.5 Write EEPROM

The on-chip EEPROM is a non-Volatile memory array used to permanently store register data for a custom device start-up configuration setting to initialize registers upon power up or POR. The EEPROM is comprised of bits shown in the EEPROM Map. The transfer must first happen to the SRAM and then to the EEPROM. During *EEPROM write*, R49.2 is a 1 and the EEPROM contents cannot be accessed. The following details the programming sequence to transfer the entire contents of SRAM to EEPROM.

1. Make sure the *Write SRAM* procedure (Write SRAM) is done to commit the register settings to the SRAM with start-up configurations intended for programming to the EEPROM.
2. Write 0xBE to R56. This provides basic protection from inadvertent programming of EEPROM.
3. Write a 1 to R49.0. This programs the entire SRAM contents to EEPROM. Once completed, the contents in R48 increment by 1. R48 contains the total number of EEPROM programming cycles that are successfully completed.

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4. Write 0x00 to R56 to protect against inadvertent programming of EEPROM.

7.5.6 Read SRAM

The contents of the SRAM can be read out, one word at a time, starting with that of the requested address. Following details the programming sequence for an SRAM read by address.

1. Write the SRAM address in R51.
2. The SRAM data located at the address specified in the step above can be obtained by reading R53 in the same I^2C transaction. Any additional access that is part of the same transaction causes the SRAM address to be incremented and a read takes place of the next SRAM address. Access to SRAM terminates at the end of current I^2C transaction.

注

Incrementing the SRAM address incorrectly is possible when 2 successive accesses are made to R51.

7.5.7 Read EEPROM

The contents of the EEPROM can be read out, one word at a time, starting with that of the requested address. Following details the programming sequence for an EEPROM read by address.

1. Write the EEPROM address in R51.
2. The EEPROM data located at the address specified in the step above can be obtained by reading R52 in the same I^2C transaction. Any additional access that is part of the same transaction causes the EEPROM address to be incremented and a read takes place of the next EEPROM address. Access to EEPROM terminates at the end of current I^2C transaction.

注

The EEPROM address can be incremented incorrectly when 2 successive accesses are made to R51.

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7.6 EEPROM Map

Any bit that is labeled as RESERVED must be written with a 0.

Byte #	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED
1	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED
2	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED
3	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED
4	NVMSCRC[7]	NVMSCRC[6]	NVMSCRC[5]	NVMSCRC[4]	NVMSCRC[3]	NVMSCRC[2]	NVMSCRC[1]	NVMSCRC[0]
5	NVMCNT[7]	NVMCNT[6]	NVMCNT[5]	NVMCNT[4]	NVMCNT[3]	NVMCNT[2]	NVMCNT[1]	NVMCNT[0]
6	1	RESERVED	RESERVED	RESERVED	RESERVED	1	RESERVED	RESERVED
7	RESERVED	RESERVED	1	RESERVED	RESERVED	RESERVED	RESERVED	1
8	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED
9	TARGETADR[7]	TARGETADR[6]	TARGETADR[5]	TARGETADR[4]	TARGETADR[3]	RESERVED	RESERVED	RESERVED
10	EEREV[7]	EEREV[6]	EEREV[5]	EEREV[4]	EEREV[3]	EEREV[2]	EEREV[1]	EEREV[0]
11	RESERVED	PLL_PDN	RESERVED	RESERVED	RESERVED	RESERVED	AUTOSTRT	RESERVED
14	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	1	RESERVED	1
15	RESERVED	XO_CAPCTRL[1]	XO_CAPCTRL[0]	XO_CAPCTRL[9]	XO_CAPCTRL[8]	XO_CAPCTRL[7]	XO_CAPCTRL[6]	XO_CAPCTRL[5]
16	XO_CAPCTRL[4]	XO_CAPCTRL[3]	XO_CAPCTRL[2]	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED
19	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	OUT_SEL[2]
20	OUT_SEL[1]	OUT_SEL[0]	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED
21	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED
22	PLL_NDIV[11]	PLL_NDIV[10]	PLL_NDIV[9]	PLL_NDIV[8]	PLL_NDIV[7]	PLL_NDIV[6]	PLL_NDIV[5]	PLL_NDIV[4]
23	PLL_NDIV[3]	PLL_NDIV[2]	PLL_NDIV[1]	PLL_NDIV[0]	PLL_NUM[21]	PLL_NUM[20]	PLL_NUM[19]	PLL_NUM[18]
24	PLL_NUM[17]	PLL_NUM[16]	PLL_NUM[15]	PLL_NUM[14]	PLL_NUM[13]	PLL_NUM[12]	PLL_NUM[11]	PLL_NUM[10]
25	PLL_NUM[9]	PLL_NUM[8]	PLL_NUM[7]	PLL_NUM[6]	PLL_NUM[5]	PLL_NUM[4]	PLL_NUM[3]	PLL_NUM[2]
26	PLL_NUM[1]	PLL_NUM[0]	PLL_DEN[21]	PLL_DEN[20]	PLL_DEN[19]	PLL_DEN[18]	PLL_DEN[17]	PLL_DEN[16]
27	PLL_DEN[15]	PLL_DEN[14]	PLL_DEN[13]	PLL_DEN[12]	PLL_DEN[11]	PLL_DEN[10]	PLL_DEN[9]	PLL_DEN[8]
28	PLL_DEN[7]	PLL_DEN[6]	PLL_DEN[5]	PLL_DEN[4]	PLL_DEN[3]	PLL_DEN[2]	PLL_DEN[1]	PLL_DEN[0]
29	PLL_ DTHRMODE[1]	PLL_DTHRMODE[0]	PLL_ORDER[1]	PLL_ORDER[0]	RESERVED	RESERVED	PLL_D	PLL_CP[3]
30	PLL_CP[2]	PLL_CP[1]	PLL_CP[0]	PLL_CP_PHASE_ SHIFT[2]	PLL_CP_PHASE_ SHIFT[1]	PLL_CP_PHASE_ SHIFT[0]	PLL_ENABLE_ C3[2]	PLL_ENABLE_ C3[1]
31	PLL_ENABLE_ C3[0]	PLL_LF_R2[7]	PLL_LF_R2[6]	PLL_LF_R2[5]	PLL_LF_R2[4]	PLL_LF_R2[3]	PLL_LF_R2[2]	PLL_LF_R2[1]

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Byte #	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
32	PLL_LF_R2[0]	PLL_LF_C1[2]	PLL_LF_C1[1]	PLL_LF_C1[0]	PLL_LF_R3[6]	PLL_LF_R3[5]	PLL_LF_R3[4]	PLL_LF_R3[3]
33	PLL_LF_R3[2]	PLL_LF_R3[1]	PLL_LF_R3[0]	PLL_LF_C3[2]	PLL_LF_C3[1]	PLL_LF_C3[0]	RESERVED	RESERVED
34	RESERVED	OUT_DIV[8]	OUT_DIV[7]	OUT_DIV[6]	OUT_DIV[5]	OUT_DIV[4]	OUT_DIV[3]	OUT_DIV[2]
35	OUT_DIV[1]	OUT_DIV[0]	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED

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8 Register Map

The default/reset values for each register is specified for LMK61E2.

Name	Addr	Reset	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
VNDRID_BY1	0	0x10	VNDRID[15:8]							
VNDRID_BY0	1	0x0B	VNDRID[7:0]							
PRODID	2	0x33	PRODID[7:0]							
REVID	3	0x00	REVID[7:0]							
TARGETADR	8	0xB0	TARGETADR[7:1]							RESERVED
EEREV	9	0x00	EEREV[7:0]							
DEV_CTL	10	0x01	RESERVED	PLL_PDN	RESERVED				ENCAL	AUTOSTRT
XO_CAPCTRL_BY1	16	0x00	RESERVED						XO_CAPCTRL[1:0]	
XO_CAPCTRL_BY0	17	0x80	XO_CAPCTRL[9:2]							
DIFFCTL	21	0x01	DIFF_OUT_PD	RESERVED					OUT_SEL[1:0]	
OUTDIV_BY1	22	0x00	RESERVED							OUT_DIV[8]
OUTDIV_BY0	23	0x20	OUT_DIV[7:0]							
PLL_NDIV_BY1	25	0x00	RESERVED				PLL_NDIV[11:8]			
PLL_NDIV_BY0	26	0x32	PLL_NDIV[7:0]							
PLL_FRACNUM_BY2	27	0x00	RESERVED		PLL_NUM[21:16]					
PLL_FRACNUM_BY1	28	0x00	PLL_NUM[15:8]							
PLL_FRACNUM_BY0	29	0x00	PLL_NUM[7:0]							
PLL_FRACDEN_BY2	30	0x00	RESERVED		PLL_DEN[21:16]					
PLL_FRACDEN_BY1	31	0x00	PLL_DEN[15:8]							
PLL_FRACDEN_BY0	32	0x01	PLL_DEN[7:0]							
PLL_MASHCTRL	33	0x0C	RESERVED				PLL_DTHRMODE[1:0]		PLL_ORDER[1:0]	
PLL_CTRL0	34	0x28	RESERVED		PLL_D	RESERVED	PLL_CP[3:0]			
PLL_CTRL1	35	0x03	RESERVED	PLL_CP_PHASE_SHIFT[2:0]			RESERVED	PLL_ENABLE_C3[2:0]		
PLL_LF_R2	36	0x28	PLL_LF_R2[7:0]							

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Name	Addr	Reset	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
PLL_LF_C1	37	0x00	RESERVED					PLL_LF_C1[2:0]		
PLL_LF_R3	38	0x00	RESERVED	PLL_LF_R3[6:0]						
PLL_LF_C3	39	0x00	RESERVED					PLL_LF_C3[2:0]		
PLL_CALCTRL	42	0x09	RESERVED				PLL_CLSDWAIT[1:0]		PLL_VCOWAIT[1:0]	
NVMSCRC	47	0x00	NVMSCRC[7:0]							
NVMCNT	48	0x00	NVMCNT[7:0]							
NVMCTL	49	0x10	RESERVED	REGCOMMIT	NVMCRCERR	NVMAUTOCRC	NVMCOMMIT	NVMBUSY	NVMERASE	NVMPROG
NVMLCRC	50	0x00	NVMLCRC[7:0]							
MEMADR	51	0x00	RESERVED	MEMADR[6:0]						
NVMDAT	52	0x00	NVMDAT[7:0]							
RAMDAT	53	0x00	RAMDAT[7:0]							
NVMUNLK	56	0x00	NVMUNLK[7:0]							
INT_LIVE	66	0x00	RESERVED						LOL	CAL
SWRST	72	0x00	RESERVED						SWR2PLL	RESERVED

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8.1 Register Descriptions

8.1.1 VNDRID_BY1 Register; R0

VNDRID_BY1 and VNDRID_BY0 registers are used to store the unique 16-bit Vendor Identification number assigned to I^{2}C vendors.

Bit #	Field	Type	Reset	EEPROM	Description
[7:0]	VNDRID[15:8]	R	0x10	N	Vendor Identification Number Byte 1.

8.1.2 VNDRID_BY0 Register; R1

VNDRID_BY1 and VNDRID_BY0 registers are used to store the unique 16-bit Vendor Identification number assigned to I^{2}C vendors.

Bit #	Field	Type	Reset	EEPROM	Description
[7:0]	VNDRID[7:0]	R	0x0B	N	Vendor Identification Number Byte 0.

8.1.3 PRODID Register; R2

The Product Identification Number is a unique 8-bit identification number used to identify the LMK61E2.

Bit #	Field	Type	Reset	EEPROM	Description
[7:0]	PRODID[7:0]	R	0x33	N	Product Identification Number.

8.1.4 REVID Register; R3

The REVID register is used to identify the LMK61E2 mask revision.

Bit #	Field	Type	Reset	EEPROM	Description
[7:0]	REVID[7:0]	R	0x00	N	Device Revision Number. The Device Revision Number is used to identify the LMK61E2 mask-set revision used to fabricate this device.

8.1.5 TARGETADR Register; R8

The TARGETADR register reflects the 7-bit I^{2}C Target Address value initialized from on-chip EEPROM.

Bit #	Field	Type	Reset	EEPROM	Description	
[7:1]	TARGETADR[7:1]	R	0x58	Y	I^{2}C Target Address.This field holds the 7-bit Target Address used to identify this device during I^{2}C transactions. The two least significant bits of the address can be configured using ADD pin as shown.	
					TARGETADR[2:1]	**ADD pin**
					0 (0x0)	0
					1 (0x1)	Float
					2 (0x2)	1
[0]	RESERVED	-	-	N	Reserved.	

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8.1.6 EEREV Register; R9

The EEREV register provides an EEPROM image revision record. EEPROM Image Revision is automatically retrieved from EEPROM and stored in the EEREV register after a reset or after a EEPROM commit operation.

Bit #	Field	Type	Reset	EEPROM	Description
[7:0]	EEREV[7:0]	R	0x00	Y	EEPROM Image Revision ID

8.1.7 DEV_CTL Register; R10

The DEV_CTL register holds the control functions described in the following table.

Bit #	Field	Type	Reset	EEPROM	Description
[7]	RESERVED	-	0	Y	Reserved.
[6]	PLL_PDN	RW	0	Y	PLL Powerdown. The PLL_PDN bit determines whether PLL is automatically enabled and calibrated after a hardware reset. If the PLL_PDN bit is set to 1 during normal operation then PLL is disabled and the calibration circuit is reset. When PLL_PDN is then cleared to 0 PLL is re-enabled and the calibration sequence is automatically restarted.
					PLL_PDN / **Value**
					0 / PLL Enabled
					1 / PLL Disabled
[5:2]	RESERVED[5:2]	RW	0	Y	Reserved.
[1]	ENCAL	RWSC	0	N	Enable Frequency Calibration. Triggers PLL/VCO calibration on the PLL on 0 –> 1 transition of ENCAL. This bit is self-clearing and set to a 0 after PLL/VCO calibration is complete. In power up or software rest mode, AUTOSTRT takes precedence.
[0]	AUTOSTRT	RW	1	Y	Autostart. If AUTOSTRT is set to 1 the device automatically attempts to achieve lock and enable outputs after a device reset. A device reset can be triggered by the power-on-reset or by writing to the SWR2PLL bit. If AUTOSTRT is 0 then the device halts after the configuration phase, a subsequent write to set the AUTOSTRT bit to 1 triggers the PLL Lock sequence.

8.1.8 XO_CAPCTRL_BY1 Register; R16

XO Margining Offset Value bits[9:8]

Bit #	Field	Type	Reset	EEPROM	Description
[7:2]	RESERVED[5:0]	-	-	N	Reserved.
[1:0]	XO_CAPCTRL [1:0]	RW	0x0	Y	XO Offset Value bits [1:0]

8.1.9 XO_CAPCTRL_BY0 Register; R17

XO margining Offset Value bits[7:0]

Bit #	Field	Type	Reset	EEPROM	Description
[7:0]	XO_CAPCTRL [9:2]	RW	0x80	Y	XO Offset Value bits[9:2]

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8.1.10 DIFFCTL Register; R21

The DIFFCTL register provides control over Output.

Bit #	Field	Type	Reset	EEPROM	Description	
[7]	DIFF_OUT_PD	RW	0	N	Power down differential output buffer.	
[6:2]	RESERVED	-	-	N	Reserved.	
[1:0]	OUT_SEL[1:0]	RW	0x1	Y	Channel Output Driver Format Select. The OUT_SEL field controls the Channel Output Driver as shown below.	
					OUT_SEL	**OUTPUT OPERATION**
					0 (0x0)	Tri-State
					1 (0x1)	LVPECL
					2 (0x2)	LVDS
					3 (0x3)	HCSL

8.1.11 OUTDIV_BY1 Register; R22

The 9-bit output integer divider value is set by the OUTDIV_BY1 and OUTDIV_BY0 registers.

Bit #	Field	Type	Reset	EEPROM	Description	
[7:1]	RESERVED	RW	0x00	Y	Reserved.	
[0]	OUT_DIV[8]	RW	0	Y	Channel's Output Divider Byte 1 (Bit 8). The Channel Divider, OUT_DIV, is a 9-bit divider. The valid values for OUT_DIV range from 5 to 511 as shown below.	
					OUT_DIV	**DIVIDE RATIO**
					0-4	RESERVED
					5 (0x005)	5
					6 (0x006)	6
					7 (0x007)	7
					255 (0x0FF)	255
					256 (0x100)	256
					257 (0x101)	257
					...	...
					511 (0x1FF)	511

8.1.12 OUTDIV_BY0 Register; R23

The 9-bit output integer divider value is set by the OUTDIV_BY1 and OUTDIV_BY0 registers.

Bit #	Field	Type	Reset	EEPROM	Description
[7:0]	OUT_DIV[7:0]	RW	0x20	Y	Channel's Output Divider Byte 0 (Bits 7-0).

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8.1.13 PLL_NDIV_BY1 Register; R25

The 12-bit N integer divider value for PLL is set by the PLL_NDIV_BY1 and PLL_NDIV_BY0 registers.

Bit #	Field	Type	Reset	EEPROM	Description
[7:4]	RESERVED	-	-	N	Reserved.
[3:0]	PLL_NDIV[11:8]	RW	0x0	Y	PLL N Divider Byte 1. PLL Integer N Divider bits [11:8].

8.1.14 PLL_NDIV_BY0 Register; R26

The PLL_NDIV_BY0 register is described in the following table.

Bit #	Field	Type	Reset	EEPROM	Description
[7:0]	PLL_NDIV[7:0]	RW	0x32	Y	PLL N Divider Byte 0. PLL Integer N Divider bits [7:0].

8.1.15 PLL_FRACNUM_BY2 Register; R27

The 22-bit Fractional Divider Numerator value for PLL is set by registers PLL_FRACNUM_BY2, PLL_FRACNUM_BY1 and PLL_FRACNUM_BY0.

Bit #	Field	Type	Reset	EEPROM	Description
[7:6]	RESERVED	-	-	N	Reserved.
[5:0]	PLL_NUM[21:16]	RW	0x00	Y	PLL Fractional Divider Numerator Byte 2. Bits [21:16]

8.1.16 PLL_FRACNUM_BY1 Register; R28

The PLL_FRACNUM_BY1 register is described in the following table.

Bit #	Field	Type	Reset	EEPROM	Description
[7:0]	PLL_NUM[15:8]	RW	0x00	Y	PLL Fractional Divider Numerator Byte 1. Bits [15:8].

8.1.17 PLL_FRACNUM_BY0 Register; R29

The PLL_FRACNUM_BY0 register is described in the following table.

Bit #	Field	Type	Reset	EEPROM	Description
[7:0]	PLL_NUM[7:0]	RW	0x00	Y	PLL Fractional Divider Numerator Byte 0. Bits [7:0].

8.1.18 PLL_FRACDEN_BY2 Register; R30

The 22-bit Fractional Divider Denominator value for PLL is set by registers PLL_FRACDEN_BY2, PLL_FRACDEN_BY1 and PLL_FRACDEN_BY0.

Bit #	Field	Type	Reset	EEPROM	Description
[7:6]	RESERVED	-	-	N	Reserved.
[5:0]	PLL_DEN[21:16]	RW	0x00	Y	PLL Fractional Divider Denominator Byte 2. Bits [21:16].

8.1.19 PLL_FRACDEN_BY1 Register; R31

The PLL_FRACDEN_BY1 register is described in the following table.

Bit #	Field	Type	Reset	EEPROM	Description
[7:0]	PLL_DEN[15:8]	RW	0x00	Y	PLL Fractional Divider Denominator Byte 1. Bits [15:8].

8.1.20 PLL_FRACDEN_BY0 Register; R32

The PLL_FRACDEN_BY0 register is described in the following table.

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Bit #	Field	Type	Reset	EEPROM	Description
[7:0]	PLL_DEN[7:0]	RW	0x01	Y	PLL Fractional Divider Denominator Byte 0. Bits [7:0].

8.1.21 PLL_MASHCTRL Register; R33

The PLL_MASHCTRL register provides control of the fractional divider for PLL.

Bit #	Field	Type	Reset	EEPROM	Description	
[7:4]	RESERVED	-	-	N	Reserved.	
[3:2]	PLL_DTHRMODE[1:0]	RW	0x3	Y	Mash Engine dither mode control.	
					DITHERMODE	**Dither Configuration**
					0 (0x0)	Weak
					1 (0x1)	Reserved
					2 (0x2)	Reserved
					3 (0x3)	Dither Disabled
[1:0]	PLL_ORDER[1:0]	RW	0x0	Y	Mash Engine Order.	
					ORDER	**Order Configuration**
					0 (0x0)	Integer Mode Divider
					1 (0x1)	Reserved
					2 (0x2)	Reserved
					3 (0x3)	3rd order

8.1.22 PLL_CTRL0 Register; R34

The PLL_CTRL1 register provides control of PLL. The PLL_CTRL1 register fields are described in the following table.

Bit #	Field	Type	Reset	EEPROM	Description	
[7:6]	RESERVED	RW	0x0	Y	Reserved.	
[5]	PLL_D	RW	1	Y	PLL R Divider Frequency Doubler Enable. If PLL_D is 1 the R Divider Frequency Doubler is enabled.	
[4]	RESERVED	-	-	N	Reserved.	
[3:0]	PLL_CP[3:0]	RW	0x8	Y	PLL Charge Pump Current. Other combinations of PLL_CP[3:0] not in table below are reserved and not supported.	
					PLL_CP[3:0]	PLL Charge Pump Current
					4 (0x4)	1.6mA
					8 (0x8)	6.4mA

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8.1.23 PLL_CTRL1 Register; R35

The PLL_CTRL3 register provides control of PLL. The PLL_CTRL3 register fields are described in the following table.

Bit #	Field	Type	Reset	EEPROM	Description	
[7]	RESERVED	-	-	N	Reserved.	
[6:4]	PLL_CP_PHASE_SHIFT[2:0]	RW	0x0	Y	Program Charge Pump Phase Shift.	
					PLL_CP_PHASE_SHIFT[2:0]	**Phase Shift**
					0 (0x0)	No delay
					1 (0x1)	1.3ns for 100MHz f_{PD}
					2 (0x2)	1ns for 100MHz f_{PD}
					3 (0x3)	0.9ns for 100MHz f_{PD}
					4 (0x4)	1.3ns for 50MHz f_{PD}
					5 (0x5)	1ns for 50MHz f_{PD}
					6 (0x6)	0.9ns for 50MHz f_{PD}
					7 (0x7)	0.7ns for 50MHz f_{PD}
[3]	RESERVED	-	-	N	Reserved.	
[2]	PLL_ENABLE_C3	RW	0	Y	Disable third order capacitor in the low pass filter.	
					PLL_ENABLE_C3	**MODE**
					0	2nd order loop filter recommended setting
					1	Enables C3, 3rd order loop filter enabled
[1:0]	RESERVED	-	0x3	Y	Reserved.	

8.1.24 PLL_LF_R2 Register; R36

The PLL_LF_R2 register controls the value of the PLL Loop Filter R2.

Bit #	Field	Type	Reset	EEPROM	Description	
[7:0]	PLL_LF_R2[7:0]	RW	0x28	Y	PLL Loop Filter R2. NOTE: Table below lists commonly used R2 values but more selections are available.	
					PLL_LF_R2[7:0]	**R2 (Ω)**
					1 (0x01)	200
					4 (0x04)	500
					8 (0x08)	700
					32 (0x20)	1600
					48 (0x30)	2400
					64 (0x40)	3200

8.1.25 PLL_LF_C1 Register; R37

The PLL_LF_C1 register controls the value of the PLL Loop Filter C1.

Bit #	Field	Type	Reset	EEPROM	Description
[7:3]	RESERVED	-	-	N	Reserved.
[2:0]	PLL_LF_C1[2:0]	RW	0x0	Y	PLL Loop Filter C1. The value in pF is given by 5 + 50 * PLL_LF_C1 (in decimal).

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8.1.26 PLL_LF_R3 Register; R38

The PLL_LF_R3 register controls the value of the PLL Loop Filter R3.

Bit #	Field	Type	Reset	EEPROM	Description	
[7]	RESERVED	-	-	N	Reserved.	
[6:0]	PLL_LF_R3[6:0]	RW	0x00	Y	PLL Loop Filter R3. NOTE: Table below lists commonly used R3 values but more selections are available.	
					PLL_LF_R3[6:0]	**R3 (Ω)**
					0 (0x00)	18
					3 (0x03)	205
					8 (0x08)	854
					9 (0x09)	1136
					12 (0x0C)	1535
					17 (0x11)	1936
					20 (0x14)	2335

8.1.27 PLL_LF_C3 Register; R39

The PLL_LF_C3 register controls the value of the PLL Loop Filter C3.

Bit #	Field	Type	Reset	EEPROM	Description
[7:3]	RESERVED	-	-	N	Reserved.
[2:0]	PLL_LF_C3[2:0]	RW	0x0	Y	PLL Loop Filter C3. The value in pF is given by 5 * PLL_LF_C3 (in decimal).

8.1.28 PLL_CALCTRL Register; R42

The PLL_CALCTRL register is described in the following table.

Bit #	Field	Type	Reset	EEPROM	Description	
[7:4]	RESERVED	-	-	N	Reserved.	
[3:2]	PLL_CLSDWAIT[1:0]	RW	0x2	Y	Closed Loop Wait Period. The CLSDWAIT field sets the closed loop wait period. Recommended value is 0x2.	
					CLSDWAIT	**Analog closed loop VCO stabilization time**
					0 (0x0)	150µs
					1 (0x1)	300µs
					2 (0x2)	500µs
					3 (0x3)	2000µs
[1:0]	PLL_VCOWAIT[1:0]	RW	0x1	Y	VCO Wait Period. Recommended value is 0x1.	
					VCOWAIT	**VCO stabilization time**
					0 (0x0)	20µs
					1 (0x1)	400µs
					2 (0x2)	4000µs
					3 (0x3)	10000µs

8.1.29 NVMSCRC Register; R47

The NVMSCRC register holds the Stored CRC (Cyclic Redundancy Check) byte that has been retrieved from on-chip EEPROM.

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Bit #	Field	Type	Reset	EEPROM	Description
[7:0]	NVMSCRC[7:0]	R	0x00	Y	EEPROM Stored CRC.

8.1.30 NVMCNT Register; R48

The NVMCNT register is intended to reflect the number of on-chip EEPROM Erase/Program cycles that have taken place in EEPROM. The count is automatically incremented by hardware and stored in EEPROM.

Bit #	Field	Type	Reset	EEPROM	Description
[7:0]	NVMCNT[7:0]	R	0x00	Y	EEPROM Program Count. The NVMCNT increments automatically after every EEPROM Erase/Program Cycle. The NVMCNT value is retrieved automatically after reset, after a EEPROM Commit operation or after a Erase/Program cycle. The NVMCNT register increments until the register reaches the maximum value of 255 after which no further increments takes place.

8.1.31 NVMCTL Register; R49

The NVMCTL register allows control of the on-chip EEPROM Memories.

Bit #	Field	Type	Reset	EEPROM	Description
[7]	RESERVED	-	-	N	Reserved.
[6]	REGCOMMIT	RWSC	0	N	REG Commit to EEPROM SRAM Array. The REGCOMMIT bit is used to initiate a transfer from the on-chip registers back to the corresponding location in the EEPROM SRAM Array. The REGCOMMIT bit is automatically cleared to 0 when the transfer is complete.
[5]	NVMCRCERR	R	0	N	EEPROM CRC Error Indication. The NVMCRCERR bit is set to 1 if a CRC Error has been detected when reading back from on-chip EEPROM during device configuration.
[4]	NVMAUTOCRC	RW	1	N	EEPROM Automatic CRC. When NVMAUTOCRC is 1 then the EEPROM Stored CRC byte is automatically calculated whenever a EEPROM program takes place.
[3]	NVMCOMMIT	RWSC	0	N	EEPROM Commit to Registers. The NVMCOMMIT bit is used to initiate a transfer of the on-chip EEPROM contents to internal registers. The transfer happens automatically after reset or when NVMCOMMIT is set to 1. The NVMCOMMIT bit is automatically cleared to 0. The I^2C registers cannot be read while a EEPROM Commit operation is taking place.
[2]	NVMBUSY	R	0	N	EEPROM Program Busy Indication. The NVMBUSY bit is 1 during an on-chip EEPROM Erase/Program cycle. While NVMBUSY is 1 the on-chip EEPROM cannot be accessed.
[1]	NVMERASE	RWSC	0	N	EEPROM Erase Start. The NVMERASE bit is used to begin an on-chip EEPROM Erase cycle. The Erase cycle is only initiated if the immediately preceding I^2C transaction is a write to the NVMUNLK register with the appropriate code. The NVMERASE bit is automatically cleared to 0. The EEPROM Erase operation takes around 115ms.
[0]	NVMPROG	RWSC	0	N	EEPROM Program Start. The NVMPROG bit is used to begin an on-chip EEPROM Program cycle. The Program cycle is only initiated if the immediately preceding I^2C transaction is a write to the NVMUNLK register with the appropriate code. The NVMPROG bit is automatically cleared to 0. If the NVMERASE and NVMPROG bits are set simultaneously then an ERASE/PROGRAM cycle is executed. The EEPROM Program operation takes around 115ms.

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8.1.32 NVMLCRC Register; R50

The NVMLCRC register holds the live CRC (Cyclic Redundancy Check) byte computed based on the live register values.

Bit #	Field	Type	Reset	EEPROM	Description
[7:0]	NVMLCRC[7:0]	R	0x00	N	NVM Live CRC

8.1.33 MEMADR Register; R51

The MEMADR register holds 7-bits of the starting address for on-chip SRAM or EEPROM access.

Bit #	Field	Type	Reset	EEPROM	Description
[7]	RESERVED	-	-	N	Reserved.
[6:0]	MEMADR[6:0]	RW	0x00	N	Memory Address. The MEMADR value determines the starting address for on-chip SRAM read/write access or on-chip EEPROM access. The internal address to access SRAM or EEPROM is automatically incremented; however the MEMADR register does not reflect the internal address in this way. When the SRAM or EEPROM arrays are accessed using the I^2C interface only bits [4:0] of MEMADR are used to form the byte Wise address.

8.1.34 NVMDAT Register; R52

The NVMDAT register returns the on-chip EEPROM contents from the starting address specified by the MEMADR register.

Bit #	Field	Type	Reset	EEPROM	Description
[7:0]	NVMDAT[7:0]	R	0x00	N	EEPROM Read Data. The first time an I^2C read transaction accesses the NVMDAT register address, either because the address is explicitly targeted or because the address is auto-incremented, the read transaction returns the EEPROM data located at the address specified by the MEMADR register. Any additional reads which are part of the same transaction cause the EEPROM address to be incremented and the next EEPROM data byte is returned. The I^2C address is no longer auto-incremented, that is the I^2C address is locked to the NVMDAT register after the first access. Access to the NVMDAT register terminates at the end of the current I^2C transaction.

8.1.35 RAMDAT Register; R53

The RAMDAT register provides read and write access to the SRAM that forms part of the on-chip EEPROM module.

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Bit #	Field	Type	Reset	EEPROM	Description
[7:0]	RAMDAT[7:0]	RW	0x00	N	RAM Read/Write Data. The first time an I^2C read or write transaction accesses the RAMDAT register address, either because the register is explicitly targeted or because the address is auto-incremented, a read transaction returns the RAM data located at the address specified by the MEMADR register and a write transaction causes the current I^2C data to be written to the address specified by the MEMADR register. Any additional accesses which are part of the same transaction causes the RAM address to be incremented and a read or write access takes place to the next SRAM address. The I^2C address no longer is auto-incremented; the I^2C address is locked to the RAMDAT register after the first access. Access to the RAMDAT register terminates at the end of the current I^2C transaction.

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8.1.36 NVMUNLK Register; R56

The NVMUNLK register provides a rudimentary level of protection to prevent inadvertent programming of the on-chip EEPROM.

Bit #	Field	Type	Reset	EEPROM	Description
[7:0]	NVMUNLK[7:0]	RW	0x00	N	EEPROM Prog Unlock. The NVMUNLK register must be written immediately prior to setting the NVMPROG bit of register NVMCTL, otherwise the Erase/Program cycle is not triggered. NVMUNLK must be written with a value of 0xBE.

8.1.37 INT_LIVE Register; R66

The INT_LIVE register reflects the current status of the interrupt sources.

Bit #	Field	Type	Reset	EEPROM	Description
[7:2]	RESERVED	-	-	N	Reserved.
[1]	LOL	R	0	N	Loss of Lock PLL.
[0]	CAL	R	0	N	Calibration Active PLL.

8.1.38 SWRST Register; R72

The SWRST1 register provides software reset control for specific on-chip modules. Each bit in this register is individually self cleared after a write operation. The SWRST1 register always returns 0x00 in a read transaction.

Bit #	Field	Type	Reset	EEPROM	Description
[7:2]	RESERVED	-	-	N	Reserved.
[1]	SWR2PLL	RWSC	0	N	Software Reset PLL. Setting SWR2PLL to 1 resets the PLL calibrator and clock dividers. This bit is automatically cleared to 0.
[0]	RESERVED	-	-	N	Reserved.

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9 Application and Implementation

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9.1 Application Information

The LMK61E2 is an ultra-low jitter programmable oscillator that can be used to provide reference clocks for high-speed serial links resulting in improved system performance. The LMK61E2 also supports a variety of features that aids the hardware designer during the system debug and validation phase.

9.2 Typical Applications

9.2.1 Jitter Considerations in Serdes Systems

Jitter-sensitive applications such as 10Gbps or 100Gbps Ethernet, deploy a serial link using a Serializer in the transmit section (TX) and a De-serializer in the receive section (RX). These SERDES blocks are typically embedded in an ASIC or FPGA. Estimating the clock jitter impact on the link budget requires understanding of the TX PLL bandwidth and the RX CDR bandwidth.

As can be seen in 図 9-1, the pass band region between the TX low-pass cutoff and RX high-pass cutoff frequencies is the range over which the reference clock jitter adds without any attenuation to the jitter budget of the link. Outside of these frequencies, the SERDES link attenuates the reference clock jitter with a 20dB/dec or even steeper roll-off. Modern ASIC or FPGA designs have some flexibility on deciding the optimal RX CDR bandwidth and TX PLL bandwidth. These bandwidths are typically set based on what is achievable in the ASIC or FPGA process node, without increasing design complexity, and on any jitter tolerance or wander specification that needs to be met, as related to the RX CDR bandwidth.

The overall allowable jitter in a serial link is dictated by IEEE or other relevant standards. For example, IEEE802.3ba states that the maximum transmit jitter (peak-peak) for 10Gbps Ethernet must be no more than 0.28 × UI and this equates to a 27.1516ps, p-p for the overall allowable transmit jitter.

The jitter contributing elements are made up of the reference clock, generated potentially from a device like LMK61E2, the transmit medium, transmit driver, and so forth. Only a portion of the overall allowable transmit jitter is allocated to the reference clock, typically 20% or lower. Therefore, the allowable reference clock jitter, for a 20% clock jitter budget, is 5.43ps, p-p.

Jitter in a reference clock is made up of deterministic jitter (arising from spurious signals due to supply noise or mixing from other outputs or from the reference input) and random jitter (typically due to thermal noise and other uncorrelated noise sources). A typical clock tree in a serial link system consists of clock generators and fanout buffers. The allowable reference clock jitter of 5.43ps, p-p is needed at the output of the fanout buffer. Modern fanout buffers have low-additive random jitter (less than 100fs RMS) with no substantial contribution to the deterministic jitter. Therefore, the clock generator and fanout buffer contribute to the random jitter while the primary contributor to the deterministic jitter is the clock generator. General guidance, for modern clock generators, is to allocate 25% of allowable reference clock jitter to the deterministic jitter and 75% to the random jitter. This amounts to an allowable deterministic jitter of 1.36ps, p-p and an allowable random jitter of 4.07ps, p-p. For serial link systems that need to meet a bit error rate (BER) of 10^{-12}, the allowable random jitter in root-mean-square is 0.29ps RMS. This is calculated by dividing the p-p jitter by 14 for a BER of 10^{-12}. Accounting for random jitter from the fanout buffer, the random jitter needed from the clock generator is 0.27ps RMS. This is calculated by the root-mean-square subtraction from the desired jitter at the fanout buffer's output assuming 100fs RMS of additive jitter from the fanout buffer.

With careful frequency planning techniques, like spur optimization (covered in *Spur Mitigation Techniques*) and on-chip LDOs to suppress supply noise, the LMK61E2 is able to generate clock outputs with deterministic jitter

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that is below 1ps, p-p and random jitter that is below 0.2ps RMS. This gives the serial link system with additional margin on the allowable transmit jitter resulting in a BER better than 10^{-12}.

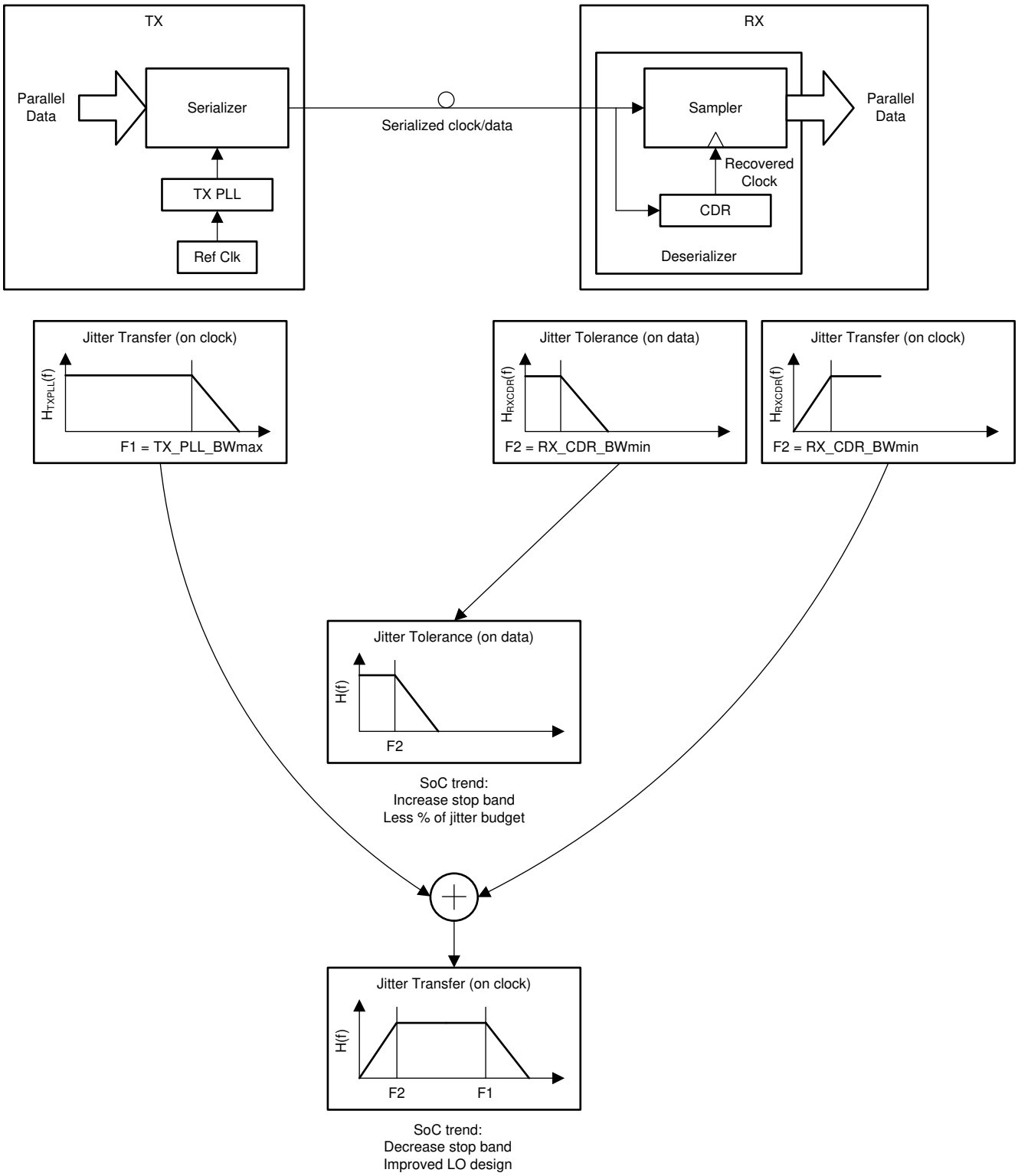


図 9-1. Dependence of Clock Jitter in Serial Links

9.2.2 Frequency Margining

9.2.2.1 Fine Frequency Margining

IEEE802.3 dictates that Ethernet frames stay compliant to the standard specifications when clocked with a reference clock that is within ±100ppm of the nominal frequency. In the worst case, an RX node with the local reference clock at –100ppm from the nominal frequency must be able to work seamlessly with a TX node that has a dedicated local reference clock at +100ppm from the nominal frequency. Without any clock compensation on the RX node, the read pointer severely lags behind the write pointer and cause FIFO overflow errors. On the contrary, when the local clock of the RX node operates at +100ppm from the nominal frequency and the local clock of the TX node operates at –100ppm from the nominal frequency, FIFO underflow errors occur without any clock compensation.

To prevent such overflow and underflow errors from occurring, modern ASICs and FGPAs include a clock compensation scheme that introduces elastic buffers. Such a system, shown in 図 9-2, is validated thoroughly during the validation phase by interfacing slower nodes with faster ones and verifying compliance to IEEE802.3. The LMK61E2 provides the ability to fine tune the frequency of the outputs based on changing the load capacitance for the integrated oscillator. This fine tuning can be done through I^2C as described in *Integrated Oscillator*. The change in load capacitance is implemented in a manner such that the output of LMK61E2 undergoes a smooth monotonic change in frequency.

9.2.2.2 Coarse Frequency Margining

Certain systems require the processors to be tested at clock frequencies that are slower or faster by 5% or 10%. The LMK61E2 offers the ability to change the output divider for the desired change from the nominal output frequency as explained in the *High-Speed Output Divider* section.

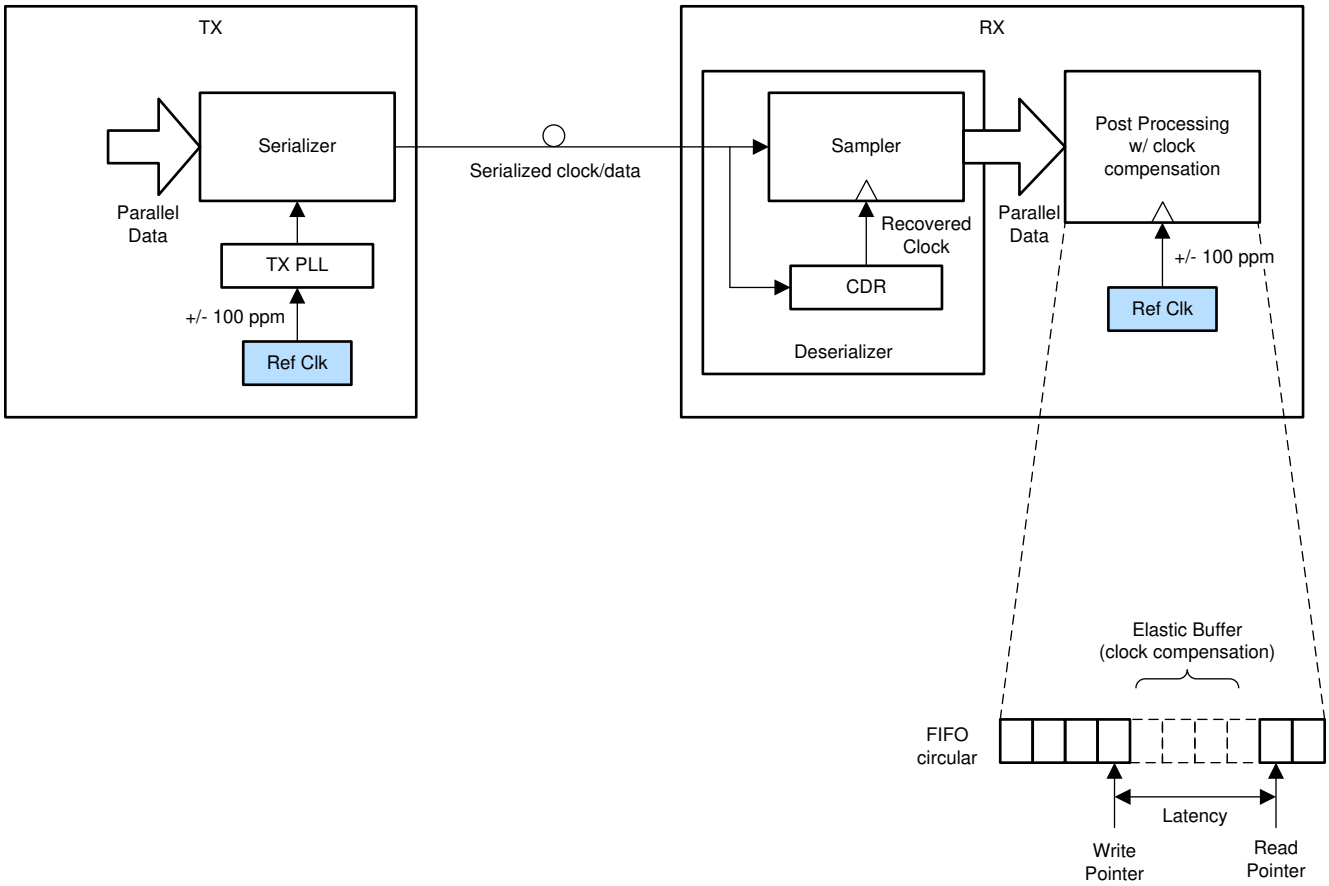


図 9-2. System Implementation With Clock Compensation for Standards Compliance

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9.2.3 Design Requirements

Consider a typical wired communications application, like a top-of-rack switch, which needs to clock high data rate 10Gbps or 100Gbps Ethernet PHYs. In such systems, the clock is expected to be available upon power up without the need for any device-level programming. An example of such a clock frequency is 156.25MHz in LVPECL output format.

The *Detailed Design Procedure* below describes the detailed design procedure to generate the required output frequencies for the above scenario using LMK61E2.

9.2.3.1 Detailed Design Procedure

Design of all aspects of the LMK61E2 is simplified with software support that assists in part selection, part programming, loop filter design, and phase noise simulation. This design procedure provides a quick outline of the process.

1. Device Selection
   - The first step to calculate the specified VCO frequency given required output frequency. The device must be able to produce the VCO frequency that can be divided down to the required output frequency.
   - The WEBENCH Clock Architect Tool from TI aids in the selection of the right device that meets the designer output frequency and format requirements.
2. Device Configuration
   - There are many device configurations to achieve the desired output frequency from a device. However, the user must consider some optimizations and trade-offs.
   - The WEBENCH Clock Architect Tool attempts to maximize the phase detector frequency, use smallest dividers, and maximizes PLL charge pump current.
   - These guidelines below can be followed when configuring PLL related dividers or other related registers:
     – For lowest possible in-band PLL flat noise, maximize phase detector frequency to minimize N divide value.
     – For lowest possible in-band PLL flat noise, maximize charge pump current. The highest value charge pump currents often have similar performance due to diminishing returns.
     – For fractional divider values, keep the denominator at highest value possible to minimize spurs. Use higher order modulator wherever possible for the same reason.
     – The general guidance is to keep the phase detector frequency approximately between 10 × PLL loop bandwidth and 100 × PLL loop bandwidth. A phase detector frequency less than 5 × PLL bandwidth can be unstable and a phase.
3. PLL Loop Filter Design
   - Using the WEBENCH Clock Architect Tool to design your loop filter is recommended.
   - The desirable loop filter design and simulation can be achieved when custom reference phase noise profiles are loaded into the software tool.
   - While designing the loop filter, adjusting the charge pump current or N value can help with loop filter component selection. Lower charge pump currents and larger N values result in smaller component values but can increase impacts of leakage and reduce PLL phase noise performance.
   - For a more detailed understanding of loop filter design can be found in *PLL Performance, Simulation, and Design* (SNAA106).
4. Device Programming
   - The EVM programming software tool CodeLoader can be used to program the device with the desired configuration.

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9.2.3.1.1 Custom Design With WEBENCH® Tools

Click here to create a custom design using the LMK61E2 device with the WEBENCH® Power Designer.

1. Start by entering the input voltage (V_{IN}), output voltage (V_{OUT}), and output current (I_{OUT}) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance
- Run thermal simulations to understand board thermal performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

9.2.3.1.2 Device Selection

Use the WEBENCH Clock Architect Tool. Enter the required output frequencies and formats into the tool. To use this device, find a solution using the LMK61E2.

9.2.3.1.3 VCO Frequency Calculation

In this example, the VCO frequency of the LMK61E2 to generate 156.25MHz can be calculated as 5GHz.

9.2.3.1.4 Device Configuration

For this example, enter the desired output frequency and click on *Generate Solutions*. Select LMK61E2 from the solution list. To maximize the phase detector frequency using the simulation page of the WEBENCH Clock Architect Tool, the PLL R divider is set to 1, doubler is enabled and N divider is set to 50 for a PFD frequency of 100MHz. This results in a VCO frequency of 5GHz. At this point the design meets the output frequency requirements and design a loop filter can be made for the system and performance can be simulated on the clock output.

9.2.3.1.5 PLL Loop Filter Design

In the WEBENCH Clock Architect Tool simulator, click on the PLL loop filter design button, then press recommend design. For the PLL loop filter, maximum phase detector frequency and maximum charge pump current are typically used. The tool recommends a loop filter that is designed to minimize jitter. The integrated loop filter's components are minimized with this recommendation as to allow maximum flexibility in achieving wide loop bandwidths for low PLL noise. With the recommended loop filter calculated, this loop filter is ready to be simulated.

The PLL loop filter's bode plot can additionally be viewed and adjustments can be made to the integrated components. The effective loop bandwidth and phase margin with the updated values is then calculated. The integrated loop filter components are good to use when attempting to eliminate certain spurs. The recommended procedure is to increase C3 capacitance, then R3 resistance. Large R3 resistance can result in degraded VCO phase noise performance.

9.2.3.1.6 Spur Mitigation Techniques

The LMK61E2 offers several programmable features for optimizing fractional spurs. To obtain the best optimization from these features, understanding the different kinds of spurs and spur behaviors, causes, and remedies is necessary. Although optimizing spurs can involve some trial and error, there are ways to make optimizing the process more systematic. TI offers the *Clock Design Tool* for more information and estimation of fractional spurs.

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9.2.3.1.6.1 Phase Detection Spur

The phase detector spur occurs at an offset from the carrier equal to the phase detector frequency, f_{PD}. To minimize this spur, a lower phase detector frequency must be considered. In some cases where the loop bandwidth is very wide relative to the phase detector frequency, some benefit can be gained from using a narrower loop bandwidth or adding poles to the loop filter by using R3 and C3 if previously unused, but otherwise the loop filter has minimal impact. Bypassing at the supply pins and board layout can also have an impact on this spur, especially at higher phase detector frequencies.

9.2.3.1.6.2 Integer Boundary Fractional Spur

This spur occurs at an offset equal to the difference between the VCO frequency and the closest integer channel for the VCO. For instance, if the phase detector frequency is 100MHz and the VCO frequency is 5003MHz, then the integer boundary spur is at 3MHz offset. This spur can be either PLL or VCO dominated. If the spur is PLL dominated, decreasing the loop bandwidth and some of the programmable fractional can impact this spur. If the spur is VCO dominated, then reducing the loop filter does not help, but rather reducing the phase detector and having good slew rate and signal integrity at the selected reference input helps.

9.2.3.1.6.3 Primary Fractional Spur

These spurs occur at multiples of f_{PD}/DEN and are not the integer boundary spur. For instance, if the phase detector frequency is 100MHz and the fraction is 3/100, the primary fractional spurs are at 1MHz, 2MHz, 4MHz, 5MHz, 6MHz, and so forth. These are impacted by the loop filter bandwidth and modulator order. If a small frequency error is acceptable, then a larger equivalent fraction can improve these spurs. This larger inequivalent fraction pushes the fractional spur energy to much lower frequencies to reduce impact on the system performance.

9.2.3.1.6.4 Sub-Fractional Spur

These spurs appear at a fraction of f_{PD}/DEN and depend on modulator order. With the first order modulator, there are no sub-fractional spurs. The second order modulator can produce 1/2 sub-fractional spurs if the denominator is even. A third order modulator can produce sub-fractional spurs at 1/2, 1/3, or 1/6 of the offset, depending if the offset is divisible by 2 or 3. For instance, if the phase detector frequency is 100MHz and the fraction is 3/100, no sub-fractional spurs for a first order modulator or sub-fractional spurs at multiples of 1.5MHz for a second or third order modulator is expected. Aside from strategically choosing the fractional denominator and using a lower order modulator, another tactic to eliminate these spurs is to use dithering and express the fraction in larger equivalent terms. Because dithering also adds phase noise, the level needs to be managed to achieve acceptable phase noise and spurious performance.

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表 9-1 summarizes spur and mitigation techniques.

表 9-1. Spur and Mitigation Techniques

SPUR TYPE	OFFSET	WAYS TO REDUCE	TRADE-OFFS
Phase Detector	f_{PD}	Reduce Phase Detector Frequency.	Although reducing the phase detector frequency does improve this spur, this reduction also degrades phase noise.
Integer Boundary	f_{VCO} mod f_{PD}	**Methods for PLL Dominated Spurs**	Reducing the loop bandwidth can degrade the total integrated noise if the bandwidth is too narrow.
		- Avoid the worst case VCO frequencies if possible.	
		- Provide good slew rate and signal integrity at reference input.	
		- Reduce loop bandwidth or add more filter poles to suppress out of band spurs.	
		Methods for VCO Dominated Spurs	Reducing the phase detector can degrade the phase noise.
		- Avoid the worst case VCO frequencies if possible.	
		- Reduce Phase Detector Frequency.	
		- Provide good slew rate and signal integrity at reference input.	
Primary Fractional	f_{PD}/DEN	- Decrease Loop Bandwidth.	Decreasing the loop bandwidth can degrade in-band phase noise. Also, larger inequivalent fractions do not always reduce spurs.
		- Change Modulator Order.	
		- Use Larger Inequivalent Fractions.	
Sub-Fractional	f_{PD}/DEN/k k=2,3, or 6	- Use Dithering.	Dithering and larger fractions can increase phase noise.
		- Use Larger Equivalent Fractions.	
		- Use Larger Inequivalent Fractions.	
		- Reduce Modulator Order.	
		- Eliminate factors of 2 or 3 in denominator.	

9.3 Power Supply Recommendations

For best electrical performance of the LMK61E2 device, use a combination of 10µF, 1µF, and 0.1µF on the power supply bypass network. TI also recommends using component side mounting of the power supply bypass capacitors and to use 0201 or 0402 body size capacitors to facilitate signal routing. Keep the connections between the bypass capacitors and the power supply on the device as short as possible. Ground the other side of the capacitor using a low impedance connection to the ground plane. 図 9-3 shows the layout recommendation for power supply decoupling of LMK61E2.

9.4 Layout

9.4.1 Layout Guidelines

Verified Thermal Reliability, *Best Practices for Signal Integrity* and *Recommended Solder Reflow Profile* provide recommendations for board layout, solder reflow profile and power supply bypassing when using LMK61E2 to provide good thermal / electrical performance and overall signal integrity of entire system.

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9.4.1.1 Verified Thermal Reliability

The LMK61E2 is a high performance device. Therefore careful attention must be paid to device configuration and printed circuit board (PCB) layout with respect to power consumption. The ground pin needs to be connected to the ground plane of the PCB through three vias or more, as shown in 図 9-3, to maximize thermal dissipation out of the package.

式 3 describes the relationship between the PCB temperature around the LMK61E2 and the junction temperature.

$$T_B = T_J – \Psi_{JB} * P \quad (3)$$

where

- T_B: PCB temperature around the LMK61E2
- T_J: Junction temperature of LMK61E2
- Ψ_{JB}: Junction-to-board thermal resistance parameter of LMK61E2 (36.7°C/W without airflow)
- P: On-chip power dissipation of LMK61E2

To verify that the maximum junction temperature of LMK61E2 is below 125°C, the temperature can be calculated that the maximum PCB temperature without airflow must be at 100°C or below when the device is optimized for best performance resulting in maximum on-chip power dissipation of 0.68W.

9.4.1.2 Best Practices for Signal Integrity

For best electrical performance and signal integrity of entire system with LMK61E2, route vias into decoupling capacitors and then into the LMK61E2. In additions, increase the via count and width of the traces wherever possible. These steps provide the lowest impedance and shortest path for high frequency current flow. 図 9-3 shows the layout recommendation for LMK61E2.

9.4.1.3 Recommended Solder Reflow Profile

Follow the solder paste supplier recommendations to optimize flux activity and to achieve proper melting temperatures of the alloy within the guidelines of J-STD-20. Best practise is for the LMK61E2 to be processed with the lowest peak temperature possible while also remaining below the components peak temperature rating as listed on the MSL label. The exact temperature profile depends on several factors including maximum peak temperature for the component as rated on the MSL label, Board thickness, PCB material type, PCB geometries, component locations, sizes, densities within PCB, as well solder manufactures recommended profile, and capability of the reflow equipment to as confirmed by the SMT assembly operation.

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9.4.2 Layout Example

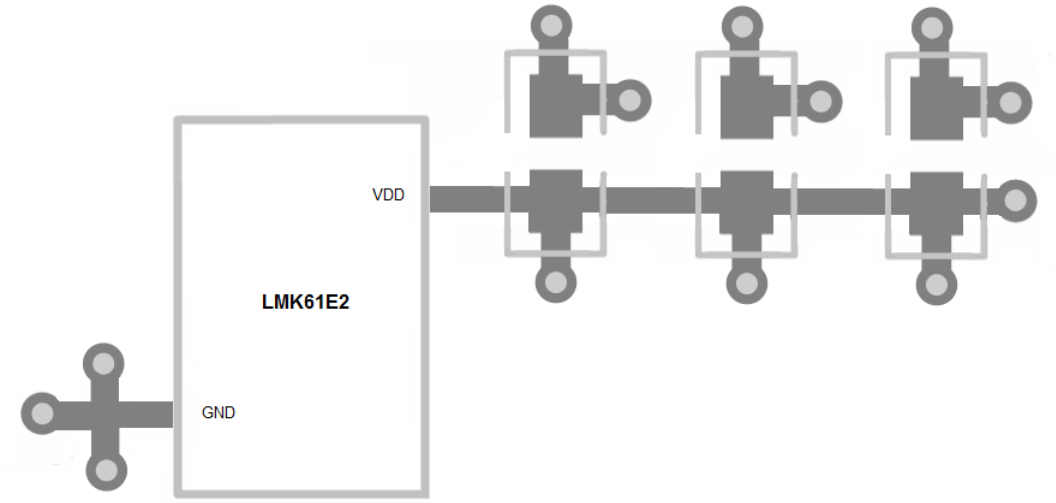


図 9-3. LMK61E2 Layout Recommendation for Power Supply and Ground

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10 Device and Documentation Support

10.1 Device Support

10.1.1 Development Support

For development support, see the following:

- WEBENCH Clock Architect Tool
- CodeLoader

10.1.1.1 Custom Design With WEBENCH® Tools

Click here to create a custom design using the LMK61E2 device with the WEBENCH® Power Designer.

1. Start by entering the input voltage (V_{IN}), output voltage (V_{OUT}), and output current (I_{OUT}) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance
- Run thermal simulations to understand board thermal performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

10.2 Documentation Support

10.2.1 Related Documentation

For related documentation, see the following:

- *Clock Design Tool* (SNAU082)
- *PLL Performance, Simulation, and Design* (SNAA106)
- *Semiconductor and IC Package Thermal Metrics* (SPRA953)

10.3 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、www.tij.co.jp のデバイス製品フォルダを開いてください。[通知] をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取ることができます。 変更の詳細については、改訂されたドキュメントに含まれている改訂履歴をご覧ください。

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10.7 用語集

テキサス・インスツルメンツ用語集　この用語集には、用語や略語の一覧および定義が記載されています。

11 Revision History

Changes from Revision B (February 2017) to Revision C (May 2025)	Page
• ドキュメント全体にわたって表、図、相互参照の採番方法を更新	1
• 表のタイトルを「*製品情報*」から：パッケージ情報	1
• Updated specified device in register map from LMK61E2-I3 to LMK61E2. Updated reset values for XO_CAPCTRL_BY0, PLL_NDIV_BY0, PLL_CTRL0, PLL_FRACDEN_BY0, and PLL_CALCTRL	27
• Updated SLAVEADR value based on status of ADD pin	29
• Deleted mentions of multiple PLLs and RESETn pin in R10 (DEV_CTL) description	30
• Changed PLL_FRACDEN_BY0 reset value from 0x00 to 0x01	32
• Added description for R50 (NVMLCRC)	37
• Moved the *Power Supply Recommendations* and *Layout* sections to the *Application and Implementation* section	46

Changes from Revision A (September 2015) to Revision B (February 2017)	Page
• カスタム設計用の WEBENCH リンクと情報を追加	1
• LMK61E2BAA、LMK61E2BBA の新規リリース	1
• 最新のドキュメントおよび翻訳標準に合わせて、データシートのテキストを更新	1
• Moved 図 9-3 to *Layout Example*	48

Changes from Revision * (September 2015) to Revision A (March 2016)	Page
• Moved conditions from figure title to table under each graphic	11
• Updated 図 7-3	19
• Added Related Documentation section	49

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LMK61E2-SIAR	Active	Production	QFM (SIA) | 8	2500 | LARGE T&R	In-Work	NIAU	Level-3-260C-168 HR	-40 to 85	LMK61E2
LMK61E2-SIAR.A	Active	Production	QFM (SIA) | 8	2500 | LARGE T&R	In-Work	NIAU	Level-3-260C-168 HR	-40 to 85	LMK61E2
LMK61E2-SIAT	Active	Production	QFM (SIA) | 8	250 | SMALL T&R	In-Work	NIAU	Level-3-260C-168 HR	-40 to 85	LMK61E2
LMK61E2-SIAT.A	Active	Production	QFM (SIA) | 8	250 | SMALL T&R	In-Work	NIAU	Level-3-260C-168 HR	-40 to 85	LMK61E2
LMK61E2BAA-SIAR	Active	Production	QFM (SIA) | 8	2500 | LARGE T&R	Yes	NIAU	Level-3-260C-168 HR	-40 to 85	LMK61E2 BAA
LMK61E2BAA-SIAR.A	Active	Production	QFM (SIA) | 8	2500 | LARGE T&R	Yes	NIAU	Level-3-260C-168 HR	-40 to 85	LMK61E2 BAA
LMK61E2BAA-SIAT	Active	Production	QFM (SIA) | 8	250 | SMALL T&R	Yes	NIAU	Level-3-260C-168 HR	-40 to 85	LMK61E2 BAA
LMK61E2BAA-SIAT.A	Active	Production	QFM (SIA) | 8	250 | SMALL T&R	Yes	NIAU	Level-3-260C-168 HR	-40 to 85	LMK61E2 BAA
LMK61E2BBA-SIAR	Active	Production	QFM (SIA) | 8	2500 | LARGE T&R	Yes	NIAU	Level-3-260C-168 HR	-40 to 85	LMK61E2 BBA
LMK61E2BBA-SIAR.A	Active	Production	QFM (SIA) | 8	2500 | LARGE T&R	Yes	NIAU	Level-3-260C-168 HR	-40 to 85	LMK61E2 BBA
LMK61E2BBA-SIAT.A	Active	Production	QFM (SIA) | 8	250 | SMALL T&R	Yes	NIAU	Level-3-260C-168 HR	-40 to 85	LMK61E2 BBA

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

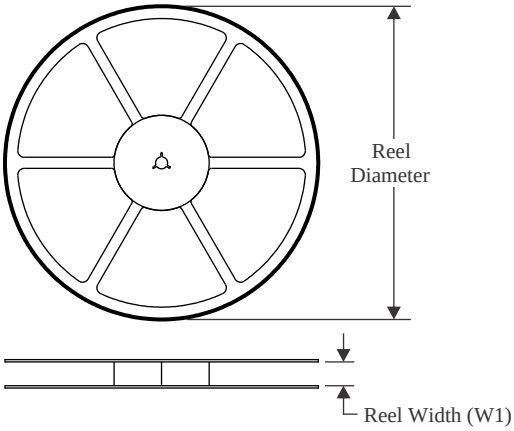
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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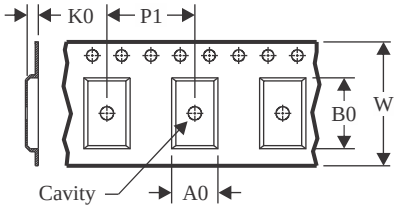
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TAPE AND REEL INFORMATION

REEL DIMENSIONS

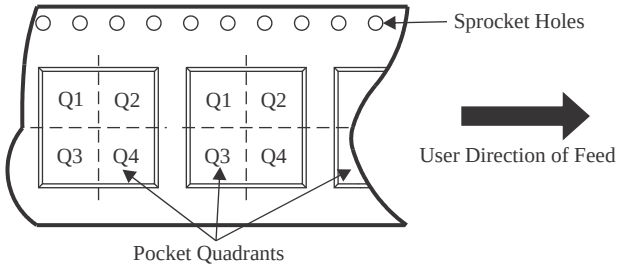


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

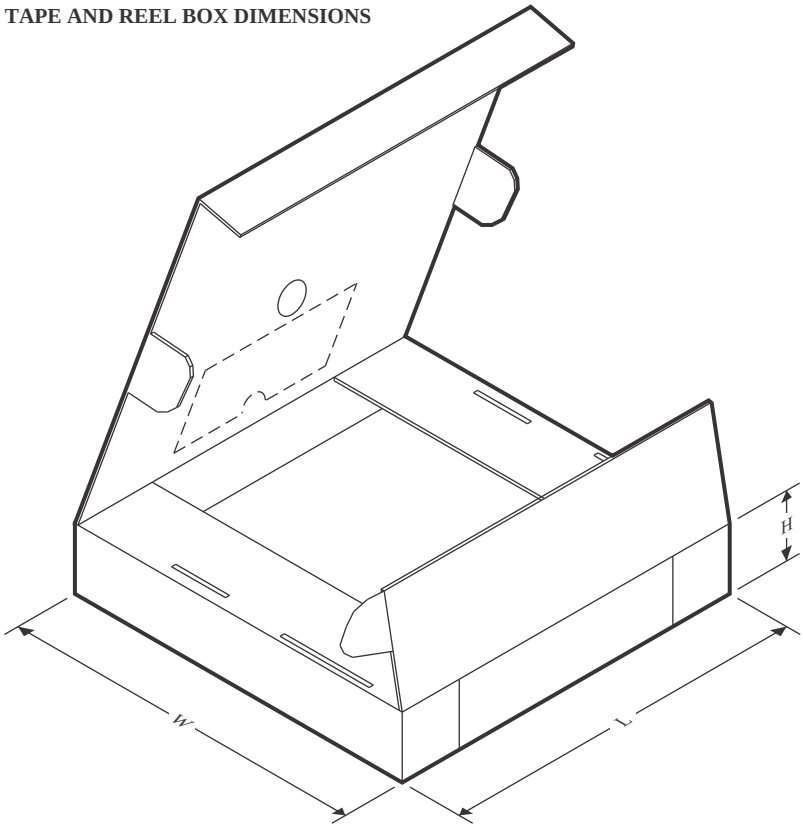
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMK61E2-SIAR	QFM	SIA	8	2500	330.0	16.4	5.5	7.5	1.5	8.0	16.0	Q1
LMK61E2-SIAT	QFM	SIA	8	250	178.0	16.4	5.5	7.5	1.5	8.0	16.0	Q1
LMK61E2BAA-SIAR	QFM	SIA	8	2500	330.0	16.4	5.5	7.5	1.5	8.0	16.0	Q1
LMK61E2BAA-SIAT	QFM	SIA	8	250	178.0	16.4	5.5	7.5	1.5	8.0	16.0	Q1
LMK61E2BBA-SIAR	QFM	SIA	8	2500	330.0	16.4	5.5	7.5	1.5	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

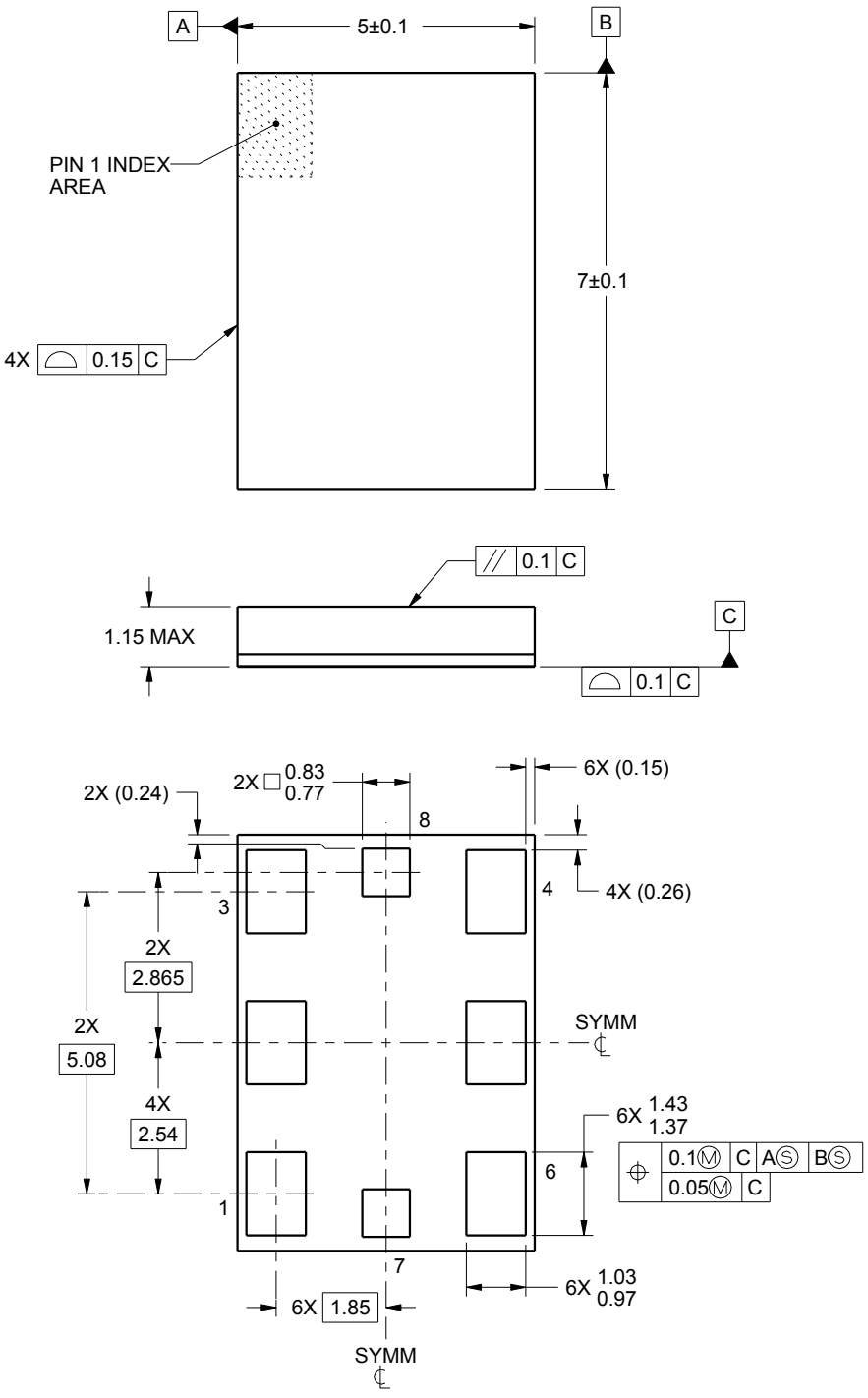
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMK61E2-SIAR	QFM	SIA	8	2500	356.0	356.0	36.0
LMK61E2-SIAT	QFM	SIA	8	250	208.0	191.0	35.0
LMK61E2BAA-SIAR	QFM	SIA	8	2500	356.0	356.0	36.0
LMK61E2BAA-SIAT	QFM	SIA	8	250	213.0	191.0	55.0
LMK61E2BBA-SIAR	QFM	SIA	8	2500	356.0	356.0	36.0

PACKAGE OUTLINE

SIA0008B

QFM - 1.15 mm max height

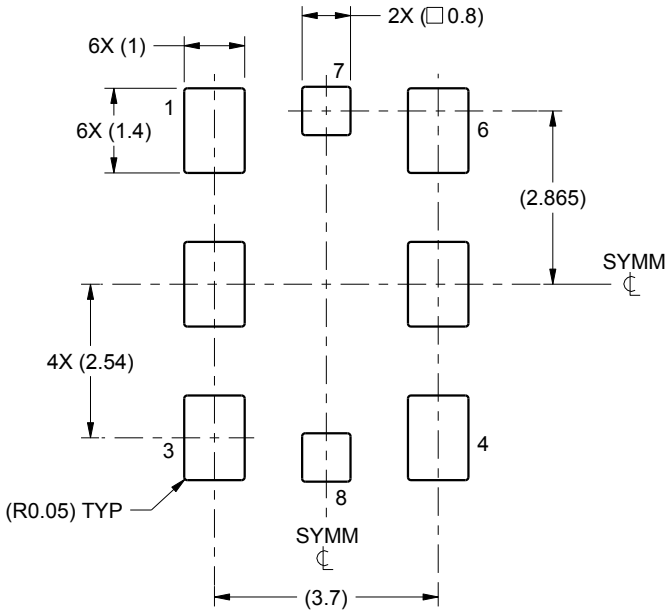
QUAD FLAT MODULE



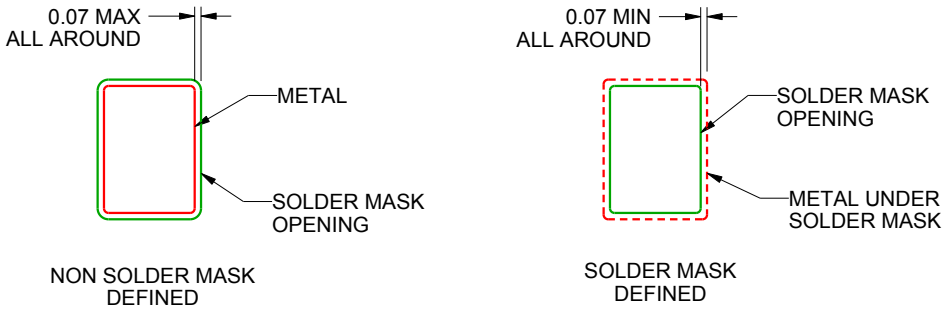
4221443/B 09/2015

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
1:1 RATIO WITH PACKAGE SOLDER PADS
SCALE:8X



SOLDER MASK DETAILS
NOT TO SCALE

4221443/B 09/2015

NOTES: (continued)

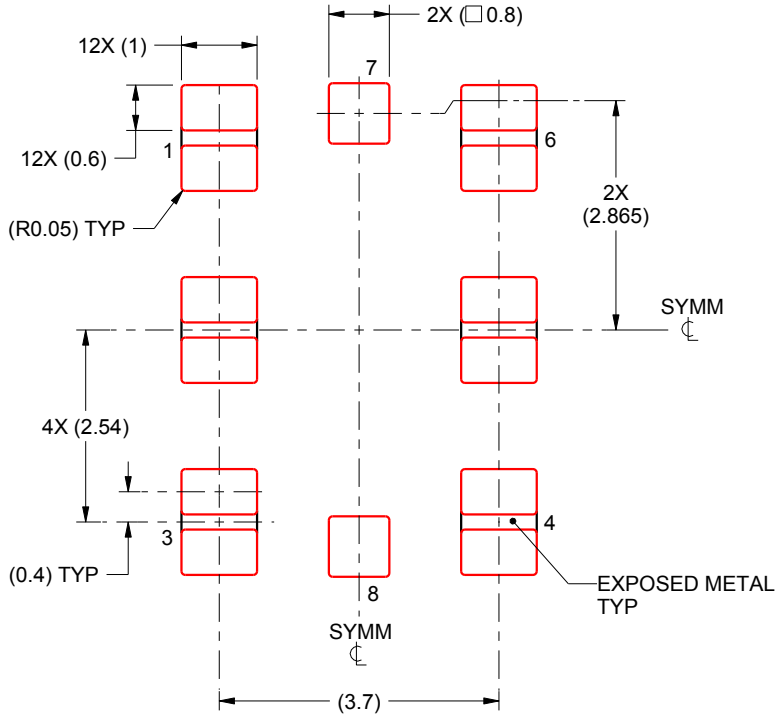
3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).

EXAMPLE STENCIL DESIGN

SIA0008B

QFM - 1.15 mm max height

QUAD FLAT MODULE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

PRINTED SOLDER COVERAGE BY AREA
PADS 1-3 & 4-6: 86%
SCALE:10X

4221443/B 09/2015

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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