TEXAS INSTRUMENTS
LMR23625-Q1
JAJSCQ0B – DECEMBER 2016 – REVISED MARCH 2018

LMR23625-Q1 SIMPLE SWITCHER® 36V、2.5A、同期整流降圧型コンバータ

1 特長

- 車載アプリケーションに対応
- 下記内容でAEC-Q100認定済み：
  - デバイス温度グレード 1: 動作時周囲温度 –40℃～+125°C
  - デバイスHBM ESD分類レベルH1C
  - デバイスCDM ESD分類レベルC4A
- 入力電圧範囲: 4V～36V
- 2.5Aの連続出力電流をサポート
- 同期整流器内蔵
- 最小スイッチオン時間: 60ns
- 設計を容易にする内部補償
- 2.1MHz固定のスイッチング周波数
- 軽負荷時のPFMおよび強制PWMモードのオプション
- 外部クロックへの周波数同期
- PFMオプションのとき、無負荷時の静止電流75µA
- パワー・グッドのオプション
- プリバイアスされた負荷へのソフトスタート
- 高いデューティ・サイクルでの動作をサポート
- ヒカップ・モードによる出力短絡保護
- 8ピンのHSOICと12ピンのWSONウェッタブル・フランク、 PowerPAD™付きのパッケージ・オプション
- WEBENCH® Power Designerにより、LMR23625-Q1を使用するカスタム設計を作成

2 アプリケーション

- 車載用インフォテイメント: クラスタ、ヘッド・ユニット、ヘッドアップ・ディスプレイ
- USB充電
- 一般的なオフ・バッテリ電源アプリケーション

3 概要

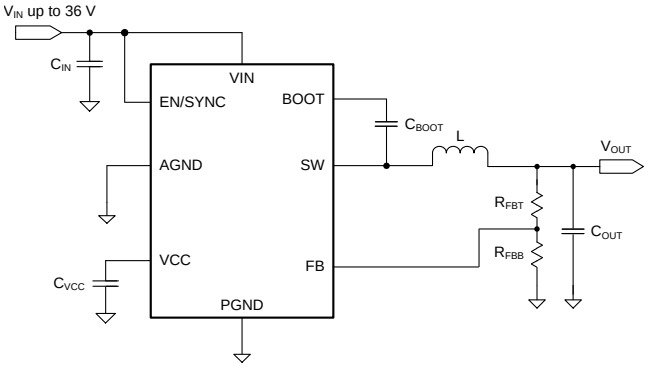
LMR23625-Q1 SIMPLE SWITCHER®は使いやすい36V、2.5Aの同期整流降圧型レギュレータです。4V～36Vという幅広い入力範囲により、産業用から車載向けまで、非レギュレーション電源からの電源調整を行うさまざまなアプリケーションに適しています。ピーク電流モード制御の採用により、単純な制御ループ補償と、サイクル単位の電流制限が実現されています。静止電流が75µAであるため、バッテリ駆動のシステムに適しています。内部ループ補償により、ユーザーはループ補償を設計する煩雑な作業から解放されます。これによって、外付け部品の数も最小限に抑えられます。このデバイスは、軽負荷時に出力電圧リップルを小さくするために、固定周波数の強制パルス幅変調(FPWM)モードを選択できます。拡張ファミリとして、1A (LMR23610-Q1)、1.5A (LMR23615-Q1)、3A (LMR23630-Q1)の負荷電流のオプションがあり、これらはピン単位で互換のパッケージなため、PCBレイアウトが単純になり、最適化されます。高精度のイネーブル入力により、レギュレータ制御とシステムの電力シーケンシングが簡単になります。保護機能として、サイクル単位の電流制限、ヒカップ・モードの短絡保護、過剰な消費電力によるサーマル・シャットダウンが搭載されています。

製品情報(1)

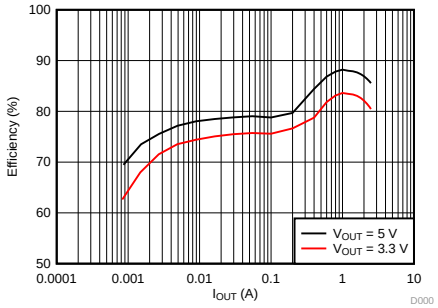
型番	パッケージ	本体サイズ(公称)
LMR23625-Q1	HSOIC (8)	4.90mm×3.90mm
	WSON (12)	3.00mm×3.00mm

(1) 提供されているすべてのパッケージについては、データシートの末尾にある注文情報を参照してください。

概略回路図



効率と負荷との関係、V_{IN} = 12V、PFMオプション



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4 改訂履歴

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Revision A (April 2017) から **Revision B** に変更 **Page**

- 12ピンWSONに「ウェッタブル」を追加 ... 1
- 車載用バッテリ・レギュレーション、産業用電源、テレコムおよびデータコム・システムを削除し、表紙の「アプリケーション」の記述を修正 ... 1
- WSONパッケージ・デバイスのRTMリリースについて編集上の変更 ... 1
- Revising the title for WSON Pin Configuration and Functions to be "12-Pin WSON with PGOOD" ... 3
- Updated the WSON Pin Functions Title to "WSON with PGOOD" ... 3
- Updating the ESD Ratings to include WSON ESD numbers ... 4
- Updating the Electrical Characteristic Table EN Pin to EN/SYNC Pin ... 5
- Adding WSON Only to PGOOD Electrical Characteristic Table ... 5
- Adding WSON Peak and Valley Inductor Current limit row ... 6
- Adding WSON High Side and Low Side MOSFET ON-resistance ... 6

2016年12月発行のものから更新 **Page**

- 先頭ページにWEBENCHへのリンクを追加、効率グラフを 変更 ... 1
- Changed the value of HBM to ±2000 from ±2500 ... 4
- Changed this efficiency graph ... 8
- Updated efficiency graphs ... 8

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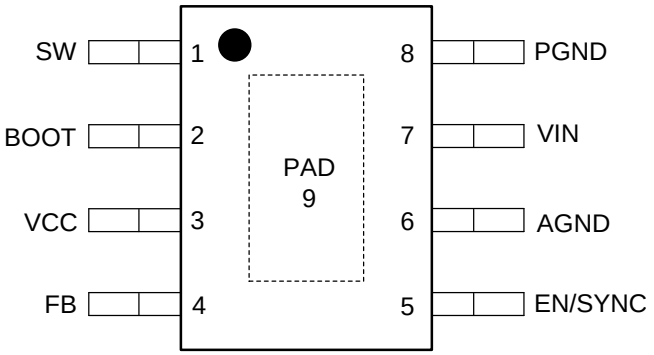
5 Device Comparison

Table 1. Package Comparison

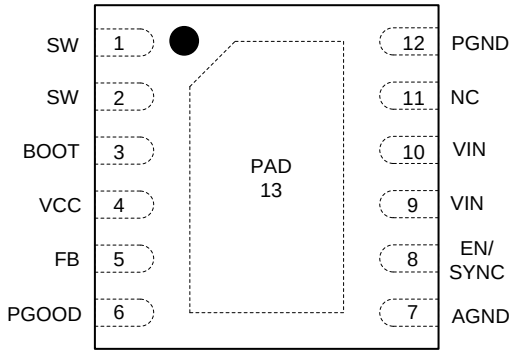
PACKAGE	PART NUMBER	FIXED 2.1 MHz	POWER GOOD	FPWM
SOIC (8)	LMR23625CQDDARQ1	Yes	No	No
	LMR23625CFQDDARQ1	Yes	No	Yes
WSON (12)	LMR23625CFPQDRRRQ1	Yes	Yes	Yes

6 Pin Configuration and Functions

DDA Package
8-Pin SOIC
Top View



DRR Package
12-Pin WSON with PGOOD
Top View



Pin Functions

PIN			I/O (1)	DESCRIPTION
NAME	SOIC	WSON with PGOOD		
SW	1	1, 2	P	Switching output of the regulator. Internally connected to both power MOSFETs. Connect to power inductor.
BOOT	2	3	P	Bootstrap capacitor connection for high-side driver. Connect a high-quality 470-nF capacitor from BOOT to SW.
VCC	3	4	P	Internal bias supply output for bypassing. Connect a 2.2-µF, 16-V or higher capacitance bypass capacitor from this pin to AGND. Do not connect external loading to this pin. Never short this pin to ground during operation.
FB	4	5	A	Feedback input to regulator, connect the feedback resistor divider tap to this pin.
PGOOD	N/A	6	A	Open drain output for power-good flag. Use a 10-kΩ to 100-kΩ pullup resistor to logic rail or other DC voltage no higher than 12 V.
EN/SYNC	5	8	A	Enable input to regulator. High = On, Low = Off. Can be connected to VIN. Do not float. Adjust the input undervoltage lockout with two resistors. The internal oscillator can be synchronized to an external clock by coupling a positive pulse into this pin through a small coupling capacitor. See *EN/SYNC* for detail.
AGND	6	7	G	Analog ground pin. Ground reference for internal references and logic. Connect to system ground.
VIN	7	9, 10	P	Input supply voltage.
PGND	8	12	G	Power ground pin, connected internally to the low side power FET. Connect to system ground, PAD, AGND, ground pins of C_{IN} and C_{OUT}. Path to C_{IN} must be as short as possible.
PAD	9	13	G	Low impedance connection to AGND. Connect to PGND on PCB. Major heat dissipation path of the die. Must be used for heat sinking to ground plane on PCB.
NC	N/A	11	N/A	Not for use. Leave this pin floating.

(1) A = Analog, P = Power, G = Ground.

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7 Specifications

7.1 Absolute Maximum Ratings

Over the recommended operating junction temperature range of –40°C to 125°C (unless otherwise noted) (1)

PARAMETER		MIN	MAX	UNIT
Input voltages	VIN to PGND	–0.3	42	V
	EN/SYNC to AGND	–5.5	V_{IN} + 0.3	
	FB to AGND	–0.3	4.5	
	PGOOD to AGND	–0.3	15	
	AGND to PGND	–0.3	0.3	
Output voltages	SW to PGND	–1	V_{IN} + 0.3	V
	SW to PGND less than 10-ns transients	–5	42	
	BOOT to SW	–0.3	5.5	
	VCC to AGND	–0.3	4.5 (2)	
Junction temperature, T_J		–40	150	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) In shutdown mode, the VCC to AGND maximum value is 5.25 V.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM) for SOIC (1)	±2000	V
		Human-body model (HBM) for WSON with PGOOD	±2500	
		Charged-device model (CDM) for SOIC	±1000	
		Charged-device model (CDM) for WSON with PGOOD	±750	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

7.3 Recommended Operating Conditions

Over the recommended operating junction temperature range of –40°C to 125°C (unless otherwise noted) (1)

		MIN	MAX	UNIT
Input voltage	VIN	4	36	V
	EN/SYNC	–5	36	
	FB	–0.3	1.2	
	PGOOD	–0.3	12	
Input current	PGOOD pin current	0	1	mA
Output voltage, V_{OUT}		1	28	V
Output current, I_{OUT}		0	2.5	A
Operating junction temperature, T_J		–40	125	°C

(1) Recommended Operating Ratings indicate conditions for which the device is intended to be functional, but do not ensured specific performance limits. For specified specifications, see *Electrical Characteristics*.

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7.4 Thermal Information

THERMAL METRIC(1)(2)		LMR23625-Q1 DDA (SOIC) 8 PINS	LMR23625-Q1 DDR (WSON 12 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	42.0	41.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	5.9	0.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	23.4	16.5	°C/W
ψ_{JT}	Junction-to-top characterization parameter	45.8	39.1	°C/W
ψ_{JB}	Junction-to-board characterization parameter	3.6	3.4	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	23.4	16.3	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.
(2) Determine power rating at a specific ambient temperature (T_A) with a maximum junction temperature (T_J) of 125°C, which is illustrated in *Recommended Operating Conditions* section.

7.5 Electrical Characteristics

Limits apply over the recommended operating junction temperature (T_J) range of –40°C to +125°C, unless otherwise stated. Minimum and Maximum limits are specified through test, design or statistical correlation. Typical values represent the most likely parametric norm at T_J = 25°C, and are provided for reference purposes only.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLY (VIN PIN)						
V_{IN}	Operation input voltage		4		36	V
VIN_UVLO	Undervoltage lockout thresholds	Rising threshold	3.3	3.7	3.9	V
		Falling threshold	2.9	3.3	3.5	
I_{SHDN}	Shutdown supply current	V_{EN} = 0 V, V_{IN} = 12 V, T_J = –40°C to 125°C		2	4	µA
I_Q	Operating quiescent current (non-switching)	V_{IN} =12 V, V_{FB} = 1.1 V, T_J = –40°C to 125°C, PFM mode		75		µA
ENABLE (EN/SYNC PIN)						
V_{EN_H}	Enable rising threshold voltage		1.4	1.55	1.7	V
V_{EN_HYS}	Enable hysteresis voltage			0.4		V
V_{WAKE}	Wake-up threshold		0.4			V
I_{EN}	Input leakage current at EN pin	V_{IN} = 4 V to 36 V, V_{EN}= 2 V		10	100	nA
		V_{IN} = 4 V to 36 V, V_{EN}= 36 V			1	µA
VOLTAGE REFERENCE (FB PIN)						
V_{REF}	Reference voltage	V_{IN} = 4 V to 36 V, T_J = 25°C	0.985	1	1.015	V
		V_{IN} = 4 V to 36 V, T_J = –40°C to 125°C	0.98	1	1.02	
I_{LKG_FB}	Input leakage current at FB pin	V_{FB}= 1 V		10		nA
POWER GOOD (PGOOD PIN) WSON Only						
V_{PG_OV}	Power-good flag overvoltage tripping threshold	% of reference voltage	104%	107%	110%	
V_{PG_UV}	Power-good flag undervoltage tripping threshold	% of reference voltage	92%	94%	96.5%	
V_{PG_HYS}	Power-good flag recovery hysteresis			1.5%		
$V_{IN_PG_MIN}$	Minimum V_{IN} for valid PGOOD output	50 µA pullup to PGOOD pin, V_{EN} = 0 V, T_J = 25°C			1.5	V
V_{PG_LOW}	PGOOD low level output voltage	50 µA pullup to PGOOD pin, V_{IN} = 1.5 V, V_{EN} = 0 V			0.4	V
		0.5 mA pullup to PGOOD pin, V_{IN} =13.5 V, V_{EN} = 0 V			0.4	
INTERNAL LDO (VCC PIN)						
V_{CC}	Internal LDO output voltage			4.1		V
VCC_UVLO	VCC undervoltage lockout thresholds	Rising threshold	2.8	3.2	3.6	V
		Falling threshold	2.4	2.8	3.2	

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Electrical Characteristics (continued)

Limits apply over the recommended operating junction temperature (T_J) range of –40°C to +125°C, unless otherwise stated. Minimum and Maximum limits are specified through test, design or statistical correlation. Typical values represent the most likely parametric norm at T_J = 25°C, and are provided for reference purposes only.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
CURRENT LIMIT						
I_{HS_LIMIT}	Peak inductor current limit	HSOIC package	3.6	4.8	6.2	A
		WSON package	4.0	5.5	6.6	
I_{LS_LIMIT}	Valley inductor current limit	HSOIC package	2.8	3.5	4.6	A
		WSON package	2.9	3.6	4.2	
I_{L_ZC}	Zero cross current limit			–0.04		A
I_{L_NEG}	Negative current limit (FPWM option)		–2.7	–2	–1.3	A
INTEGRATED MOSFETS						
$R_{DS_ON_HS}$	High-side MOSFET ON-resistance	HSOIC package, V_{IN} = 12 V, I_{OUT} = 1 A		185		mΩ
		WSON package, V_{IN} = 12 V, I_{OUT} = 1 A		160		
$R_{DS_ON_LS}$	Low-side MOSFET ON-resistance	HSOIC package V_{IN} = 12 V, I_{OUT} = 1 A		105		mΩ
		WSON package, V_{IN} = 12 V, I_{OUT} = 1 A		95		
THERMAL SHUTDOWN						
T_{SHDN}	Thermal shutdown threshold		162	170	178	°C
T_{HYS}	Hysteresis			15		°C

7.6 Timing Characteristics

Over the recommended operating junction temperature range of –40°C to +125°C (unless otherwise noted)

			MIN	NOM	MAX	UNIT
HICCUP MODE						
N_{OC} (1)	Number of cycles that LS current limit is tripped to enter hiccup mode			64		Cycles
T_{OC}	Hiccup retry delay time	SOIC package		5		ms
		WSON package		12		
SOFT START						
T_{SS}	Internal soft-start time. The time of internal reference to increase from 0 V to 1 V	SOIC package	1	2	3	ms
		WSON package		6		
POWER GOOD						
T_{PGOOD_RISE}	Power-good flag rising transition deglitch delay			150		µs
T_{PGOOD_FALL}	Power-good flag falling transition deglitch delay			18		µs

(1) Specified by design.

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7.7 Switching Characteristics

Over the recommended operating junction temperature range of –40°C to +125°C (unless otherwise noted)

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
SW (SW PIN)						
f_{SW}	Default switching frequency		1785	2100	2415	kHz
T_{ON_MIN}	Minimum turnon time			60	90	ns
T_{OFF_MIN} (1)	Minimum turnoff time			100		ns
SYNC (EN/SYNC PIN)						
f_{SYNC}	SYNC frequency range		200		2200	kHz
V_{SYNC}	Amplitude of SYNC clock AC signal (measured at SYNC pin)		2.8		5.5	V
T_{SYNC_MIN}	Minimum sync clock ON and OFF time			100		ns

(1) Specified by design.

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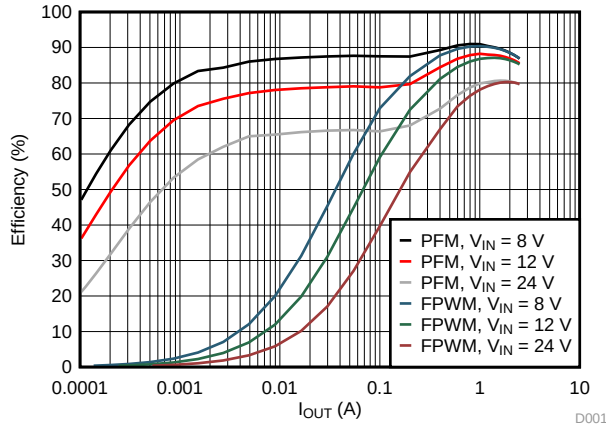
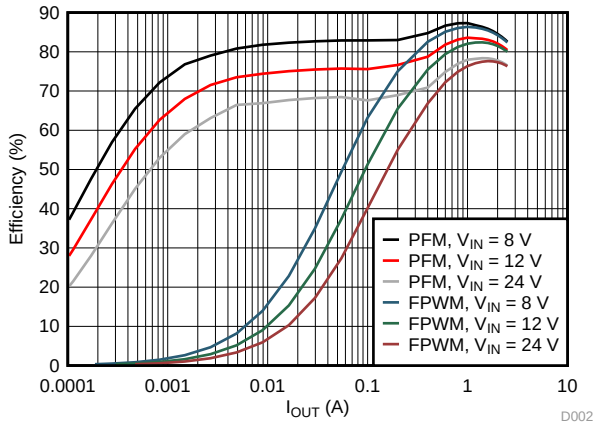
7.8 Typical Characteristics

Unless otherwise specified the following conditions apply: V_{IN} = 12 V, f_{SW} = 2100 kHz, L = 2.2 µH, C_{OUT} = 47 µF, T_A = 25°C.



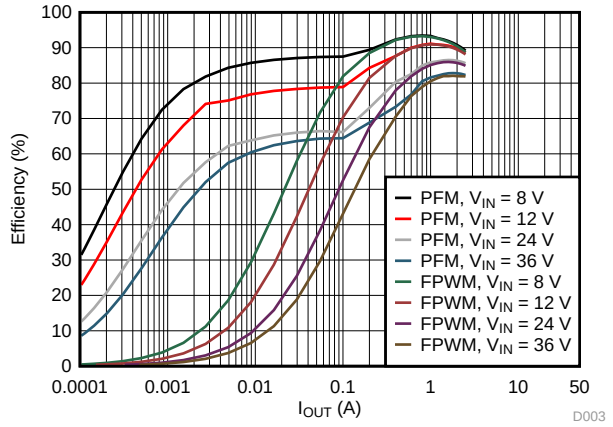
f_{SW} = 2100 kHz V_{OUT} = 5 V

Figure 1. Efficiency vs Load Current



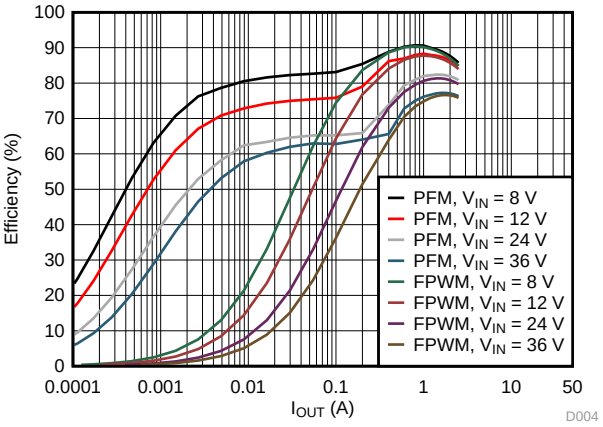
f_{SW} = 2100 kHz V_{OUT} = 3.3 V

Figure 2. Efficiency vs Load Current



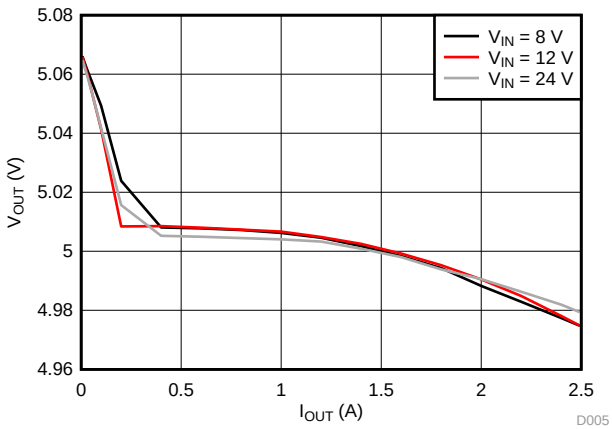
f_{SW} = 1000 kHz (Sync) V_{OUT} = 5 V

Figure 3. Efficiency vs Load Current



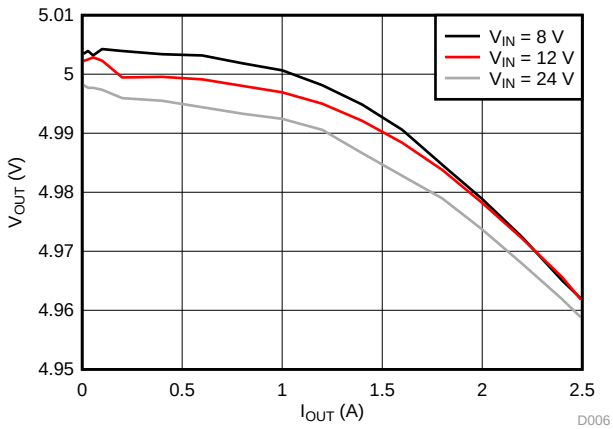
f_{SW} = 1000 kHz (Sync) V_{OUT} = 3.3 V

Figure 4. Efficiency vs Load Current



PFM Option V_{OUT} = 5 V

Figure 5. Load Regulation



FPWM Option V_{OUT} = 5 V

Figure 6. Load Regulation

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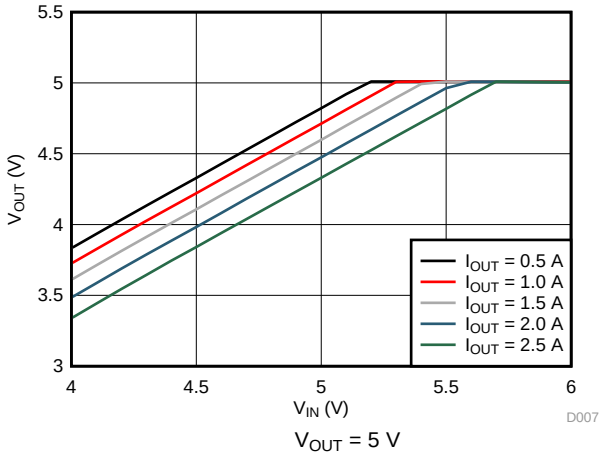
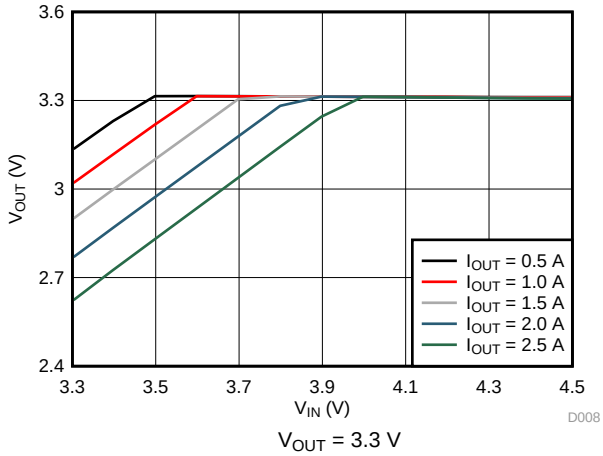
Typical Characteristics (continued)

Unless otherwise specified the following conditions apply: V_{IN} = 12 V, f_{SW} = 2100 kHz, L = 2.2 µH, C_{OUT} = 47 µF, T_A = 25°C.



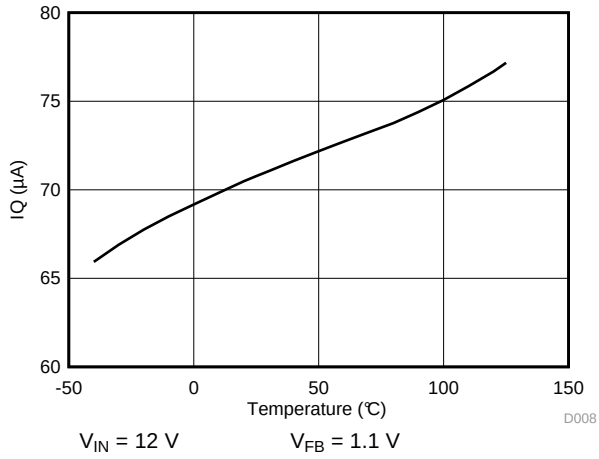
V_{OUT} = 5 V

Figure 7. Dropout Curve



V_{OUT} = 3.3 V

Figure 8. Dropout Curve



V_{IN} = 12 V V_{FB} = 1.1 V

Figure 9. I_Q vs Junction Temperature

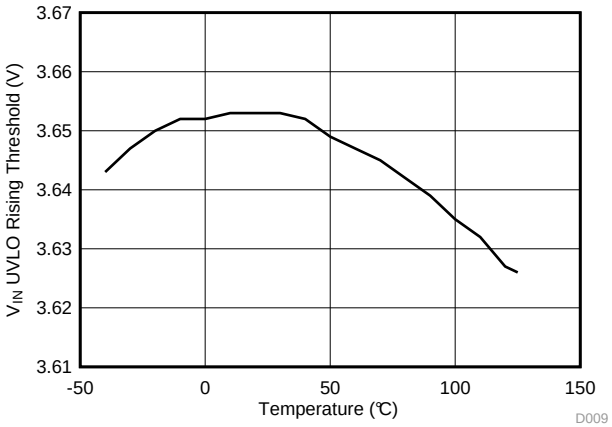


Figure 10. VIN UVLO Rising Threshold vs Junction Temperature

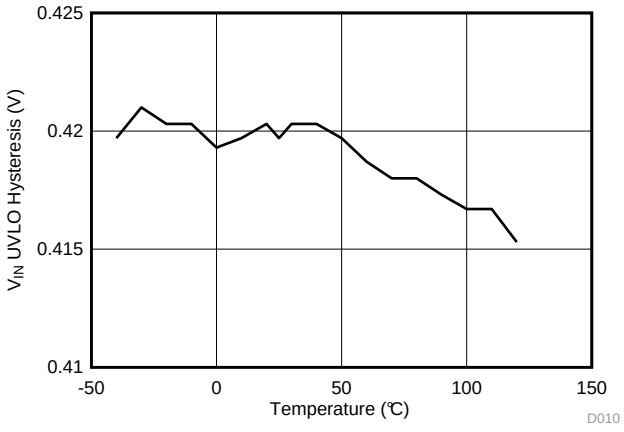
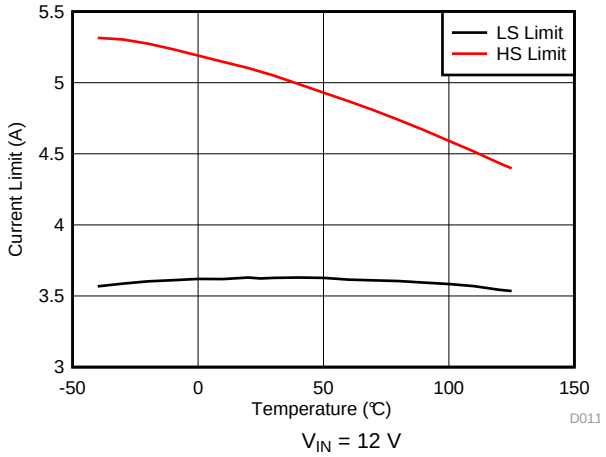


Figure 11. VIN UVLO Hysteresis vs Junction Temperature



V_{IN} = 12 V

Figure 12. HS and LS Current Limit vs Junction Temperature

8 Detailed Description

8.1 Overview

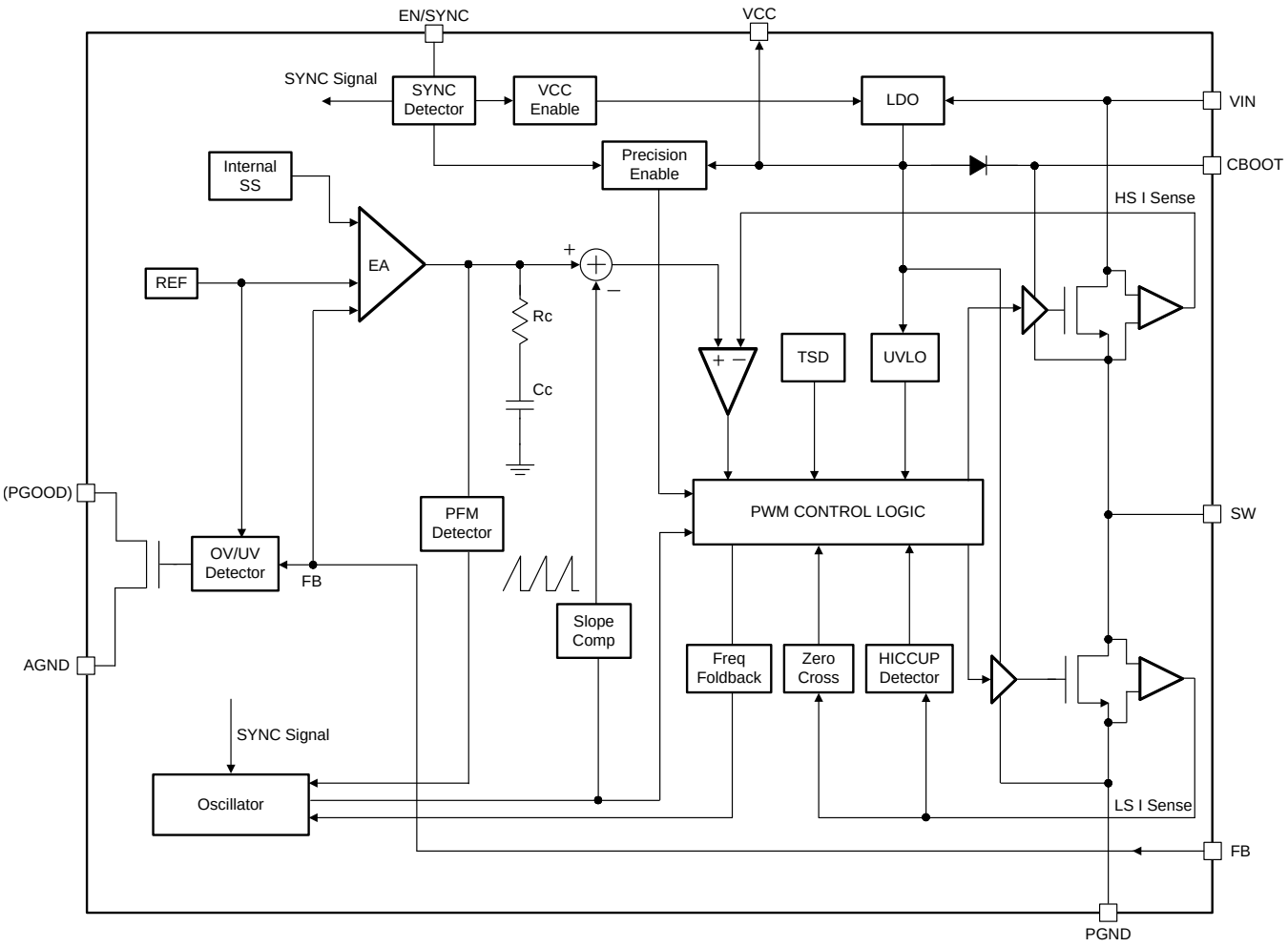
The LMR23625-Q1 SIMPLE SWITCHER® regulator is an easy-to-use synchronous step-down DC-DC converter operating from a 4-V to 36-V supply voltage. It is capable of delivering up to 2.5-A, DC-load current with good thermal performance in a small solution size. An extended family is available, for both the SOIC and WSON packages, in multiple current options from 1 A to 3 A in pin-to-pin compatible packages.

The LMR23625-Q1 employs fixed-frequency peak-current-mode control. The device enters PFM mode at light load to achieve high efficiency. A user-selectable FPWM option is provided to achieve low output voltage ripple, tight output voltage regulation, and constant switching frequency. The device is internally compensated, which reduces design time and requires few external components. The LMR23625-Q1 is capable of synchronization to an external clock within the range of 200 kHz to 2.2 MHz.

Additional features such as precision enable, power-good flag, and internal soft-start provide a flexible and easy to use solution for a wide range of applications. Protection features include thermal shutdown, VIN and VCC undervoltage lockout (UVLO), cycle-by-cycle current limit, and hiccup-mode short-circuit protection.

The family requires very few external components and has a pinout designed for simple, optimum PCB layout.

8.2 Functional Block Diagram



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8.3 Feature Description

8.3.1 Fixed-Frequency Peak-Current-Mode Control

The following operating description of the LMR23625-Q1 refer to the *Functional Block Diagram* and to the waveforms in Figure 13. LMR23625-Q1 is a step-down synchronous buck regulator with integrated high-side (HS) and low-side (LS) switches (synchronous rectifier). The LMR23625-Q1 supplies a regulated output voltage by turning on the HS and LS NMOS switches with controlled duty cycle. During high-side switch ON time, the SW pin voltage swings up to approximately V_{IN}, and the inductor current i_L increase with linear slope ($V_{IN} – V_{OUT}$) / L. When the HS switch is turned off by the control logic, the LS switch is turned on after an anti-shoot-through dead time. Inductor current discharges through the LS switch with a slope of $–V_{OUT}$ / L. The control parameter of a buck converter is defined as duty cycle D = t_{ON} / T_{SW}, where t_{ON} is the high-side switch ON time and T_{SW} is the switching period. The regulator control loop maintains a constant output voltage by adjusting the duty cycle D. In an ideal buck converter, where losses are ignored, D is proportional to the output voltage and inversely proportional to the input voltage: D = V_{OUT} / V_{IN}.

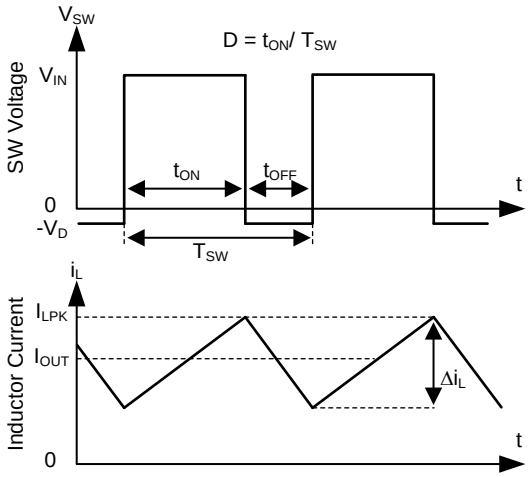

Figure 13. SW Node and Inductor Current Waveforms in Continuous Conduction Mode (CCM)

The LMR23625-Q1 employs fixed-frequency peak-current-mode control. A voltage feedback loop is used to get accurate DC voltage regulation by adjusting the peak current command based on voltage offset. The peak inductor current is sensed from the high-side switch and compared to the peak current threshold to control the ON-time of the high-side switch. The voltage feedback loop is internally compensated, which allows for fewer external components, makes it easy to design, and provides stable operation with almost any combination of output capacitors. The regulator operates with fixed switching frequency at normal load condition. At light load condition, the LMR23625-Q1 operates in PFM mode to maintain high efficiency (PFM option) or in FPWM mode for low output voltage ripple, tight output voltage regulation, and constant switching frequency (FPWM option).

8.3.2 Adjustable Output Voltage

A precision 1-V reference voltage is used to maintain a tightly regulated output voltage over the entire operating temperature range. The output voltage is set by a resistor divider from output voltage to the FB pin. TI recommends using 1% tolerance resistors with a low temperature coefficient for the FB divider. Select the low-side resistor R_{FBB} for the desired divider current and use Equation 1 to calculate high-side R_{FBT}. R_{FBT} in the range from 10 kΩ to 100 kΩ is recommended for most applications. A lower R_{FBT} value can be used if static loading is desired to reduce V_{OUT} offset in PFM operation. Lower R_{FBT} reduces efficiency at very light load. Less static current goes through a larger R_{FBT} and might be more desirable when light load efficiency is critical. R_{FBT} larger than 1 MΩ is not recommended because it makes the feedback path more susceptible to noise. Larger R_{FBT} value requires more carefully designed feedback path on the PCB. The tolerance and temperature variation of the resistor dividers affect the output voltage regulation.

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Feature Description (continued)

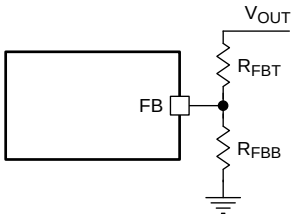

Figure 14. Output Voltage Setting

$$R_{FBT} = \frac{V_{OUT} - V_{REF}}{V_{REF}} \times R_{FBB} \quad (1)$$

8.3.3 EN/SYNC

The voltage on the EN pin controls the ON or OFF operation of LMR23625-Q1. A voltage less than 1 V (typical) shuts down the device while a voltage higher than 1.6 V (typical) is required to start the regulator. The EN pin is an input and cannot be left open or floating. The simplest way to enable the operation of the LMR23625-Q1 is to connect the EN to V_{IN}. This allows self-start-up of the LMR23625-Q1 when V_{IN} is within the operation range.

Many applications benefit from the employment of an enable divider R_{ENT} and R_{ENB} (Figure 15) to establish a precision system UVLO level for the converter. System UVLO can be used for supplies operating from utility power as well as battery power. It can be used for sequencing, ensuring reliable operation, or supply protection, such as a battery discharge level. An external logic signal can also be used to drive EN input for system sequencing and protection.

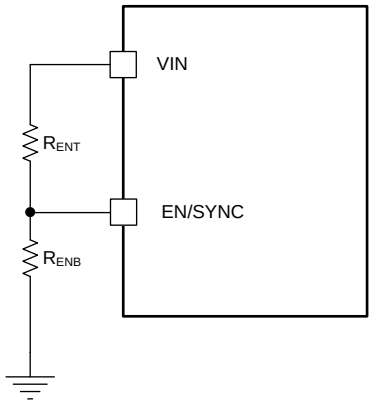

Figure 15. System UVLO by Enable Divider

The EN pin also can be used to synchronize the internal oscillator to an external clock. The internal oscillator can be synchronized by AC coupling a positive edge into the EN pin. The AC-coupled peak-to-peak voltage at the EN pin must exceed the SYNC amplitude threshold of 2.8 V (typical) to trip the internal synchronization pulse detector, and the minimum SYNC clock ON- and OFF-time must be longer than 100 ns (typical). A 3.3-V or a higher amplitude pulse signal coupled through a 1-nF capacitor C_{SYNC} is a good starting point. Keeping R_{ENT} // R_{ENB} (R_{ENT} parallel with R_{ENB}) in the 100-kΩ range is a good choice. R_{ENT} is required for this synchronization circuit, but R_{ENB} can be left unmounted if system UVLO is not needed. LMR23625-Q1 switching action can be synchronized to an external clock from 200 kHz to 2.2 MHz. Figure 17 and Figure 18 show the device synchronized to an external system clock.

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Feature Description (continued)

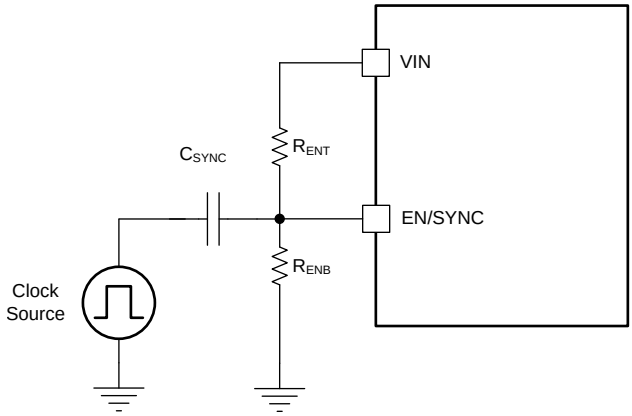

Figure 16. Synchronize to External Clock

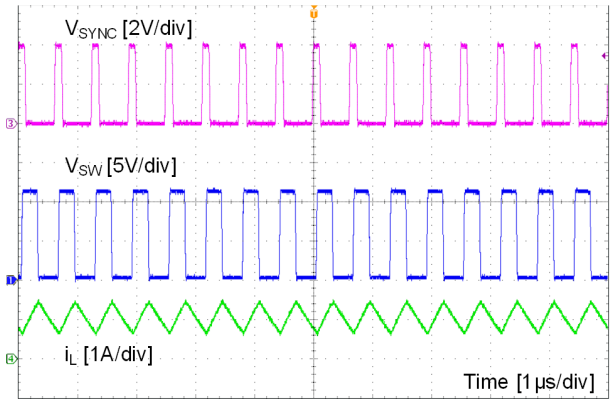

Figure 17. Synchronizing in PWM Mode

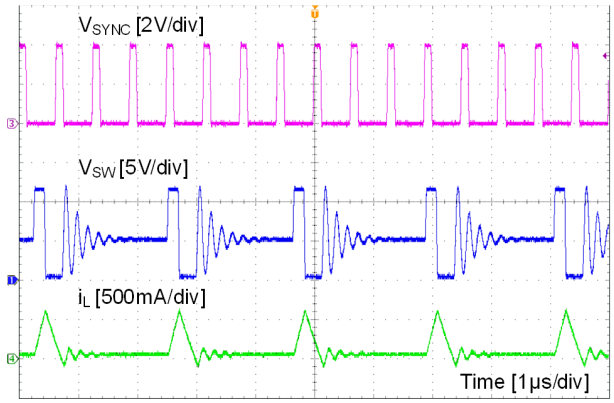

Figure 18. Synchronizing in PFM Mode

8.3.4 VCC, UVLO

The LMR23625-Q1 integrates an internal LDO to generate V_{CC} for control circuitry and MOSFET drivers. The nominal voltage for V_{CC} is 4.1 V. The VCC pin is the output of an LDO and must be properly bypassed. Place high-quality ceramic capacitor with a value of 2.2 µF to 10 µF, 16 V or higher rated voltage as close as possible to VCC and grounded to the exposed PAD and ground pins. The VCC output pin must not be loaded or shorted to ground during operation. Shorting VCC to ground during operation may cause damage to the LMR23625-Q1 device.

VCC UVLO prevents the LMR23625-Q1 from operating until the V_{CC} voltage exceeds 3.2 V (typical). The VCC UVLO threshold has 400 mV (typical) of hysteresis to prevent undesired shutdown due to temporary V_{IN} drops.

8.3.5 Minimum ON-Time, Minimum OFF-Time and Frequency Foldback at Dropout Conditions

Minimum ON-time, T_{ON_MIN}, is the smallest duration of time that the HS switch can be on. T_{ON_MIN} is typically 60 ns in the LMR23625-Q1. Minimum OFF-time, T_{OFF_MIN}, is the smallest duration that the HS switch can be off. T_{OFF_MIN} is typically 100 ns in the LMR23625-Q1. In CCM operation, T_{ON_MIN} and T_{OFF_MIN} limit the voltage conversion range given a selected switching frequency.

The minimum duty cycle allowed is:

$$D_{MIN} = T_{ON_MIN} \times f_{SW} \quad (2)$$

And the maximum duty cycle allowed is:

$$D_{MAX} = 1 - T_{OFF_MIN} \times f_{SW} \quad (3)$$

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Feature Description (continued)

Given fixed T_{ON_MIN} and T_{OFF_MIN}, the higher the switching frequency the narrower the range of the allowed duty cycle. In the LMR23625-Q1, a frequency foldback scheme is employed to extend the maximum duty cycle when T_{OFF_MIN} is reached. The switching frequency decreases once longer duty cycle is needed under low V_{IN} conditions. Wide range of frequency foldback allows the LMR23625-Q1 output voltage stay in regulation with a much lower supply voltage V_{IN}. This leads to a lower effective dropout voltage.

Given an output voltage, the choice of the switching frequency affects the allowed input voltage range, solution size, and efficiency. The maximum operation supply voltage can be found by:

$$V_{IN_MAX} = \frac{V_{OUT}}{\left(f_{SW} \times T_{ON_MIN}\right)} \quad (4)$$

At lower supply voltage, the switching frequency decreases once T_{OFF_MIN} is tripped. The minimum V_{IN} without frequency foldback can be approximated by:

$$V_{IN_MIN} = \frac{V_{OUT}}{\left(1 - f_{SW} \times T_{OFF_MIN}\right)} \quad (5)$$

Taking considerations of power losses in the system with heavy load operation, V_{IN_MAX} is higher than the result calculated in Equation 4. With frequency foldback, V_{IN_MIN} is lowered by decreased f_{SW}.

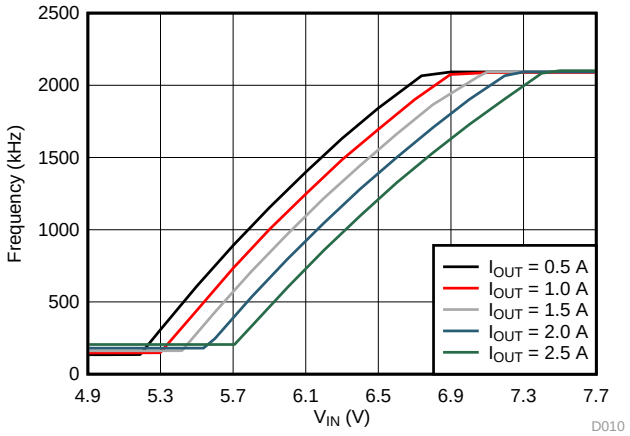

Figure 19. Frequency Foldback at Dropout (V_{OUT} = 5 V, f_{SW} = 2100 kHz)

8.3.6 Power Good (PGOOD)

The LMR23625AP has a built-in power-good flag shown on PGOOD pin to indicate whether the output voltage is within its regulation level. The PGOOD signal can be used for start-up sequencing of multiple rails or fault protection. The PGOOD pin is an open-drain output that requires a pullup resistor to an appropriate DC voltage. Voltage detected by the PGOOD pin must never exceed 15 V; limit the maximum current into this pin to 1 mA. A resistor divider pair can be used to divide the voltage down from a higher potential. A typical range of pullup resistor value is 10 kΩ to 100 kΩ.

When the FB voltage is within the power-good band, +6% above and –6% below the internal reference VREF typically, the PGOOD switch is turned off, and the PGOOD voltage is pulled up to the voltage level defined by the pullup resistor or divider. When the FB voltage is outside of the tolerance band, +7% above or –7% below VREF typically, the PGOOD switch is turned on, and the PGOOD pin voltage is pulled low to indicate power bad. A glitch filter prevents false-flag operation for short excursions in the output voltage, such as during line and load transients. The values for the various filter and delay times can be found in *Typical Characteristics*. Power-good operation can best be understood by reference to Figure 20.

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Feature Description (continued)

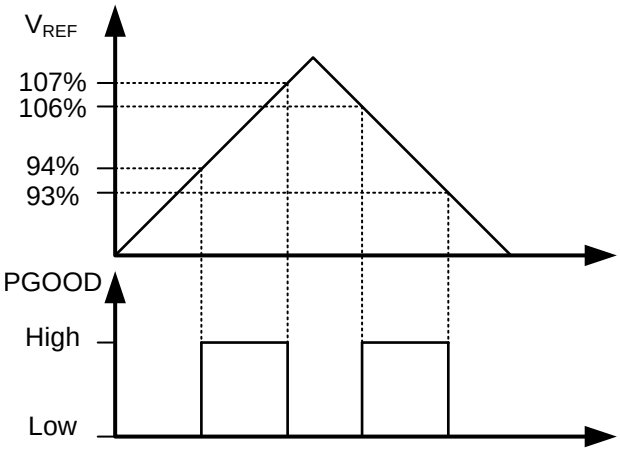

Figure 20. Power-Good Flag

8.3.7 Internal Compensation and C_{FF}

The LMR23625-Q1 is internally compensated as shown in *Functional Block Diagram*. The internal compensation is designed such that the loop response is stable over the entire operating frequency and output voltage range. Depending on the output voltage, the compensation loop phase margin can be low with all ceramic capacitors. An external feed-forward capacitor C_{FF} is recommended to be placed in parallel with the top resistor divider R_{FBT} for optimum transient performance.

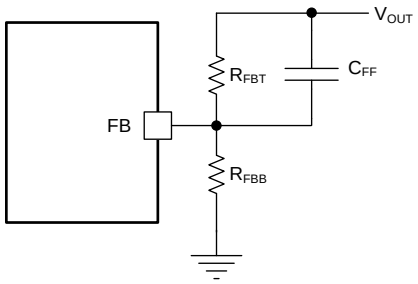

Figure 21. Feed-forward Capacitor for Loop Compensation

The feed-forward capacitor C_{FF} in parallel with R_{FBT} places an additional zero before the crossover frequency of the control loop to boost phase margin. The zero frequency can be found by:

$$f_{Z_CFF} = \frac{1}{\left(2\pi \times C_{FF} \times R_{FBT}\right)} \quad (6)$$

An additional pole is also introduced with C_{FF} at the frequency of:

$$f_{P_CFF} = \frac{1}{\left(2\pi \times C_{FF} \times R_{FBT} // R_{FBB}\right)} \quad (7)$$

The zero f_{Z_CFF} adds phase boost at the crossover frequency and improves transient response. The pole $f_{P\text{-}CFF}$ helps maintaining proper gain margin at frequency beyond the crossover. Table 2 lists the combination of C_{OUT}, C_{FF} and R_{FBT} for typical applications, designs with similar C_{OUT} but R_{FBT} other than recommended value, adjust C_{FF} such that (C_{FF} × R_{FBT}) is unchanged, and adjust R_{FBB} such that (R_{FBT} / R_{FBB}) is unchanged.

Designs with different combinations of output capacitors need different C_{FF}. Different types of capacitors have different equivalent series resistance (ESR). Ceramic capacitors have the smallest ESR and need the most C_{FF}. Electrolytic capacitors have much larger ESR and the ESR zero frequency would be low enough to boost the phase up around the crossover frequency. Designs using mostly electrolytic capacitors at the output may not need any C_{FF}. See Equation 8

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Feature Description (continued)

$$f_{Z_ESR} = \frac{1}{(2\pi \times C_{OUT} \times ESR)} \quad (8)$$

The C_{FF} creates a time constant with R_{FBT} that couples in the attenuate output voltage ripple to the FB node. If the C_{FF} value is too large, it can couple too much ripple to the FB and affect V_{OUT} regulation. Therefore, calculate C_{FF} based on output capacitors used in the system. At cold temperatures, the value of C_{FF} might change based on the tolerance of the chosen component. This may reduce its impedance and ease noise coupling on the FB node. To avoid this, more capacitance can be added to the output or the value of C_{FF} can be reduced.

8.3.8 Bootstrap Voltage (BOOT)

The LMR23625-Q1 provides an integrated bootstrap voltage regulator. A small capacitor between the BOOT and SW pins provides the gate-drive voltage for the high-side MOSFET. The BOOT capacitor is refreshed when the high-side MOSFET is off and the low-side switch conducts. The recommended value of the BOOT capacitor is 0.1 μF. TI recommends a ceramic capacitor with an X7R or X5R grade dielectric with a voltage rating of 16V or higher for stable performance over temperature and voltage.

8.3.9 Overcurrent and Short-Circuit Protection

The LMR23625-Q1 is protected from overcurrent conditions by cycle-by-cycle current limit on both the peak and valley of the inductor current. Hiccup mode is activated if a fault condition persists to prevent overheating.

High-side MOSFET overcurrent protection is implemented by the nature of the peak-current-mode control. The HS switch current is sensed when the HS is turned on after a set blanking time. The HS switch current is compared to the output of the error amplifier (EA) minus slope compensation every switching cycle. See the *Functional Block Diagram* for more details. The peak current of HS switch is limited by a clamped maximum-peak-current threshold I_{HS_LIMIT}, which is constant. So the peak-current limit of the high-side switch is not affected by the slope compensation and remains constant over the full duty-cycle range.

The current going through LS MOSFET is also sensed and monitored. When the LS switch turns on, the inductor current begins to ramp down. The LS switch is not turned OFF at the end of a switching cycle if its current is above the LS current limit I_{LS_LIMIT}. The LS switch is kept ON so that inductor current keeps ramping down, until the inductor current ramps below the LS current limit I_{LS_LIMIT}. The LS switch is then turned OFF, and the HS switch is turned on after a dead time. This is somewhat different than the more typical peak-current limit and results in Equation 9 for the maximum load current.

$$I_{OUT_MAX} = I_{LS_LIMIT} + \frac{(V_{IN} - V_{OUT})}{2 \times f_{SW} \times L} \times \frac{V_{OUT}}{V_{IN}} \quad (9)$$

If the current of the LS switch is higher than the LS current limit for 64 consecutive cycles, hiccup current protection mode is activated. In hiccup mode the regulator is shut down and kept off for 5 ms typically before the LMR23625-Q1 tries to start again. If overcurrent or short-circuit fault condition still exists, hiccup repeats until the fault condition is removed. Hiccup mode reduces power dissipation under severe overcurrent conditions, prevents overheating and potential damage to the device.

For FPWM option, the inductor current is allowed to go negative. If this current exceeds I_{L_NEG}, the LS switch is turned off until the next clock cycle. This is used to protect the LS switch from excessive negative current.

8.3.10 Thermal Shutdown

The LMR23625-Q1 provides an internal thermal shutdown to protect the device when the junction temperature exceeds 170°C (typical). The device is turned off when thermal shutdown activates. Once the die temperature falls below 155°C (typical), the device reinitiates the power-up sequence controlled by the internal soft-start circuitry.

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8.4 Device Functional Modes

8.4.1 Shutdown Mode

The EN pin provides electrical ON and OFF control for the LMR23625-Q1. When V_{EN} is below 1 V (typical), the device is in shutdown mode. The LMR23625-Q1 also employs VIN and VCC UVLO protection. If V_{IN} or V_{CC} voltage is below their respective UVLO level, the regulator is turned off.

8.4.2 Active Mode

The LMR23625-Q1 is in active mode when V_{EN} is above the precision enable threshold, V_{IN} and V_{CC} are above their respective UVLO level. The simplest way to enable the LMR23625-Q1 is to connect the EN pin to VIN pin. This allows self startup when the input voltage is in the operating range: 4 V to 36 V. See *VCC, UVLO and EN/SYNC* for details on setting these operating levels.

In active mode, depending on the load current, the LMR23625-Q1 is in one of four modes:

1. Continuous conduction mode (CCM) with fixed switching frequency when load current is above half of the peak-to-peak inductor current ripple (for both PFM and FPWM options).
2. Discontinuous conduction mode (DCM) with fixed switching frequency when load current is lower than half of the peak-to-peak inductor current ripple in CCM operation (only for PFM option).
3. Pulse frequency modulation mode (PFM) when switching frequency is decreased at very light load (only for PFM option).
4. Forced pulse width modulation mode (FPWM) with fixed switching frequency even at light load (only for FPWM option).

8.4.3 CCM Mode

CCM operation is employed in the LMR23625-Q1 when the load current is higher than half of the peak-to-peak inductor current. In CCM operation, the frequency of operation is fixed, output voltage ripple is at a minimum in this mode and the maximum output current of 2.5 A can be supplied by the LMR23625-Q1.

8.4.4 Light Load Operation (PFM Option)

For PFM option, when the load current is lower than half of the peak-to-peak inductor current in CCM, the LMR23625-Q1 operates in DCM, also known as diode emulation mode (DEM). In DCM, the LS switch is turned off when the inductor current drops to I_{L_ZC} (–40 mA typical). Both switching losses and conduction losses are reduced in DCM, compared to forced PWM operation at light load.

At even lighter current loads, PFM is activated to maintain high efficiency operation. When either the minimum HS switch ON-time (t_{ON_MIN}) or the minimum peak inductor current I_{PEAK_MIN} (300 mA typical) is reached, the switching frequency decreases to maintain regulation. In PFM, switching frequency is decreased by the control loop when load current reduces to maintain output voltage regulation. Switching loss is further reduced in PFM operation due to less frequent switching actions. The external clock synchronizing is not valid when LMR23625-Q1 enters into PFM mode.

8.4.5 Light Load Operation (FPWM Option)

For FPWM option, LMR23625-Q1 is locked in PWM mode at full load range. This operation is maintained, even at no-load, by allowing the inductor current to reverse its normal direction. This mode trades off reduced light load efficiency for low output voltage ripple, tight output voltage regulation, and constant switching frequency. In this mode, a negative current limit of I_{L_NEG} is imposed to prevent damage to the regulators low side FET. When in FPWM mode the converter synchronizes to any valid clock signal on the EN/SYNC input.

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9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The LMR23625-Q1 is a step-down DC-to-DC regulator. It is typically used to convert a higher DC voltage to a lower DC voltage with a maximum output current of 2.5 A. The following design procedure can be used to select components for the LMR23625-Q1. Alternately, the WEBENCH software may be used to generate complete designs. When generating a design, the WEBENCH software utilizes iterative design procedure and accesses comprehensive databases of components. See *Custom Design With WEBENCH® Tools* and ti.com for more details.

9.2 Typical Applications

The LMR23625-Q1 only requires a few external components to convert from a wide voltage-range supply to a fixed-output voltage. Figure 22 shows a basic schematic.

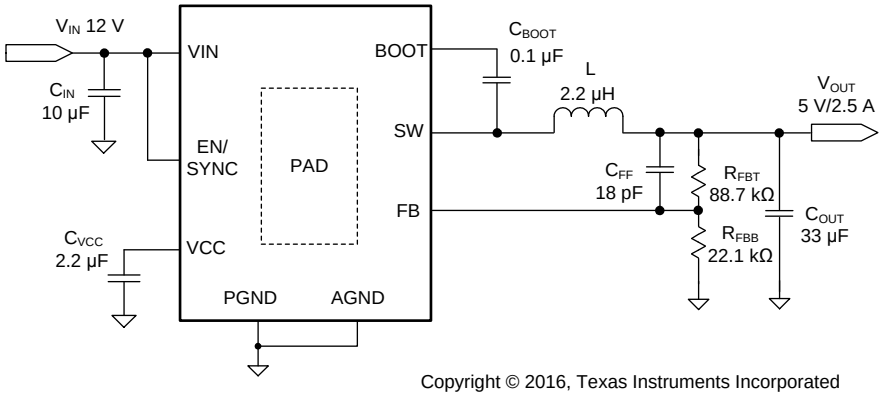

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Figure 22. LMR23625-Q1 Application Circuit

The external components have to fulfill the needs of the application, but also the stability criteria of the device control loop. Table 2 can be used to simplify the output filter component selection.

Table 2. L, C_{OUT} and C_{FF} Typical Values

f_{SW} (kHz)	V_{OUT} (V)	L (µH) (1)	C_{OUT} (µF) (2)	C_{FF} (pF) (3)	R_{FBT} (kΩ) (4)
2100	3.3	2.2	47	33	51
2100	5	2.2	33	18	88.7

(1) Inductance value is calculated based on V_{IN} = 20 V.
(2) All the C_{OUT} values are after derating. Add more when using ceramic capacitors.
(3) High ESR C_{OUT} will give enough phase boost and C_{FF} not needed.
(4) For designs with R_{FBT} other than recommended value, please adjust C_{FF} such that (C_{FF} × R_{FBT}) is unchanged and adjust R_{FBB} such that (R_{FBT} / R_{FBB}) is unchanged.

9.2.1 Design Requirements

Detailed design procedure is described based on a design example. For this design example, use the parameters listed in Table 3 as the input parameters.

Table 3. Design Example Parameters

DESIGN PARAMETER	EXAMPLE VALUE

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Table 3. Design Example Parameters (continued)

Input voltage, V_{IN}	12 V typical, range from 8 V to 28 V
Output voltage, V_{OUT}	5 V
Maximum output current I_{O_MAX}	2.5 A
Transient response 0.2 A to 2.5 A	5%
Output voltage ripple	50 mV
Input voltage ripple	400 mV
Switching frequency f_{SW}	2100 kHz

9.2.2 Detailed Design Procedure

9.2.2.1 Custom Design With WEBENCH® Tools

Click here to create a custom design using the LMR23625-Q1 device with the WEBENCH® Power Designer.

1. Start by entering the input voltage (V_{IN}), output voltage (V_{OUT}), and output current (I_{OUT}) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance
- Run thermal simulations to understand board thermal performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

9.2.2.2 Output Voltage Setpoint

The output voltage of LMR23625-Q1 is externally adjustable using a resistor divider network. The divider network is comprised of top feedback resistor R_{FBT} and bottom feedback resistor R_{FBB}. Equation 10 is used to determine the output voltage:

$$R_{FBT} = \frac{V_{OUT} - V_{REF}}{V_{REF}} \times R_{FBB} \tag{10}$$

Choose the value of R_{FBB} to be 22.1 kΩ. With the desired output voltage set to 5 V and the V_{REF} = 1 V, the R_{FBB} value can then be calculated using Equation 10. The formula yields to a value 88.7 kΩ.

9.2.2.3 Switching Frequency

The default switching frequency of the LMR23625-Q1 is 2100 kHz. For other switching frequencies, the device must be synchronized to an external clock, see *EN/SYNC* for more details.

9.2.2.4 Inductor Selection

The most critical parameters for the inductor are the inductance, saturation current, and the rated current. The inductance is based on the desired peak-to-peak ripple current Δi_L. Since the ripple current increases with the input voltage, the maximum input voltage is always used to calculate the minimum inductance L_{MIN}. Use Equation 12 to calculate the minimum value of the output inductor. K_{IND} is a coefficient that represents the amount of inductor ripple current relative to the maximum output current of the device. A reasonable value of K_{IND} is 20% to 40%. During an instantaneous short or over current operation event, the RMS and peak inductor current can be high. The inductor current rating must be higher than the current limit of the device.

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$$\Delta i_L = \frac{V_{OUT} \times \left(V_{IN_MAX} - V_{OUT}\right)}{V_{IN_MAX} \times L \times f_{SW}} \quad (11)$$

$$L_{MIN} = \frac{V_{IN_MAX} - V_{OUT}}{I_{OUT} \times K_{IND}} \times \frac{V_{OUT}}{V_{IN_MAX} \times f_{SW}} \quad (12)$$

In general, it is preferable to choose lower inductance in switching power supplies, because it usually corresponds to faster transient response, smaller DCR, and reduced size for more compact designs. But too low of an inductance can generate too large of an inductor current ripple such that over current protection at the full load could be falsely triggered. It also generates more conduction loss and inductor core loss. Larger inductor current ripple also implies larger output voltage ripple with same output capacitors. With peak current mode control, it is not recommended to have too small of an inductor current ripple. A larger peak current ripple improves the comparator signal to noise ratio.

For this design example, choose K_{IND} = 0.4, the minimum inductor value is calculated to be 1.9 µH. Choose the nearest standard 2.2-µH ferrite inductor with a capability of 3.5-A RMS current, and 6-A saturation current.

9.2.2.5 Output Capacitor Selection

Choose the output capacitor(s), C_{OUT}, with care since it directly affects the steady-state output-voltage ripple, loop stability, and the voltage over/undershoot during load current transients.

The output ripple is essentially composed of two parts. One is caused by the inductor current ripple going through the ESR of the output capacitors:

$$\Delta V_{OUT_ESR} = \Delta i_L \times ESR = K_{IND} \times I_{OUT} \times ESR \quad (13)$$

The other is caused by the inductor current ripple charging and discharging the output capacitors:

$$\Delta V_{OUT_C} = \frac{\Delta i_L}{\left(8 \times f_{SW} \times C_{OUT}\right)} = \frac{K_{IND} \times I_{OUT}}{\left(8 \times f_{SW} \times C_{OUT}\right)} \quad (14)$$

The two components in the voltage ripple are not in phase, so the actual peak-to-peak ripple is smaller than the sum of two peaks.

Output capacitance is usually limited by transient performance specifications if the system requires tight voltage regulation with presence of large current steps and fast slew rate. When a fast large load increase happens, output capacitors provide the required charge before the inductor current can slew up to the appropriate level. The regulator control loop usually needs four or more clock cycles to respond to the output voltage droop. The output capacitance must be large enough to supply the current difference for four clock cycles to maintain the output voltage within the specified range. Equation 15 shows the minimum output capacitance needed for specified output undershoot. When a sudden large load decrease occurs, the output capacitors absorb energy stored in the inductor. which results in an output voltage overshoot. Equation 16 calculates the minimum capacitance required to keep the voltage overshoot within a specified range.

$$C_{OUT} > \frac{4 \times \left(I_{OH} - I_{OL}\right)}{f_{SW} \times V_{US}} \quad (15)$$

$$C_{OUT} > \frac{I_{OH}^2 - I_{OL}^2}{\left(V_{OUT} + V_{OS}\right)^2 - V_{OUT}^2} \quad (16)$$

where

- K_{IND} = Ripple ratio of the inductor ripple current (Δi_L / I_{OUT})
- I_{OL} = Low level output current during load transient
- I_{OH} = High level output current during load transient
- V_{US} = Target output voltage undershoot
- V_{OS} = Target output voltage overshoot

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For this design example, the target output ripple is 50 mV. Presuppose $\Delta V_{OUT_ESR} = \Delta V_{OUT_C}$ = 50 mV and chose K_{IND} = 0.4. Equation 13 yields ESR no larger than 50 mΩ and Equation 14 yields C_{OUT} no smaller than 1.2 µF. For the target over/undershoot range of this design, $V_{US} = V_{OS}$ = 5% × V_{OUT} = 250 mV. The C_{OUT} can be calculated to be no smaller than 17.5 µF and 5.3 µF by Equation 15 and Equation 16 respectively. Consider of derating, one 33-µF, 16-V ceramic capacitor with 5-mΩ ESR is used.

9.2.2.6 Feed-Forward Capacitor

The LMR23625-Q1 is internally compensated. Depending on the V_{OUT} and frequency f_{SW}, if the output capacitor C_{OUT} is dominated by low ESR (ceramic types) capacitors, it could result in low phase margin. To improve the phase boost an external feed-forward capacitor C_{FF} can be added in parallel with R_{FBT}. Choose C_{FF} is so that phase margin is boosted at the crossover frequency without C_{FF}. A simple estimation for the crossover frequency (f_X) without C_{FF} is shown in Equation 17, assuming C_{OUT} has very small ESR, and C_{OUT} value is after derating.

$$f_X = \frac{8.32}{V_{OUT} \times C_{OUT}} \tag{17}$$

Equation 18 for C_{FF} was tested:

$$C_{FF} = \frac{1}{4\pi \times f_X \times R_{FBT}} \tag{18}$$

For designs with higher ESR, C_{FF} is not needed when C_{OUT} has very high ESR; reduce C_{FF} calculated from Equation 18 with medium ESR. Table 2 can be used as a quick starting point.

For the application in this design example, a 18-pF, 50-V COG capacitor is selected.

9.2.2.7 Input Capacitor Selection

The LMR23625-Q1 device requires high-frequency input decoupling capacitor(s) and a bulk input capacitor, depending on the application. The typical recommended value for the high frequency decoupling capacitor is 4.7 µF to 10 µF. TI recommends a high-quality ceramic capacitor type X5R or X7R with sufficiency voltage rating is recommended. To compensate the derating of ceramic capacitors, a voltage rating of twice the maximum input voltage. Additionally, some bulk capacitance can be required, especially if the LMR23625-Q1 circuit is not located within approximately 5 cm from the input voltage source. This capacitor is used to provide damping to the voltage spike due to the lead inductance of the cable or the trace. For this design, two 4.7-µF, 50-V, X7R ceramic capacitors are used. For high-frequency filtering place a 0.1-µF capacitor as close as possible to the device pins.

9.2.2.8 Bootstrap Capacitor Selection

Every LMR23625-Q1 design requires a bootstrap capacitor (C_{BOOT}). The recommended capacitor is 0.1 µF and rated 16 V or higher. The bootstrap capacitor is located between the SW pin and the BOOT pin. The bootstrap capacitor must be a high-quality ceramic type with an X7R or X5R grade dielectric for temperature stability.

9.2.2.9 VCC Capacitor Selection

The VCC pin is the output of an internal LDO for LMR23625-Q1. To insure stability of the device, place a minimum of 2.2-µF, 16-V, X7R capacitor from VCC pin to ground.

9.2.2.10 Undervoltage Lockout Setpoint

The system UVLO is adjusted using the external voltage divider network of R_{ENT} and R_{ENB}. The UVLO has two thresholds, one for power up when the input voltage is rising and one for power down or brownouts when the input voltage is falling. Use Equation 19 to determine the V_{IN} UVLO level.

$$V_{IN_RISING} = V_{ENH} \times \frac{R_{ENT} + R_{ENB}}{R_{ENB}} \tag{19}$$

The EN rising threshold (V_{ENH}) for LMR23625-Q1 is set to be 1.55 V (typical). Choose the value of R_{ENB} to be 287 kΩ to minimize input current from the supply. If the desired V_{IN} UVLO level is at 6 V, the value of R_{ENT} can be calculated using Equation 20:

$$R_{ENT} = \left(\frac{V_{IN_RISING}}{V_{ENH}} - 1 \right) \times R_{ENB} \tag{20}$$

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Equation 20 yields a value of 820 kΩ. The resulting falling UVLO threshold, equals 4.4 V, can be calculated by Equation 21, where EN hysteresis (V_{EN_HYS}) is 0.4 V (typical).

$$V_{IN_FALLING} = \left(V_{ENH} - V_{EN_HYS}\right) \times \frac{R_{ENT} + R_{ENB}}{R_{ENB}} \quad (21)$$

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9.2.3 Application Curves

Unless otherwise specified the following conditions apply: V_{IN} = 12 V, f_{SW} = 2100 kHz, L = 2.2 µH, C_{OUT} = 47 µF, T_A = 25°C.

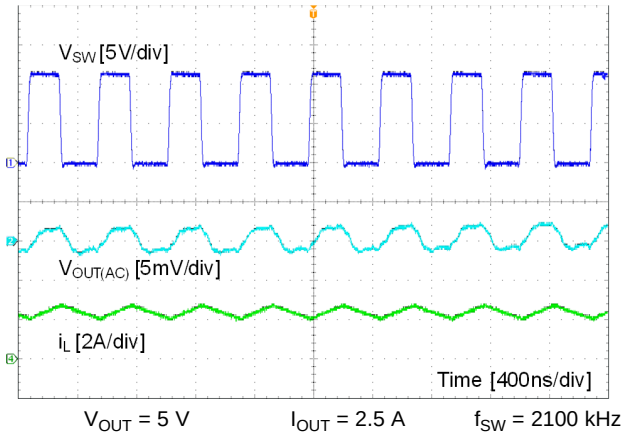

Figure 23. CCM Mode

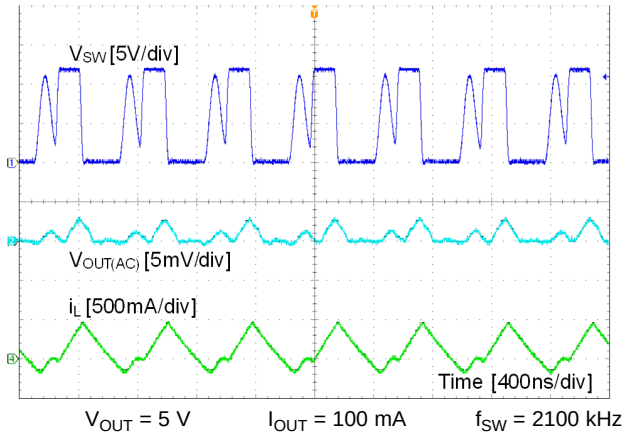

Figure 24. DCM Mode

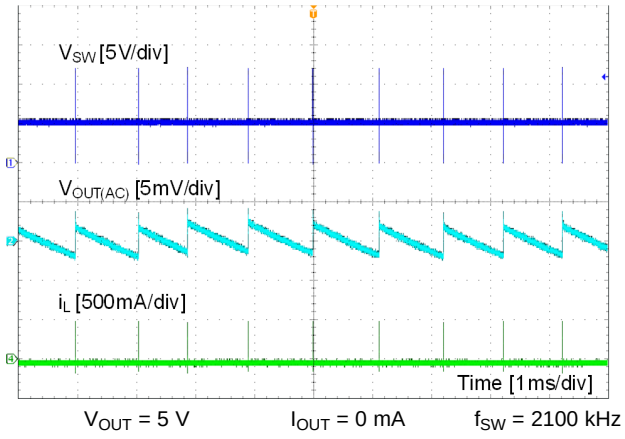

Figure 25. PFM Mode

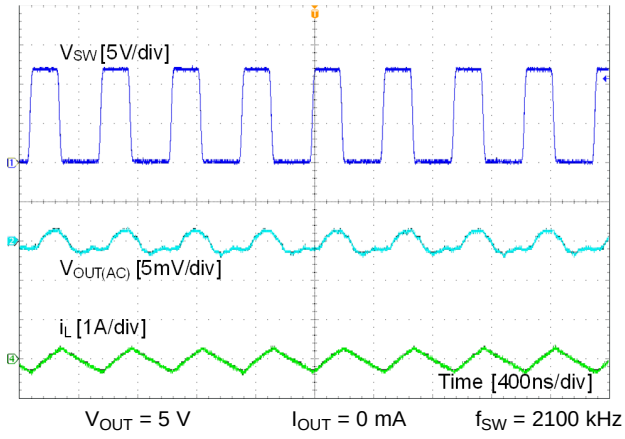

Figure 26. FPWM Mode

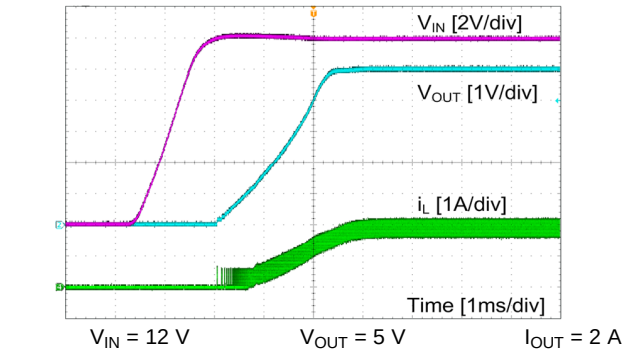

Figure 27. Start-Up by V_{IN}

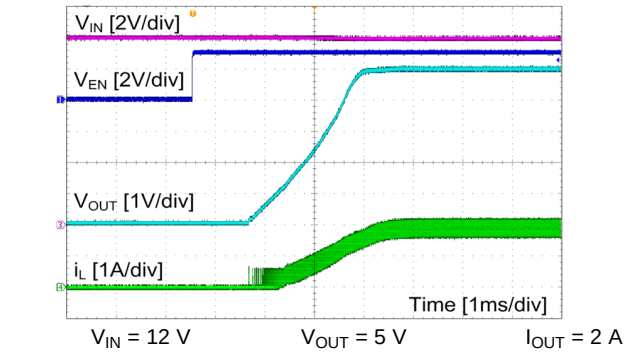

Figure 28. Start-Up by EN

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Unless otherwise specified the following conditions apply: V_{IN} = 12 V, f_{SW} = 2100 kHz, L = 2.2 µH, C_{OUT} = 47 µF, T_A = 25°C.

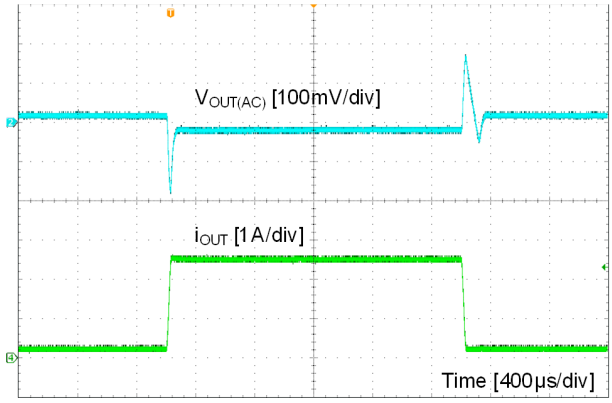

Figure 29. Load Transient

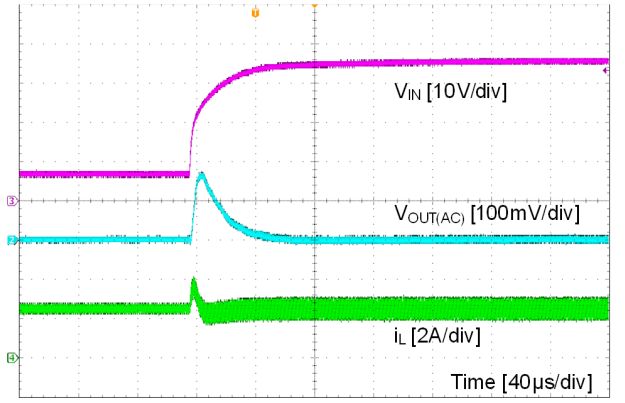

Figure 30. Line Transient

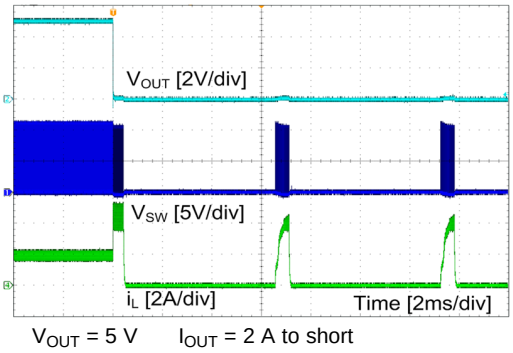

Figure 31. Short Protection

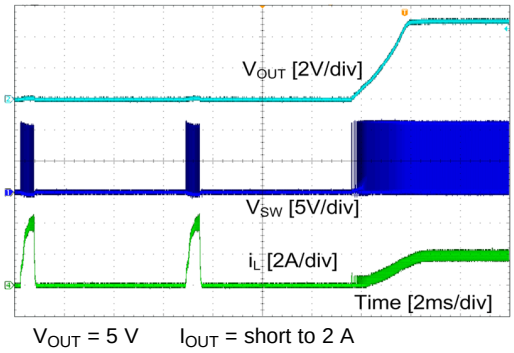

Figure 32. Short Recovery

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10 Power Supply Recommendations

The LMR23625-Q1 is designed to operate from an input voltage supply range between 4 V and 36 V. This input supply must be able to withstand the maximum input current and maintain a stable voltage. The resistance of the input supply rail must be low enough that an input current transient does not cause a high enough drop at the LMR23625-Q1 supply voltage that can cause a false UVLO fault triggering and system reset. If the input supply is located more than a few inches from the LMR23625-Q1, additional bulk capacitance may be required in addition to the ceramic input capacitors. The amount of bulk capacitance is not critical, but a 47-µF or 100-µF electrolytic capacitor is a typical choice.

11 Layout

11.1 Layout Guidelines

Layout is a critical portion of good power supply design. The following guidelines will help users design a PCB with the best power conversion performance, thermal performance, and minimized generation of unwanted EMI.

1. The input bypass capacitor C_{IN} must be placed as close as possible to the VIN and PGND pins. Grounding for both the input and output capacitors must consist of localized top side planes that connect to the PGND pin and PAD.
2. Place bypass capacitors for V_{CC} close to the VCC pin and ground the bypass capacitor to device ground.
3. Minimize trace length to the FB pin net. Both feedback resistors, R_{FBT} and R_{FBB} must be located close to the FB pin. Place C_{FF} directly in parallel with R_{FBT}. If V_{OUT} accuracy at the load is important, make sure V_{OUT} sense is made at the load. Route V_{OUT} sense path away from noisy nodes and preferably through a layer on the other side of a shielded layer.
4. Use ground plane in one of the middle layers as noise shielding and heat dissipation path.
5. Have a single point ground connection to the plane. Route he ground connections for the feedback and enable components to the ground plane. This prevents any switched or load currents from flowing in the analog ground traces. If not properly handled, poor grounding can result in degraded load regulation or erratic output voltage ripple behavior.
6. Make V_{IN}, V_{OUT} and ground bus connections as wide as possible. This reduces any voltage drops on the input or output paths of the converter and maximizes efficiency.
7. Provide adequate device heat sinking. Use an array of heat-sinking vias to connect the exposed pad to the ground plane on the bottom PCB layer. If the PCB has multiple copper layers, these thermal vias can also be connected to inner layer heat-spreading ground planes. Ensure enough copper area is used for heat-sinking to keep the junction temperature below 125°C.

11.1.1 Compact Layout for EMI Reduction

Radiated EMI is generated by the high di/dt components in pulsing currents in switching converters. The larger area covered by the path of a pulsing current, the more EMI is generated. High-frequency ceramic bypass capacitors at the input side provide primary path for the high di/dt components of the pulsing current. Placing ceramic bypass capacitor(s) as close as possible to the VIN and PGND pins is the key to EMI reduction.

The SW pin connecting to the inductor must be as short as possible, just wide enough to carry the load current without excessive heating. Short, thick traces or copper pours (shapes) must be used for high-current conduction path to minimize parasitic resistance. Place the output capacitors close to the V_{OUT} end of the inductor and closely grounded to PGND pin and exposed PAD.

Place the bypass capacitors on VCC as close as possible to the pin and closely grounded to PGND and the exposed PAD.

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Layout Guidelines (continued)

11.1.2 Ground Plane and Thermal Considerations

TI recommends using one of the middle layers as a solid ground plane. Ground plane provides shielding for sensitive circuits and traces. It also provides a quiet reference potential for the control circuitry. The AGND and PGND pins must be connected to the ground plane using vias right next to the bypass capacitors. PGND pin is connected to the source of the internal LS switch. They must be connected directly to the grounds of the input and output capacitors. The PGND net contains noise at switching frequency and may bounce due to load variations. Constrain the PGND trace, as well as VIN and SW traces, to one side of the ground plane. The other side of the ground plane contains much less noise and must be used for sensitive routes.

TI recommends providing adequate device heat sinking by utilizing the PAD of the device as the primary thermal path. Use a minimum 4 by 2 array of 12 mil thermal vias to connect the PAD to the system ground plane heat sink. The vias must be evenly distributed under the PAD. Use as much copper as possible, for system ground plane, on the top and bottom layers for the best heat dissipation. Use a four-layer board with the copper thickness for the four layers, starting from the top of 2 oz / 1 oz / 1 oz / 2 oz. Four-layer boards with enough copper thickness provides low current-conduction impedance, proper shielding and lower thermal resistance.

The thermal characteristics of the LMR23625-Q1 are specified using the parameter $R_{\theta JA}$, which characterize the junction temperature of silicon to the ambient temperature in a specific system. Although the value of $R_{\theta JA}$ is dependent on many variables, it still can be used to approximate the operating junction temperature of the device. To obtain an estimate of the device junction temperature, one may use Equation 22:

$$T_J = P_D \times R_{\theta JA} + T_A$$

where

- T_J = junction temperature in °C
- $P_D = V_{IN} \times I_{IN} \times (1 - \text{efficiency}) - 1.1 \times I_{OUT}^2 \times \text{DCR}$ in Watt
- DCR = Inductor DC parasitic resistance in Ω
- $r_{\theta JA}$ = Junction-to-ambient thermal resistance of the device in °C/W
- T_A = ambient temperature in °C (22)

The maximum operating junction temperature of the LMR23625-Q1 is 125°C. $R_{\theta JA}$ is highly related to PCB size and layout, as well as environmental factors such as heat sinking and air flow.

11.1.3 Feedback Resistors

To reduce noise sensitivity of the output voltage feedback path, it is important to place the resistor divider and C_{FF} close to the FB pin, rather than close to the load. The FB pin is the input to the EA, so it is a high impedance node and very sensitive to noise. Placing the resistor divider and C_{FF} closer to the FB pin reduces the trace length of FB signal and reduces noise coupling. The output node is a low impedance node, so the trace from V_{OUT} to the resistor divider can be long if short path is not available.

If voltage accuracy at the load is important, make sure voltage sense is made at the load. Doing so corrects for voltage drops along the traces and provide the best output accuracy. Route the voltage sense trace from the load to the feedback resistor divider away from the SW node path and the inductor to avoid contaminating the feedback signal with switch noise, while also minimizing the trace length. This is most important when high-value resistors are used to set the output voltage. TI recommends routing the voltage sense trace and place the resistor divider on a different layer than the inductor and SW node path, such that there is a ground plane in between the feedback trace and inductor/SW node polygon. This provides further shielding for the voltage feedback path from EMI noises.

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11.2 Layout Examples

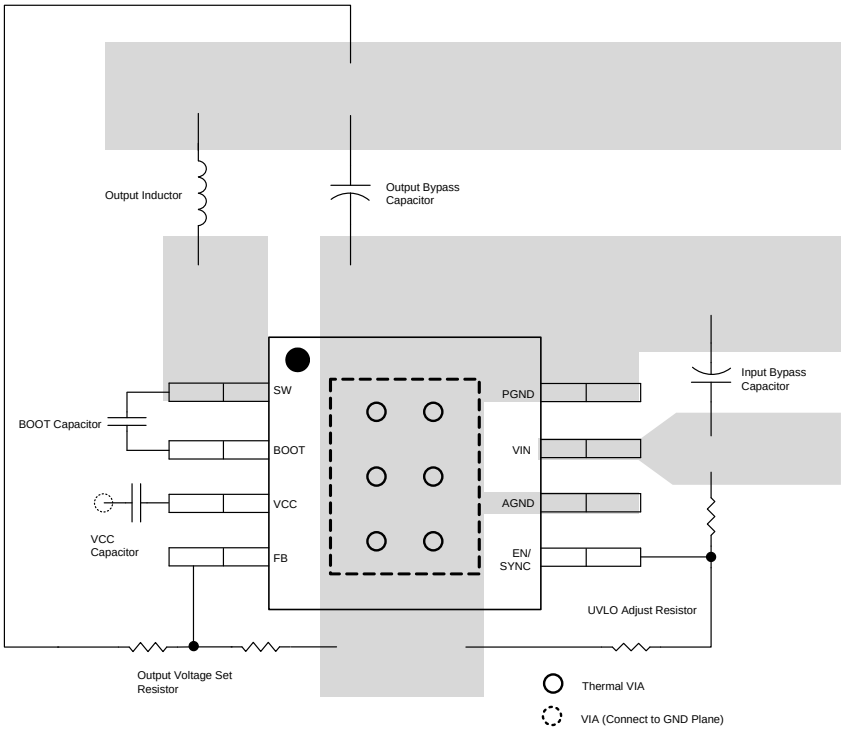

Figure 33. SOIC Layout

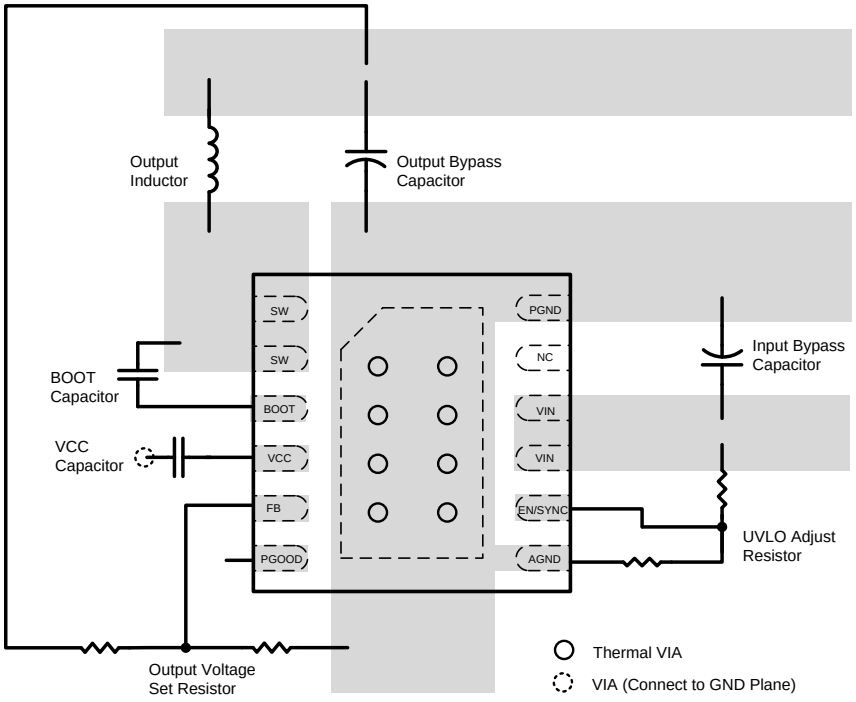

Figure 34. WSON Layout

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12 デバイスおよびドキュメントのサポート

12.1 デバイス・サポート

12.1.1 開発サポート

12.1.1.1 WEBENCH®ツールによるカスタム設計

ここをクリックすると、WEBENCH® Power Designerにより、LMR23625-Q1デバイスを使用するカスタム設計を作成できます。

1. 最初に、入力電圧(V_{IN})、出力電圧(V_{OUT})、出力電流(I_{OUT})の要件を入力します。
2. オプティマイザのダイヤルを使用して、効率、占有面積、コストなどの主要なパラメータについて設計を最適化します。
3. 生成された設計を、テキサス・インスツルメンツが提供する他のソリューションと比較します。

WEBENCH Power Designerでは、カスタマイズされた回路図と部品リストを、リアルタイムの価格と部品の在庫情報と併せて参照できます。

ほとんどの場合、次の操作を実行可能です。

- 電気的なシミュレーションを実行し、重要な波形と回路の性能を確認する。
- 熱シミュレーションを実行し、基板の熱特性を把握する。
- カスタマイズされた回路図やレイアウトを、一般的なCADフォーマットでエクスポートする。
- 設計のレポートをPDFで印刷し、同僚と設計を共有する。

WEBENCHツールの詳細は、www.ti.com/WEBENCHでご覧になれます。

12.2 ドキュメントの更新通知を受け取る方法

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12.3 コミュニティ・リソース

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

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設計サポート ***TIの設計サポート*** **役に立つE2Eフォーラムや、設計サポート・ツールをすばやく見つけることができます。技術サポート用の連絡先情報も参照できます。**

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12.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

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13 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。この情報は、そのデバイスについて利用可能な最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LMR23625CFPQDRRRQ1	Active	Production	WSON (DRR) | 12	3000 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	362PQ
LMR23625CFPQDRRRQ1.A	Active	Production	WSON (DRR) | 12	3000 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	362PQ
LMR23625CFPQDRRRQ1.B	Active	Production	WSON (DRR) | 12	3000 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	362PQ
LMR23625CFPQDRRTQ1	Active	Production	WSON (DRR) | 12	250 | SMALL T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	362PQ
LMR23625CFPQDRRTQ1.A	Active	Production	WSON (DRR) | 12	250 | SMALL T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	362PQ
LMR23625CFPQDRRTQ1.B	Active	Production	WSON (DRR) | 12	250 | SMALL T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	362PQ
LMR23625CFQDDAQ1	Active	Production	SO PowerPAD (DDA) | 8	75 | TUBE	Yes	NIPDAU | NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	F25CFQ
LMR23625CFQDDAQ1.A	Active	Production	SO PowerPAD (DDA) | 8	75 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	F25CFQ
LMR23625CFQDDAQ1.B	Active	Production	SO PowerPAD (DDA) | 8	75 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	F25CFQ
LMR23625CFQDDARQ1	Active	Production	SO PowerPAD (DDA) | 8	2500 | LARGE T&R	Yes	NIPDAU | NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	F25CFQ
LMR23625CFQDDARQ1.A	Active	Production	SO PowerPAD (DDA) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	F25CFQ
LMR23625CFQDDARQ1.B	Active	Production	SO PowerPAD (DDA) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	F25CFQ
LMR23625CQDDAQ1	Active	Production	SO PowerPAD (DDA) | 8	75 | TUBE	Yes	NIPDAU | NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	F25CQ
LMR23625CQDDAQ1.A	Active	Production	SO PowerPAD (DDA) | 8	75 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	F25CQ
LMR23625CQDDAQ1.B	Active	Production	SO PowerPAD (DDA) | 8	75 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	F25CQ
LMR23625CQDDARQ1	Active	Production	SO PowerPAD (DDA) | 8	2500 | LARGE T&R	Yes	NIPDAU | NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	F25CQ
LMR23625CQDDARQ1.A	Active	Production	SO PowerPAD (DDA) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	F25CQ
LMR23625CQDDARQ1.B	Active	Production	SO PowerPAD (DDA) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	F25CQ

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF LMR23625-Q1 :

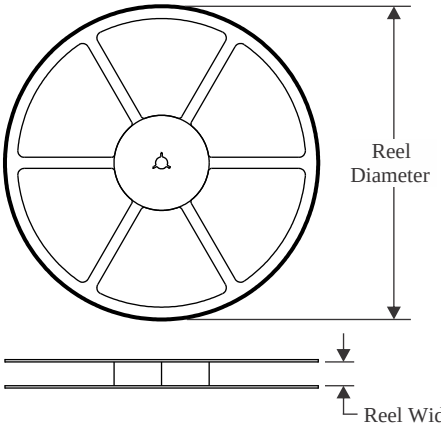
- Catalog : LMR23625

NOTE: Qualified Version Definitions:

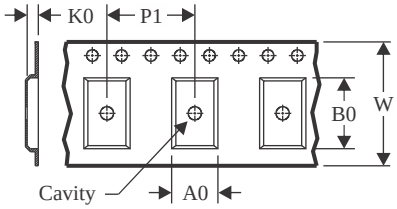
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

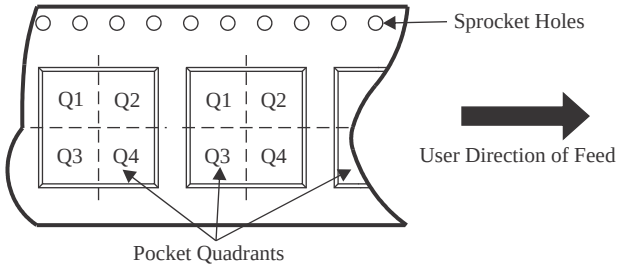


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

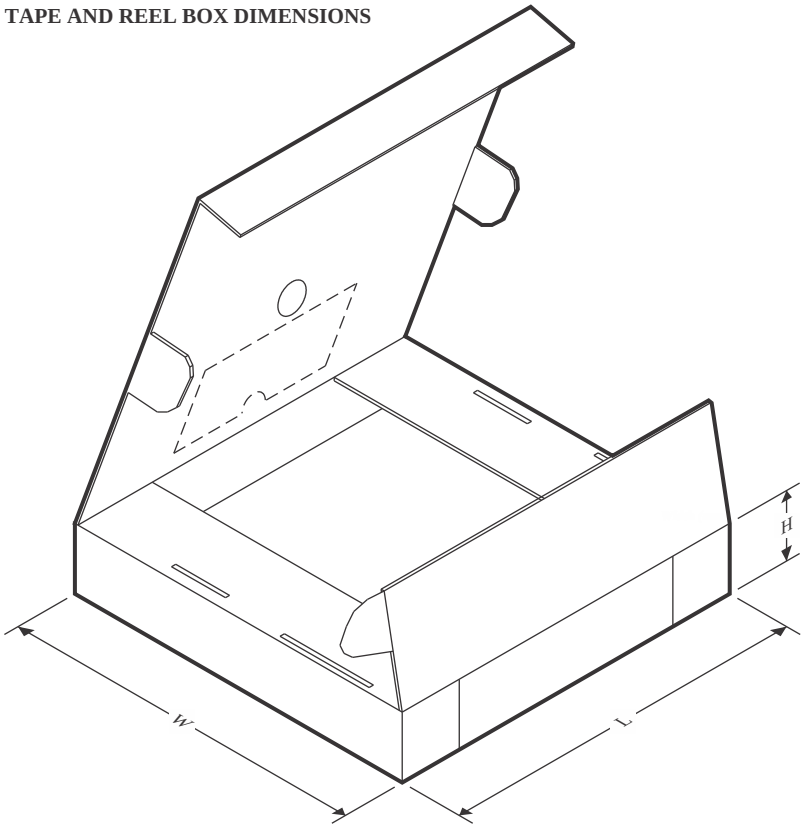
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMR23625CFPQDRRRQ1	WSON	DRR	12	3000	330.0	12.4	3.3	3.3	1.0	8.0	12.0	Q2
LMR23625CFPQDRRTQ1	WSON	DRR	12	250	180.0	12.4	3.3	3.3	1.0	8.0	12.0	Q2
LMR23625CFQDDARQ1	SO PowerPAD	DDA	8	2500	330.0	12.8	6.4	5.2	2.1	8.0	12.0	Q1
LMR23625CQDDARQ1	SO PowerPAD	DDA	8	2500	330.0	12.8	6.4	5.2	2.1	8.0	12.0	Q1

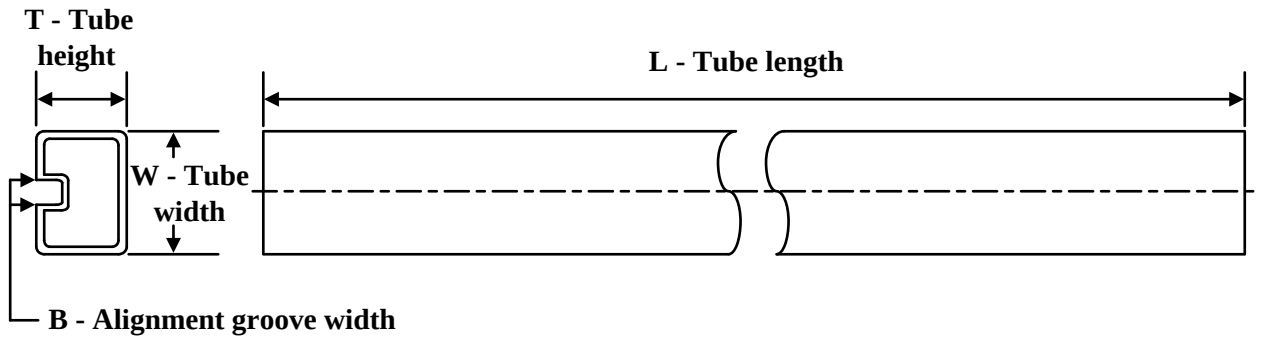
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMR23625CFPQDRRRQ1	WSON	DRR	12	3000	367.0	367.0	38.0
LMR23625CFPQDRRTQ1	WSON	DRR	12	250	213.0	191.0	35.0
LMR23625CFQDDARQ1	SO PowerPAD	DDA	8	2500	366.0	364.0	50.0
LMR23625CQDDARQ1	SO PowerPAD	DDA	8	2500	366.0	364.0	50.0

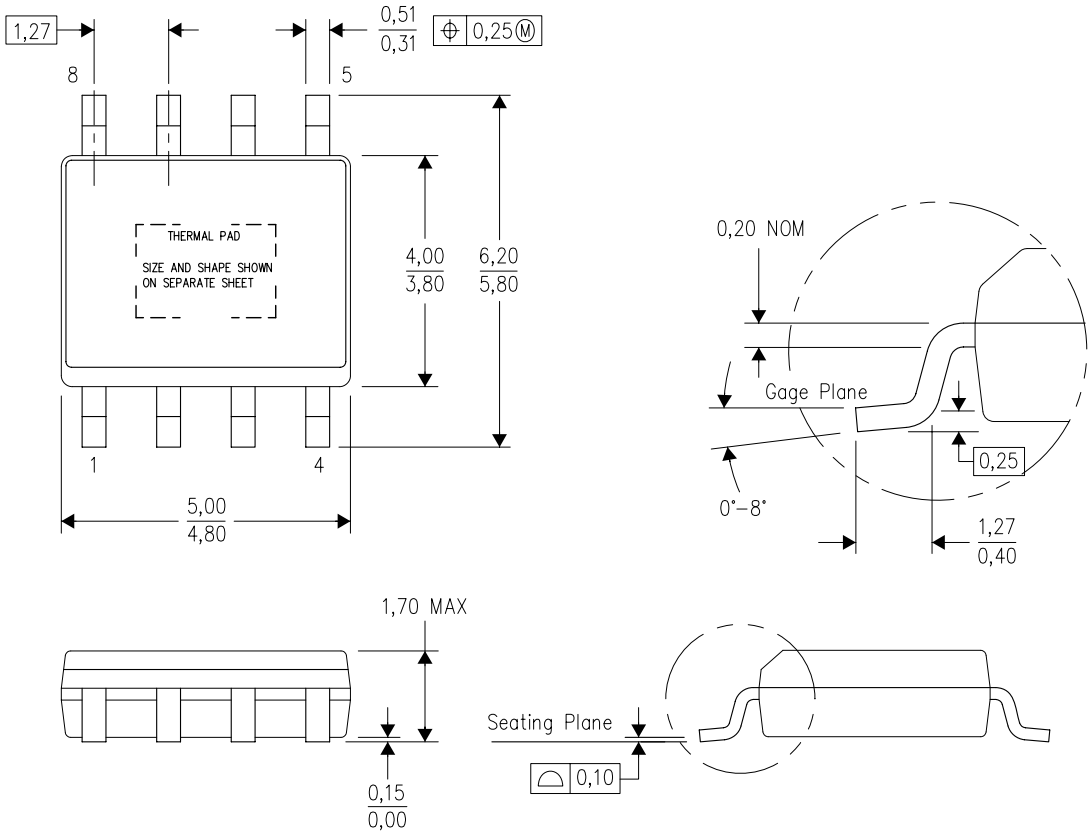
TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
LMR23625CFQDDAQ1	DDA	HSOIC	8	75	517	7.87	635	4.25
LMR23625CFQDDAQ1	DDA	HSOIC	8	75	507	8	3940	4.32
LMR23625CFQDDAQ1.A	DDA	HSOIC	8	75	517	7.87	635	4.25
LMR23625CFQDDAQ1.A	DDA	HSOIC	8	75	507	8	3940	4.32
LMR23625CFQDDAQ1.B	DDA	HSOIC	8	75	507	8	3940	4.32
LMR23625CFQDDAQ1.B	DDA	HSOIC	8	75	517	7.87	635	4.25
LMR23625CQDDAQ1	DDA	HSOIC	8	75	507	8	3940	4.32
LMR23625CQDDAQ1	DDA	HSOIC	8	75	517	7.87	635	4.25
LMR23625CQDDAQ1.A	DDA	HSOIC	8	75	517	7.87	635	4.25
LMR23625CQDDAQ1.A	DDA	HSOIC	8	75	507	8	3940	4.32
LMR23625CQDDAQ1.B	DDA	HSOIC	8	75	507	8	3940	4.32
LMR23625CQDDAQ1.B	DDA	HSOIC	8	75	517	7.87	635	4.25

DDA (R–PDSO–G8) PowerPAD™ PLASTIC SMALL–OUTLINE



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5–1994.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. This package complies to JEDEC MS–012 variation BA

PowerPAD is a trademark of Texas Instruments.

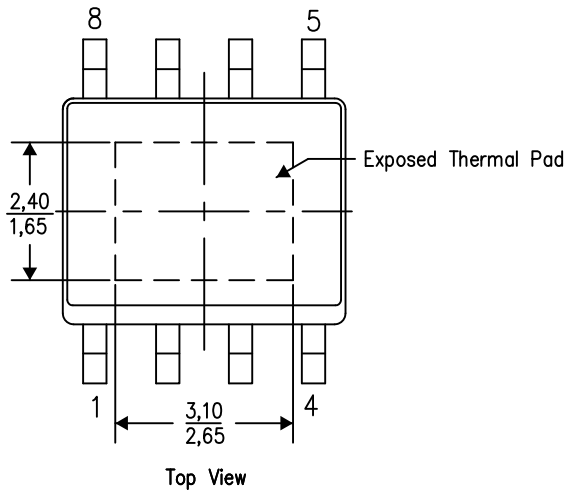
DDA (R–PDSO–G8) PowerPAD™ PLASTIC SMALL OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



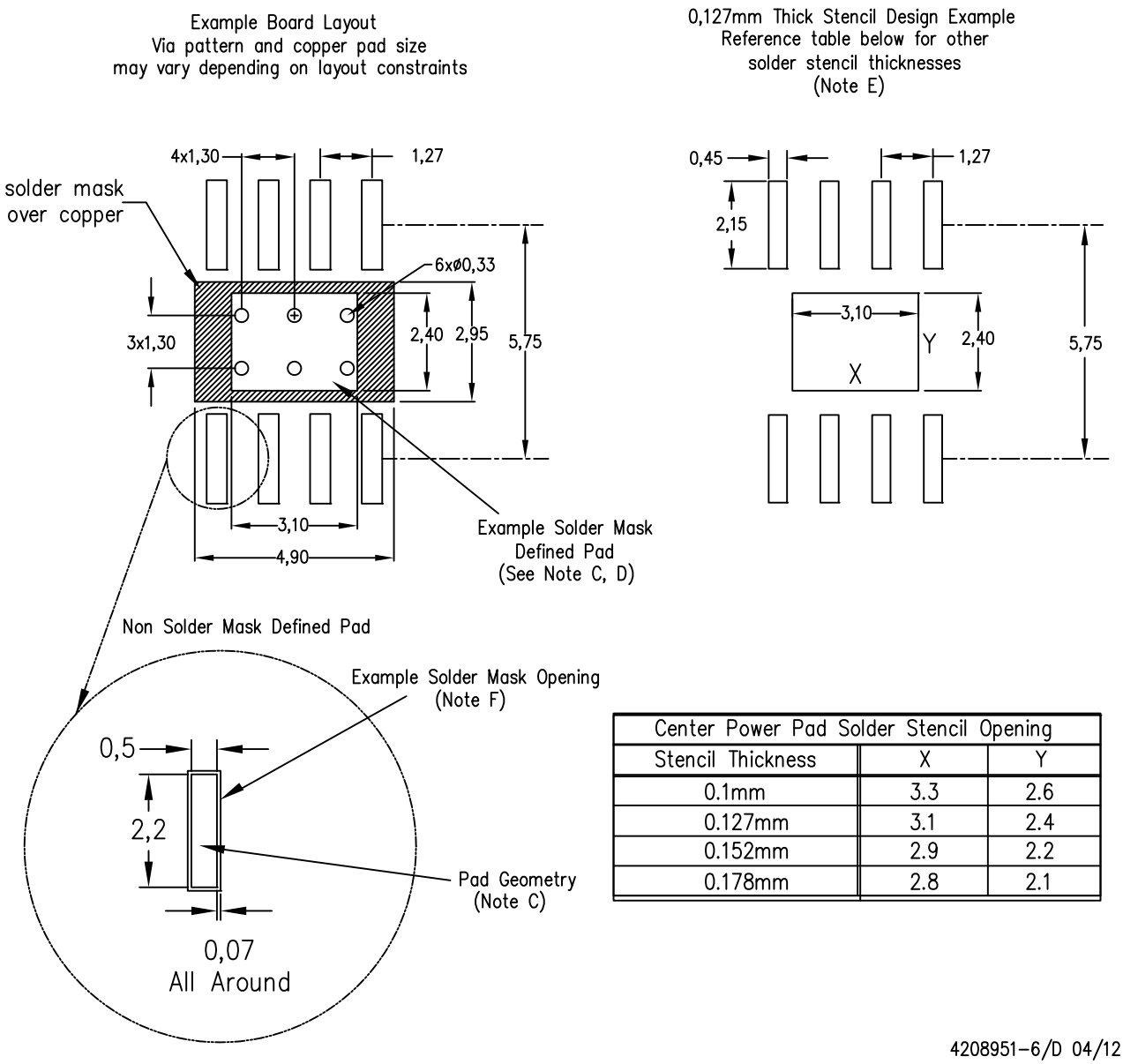
Exposed Thermal Pad Dimensions

4206322–6/L 05/12

NOTE: A. All linear dimensions are in millimeters

PowerPAD is a trademark of Texas Instruments

DDA (R–PDSO–G8) PowerPAD™ PLASTIC SMALL OUTLINE



Center Power Pad Solder Stencil Opening		
Stencil Thickness	X	Y
0.1mm	3.3	2.6
0.127mm	3.1	2.4
0.152mm	2.9	2.2
0.178mm	2.8	2.1

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.
F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

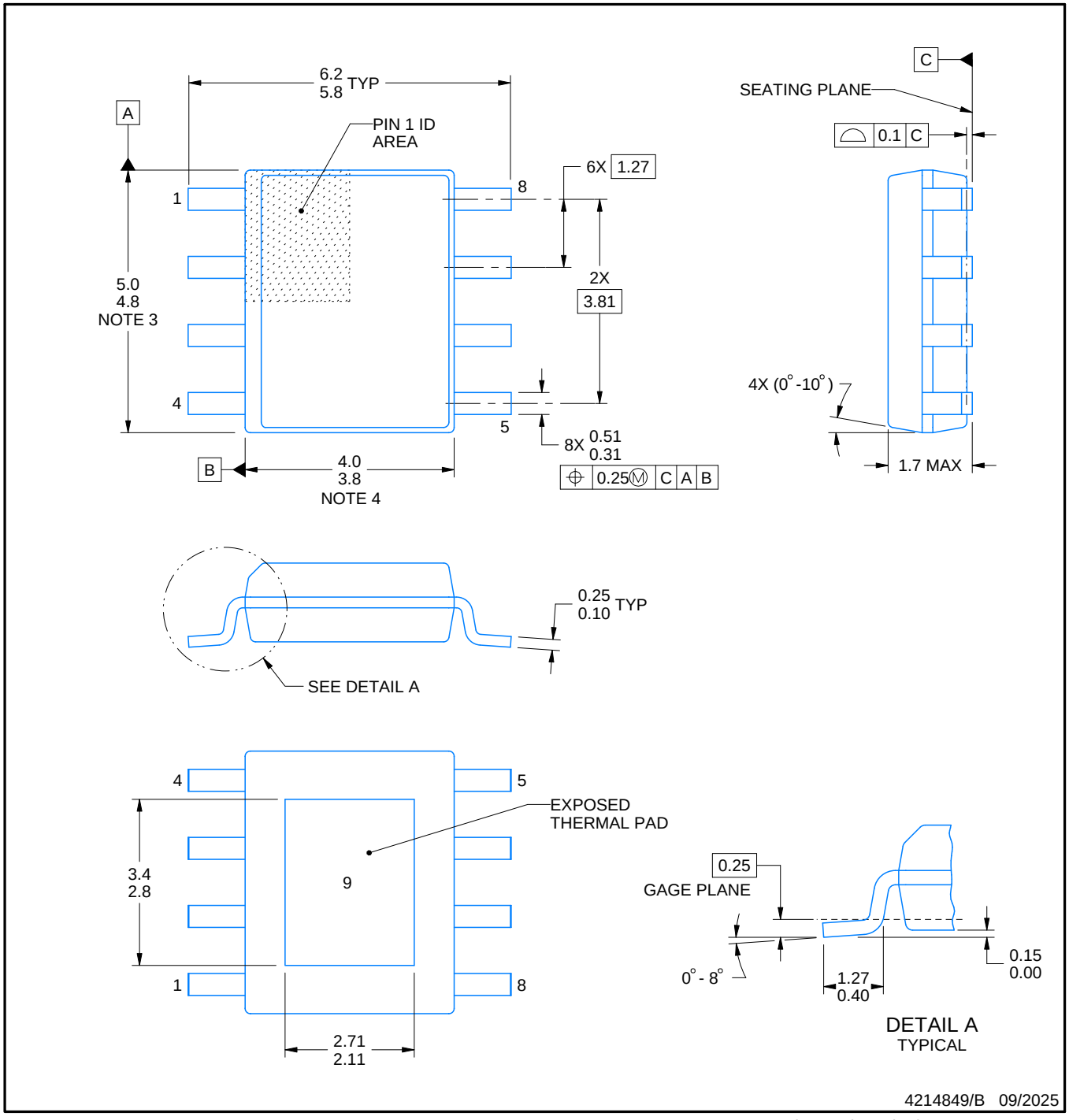
PowerPAD is a trademark of Texas Instruments.

PACKAGE OUTLINE

DDA0008B

PowerPAD™ SOIC - 1.7 mm max height

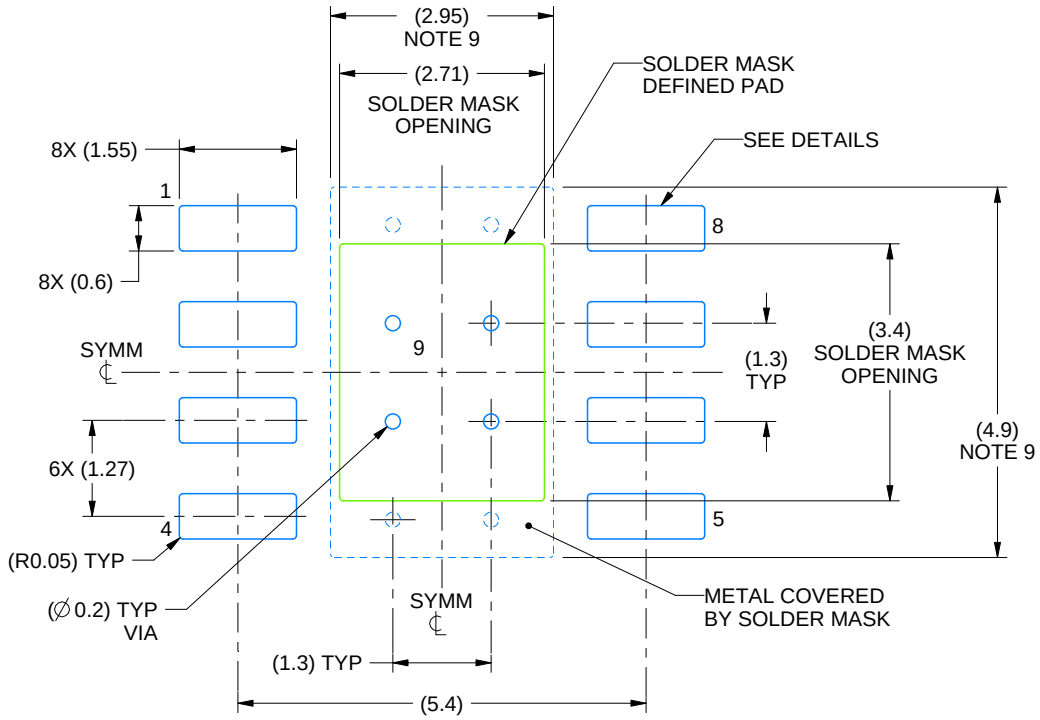
PLASTIC SMALL OUTLINE



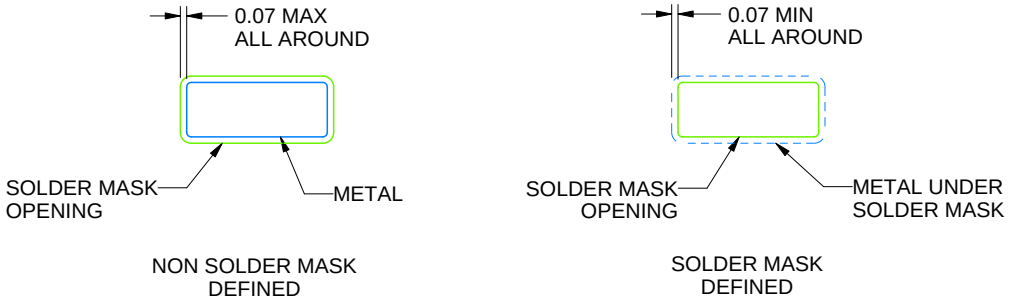
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MS-012.



LAND PATTERN EXAMPLE
SCALE:10X



SOLDER MASK DETAILS
PADS 1-8

4214849/B 09/2025

NOTES: (continued)

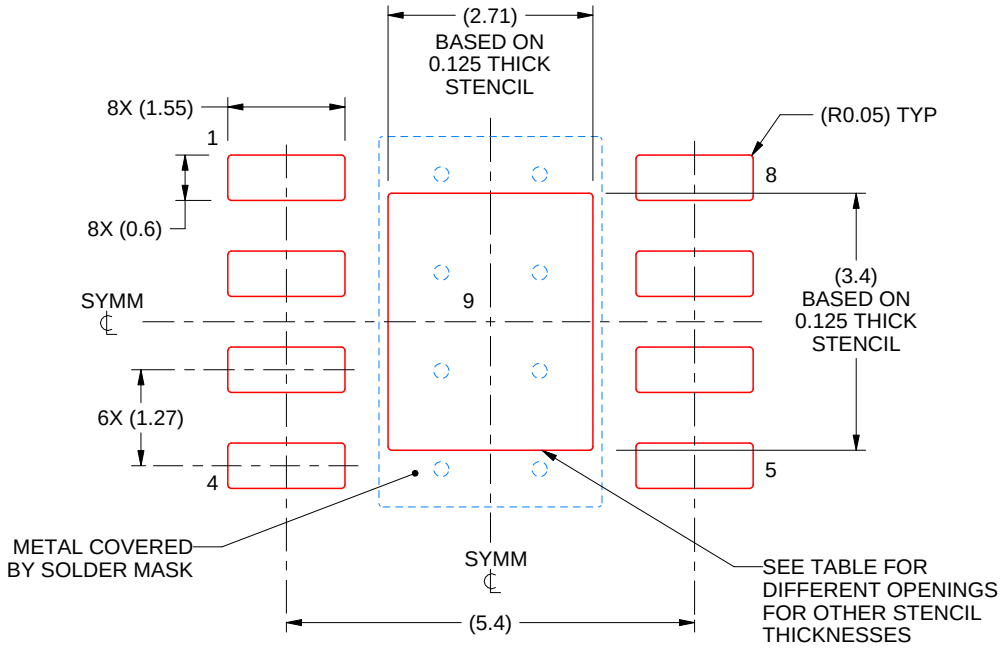
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.
10. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

DDA0008B

PowerPAD™ SOIC - 1.7 mm max height

PLASTIC SMALL OUTLINE



SOLDER PASTE EXAMPLE
EXPOSED PAD
100% PRINTED SOLDER COVERAGE BY AREA
SCALE:10X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	3.03 X 3.80
0.125	2.71 X 3.40 (SHOWN)
0.150	2.47 X 3.10
0.175	2.29 X 2.87

4214849/B 09/2025

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

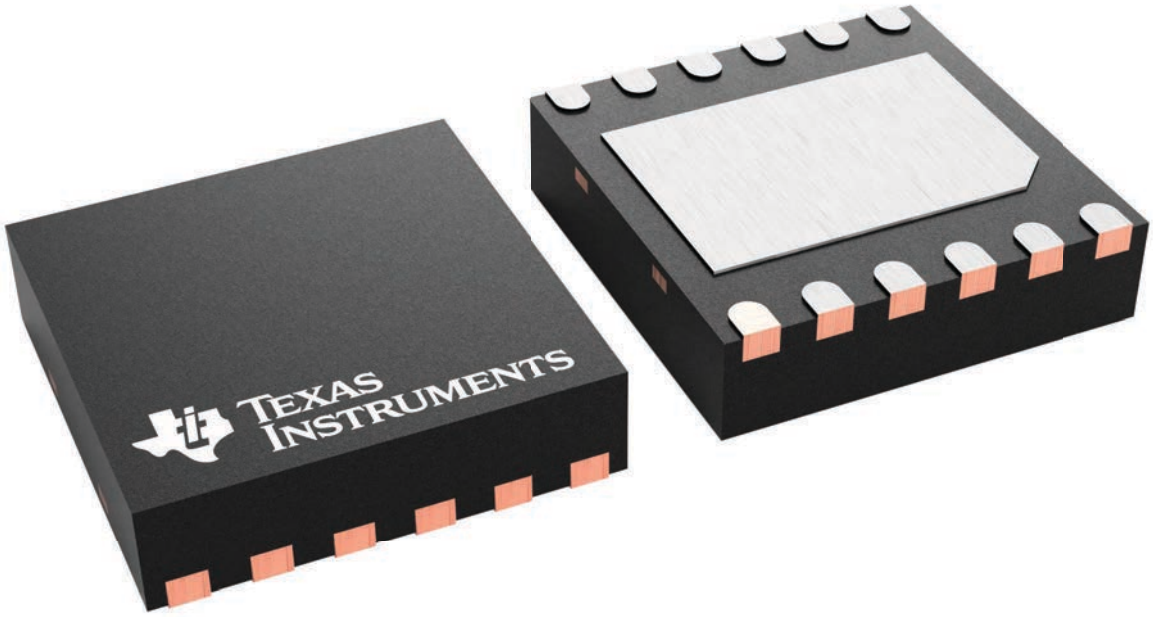
DRR 12

WSON - 0.8 mm max height

3 x 3, 0.5 mm pitch

PLASTIC SMALL OUTLINE - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4223490/B

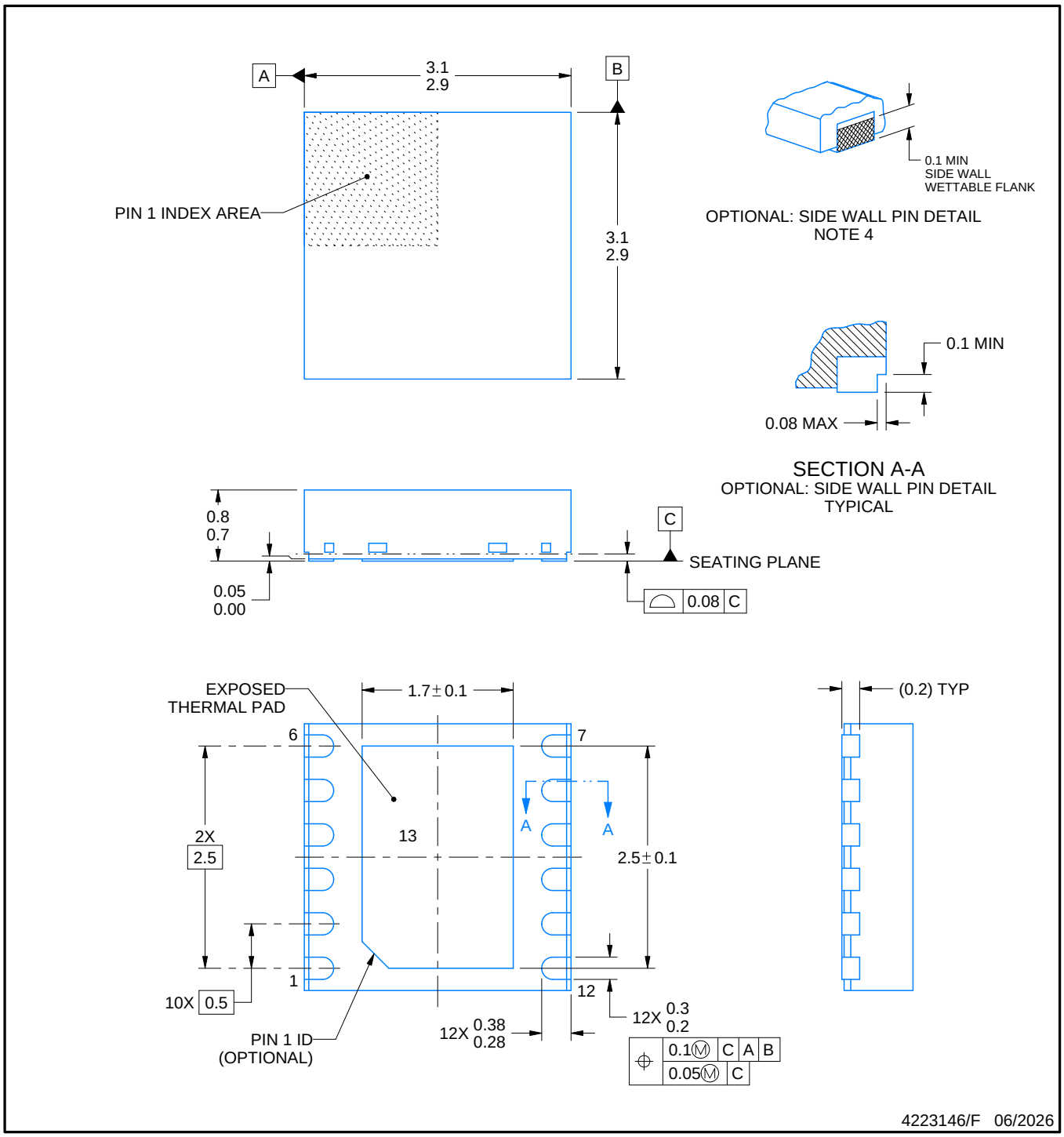
DRR0012D



PACKAGE OUTLINE

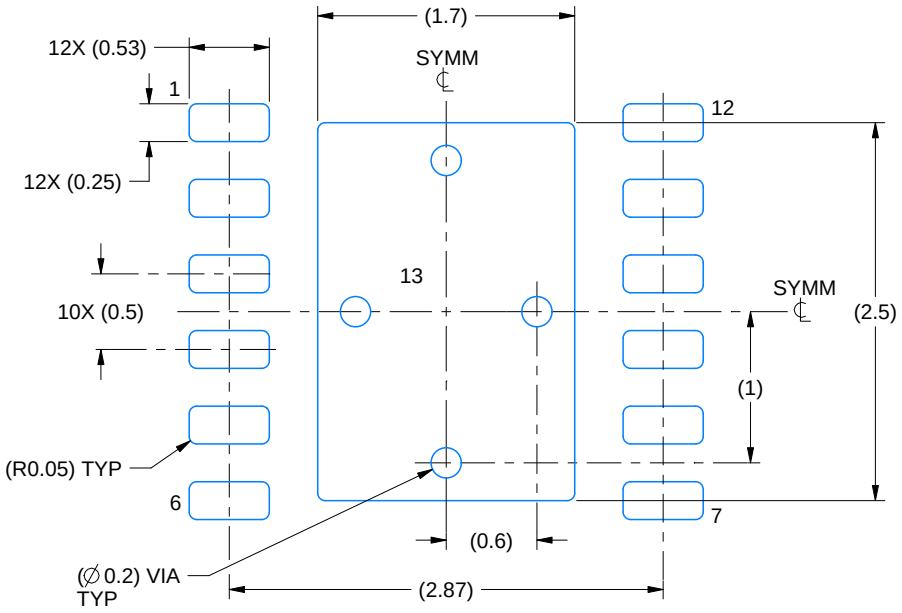
WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

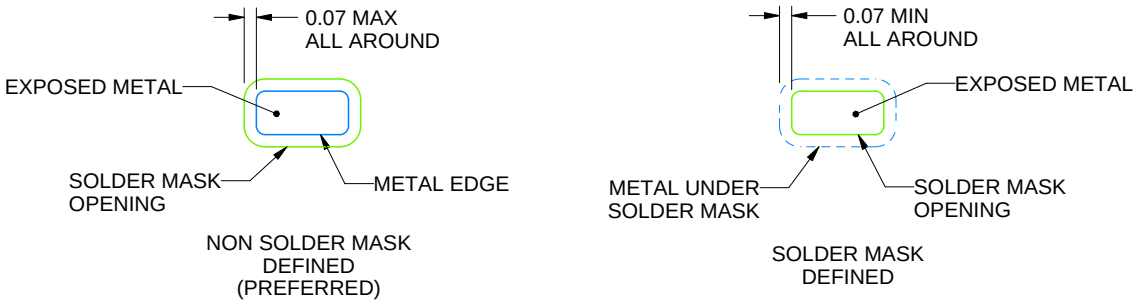


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.
4. Minimum 0.1 mm solder wetting on pin side wall. Available for wettable flank version only.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X



SOLDER MASK DETAILS

4223146/F 06/2026

NOTES: (continued)

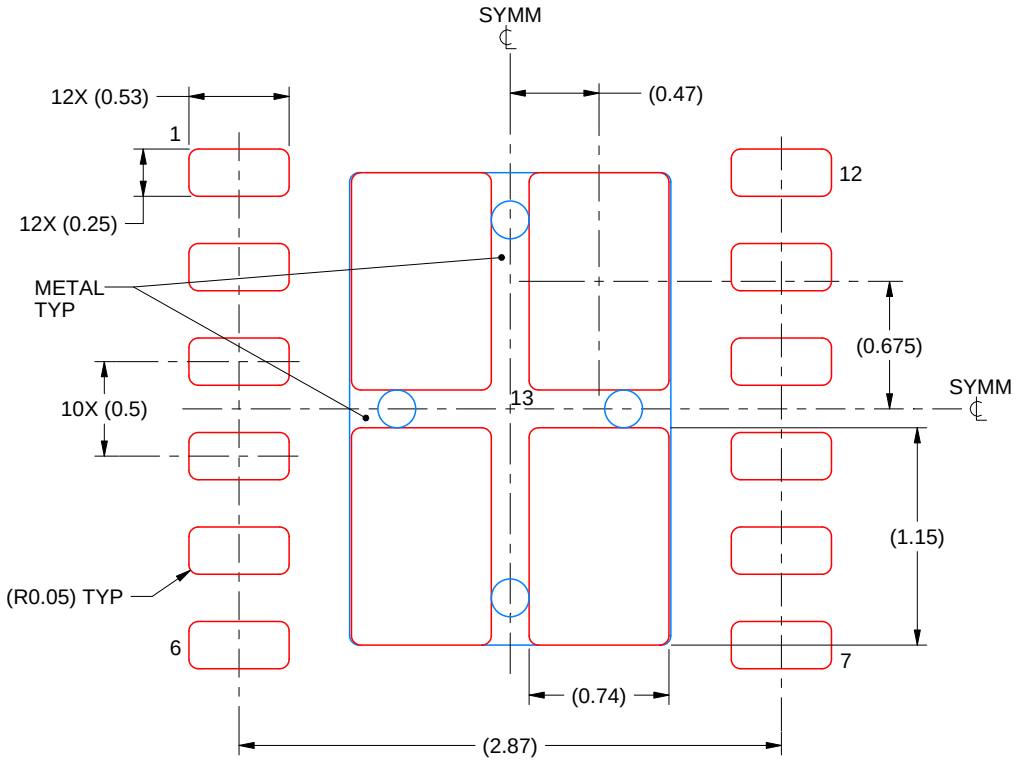
5. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
6. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

DRR0012D

WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
80.1% PRINTED SOLDER COVERAGE BY AREA
SCALE:25X

4223146/F 06/2026

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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最終更新日：2025 年 10 月