TEXAS INSTRUMENTS
LMR36503-Q1
JAJSIO6B – SEPTEMBER 2019 – REVISED SEPTEMBER 2020

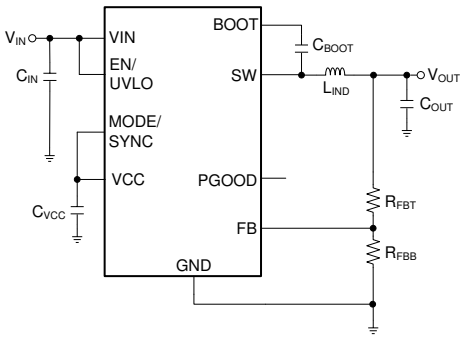
LMR36503-Q1 3V～65V、0.3A サイズと軽負荷時効率を最適化した同期整流降圧コンバータ

1 特長

- 車載アプリケーション用の AEC-Q100 認定取得済み:
  - デバイス温度グレード 1:–40℃～125℃、T_A
- 機能安全対応
  - 機能安全システムの設計に役立つ資料を利用可能
- 70% を超える効率 (5mA 時)
  - I_q:4μA (スイッチング時、24V_{IN}、3.3V_{OUT}、固定出力オプション)
- 小さなソリューション・サイズとわずかな部品コスト
  - ウェッタブル・フランク付きの 2mm × 2mm HotRod™ パッケージ
  - 内部補償
- 車載アプリケーション向けの設計:
  - 接合部温度範囲:–40℃～+150℃
  - CISPR 25 EMI 規格に準拠した疑似ランダム・スペクトラム拡散機能
  - 広い入力電圧範囲:3.0V (立ち下がりスレッショルド)～65V
  - 可変、3.3V および 5V 固定の出力電圧を選択可能
  - MODE/SYNC ピン・バリアントでは同期可能
  - 調整可能な F_{SW}:200kHz～2.2MHz (RT ピン・バリアントの場合)
  - LMR36506-Q1 (65V、600mA) とピン互換

2 アプリケーション

- 先進運転支援システム (ADAS)
- ボディ・エレクトロニクス / 照明
- インフォテインメントとクラスタ



概略回路図

3 概要

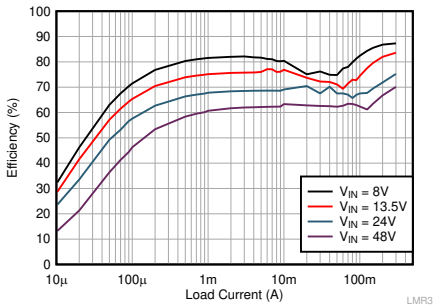
LMR36503-Q1 は、業界で最も小さな 2mm × 2mm の HotRod™ パッケージの 65V、0.3A 同期整流降圧 DC/DC コンバータです。この使いやすいコンバータは、最大 70V の入力過渡電圧に対応でき、非常に優れた EMI 性能を実現するとともに、固定 3.3V、5V およびその他の可変出力電圧をサポートしています。

LMR36503-Q1 はピーク電流モード制御アーキテクチャと内部補償により、最小の出力容量で安定した動作を維持します。LMR36503-Q1 は、広い入力動作範囲により、入力電圧に深いサグ状態が生じたときも動作し続けるため、過酷なコールド・クランク開始インパルスに耐える車載用アプリケーションに最適です。LMR36503-Q1 の PGOOD フラグは、出力電圧の状態を正確に示すため、外部のスーパーバイザは不要です。FPWM から PFM へのシームレスな移行と、超低スタンバイ静止電流により、LMR36503-Q1 は小さな出力負荷ではるかに高いシステム効率をサポートします。MODE/SYNC ピン・バリアントは、LMR36503-Q1 を外部クロックに同期させるのに役立ちます。適切な抵抗を選択することで、LMR36503-Q1 RT ピン・バリアントは、目的の任意のスイッチング周波数に外部でプログラムすることもできます。LMR36503-Q1 の豊富な機能セットは、広範な車載用最終機器を簡単に実装できるように設計されています。

製品情報

部品番号	パッケージ(1)	本体サイズ (公称)
LMR36503-Q1	VQFN-HR (9)	2.00mm × 2.00mm

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。



効率と出力電流の関係 V_{OUT} = 3.3V (固定)、2.2MHz

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Table of Contents

1 特長 ... 1
2 アプリケーション ... 1
3 概要 ... 1
4 Revision History ... 2
5 Device Comparison Table ... 3
6 Pin Configuration and Functions ... 4
Pin Functions ... 4
7 Specifications ... 5
7.1 Absolute Maximum Ratings ... 5
7.2 ESD (Automotive) Ratings ... 5
7.3 Recommended Operating Conditions ... 5
7.4 Thermal Information ... 6
7.5 Electrical Characteristics ... 6
7.6 Timing Characteristics ... 8
7.7 Switching Characteristics ... 8
7.8 System Characteristics ... 8
7.9 Typical Characteristics ... 10
8 Detailed Description ... 11
8.1 Overview ... 11
8.2 Functional Block Diagram ... 12
8.3 Feature Description ... 13
8.4 Device Functional Modes ... 23
9 Application and Implementation ... 29
9.1 Application Information ... 29
9.2 Typical Application ... 30
9.3 What to Do and What Not to Do ... 41
10 Power Supply Recommendations ... 41
11 Layout ... 42
11.1 Layout Guidelines ... 42
11.2 Layout Example ... 43
12 Device and Documentation Support ... 44
12.1 Documentation Support ... 44
12.2 ドキュメントの更新通知を受け取る方法 ... 44
12.3 サポート・リソース ... 44
12.4 Trademarks ... 44
12.5 静電気放電に関する注意事項 ... 44
12.6 用語集 ... 44
13 Mechanical, Packaging, and Orderable Information ... 45

4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision A (December 2019) to Revision B (September 2020)	Page
• デバイス・ステータスを「事前情報」から「量産データ」に変更	1
• 文書全体にわたって表、図、相互参照の採番方法を更新	1

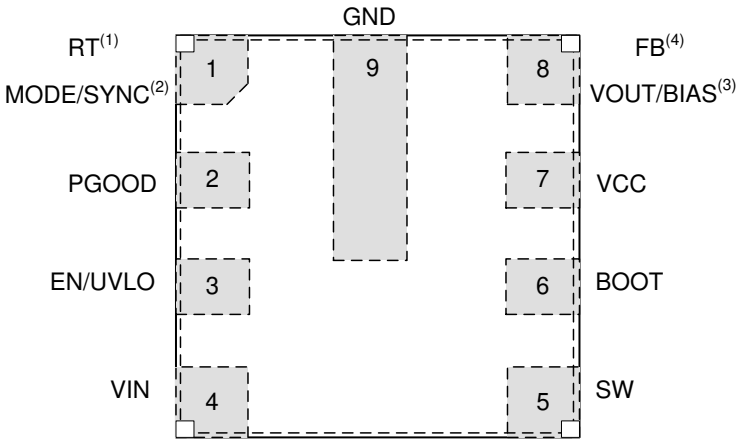
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5 Device Comparison Table

ORDERABLE PART NUMBER	OUTPUT VOLTAGE	EXTERNAL SYNC	F_{SW}	SPREAD SPECTRUM
LMR36503MSCQRPERQ1	Adjustable	Yes (PFM/FPWM Selectable)	Fixed 2.2 MHz	Yes
LMR36503MSC5RPERQ1	5-V Fixed	Yes (PFM/FPWM Selectable)	Fixed 2.2 MHz	Yes
LMR36503MSC3RPERQ1	3.3-V Fixed	Yes (PFM/FPWM Selectable)	Fixed 2.2 MHz	Yes
LMR36503RS3QRPERQ1	3.3-V Fixed	No (Default PFM at light load)	Adjustable with RT resistor	Yes
LMR36503RS5QRPERQ1	5-V Fixed	No (Default PFM at light load)	Adjustable with RT resistor	Yes

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6 Pin Configuration and Functions



A. See セクション 5 for more details. Pin 1 trimmed and factory-set for externally adjustable switching frequency RT variants only.
B. Pin 1 factory-set for fixed switching frequency MODE/SYNC variants only.
C. Pin 8 trimmed and factory-set for fixed output voltage VOUT/BIAS variants only.
D. Pin 8 factory-set for adjustable output voltage FB variants only.

図 6-1. 9-Pin (2 mm x 2 mm) VQFN-HR RPE Package (Top View)

Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
1	RT or MODE/SYNC	A	When part is trimmed as the RT variant, the switching frequency can be adjusted from 200 kHz to 2.2 MHz. When the part is trimmed as the MODE/SYNC variant, it can operate in user-selectable PFM/FPWM mode and can be synchronized to an external clock. *Do not float this pin.*
2	PGOOD	A	Open-drain power-good flag output. Connect to suitable voltage supply through a current limiting resistor. High = power OK, low = power bad. It goes low when EN = low. It can be open or grounded when not used.
3	EN/UVLO	A	Enable input to regulator. High = ON, low = OFF. Can be connected directly to VIN. *Do not float this pin.*
4	VIN	P	Input supply to regulator. Connect a high-quality bypass capacitor or capacitors directly to this pin and GND.
5	SW	P	Regulator switch node. Connect to power inductor.
6	BOOT	P	Bootstrap supply voltage for internal high-side driver. Connect a high-quality 100-nF capacitor from this pin to the SW pin.
7	VCC	P	Internal LDO output. Used as supply to internal control circuits. Do not connect to external loads. Can be used as logic supply for power-good flag. Connect a high-quality 1-µF capacitor from this pin to GND.
8	VOUT/BIAS or FB	A	Fixed output options are available with the VOUT/BIAS pin variant. Connect to output voltage node for fixed VOUT. Check セクション 5 for more details. The FB pin variant can help adjust the output voltage. Connect to tap point of feedback voltage divider. *Do not float this pin.*
9	GND	G	Power ground terminal. Connect to system ground. Connect to C_{IN} with short, wide traces.
A = Analog, P = Power, G = Ground			

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7 Specifications

7.1 Absolute Maximum Ratings

Over the recommended operating junction temperature range(1)

PARAMETER		MIN	MAX	UNIT
Voltage	VIN to GND	–0.3	70	V
	EN to GND	–0.3	70	V
	SW to GND	–0.3	70.3	V
	PGOOD to GND	0	20	V
	VOUT/BIAS to GND (Fixed output)	–0.3	16	V
	FB to GND - (Adjustable output)	–0.3	16	V
	BOOT to SW	–0.3	5.5	V
	VCC to GND	–0.3	5.5	V
	RT to GND (RT variant)	–0.3	5.5	V
	MODE/SYNC to GND (MODE/SYNC variant)	–0.3	5.5	V
T_J	Junction temperature	–40	150	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Stresses beyond those listed under セクション 7.1 may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under セクション 7.3. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 ESD (Automotive) Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002(1) HBM ESD classification level 2	±2000	V
		Charged-device model (CDM), per AEC Q100-011 CDM ESD classification level C5	±750	V

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

7.3 Recommended Operating Conditions

Over the recommended operating junction temperature range of –40 °C to 150 °C (unless otherwise noted)(1) (2)

		MIN	TYP	MAX	UNIT
Input voltage	Input voltage range after startup	3.6		65	V
Output current	Load current range(3)	0		0.3	A
Frequency setting	Selectable frequency range with RT (RT variant only)	0.2		2.2	MHz
	Set frequency value with RT connected to GND (RT variant only)		2.2		MHz
	Set frequency value with RT connected to VCC (RT variant only)		1		MHz
External clock setting	External Sync CLK (MODE/SYNC variant only)	0.2		2.2	MHz

(1) Recommended operating conditions indicate conditions for which the device is intended to be functional, but do not ensure specific performance limits. For ensured specifications, see Electrical Characteristics table.
(2) High junction temperatures degrade operating lifetimes. Operating lifetime is de-rated for junction temperatures greater than 125°C
(3) Maximum continuous DC current may be derated when operating with high switching frequency and/or high ambient temperature. See Application section for details.

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7.4 Thermal Information

The value of $R_{\theta JA}$ given in this table is only valid for comparison with other packages and cannot be used for design purposes. These values were calculated in accordance with JESD 51-7, and simulated on a 4-layer JEDEC board. They do not represent the performance obtained in an actual application. For example, with a 4-layer PCB, a $R_{\theta JA}$= 58°C/W can be achieved

THERMAL METRIC(1)		LMR36503-Q1 VQFN (RPE) 9 Pins	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	84.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	47.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	26.1	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	0.9	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	25.9	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report. The value of $R_{\Theta JA}$ given in this table is only valid for comparison with other packages and can not be used for design purposes. This value was calculated in accordance with JESD 51-7, and simulated on a 4-layer JEDEC board. It does not represent the performance obtained in an actual application. For design information see the Maximum Ambient Temperature section.

7.5 Electrical Characteristics

Limits apply over the recommended operating junction temperature (T_J) range of –40°C to +150°C, unless otherwise stated. Minimum and maximum limits are specified through test, design or statistical correlation. Typical values represent the most likely parametric norm at T_J = 25°C, and are provided for reference purposes only. Unless otherwise stated, the following conditions apply: V_{IN} = 24 V.(1)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY VOLTAGE (VIN PIN)						
V_{IN_R}	Minimum operating input voltage (rising)	Rising threshold		3.4	3.5	V
V_{IN_F}	Minimum operating input voltage (falling)	Once operating; Falling threshold	2.45	3.0		V
$I_{Q_13p5_Fixed}$	Non-switching input current; measured at VIN pin(2)	V_{IN} = V_{EN} = 13.5V ; $V_{OUT/BIAS}$ = 5.25V, $V_{MODE/SYNC}$ = V_{RT} = 0V; Fixed output	0.25	0.672	1.05	µA
$I_{Q_13p5_Adj}$	Non-switching input current; measured at VIN pin(2)	V_{IN} = V_{EN} = 13.5V ; V_{FB} = 1.05V, $V_{MODE/SYNC}$ = V_{RT} = 0V; Adjustable output	14	17	22	µA
$I_{Q_24p0_Fixed}$	Non-switching input current; measured at VIN pin(2)	V_{IN} = V_{EN} = 24V ; $V_{OUT/BIAS}$ = 5.25V, $V_{MODE/SYNC}$ = V_{RT} = 0V; Fixed output	0.8	1.2	1.7	µA
$I_{Q_24p0_Adj}$	Non-switching input current; measured at VIN pin(2)	V_{IN} = V_{EN} = 24V ; V_{FB} = 1.05V, $V_{MODE/SYNC}$ = V_{RT} = 0V; Adjustable output	14	18	22	µA
I_{B_13p5}	Current into VOUT/BIAS pin (not switching)(2)	V_{IN} = 13.5V, $V_{OUT/BIAS}$ = 5.25V, $V_{MODE/SYNC}$ = V_{RT} = 0V; Fixed output	14	17	22	µA
I_{B_24p0}	Current into VOUT/BIAS pin (not switching)(2)	V_{IN} = 24V, $V_{OUT/BIAS}$ = 5.25V, $V_{MODE/SYNC}$ = V_{RT} = 0V; Fixed output	14	18	22	µA
I_{SD_13p5}	Shutdown quiescent current; measured at VIN pin(2)	V_{EN} = 0; V_{IN} = 13.5V		0.5	1.1	µA
I_{SD_24p0}	Shutdown quiescent current; measured at VIN pin(2)	V_{EN} = 0; V_{IN} = 24V		1	1.6	µA
ENABLE (EN PIN)						
$V_{EN-WAKE}$	Enable wake-up threshold		0.4			V
$V_{EN-VOUT}$	Precision enable high level for VOUT		1.16	1.263	1.36	V
$V_{EN-HYST}$	Enable threshold hysteresis below $V_{EN-\ VOUT}$		0.3	0.35	0.4	V
I_{LKG-EN}	Enable input leakage current	VEN = 3.3 V		0.3	8	nA
INTERNAL LDO						

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Limits apply over the recommended operating junction temperature (T_J) range of –40°C to +150°C, unless otherwise stated. Minimum and maximum limits are specified through test, design or statistical correlation. Typical values represent the most likely parametric norm at T_J = 25°C, and are provided for reference purposes only. Unless otherwise stated, the following conditions apply: V_{IN} = 24 V.(1)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{CC}	Internal VCC voltage	Adjustable or fixed output; Auto mode	3.125	3.15	3.22	V
I_{CC}	Bias regulator current limit			65	240	mA
$V_{CC-UVLO}$	Internal VCC undervoltage lockout	VCC rising under voltage threshold	3	3.3	3.65	V
$V_{CC-UVLO-HYST}$	Internal VCC under voltage lock-out hysteresis	Hysteresis below $V_{CC-UVLO}$	0.4	0.8	1.2	V
CURRENT LIMITS						
I_{SC-0p3}	Short circuit high side current Limit(3)	0.3A Version	0.42	0.5	0.575	A
$I_{LS-LIMIT-0p3}$	Low side current limit(3)	0.3A Version	0.3	0.35	0.4	A
$I_{PEAK-MIN-0p3}$	Minimum peak inductor current(3)	PFM Operation, 0.3A Version; Duty Factor = 0	0.067	0.09	0.11	A
I_{ZC}	Zero cross current(3)	Auto mode	0	0.01	0.022	A
I_{L-NEG}	Sink current limit (negative)(3)	FPWM mode	0.6	0.7	0.8	A
POWER GOOD						
PG-OV	PGOOD upper threshold - rising	% of FB (Adjustable output) or % of VOUT/BIAS (Fixed output)	106	107	110	%
PG-UV	PGOOD lower threshold - falling	% of FB (Adjustable output) or % of VOUT/BIAS (Fixed output)	93	94	96.5	%
PG-HYS	PGOOD hysteresis - rising/falling	% of FB (Adjustable output) or % of VOUT/BIAS (Fixed output)	1.3	1.8	2.3	%
$V_{PG-VALID}$	Minimum input voltage for proper PG function		0.75	1	2	V
$R_{PG-EN5p0}$	$R_{DS(ON)}$ PGOOD output	VEN = 5.0V, 1mA pull-up current	20	40	70	Ω
R_{PG-EN0}	$R_{DS(ON)}$ PGOOD output	VEN = 0 V, 1mA pull-up current	10	18	31	Ω
OSCILLATOR (MODE/SYNC)						
V_{MODE_H}	Sync input and mode high level threshold		1.8			V
$V_{SYNC-HYS}$	Sync input hysteresis		230	300	380	mV
V_{MODE_L}	Sync input and mode low level threshold				0.8	V
MOSFETS						
$R_{DS-ON-HS}$	High-side MOSFET on-resistance	Load = 0.3 A		560	920	mΩ
$R_{DS-ON-LS}$	Low-side MOSFET on-resistance	Load = 0.3 A		280	460	mΩ
$V_{CBOOT-UVLO}$	Cboot - SW UVLO threshold(4)		2.14	2.3	2.42	V
VOLTAGE REFERENCE						
$V_{OUT_Fixed3p3}$	Initial VOUT voltage accuracy for 3.3 V	FPWM mode	3.25	3.3	3.34	V
$V_{OUT_Fixed5p0}$	Initial VOUT voltage accuracy for 5 V	FPWM mode	4.93	5	5.07	V
V_{REF}	Internal reference voltage	V_{IN} = 3.6V to 65V, FPWM mode	0.985	1	1.01	V
I_{FB}	FB input current	Adjustable output, FB = 1V		85	110	nA

(1) MIN and MAX limits are 100% production tested at 25ºC. Limits over the operating temperature range verified through correlation using Statistical Quality Control (SQC) methods. Limits are used to calculate Average Outgoing Quality Level (AOQL).
(2) This is the current used by the device open loop. It does not represent the total input current of the system when in regulation.
(3) The current limit values in this table are tested, open loop, in production. They may differ from those found in a closed loop application.
(4) When the voltage across the C_{BOOT} capacitor falls below this voltage, the low side MOSFET is turn to recharge the boot capacitor

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7.6 Timing Characteristics

Limits apply over the recommended operating junction temperature (T_J) range of –40°C to +150°C, unless otherwise stated. Minimum and maximum limits are specified through test, design or statistical correlation. Typical values represent the most likely parametric norm at T_J = 25°C, and are provided for reference purposes only. Unless otherwise stated, the following conditions apply: V_{IN} = 24 V.(1)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SOFT START						
t_{SS}	Time from first SW pulse to V_{FB} at 90%, of V_{REF}	V_{IN} ≥ 3.6 V	1.95	2.58	3.2	ms
POWER GOOD						
t_{RESET_FILTER}	Glitch filter time constant for PG function		15	25	40	µs
t_{PGOOD_ACT}	Delay time to PG high signal		1.7	1.956	2.16	ms
OSCILLATOR (MODE/SYNC)						
t_{PULSE_H}	High duration needed to be recognized as a pulse		100			ns
t_{PULSE_L}	Low duration needed to be recognized as a pulse		100			ns
t_{SYNC}	High/low signal duration in a valid synchronization signal		6	9	12	µs
t_{MODE}	Time at one level needed to indicate FPWM or Auto Mode		18			µs

(1) MIN and MAX limits are 100% production tested at 25°C. Limits over the operating temperature range are verified through correlation usingStatistical Quality Control (SQC) methods. Limits are used to calculate Average Outgoing Quality Level (AOQL).

7.7 Switching Characteristics

Limits apply over the recommended operating junction temperature (T_J) range of –40°C to +150°C, unless otherwise stated. Minimum and maximum limits are specified through test, design or statistical correlation. Typical values represent the most likely parametric norm at T_J = 25°C, and are provided for reference purposes only. Unless otherwise stated, the following conditions apply: V_{IN} = 24 V.(1)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
PWM LIMITS (SW)						
$t_{ON\text{-}MIN}$	Minimum switch on-time	I_{OUT} = 0.3 A	35	60	97	ns
$t_{OFF\text{-}MIN}$	Minimum switch off-time		40	58	77	ns
$t_{ON\text{-}MAX}$	Maximum switch on-time	HS timeout in dropout	7.6	9	9.8	µs
OSCILLATOR (RT)						
f_{OSC_2p2MHz}	Internal oscillator frequency	RT = GND	2.1	2.2	2.3	MHz
f_{OSC_1p0MHz}	Internal oscillator frequency	RT = VCC	0.93	1	1.05	MHz
f_{ADJ_400kHz}		RT = 39.2 kΩ	0.34	0.4	0.46	MHz

(1) MIN and MAX limits are 100% production tested at 25°C. Limits over the operating temperature range are verified through correlation usingStatistical Quality Control (SQC) methods. Limits are used to calculate Average Outgoing Quality Level (AOQL).

7.8 System Characteristics

The following specifications apply only to the typical applications circuit, with nominal component values. Specifications in the typical (TYP) column apply to T_J = 25°C only. Specifications in the minimum (MIN) and maximum (MAX) columns apply to the case of typical components over the temperature range of T_J = –40°C to 150°C. These specifications are not ensured by production testing.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
STANDBY CURRENT AND DUTY RATIO						
I_{SUPPLY}	Input supply current when in regulation	V_{IN} = 13.5 V, $V_{OUT/BIAS}$ = 3.3 V, I_{OUT} = 0 A, PFM mode		6.5		µA
I_{SUPPLY}	Input supply current when in regulation	V_{IN} = 24 V, $V_{OUT/BIAS}$ = 3.3 V, I_{OUT} = 0 A, PFM mode		4		µA

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The following specifications apply only to the typical applications circuit, with nominal component values. Specifications in the typical (TYP) column apply to T_J = 25°C only. Specifications in the minimum (MIN) and maximum (MAX) columns apply to the case of typical components over the temperature range of T_J = –40°C to 150°C. These specifications are not ensured by production testing.

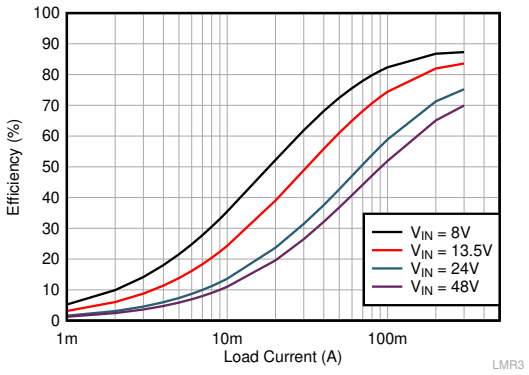
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
D_{MAX}	Maximum switch duty cycle(1)			98%		
OUTPUT VOLTAGE ACCURACY (VOUT/BIAS)						
$V_{OUT_3p3V_ACC}$	V_{OUT} = 3.3 V, V_{IN} = 3.6 V to 65 V, I_{OUT} = 0 to full load(2)	FPWM mode	–1.5		1.5	%
$V_{OUT_3p3V_ACC}$	V_{OUT} = 3.3 V, V_{IN} = 3.6V to 65 V, I_{OUT} = 0 A to full load(2)	Auto mode	–1.5		2.5	%
SPREAD SPECTRUM						
f_{SSS}	Frequency span of spread spectrum operation - largest deviation from center frequency	Spread spectrum active		±2		%
f_{PSS}	Spread spectrum pseudo random pattern frequency			0.98	1.5	Hz
THERMAL SHUTDOWN						
T_{SD-R}	Thermal shutdown rising	Shutdown threshold	158	168	180	°C
T_{SD-F}	Thermal shutdown falling	Recovery threshold	150	158	165	°C
T_{SD-HYS}	Thermal shutdown hysteresis		8	10	15	°C

(1) In dropout the switching frequency drops to increase the effective duty cycle. The lowest frequency is clamped at approximately: f_{MIN} = 1 / (t_{ON-MAX} + $T_{OFF-MIN}$). D_{MAX} = t_{ON-MAX} /(t_{ON-MAX} + $t_{OFF-MIN}$).
(2) Deviation is with respect to V_{IN} =13.5 V

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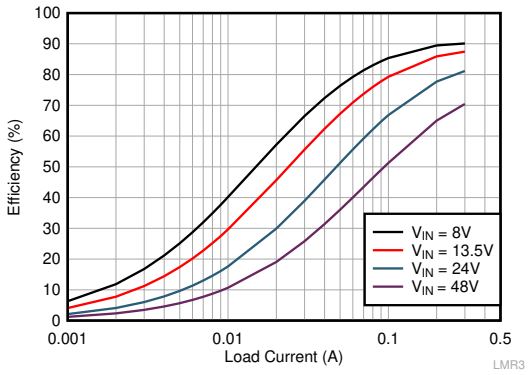
7.9 Typical Characteristics

Unless otherwise specified, the following conditions apply: T_A = 25°C, V_{IN} = 13.5 V.



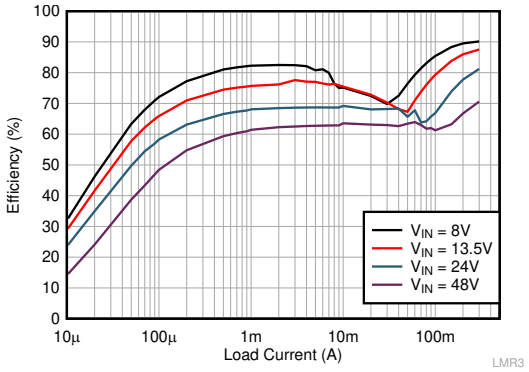
V_{OUT} = 3.3 V Fixed F_{SW} = 2.2 MHz (FPWM)

図 7-1. Efficiency 3.3-V Output, FPWM



V_{OUT} = 5 V Fixed F_{SW} = 2.2 MHz (FPWM)

図 7-2. Efficiency 5-V Output, FPWM



V_{OUT} = 5 V Fixed F_{SW-NOM} = 2.2 MHz (Auto)

図 7-3. Efficiency 5-V Output, Auto Mode

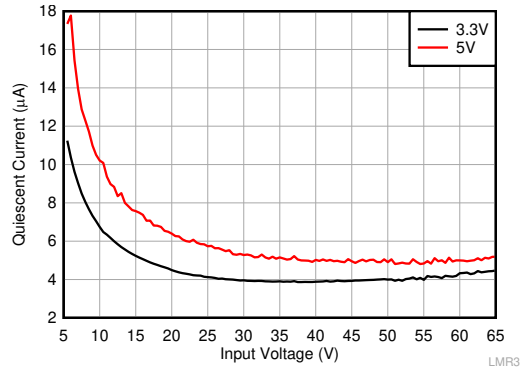
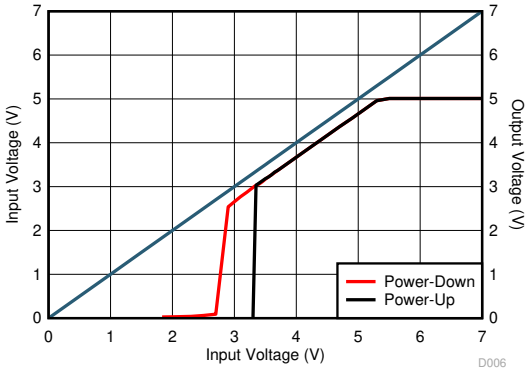


図 7-4. Typical Input Supply Current at No Load for Fixed 3.3-V and 5-V Output



I_{Load} = 300 mA V_{OUT} = 5 V Fixed F_{SW-NOM} = 2.2 MHz (Auto)

図 7-5. Dropout at Power-Up and Power-Down

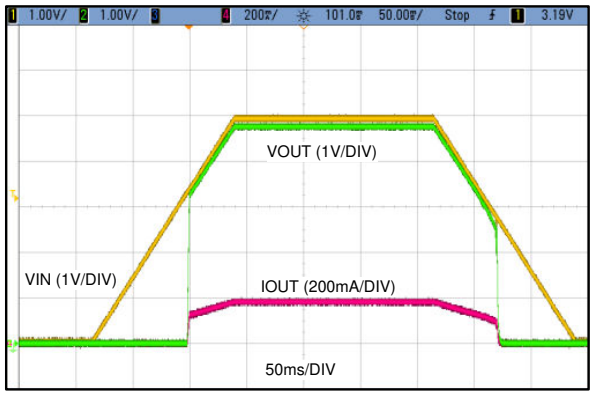


図 7-6. Typical Start-up and Shutdown at V_{OUT} = 5 V

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8 Detailed Description

8.1 Overview

The LMR36503-Q1 is a wide input, low-quiescent current, high-performance regulator that can operate over a wide range of duty ratio and the switching frequencies, including sub-AM band at 400 kHz and above AM band at 2.2 MHz. During wide input transients, if the minimum ON-time or the minimum OFF-time cannot support the desired duty ratio at the higher switching frequency settings, the switching frequency is reduced automatically, allowing the LMR36503-Q1 to maintain the output voltage regulation. With an internally-compensated design optimized for minimal output capacitors, the system design process with the LMR36503-Q1 is simplified significantly compared to other buck regulators available in the market.

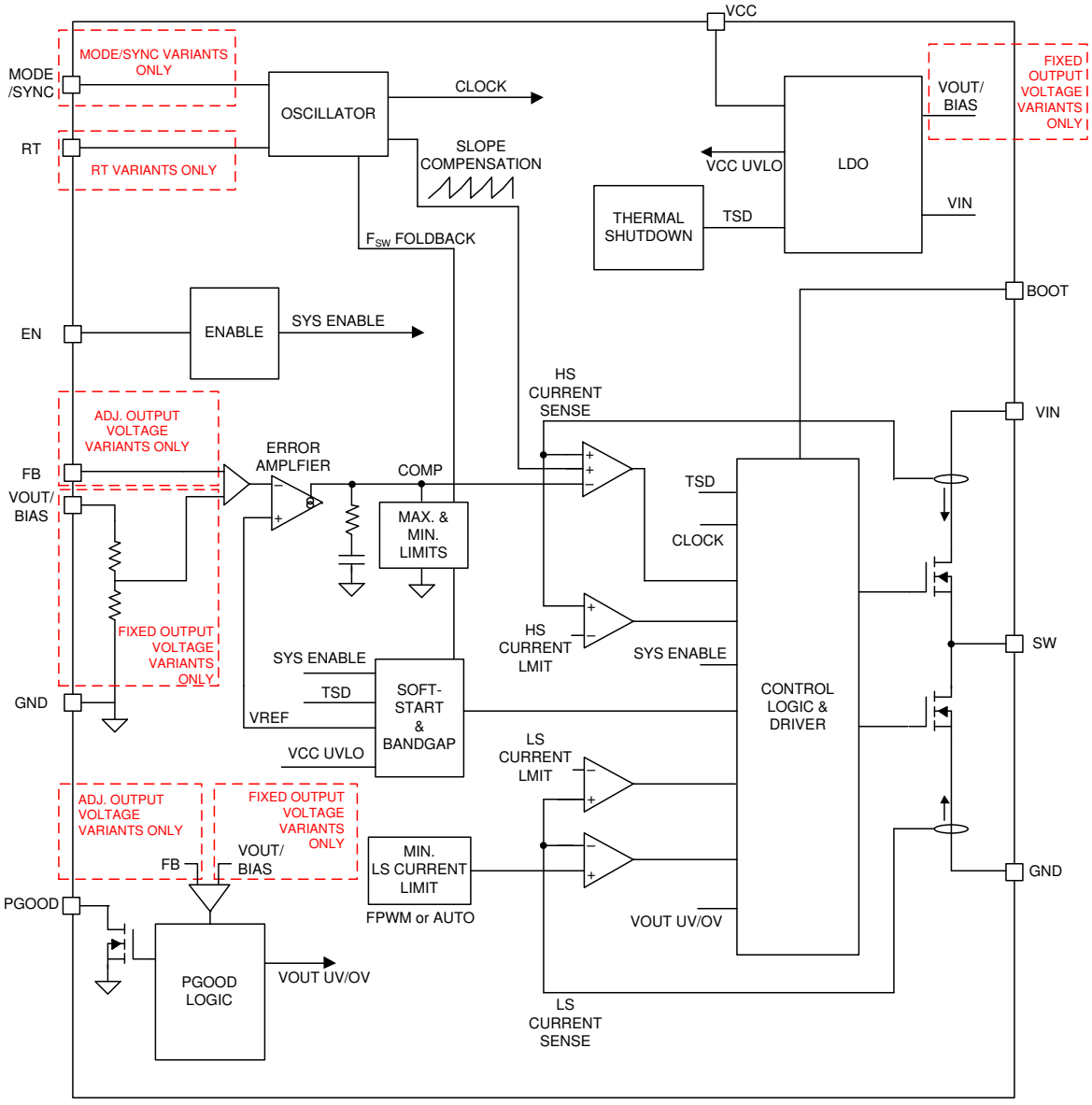
The LMR36503-Q1 is designed to minimize external component cost and solution size while operating in all demanding automotive environments. The LMR36503-Q1 family includes variants that can be set-up to operate over a wide switching frequency range, from 200 kHz to 2.2 MHz, with the correct resistor selection from RT pin to ground. To further reduce system cost, the PGOOD output feature with built-in delayed release allows the elimination of the reset supervisor in many applications.

The LMR36503-Q1 family is designed to reduce EMI/EMC emissions. The design includes a pseudo-random spread spectrum switching frequency dithering scheme, has no bond-wire flip-chip on the lead (HotRod™) package, and is available with the MODE/SYNC feature (select variants), allowing synchronization to an external clock, when available. Together, these features eliminate the need for any common-mode choke or shielding or any elaborate input filter design scheme, greatly reducing the complexity and cost of the EMI/EMC mitigation measures.

The LMR36503-Q1 comes in an ultra-small 2-mm x 2-mm QFN package with wettable flanks allowing for quick optical inspection along with specially designed corner anchor pins for reliable board level solder connections.

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8.2 Functional Block Diagram



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8.3 Feature Description

8.3.1 Enable, Start-up and Shutdown

Voltage at the EN pin controls the start-up or remote shutdown of the LMR36503-Q1 family of devices. The part stays shut down as long as the EN pin voltage is less than $V_{EN-WAKE}$ = 0.4 V. During the shutdown, the input current drawn by the device typically drops down to 0.5 µA (VIN = 13.5 V). With the voltage at the EN pin greater than the $V_{EN-WAKE}$, the device enters the device standby mode, the internal LDO powers up to generate VCC. As the EN voltage increases further, approaching $V_{EN-VOUT}$, the device finally starts to switch, entering the start-up mode, with a soft start. During the device shutdown process, when the EN input voltage measures less than ($V_{EN-VOUT}$ − $V_{EN-HYST}$), the regulator stops switching and re-enters the device standby mode. Any further decrease in the EN pin voltage, below $V_{EN-WAKE}$, the device is then firmly shut down. The high-voltage compliant EN input pin can be connected directly to the VIN input pin if remote precision control is not needed. The EN input pin must not be allowed to float. The various EN threshold parameters and their values are listed in *セクション 7.5*. 図 8-2 shows the precision enable behavior. 図 8-3 shows a typical remote EN start-up waveform in an application. Once EN goes high, after a delay of about 1 ms, the output voltage begins to rise with a soft start and reaches close to the final value in about 2.67 ms (t_{ss}). After a delay of about 2 ms (t_{PGOOD_ACT}), the PGOOD flag goes high. During start-up, the device is not allowed to enter FPWM mode until the soft-start time has elapsed. This time is measured from the rising edge of EN. Check *セクション 9.2.2.8.1* for component selection.

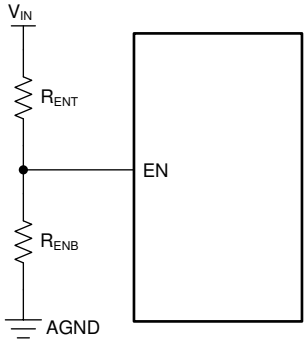


図 8-1. VIN UVLO Using the EN pin

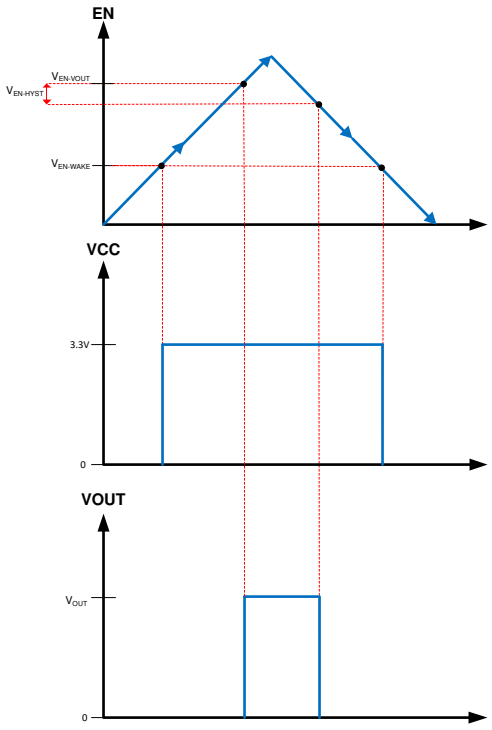


図 8-2. Precision Enable Behavior

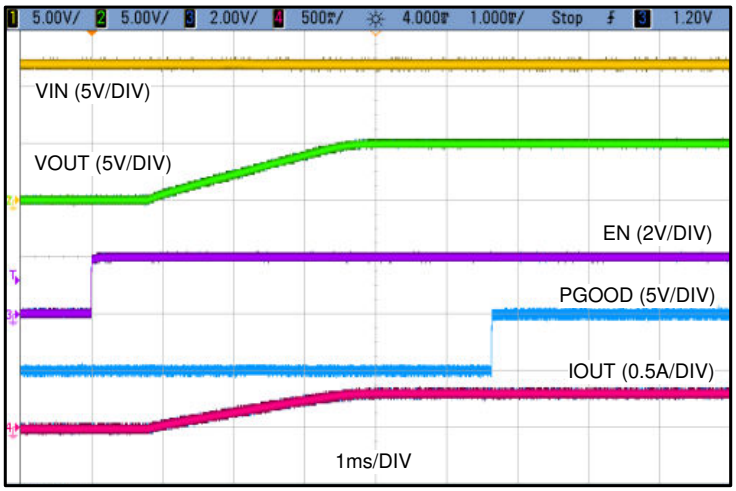


図 8-3. Enable Start-up V_{IN} = 12 V, V_{OUT} = 5 V, I_{OUT} = 300 mA

8.3.2 External CLK SYNC (with MODE/SYNC)

It is often desirable to synchronize the operation of multiple regulators in a single system, resulting in a well-defined system level performance. The select variants in the LMR36503-Q1 with the MODE/SYNC pin allow the power designer to synchronize the device to a common external clock. The LMR36503-Q1 implements an in-phase locking scheme, where the rising edge of the clock signal, provided to the MODE/SYNC pin of the LMR36503-Q1, corresponds to the turning on of the high-side device. The external clock synchronization is implemented using a phase locked loop (PLL) eliminating any large glitches. The external clock fed into the LMR36503-Q1 replaces the internal free-running clock, but does not affect any frequency foldback operation. Output voltage continues to be well-regulated. The device remains in FPWM mode and operates in CCM for light loads when synchronization input is provided.

The MODE/SYNC input pin in the LMR36503-Q1 can operate in one of three selectable modes:

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- Auto Mode: Pulse frequency modulation (PFM) operation is enabled during light load and diode emulation prevents reverse current through the inductor. See セクション 8.4.3.2 for more details.
- FPWM Mode: In FPWM mode, diode emulation is disabled, allowing current to flow backwards through the inductor. This allows operation at full frequency even without load current. See セクション 8.4.3.3 for more details.
- SYNC Mode: The internal clock locks to an external signal applied to the MODE/SYNC pin. As long as output voltage can be regulated at full frequency and is not limited by minimum off-time or minimum on-time, clock frequency is matched to the frequency of the signal applied to the MODE/SYNC pin. While the device is in SYNC mode, it operates as though in FPWM mode: diode emulation is disabled allowing the frequency applied to the MODE/SYNC pin to be matched without a load.

8.3.2.1 Pulse-Dependent MODE/SYNC Pin Control

Most systems that require more than a single mode of operation from the LMR36503-Q1 are controlled by digital circuitry such as a microprocessor. These systems can generate dynamic signals easily but have difficulty generating multi-level signals. Pulse-Dependent MODE/SYNC pin control is useful with these systems. To initiate Pulse-Dependent MODE/SYNC pin control, a valid sync signal must be applied. 表 8-1 shows a summary of the pulse dependent mode selection settings.

表 8-1. Pulse-Dependent Mode Selection Settings

MODE/SYNC INPUT	MODE
> V_{MODE_H}	FPWM with Spread Spectrum factory setting
< V_{MODE_L}	Auto Mode with Spread Spectrum factory setting
Synchronization Clock	SYNC Mode

図 8-4 shows the transition between AUTO Mode and FPWM Mode while in Pulse-Dependent MODE/SYNC control. The LMR36503-Q1 transitions to a new mode of operation after the time, t_{MODE}. 図 8-4 and 図 8-5 show the details.

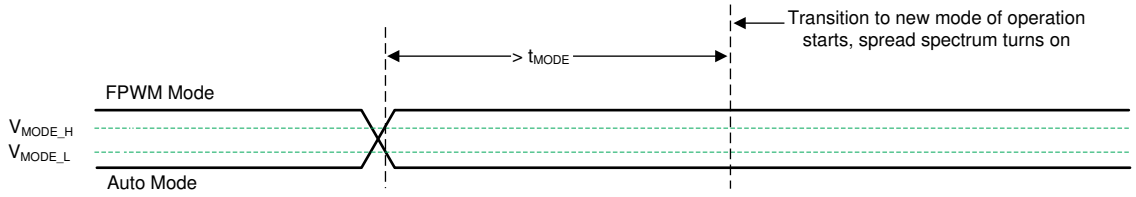


図 8-4. Transition from Auto Mode and FPWM Mode

If MODE/SYNC voltage remains constant longer than t_{MODE}, the LMR36503-Q1 enters either Auto mode or FPWM mode with spread spectrum turned on (if factory setting is enabled) and MODE/SYNC continues to operate in Pulse-Dependent scheme.

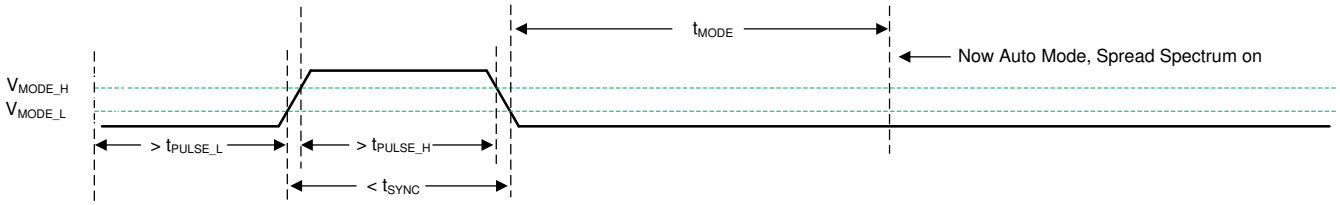


図 8-5. Transition from SYNC Mode to Auto Mode

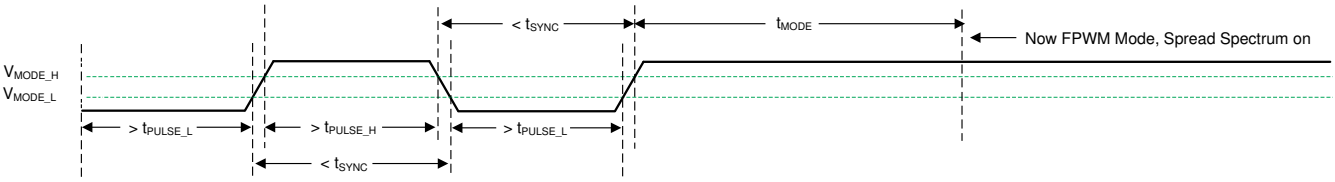


図 8-6. Transition from SYNC Mode to FPWM Mode

8.3.3 Adjustable Switching Frequency (with RT)

The select variants in the LMR36503-Q1 family with the RT pin allow the power designers to set any desired operating frequency between 200 kHz and 2.2 MHz in their applications. See 図 8-7 to determine the resistor value needed for the desired switching frequency. The RT pin and the MODE/SYNC pin variants share the same pin location. The power supply designer can either use the RT pin variant and adjust the switching frequency of operation as warranted by the application or use the MODE/SYNC variant and synchronize to an external clock signal. See 表 8-2 for selection on programming the RT pin.

表 8-2. RT Pin Setting

RT INPUT	SWITCHING FREQUENCY
VCC	1 MHz
GND	2.2 MHz
RT to GND	Adjustable according to 図 8-7
Float (Not Recommended)	No Switching

式 1 can be used to calculate the value of RT for a desired frequency.

$$RT = \frac{18286}{Fsw^{1.021}} \quad (1)$$

where

- RT = Frequency setting resistor value (kΩ)
- F_{SW} = Switching frequency (kHz)

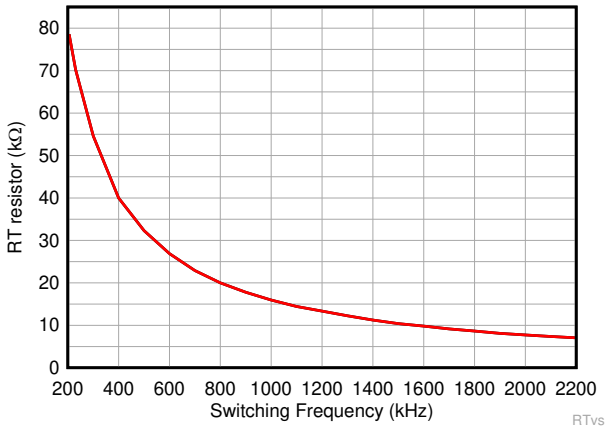


図 8-7. RT Values vs Frequency

8.3.4 Power-Good Output Operation

The power-good feature using the PG pin of the LMR36503-Q1 can be used to reset a system microprocessor whenever the output voltage is out of regulation. This open-drain output remains low under device fault conditions, such as current limit and thermal shutdown, as well as during normal start-up. A glitch filter prevents false flag operation for any short duration excursions in the output voltage, such as during line and load

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transients. Output voltage excursions lasting less than t_{RESET_FILTER} do not trip the power-good flag. Power-good operation can best be understood in reference to 図 8-8. 表 8-3 gives a more detailed breakdown the PGOOD operation. Here, V_{PG-UV} is defined as the PG-UV scaled version of the $V_{OUT-Reg}$ (target regulated output voltage) and V_{PG-HYS} as the PG-HYS scaled version of the $V_{OUT-Reg}$, where both PG-UV and PG-HYS are listed in セクション 7.5. During the initial power up, a total delay of 5 ms (typ.) is encountered from the time the $V_{EN-VOUT}$ is triggered to the time that the power-good is flagged high. This delay only occurs during the device start-up and is not encountered during any other normal operation of the power-good function. When EN is pulled low, the power-good flag output is also forced low. With EN low, power-good remains valid as long as the input voltage ($V_{PG-VALID}$ is ≥ 1 V (typical).

The power-good output scheme consists of an open-drain n-channel MOSFET, which requires an external pullup resistor connected to a suitable logic supply. It can also be pulled up to either V_{CC} or V_{OUT} through an appropriate resistor, as desired. If this function is not needed, the PGOOD pin can be open or grounded. Limit the current into this pin to ≤ 4 mA.

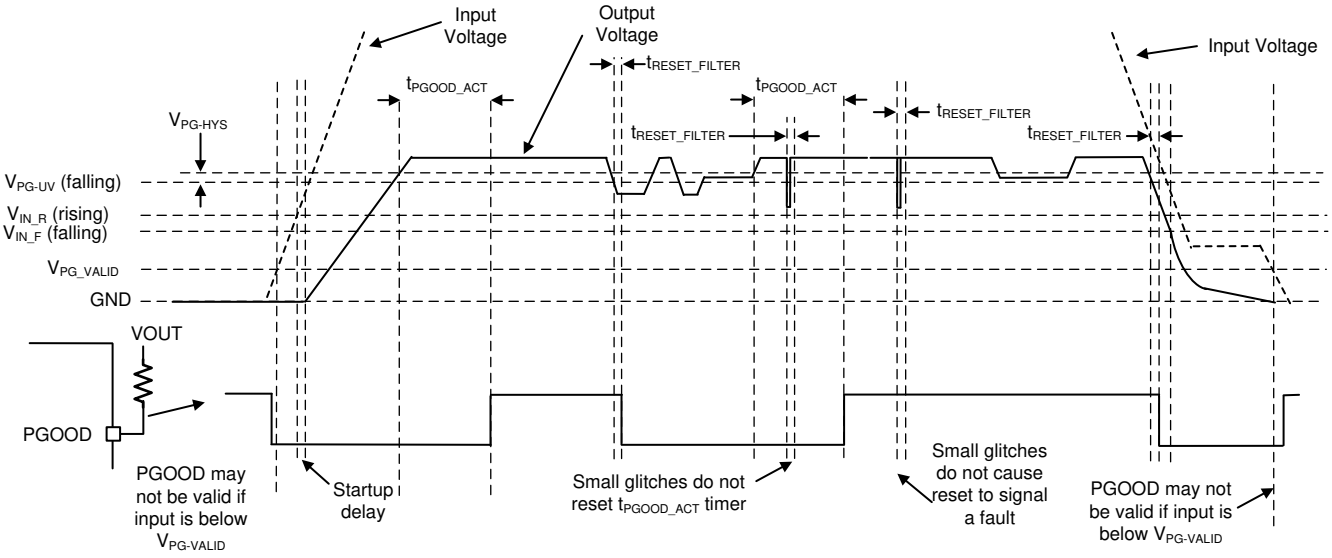


図 8-8. Power-Good Operation (OV Events Not Included)

表 8-3. Fault Conditions for PGOOD (Pull Low)

FAULT CONDITION INITIATED	FAULT CONDITION ENDS (AFTER WHICH t_{PGOOD_ACT} MUST PASS BEFORE PGOOD OUTPUT IS RELEASED)
$V_{OUT} < V_{PG-UV}$ AND $t > t_{RESET_FILTER}$	Output voltage in regulation: $V_{PG-UV} + V_{PG-HYS} < V_{OUT} < V_{PG-OV} - V_{PG-HYS}$
$V_{OUT} > V_{PG-OV}$ AND $t > t_{RESET_FILTER}$	Output voltage in regulation
$T_J > T_{SD-R}$	$T_J < T_{SD-F}$ AND output voltage in regulation
$EN < V_{EN-VOUT} - V_{EN-HYST}$	$EN > V_{EN-VOUT}$ AND output voltage in regulation
$V_{CC} < V_{CC-UVLO} - V_{CC-UVLO-HYST}$	$V_{CC} > V_{CC-UVLO}$ AND output voltage in regulation

8.3.5 Internal LDO, VCC UVLO, and VOUT/BIAS Input

The LMR36503-Q1 uses the internal LDO output and the VCC pin for all internal power supply. The VCC pin draws power either from the VIN (in adjustable output variants) or the VOUT/BIAS (in fixed-output variants). In the fixed output variants, once the LMR36503-Q1 is active but has yet to regulate, the VCC rail will continue to draw power from the input voltage, VIN, until the VOUT/BIAS voltage reaches > 3.15 V (or when the device has reached steady-state regulation post the soft start). The VCC rail typically measures 3.15 V in both adjustable and fixed output variants. To prevent unsafe operation, VCC has an undervoltage lockout, which prevents switching if the internal voltage is too low. See $V_{VCC-UVLO}$ and $V_{VCC-UVLO-HYST}$ in セクション 7.5. During start-up, VCC momentarily exceeds the normal operating voltage until $V_{VCC-UVLO}$ is exceeded, then drops to the normal

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operating voltage. Note that these undervoltage lockout values, when combined with the LDO dropout, drives the minimum input voltage rising and falling thresholds.

8.3.6 Bootstrap Voltage and $V_{CBOOT-UVLO}$ (CBOOT Terminal)

The high-side switch driver circuit requires a bias voltage higher than VIN to ensure the HS switch is turned ON. The capacitor connected between CBOOT and SW works as a charge pump to boost voltage on the CBOOT terminal to (SW+VCC). The boot diode is integrated on the LMR36503-Q1 die to minimize physical solution size. A 100-nF capacitor rated for 10 V or higher is recommended for CBOOT. The CBOOT rail has an UVLO setting. This UVLO has a threshold of $V_{CBOOT-UVLO}$ and is typically set at 2.3 V. If the CBOOT capacitor is not charged above this voltage with respect to the SW pin, then the part initiates a charging sequence, turning on the low-side switch before attempting to turn on the high-side device.

8.3.7 Output Voltage Selection

In the LMR36503-Q1 family, select variants with an adjustable output voltage option (see *セクション 5*), and you need an external resistor divider connection between the output voltage node, the device FB pin, and the system GND, as shown in 図 8-9. The variants with adjustable output voltage option in the LMR36503-Q1 family are designed with a 1-V internal reference voltage.

$$R_{FBB} = \frac{R_{FBT}}{V_{OUT} - 1} \tag{2}$$

When using the fixed-output variants from the LMR36503-Q1 family, simply connect the FB pin (will be identified as VOUT/BIAS pin for fixed-output variants in the rest of the data sheet) to the system output voltage node. See *セクション 5* for more details.

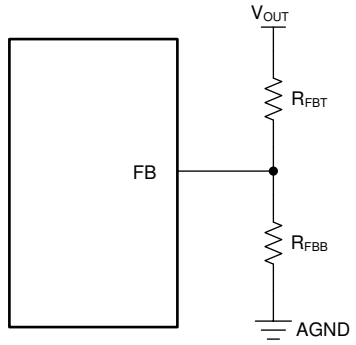


図 8-9. Setting Output Voltage for Adjustable Output Variant

In adjustable output voltage variants, an addition feed-forward capacitor, C_{FF}, in parallel with the R_{FBT}, can be used to optimize the phase margin and transient response. See *セクション 9.2.2.8* for more details. No additional resistor divider or feed-forward capacitor, C_{FF}, is needed in fixed-output variants.

8.3.8 Soft Start and Recovery from Dropout

When designing with the LMR36503-Q1, slow rise in output voltage due to recovery from dropout and soft start should be considered as a two separate operating conditions, as shown in 図 8-10 and 図 8-11. Soft start is triggered by any of the following conditions:

- Power is applied to the VIN pin of the device, releasing undervoltage lockout.
- EN is used to turn on the device.
- Recovery from shutdown due to overtemperature protection.

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Once soft start is triggered, the IC takes the following actions:

- The reference used by the IC to regulate output voltage is slowly ramped up. The net result is that output voltage, if previously 0 V, takes t_{SS} to reach 90% of the desired value.
- Operating mode is set to auto mode of operation, activating the diode emulation mode for the low-side MOSFET. This allows start-up without pulling the output low. This is true even when there is a voltage already present at the output during a pre-bias start-up.

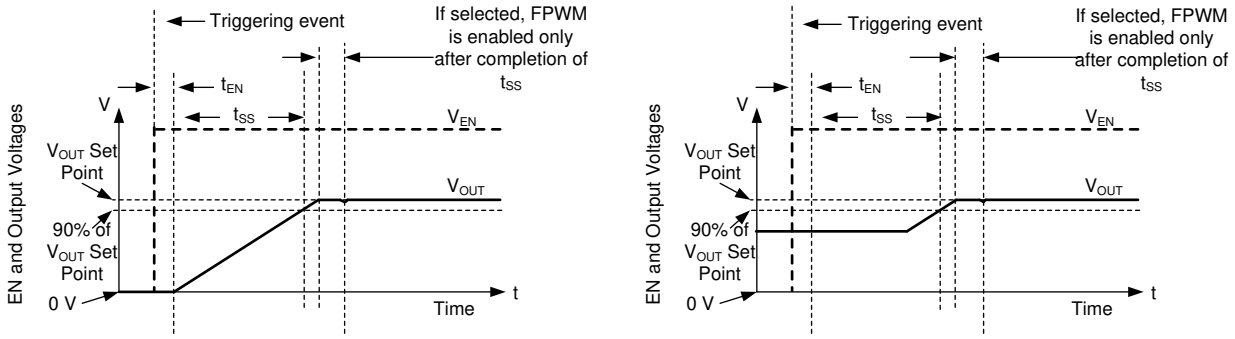


図 8-10. Soft Start With and Without Pre-bias Voltage

8.3.8.1 Recovery from Dropout

Any time the output voltage falls more than a few percent, output voltage ramps up slowly. This condition, called graceful recovery from dropout in this document, differs from soft start in two important ways:

- The reference voltage is set to approximately 1% above what is needed to achieve the existing output voltage.
- If the device is set to FPWM, it will continue to operate in that mode during its recovery from dropout. If output voltage were to suddenly be pulled up by an external supply, the LMR36503-Q1 can pull down on the output. Note that all protections that are present during normal operation are in place, preventing any catastrophic failure if output is shorted to a high voltage or ground.

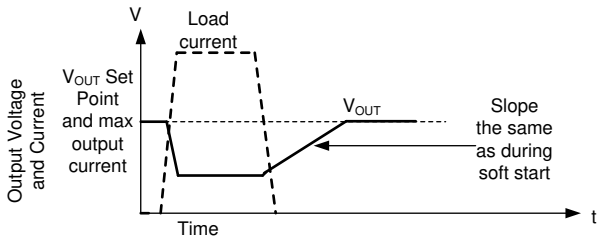


図 8-11. Recovery from Dropout

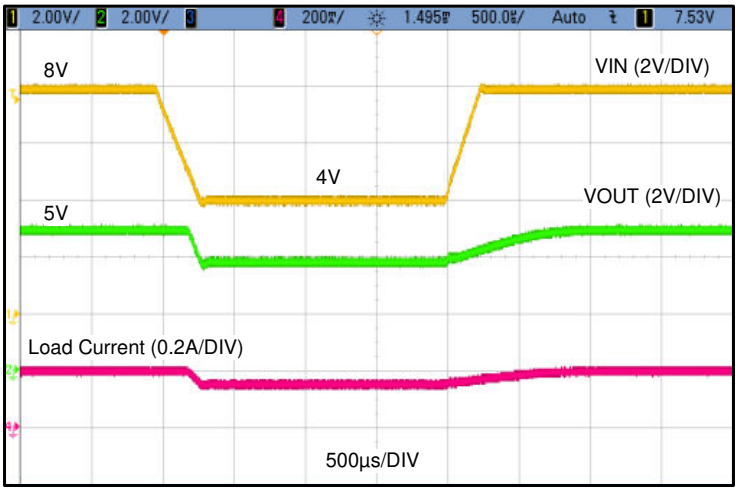


図 8-12. Typical Output Recovery from Dropout from 8 V to 4 V

Whether output voltage falls due to high load or low input voltage, once the condition that causes output to fall below its set point is removed, the output climbs at the same speed as during start-up. shows an example of this behavior.

8.3.9 Current Limit and Short Circuit

The LMR36503-Q1 is protected from overcurrent conditions by cycle-by-cycle current limiting on both high-side and low-side MOSFETs.

High-side MOSFET overcurrent protection is implemented by the typical peak-current mode control scheme. The HS switch current is sensed when the HS is turned on after a short blanking time. The HS switch current is compared to either the minimum of a fixed current set point or the output of the internal error amplifier loop minus the slope compensation every switching cycle. Since the output of the internal error amplifier loop has a maximum value and slope compensation increases with duty cycle, HS current limit decreases with increased duty factor if duty factor is typically above 35%.

When the LS switch is turned on, the current going through it is also sensed and monitored. Like the high-side device, the low-side device has a turnoff commanded by the internal error amplifier loop. In the case of the low-side device, turnoff is prevented if the current exceeds this value, even if the oscillator normally starts a new switching cycle. Also like the high-side device, there is a limit on how high the turnoff current is allowed to be. This is called the low-side current limit, $I_{LS-LIMIT}$ (or I_{L-LS} in 図 8-13). If the LS current limit is exceeded, the LS MOSFET stays on and the HS switch is not to be turned on. The LS switch is turned off once the LS current falls below this limit and the HS switch is turned on again as long as at least one clock period has passed since the last time the HS device has turned on.

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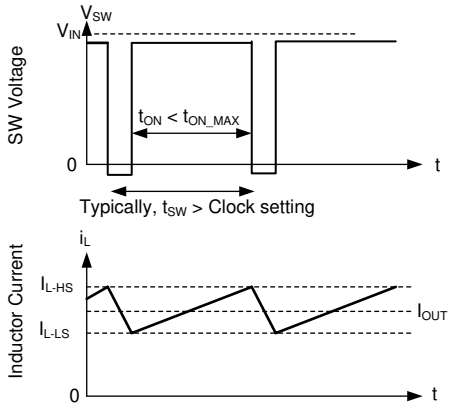


図 8-13. Current Limit Waveforms

Since the current waveform assumes values between I_{SC} (or I_{L-HS} in 図 8-13) and $I_{LS-LIMIT}$, the maximum output current is very close to the average of these two values unless duty factor is very high. Once operating in current limit, hysteretic control is used and current does not increase as output voltage approaches zero.

If duty factor is very high, current ripple must be very low in order to prevent instability. Since current ripple is low, the part is able to deliver full current. The current delivered is very close to $I_{LS-LIMIT}$.

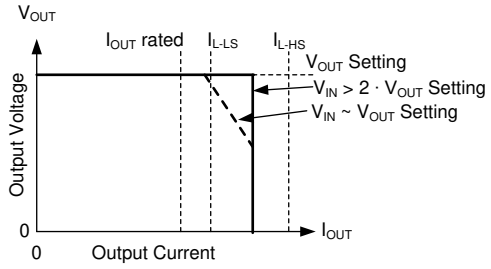


図 8-14. Output Voltage versus Output Current

Under most conditions, current is limited to the average of I_{L-HS} and I_{L-LS}, which is approximately 1.3 times the maximum-rated current. If input voltage is low, current can be limited to approximately I_{L-LS}. Also note that the maximum output current does not exceed the average of I_{L-HS} and I_{L-LS}. Once the overload is removed, the part recovers as though in soft start.

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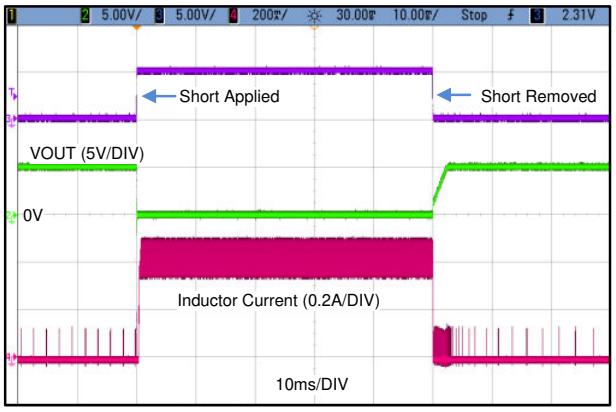


図 8-15. Short Circuit Waveform

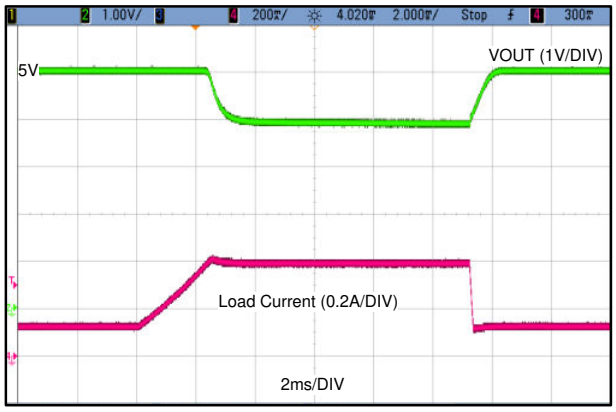


図 8-16. Overload Output Recovery

8.3.10 Thermal Shutdown

Thermal shutdown limits total power dissipation by turning off the internal switches when the device junction temperature exceeds 168°C (typical). Thermal shutdown does not trigger below 158°C (minimum). After thermal shutdown occurs, hysteresis prevents the part from switching until the junction temperature drops to approximately 158°C (typical). When the junction temperature falls below 158°C (typical), the LMR36503-Q1 attempts another soft start.

While the LMR36503-Q1 is shut down due to high junction temperature, power continues to be provided to VCC. To prevent overheating due to a short circuit applied to VCC, the LDO that provides power for VCC has reduced current limit while the part is disabled due to high junction temperature. The LDO only provides a few milliamperes during thermal shutdown.

8.3.11 Input Supply Current

The LMR36503-Q1 is designed to have very low input supply current when regulating light loads. This is achieved by powering much of the internal circuitry from the output. The VOUT/BIAS pin in the fixed-output voltage variants is the input to the LDO that powers the majority of the control circuits. By connecting the VOUT/BIAS input pin to the output node of the regulator, a small amount of current is drawn from the output. This current is reduced at the input by the ratio of V_{OUT} / V_{IN}.

$$I_{Q_VIN} = I_Q + I_{EN} + I_{BIAS} \frac{V_{OUT}}{\eta_{eff} \times V_{IN}} \quad (3)$$

where

- I_{Q_VIN} is the total standby (switching) current consumed by the operating (switching) buck converter when unloaded.
- I_Q is the current drawn from the V_{IN} terminal. Check $I_{Q_13p5_Fixed}$ or $I_{Q_24p0_Fixed}$ in *セクション 7.5* for I_Q.
- I_{EN} is current drawn by the EN terminal. Include this current if EN is connected to VIN. Check I_{LKG-EN} in *セクション 7.5* for I_{EN}.
- I_{BIAS} is bias current drawn by the BIAS input. Check I_{B_13p5} or I_{B_24p0} in *セクション 7.5* for I_{BIAS}.
- η_{eff} is the light-load efficiency of the buck converter with I_{Q_VIN} removed from the input current of the buck converter. η_{eff} = 0.8 is a conservative value that can be used under normal operating conditions. This can be traced back as the I_{SUPPLY} in *セクション 7.7*.

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8.4 Device Functional Modes

8.4.1 Shutdown Mode

The EN pin provides electrical ON and OFF control of the device. When the EN pin voltage is below 0.4 V, both the converter and the internal LDO have no output voltage and the part is in shutdown mode. In shutdown mode, the quiescent current drops to typically 0.5 µA.

8.4.2 Standby Mode

The internal LDO has a lower EN threshold than the output of the converter. When the EN pin voltage is above 1.1 V (maximum) and below the precision enable threshold for the output voltage, the internal LDO regulates the VCC voltage at 3.3 V typical. The precision enable circuitry is ON once VCC is above its UVLO. The internal power MOSFETs of the SW node remain off unless the voltage on EN pin goes above its precision enable threshold. The LMR36503-Q1 also employs UVLO protection. If the VCC voltage is below its UVLO level, the output of the converter is turned off.

8.4.3 Active Mode

The LMR36503-Q1 is in active mode whenever the EN pin is above $V_{EN-VOUT}$, V_{IN} is high enough to satisfy V_{IN_R}, and no other fault conditions are present. The simplest way to enable the operation is to connect the EN pin to V_{IN}, which allows self start-up when the applied input voltage exceeds the minimum V_{IN_R}.

In active mode, depending on the load current, input voltage, and output voltage, the LMR36503-Q1 is in one of five modes:

- Continuous conduction mode (CCM) with fixed switching frequency when load current is above half of the inductor current ripple
- Auto Mode - Light Load Operation: PFM when switching frequency is decreased at very light load
- FPWM Mode - Light Load Operation: Discontinuous conduction mode (DCM) when the load current is lower than half of the inductor current ripple
- Minimum on-time: At high input voltage and low output voltages, the switching frequency is reduced to maintain regulation.
- Dropout mode: When switching frequency is reduced to minimize voltage dropout.

8.4.3.1 CCM Mode

The following operating description of the LMR36503-Q1 refers to the *セクション 8.2* and to the waveforms in 図 8-17. In CCM, the LMR36503-Q1 supplies a regulated output voltage by turning on the internal high-side (HS) and low-side (LS) switches with varying duty cycle (D). During the HS switch on-time, the SW pin voltage, V_{SW}, swings up to approximately V_{IN}, and the inductor current, i_L, increases with a linear slope. The HS switch is turned off by the control logic. During the HS switch off-time, t_{OFF}, the LS switch is turned on. Inductor current discharges through the LS switch, which forces the V_{SW} to swing below ground by the voltage drop across the LS switch. The converter loop adjusts the duty cycle to maintain a constant output voltage. D is defined by the on-time of the HS switch over the switching period:

$$D = T_{ON} / T_{SW} \quad (4)$$

In an ideal buck converter where losses are ignored, D is proportional to the output voltage and inversely proportional to the input voltage:

$$D = V_{OUT} / V_{IN} \quad (5)$$

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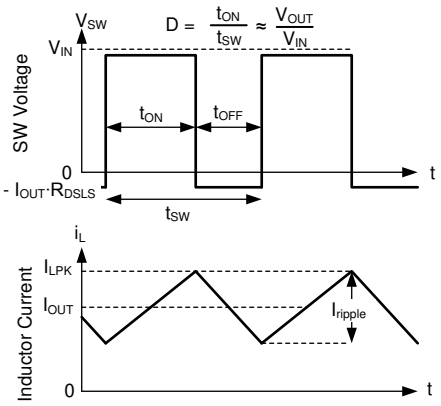


図 8-17. SW Voltage and Inductor Current Waveforms in Continuous Conduction Mode (CCM)

8.4.3.2 Auto Mode - Light Load Operation

The LMR36503-Q1 can have two behaviors while lightly loaded. One behavior, called auto mode operation, allows for seamless transition between normal current mode operation while heavily loaded and highly efficient light load operation. The other behavior, called FPWM Mode, maintains full frequency even when unloaded. Which mode the LMR36503-Q1 operates in depends on which variant from this family is selected. Note that all parts operate in FPWM mode when synchronizing frequency to an external signal.

The light load operation is employed in the LMR36503-Q1 only in the auto mode. The light load operation employs two techniques to improve efficiency:

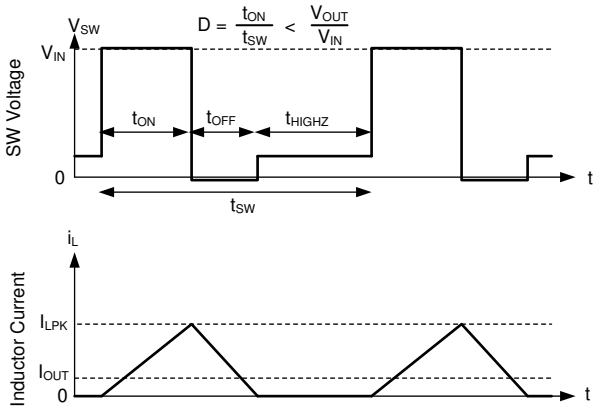
- Diode emulation, which allows DCM operation. See 図 8-18.
- Frequency reduction. See 図 8-19.

Note that while these two features operate together to improve light load efficiency, they operate independent of each other.

8.4.3.2.1 Diode Emulation

Diode emulation prevents reverse current through the inductor which requires a lower frequency needed to regulate given a fixed peak inductor current. Diode emulation also limits ripple current as frequency is reduced. With a fixed peak current, as output current is reduced to zero, frequency must be reduced to near zero to maintain regulation.

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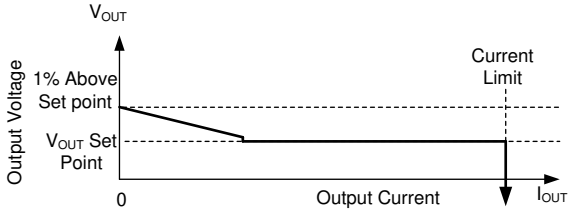
In auto mode, the low-side device is turned off once SW node current is near zero. As a result, once output current is less than half of what inductor ripple would be in CCM, the part operates in DCM which is equivalent to the statement that diode emulation is active.

図 8-18. PFM Operation

The LMR36503-Q1 has a minimum peak inductor current setting (I_{LPK} (see $I_{PEAK-MIN}$ in *セクション 7.5*) while in auto mode. Once current is reduced to a low value with fixed input voltage, on-time is constant. Regulation is then achieved by adjusting frequency. This mode of operation is called PFM mode regulation.

8.4.3.2.2 Frequency Reduction

The LMR36503-Q1 reduces frequency whenever output voltage is high. This function is enabled whenever the internal error amplifier compensation output, COMP, an internal signal, is low and there is an offset between the regulation set point of FB and the voltage applied to FB. The net effect is that there is larger output impedance while lightly loaded in auto mode than in normal operation. Output voltage must be approximately 1% high when the part is completely unloaded.



In auto mode, once output current drops below approximately 1/10th the rated current of the part, output resistance increases so that output voltage is 1% high while the buck is completely unloaded.

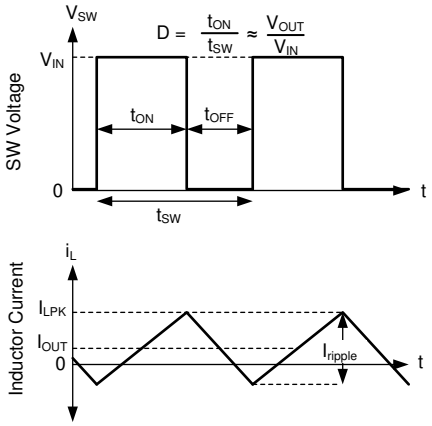
図 8-19. Steady State Output Voltage versus Output Current in Auto Mode

In PFM operation, a small DC positive offset is required on the output voltage to activate the PFM detector. The lower the frequency in PFM, the more DC offset is needed on V_{OUT}. If the DC offset on V_{OUT} is not acceptable, a dummy load at V_{OUT} or FPWM Mode can be used to reduce or eliminate this offset.

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8.4.3.3 FPWM Mode - Light Load Operation

In FPWM Mode, frequency is maintained while lightly loaded. To maintain frequency, a limited reverse current is allowed to flow through the inductor. Reverse current is limited by reverse current limit circuitry, see セクション 7.5 for reverse current limit values.



In FPWM mode, Continuous Conduction (CCM) is possible even if I_{OUT} is less than half of I_{ripple}.

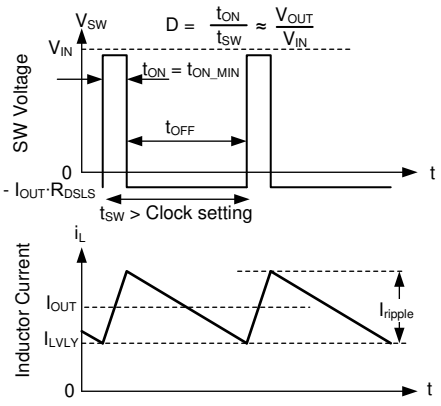
図 8-20. FPWM Mode Operation

For all devices, in FPWM mode, frequency reduction is still available if output voltage is high enough to command minimum on-time even while lightly loaded, allowing good behavior during faults which involve output being pulled up.

8.4.3.4 Minimum On-time (High Input Voltage) Operation

The LMR36503-Q1 continues to regulate output voltage even if the input-to-output voltage ratio requires an on-time less than the minimum on-time of the chip with a given clock setting. This is accomplished using valley current control. At all times, the compensation circuit dictates both a maximum peak inductor current and a maximum valley inductor current. If for any reason, valley current is exceeded, the clock cycle is extended until valley current falls below that determined by the compensation circuit. If the converter is not operating in current limit, the maximum valley current is set above the peak inductor current, preventing valley control from being used unless there is a failure to regulate using peak current only. If the input-to-output voltage ratio is too high, such that the inductor current peak value exceeds the peak command dictated by compensation, the high-side device cannot be turned off quickly enough to regulate output voltage. As a result, the compensation circuit reduces both peak and valley current. Once a low enough current is selected by the compensation circuit, valley current matches that being commanded by the compensation circuit. Under these conditions, the low-side device is kept on and the next clock cycle is prevented from starting until inductor current drops below the desired valley current. Since on-time is fixed at its minimum value, this type of operation resembles that of a device using a Constant On-Time (COT) control scheme; see 図 8-21.

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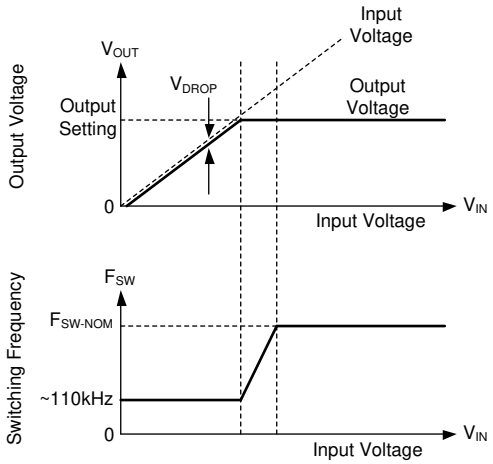


In valley control mode, minimum inductor current is regulated, not peak inductor current.

図 8-21. Valley Current Mode Operation

8.4.3.5 Dropout

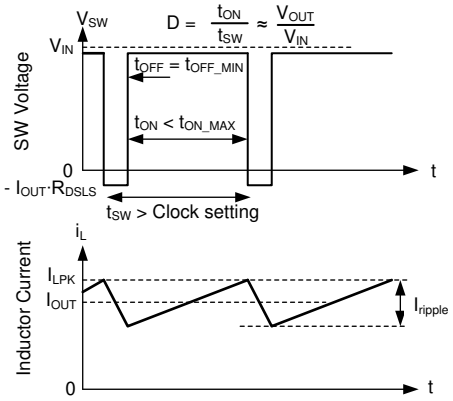
Dropout operation is defined as any input-to-output voltage ratio that requires frequency to drop to achieve the required duty cycle. At a given clock frequency, duty cycle is limited by minimum off-time. Once this limit is reached as shown in 図 8-23 if clock frequency was to be maintained, the output voltage would fall. Instead of allowing the output voltage to drop, the LMR36503-Q1 extends the high side switch on-time past the end of the clock cycle until the needed peak inductor current is achieved. The clock is allowed to start a new cycle once peak inductor current is achieved or once a pre-determined maximum on-time, t_{ON-MAX}, of approximately 9 µs passes. As a result, once the needed duty cycle cannot be achieved at the selected clock frequency due to the existence of a minimum off-time, frequency drops to maintain regulation. As shown in 図 8-22 if input voltage is low enough so that output voltage cannot be regulated even with an on-time of t_{ON-MAX}, output voltage drops to slightly below the input voltage by V_{DROP}. For additional information on recovery from dropout, refer back to 図 8-11.



Output voltage and frequency versus input voltage: If there is little difference between input voltage and output voltage setting, the IC reduces frequency to maintain regulation. If input voltage is too low to provide the desired output voltage at approximately 110 kHz, input voltage tracks output voltage.

図 8-22. Frequency and Output Voltage in Dropout

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Switching waveforms while in dropout. Inductor current takes longer than a normal clock to reach the desired peak value. As a result, frequency drops. This frequency drop is limited by t_{ON-MAX}.

図 8-23. Dropout Waveforms

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9 Application and Implementation

Note

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9.1 Application Information

The LMR36503-Q1 step-down DC-to-DC converter is typically used to convert a higher DC voltage to a lower DC voltage with a maximum output current of 0.3 A. The following design procedure can be used to select components for the LMR36503-Q1.

Note

All of the capacitance values given in the following application information refer to *effective* values unless otherwise stated. The *effective* value is defined as the actual capacitance under DC bias and temperature, not the rated or nameplate values. Use high-quality, low-ESR, ceramic capacitors with an X7R or better dielectric throughout. All high value ceramic capacitors have a large voltage coefficient in addition to normal tolerances and temperature effects. Under DC bias the capacitance drops considerably. Large case sizes and higher voltage ratings are better in this regard. To help mitigate these effects, multiple capacitors can be used in parallel to bring the minimum *effective* capacitance up to the required value. This can also ease the RMS current requirements on a single capacitor. A careful study of bias and temperature variation of any capacitor bank must be made to ensure that the minimum value of *effective* capacitance is provided.

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9.2 Typical Application

図 9-1 shows a typical application circuit for the LMR36503-Q1. This device is designed to function over a wide range of external components and system parameters. However, the internal compensation is optimized for a certain range of external inductance and output capacitance. As a quick-start guide, 表 9-1 provides typical component values for a range of the most common output voltages.

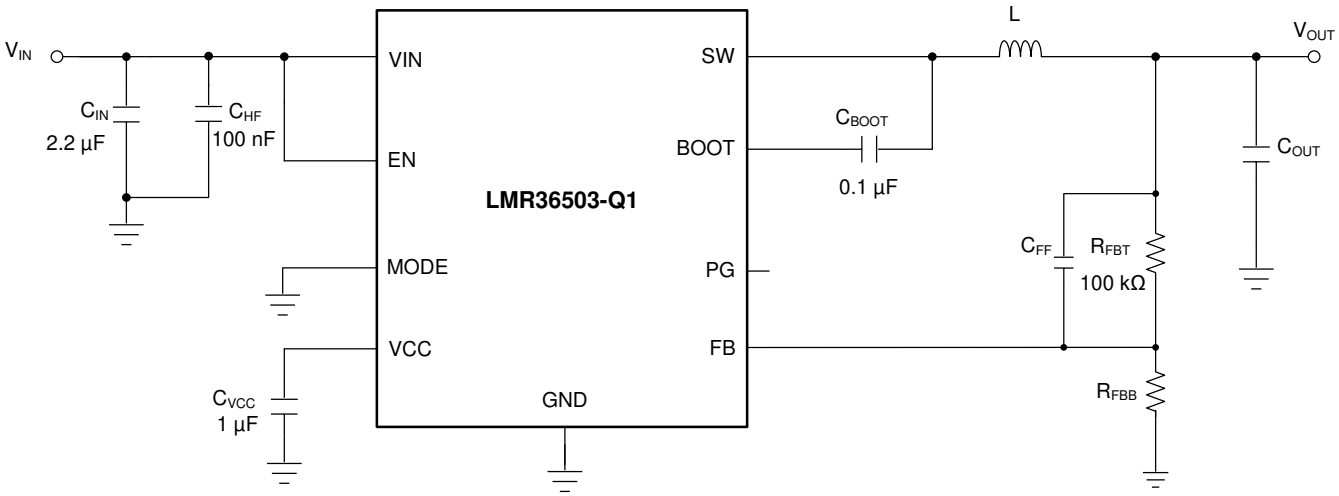


図 9-1. Example Application Circuit

表 9-1. Typical External Component Values(1)

f_{SW} (kHz)	V_{OUT} (V)	L (µH)	NOMINAL C_{OUT} (RATED CAPACITANCE)	MINIMUM C_{OUT} (RATED CAPACITANCE)	R_{FBT} (Ω)	R_{FBB} (Ω)	C_{IN}	C_{BOOT}	C_{VCC}
400	3.3	68	1 x 47 µF	1 x 22 µF	100 k	43.2 k	2.2 µF + 1 × 100 nF	100 nF	1 µF
2200	3.3	10	1 × 10 µF	1 x 10 µF	100 k	43.2 k	2.2 µF + 1 × 100 nF	100 nF	1 µF
400	5	82	1 x 47 µF	1 × 22 µF	100 k	24.9 k	2.2 µF + 1 × 100 nF	100 nF	1 µF
2200	5	15	1 × 10 µF	1 x 10 µF	100 k	24.9 k	2.2 µF + 1 × 100 nF	100 nF	1 µF

(1) Inductor values are calculated based on typical V_{IN} = 13.5 V.

9.2.1 Design Requirements

セクション 9.2.2 provides a detailed design procedure based on 表 9-2.

表 9-2. Detailed Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage	13.5 V (6 V to 60 V)
Output voltage	5 V
Maximum output current	0 A to 0.3 A
Switching frequency	2200 kHz

9.2.2 Detailed Design Procedure

The following design procedure applies to 図 9-1 and 表 9-1.

9.2.2.1 Choosing the Switching Frequency

The choice of switching frequency is a compromise between conversion efficiency and overall solution size. Lower switching frequency implies reduced switching losses and usually results in higher system efficiency. However, higher switching frequency allows the use of smaller inductors and output capacitors, hence, a more compact design. For this example, 2200 kHz is used.

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9.2.2.2 Setting the Output Voltage

For the fixed output voltage versions, pin 8 (VOUT/BIAS) of the device must be connected directly to the output voltage node. This output sensing point is normally located near the top of the output capacitor. If the sensing point is located further away from the output capacitors (that is, remote sensing), then a small 100-nF capacitor can be needed at the sensing point.

9.2.2.2.1 FB for Adjustable Output

In an adjustable output voltage version, pin 8 of the device is FB. The output voltage of LMR36503-Q1 is externally adjustable using an external resistor divider network. The divider network is comprised of R_{FBT} and R_{FBB}, and closes the loop between the output voltage and the converter. The converter regulates the output voltage by holding the voltage on the FB pin equal to the internal reference voltage, V_{REF}. The resistance of the divider is a compromise between excessive noise pickup and excessive loading of the output. Smaller values of resistance reduce noise sensitivity but also reduce the light-load efficiency. The recommended value for R_{FBT} is 100 kΩ with a maximum value of 1 MΩ. Once R_{FBT} is selected, 式 6 is used to select R_{FBB}. V_{REF} is nominally 1 V. See セクション 7.5.

$$R_{FBB} = \frac{R_{FBT}}{\left[\frac{V_{OUT}}{V_{REF}} - 1\right]} \tag{6}$$

For this 5-V example, R_{FBT} = 100 kΩ and R_{FBB} = 24.9 kΩ is chosen.

9.2.2.3 Inductor Selection

The parameters for selecting the inductor are the inductance and saturation current. The inductance is based on the desired peak-to-peak ripple current and is normally chosen to be in the range of 20% to 40% of the maximum output current. Experience shows that the best value for inductor ripple current is 30% of the maximum load current. Note that when selecting the ripple current for applications with much smaller maximum load than the maximum available from the device, use the maximum device current. 式 7 can be used to determine the value of inductance. The constant K is the percentage of inductor current ripple. For this example, choose K = 0.4 and find an inductance of L = 11.9 µH. Select the next standard value of L = 15 µH.

$$L = \frac{(V_{IN} - V_{OUT})}{f_{SW} \cdot K \cdot I_{OUT\,max}} \cdot \frac{V_{OUT}}{V_{IN}} \tag{7}$$

Ideally, the saturation current rating of the inductor is at least as large as the high-side switch current limit, I_{SC} (see セクション 7.5). This ensures that the inductor does not saturate, even during a short circuit on the output. When the inductor core material saturates, the inductance falls to a very low value, causing the inductor current to rise very rapidly. Although the valley current limit, I_{LIMIT}, is designed to reduce the risk of current runaway, a saturated inductor can cause the current to rise to high values very rapidly. This can lead to component damage. Do not allow the inductor to saturate. Inductors with a ferrite core material have very *hard* saturation characteristics, but usually have lower core losses than powdered iron cores. Powered iron cores exhibit a *soft* saturation, allowing some relaxation in the current rating of the inductor. However, they have more core losses at frequencies above about 1 MHz. In any case, the inductor saturation current must not be less than the maximum peak inductor current at full load.

To avoid subharmonic oscillation, the inductance value must not be less than that given in

$$L_{MIN} \geq 2.5 \times \frac{V_{OUT}}{f_{SW}} \tag{8}$$

The maximum inductance is limited by the minimum current ripple for the current mode control to perform correctly. As a rule-of-thumb, the minimum inductor ripple current must be no less than about 10% of the device maximum rated current under nominal conditions.

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9.2.2.4 Output Capacitor Selection

The current mode control scheme of the LMR36503-Q1 devices allows operation over a wide range of output capacitance. The output capacitor bank is usually limited by the load transient requirements and stability rather than the output voltage ripple. Please refer to セクション 9.2 for typical output capacitor value for 3.3-V and 5-V output voltages. Based on this table, for a 5-V output design, you can choose the recommended 1 × 10-µF ceramic output capacitor for this example. For other designs with other output voltages, WEBENCH can be used as a starting point for selecting the value of output capacitor.

In practice, the output capacitor has the most influence on the transient response and loop-phase margin. Load transient testing and bode plots are the best way to validate any given design and must always be completed before the application goes into production. In addition to the required output capacitance, a small ceramic placed on the output can help reduce high-frequency noise. Small-case size ceramic capacitors in the range of 1 nF to 100 nF can be very helpful in reducing spikes on the output caused by inductor and board parasitics.

Limit the maximum value of total output capacitance to about 10 times the design value, or 1000 µF, whichever is smaller. Large values of output capacitance can adversely affect the start-up behavior of the regulator as well as the loop stability. If values larger than noted here must be used, then a careful study of start-up at full load and loop stability must be performed.

9.2.2.5 Input Capacitor Selection

The ceramic input capacitors provide a low impedance source to the regulator in addition to supplying the ripple current and isolating switching noise from other circuits. A minimum ceramic capacitance of 2.2 µF is required on the input of the LMR36503-Q1. This must be rated for at least the maximum input voltage that the application requires, preferably twice the maximum input voltage. This capacitance can be increased to help reduce input voltage ripple and maintain the input voltage during load transients. In addition, a small case size 100-nF ceramic capacitor must be used at the input, as close a possible to the regulator. This provides a high frequency bypass for the control circuits internal to the device. For this example a 2.2-µF, 100-V, X7R (or better) ceramic capacitor is chosen. The 100 nF must also be rated at 100 V with an X7R dielectric.

It is often desirable to use an electrolytic capacitor on the input in parallel with the ceramics. This is especially true if long leads or traces are used to connect the input supply to the regulator. The moderate ESR of this capacitor can help damp any ringing on the input supply caused by the long power leads. The use of this additional capacitor also helps with voltage dips caused by input supplies with unusually high impedance.

Most of the input switching current passes through the ceramic input capacitor or capacitors. The approximate RMS value of this current can be calculated from 式 9 and must be checked against the manufacturers' maximum ratings.

$$I_{RMS} \cong \frac{I_{OUT}}{2} \tag{9}$$

9.2.2.6 C_{BOOT}

The LMR36503-Q1 requires a bootstrap capacitor connected between the BOOT pin and the SW pin. This capacitor stores energy that is used to supply the gate drivers for the power MOSFETs. A high-quality ceramic capacitor of 100 nF and at least 16 V is required.

9.2.2.7 VCC

The VCC pin is the output of the internal LDO used to supply the control circuits of the regulator. This output requires a 1-µF, 16-V ceramic capacitor connected from VCC to GND for proper operation. In general, this output must not be loaded with any external circuitry. However, this output can be used to supply the pullup for the power-good function (see セクション 8.3.4). A value in the range of 10 kΩ to 100 kΩ is a good choice in this case. The nominal output voltage on VCC is 3.2 V; see セクション 7.5 for limits.

9.2.2.8 C_{FF} Selection

In some cases, a feedforward capacitor can be used across R_{FBT} to improve the load transient response or improve the loop-phase margin. This is especially true when values of R_{FBT} > 100 kΩ are used. Large values of

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R_{FBT}, in combination with the parasitic capacitance at the FB pin, can create a small signal pole that interferes with the loop stability. A C_{FF} can help mitigate this effect. Use 式 10 to estimate the value of C_{FF}. The value found with 式 10 is a starting point; use lower values to determine if any advantage is gained by the use of a C_{FF} capacitor. The *Optimizing Transient Response of Internally Compensated DC-DC Converters with Feedforward Capacitor Application Report* is helpful when experimenting with a feedforward capacitor.

$$C_{FF} < \frac{V_{OUT} \cdot C_{OUT}}{120 \cdot R_{FBT} \cdot \sqrt{\frac{V_{REF}}{V_{OUT}}}} \tag{10}$$

9.2.2.8.1 External UVLO

In some cases, an input UVLO level different than that provided internal to the device is needed. This can be accomplished by using the circuit shown in 図 9-2. The input voltage at which the device turns on is designated as V_{ON} while the turnoff voltage is V_{OFF}. First, a value for R_{ENB} is chosen in the range of 10 kΩ to 100 kΩ, then 式 11 is used to calculate R_{ENT} and V_{OFF}.

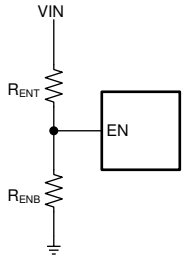


図 9-2. Setup for External UVLO Application

$$R_{ENT} = \left(\frac{V_{ON}}{V_{EN-H}} - 1 \right) \cdot R_{ENB}$$

$$V_{OFF} = V_{ON} \cdot \left(1 - \frac{V_{EN-HYS}}{V_{EN}} \right) \tag{11}$$

where

- V_{ON} is the V_{IN} turnon voltage.
- V_{OFF} is the V_{IN} turnoff voltage.

9.2.2.9 Maximum Ambient Temperature

As with any power conversion device, the LMR36503-Q1 dissipates internal power while operating. The effect of this power dissipation is to raise the internal temperature of the converter above ambient. The internal die temperature (T_J) is a function of the ambient temperature, the power loss, and the effective thermal resistance, $R_{\theta JA}$, of the device and PCB combination. The maximum junction temperature for the LMR36503-Q1 must be limited to 150°C. This establishes a limit on the maximum device power dissipation and, therefore, the load current. 式 12 shows the relationships between the important parameters. It is easy to see that larger ambient temperatures (T_A) and larger values of $R_{\theta JA}$ reduce the maximum available output current. The converter efficiency can be estimated by using the curves provided in this data sheet. If the desired operating conditions cannot be found in one of the curves, interpolation can be used to estimate the efficiency. Alternatively, the EVM can be adjusted to match the desired application requirements and the efficiency can be measured directly. The correct value of $R_{\theta JA}$ is more difficult to estimate. As stated in the *Semiconductor and IC Package Thermal Metrics Application Report*, the values given in *セクション 7.4* are not valid for design purposes and must not be used to estimate the thermal performance of the application. The values reported in that table were measured under a specific set of conditions that are rarely obtained in an actual application.

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$$I_{OUT}|_{MAX} = \frac{(T_J - T_A)}{R_{\theta JA}} \cdot \frac{\eta}{(1-\eta)} \cdot \frac{1}{V_{OUT}} \quad (12)$$

where

- η = efficiency

The effective $R_{\theta JA}$ is a critical parameter and depends on many factors such as the following:

- Power dissipation
- Air temperature/flow
- PCB area
- Copper heat-sink area
- Number of thermal vias under the package
- Adjacent component placement

A typical example of $R_{\theta JA}$ versus copper board area can be found in 図 9-3. The copper area given in the graph is for each layer. For a 4-layer PCB design, the top and bottom layers are 2-oz. copper each, while the inner layers are 1 oz. For a 2-layer PCB design, the top and bottom layers are 2-oz. copper each. Note that the data given in these graphs are for illustration purposes only, and the actual performance in any given application depends on all of the factors mentioned above.

Using the value of $R_{\theta JA}$ from 図 9-3 for a given PCB copper area and Ψ_{JT} from *セクション 7.4*, one can approximate the junction temperature of the IC for a given operating condition using 式 13

$$T_J \approx T_A + R_{\theta JA} \times \text{IC Power Loss} \quad (13)$$

where

- T_J = IC Junction Temperature (°C)
- T_A = Ambient Temperature (°C)
- $R_{\theta JA}$ = Thermal Resistance (°C/W)
- IC Power Loss = Power loss for the IC (W)

The IC Power loss mentioned above is the overall power loss minus the loss that comes from the inductor DC Resistance. The overall power loss can be approximated from the efficiency curves in the *セクション 9.2.3* or by using WEBENCH for a specific operating condition and temperature.

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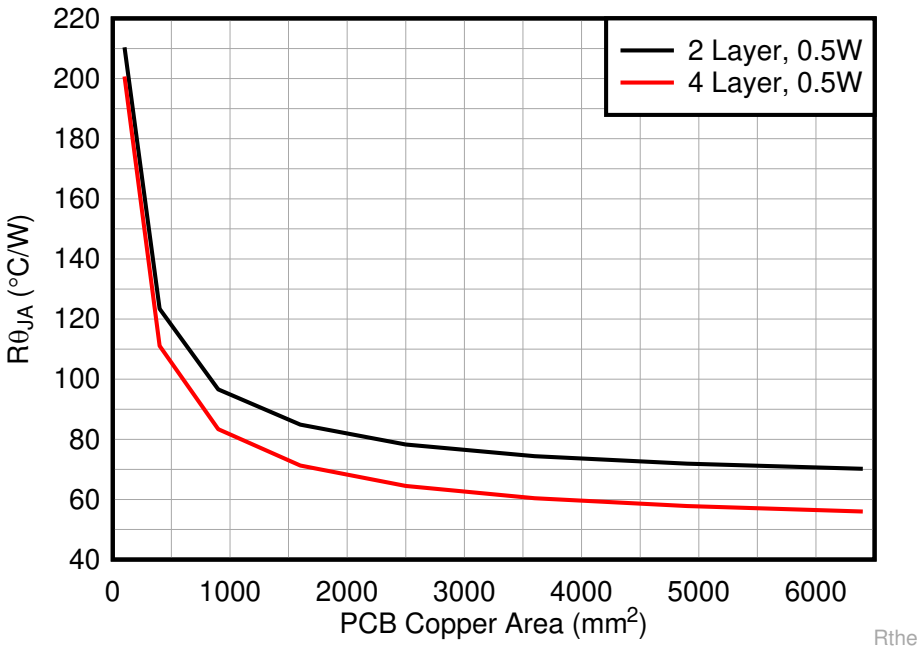


図 9-3. $R_{\theta JA}$ versus PCB Copper Area for the VQFN (RPE) Package

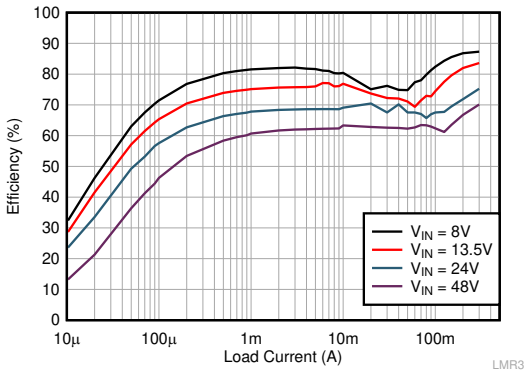
Use the following resources as guides to optimal thermal PCB design and estimating $R_{\theta JA}$ for a given application environment:

- *Thermal Design by Insight not Hindsight Application Report*
- *A Guide to Board Layout for Best Thermal Resistance for Exposed Pad Packages Application Report*
- *Semiconductor and IC Package Thermal Metrics Application Report*
- *Thermal Design Made Simple with LM43603 and LM43602 Application Report*
- *PowerPAD™ Thermally Enhanced Package Application Report*
- *PowerPAD™ Made Easy Application Report*
- *Using New Thermal Metrics Application Report*
- *PCB Thermal Calculator*

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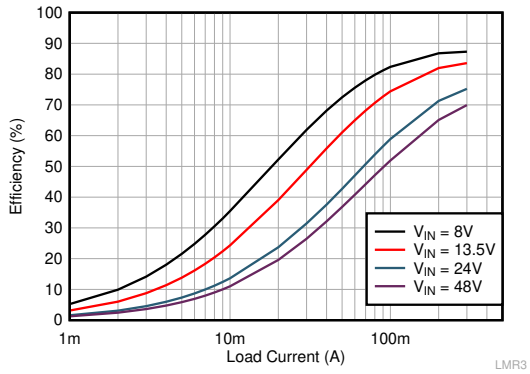
9.2.3 Application Curves

Unless otherwise specified the following conditions apply: V_{IN} = 13.5V, T_A = 25°C. 図 9-25 shows the circuit with the appropriate BOM in 表 9-3



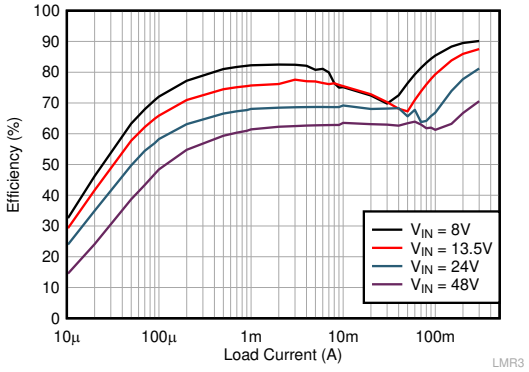
LMR36503MSC3 V_{OUT} = 3.3 V Fixed 2.2 MHz (AUTO)

図 9-4. Efficiency



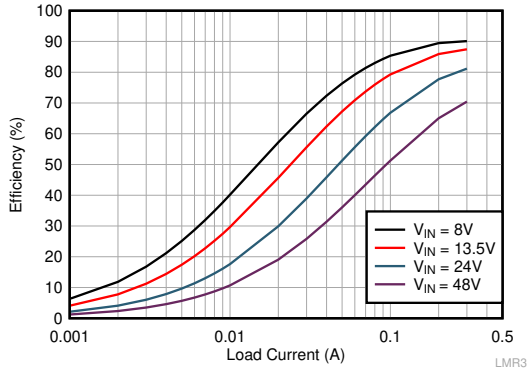
LMR36503MSC3 V_{OUT} = 3.3 V Fixed 2.2 MHz (FPWM)

図 9-5. Efficiency



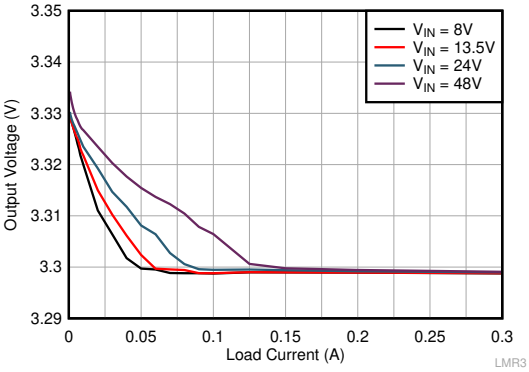
LMR36503MSC5 V_{OUT} = 5 V Fixed 2.2 MHz (AUTO)

図 9-6. Efficiency



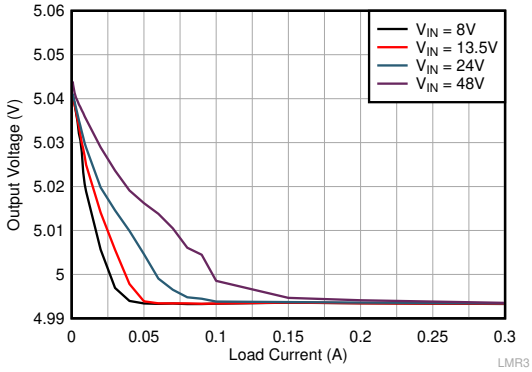
LMR36503MSC5 V_{OUT} = 5 V Fixed 2.2 MHz (FPWM)

図 9-7. Efficiency



LMR36503MSC3 V_{OUT} = 3.3 V Fixed 2.2 MHz (AUTO)

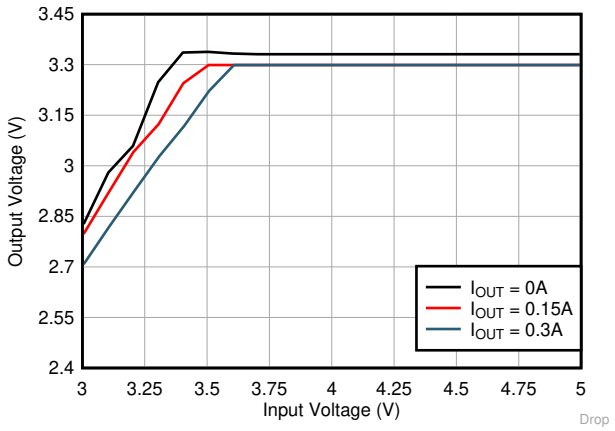
図 9-8. Line and Load Regulation



LMR36503MSC5 V_{OUT} = 5 V Fixed 2.2 MHz (AUTO)

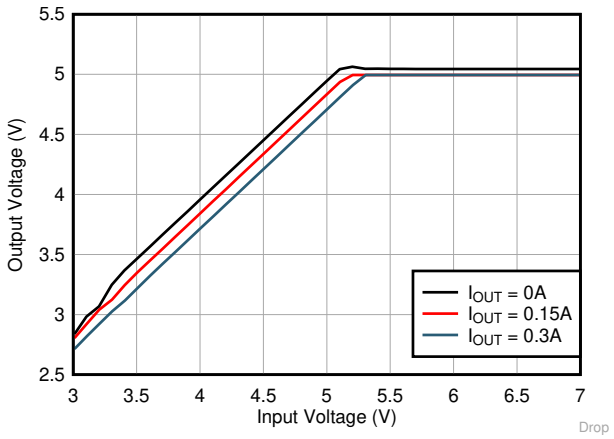
図 9-9. Line and Load Regulation

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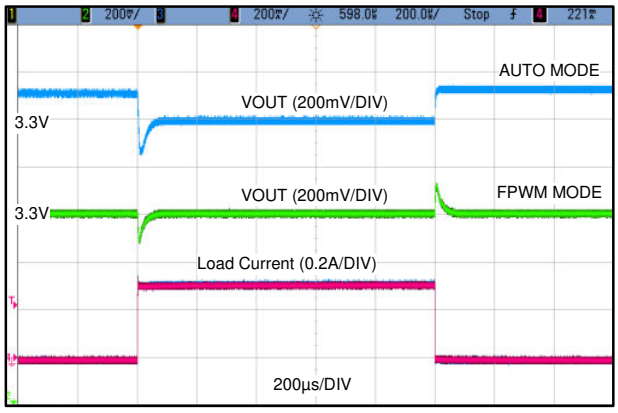
LMR36503MSC3 V_{OUT} = 3.3 V Fixed 2.2 MHz (AUTO)

図 9-10. Dropout



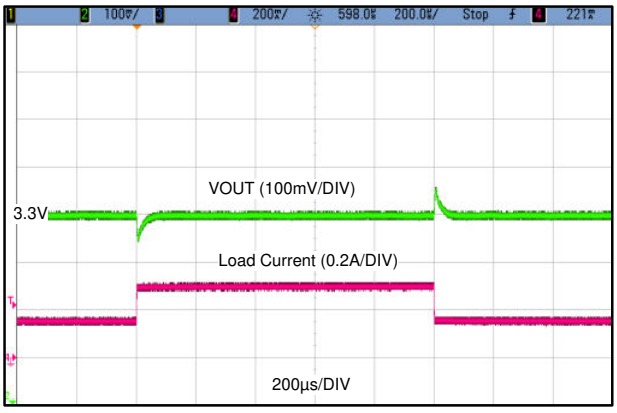
LMR36503MSC5 V_{OUT} = 5 V Fixed 2.2 MHz (AUTO)

図 9-11. Dropout



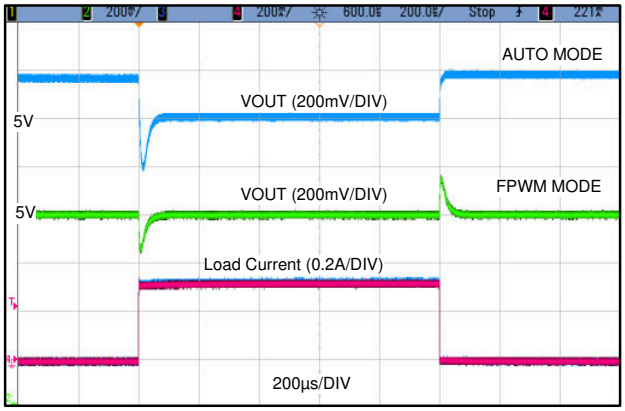
LMR36503MSC3 V_{OUT} = 3.3 V Fixed 2.2 MHz
0 A to 0.3 A,1 A/µs

図 9-12. Load Transient



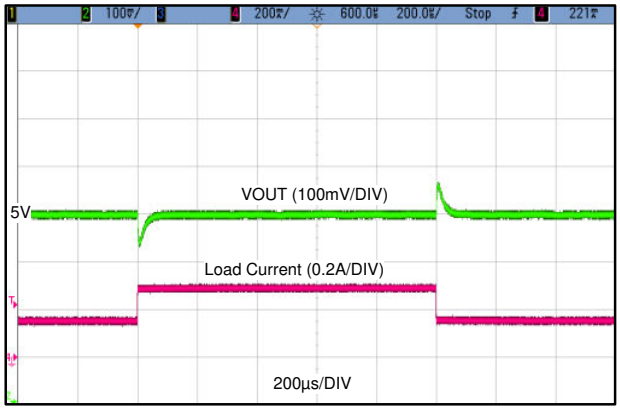
LMR36503MSC3 V_{OUT} = 3.3 V Fixed 2.2 MHz
0.15 A to 0.3 A,1 A/µs

図 9-13. Load Transient



LMR36503MSC5 V_{OUT} = 5 V Fixed 2.2 MHz
0 A to 0.3 A,1 A/µs

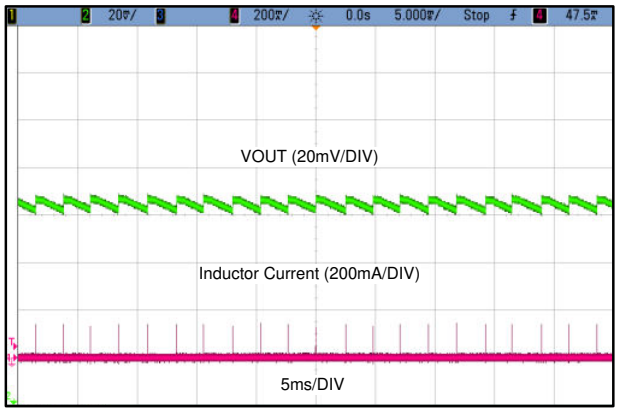
図 9-14. Load Transient



LMR36503MSC5 V_{OUT} = 5 V Fixed 2.2 MHz
0.15 A to 0.3 A,1 A/µs

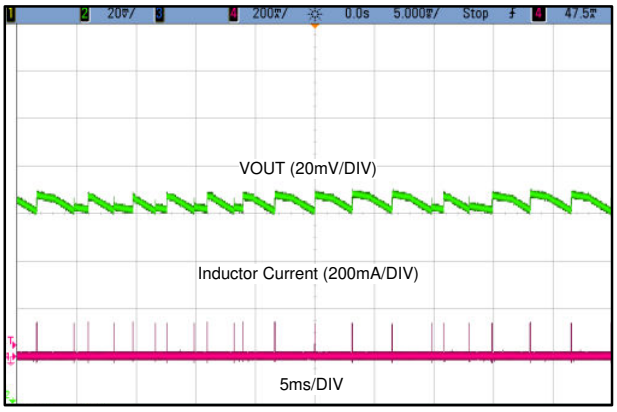
図 9-15. Load Transient

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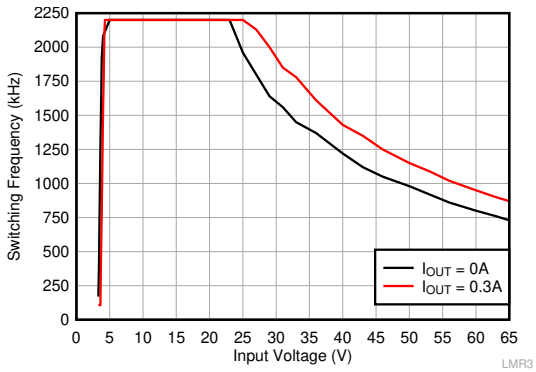
LMR36503MSC3 V_{OUT} = 3.3 V Fixed No Load

図 9-16. Output Ripple



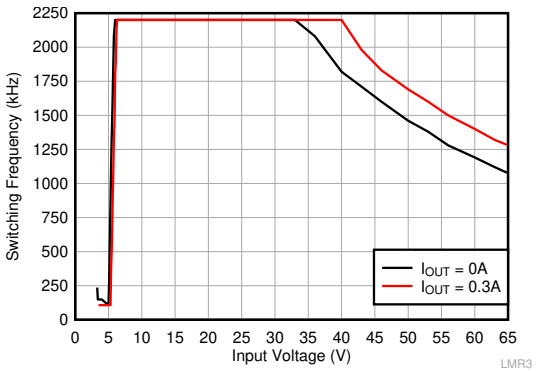
LMR36503MSC5 V_{OUT} = 5 V Fixed No Load

図 9-17. Output Ripple



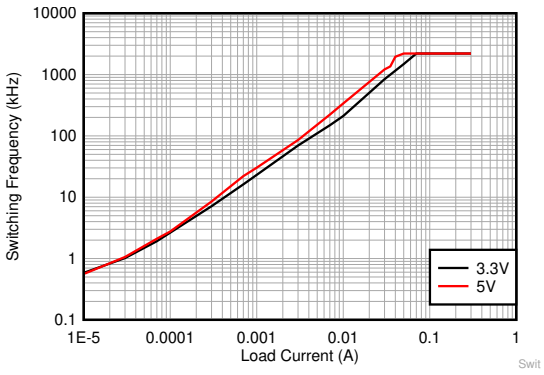
LMR36503MSC3 V_{OUT} = 3.3 V Fixed 2200 kHz FPWM

図 9-18. Switching Frequency over Input Voltage



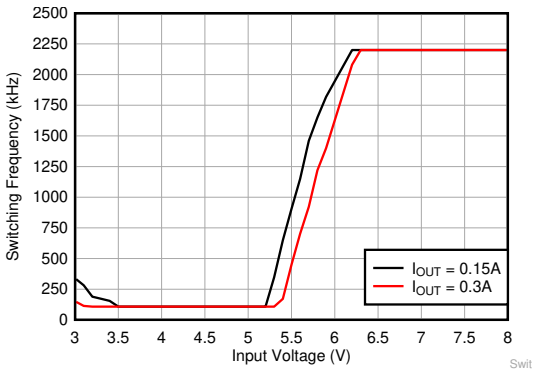
LMR36503MSC5 V_{OUT} = 5 V Fixed 2200 kHz FPWM

図 9-19. Switching Frequency over Input Voltage



LMR36503MSC3 V_{OUT} = 3.3 V Fixed V_{IN} = 13.5 V
LMR36503MSC5 V_{OUT} = 5 V Fixed AUTO

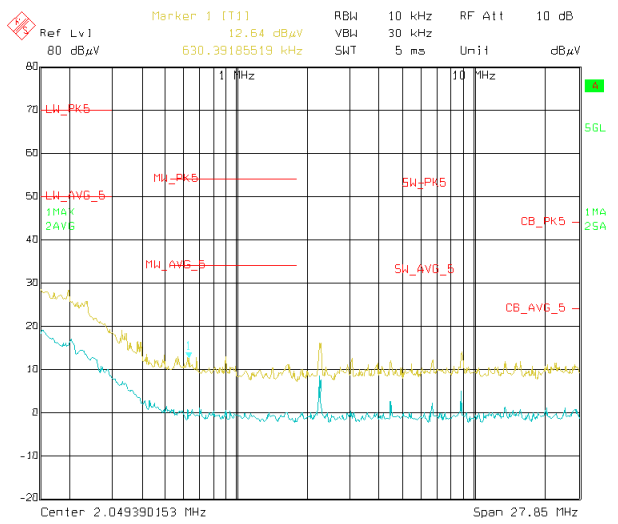
図 9-20. Switching Frequency over Load Current



LMR36503MSC5 V_{OUT} = 5 V Fixed AUTO

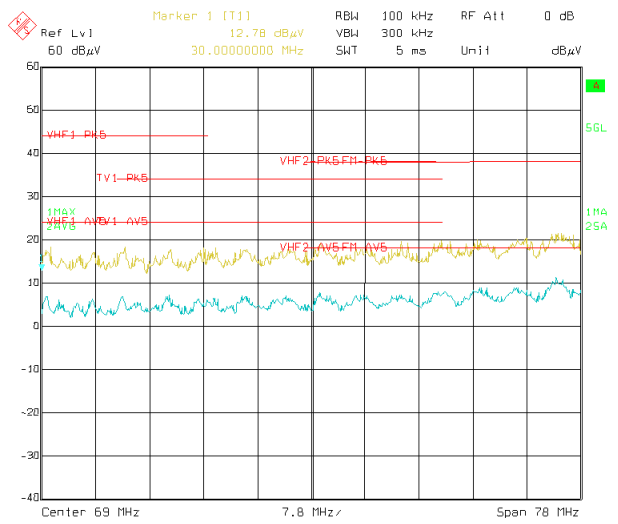
図 9-21. Switching Frequency during Dropout

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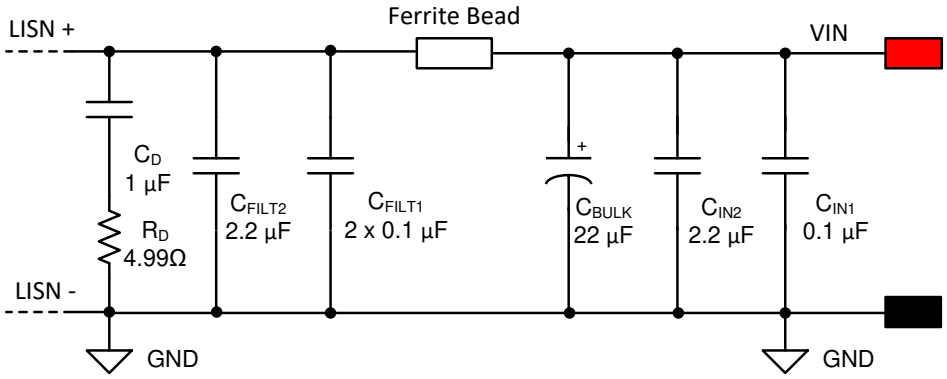
V_{IN} = 13.5 V V_{OUT} = 5 V Fsw = 2.2 MHz
Load = 0.3 A

図 9-22. Typical CISPR 25 Conducted EMI 150kHz - 30MHz Yellow: Peak Detect, Blue = Average Detect



V_{IN} = 13.5 V V_{OUT} = 5 V Fsw = 2.2 MHz
Load = 0.3 A

図 9-23. Typical CISPR 25 Conducted EMI 30MHz - 108MHz Yellow: Peak Detect, Blue = Average Detect



Ferrite Bead Part Number:
FBMH3225HM601NT

図 9-24. Typical Input EMI Filter for 2.2 MHz

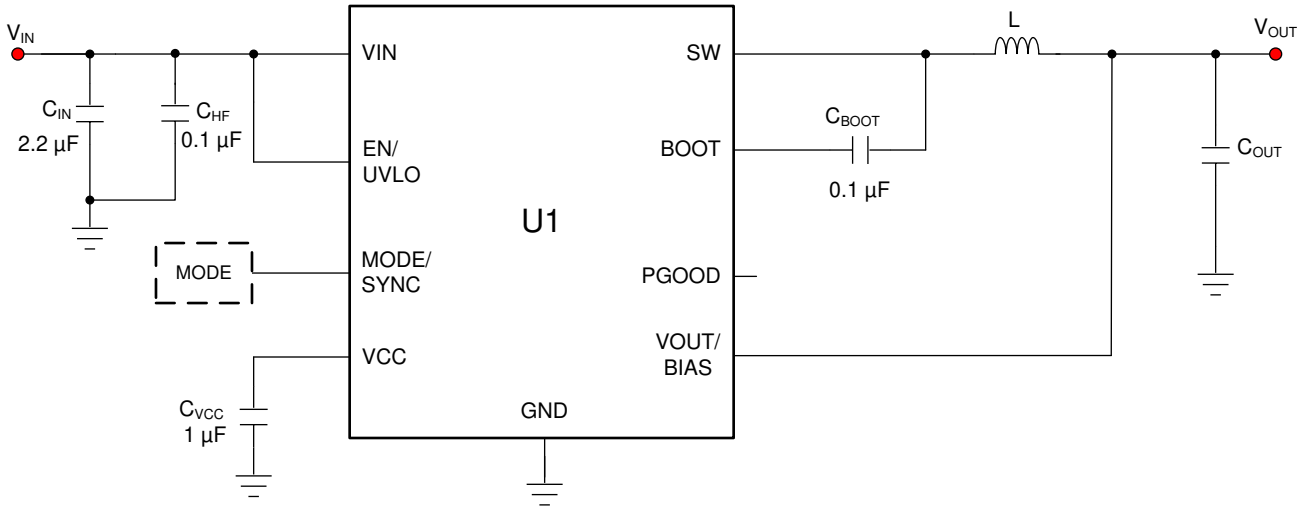


図 9-25. Schematic for Typical Application Curves

表 9-3. BOM for Typical Application Curves

U1	f_{SW}	V_{OUT}	L	NOMINAL C_{OUT} (RATED CAPACITANCE)
LMR36503MSC3RPERQ1	2200 kHz	3.3 V	15 µH. 260 mΩ	1 × 10 µF
LMR36503MSC5RPERQ1	2200 kHz	5 V	15 µH. 260 mΩ	1 × 10 µF

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9.3 What to Do and What Not to Do

- Do not exceed the *Absolute Maximum Ratings*.
- Do not exceed the *Recommended Operating Conditions*.
- Do not exceed the *ESD Ratings*.
- Do not allow the EN input to float.
- Do not allow the output voltage to exceed the input voltage, nor go below ground.
- Follow all the guidelines and suggestions found in this data sheet before committing the design to production. TI application engineers are ready to help critique your design and PCB layout to help make your project a success.

10 Power Supply Recommendations

The characteristics of the input supply must be compatible with セクション 7 found in this data sheet. In addition, the input supply must be capable of delivering the required input current to the loaded regulator. The average input current can be estimated with 式 14.

$$I_{IN} = \frac{V_{OUT} \cdot I_{OUT}}{V_{IN} \cdot \eta} \tag{14}$$

where

- η is the efficiency

If the regulator is connected to the input supply through long wires or PCB traces, special care is required to achieve good performance. The parasitic inductance and resistance of the input cables can have an adverse effect on the operation of the regulator. The parasitic inductance, in combination with the low-ESR, ceramic input capacitors, can form an underdamped resonant circuit, resulting in overvoltage transients at the input to the regulator. The parasitic resistance can cause the voltage at the VIN pin to dip whenever a load transient is applied to the output. If the application is operating close to the minimum input voltage, this dip can cause the regulator to momentarily shut down and reset. The best way to solve these kind of issues is to limit the distance from the input supply to the regulator or plan to use an aluminum or tantalum input capacitor in parallel with the ceramics. The moderate ESR of these types of capacitors help dampen the input resonant circuit and reduce any overshoots. A value in the range of 20 µF to 100 µF is usually sufficient to provide input damping and help to hold the input voltage steady during large load transients.

Sometimes, for other system considerations, an input filter is used in front of the regulator. This can lead to instability, as well as some of the effects mentioned above, unless it is designed carefully. The *AN-2162 Simple Success With Conducted EMI From DC/DC Converters User's Guide* provides helpful suggestions when designing an input filter for any switching regulator.

In some cases, a transient voltage suppressor (TVS) is used on the input of regulators. One class of this device has a *snap-back* characteristic (thyristor type). The use of a device with this type of characteristic is not recommended. When the TVS fires, the clamping voltage falls to a very low value. If this voltage is less than the output voltage of the regulator, the output capacitors discharge through the device back to the input. This uncontrolled current flow can damage the device.

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11 Layout

11.1 Layout Guidelines

The PCB layout of any DC/DC converter is critical to the optimal performance of the design. Poor PCB layout can disrupt the operation of an otherwise good schematic design. Even if the converter regulates correctly, bad PCB layout can mean the difference between a robust design and one that cannot be mass produced. Furthermore, to a great extent, the EMI performance of the regulator is dependent on the PCB layout. In a buck converter, the most critical PCB feature is the loop formed by the input capacitor or capacitors and power ground, as shown in 図 11-1. This loop carries large transient currents that can cause large transient voltages when reacting with the trace inductance. These unwanted transient voltages disrupt the proper operation of the converter. Because of this, the traces in this loop must be wide and short, and the loop area as small as possible to reduce the parasitic inductance. 図 11-2 shows a recommended layout for the critical components of the LMR36503-Q1.

1. *Place the input capacitors as close as possible to the VIN and GND terminals.*
2. *Place bypass capacitor for VCC close to the VCC pin.* This capacitor must be placed close to the device and routed with short, wide traces to the VCC and GND pins.
3. *Use wide traces for the C_{BOOT} capacitor.* Place C_{BOOT} close to the device with short/wide traces to the BOOT and SW pins. Route the SW pin to the N/C pin and used to connect the BOOT capacitor to SW.
4. *Place the feedback divider as close as possible to the FB pin of the device.* Place R_{FBB}, R_{FBT}, and C_{FF}, if used, physically close to the device. The connections to FB and GND must be short and close to those pins on the device. The connection to V_{OUT} can be somewhat longer. However, the latter trace must not be routed near any noise source (such as the SW node) that can capacitively couple into the feedback path of the regulator.
5. *Use at least one ground plane in one of the middle layers.* This plane acts as a noise shield and as a heat dissipation path.
6. *Provide wide paths for VIN, VOUT, and GND.* Making these paths as wide and direct as possible reduces any voltage drops on the input or output paths of the converter and maximizes efficiency.
7. *Provide enough PCB area for proper heat-sinking.* As stated in *セクション 9.2.2.9*, enough copper area must be used to ensure a low $R_{\theta JA}$, commensurate with the maximum load current and ambient temperature. The top and bottom PCB layers must be made with two ounce copper and no less than one ounce. If the PCB design uses multiple copper layers (recommended), these thermal vias can also be connected to the inner layer heat-spreading ground planes.
8. *Keep switch area small.* Keep the copper area connecting the SW pin to the inductor as short and wide as possible. At the same time, the total area of this node must be minimized to help reduce radiated EMI.

See the following PCB layout resources for additional important guidelines:

- *Layout Guidelines for Switching Power Supplies Application Report*
- *Simple Switcher PCB Layout Guidelines Application Report*
- *Construction Your Power Supply- Layout Considerations Seminar*
- *Low Radiated EMI Layout Made Simple with LM4360x and LM4600x Application Report*

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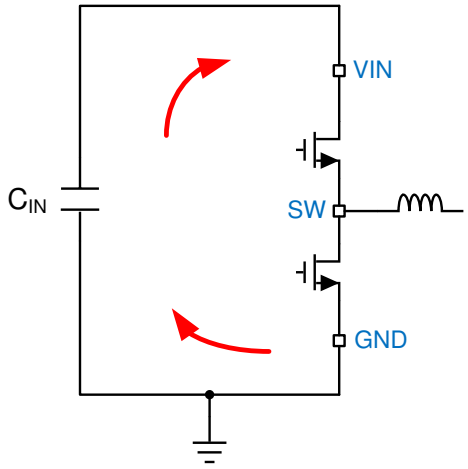


図 11-1. Current Loops with Fast Edges

11.1.1 Ground and Thermal Considerations

As previously mentioned, TI recommends using one of the middle layers as a solid ground plane. A ground plane provides shielding for sensitive circuits and traces as well as a quiet reference potential for the control circuitry. Connect the GND pin to the ground planes using vias next to the bypass capacitors. The GND trace, as well as the VIN and SW traces, must be constrained to one side of the ground planes. The other side of the ground plane contains much less noise; use for sensitive routes.

TI recommends providing adequate device heat-sinking by having enough copper near the GND pin. See 図 11-2 for example layout. Use as much copper as possible, for system ground plane, on the top and bottom layers for the best heat dissipation. Use a four-layer board with the copper thickness for the four layers, starting from the top as: 2 oz / 1 oz / 1 oz / 2 oz. A four-layer board with enough copper thickness, and proper layout, provides low current conduction impedance, proper shielding and lower thermal resistance.

11.2 Layout Example

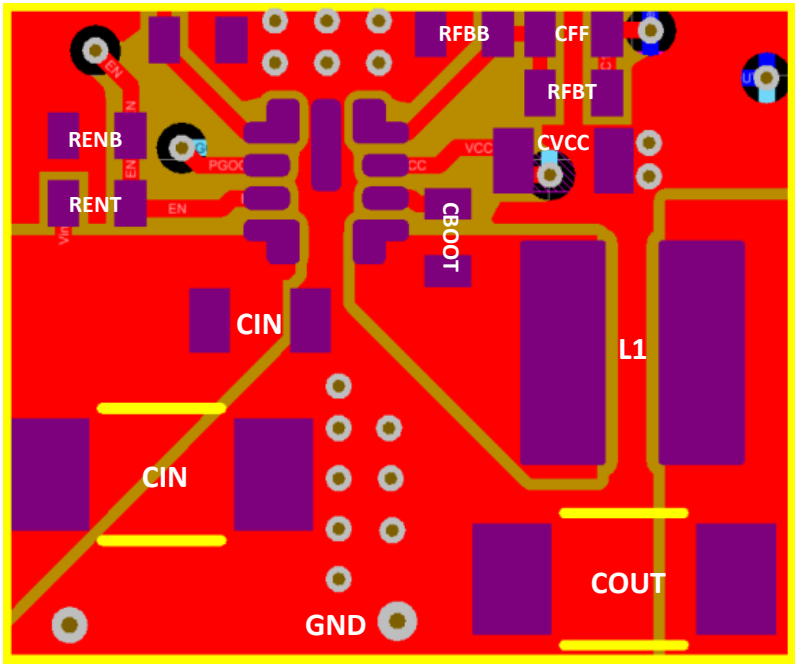


図 11-2. Example Layout

12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *Thermal Design by Insight not Hindsight Application Report*
- Texas Instruments, *A Guide to Board Layout for Best Thermal Resistance for Exposed Pad Packages Application Report*
- Texas Instruments, *Semiconductor and IC Package Thermal Metrics Application Report*
- Texas Instruments, *Thermal Design Made Simple with LM43603 and LM43602 Application Report*
- Texas Instruments, *PowerPAD™ Thermally Enhanced Package Application Report*
- Texas Instruments, *PowerPAD™ Made Easy Application Report*
- Texas Instruments, *Using New Thermal Metrics Application Report*
- Texas Instruments, *Layout Guidelines for Switching Power Supplies Application Report*
- Texas Instruments, *Simple Switcher PCB Layout Guidelines Application Report*
- Texas Instruments, *Construction Your Power Supply- Layout Considerations Seminar*
- Texas Instruments, *Low Radiated EMI Layout Made Simple with LM4360x and LM4600x Application Report*

12.2 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、ti.com のデバイス製品フォルダを開いてください。*「更新の通知を受け取る」をクリック*して登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

12.3 サポート・リソース

TI E2E™ サポート・フォーラムは、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計で必要な支援を迅速に得ることができます。

リンクされているコンテンツは、該当する貢献者により、現状のまま提供されるものです。これらは TI の仕様を構成するものではなく、必ずしも TI の見解を反映したものではありません。TI の使用条件を参照してください。

12.4 Trademarks

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PowerPAD™ and TI E2E™ are trademarks of Texas Instruments.
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12.5 静電気放電に関する注意事項



この IC は、ESD によって破損する可能性があります。テキサス・インスツルメンツは、IC を取り扱う際には常に適切な注意を払うことを推奨します。正しい ESD 対策をとらないと、デバイスを破損するおそれがあります。

ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

12.6 用語集

TI 用語集　この用語集には、用語や略語の一覧および定義が記載されています。

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13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LMR36503MSC3RPERQ1	Active	Production	VQFN-HR (RPE) | 9	3000 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 150	MCGQ
LMR36503MSC3RPERQ1.A	Active	Production	VQFN-HR (RPE) | 9	3000 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 150	MCGQ
LMR36503MSC5RPERQ1	Active	Production	VQFN-HR (RPE) | 9	3000 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 150	MCFQ
LMR36503MSC5RPERQ1.A	Active	Production	VQFN-HR (RPE) | 9	3000 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 150	MCFQ
LMR36503MSCQRPERQ1	Active	Production	VQFN-HR (RPE) | 9	3000 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 150	MCEQ
LMR36503MSCQRPERQ1.A	Active	Production	VQFN-HR (RPE) | 9	3000 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 150	MCEQ
LMR36503RS3QRPERQ1	Active	Production	VQFN-HR (RPE) | 9	3000 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 150	MCHQ
LMR36503RS3QRPERQ1.A	Active	Production	VQFN-HR (RPE) | 9	3000 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 150	MCHQ
LMR36503RS5QRPERQ1	Active	Production	VQFN-HR (RPE) | 9	3000 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 150	MCIQ
LMR36503RS5QRPERQ1.A	Active	Production	VQFN-HR (RPE) | 9	3000 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 150	MCIQ

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF LMR36503-Q1 :

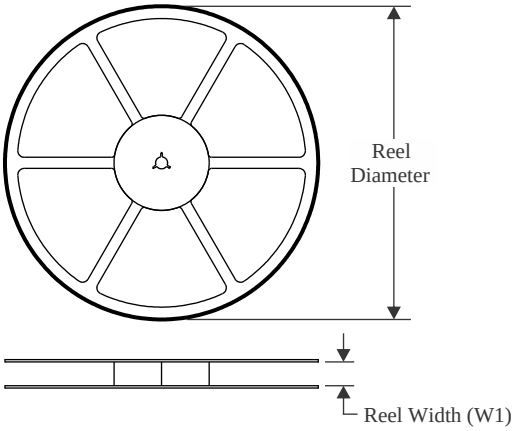
- Catalog : LMR36503

NOTE: Qualified Version Definitions:

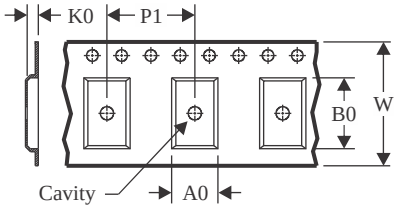
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

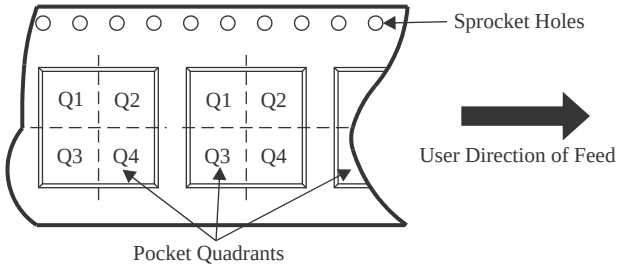


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

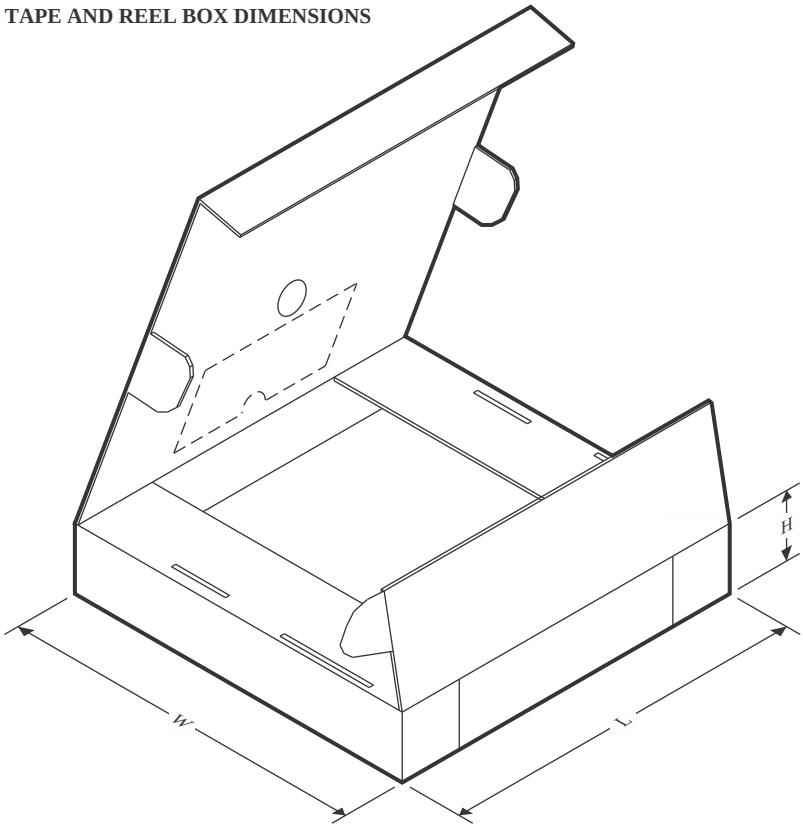
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMR36503MSC3RPERQ1	VQFN-HR	RPE	9	3000	180.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
LMR36503MSC5RPERQ1	VQFN-HR	RPE	9	3000	180.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
LMR36503MSCQRPERQ1	VQFN-HR	RPE	9	3000	180.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
LMR36503RS3QRPERQ1	VQFN-HR	RPE	9	3000	180.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
LMR36503RS5QRPERQ1	VQFN-HR	RPE	9	3000	180.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMR36503MSC3RPERQ1	VQFN-HR	RPE	9	3000	213.0	191.0	35.0
LMR36503MSC5RPERQ1	VQFN-HR	RPE	9	3000	213.0	191.0	35.0
LMR36503MSCQRPERQ1	VQFN-HR	RPE	9	3000	213.0	191.0	35.0
LMR36503RS3QRPERQ1	VQFN-HR	RPE	9	3000	213.0	191.0	35.0
LMR36503RS5QRPERQ1	VQFN-HR	RPE	9	3000	213.0	191.0	35.0

GENERIC PACKAGE VIEW

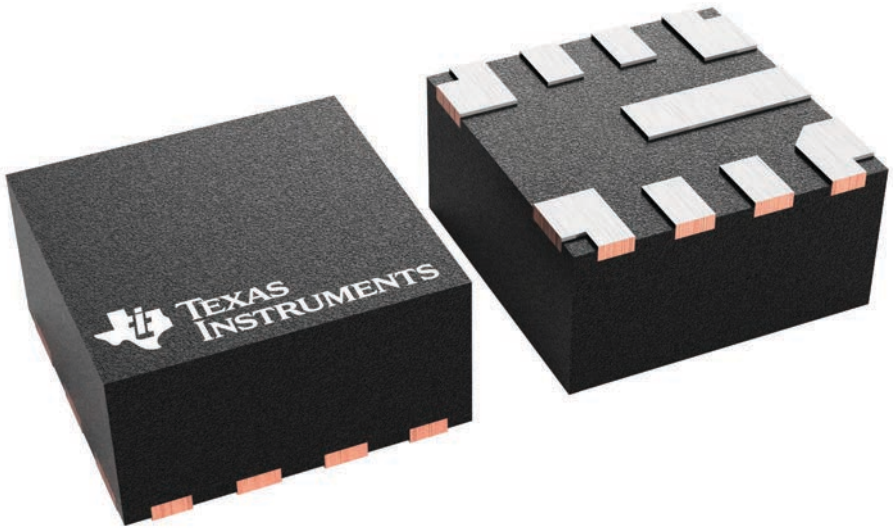
RPE 9

VQFN-HR - 1.0 mm max height

2 x 2, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



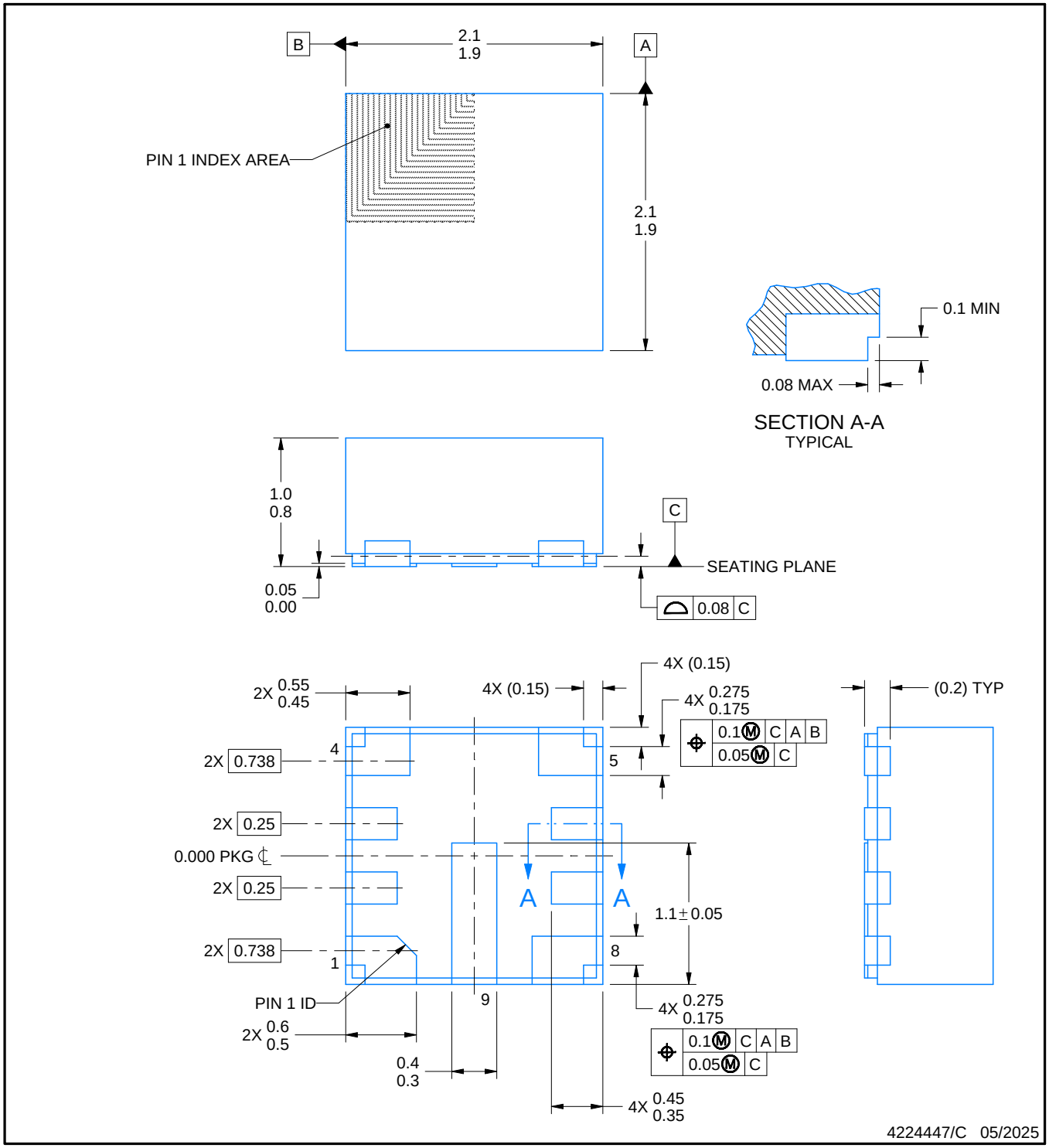
4227057/A

PACKAGE OUTLINE

RPE0009A

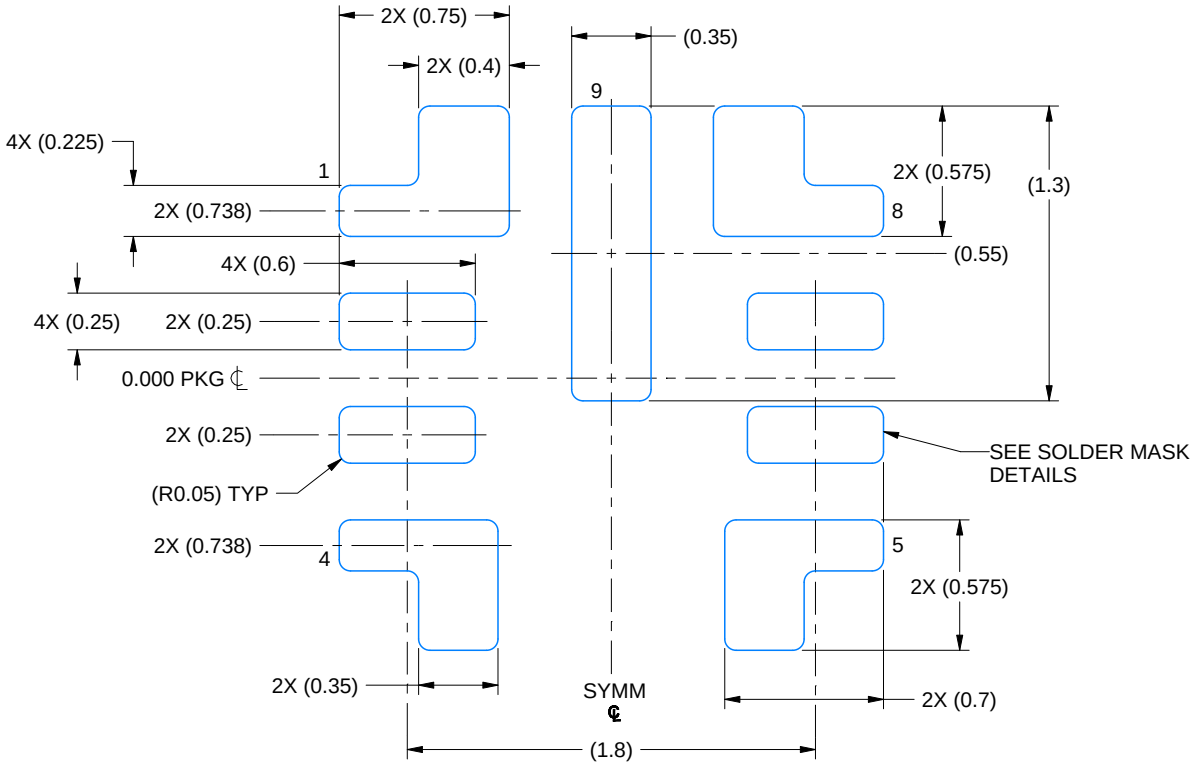
VQFN-HR - 1.0 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

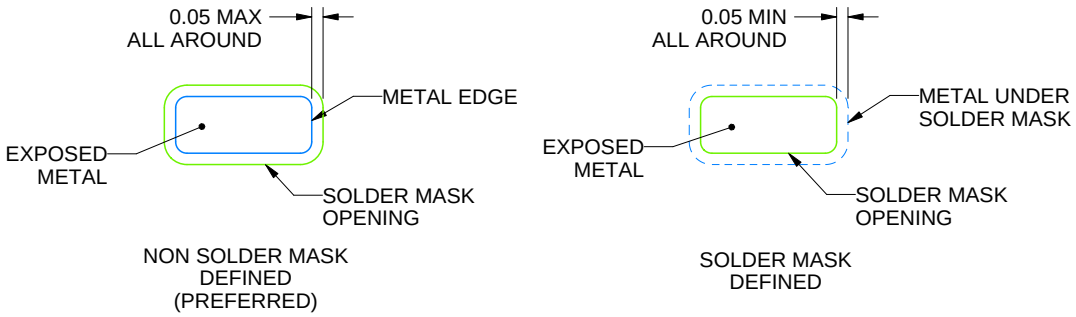


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 30X

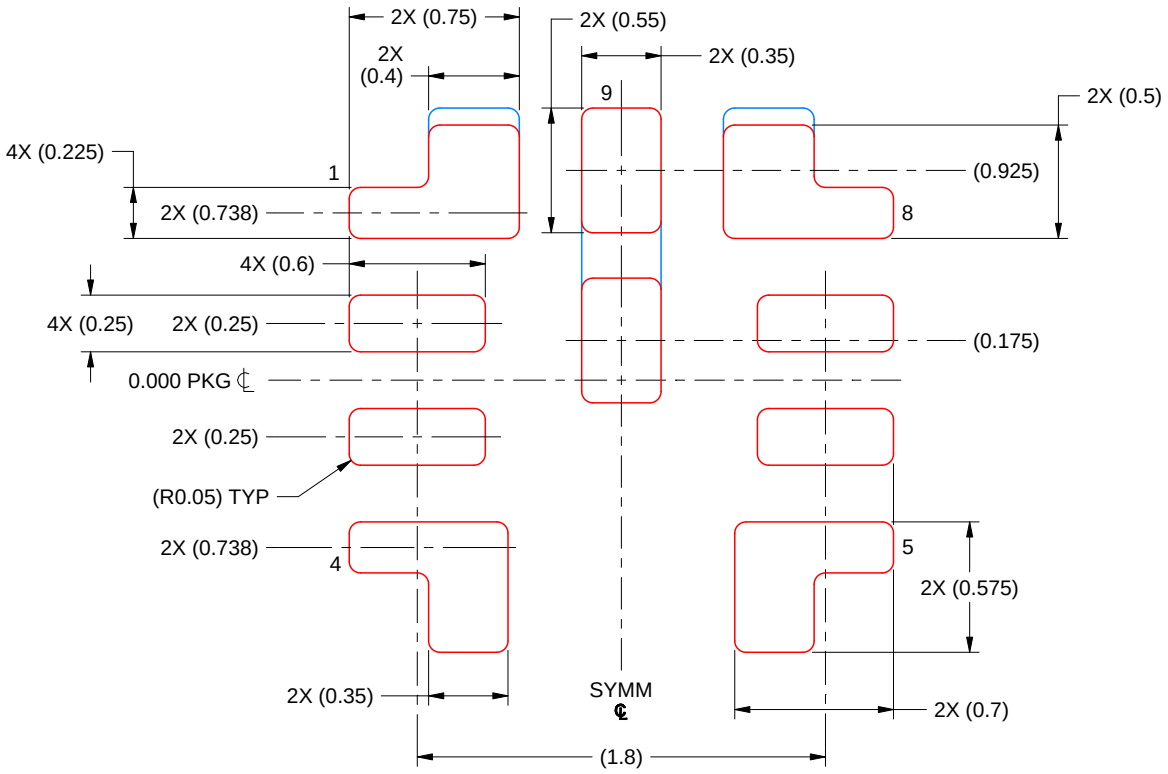


SOLDER MASK DETAILS

4224447/C 05/2025

NOTES: (continued)

3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
4. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 30X

PADS 1 & 8:
90% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
PAD 9:
85% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

DWG_NO:5/REV:5 MM_YYYY:5

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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