# LMX1214 低ノイズ、高周波バッファおよびデバイダ

## 1 特長

- 300MHz から 18GHz までの周波数に対応するクロック バッファ
- 最大 8GHz のデバイダ出力周波数をサポート
- 超低ノイズ
  - ノイズ フロア (6GHz 出力):-161dBc/Hz
  - 6GHz 出力時の 36fs の追加ジッタ (100Hz～$f_{CLK}$)
  - 5fs の追加ジッタ (100Hz～100MHz)
- 4 つの高周波クロック出力
  - 共有分周比は 1 (バイパス)、2、3、4、5、6、7、8
- 出力間スキュー標準値:1ps
- 出力イネーブルおよびデバイダ /2、/3、/4 の値を設定するためのピン モード オプションをサポート
- AUXCLK 出力
  - 個別の分周バンク上
  - 1、2、4 プリデバイダ
  - 1 (バイパス)、2 、…、1023 ポストディバイダ
- 8 つのプログラム可能な出力電力レベル
- すべてのデバイダへの同期機能
- 2.5V の動作電圧
- 動作温度:-40℃～+85℃

## 2 アプリケーション

- 試験 & 測定:
  - オシロスコープ
  - ワイヤレス機器テスター
  - 広帯域デジタイザ
- 航空宇宙 & 防衛:
  - レーダー
  - 電子戦
  - シーカー フロント エンド
  - 軍需品
  - フェーズド アレイ アンテナ / ビーム フォーミング
- 汎用:
  - データ コンバータのクロック供給
  - クロック バッファの分配 / 分周

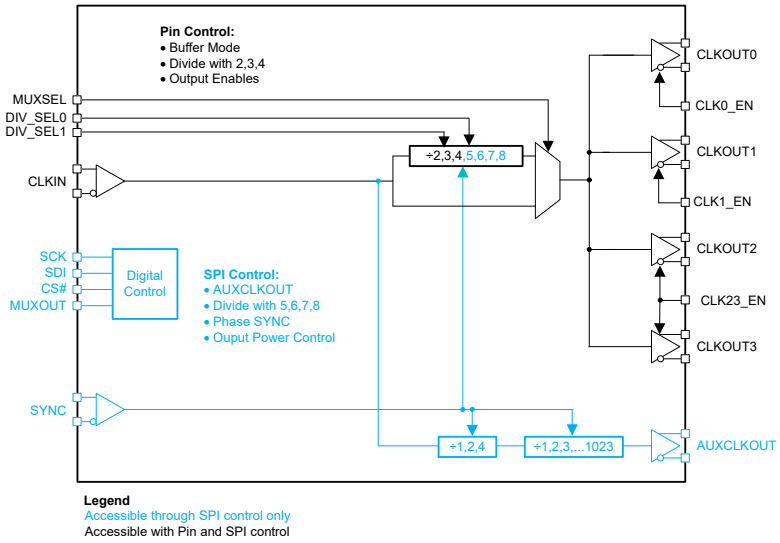
## 3 概要

LMX1214 は、高い出力周波数、超低ノイズ フロア、超低スキュー クロック分配を特長としています。このデバイスは、4 つの高周波出力クロックと、低周波数の補助クロック出力を備えています。このデバイスは、高周波クロックのバッファ モードと分周モードの両方をサポートしています。このデバイスは、マルチチャネル、低スキュー、超低ノイズの局所発振器信号を複数のミキサに分配できます。

**パッケージ情報**

| 部品番号 | パッケージ (1) | パッケージ サイズ(2) |
|---|---|---|
| LMX1214 | RHA (VQFN、40) | 6 mm × 6 mm |

(1) 利用可能なすべてのパッケージについては、データシートの末尾にある注文情報を参照してください。
(2) パッケージ サイズ (長さ × 幅) は公称値であり、該当する場合はピンも含まれます。




ブロック図

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# 4 Pin Configuration and Functions

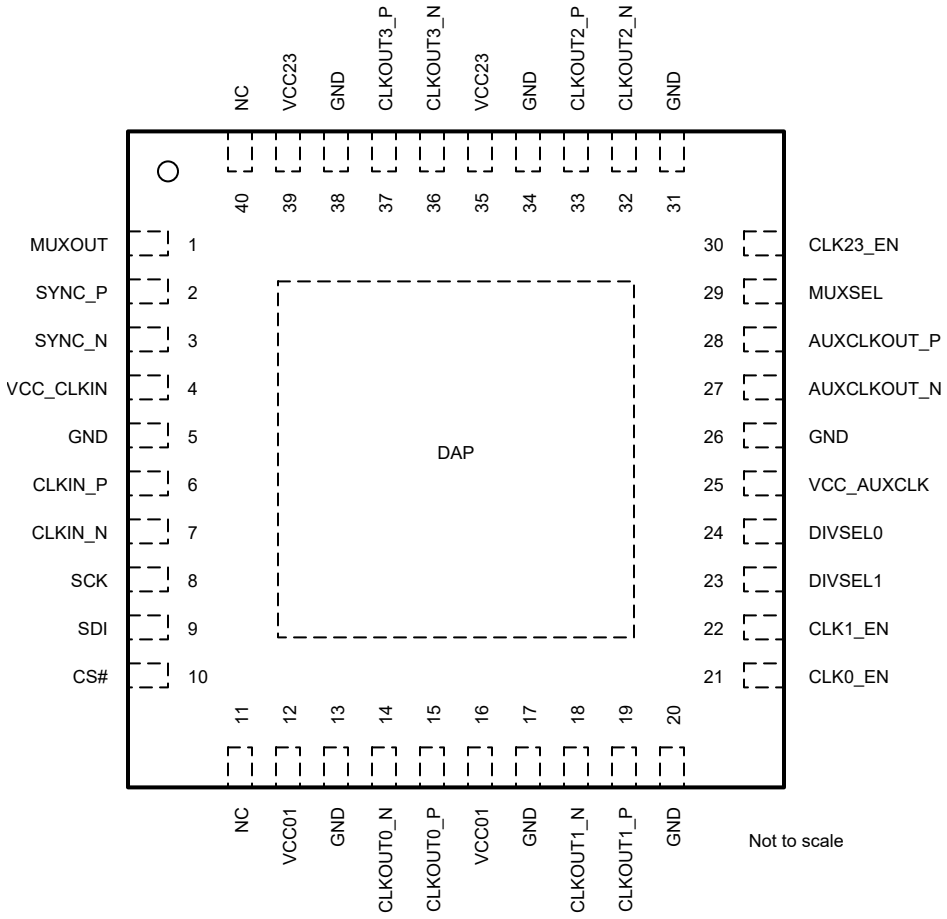



**図 4-1. RHA0040C Package 40-Pin VQFN Top View**

**表 4-1. Pin Functions**

| NO. | NAME | TYPE[1] | DESCRIPTION |
|---|---|---|---|
| 1 | MUXOUT | O | SPI readback output (SDO). |
| 2 | SYNC_P | I | Differential synchronization input. Internal 100-Ω differential termination AC-coupled to GND with a 10-pf capacitor. Supports AC and DC coupling which can directly accept a common mode voltage of 1.2 V to 2 V. |
| 3 | SYNC_N | | |
| 4 | VCC_CLKIN | PWR | Connect to a 2.5-V supply. Recommend a shunt RF wideband capacitor (typically 0.1 µF or smaller) close to the pin in parallel with larger capacitors (typically 1 µF and 10 µF). Large capacitors can be placed bit further away from the pin. |
| 5 | GND | GND | Ground these pins. |
| 6 | CLKIN_P | I | Differential reference input clock. Internal 100-Ω differential termination. AC-couple with a capacitor appropriate to the input frequency (typically 0.1 µF or smaller). If using single-ended, terminate unused pin with 50-Ω resistor AC-coupled to ground. |
| 7 | CLKIN_N | | |
| 8 | SCK | I | SPI clock. High impedance CMOS input. Accepts up to 3.3 V. |
| 9 | SDI | I | SPI data input. High impedance CMOS input. Accepts up to 3.3 V. |
| 10 | CS# | I | SPI chip select. High impedance CMOS input. Accepts up to 3.3 V. |
| 11 | NC | — | Not connected |

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**表 4-1. Pin Functions (続き)**

| NO. | NAME | TYPE(1) | DESCRIPTION |
|---|---|---|---|
| 12 | VCC01 | PWR | Connect to a 2.5-V supply. Recommend a shunt RF wideband capacitor (typically 0.1 µF or smaller) close to the pin in parallel with larger capacitors (typically 1 µF and 10 µF). Large capacitors can be placed bit further away from the pin. |
| 13 | GND | GND | Ground this pin |
| 14 | CLKOUT0_N | O | Differential clock output pairs. Each pin is an open-collector output with internally integrated 50-Ω resistor with programmable output swing. AC coupling required. |
| 15 | CLKOUT0_P | | |
| 16 | VCC01 | PWR | Connect to a 2.5-V supply. Recommend a shunt RF wideband capacitor (typically 0.1 µF or smaller) close to the pin in parallel with larger capacitors (typically 1 µF and 10 µF). Large capacitors can be placed bit further away from the pin. |
| 17 | GND | GND | Ground this pin |
| 18 | CLKOUT1_N | O | Differential clock output pairs. Each pin is an open-collector output with internally integrated 50-Ω resistor with programmable output swing. AC coupling required. |
| 19 | CLKOUT1_P | | |
| 20 | GND | GND | Ground this pin |
| 21 | CLK0_EN | I | CLKOUT0 output enable pin |
| 22 | CLK1_EN | I | CLKOUT1 output enable pin |
| 23 | DIVSEL1 | I | Main clock out divider value 2, 3, and 4 selection control pins |
| 24 | DIVSEL0 | | |
| 25 | VCC_AUXCLK | PWR | Connect to a 2.5-V supply. Recommend a shunt RF wideband capacitor (typically 0.1 µF or smaller) close to the pin in parallel with larger capacitors (typically 1 µF and 10 µF). Large capacitors can be placed bit further away from the pin. |
| 26 | GND | GND | Ground this pin |
| 27 | AUXCLKOUT_N | O | Differential clock output pair. Selectable CML, or LVDS format. Programmable common-mode voltage. |
| 28 | AUXCLKOUT_P | | |
| 29 | MUXSEL | I | Clock out Bypass or Divider path MUX selection |
| 30 | CLK23_EN | I | CLKOUT2 & CLKOUT3 output enable pin |
| 31 | GND | GND | Ground this pin |
| 32 | CLKOUT2_N | O | Differential clock output pairs. Each pin is an open-collector output with internally integrated 50-Ω resistor with programmable output swing. AC coupling required. |
| 33 | CLKOUT2_P | | |
| 34 | GND | GND | Ground this pin |
| 35 | VCC23 | PWR | Connect to a 2.5-V supply. Recommend a shunt RF wideband capacitor (typically 0.1 µF or smaller) close to the pin in parallel with larger capacitors (typically 1 µF and 10 µF). Large capacitors can be placed bit further away from the pin. |
| 36 | CLKOUT3_N | O | Differential clock output pairs. Each pin is an open-collector output with internally integrated 50-Ω resistor with programmable output swing. AC coupling required. |
| 37 | CLKOUT3_P | | |
| 38 | GND | GND | Ground this pin |
| 39 | VCC23 | PWR | Connect to a 2.5-V supply. Recommend a shunt RF wideband capacitor (typically 0.1 µF or smaller) close to the pin in parallel with larger capacitors (typically 1 µF and 10 µF). Large capacitors can be placed bit further away from the pin. |
| 40 | NC | — | Not connected |
| GND | DAP | GND | Ground this pin |

(1) I = Input; O = Output; GND = Ground; PWR = Power


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# 5 Specifications

## 5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| $V_{DD}$ | Power supply voltage | –0.3 | 2.75 | V |
| $V_{IN}$ | DC Input Voltage (SCK, SDI, CSB) | GND | 3.6 | V |
| $V_{IN}$ | DC Input Voltage (SYNC) | GND | $V_{DD}$ + 0.3 | V |
| $V_{IN}$ | AC Input Voltage (CLKIN) | | 2.1 | Vpp |
| $T_J$ | Junction temperature | | 150 | °C |
| $T_{stg}$ | Storage temperature | –65 | 150 | °C |

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

## 5.2 ESD Ratings

| | | | VALUE | UNIT |
|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1) | ±2500 | V |
| | | Charged device model (CDM), per ANSI/ESDA/JEDEC JS-002, all pins(2) | ±500 | |

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

## 5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

| | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{DD}$ | Supply voltage | 2.4 | 2.5 | 2.6 | V |
| $T_A$ | Ambient temperature | –40 | | 85 | °C |
| $T_J$ | Junction temperature | | | 125 | °C |

## 5.4 Thermal Information

| SYMBOL | THERMAL METRIC(1) | VALUE | UNIT |
|---|---|---|---|
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 24.8 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 13.0 | °C/W |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 6.9 | °C/W |
| $\Psi_{JT}$ | Junction-to-top characterization parameter | 0.1 | °C/W |
| $\Psi_{JB}$ | Junction-to-board characterization parameter | 6.9 | °C/W |
| $R_{\theta JC(bot)}$ | Junction-to-case (bottom) thermal resistance | 0.5 | °C/W |

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application note.

## 5.5 Electrical Characteristics

2.4 V ≤ VCC ≤ 2.6 V, –40°C ≤ $T_A$ ≤ +85°C. Typical values are at VCC = 2.5 V, 25°C (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| **Current Consumption** | | | | | |

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2.4 V ≤ VCC ≤ 2.6 V, –40°C ≤ $T_A$ ≤ +85°C. Typical values are at VCC = 2.5 V, 25°C (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $I_{CC}$ | Supply current (1) | Powered up, all outputs on | | | 530 | | mA |
| | | Powered up, all outputs off | | | 290 | | |
| | | Powered down | | | 12 | | |
| $I_{ADD}$ | Additive output current | OUTx_PWR = 7 | | | 70 | | mA |
| | Divider current | Divide, CLK_DIV = 8 | | | 36 | | |
| Isync | Supply current | with SYNC enable | | | 685 | | mA |
| **SYNC Pins** | | | | | | | |
| $V_{SYNC_single}$ | Voltage input range | DC Coupled single ended | | 0.6 | | 1 | Vpp |
| $V_{SYNC}$ | Voltage input range | AC differential voltage | | 0.8 | | 2 | Vpp |
| $V_{CM}$ | Input common mode | Differential 100 Ω Termination, DC coupled Set externally | | 1.2 | 1.3 | 2 | V |
| **Clock Input** | | | | | | | |
| $f_{IN}$ | Input frequency | Buffer Mode Only | | 0.3 | | 18(2) | GHz |
| $P_{IN}$ | Input power | Single-ended power at CLKIN_P or CLKIN_N | | 0 | | 10 | dBm |
| **Clock Outputs** | | | | | | | |
| $f_{OUT}$ | Output frequency | Divide-by-2 | Without Sync (pin mode) | 0.15 | | 8 | GHz |
| $f_{OUT}$ | Output frequency | Divide-by-2 | With Sync | 0.15 | | 6.4 | GHz |
| $f_{OUT}$ | Output frequency | Buffer Mode | | 0.3 | | 18(2) | |
| $f_{OUT}$ | Output frequency | AUXCLK output | | 1 | | 800 | MHz |
| $p_{OUT}$ | Output power | Single-Ended | $f_{CLKLOUT}$= 6 GHz OUTx_PWR = 7 | | 6.5 | | dBm |
| | | | $f_{CLKLOUT}$= 12.8 GHz OUTx_PWR = 7 | | 3.5 | | |
| | | | $f_{CLKLOUT}$= 18 GHz OUTx_PWR = 7 | | 1.5 | | |
| Φimb | Output phase imbalance between P & N | Buffer mode | | | | 5 | ps |
| $t_{RISE}$ | Rise time (20% to 80%) | $f_{CLKOUT}$ = 300 MHz | | | 45 | | ps |
| $t_{FALL}$ | Fall time (20% to 80%) | $f_{CLKOUT}$ = 300 MHz | | | 45 | | ps |
| $t_{MUTE}$ | Output mute time | Falling edge of OE pin | | | | 30 | µs |
| $t_{UNMUTE}$ | Output unmute time | Rising edge of OE pin | | | | 30 | µs |
| **Propagation Delay and Skew** | | | | | | | |
| \| $t_{SKEW}$ \| | Magnitude of skew between outputs | CLKOUTx to CLKOUTy, not AUXCLK | | | 1 | 10 | ps |
| $t_{DLY}$ | Propagation delay | $T_A$=25°C | Bypass Mode | | 120 | | ps |
| | | | Divide Mode | | 125 | | |
| $\Delta t_{DLY}/\Delta T$ | Propagation delay variation over temperature | Bypass Mode | | | 0.06 | | ps/C |
| **Noise, Jitter, and Spurs** | | | | | | | |
| $J_{CKx}$ | Additive jitter | Additive Jitter. 12k to 100 MHz integration bandwidth. | Buffer Mode | | 5 | | fs, rms |
| Flicker | 1/f flicker noise | Slew Rate > 8 V/ns, $f_{CLK}$=6 GHz | Buffer Mode | | –154 | | dBc/Hz |
| NFL | Noise Floor | $f_{OUT}$ = 6 GHz; $f_{Offset}$ = 100 MHz | Buffer Mode | | –161 | | dBc/Hz |
| NFL | | | Divide-by-2 | | –160.5 | | |


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2.4 V ≤ VCC ≤ 2.6 V, –40°C ≤ $T_A$ ≤ +85°C. Typical values are at VCC = 2.5 V, 25°C (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| H2 | Second harmonic | $f_{OUT}$ = 6 GHz (differential), Buffer Mode | | | –25 | | dBc |
| | | $f_{OUT}$ = 6 GHz (single-ended), Buffer Mode | | | –12 | | |
| | | $f_{OUT}$ = 6 GHz, single-ended, Divide by 2 | | | –13.5 | | |
| Coupling | AUXCLK to CLKOUT coupling | fout = 6 GHz, Single-ended; $f_{AUXCLK}$ = 300MHz | | | –70 | | dBc |
| NFL | Noise Floor | $f_{AUXCLK}$ = 300MHz; LVDS mode | | | –152 | | dBc |
| NFL | Noise Floor | $f_{AUXCLK}$ = 300MHz; CML mode | | | –151 | | dBc |
| P leakage | Leakage power Input to Output | Chip power down | Single Ended Input | | –45 | | dBc |
| P leakage | Leakage power Input to Output | Pin OE = 0 | Single Ended Input | | –40 | | dBc |
| **Digital Interface (SCK, SDI, CS#, MUXOUT,CLKx_EN,MUXSEL,DIVSELx)** | | | | | | | |
| $V_{IH}$ | High-level input voltage | SCK, SDI, CS# | | 1.4 | | 3.3 | V |
| | High-level input voltage | CLKx_EN,DIVSELx,MUXSEL | | 1.4 | | 3.3 | V |
| $V_{IL}$ | Low-level input voltage | SCK, SDI, CS# | | 0 | | 0.4 | V |
| | Low-level input voltage | CLKx_EN,DIVSELx,MUXSEL | | 0 | | 0.4 | V |
| $I_{IH}$ | High-level input current | SCK, SDI, CS# | | –42 | | 42 | µA |
| | High-level input current | CLKx_EN,DIVSELx,MUXSEL | | –42 | | 42 | µA |
| $I_{IL}$ | Low-level input current | SCK, SDI, CS# | | –25 | | 25 | µA |
| | Low-level input current | CLKx_EN,DIVSELx,MUXSEL | | –25 | | 25 | µA |
| $V_{OH}$ | High-level output voltage | MUXOUT | $I_{OH}$ = 5 mA | 1.4 | | Vcc | V |
| | High-level output voltage | | $I_{OH}$ = 0.1 mA | 2.2 | | Vcc | V |
| $V_{OL}$ | Low-level output voltage | MUXOUT | $I_{OL}$ = 5 mA | | | 0.45 | V |

(1) Unless Otherwise Stated, $f_{CLKIN}$=6 GHz, CLK_MUX=Buffer, All clocks on with OUTx_PWR=7.
(2) SYNC and dividers supported up to 12.8GHz frequency

## 5.6 Timing Requirements

| | | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|
| **Timing Requirements** | | | | | | |
| $f_{SPI}$ | SPI Read/Write Speed | | | | 2 | MHz |
| $t_{CE}$ | Clock to enable low time | | 20 | | | ns |
| $t_{CS}$ | Clock to data wait time | | 20 | | | ns |
| $t_{CH}$ | Clock to data hold time | | 20 | | | ns |
| $t_{CWH}$ | Clock pulse width high | | 100 | | | ns |
| $t_{CWL}$ | Clock pulse width low | | 100 | | | ns |
| $t_{CES}$ | Enable to clock setup time | | 20 | | | ns |
| $t_{EWH}$ | Enable pulse width high | | 50 | | | ns |
| $t_{CD}$ | Falling clock edge to data wait time | | 0 | | 100 | ns |

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## 5.7 Timing Diagram

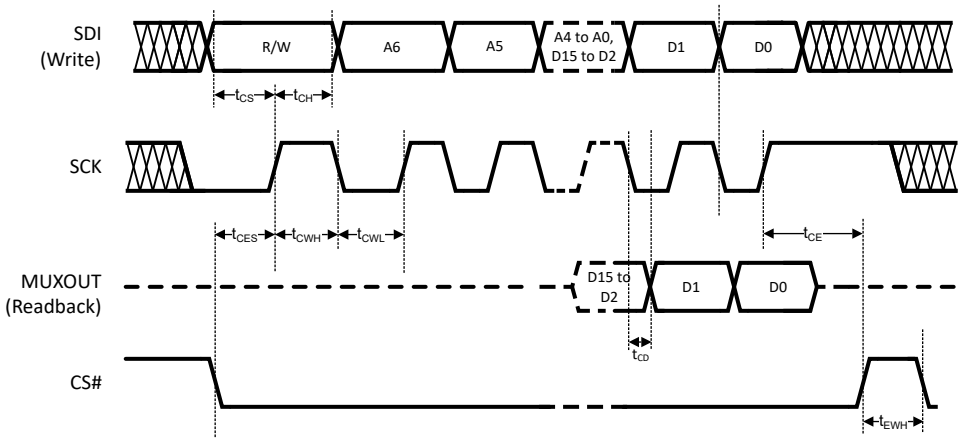



**図 5-1. Serial Data Input Timing Diagram**

There are several other considerations for writing on the SPI:

- The R/W bit must be set to 0.
- The data on SDI pin is clocked into a shift register on each rising edge on the SCK pin.
- The CS# must be held low for data to be clocked. The device ignores clock pulses if CS# is held high.
- Recommended SPI settings for this device are CPOL=0 and CPHA=0.
- When SCK and SDI lines are shared between devices, TI recommends to hold the CS# line high on the device that is not to be clocked.

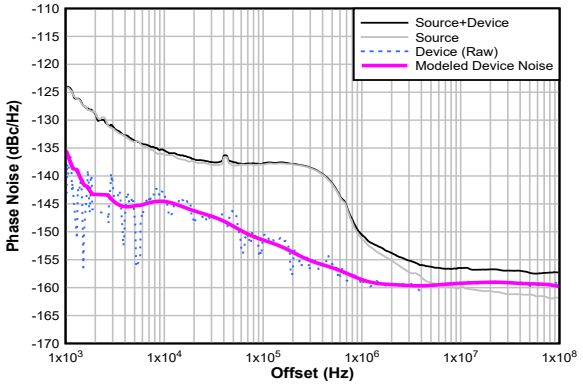
There are several other considerations for SPI readback:

- The R/W bit must be set to 1.
- The MUXOUT pin is always be low for the address portion of the transaction.
- The data on MUXOUT is clocked out at the falling edge of SCK. In other words, the readback data is available at the MUXOUT pin $t_{CD}$ after the clock falling edge.
- The data portion of the transition on the SDI line is always ignored.
- The MUXOUT pin does not automatically tri-state after a readback transaction completes. When sharing the SPI bus readback pin with other devices, set MUXOUT_EN=0 after all readback transactions from device are complete to manually tri-state the MUXOUT pin, permitting other devices to control the readback line.
- The values read back, even for R/W bits are not always the value written but rather an internal device state that takes into account the programmed value as well as other factors, such as pin states.


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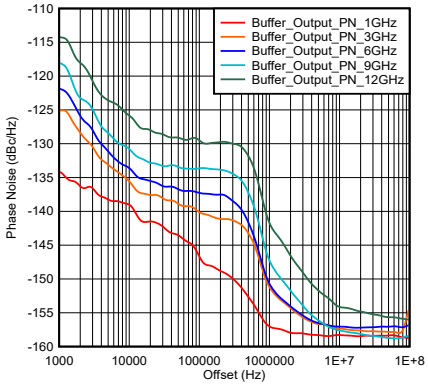
## 5.8 Typical Characteristics

If not otherwise, the following conditions can be assumed: Temperature = 25°C, Vcc = 2.5 V, OUTx_PWR = 7, CLKIN driven differentially with 8 dBm at each pin. Signal source used is SMA100B with ultra-low noise option B711.




Noise floor = -160dBc/Hz

**図 5-2. Buffer Phase Noise Plot at 6-GHz Output**




Source noise is not de-embedded.

**図 5-3. Buffer Output Phase Noise Plots vs Output Frequencies**

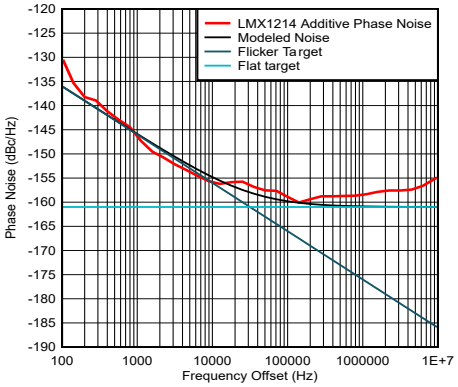



**図 5-4. LMX1214 Flicker Noise at 6 GHz**

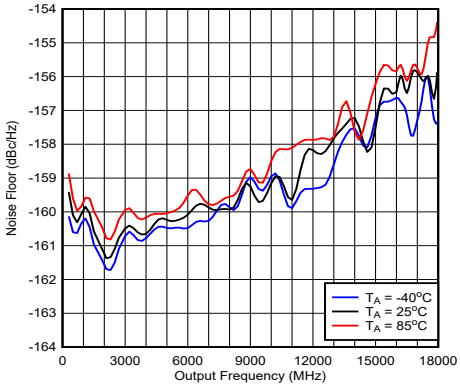



**図 5-5. Noise Floor in Buffer Mode**

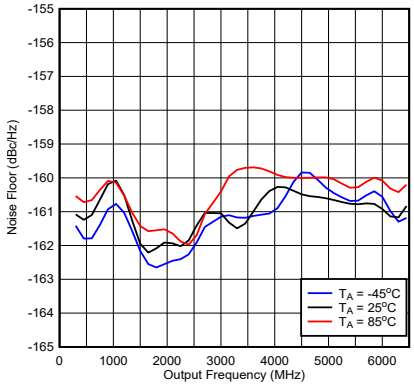



**図 5-6. Noise Floor in Divider Mode**

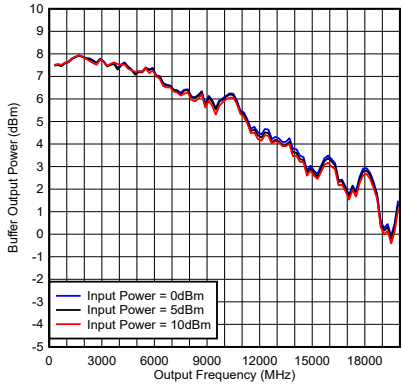



**図 5-7. Buffer Mode Single-Ended Output Power vs Input Power**

## 5.8 Typical Characteristics (continued)

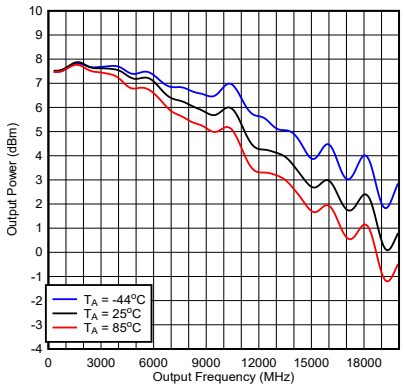
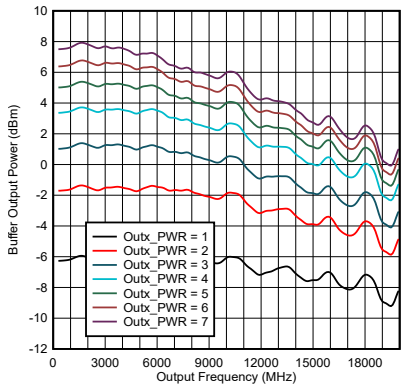



**図 5-8. Buffer Mode Single-Ended Output Power Over Temperature**




Applies to all modes except divider mode with odd divide (which have slightly lower power).

**図 5-9. Buffer Mode Single-Ended Output Power vs Power Codes**

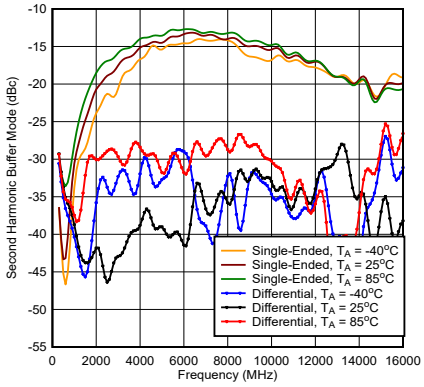
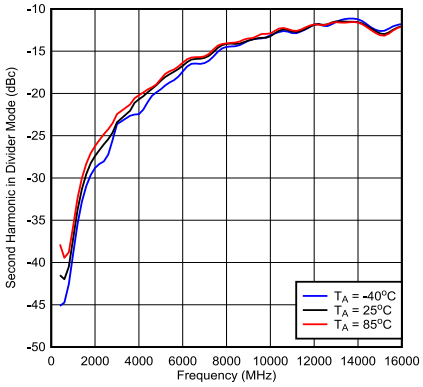



**図 5-10. Second Harmonic in Buffer Mode**




Single-Ended Input Power

**図 5-11. Second Harmonic in Divider Mode**

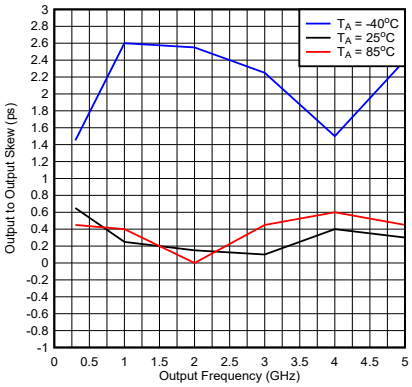
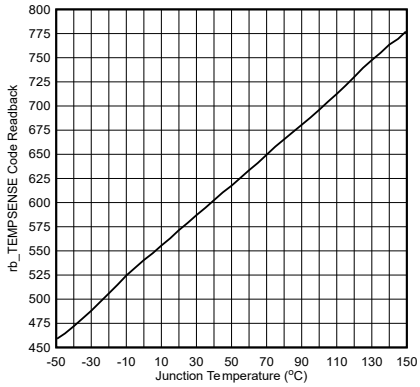



**図 5-12. Output to Output Skew**

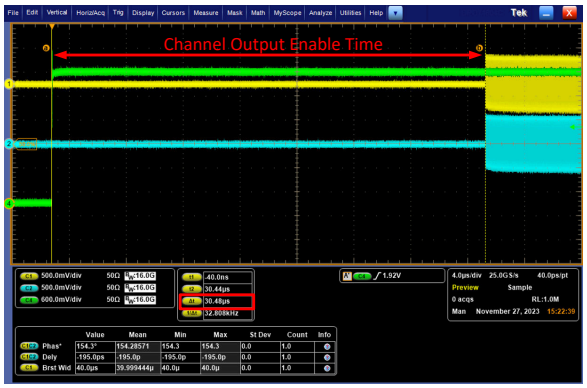



Measured in power-down mode to make Junction Temperature = Ambient Temperature.

**図 5-13. Temperature Sensor Readback**

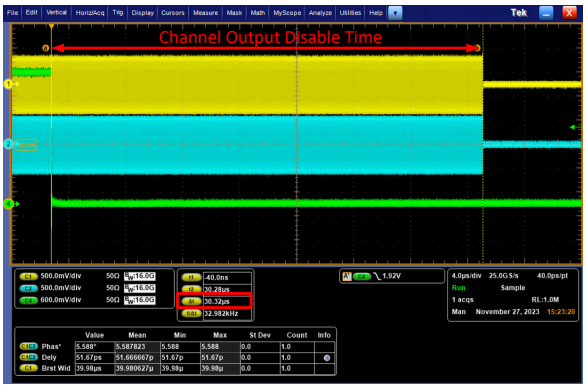

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## 5.8 Typical Characteristics (continued)




at 300-MHz Output Frequency

**図 5-14. Channel Enable Setting Time**




at 300-MHz Output Frequency

**図 5-15. Channel Disable Setting Time**

# 6 Detailed Description

## 6.1 Overview

This device has four main clock outputs and another AUXCLK output. The main clock outputs are all the same frequency. This frequency can be the same or divided relative to the input clock. Each of these clock outputs has programmable power level. The AUXCLK output frequency is independent and typically lower frequency than the other four main clocks and has programmable output format (CML and LVDS) and power level.

### *6.1.1 Range of Dividers*

There are dividers that allow the main and AUXCLK outputs to be a divided value of the input clock. The main clock output has only one common divider, whereas the AUXCLK has a pre-divider and main divider.

**表 6-1. Range of Dividers**

| CATEGORY | | | SPI PROGRAMMABLE RANGE | PIN PROGRAMMABLE RANGE | COMMENTS |
|---|---|---|---|---|---|
| Main Clocks | Buffer | | | Yes | |
| | Divider | | 2, 3, 4, … 8 | 2,3,4 | Odd divides (except 1) do not have 50% duty cycle |
| | Power Level | | 0,1,…,7 | No | |
| AUXCLK | Divide | PreDivide | 1, 2, 4 | No | TotalDivide = PreDivide × Divide<br>Odd divides (except 1) do not have 50% duty cycle |
| | | Divide | 1, 2, 3, … 1023 | No | |

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## 6.2 Functional Block Diagram

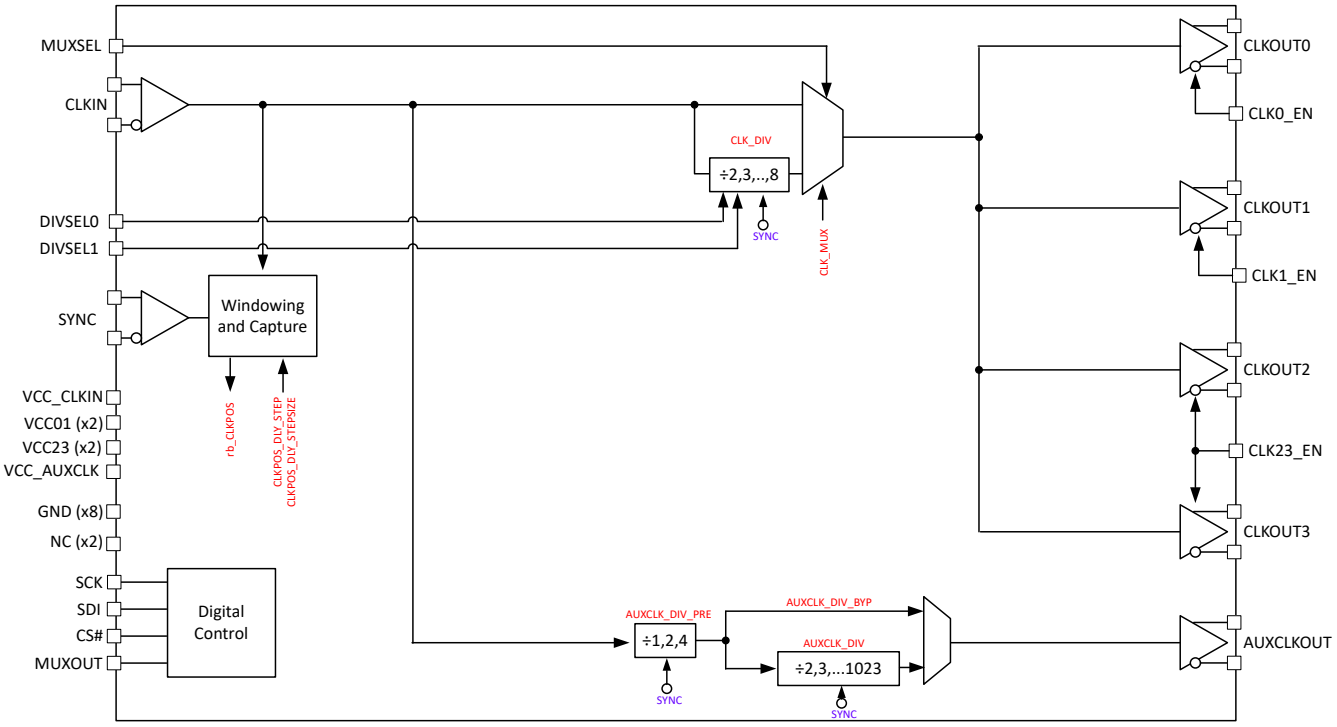



**図 6-1. Functional Block Diagram**


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## 6.3 Feature Description

### 6.3.1 Power-On Reset

When the device is powered up, the power-on reset (POR) resets all registers to a default state as well as resets all state machines and dividers. For the power-on reset state, all the dividers are bypassed and the device performs as a 4-output buffer. Wait 100 µs after the power supply rails before programming other registers to verify that this reset is finished. When there is no input clock present, the device power-on reset happens properly and functions well, but the device draws less current. The current changes after an input clock is added.

Performing a software power-on reset by writing RESET = 1 in the SPI bus is also possible and generally good practice. The RESET bit self-clears when the user writes to another register. The SPI bus can be used to override these states to the desired settings.

Although the device does have an automatic power-on reset, the device can be impacted by different ramp rates on the different supply pins, especially in the presence of a strong input clock signal. TI therefore recommends to do a software reset after POR. This can be done by programming RESET = 1. The reset bit can be cleared by programming any other register or setting RESET back to 0. Even at the maximum allowed SPI bus speed, the software reset event always completes before the subsequent SPI write.

### 6.3.2 Temperature Sensor

The junction temperature can be read back for purposes such as characterization or to make adjustments based on temperature. Such adjustments can include adjusting CLKOUTx_PWR to make the output power more stable or using external or digital delays to compensate for changes in propagation delay over temperature.

The junction temperature is typically higher than the ambient temperature due to power dissipation from the outputs and other functions on the device. 式 1 shows the relationship between the code read back and the junction temperature.

$$\text{Temperature} = 0.65 \times \text{Code} - 351 \quad (1)$$

式 1 is based on a best-fit line created from three devices from slow, nominal, and fast corner lots (nine parts total). The worst-case variation of the actual temperature from the temperature predicted by the best-fit line is 13°C, which works out to 20 codes.

### 6.3.3 Clock Outputs

This device has four main output clocks which share a common frequency. This does not include the additional lower frequency AUXCLK output.

#### 6.3.3.1 Clock Output Buffers

The output buffers have a format that is open collector with an integrated pullup resistor, similar to CML.

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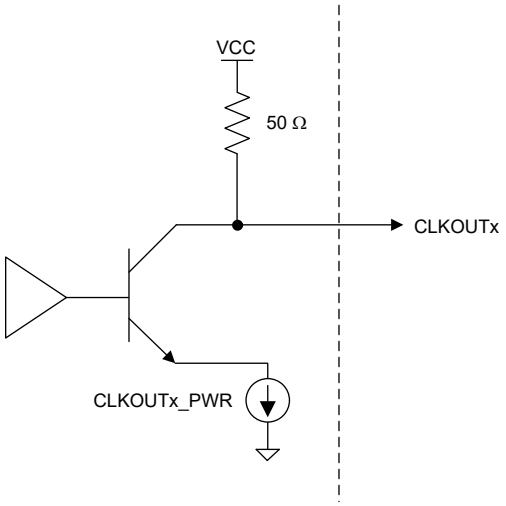



**図 6-2. CLKOUT Output Buffer**

The CLKOUTx_EN bits can enable the output buffers. The output power of the buffers can be individually set with CLKOUTx_PWR field.

**表 6-2. Clock Output Power**

| CLKOUTx_EN | CLKOUTx_PWR | OUTPUT BUFFER |
|---|---|---|
| 0 | Don't Care | Powered Down |
| 1 | 0 | Minimum |
| | 1 | |
| | ... | |
| | 7 | Maximum |

#### 6.3.3.2 Clock MUX

The four main clocks are the same frequency, but this frequency can be bypassed or divided. This is determined by the CLK_MUX word.

**表 6-3. Clock MUX**

| CLK_MUX | OPTION | VALUES SUPPORTED |
|---|---|---|
| 0 | Buffer Mode | ÷1 (bypass) |
| 1 | Divider Mode | ÷2, 3, 4, 5, 6, 7, and 8 |

#### 6.3.3.3 Clock Divider

Set the CLK_MUX to Divided to a divide value by 2, 3, 4, 5, 6, 7, or 8. This is set by the CLK_DIV word. When using the clock divider, any change to the input frequency requires the CLK_DIV_RST bit to be toggled from 1 to 0.

**表 6-4. Clock Divider**

| CLK_DIV | DIVIDE | DUTY CYCLE |
|---|---|---|
| 0 | Reserved | n/a |
| 1 | 2 | 50% |
| 2 | 3 | 33% |
| 3 | 4 | 50% |
| 4 | 5 | 40% |
| 5 | 6 | 50% |
| 6 | 7 | 43% |


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表 6-4. Clock Divider (続き)

| CLK_DIV | DIVIDE | DUTY CYCLE |
|---|---|---|
| 7 | 8 | 50% |

### 6.3.4 AUXCLK Output

The AUXCLK output can drive devices using lower frequency clocks, such as FPGAs. The AUXCLK output has the programmable output formats LVDS or CML.

#### 6.3.4.1 AUXCLKOUT Output Format

The AUXCLKOUT output format can be programmed to LVDS and CML modes. Depending on the format, the common mode can be programmable or external components can be required.

表 6-5. AUXCLKOUT Formats and Properties

| AUXCLKOUT_FMT | FORMAT | EXTERNAL COMPONENTS REQUIRED | OUTPUT LEVEL | COMMON MODE |
|---|---|---|---|---|
| 0 | LVDS | None | Fixed | Programmable through AUXCLKOUT_VCM |
| 2 | CML | Pullup Resistors 50 Ω to $V_{CC}$ | Programmable through AUXCLKOUT_PWR | Not programmable |

#### 6.3.4.2 AUXCLK_DIV_PRE and AUXCLK_DIV Dividers

The AUXCLK_DIV_PRE divider and AUXCLK_DIV dividers are used for the AUXCLKOUT output. The AUXCLK_DIV_PRE divider is necessary to divide the frequency down to verify that the input to the AUXCLK_DIV divider is 3.2 GHz or less. When AUXCLK_DIV is not even and not bypassed, the duty cycle is not be 50%. Both the AUXCLKOUT dividers are synchronized by the SYNC feature, which allows synchronization across multiple devices.

表 6-6. Minimum N-Divider Restrictions

| $f_{CLKIN}$ (MHz) | AUXCLK_DIV_PRE | AUXCLK_DIV | TOTAL DIVIDE RANGE |
|---|---|---|---|
| $f_{CLKIN}$ ≤ 3.2 GHz | ÷1,2,4 | ÷1,2 ,3 ,…1023 | [1, 2, ...1023]<br>[2, 4, ... 2046]<br>[4, 8, 4092] |
| 3.2 GHz < $f_{CLKIN}$≤ 6.4 GHz | ÷2,4 | ÷1, 2 ,3 ,…1023 | [4, ... 2046]<br>[4, 8, 4092] |
| $f_{CLKIN}$ > 6.4 GHz | ÷4 | 1, 2, 3 ,…1023 | [8, 4092] |

### 6.3.5 SYNC Input Pins

The SYNC pins are used for the SYNC and windowing features. These pins can be DC or AC coupled and have internal dual 50-Ω, single-ended termination with programmable common-mode support. SYNC input is required, when the clock dividers (device clock and AUXCLK) need to be synchronized and multi-device sync needed. For buffer mode, sync input is not necessary.

The SYNC feature allows the user to synchronize the CLK_DIV, AUXCLK_DIV, and AUXCLK_DIV_PRE dividers so that the phase offset can be made consistent between power cycles. This allows users to synchronize multiple devices. Multi-device synchronization dividers can only be done through the SYNC pin, not the software.

#### 6.3.5.1 SYNC Pins Common-Mode Voltage

The SYNC_P and SYNC_N pins can be driven either AC or DC coupled. When driven AC coupled, the common-mode voltage can be adjusted with the SYNC_VCM bit.

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**表 6-7. SYNC Pin Common-Mode Voltage**

| SYNC_VCM | COMMON-MODE VOLTAGE |
|---|---|
| 0 | 1.3 V AC-coupled |
| 1 | 1.1 V AC-coupled |
| 2 | 1.5 V AC-coupled |
| 3 | No-Bias (DC Coupled) |

#### 6.3.5.2 Windowing Feature

The windowing feature can be used to internally calibrate the timing between the SYNC and CLKIN pins to optimize setup and hold timing and trim out any mismatches between the SYNC and CLKIN paths. This feature requires that the timing from the SYNC rising edge to the CLKIN rising edge is consistent. The timing from the SYNC rising edge to the CLKIN rising edges can be tracked with the rb_CLKPOS field. After the timing to the rising edge of the CLKIN pin is found, the SYNC rising edge can be internally adjusted with the SYNC_DLY and SYNC_DLY_STEP fields to optimize setup and hold times.

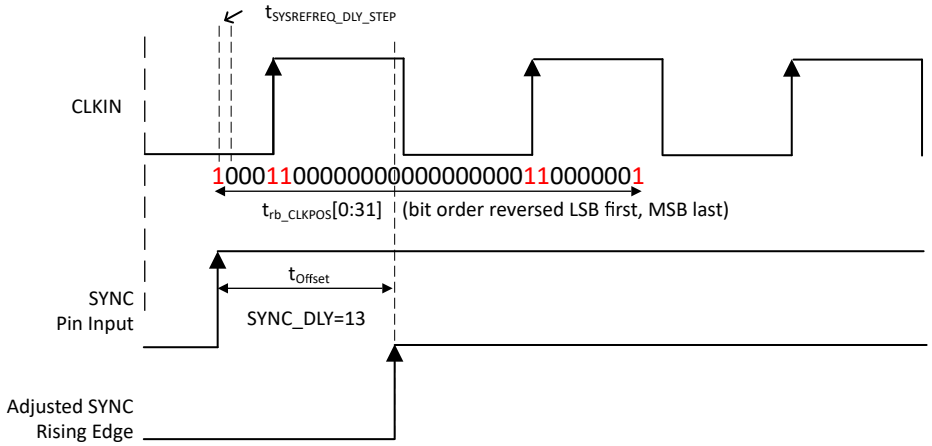



**図 6-3. SYNC Internal Timing Adjustment**


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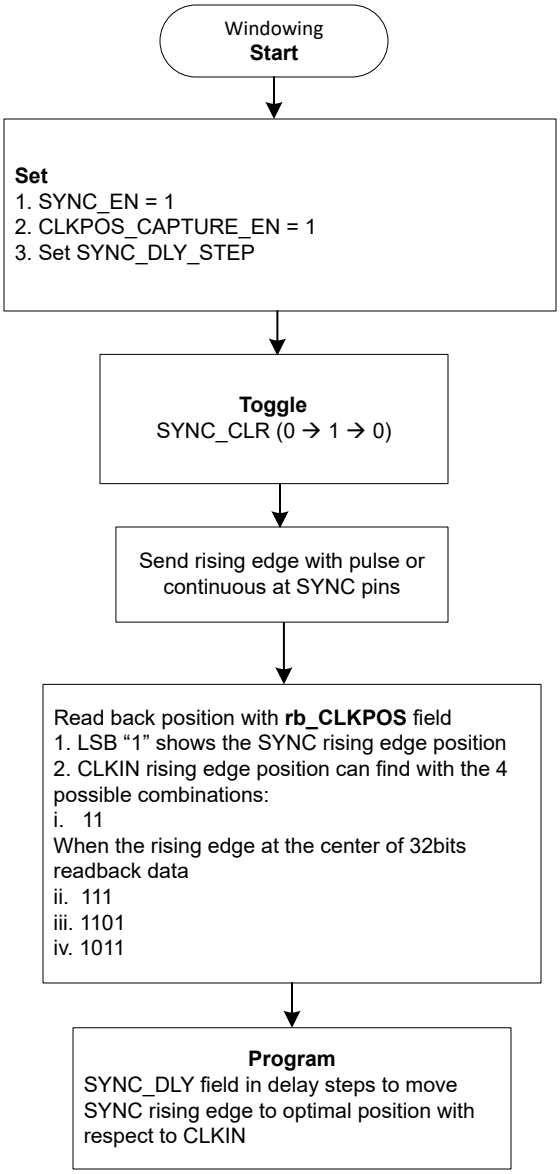



**図 6-4. Flowchart for Windowing Operation**

**表 6-8. SYNC_DLY_STEP**

| INPUT FREQUENCY | RECOMMENDED SYNC_DLY_STEP | DELAY (ps) |
|---|---|---|
| 1.4 GHz < $f_{CLKIN}$ ≤ 2.7 GHz | 0 | 28 |
| 2.4 GHz < $f_{CLKIN}$ ≤ 4.7 GHz | 1 | 15 |
| 3.1 GHz < $f_{CLKIN}$ ≤ 5.7 GHz | 2 | 11 |
| $f_{CLKIN}$ ≥ 4.5 GHz | 3 | 8 |

For the windowing feature:

1. The SYNC pins must be held high for a minimum time of $3/f_{CLKIN}$ + 1.6 ns and only after this time rb_CLKPOS field is valid.
2. If the user infers multiple valid SYNC_DLY values from rb_CLKPOS registers to avoid setup-hold violations, TI recommends to choose the lowest valid SYNC_DLY to minimize variation over temperature.

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For SYNC operation:

1. Only one SYNC pin rising edge is permitted per 75 input clock cycles
2. SYNC must stay high for more than six clock cycles

## 6.4 Device Functional Modes Configurations

The device can configure in high frequency clock buffer mode or divider mode. Each mode requires the below register configurations to function.

**表 6-9. Device Functional Modes Settings**

| REGISTER ADDRESS | BIT | FIELD | FUNCTION | BUFFER | DIVIDER |
|---|---|---|---|---|---|
| R25 | 2:0 | CLK_MUX | Select the mode | 1 | 2 |
| R25 | 5:3 | CLK_DIV | Select the division value | x | CLK_DIV<br>0x1 = ÷2<br>0x2 = ÷3<br>0x3 = ÷4<br>0x4 = ÷5<br>0x5 = ÷6<br>0x6 = ÷7<br>0x7 = ÷8 |

### *6.4.1 Pin Mode Control*

The LMX1214 supports pin mode for individual clock output control, mux selection and few dividers settings.

Below are the pin control options:

#### Output Channel Control

CLKOUT0 and CLKOUT1 have individual output control pins, whereas CLKOUT2 and CLKOUT3 uses a common control pin. These pins enable or disable the CLKOUT of particular channel outputs. Output channels can be controlled through SPI when CLKx_EN pin is high (1).

**表 6-10. Output Channel Control Selection**

| CLKx_EN | CHANNEL OUTPUT STATE | SPI OVERRIDE CONTROL |
|---|---|---|
| 0 | Disable Channel Output | No |
| 1 | Enable Channel Output | Yes |

#### Device Mode Selection

The device can function in buffer mode or divider mode, which can be set through the MUXSEL pin.

**表 6-11. Device Mode Selection**

| MUXSEL | Mode Selection | SPI OVERRIDE CONTROL |
|---|---|---|
| 0 | Buffer Mode | Yes |
| 1 | Divider Mode | No |

#### Divider Value Selection

When the divider mode is selected by MUXSEL pin logic or SPI control, the divider values (/2, /3 or /4) are selected by DIVSELx pin logic.


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**表 6-12. Divider Value Selection**

| DIVSEL1 | DIVSEL0 | DIVIDER VALUE |
|---|---|---|
| 0 | 0 | SPI Override |
| 0 | 1 | 2 |
| 1 | 0 | 3 |
| 1 | 1 | 4 |

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# 7 Register Map

| | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| R0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | POWERDOWN | 0 | 0 |
| R2 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | SMCLK_EN | 0 | 0 | 0 | 1 | 1 |
| R3 | CLKOUT3_EN | CLKOUT2_EN | CLKOUT1_EN | CLKOUT0_EN | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 0 |
| R4 | 0 | 0 | CLKOUT1_PWR | | | CLKOUT0_PWR | | | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| R5 | 0 | 0 | 1 | 1 | 0 | 1 | 1 | 0 | 1 | 1 | CLKOUT3_PWR | | | CLKOUT2_PWR | | |
| R7 | 0 | 1 | 0 | AUXCLKOUT_VCM | | 1 | 0 | AUXCLK_DIV_PWR_PRE | | 0 | 1 | 1 | AUXCLKOUT_PWR | | | 1 |
| R8 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | AUXCLK_DIV_PRE | | | AUXCLKOUT_EN | 0 | 0 | 0 | AUXCLKOUT_FMT | |
| R9 | SYNC_VCM | | SYNC_EN | 0 | AUXCLK_DIV_BYP | 0 | AUXCLK_DIV | | | | | | | | | |
| R11 | rb_CLKPOS | | | | | | | | | | | | | | | |
| R12 | rb_CLKPOS[31:16] | | | | | | | | | | | | | | | |
| R13 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | SYNC_DLY_STEP | |
| R14 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | CLKPOS_CAPTURE_EN | 1 | SYNC_LATCH |
| R15 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | SYNC_DLY | | | | | | SYNC_CLR |
| R23 | TS_EN | 1 | MUXOUT_EN | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R24 | 0 | 0 | 0 | 0 | rb_TS | | | | | | | | | | | TS_CNT_EN |
| R25 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | CLK_DIV_RST | CLK_DIV | | | CLK_MUX | | |
| R75 | rb_CLKOUT2_EN | rb_CLKOUT1_EN | rb_CLKOUT0_EN | rb_MUXSEL1 | 0 | 0 | 0 | 0 | 0 | rb_DIVSEL1 | rb_DIVSEL0 | rb_CE | 0 | 1 | 1 | 0 |
| R79 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 |
| R86 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | MUXOUT_EN_OVRD | 0 | 0 |
| R90 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | AUXCLK_DIV_BYP3 | AUXCLK_DIV_BYP2 | 0 | 0 | 0 | 0 | 0 |

| Programming is NOT required for buffer mode, but can be done to enable other features and enhancements | |
|---|---|
| Registers | Enhancements |


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| | |
|---|---|
| R0, R3, R4, and R5 | Outputs |
| R2, R75 | Pin Modes |
| R7,R8,,R9,R79,R90 | AUXCLK. R79 and R90 are only needed if using a divide by 1 if bypassing the pre-divider for the AUXCLK |
| R11,R12,R13,R14,R15 | SYNC |
| R23, R24, R86 | MUXOUT, Readback, and Temp Sensor |
| R25 | Main Divide |

## 7.1 Device Registers

表 7-1 lists the memory-mapped registers for the Device registers. All register offset addresses not listed in 表 7-1 must be considered as reserved locations and the register contents must not be modified.

**表 7-1. DEVICE Registers**

| Offset | Acronym | Description | Section |
|---|---|---|---|
| 0x0 | R0 | | セクション 7.1.1 |
| 0x2 | R2 | | セクション 7.1.2 |
| 0x3 | R3 | | セクション 7.1.3 |
| 0x4 | R4 | | セクション 7.1.4 |
| 0x5 | R5 | | セクション 7.1.5 |
| 0x7 | R7 | | セクション 7.1.6 |
| 0x8 | R8 | | セクション 7.1.7 |
| 0x9 | R9 | | セクション 7.1.8 |
| 0xB | R11 | | セクション 7.1.9 |
| 0xC | R12 | | セクション 7.1.10 |
| 0xD | R13 | | セクション 7.1.11 |
| 0xE | R14 | | セクション 7.1.12 |
| 0xF | R15 | | セクション 7.1.13 |
| 0x17 | R23 | | セクション 7.1.14 |
| 0x18 | R24 | | セクション 7.1.15 |
| 0x19 | R25 | | セクション 7.1.16 |
| 0x4B | R75 | | セクション 7.1.17 |
| 0x4F | R79 | | セクション 7.1.18 |
| 0x56 | R86 | | セクション 7.1.19 |
| 0x5A | R90 | | セクション 7.1.20 |

Complex bit access types are encoded to fit into small table cells. 表 7-2 shows the codes that are used for access types in this section.

**表 7-2. Device Access Type Codes**

| Access Type | Code | Description |
|---|---|---|
| Read Type | | |
| R | R | Read |
| Write Type | | |
| W | W | Write |
| Reset or Default Value | | |
| *-n* | | Value after reset or the default value |

### 7.1.1 R0 Register (Offset = 0x0) [Reset = 0x0000]

R0 is shown in 表 7-3.

Return to the Summary Table.

**表 7-3. R0 Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 15-3 | UNDISCLOSED | R | 0x0 | Program this field to 0x0. |
| 2 | POWERDOWN | R/W | 0x0 | Sets the device in a low-power state. The states of other registers are maintained. |
| 1-0 | UNDISCLOSED | R/W | 0x0 | Program this field to 0x0. |

### 7.1.2 R2 Register (Offset = 0x2) [Reset = 0x0223]

R2 is shown in 表 7-4.

Return to the Summary Table.

**表 7-4. R2 Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 15-11 | UNDISCLOSED | R | 0x0 | Program this field to 0x0. |
| 10-6 | UNDISCLOSED | R/W | 0x8 | Program this field to 0x8. |
| 5 | SMCLK_EN | R/W | 0x1 | Enables the state machine clock generator. This is required for pin modes to function correctly and the part must be initialized with this bit enabled. However, this bit can later on be disabled to save current and prevent the state machine clock spur. |
| 4-0 | UNDISCLOSED | R/W | 0x3 | Program this field to 0x3. |

### 7.1.3 R3 Register (Offset = 0x3) [Reset = 0xF0FE]

R3 is shown in 表 7-5.

Return to the Summary Table.

**表 7-5. R3 Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 15 | CLKOUT3_EN | R/W | 0x1 | Enables CLKOUT3 |
| 14 | CLKOUT2_EN | R/W | 0x1 | Enables CLKOUT2 |
| 13 | CLKOUT1_EN | R/W | 0x1 | Enables CLKOUT1 |
| 12 | CLKOUT0_EN | R/W | 0x1 | Enables CLKOUT0 |
| 11-0 | UNDISCLOSED | R/W | 0xFE | Program this field to 0xFE. |

### 7.1.4 R4 Register (Offset = 0x4) [Reset = 0x36FF]

R4 is shown in 表 7-6.

Return to the Summary Table.

**表 7-6. R4 Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 15-14 | UNDISCLOSED | R | 0x0 | Program this field to 0x0. |
| 13-11 | CLKOUT1_PWR | R/W | 0x6 | Sets the output power of CLKOUT1. Larger values correspond to higher output power. |
| 10-8 | CLKOUT0_PWR | R/W | 0x6 | Sets the output power of CLKOUT0. Larger values correspond to higher output power. |


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表 7-6. R4 Register Field Descriptions (続き)

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-0 | UNDISCLOSED | R/W | 0xFF | Program this field to 0xFF. |

### 7.1.5 R5 Register (Offset = 0x5) [Reset = 0x36F6]

R5 is shown in 表 7-7.

Return to the Summary Table.

表 7-7. R5 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 15 | UNDISCLOSED | R | 0x0 | Program this field to 0x0. |
| 14-6 | UNDISCLOSED | R/W | 0xDB | Program this field to 0xDB. |
| 5-3 | CLKOUT3_PWR | R/W | 0x6 | Sets the output power of CLKOUT3. Larger values correspond to higher output power. |
| 2-0 | CLKOUT2_PWR | R/W | 0x6 | Sets the output power of CLKOUT2. Larger values correspond to higher output power. |

### 7.1.6 R7 Register (Offset = 0x7) [Reset = 0x543F]

R7 is shown in 表 7-8.

Return to the Summary Table.

表 7-8. R7 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 15 | UNDISCLOSED | R | 0x0 | Program this field to 0x0. |
| 14-13 | UNDISCLOSED | R/W | 0x2 | Program this field to 0x2. |
| 12-11 | AUXCLKOUT_VCM | R/W | 0x2 | In LVDS mode, sets the output common mode of the auxiliary clock output. Other output formats ignore this field.<br>0x0 = 1.2V<br>0x1 = 1.1V<br>0x2 = 1.0V<br>0x3 = 0.9V |
| 10-9 | UNDISCLOSED | R/W | 0x2 | Program this field to 0x2. |
| 8-7 | AUXCLK_DIV_PWR_PRE | R/W | 0x0 | Sets the output power of the AUXCLK pre-driver. Larger values correspond to higher output power. |
| 6-4 | UNDISCLOSED | R/W | 0x3 | Program this field to 0x3. |
| 3-1 | AUXCLKOUT_PWR | R/W | 0x7 | Sets the output power of AYXCLKOUT for CML format only (other output formats ignore this field). Larger values correspond to higher output power. |
| 0 | UNDISCLOSED | R/W | 0x1 | Program this field to 0x1. |

### 7.1.7 R8 Register (Offset = 0x8) [Reset = 0x0120]

R8 is shown in 表 7-9.

Return to the Summary Table.

表 7-9. R8 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 15-9 | UNDISCLOSED | R | 0x0 | Program this field to 0x0. |

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**表 7-9. R8 Register Field Descriptions (続き)**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 8-6 | AUXCLK_DIV_PRE | R/W | 0x4 | Sets pre-divider value. Output of the pre-divider must be less than or equal to 3.2 GHz. When AUXCLK_DIV_PRE=1, register R79 is also required to be programmed to a value of 0x0005 and R90 to 0x0060 (AUXCLK_DIV_BYP2=1, AUXCLK_DIV_BYP3=1). Values for AUXCLK_DIV_PRE other than those listed below are reserved.<br>0x1 = /1<br>0x2 = /2<br>0x4 = /4 |
| 5 | AUXCLKOUT_EN | R/W | 0x1 | Enables AUXCLK subsystem. |
| 4-2 | UNDISCLOSED | R/W | 0x0 | Program this field to 0x0. |
| 1-0 | AUXCLKOUT_FMT | R/W | 0x0 | Selects the output driver format of the AUXCLKOUT output.<br>0x0 = LVDS<br>0x1 = Reserved<br>0x2 = CML<br>0x3 = Reserved |

### 7.1.8 R9 Register (Offset = 0x9) [Reset = 0x0020]

R9 is shown in 表 7-10.

Return to the Summary Table.

**表 7-10. R9 Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 15-14 | SYNC_VCM | R/W | 0x0 | Sets the internal DC Bias for the SYNC pins. Bias must be enabled for AC-coupled inputs; but can be enabled and overdriven, or disabled, for DC-coupled inputs. SYNC DC pin voltage must be in the range of 0.7 V to VCC, including minimum and maximum signal swing.<br>0x0 = 1.3V<br>0x1 = 1.1V<br>0x2 = 1.5V<br>0x3 = Disabled |
| 13 | SYNC_EN | R/W | 0x0 | Enables synchronization path for the dividers and allows the clock position capture circuitry to be enabled. Used for multi-device synchronization. |
| 12 | UNDISCLOSED | R/W | 0x0 | Program this field to 0x0. |
| 11 | AUXCLK_DIV_BYP | R/W | 0x0 | Bypasses the AUXCLK_DIV divider to derive the AUXCLK output directly from the AUXCLK_DIV_PRE divider. Use only when AUXCLK_DIV_PRE=1 as one of the steps to achieve a total divide of 1 for the AUXCLK. To achieve a divide by 1, the following steps are required.<br>1. Set AUXCLK_DIV_PRE=1<br>2. Verify that register R79 is programmed to a value of 0x0005<br>3. Program R90 to 0x0060 (AUXCLK_DIV_BYP2=1, AUXCLK_DIV_BYP3=1)<br>4. Set AUXCLK_DIV_BYP=1<br>If a total divide of 1 for the AUXCLK is undesired, set this bit to 0. |
| 10 | UNDISCLOSED | R/W | 0x0 | Program this field to 0x0. |
| 9-0 | AUXCLK_DIV | R/W | 0x20 | Sets AUXCLK divider value. Maximum input frequency from AUXCLK_DIV_PRE must be ≤ 3200 MHz. The maximum AUXCLKOUT frequency must be ≤ 800 MHz to avoid amplitude degradation.<br>0x0 = Reserved<br>0x1 = Reserved<br>0x2 = /2<br>0x3 = /3<br>0x3FF = /1023 |


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### 7.1.9 R11 Register (Offset = 0xB) [Reset = 0x0000]

R11 is shown in 表 7-11.

Return to the Summary Table.

**表 7-11. R11 Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 15-0 | rb_CLKPOS | R | 0x0 | Stores a snapshot of the CLKIN signal rising edge positions relative to a SYNC rising edge, with the snapshot starting from the LSB and ending at the MSB. Each bit represents a sample of the CLKIN signal, separated by a delay determined by the SYNC_DLY_STEP field. The first and last bits of rb_CLKPOS are always set, indicating uncertainty at the capture window boundary conditions. CLKIN rising edges are represented by every sequence of two set bits from LSB to MSB, including bits at the boundary conditions. The position of the CLKIN rising edges in the snapshot, along with the CLKIN signal period and the delay step size, can be used to compute the value of SYNC_DLY which maximizes setup and hold times for SYNC signals on the SYNC pins. |

### 7.1.10 R12 Register (Offset = 0xC) [Reset = 0x0000]

R12 is shown in 表 7-12.

Return to the Summary Table.

**表 7-12. R12 Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 15-0 | rb_CLKPOS[31:16] | R | 0x0 | MSB of rb_CLKPOS field. |

### 7.1.11 R13 Register (Offset = 0xD) [Reset = 0x0003]

R13 is shown in 表 7-13.

Return to the Summary Table.

**表 7-13. R13 Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 15-2 | UNDISCLOSED | R | 0x0 | Program this field to 0x0. |
| 1-0 | SYNC_DLY_STEP | R/W | 0x3 | Sets the step size of the delay element used in the SYSNC path, both for SYNC input delay and for clock position captures. The recommended frequency range for each step size creates the maximum number of usable steps for a given CLKIN frequency. The ranges include some overlap to account for process and temperature variations. If the CLKIN frequency is covered by an overlapping span, larger delay step sizes improve the likelihood of detecting a CLKIN rising edge during a clock position capture. However, since larger values include more delay steps, larger step sizes have greater total delay variation across PVT relative to smaller step sizes.<br>0x0 = 28 ps (1.4GHz to 2.7GHz)<br>0x1 = 15 ps ( 2.4GHz to 4.7GHz)<br>0x2 = 11 ps (3.1GHz to 5.7GHz)<br>0x3 = 8 ps (4.5GHz to 12.8GHz) |

### 7.1.12 R14 Register (Offset = 0xE) [Reset = 0x0002]

R14 is shown in 表 7-14.

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Return to the Summary Table.

**表 7-14. R14 Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 15-3 | UNDISCLOSED | R/W | 0x0 | Program this field to 0x0. |
| 2 | CLKPOS_CAPTURE_EN | R/W | 0x0 | Enables the windowing circuit which captures the clock position in the rb_CLKPOS registers with respect to a SYNC edge. The windowing circuit must be cleared by toggling SYNC_CLR high then low before a clock position capture. The first rising edge on the SYNC pins after clearing the windowing circuit triggers the capture. The capture circuitry greatly increases supply current, and does not need to be enabled to delay the SYNC signal in SYNC mode. Once the desired value of SYNC_DLY is determined, set this bit to 0x0 to minimize current consumption. If SYNC_EN = 0, the value of this bit is ignored, and the windowing circuit is disabled. |
| 1 | UNDISCLOSED | R/W | 0x1 | Program this field to 0x1. |
| 0 | SYNC_LATCH | R/W | 0x0 | Latches the internal SYNC state to logic high on the first rising edge of the SYNC pins. This latch can be cleared by setting SYNC_CLR=1. |

### 7.1.13 R15 Register (Offset = 0xF) [Reset = 0x0B01]

R15 is shown in 表 7-15.

Return to the Summary Table.

**表 7-15. R15 Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 15-12 | UNDISCLOSED | R | 0x0 | Program this field to 0x0. |
| 11-7 | UNDISCLOSED | R/W | 0x16 | Program this field to 0x16. |
| 6-1 | SYNC_DLY | R/W | 0x0 | Sets the delay line step for the external SYNC signal. Each delay line step delays the SYNC signal by an amount equal to SYNC_DLY_STEP x SYNC_DLY_STEP. In SYNC mode, the value for this field can be determined based on the rb_CLKPOS value to satisfy the internal setup and hold time of the SYNC signal with respect to the CLKIN signal. In SYSREF Repeater Mode, the value for this field can be used as a coarse global delay. Values greater than 0x3F are invalid. Since larger values include more delay steps, larger values have greater total step size variation across PVT relative to smaller values. Refer to the data sheet or the device TICS Pro profile for detailed description of the delay step computation procedure. |
| 0 | SYNC_CLR | R/W | 0x1 | Clears SYNC_LATCH and resets synchronization path timing for SYNC signal. Holding this bit high keeps internal SYNC signal low. This bit must be set and cleared once before the SYNC or clock position capture operations are performed. |

### 7.1.14 R23 Register (Offset = 0x17) [Reset = 0x4000]

R23 is shown in 表 7-16.

Return to the Summary Table.

**表 7-16. R23 Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 15 | TS_EN | R/W | 0x0 | Enables the on-die temperature sensor. Temperature sensor counter (TS_CNT_EN) must also be enabled for readback. |
| 14 | UNDISCLOSED | R/W | 0x1 | Program this field to 0x1. |


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表 7-16. R23 Register Field Descriptions (続き)

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 13 | MUXOUT_EN | R/W | 0x0 | Enables or tri-states the MUXOUT pin driver.<br>0x0 = Tri-States<br>0x1 = Push-Pull |
| 12-0 | UNDISCLOSED | R/W | 0x0 | Program this field to 0x0. |

### 7.1.15 R24 Register (Offset = 0x18) [Reset = 0x0000]

R24 is shown in 表 7-17.

Return to the Summary Table.

表 7-17. R24 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 15-14 | UNDISCLOSED | R | 0x0 | Program this field to 0x0. |
| 13-12 | UNDISCLOSED | R/W | 0x0 | Program this field to 0x0. |
| 11-1 | rb_TS | R | 0x0 | Readback value of on-die temperature sensor. |
| 0 | TS_CNT_EN | R/W | 0x0 | Enables temperature sensor counter. Temperature sensor (TS_EN) must be enabled for accurate data. |

### 7.1.16 R25 Register (Offset = 0x19) [Reset = 0x0211]

R25 is shown in 表 7-18.

Return to the Summary Table.

表 7-18. R25 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 15-7 | UNDISCLOSED | R/W | 0x4 | Program this field to 0x4. |
| 6 | CLK_DIV_RST | R/W | 0x0 | Resets the main clock divider. If the clock divider value is changed during operation, set this bit high then low after setting the new divider value. Synchronizing the device with the SYNC pins with SYNC_EN = 0x1 also resets the main clock divider. This bit has no effect when outside of Divider Mode. |
| 5-3 | CLK_DIV | R/W | 0x2 | Sets the clock divider value when CLK_MUX=2 (Divider Mode). The clock divider value is CLK_DIV+1. Valid value for CLK_DIV is 1 to 7. Setting this to 0 disables the main clock divider and reverts to buffer mode. |
| 2-0 | CLK_MUX | R/W | 0x1 | Selects the function for the main clock outputs<br>0x0 = Reserved<br>0x1 = Buffer<br>0x2 = Divider<br>0x3 = Reserved |

### 7.1.17 R75 Register (Offset = 0x4B) [Reset = 0x0006]

R75 is shown in 表 7-19.

Return to the Summary Table.

表 7-19. R75 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 15 | rb_CLKOUT2_EN | R | 0x0 | Readback Pin Status |
| 14 | rb_CLKOUT1_EN | R | 0x0 | Readback Pin Status |

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**表 7-19. R75 Register Field Descriptions (続き)**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 13 | rb_CLKOUT0_EN | R | 0x0 | Readback Pin Status |
| 12 | rb_MUXSEL1 | R | 0x0 | Readback Pin Status |
| 11-7 | UNDISCLOSED | R | 0x0 | Program this field to 0x0. |
| 6 | rb_DIVSEL1 | R | 0x0 | Readback Pin Status |
| 5 | rb_DIVSEL0 | R | 0x0 | Readback Pin Status |
| 4 | rb_CE | R | 0x0 | Readback Pin Status |
| 3-0 | UNDISCLOSED | R/W | 0x6 | Program this field to 0x6. |

### 7.1.18 R79 Register (Offset = 0x4F) [Reset = 0x0205]

R79 is shown in 表 7-20.

Return to the Summary Table.

**表 7-20. R79 Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 15 | UNDISCLOSED | R | 0x0 | Program this field to 0x0. |
| 14-0 | UNDISCLOSED | R/W | 0x205 | Program this field to 0x5. Note that this is different than the reset value. |

### 7.1.19 R86 Register (Offset = 0x56) [Reset = 0x0000]

R86 is shown in 表 7-21.

Return to the Summary Table.

**表 7-21. R86 Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 15-3 | UNDISCLOSED | R/W | 0x0 | Program this field to 0x0. |
| 2 | MUXOUT_EN_OVRD | R/W | 0x0 | This bit must be set to 1 to enable MUXOUT_EN to tri-state the MUXOUT pin. |
| 1-0 | UNDISCLOSED | R/W | 0x0 | Program this field to 0x0. |

### 7.1.20 R90 Register (Offset = 0x5A) [Reset = 0x0000]

R90 is shown in 表 7-22.

Return to the Summary Table.

**表 7-22. R90 Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 15-8 | UNDISCLOSED | R | 0x0 | Program this field to 0x0. |
| 7 | UNDISCLOSED | R/W | 0x0 | Program this field to 0x0. |
| 6 | AUXCLK_DIV_BYP3 | R/W | 0x0 | Set this bit to 1 if AUXCLK_BYP=1, set to 0 otherwise. |
| 5 | AUXCLK_DIV_BYP2 | R/W | 0x0 | Set this bit to 1 if AUXCLK_BYP=1, set to 0 otherwise. |
| 4-0 | UNDISCLOSED | R/W | 0x0 | Program this field to 0x0. |


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# 8 Application and Implementation

注

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## 8.1 Application Information

### *8.1.1 SYNC Input Configuration*

The SYNC pins support single-ended or differential input in AC or DC coupling mode. The SYNC pins have an internal 50-Ω termination with capacitive ground, which acts as 100-Ω differential.

図 8-1 shows the generic SYNC input circuit recommendation to support all AC or DC, single-ended or differential inputs. Some of the discrete components in fig are just placeholder for individual input signal (single-ended or differential input) and AC or DC coupled input.

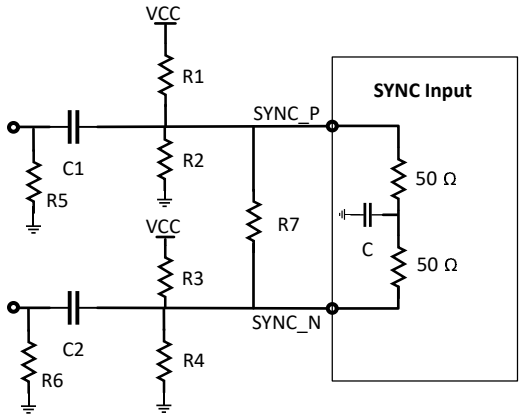



**図 8-1. SYNC Input Circuit Recommendations**

The following figures show the individual circuit diagram for each configurations:

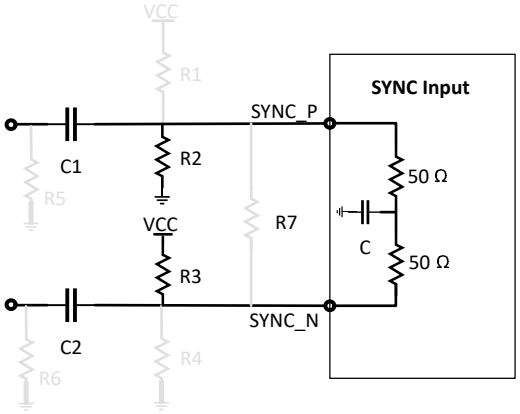



**図 8-2. AC-Coupled Differential Input**

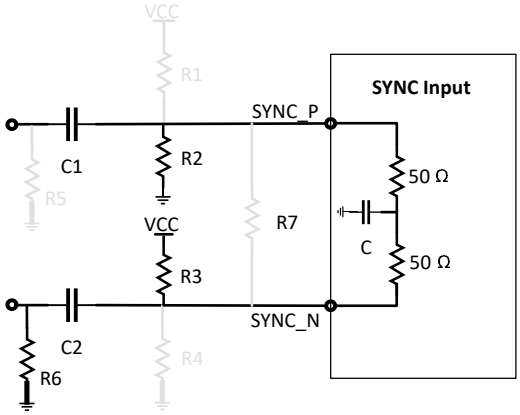



**図 8-3. AC-Coupled, Single-Ended Input**

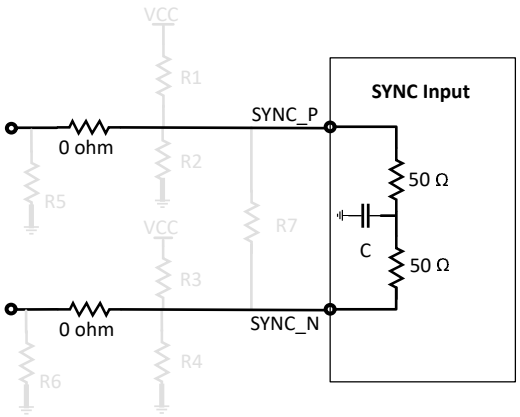



**図 8-4. DC-Coupled Differential Input**

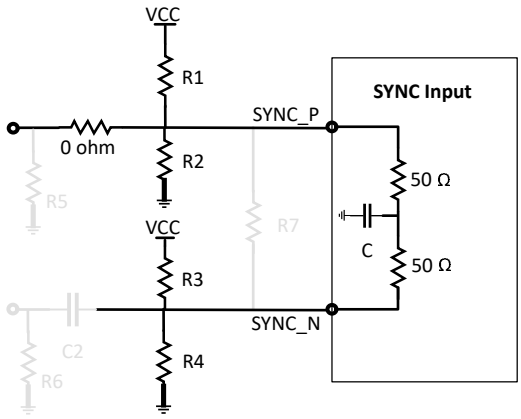



**図 8-5. DC-Coupled, Single-Ended Input**

1. AC coupled differential and single-ended input configurations required the resistor terminations (R2 and R3) to create the VCM at each pin and resistor values must select to maintain greater than 150-mV potential difference between pin P and pin N.
   a. As an example, to create the VCM of 1.5 V at pin P and 1.65 V at pin N, with the 2.5 V VCC, set R3 = 550 Ω and R2 = 1 kΩ.
   b. For single-ended input configuration, place R6 = 50 Ω to avoid any reflection at complementary input pin.
2. DC coupled differential and single-ended input configuration required to have the source common-mode voltage matched with the device input common mode specifications.
   a. For single-ended input configuration, keep the R1, R2, R3 and R4 resistors. This method creates the same common-mode voltage at both pins, and the resistive dividers create 75 Ω at pin P and 50-Ω Thevenin's equivalent at pin N.
   b. As an example, to have the common-mode voltage of 1.35 V at each pin, set the resistive divider components values to R1 = 130 Ω, R2 = 165 Ω, R3 = 86.6 Ω and R4 = 110 Ω with the 2.5-V VCC.

### *8.1.2 Treatment of Unused Pins*

In many cases, not all pins are used. 表 8-1 lists the recommendations on how to handle these unused pins.

**表 8-1. Treatment of Unused or Partially Used Pins**

| PINS | TREATMENT |
|---|---|
| All VCC Pins | These pins must always be connected to the power supply. If the block that powers these VCC pins (as implied by the pin name) is not used, then the bypassing can be minimized or eliminated. |
| SYNC_P / SYNC_N | 1. If driving single-ended input, the complementary input must terminates based on セクション 8.1.1<br>2. If the SYNC pins are unused,tie the pins to the VCC with 1-kΩ resistor. |
| CLKIN_P / CLKIN_N | If driving single-ended input, the complementary input must have an AC-coupling capacitor and 50 Ω to ground. |
| CLKOUTx_P / CLKOUTx_N | If not used, connect a AC-coupling capacitor and 50 Ω to ground. |
| AUXCLKOUT_P / AUXCLKOUT_N | If these pins are unused, connect the pins to ground with a 1-kΩ resistor. |
| CLKx_EN | 1. If operating device in SPI controlled mode, these pins must tied to VCC with 1-kΩ resistor.<br>2. If the respective output channels are not using. the pins must connect to ground with 1-kΩ resistor. |
| MUXSEL, DIVSELx | If these pins are unused, connect these pins to ground with a 1-kΩ resistor. |


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### 8.1.3 Current Consumption

The current consumption varies as a function of the setup condition. By adding up all the block currents shown in 表 8-2 users can obtain a reasonable estimate of the current for any setup condition.

**表 8-2. Current Consumption per Block**

| BLOCK | | CONDITIONS | | CURRENT (mA) |
|---|---|---|---|---|
| Device Core | | CLK_MUX = Buffer Mode | | 294 |
| | | CLK_MUX = Divide Mode | | 260 |
| SYNC Windowing | Windowing Circuitry | Windowing Circuitry (CLKPOS_CAPTURE_EN=1) | | 113 |
| CLKOUT (Per active clock channel) | Core | | | 25 |
| | Output Buffer | CLKOUTx_EN=1 | | 4+6*CLKOUTx_PWR |
| AUXCLKOUT | Core | AUXCLKOUT_EN=1 | | 49 |
| | Output Buffer | | CML($R_P$=50Ω) | 16+1*AUXCLKOUT_PWR |
| | | | LVDS | 12 |

## 8.2 Typical Application

This application shows the low additive noise impact of LMX1214, when the source LMX2820 exports the 6000-MHz clock output to LMX1214 for local oscillator distribution. This particular setup used a single-ended clock to drive the LMX1214 for the sake of simplicity of connecting two EVMs together, but driving the device differentially is generally recommended.

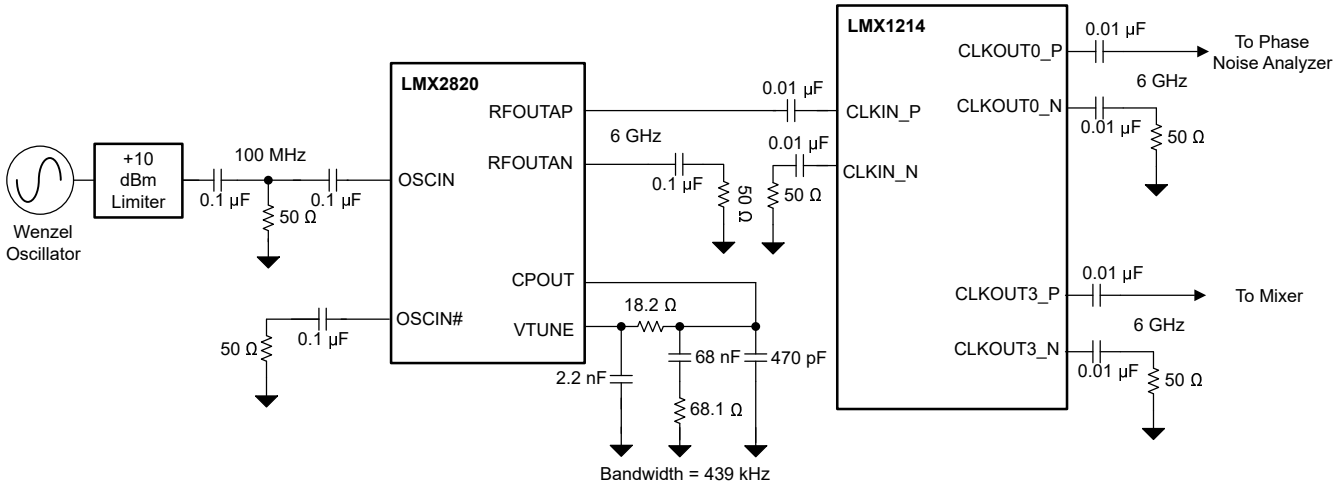



**図 8-6. Typical Application Schematic**

### 8.2.1 Design Requirements

Design Parameters shows the design parameters for this example.

If not all outputs are used, TI recommends to compress the layout to minimize trace lengths, especially that of the input trace.

**表 8-3. Design Parameters**

| PARAMETER | VALUE |
|---|---|
| LMX2820 Input Frequency | 100-MHz |
| LMX2820 Output Frequency | 6000-MHz |
| LMX1214 Input Clock Frequency | 6000-MHz |
| LMX1214 Output Clock Frequency | 6000-MHz |
| LMX1214 | Buffer Mode |

### 8.2.2 Detailed Design Procedure

In this example, a 6000-MHz input clock is bypassed to a 6000-MHz output clock. The external components do not change that much based on internal configuration. The TICS Pro software is very useful in calculating the necessary register values and configuring the device.

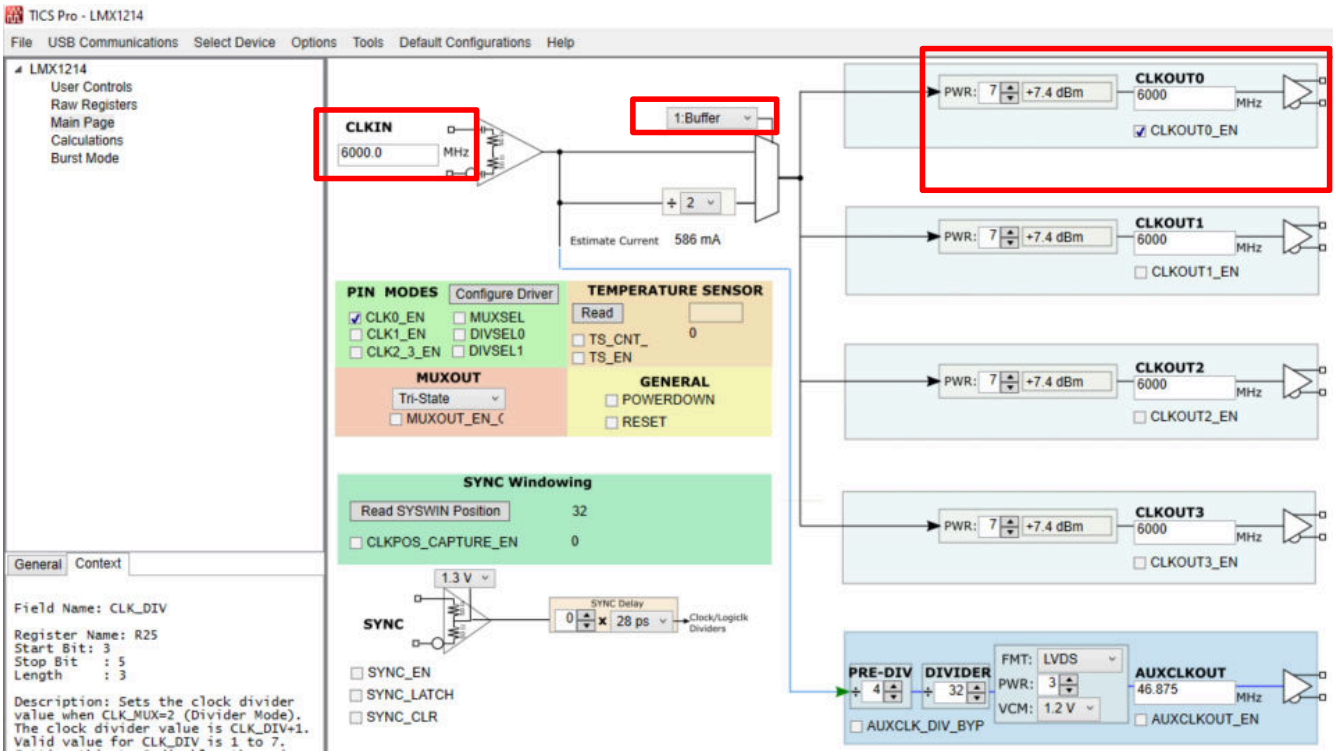



**図 8-7. LMX1214 TICS Pro Setup**


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### 8.2.3 Application Plots

図 8-8 the total plot is the sum of the noise of the LMX1214 buffer mode noise and the LMX2820 6000-MHz output. Note that the LMX1214 follow the same noise curve of LMX2820.

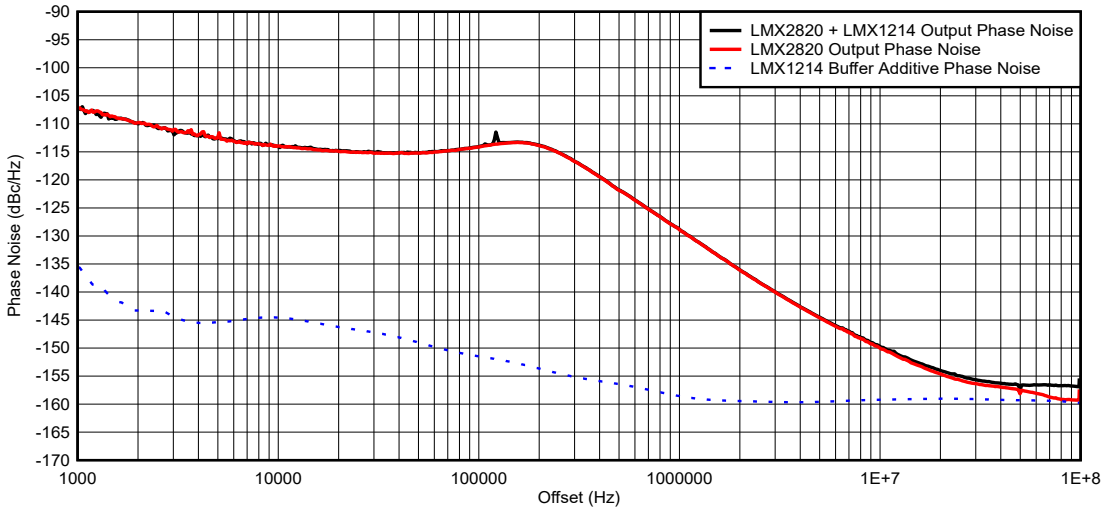



**図 8-8. LMX1214 Buffer Output**

## 8.3 Power Supply Recommendations

This devices uses a 2.5-V supply for the whole device. A direct connection to a switching power supply likely results in unwanted spurs at the output. Bypassing can be done individually at all the power pins. TI recommends placing smaller capacitors with higher frequency of minimum impedance on the same layer as the device, as close to the pins as possible. The frequencies of nearly all signals in the device are 100 MHz or greater, therefore larger value bypass capacitors with low frequency of minimum impedance are only used for internal LDO stability, and the distance to the device (and the loop inductance of the bypass path) can be larger. Isolate the supply pins for the clocks and the AUXCLKOUT with a small resistor or ferrite bead if both are being used simultaneously. See the *Pin Configuration and Functions* section for additional recommendations for each pin.

注

**This device has minimal PSRR due to the low operating voltage and internal filtering by LDOs. Verifying that this device is connected to a low noise supply that does not have excessive spurious noise is important.**

## 8.4 Layout

### 8.4.1 Layout Guidelines

- If using a single-ended output, terminate the complementary side with AC coupled to 50 Ω so that the impedance for the signal output is same as complementary pin side.
- GND pins on the outer perimeter of the package can be routed on the package back to the DAP.
- Minimize the length of the CLKIN trace for optimal phase noise. Poor matching can degrade the noise floor.
- Verify that the DAP on the device is well-grounded with many vias.
- Use a low loss dielectric material, such as Rogers 4350B, for optimal output power.
- Be aware that if all the outputs are enabled, the current consumption can be high enough to exceed the recommended internal junction temperature of 125°C; a heat sink can be necessary.

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### 8.4.2 Layout Example

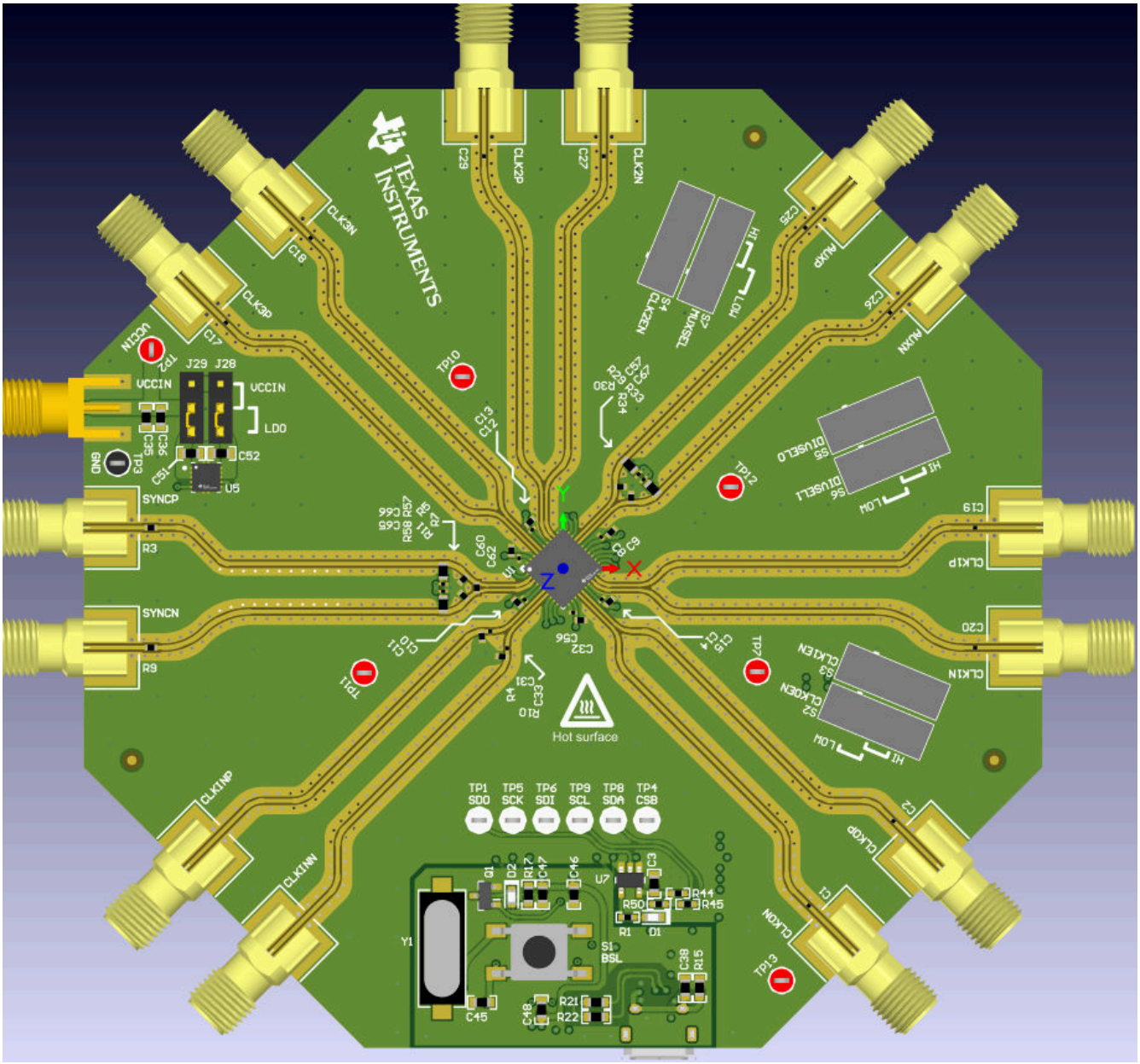



**図 8-9. Layout Example**

## 9 Device and Documentation Support

### 9.1 Device Support

TI offers an extensive line of development tools and software to simulate the device performance and program the device.

**表 9-1. Development Tools and Software**

| TOOL | TYPE | DESCRIPTION |
|---|---|---|
| PLLatinum™ Sim | Software | Simulates phase noise in all modes |


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表 9-1. Development Tools and Software (続き)

| TOOL | TYPE | DESCRIPTION |
|---|---|---|
| TICS Pro | Software | Programs the device with a user-friendly GUI with interactive feedback and hex register export. |

## 9.2 Documentation Support

### 9.2.1 Related Documentation

Texas Instruments, *LMX1214 Evaluation Module*, EVM user's guide

## 9.3 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、www.tij.co.jp のデバイス製品フォルダを開いてください。[通知] をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取ることができます。 変更の詳細については、改訂されたドキュメントに含まれている改訂履歴をご覧ください。

## 9.4 サポート・リソース

テキサス・インスツルメンツ E2E™ サポート・フォーラムは、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計で必要な支援を迅速に得ることができます。

リンクされているコンテンツは、各寄稿者により「現状のまま」提供されるものです。これらはテキサス・インスツルメンツの仕様を構成するものではなく、必ずしもテキサス・インスツルメンツの見解を反映したものではありません。テキサス・インスツルメンツの使用条件を参照してください。

## 9.5 Trademarks

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すべての商標は、それぞれの所有者に帰属します。

## 9.6 静電気放電に関する注意事項



この IC は、ESD によって破損する可能性があります。テキサス・インスツルメンツは、IC を取り扱う際には常に適切な注意を払うことを推奨します。正しい取り扱いおよび設置手順に従わない場合、デバイスを破損するおそれがあります。

ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

## 9.7 用語集

テキサス・インスツルメンツ用語集　　この用語集には、用語や略語の一覧および定義が記載されています。

# 10 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

| Changes from Revision * (December 2023) to Revision A (August 2024) | Page |
|---|---|
| • バッファおよびデバイダ モードの出力の最大周波数を、それぞれ 18GHz と 8GHz に変更 | 1 |
| • ドキュメント全体にわたって表、図、相互参照の採番方法を更新 | 1 |
| • Changed max. input frequency spec to 18GHz in buffer mode in *Electrical Characteristics clock input* section | 5 |
| • Added output frequency spec in divider-by-2 without sync in *Electrical Characteristics Clock Outputs* section | 5 |
| • Changed max. output frequency spec to 18GHz in buffer mode in *Electrical Characteristics Clock Outputs* section | 5 |
| • Changed output power value in *Electrical Characteristics Clock Outputs* section | 5 |
| • Test conditions added in *Electrical Characteristics leakage power spec* | 5 |
| • Test conditions added in *Electrical Characteristics leakage power spec* | 5 |

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- Updated the *LMX1214 Flicker Noise at 6 GHz* and *Noise Floor in Buffer Mode* figures.....9
- added LMX1214 evaluation module user's guide link in Related Documentation.....35

## 11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

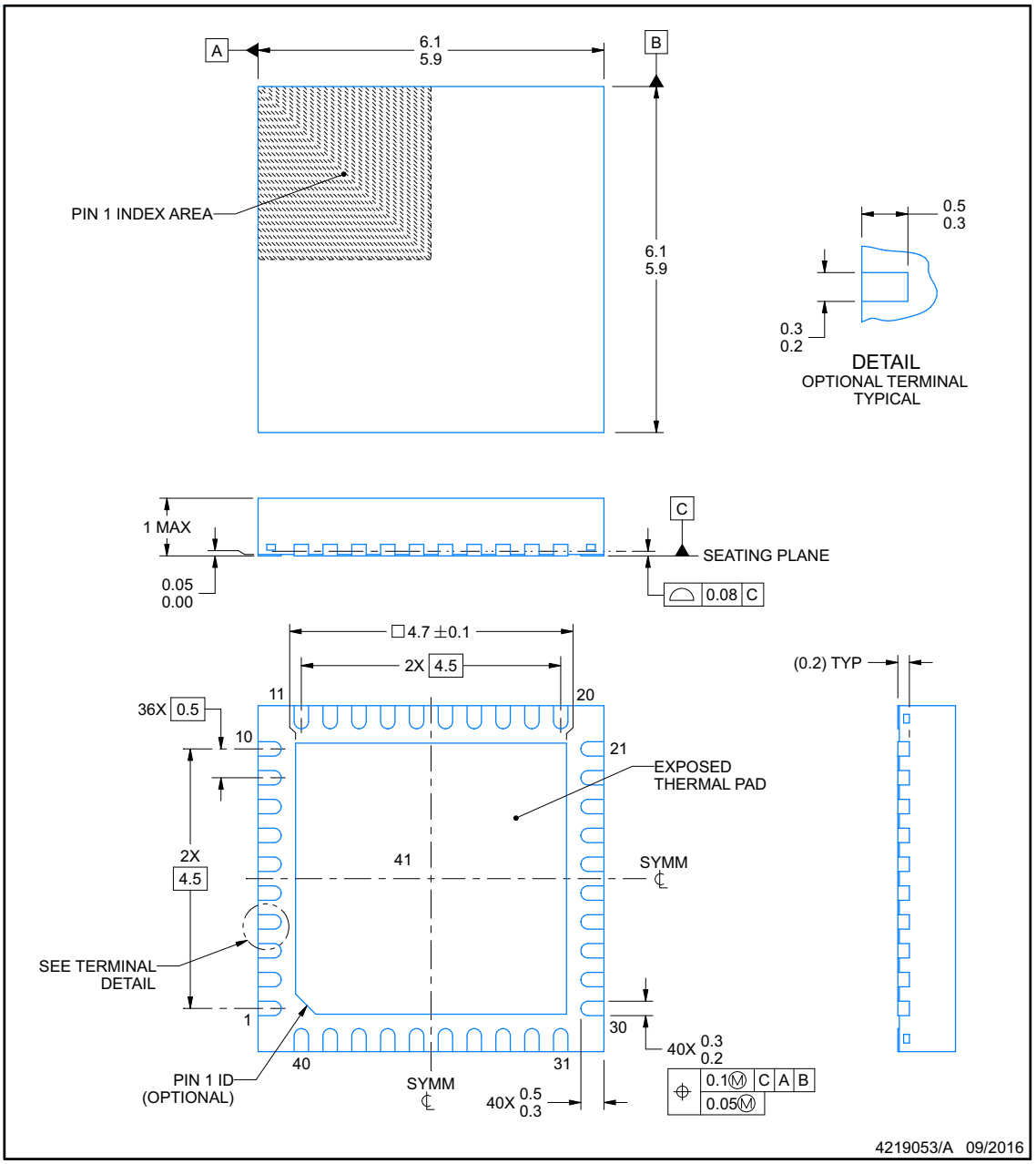

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# PACKAGE OUTLINE

## RHA0040C

## VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD




NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



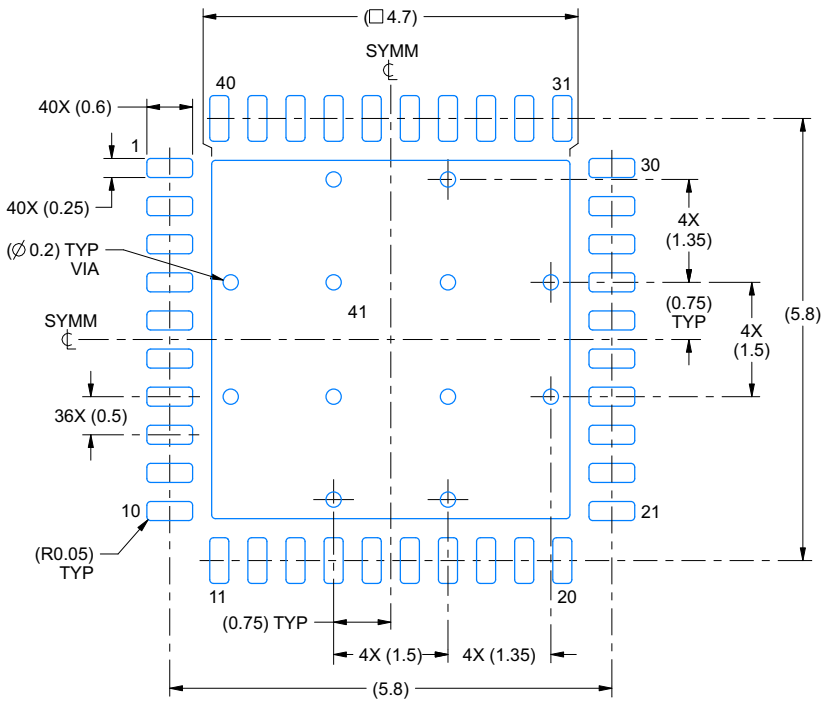
Copyright © 2024 Texas Instruments Incorporated

# EXAMPLE BOARD LAYOUT

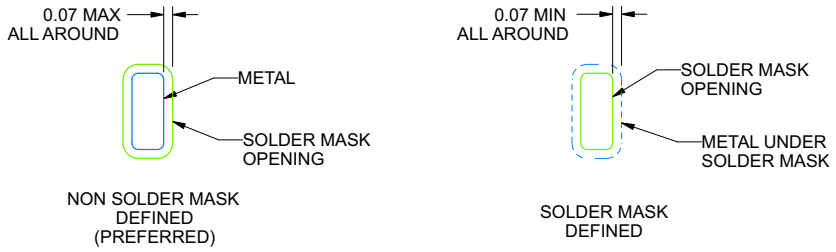
## RHA0040C

### VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD




LAND PATTERN EXAMPLE
SCALE:12X




SOLDER MASK DETAILS

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NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

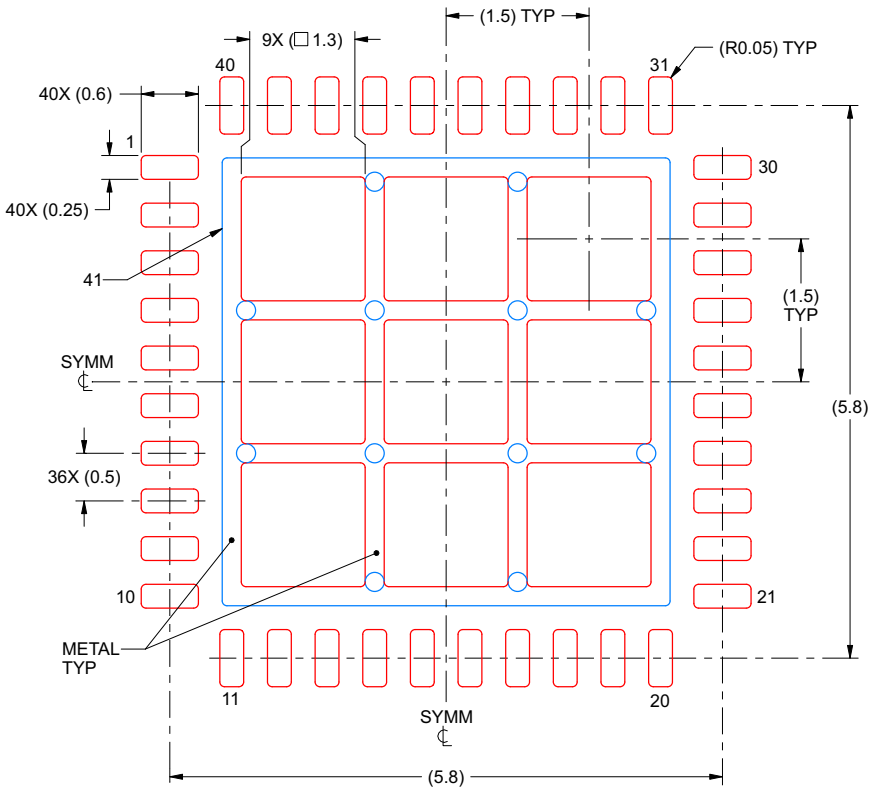

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# EXAMPLE STENCIL DESIGN

## RHA0040C

**VQFN - 1 mm max height**

PLASTIC QUAD FLATPACK - NO LEAD




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 41:
69% PRINTED SOLDER COVERAGE BY AREA
SCALE:15X

4219053/A 09/2016

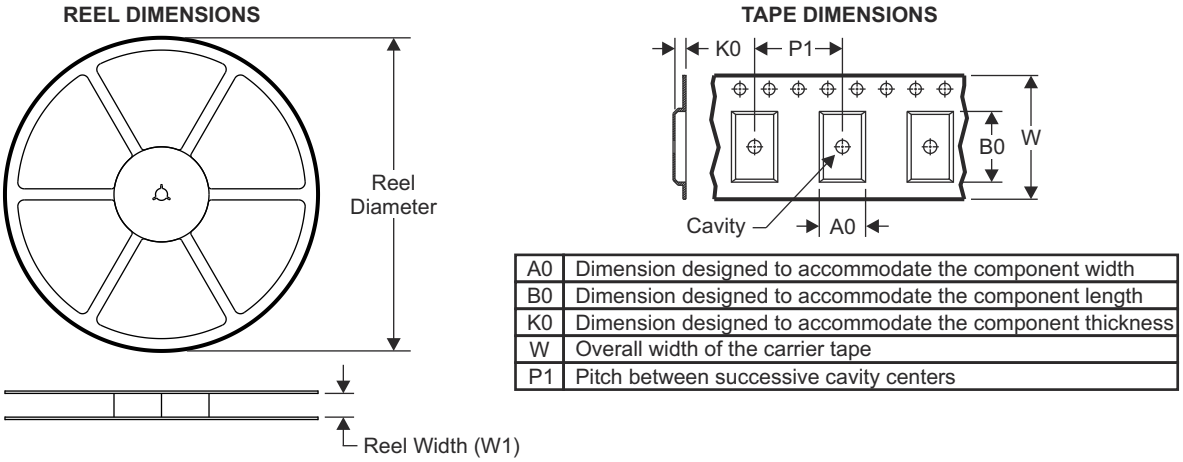
NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

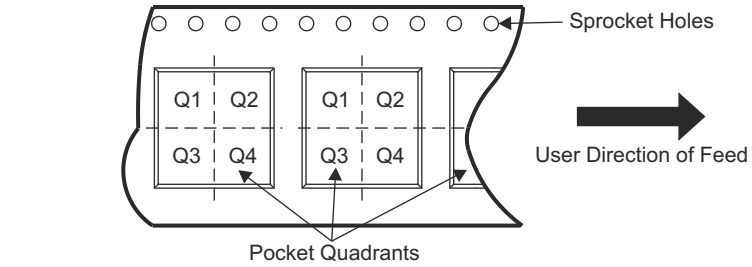


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## 11.1 Tape and Reel Information



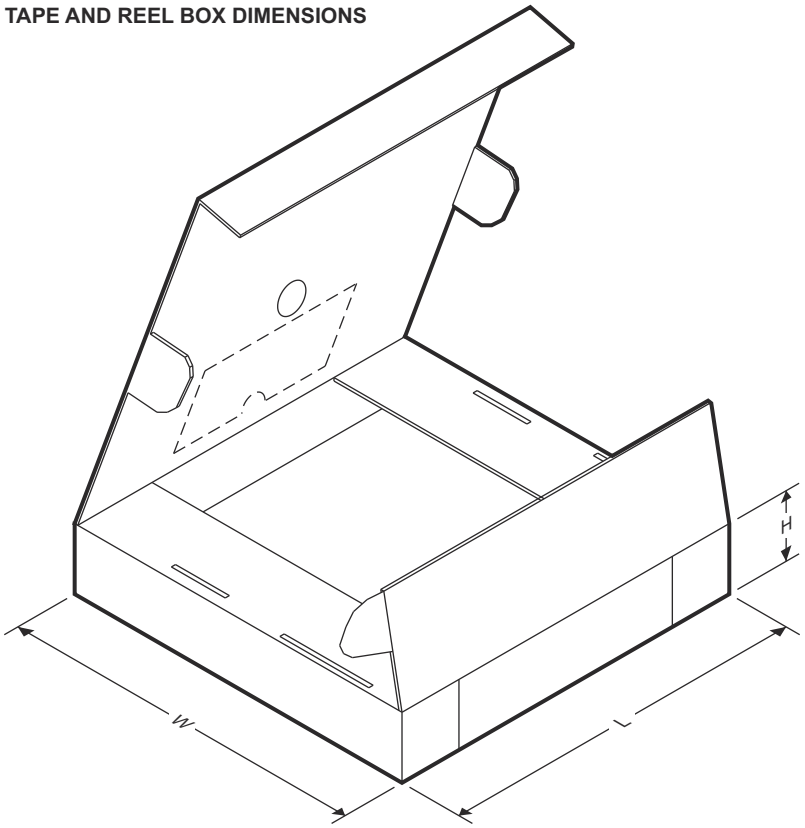

| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |




| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| MX1214RHAR | VQFN | RHA | 40 | 2500 | 330 | 16.4 | 6.3 | 6.3 | 1.1 | 12 | 16 | Q2 |
| LMX1214RHAT | VQFN | RHA | 40 | 250 | 180 | 16.4 | 6.3 | 6.3 | 1.1 | 12 | 16 | Q2 |


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**TAPE AND REEL BOX DIMENSIONS**




| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| LMX1214RHAR | VQFN | RHA | 40 | 2500 | 367 | 367 | 38 |
| LMX1214RHAT | VQFN | RHA | 40 | 250 | 210 | 185 | 35 |

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## PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package \| Pins | Package qty \| Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|---|---|---|---|---|---|---|---|---|---|
| LMX1214RHAR | Active | Production | VQFN (RHA) \| 40 | 2500 \| LARGE T&R | Yes | NIPDAUAG | Level-3-260C-168 HR | -40 to 85 | LMX1214 |
| LMX1214RHAR.A | Active | Production | VQFN (RHA) \| 40 | 2500 \| LARGE T&R | Yes | NIPDAUAG | Level-3-260C-168 HR | -40 to 85 | LMX1214 |
| LMX1214RHAT | Active | Production | VQFN (RHA) \| 40 | 250 \| SMALL T&R | Yes | NIPDAUAG | Level-3-260C-168 HR | -40 to 85 | LMX1214 |
| LMX1214RHAT.A | Active | Production | VQFN (RHA) \| 40 | 250 \| SMALL T&R | Yes | NIPDAUAG | Level-3-260C-168 HR | -40 to 85 | LMX1214 |

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

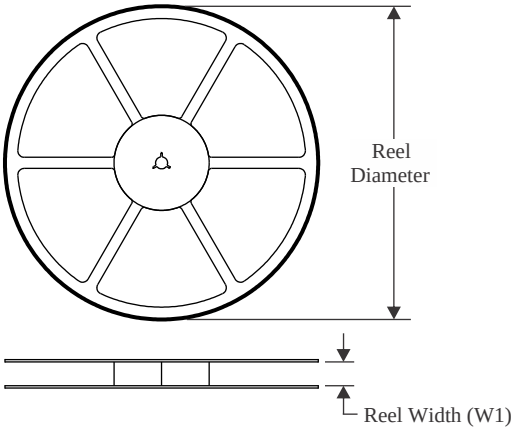
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

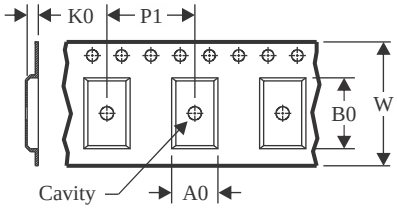
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## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

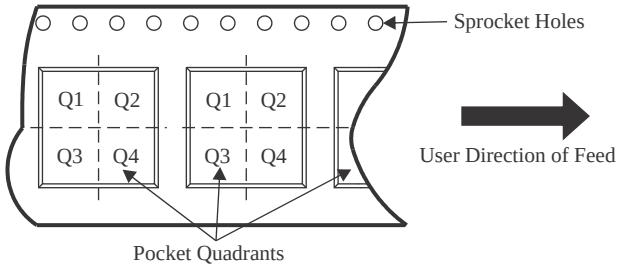



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

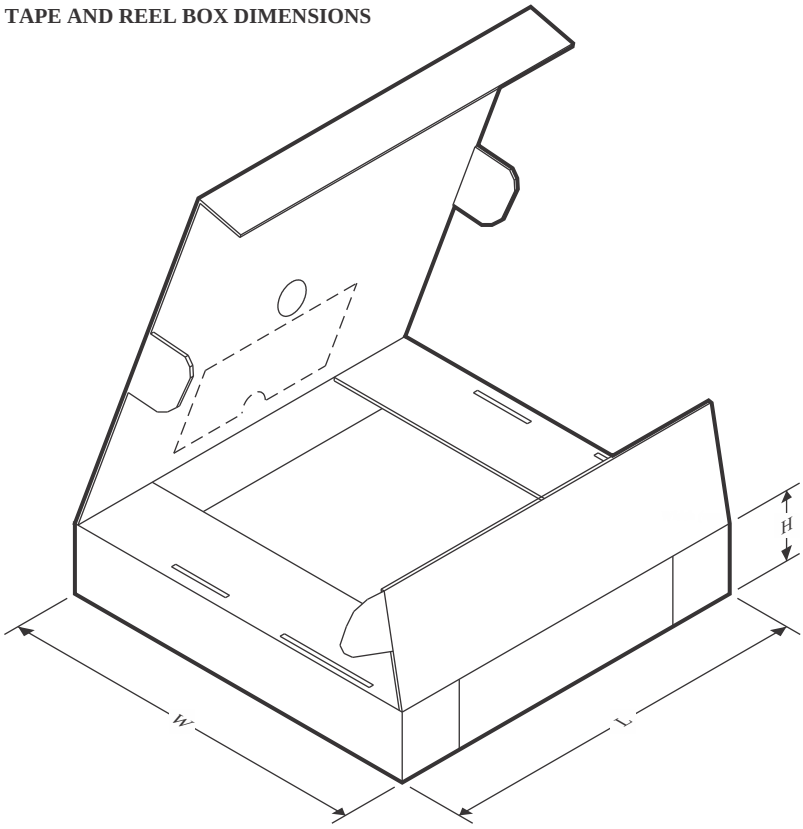
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| LMX1214RHAR | VQFN | RHA | 40 | 2500 | 330.0 | 16.4 | 6.3 | 6.3 | 1.1 | 12.0 | 16.0 | Q2 |
| LMX1214RHAT | VQFN | RHA | 40 | 250 | 180.0 | 16.4 | 6.3 | 6.3 | 1.1 | 12.0 | 16.0 | Q2 |

TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| LMX1214RHAR | VQFN | RHA | 40 | 2500 | 367.0 | 367.0 | 38.0 |
| LMX1214RHAT | VQFN | RHA | 40 | 250 | 210.0 | 185.0 | 35.0 |

# GENERIC PACKAGE VIEW

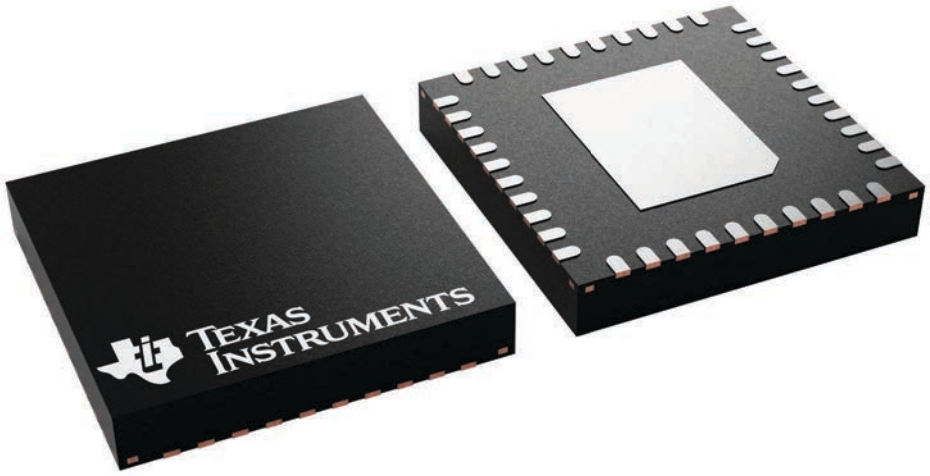
## RHA 40

## VQFN - 1 mm max height

**6 x 6, 0.5 mm pitch**

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



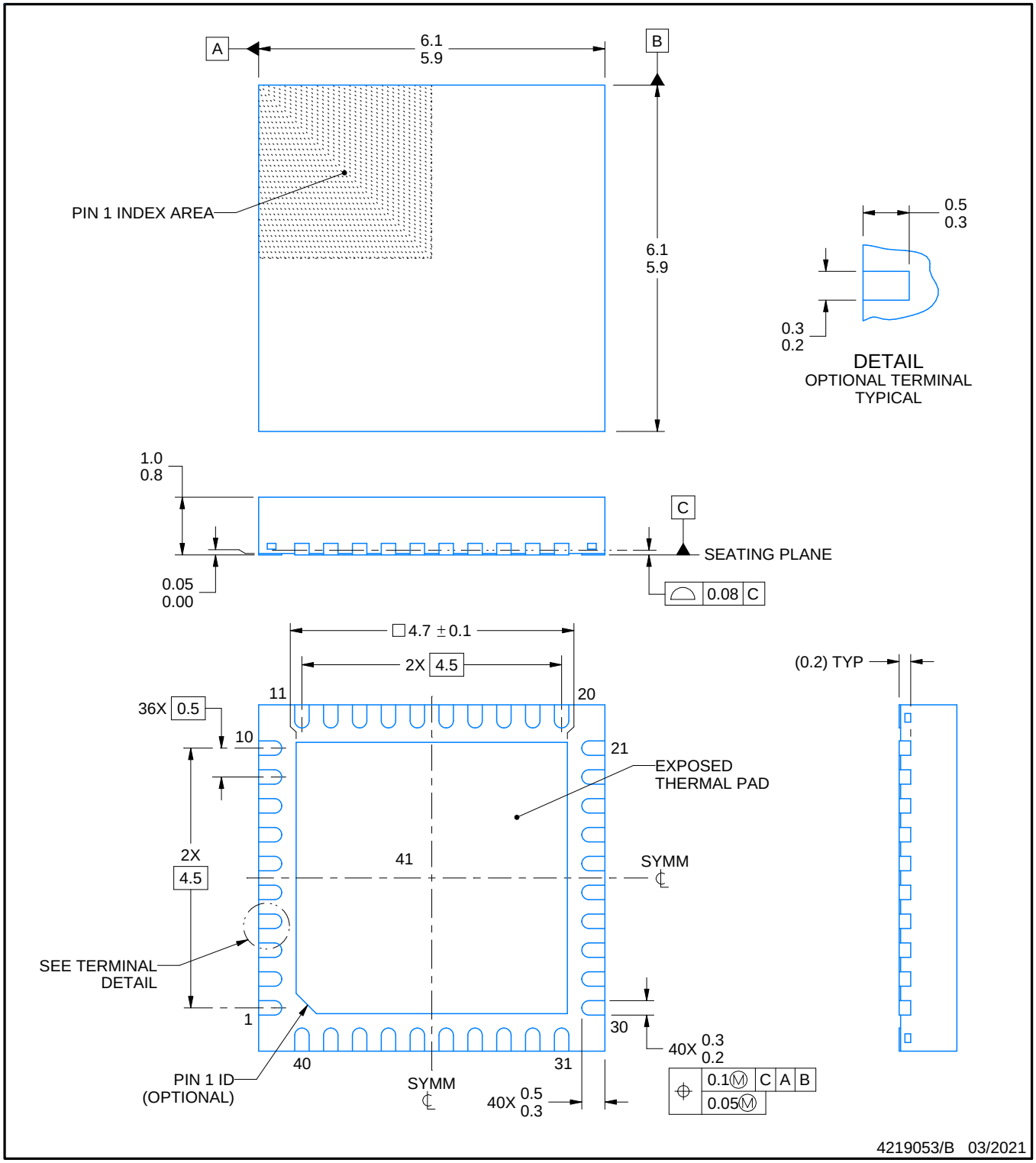

4225870/A

# RHA0040C

# PACKAGE OUTLINE

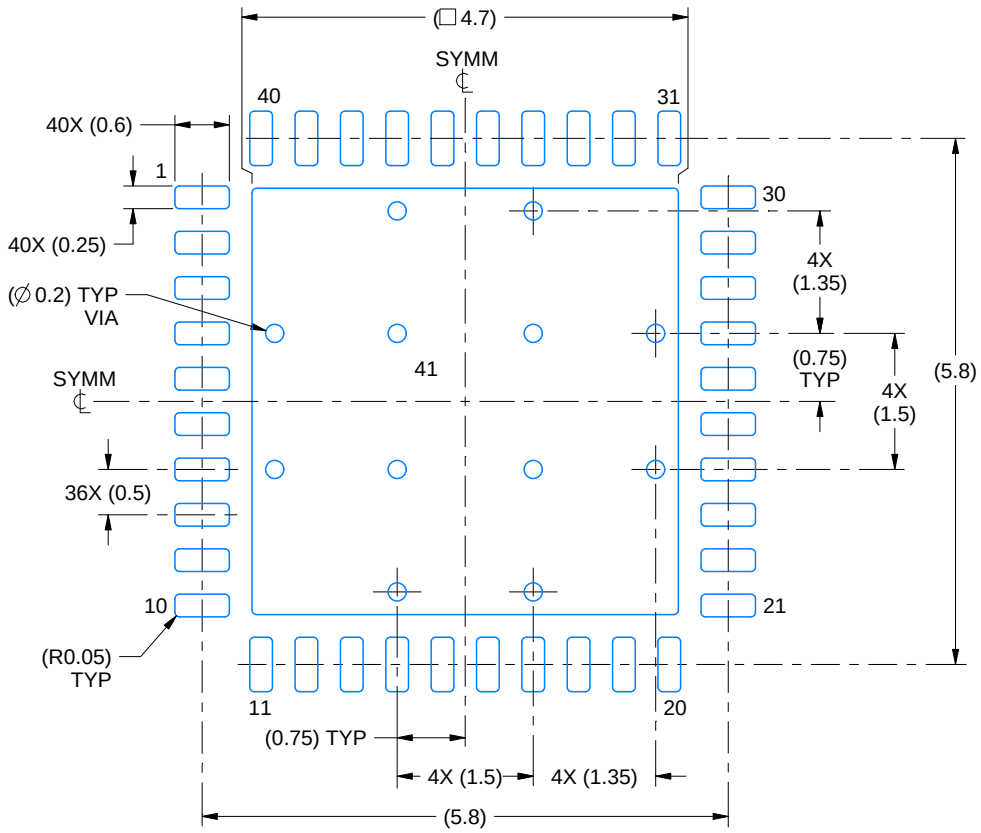
## VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

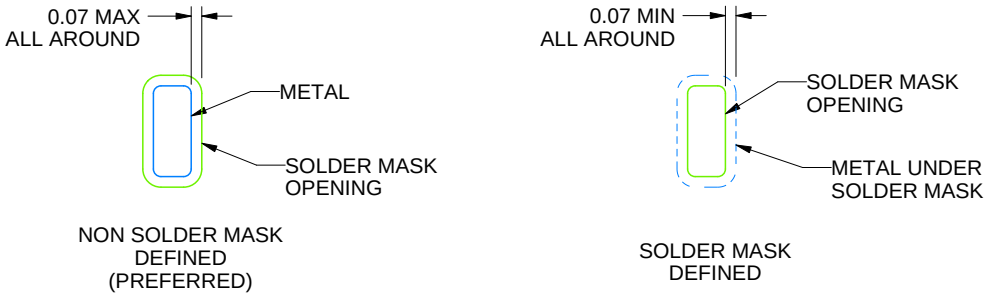



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.




LAND PATTERN EXAMPLE
SCALE:12X

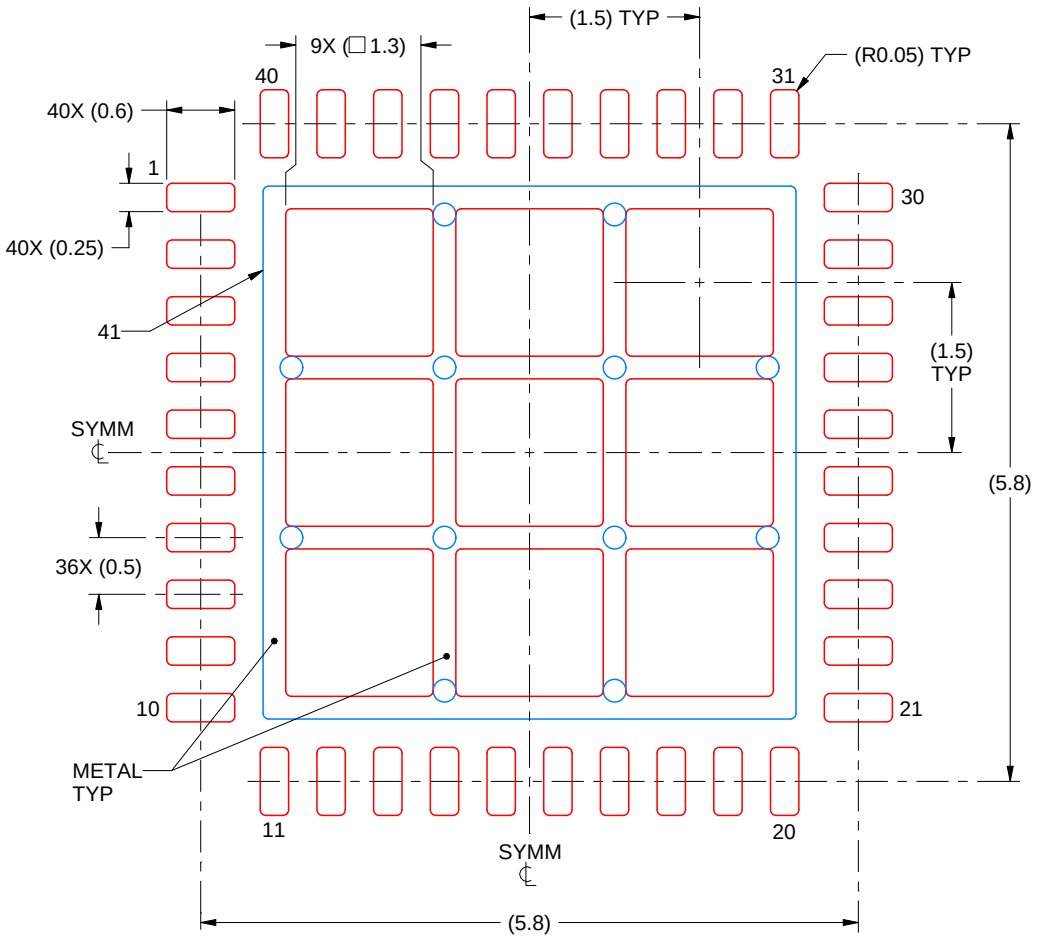



SOLDER MASK DETAILS

4219053/B 03/2021

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 41:
69% PRINTED SOLDER COVERAGE BY AREA
SCALE:15X

4219053/B 03/2021

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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