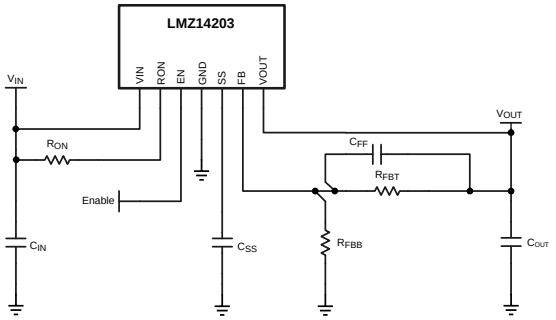
LMZ14203 SIMPLE SWITCHER® 6V～42V、3Aパワー・モジュール、リード付きSMT-TOパッケージ

1 特長

- 内蔵のシールド付きインダクタと単純なPCBレイアウト
- 外部のソフトスタートと高精度イネーブルによる柔軟なスタートアップ・シーケンシング
- 突入電流と、入力UVLOや出力短絡などのフォルトに対する保護
- 接合部温度範囲: -40℃～125℃
- 単一の露出パッドと標準ピン配置により取り付けと製造が容易
- FPGAやASICへの電源供給に適した高速な過渡応答
- 低い出力電圧リップル
- ピン単位で互換性のあるファミリ
  - LMZ1420x (42V、最大3A、2A、1A)
  - LMZ1200x (20V、最大3A、2A、1A)
- WEBENCH®Power Designerに完全対応
- 電気的特性
  - 最大合計出力電力: 18W
  - 最大3Aの出力電流
  - 入力電圧範囲: 6V～42V
  - 出力電圧範囲: 0.8V～6V
  - 最大効率90%
- 性能上の利点
  - 熱的な特性劣化なしに高い周囲温度で動作
  - 高い効率によりシステムの発熱が減少
  - 低い放射(電磁気干渉(EMI))、EN55022 Class B標準に準拠してテスト済み
  - 10V/m放射耐性EMIテスト標準EN61000 4-3に合格
- WEBENCH® Power Designerにより、LMZ14203を使用するカスタム設計を作成

簡略化されたアプリケーション回路図



2 アプリケーション

- 12Vおよび24V入力レールからのポイント・オブ・ロード(POL)変換
- 容積が制限された、または熱の要件が高いアプリケーション
- 負の出力電圧のアプリケーション
  (AN-2027 SNVA425を参照)

3 概要

LMZ14203 SIMPLE SWITCHERパワー・モジュールは使いやすい降圧型DC/DCソリューションで、非常に優れた電力変換効率、ラインおよび負荷レギュレーション、出力精度で、最大3Aの負荷を駆動できます。LMZ14203の革新的なパッケージは、熱特性を強化するとともに、人手でも機械でもハンダ付けできます。

LMZ14203は6V～42Vの入力電圧レールを受け付け、最低0.8Vの高精度かつ可変の出力電圧を供給します。LMZ14203は、わずか3つの外付け抵抗と4つの外付けコンデンサだけで、完全な電源ソリューションを構築できます。LMZ14203は信頼性が高く堅牢な設計で、サーマル・シャットダウン、入力UVLO、出力過電圧保護、短絡保護、出力電流制限の保護機能が搭載されており、プリバイアス出力へのスタートアップが可能です。スイッチング周波数は、1つの抵抗により最大1MHzに変更できます。

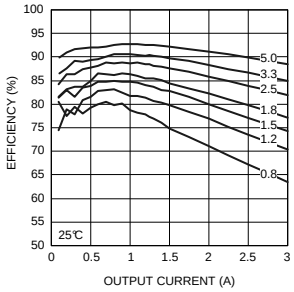
製品情報(1)(2)

型番	パッケージ	本体サイズ(公称)
LMZ14203	TO-PMOD (7)	10.16mm×9.85mm

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。

(2) ピーク・リフロー温度は245℃です。詳細については、SNAA214を参照してください。

25℃における12V入力の効率



英語版のTI製品についての情報を翻訳したこの資料は、製品の概要を確認する目的で便宜的に提供しているものです。該当する正式な英語版の最新情報は、www.ti.comで閲覧でき、その内容が常に優先されます。TIでは翻訳の正確性および妥当性につきましては一切保証いたしません。実際の設計などの前には、必ず最新版の英語版をご参照くださいますようお願いいたします。

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4 改訂履歴

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Revision R (October 2015) から **Revision S** に変更 **Page**

- Changed equation 9 to put a bracket around fsw*delta VIN ... 15
- Changed equation 10 to put a bracket around V_{IN} and R_{ON}^2 ... 16

Revision Q (August 2015) から **Revision R** に変更 **Page**

- Added this new bullet to the Power Module SMT Guidelines ... 20

Revision P (May 2015) から **Revision Q** に変更 **Page**

- ドキュメントのタイトル 変更 ... 1

Revision O (October 2013) から **Revision P** に変更 **Page**

- 「*ESD定格*」表、「*熱に関する情報*」表、「*機能説明*」セクション、「*デバイスの機能モード*」セクション、「*アプリケーションと実装*」セクション、「*電源に関する推奨事項*」セクション、「*レイアウト*」セクション、「*デバイスおよびドキュメントのサポート*」セクション、「*メカニカル、パッケージ、および注文情報*」セクション 追加 ... 1
- 使いやすいピン・パッケージの画像を削除 ... 1

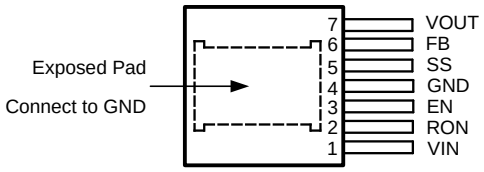
Revision N (March 2013) から **Revision O** に変更 **Page**

- Changed 12 mils ... 18
- Changed 12 mils ... 20
- Added *Power Module SMT Guidelines* ... 20

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5 Pin Configuration and Functions

NDW Package
7-Pin TO-PMOD
Top View



Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
EN	3	Analog	Enable. Input to the precision enable comparator. Rising threshold is 1.18 V nominal; 90 mV hysteresis nominal. Maximum recommended input level is 6.5 V.
FB	6	Analog	Feedback. Internally connected to the regulation, overvoltage, and short-circuit comparators. The regulation reference point is 0.8 V at this input pin. Connected the feedback resistor divider between the output and ground to set the output voltage.
GND	4	Ground	Ground. Reference point for all stated voltages. Must be externally connected to exposed thermal pad.
RON	2	Analog	ON-time resistor. An external resistor between this pin and the VIN pin sets the ON-time of the application. Typical values range from 25 kΩ to 124 kΩ.
SS	5	Analog	Soft-start. An internal 8-µA current source charges an external capacitor to produce the soft-start function. This node is discharged at 200 µA during disable, overcurrent, thermal shutdown and internal UVLO conditions.
VIN	1	Power	Supply input. Nominal operating range is 6 V to 42 V . A small amount of internal capacitance is contained within the package assembly. Additional external input capacitance is required between this pin and exposed pad.
VOUT	7	Power	Output voltage. Output from the internal inductor. Connect the output capacitor between this pin and exposed pad.
Thermal Pad	—	Ground	Exposed thermal pad. Internally connected to pin 4. Used to dissipate heat from the package during operation. Must be electrically connected to pin 4 external to the package.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)(2)

	MIN	MAX	UNIT
VIN, RON to GND	–0.3	43.5	V
EN, FB, SS to GND	–0.3	7	V
Junction Temperature		150	°C
Peak Reflow Case Temperature (30 sec)		245	°C
Storage Temperature	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) For soldering specifications, refer to the following document: *Absolute Maximum Ratings for Soldering* (SNOA549).

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6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±2000	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted) (1)

	MIN	MAX	UNIT
V_{IN}	6	42	V
EN	0	6.5	V
Operation Junction Temperature	−40	125	°C

(1) *Absolute Maximum Ratings* are limits beyond which damage to the device may occur. *Recommended Operating Ratings* are conditions under which operation of the device is intended to be functional. For ensured specifications and test conditions, see the *Electrical Characteristics*.

6.4 Thermal Information

THERMAL METRIC (1)			LMZ14203 NDW (TO-PMOD) 7 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	4-layer JEDEC Printed Circuit Board, No air flow	19.3	°C/W
		2-layer JEDEC Printed Circuit Board, No air flow	21.5	
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	No air flow	1.9	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics

T_J = 25°C unless otherwise noted. Minimum and maximum limits are ensured through test, design or statistical correlation. Typical values represent the most likely parametric norm at T_J = 25°C, and are provided for reference purposes only. Unless otherwise stated the following conditions apply: V_{IN} = 24 V, Vout = 3.3 V

PARAMETER		TEST CONDITIONS		MIN (1)	TYP (2)	MAX (1)	UNIT
SYSTEM PARAMETERS							
Enable Control (3)							
V_{EN}	EN threshold trip point	V_{EN} rising	T_J = 25°C		1.18		V
			over the junction temperature (T_J) range of –40°C to +125°C	1.1		1.25	
V_{EN-HYS}	EN threshold hysteresis	V_{EN} falling			90		mV
Soft Start							
I_{SS}	SS source current	V_{SS} = 0V	T_J = 25°C		8		µA
			over the junction temperature (T_J) range of –40°C to +125°C	5		11	
I_{SS-DIS}	SS discharge current				–200		µA
Current Limit							
I_{CL}	Current limit threshold	DC average V_{IN}= 12 V to 24 V	T_J = 25°C		4.2		A
			over the junction temperature (T_J) range of –40°C to +125°C	3.2		5.25	

(1) Minimum and maximum limits are 100% production tested at 25°C. Limits over the operating temperature range are ensured through correlation using Statistical Quality Control (SQC) methods. Limits are used to calculate Average Outgoing Quality Level (AOQL).
(2) Typical numbers are at 25°C and represent the most likely parametric norm.
(3) EN 55022:2006, +A1:2007, FCC Part 15 Subpart B: 2007. See AN-2024 and layout for information on device under test.

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Electrical Characteristics (continued)

T_J = 25°C unless otherwise noted. Minimum and maximum limits are ensured through test, design or statistical correlation. Typical values represent the most likely parametric norm at T_J = 25°C, and are provided for reference purposes only. Unless otherwise stated the following conditions apply: V_{IN} = 24 V, Vout = 3.3 V

PARAMETER		TEST CONDITIONS		MIN(1)	TYP(2)	MAX(1)	UNIT
ON/OFF Timer							
t_{ON-MIN}	ON timer minimum pulse width				150		ns
t_{OFF}	OFF timer pulse width				260		ns
Regulation and Overvoltage Comparator							
V_{FB}	In-regulation feedback voltage	V_{SS} > 0.8 V T_J = –40°C to 125°C I_O = 3 A	T_J = 25°C		0.804		V
			over the junction temperature (T_J) range of –40°C to +125°C	0.784		0.825	
		V_{SS} > 0.8 V T_J = 25°C I_O = 10 mA		0.786	0.802	0.818	V
V_{FB-OV}	Feedback overvoltage protection threshold				0.92		V
I_{FB}	Feedback input bias current				5		nA
I_Q	Nonswitching Input Current	V_{FB}= 0.86 V			1		mA
I_{SD}	Shut Down Quiescent Current	V_{EN}= 0 V			25		μA
Thermal Characteristics							
T_{SD}	Thermal Shutdown	Rising			165		°C
$T_{SD-HYST}$	Thermal shutdown hysteresis	Falling			15		°C
PERFORMANCE PARAMETERS							
ΔV_O	Output Voltage Ripple				8		mV_{PP}
$\Delta V_O/\Delta V_{IN}$	Line Regulation	V_{IN} = 12 V to 42 V, I_O= 3 A			0.01%		
$\Delta V_O/I_{OUT}$	Load Regulation	V_{IN} = 24 V			1.5		mV/A
η	Efficiency	V_{IN} = 24 V V_O = 3.3 V I_O = 1 A			92%		
η	Efficiency	V_{IN} = 24 V V_O = 3.3 V I_O = 3 A			85%		

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6.6 Typical Characteristics

Unless otherwise specified, the following conditions apply: V_{IN} = 24 V; C_{IN} = 10-µF X7R Ceramic; C_O = 100-µF X7R Ceramic; T_A = 25°C for efficiency curves and waveforms.

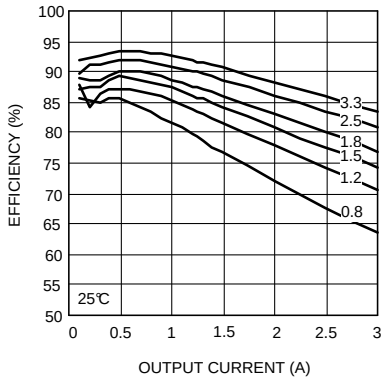


Figure 1. Efficiency 6-V Input at 25°C

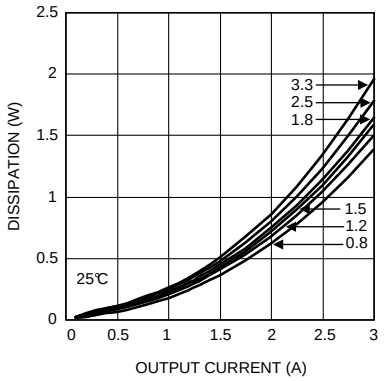


Figure 2. Dissipation 6-V Input at 25°C

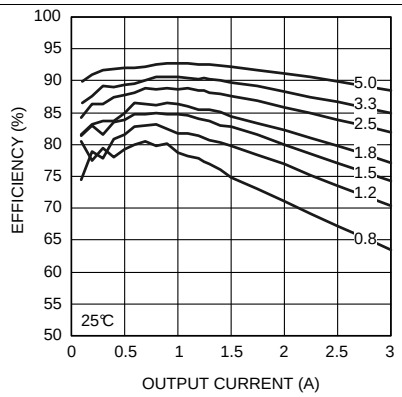


Figure 3. Efficiency 12-V Input at 25°C

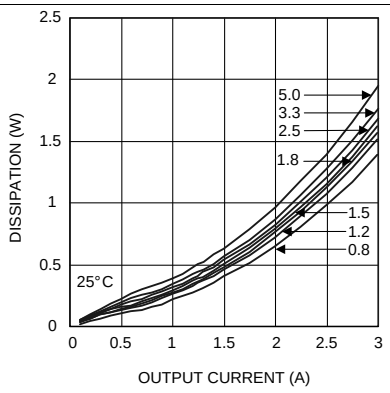


Figure 4. Dissipation 12-V Input at 25°C

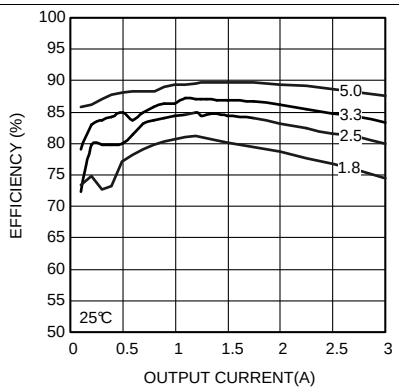


Figure 5. Efficiency 24-V Input at 25°C

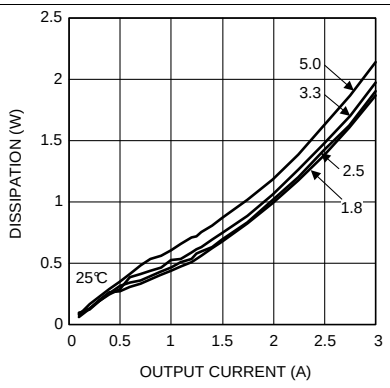


Figure 6. Dissipation 24-V Input at 25°C

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Typical Characteristics (continued)

Unless otherwise specified, the following conditions apply: V_{IN} = 24 V; C_{IN} = 10-µF X7R Ceramic; C_O = 100-µF X7R Ceramic; T_A = 25°C for efficiency curves and waveforms.

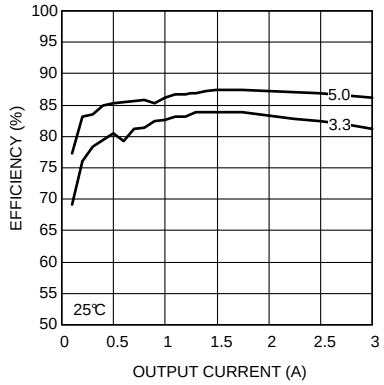


Figure 7. Efficiency 36-V Input at 25°C

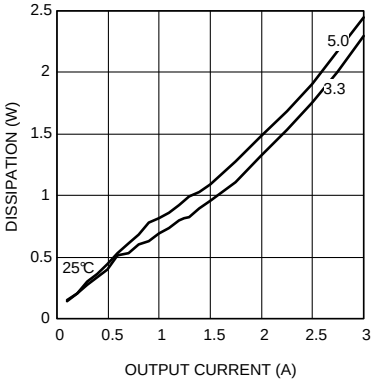


Figure 8. Dissipation 36-V Input at 25°C

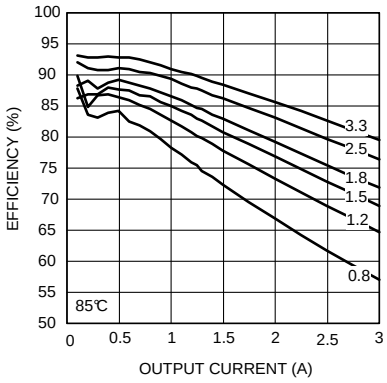


Figure 9. Efficiency 6-V Input at 85°C

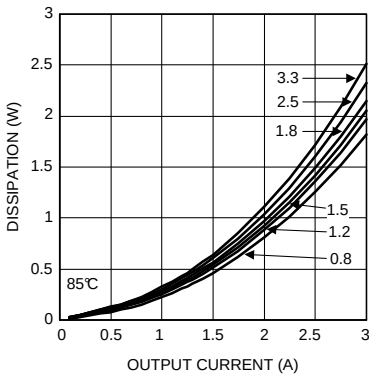


Figure 10. Dissipation 6-V Input at 85°C

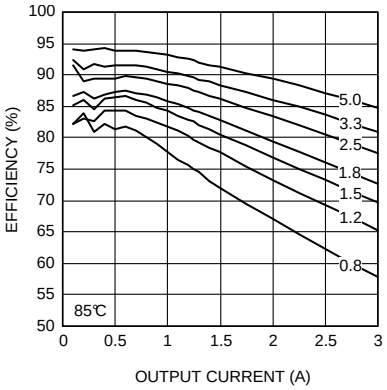


Figure 11. Efficiency 8-V Input at 85°C

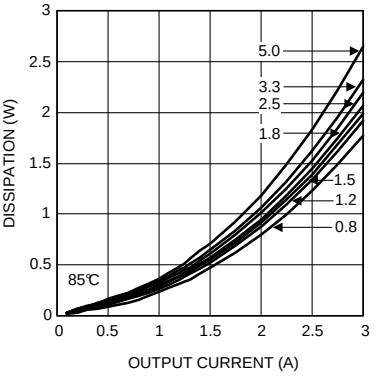


Figure 12. Dissipation 8-V Input at 85°C

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Typical Characteristics (continued)

Unless otherwise specified, the following conditions apply: V_{IN} = 24 V; C_{IN} = 10-µF X7R Ceramic; C_O = 100-µF X7R Ceramic; T_A = 25°C for efficiency curves and waveforms.

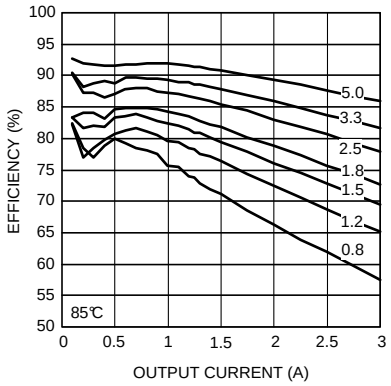


Figure 13. Efficiency 12-V Input at 85°C

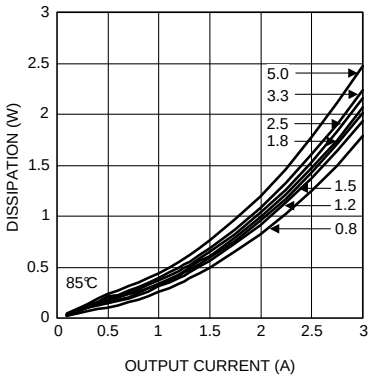


Figure 14. Dissipation 12-V Input at 85°C

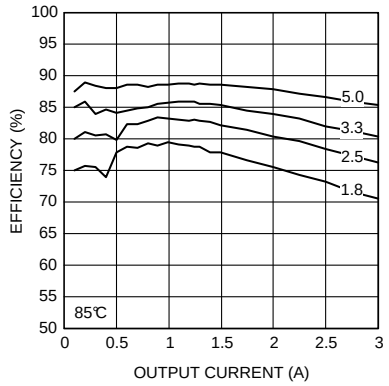


Figure 15. Efficiency 24-V Input at 85°C

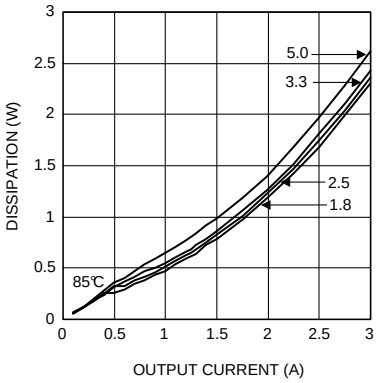


Figure 16. Dissipation 24-V Input at 85°C

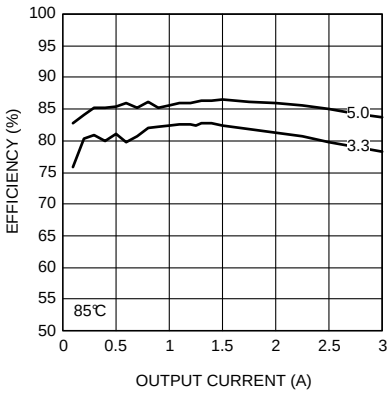


Figure 17. Efficiency 36-V Input at 85°C

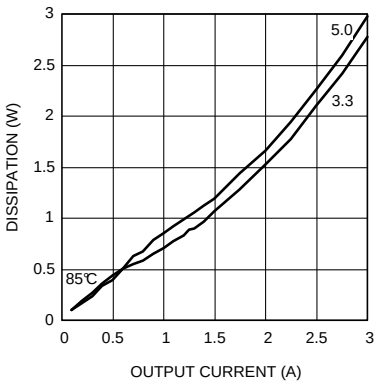


Figure 18. Dissipation 36-V Input at 85°C

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Typical Characteristics (continued)

Unless otherwise specified, the following conditions apply: V_{IN} = 24 V; C_{IN} = 10-µF X7R Ceramic; C_O = 100-µF X7R Ceramic; T_A = 25°C for efficiency curves and waveforms.

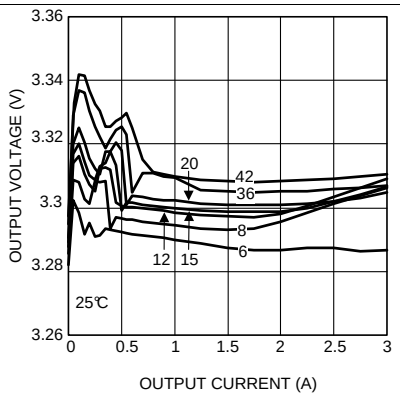


Figure 19. Line and Load Regulation at 25°C

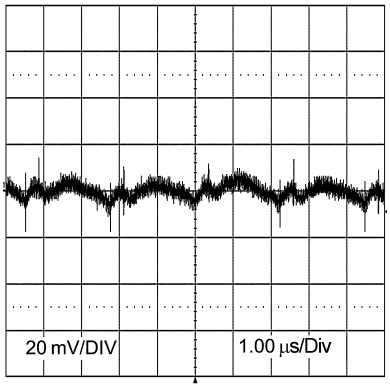


Figure 20. Output Ripple
24 V_{IN} 3.3 V_O 3 A, BW = 200 MHz

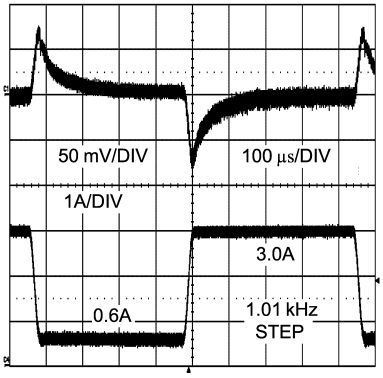


Figure 21. Transient Response
24 V_{IN} 3.3 V_O 0.6-A to 3-A Step

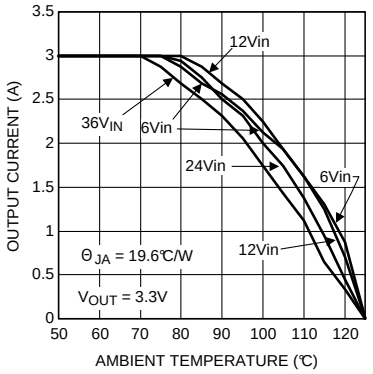


Figure 22. Thermal Derating V_{OUT} = 3.3 V

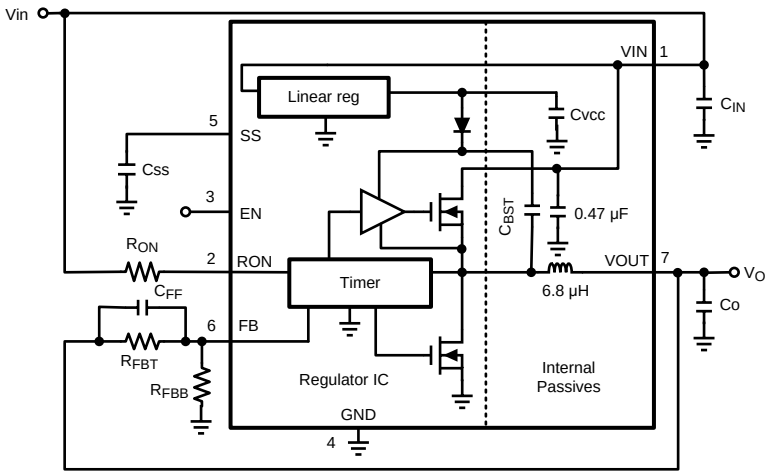
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7 Detailed Description

7.1 Overview

The LMZ14203 power module is an easy-to-use step-down DC-DC solution that can drive up to 3-A load with exceptional power conversion efficiency, line and load regulation, and output accuracy.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 COT Control Circuit Overview

Constant ON-Time control is based on a comparator and an ON-time one shot, with the output voltage feedback compared with an internal 0.8-V reference. If the feedback voltage is below the reference, the main MOSFET is turned on for a fixed ON-time determined by a programming resistor R_{ON}. R_{ON} is connected to V_{IN} such that ON-time is reduced with increasing input supply voltage. Following this ON-time, the main MOSFET remains off for a minimum of 260 ns. If the voltage on the feedback pin falls below the reference level again the ON-time cycle is repeated. Regulation is achieved in this manner.

7.3.2 Output Overvoltage Comparator

The voltage at FB is compared to a 0.92-V internal reference. If FB rises above 0.92 V the ON-time is immediately terminated. This condition is known as overvoltage protection (OVP). It can occur if the input voltage is increased very suddenly or if the output load is decreased very suddenly. Once OVP is activated, the top MOSFET ON-times will be inhibited until the condition clears. Additionally, the synchronous MOSFET will remain on until inductor current falls to zero.

7.3.3 Current Limit

Current limit detection is carried out during the OFF-time by monitoring the current in the synchronous MOSFET. Referring to the Functional Block Diagram, when the top MOSFET is turned off, the inductor current flows through the load, the PGND pin and the internal synchronous MOSFET. If this current exceeds 4.2 A (typical) the current limit comparator disables the start of the next ON-time period. The next switching cycle will occur only if the FB input is less than 0.8 V and the inductor current has decreased below 4.2 A. Inductor current is monitored during the period of time the synchronous MOSFET is conducting. So long as inductor current exceeds 4.2 A, further ON-time intervals for the top MOSFET will not occur. Switching frequency is lower during current limit due to the longer OFF-time.

NOTE

Current limit is dependent on both duty cycle and temperature.

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Feature Description (continued)

7.3.4 Thermal Protection

The junction temperature of the LMZ14203 should not be allowed to exceed its maximum ratings. Thermal protection is implemented by an internal Thermal Shutdown circuit which activates at 165 °C (typical) causing the device to enter a low power standby state. In this state the main MOSFET remains off causing V_O to fall, and additionally the CSS capacitor is discharged to ground. Thermal protection helps prevent catastrophic failures for accidental device overheating. When the junction temperature falls back below 145°C (typical hysteresis = 20 °C) the SS pin is released, V_O rises smoothly, and normal operation resumes.

Applications requiring maximum output current especially those at high input voltage may require application derating at elevated temperatures.

7.3.5 Zero Coil Current Detection

The current of the lower (synchronous) MOSFET is monitored by a zero coil current detection circuit which inhibits the synchronous MOSFET when its current reaches zero until the next ON-time. This circuit enables the DCM operating mode, which improves efficiency at light loads.

7.3.6 Prebiased Start-Up

The LMZ14203 will properly start up into a prebiased output. This start-up situation is common in multiple rail logic applications where current paths may exist between different power rails during the start-up sequence. Figure 23 is a scope capture that shows proper behavior during this event.

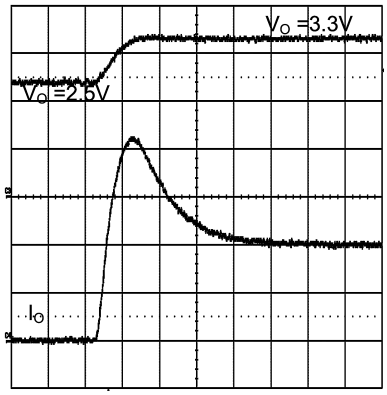


Figure 23. Prebiased Start-Up

7.4 Device Functional Modes

7.4.1 Discontinuous Conduction and Continuous Conduction Modes

At light-load, the regulator operates in discontinuous conduction mode (DCM). With load currents above the critical conduction point, it operates in continuous conduction mode (CCM). When operating in DCM the switching cycle begins at zero amps inductor current; increases up to a peak value, and then recedes back to zero before the end of the OFF-time. During the period of time that inductor current is zero, all load current is supplied by the output capacitor. The next ON-time period starts when the voltage on the FB pin falls below the internal reference. The switching frequency is lower in DCM and varies more with load current as compared to CCM. Conversion efficiency in DCM is maintained because conduction and switching losses are reduced with the smaller load and lower switching frequency.

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8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The LMZ14203 is a step-down DC-to-DC power module. It is typically used to convert a higher DC voltage to a lower DC voltage with a maximum output current of 3 A. The following design procedure can be used to select components for the LMZ14203. Alternately, the WEBENCH software may be used to generate complete designs.

When generating a design, the WEBENCH software uses iterative design procedure and accesses comprehensive databases of components. For more details, see www.ti.com.

8.2 Typical Application

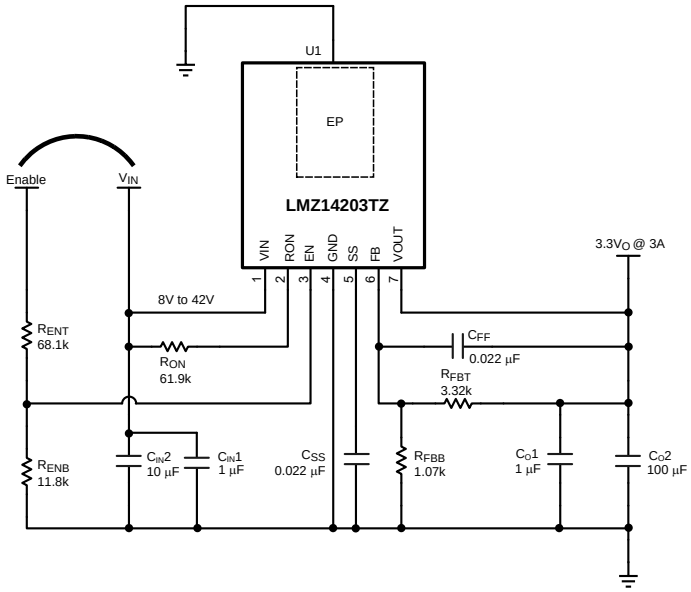


Figure 24. Evaluation Board Schematic Diagram

8.2.1 Design Requirements

For this example the following application parameters exist.

- V_{IN} Range = Up to 42 V
- V_{OUT} = 0.8 V to 5 V
- I_{OUT} = 3 A

Please refer to Table 1 for more information.

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Table 1. Component Value Combinations

VOUT (V)	R_{FBT} (kΩ)	R_{FBB} (kΩ)	$R_{DS(on)}$ (kΩ)	VIN (V)	
				MIN	MAX
5	5.62	1.07	100	7.5	42
3.3	3.32		61.9	6	42
2.5	2.26		47.5		30
1.8	1.87	1.5	32.4		25
1.5	1	1.13	28		21
1.2	4.22	8.45	22.6		19
0.8	0	39.2	24.9		18

Table 2. List of Materials

Ref Des	Description	Case Size	Manufacturer	Manufacturer P/N
U1	SIMPLE SWITCHER	PFM-7	Texas Instruments	LMZ14203TZ
C_{IN1}	1 µF, 50 V, X7R	1206	Taiyo Yuden	UMK316B7105KL-T
C_{IN2}	10 µF, 50 V, X7R	1210	Taiyo Yuden	UMK325BJ106MM-T
C_{O1}	1 µF, 50 V, X7R	1206	Taiyo Yuden	UMK316B7105KL-T
C_{O2}	100 µF, 6.3 V, X7R	1210	Taiyo Yuden	JMK325BJ107MM-T
R_{FBT}	3.32 kΩ	0603	Vishay Dale	CRCW06033K32FKEA
R_{FBB}	1.07 kΩ	0603	Vishay Dale	CRCW06031K07FKEA
R_{ON}	61.9 kΩ	0603	Vishay Dale	CRCW060361k9FKEA
R_{ENT}	68.1 kΩ	0603	Vishay Dale	CRCW060368k1FKEA
R_{ENB}	11.8 kΩ	0603	Vishay Dale	CRCW060311k8FKEA
C_{FF}	22 nF, ±10%, X7R, 16 V	0603	TDK	C1608X7R1H223K
C_{SS}	22 nF, ±10%, X7R, 16 V	0603	TDK	C1608X7R1H223K

8.2.2 Detailed Design Procedure

8.2.2.1 Custom Design With WEBENCH® Tools

Click here to create a custom design using the LMZ14203 device with the WEBENCH® Power Designer.

1. Start by entering the input voltage (V_{IN}), output voltage (V_{OUT}), and output current (I_{OUT}) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance
- Run thermal simulations to understand board thermal performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

8.2.2.2 Design Steps for the LMZ14203 Application

The LMZ14203 is fully supported by WEBENCH and offers the following: Component selection, electrical and thermal simulations as well as the build-it board for a reduction in design time. The following list of steps can be used to manually design the LMZ14203 application.

1. Select minimum operating V_{IN} with enable divider resistors
2. Program V_O with divider resistor selection
3. Program turnon time with soft-start capacitor selection

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4. Select C_O
5. Select C_{IN}
6. Set operating frequency with R_{ON}
7. Determine module dissipation
8. Lay out PCB for required thermal performance

8.2.2.2.1 Enable Divider, R_{ENT} and R_{ENB} Selection

The enable input provides a precise 1.18-V band-gap rising threshold to allow direct logic drive or connection to a voltage divider from a higher enable voltage such as V_{IN}. The enable input also incorporates 90 mV (typical) of hysteresis resulting in a falling threshold of 1.09 V. The maximum recommended voltage into the EN pin is 6.5 V. For applications where the midpoint of the enable divider exceeds 6.5 V, a small Zener diode can be added to limit this voltage.

The function of this resistive divider is to allow the designer to choose an input voltage below which the circuit will be disabled. This implements the feature of programmable under voltage lockout. This is often used in battery powered systems to prevent deep discharge of the system battery. It is also useful in system designs for sequencing of output rails or to prevent early turnon of the supply as the main input voltage rail rises at power-up. Applying the enable divider to the main input rail is often done in the case of higher input voltage systems such as 24-V AC/DC systems where a lower boundary of operation should be established. In the case of sequencing supplies, the divider is connected to a rail that becomes active earlier in the power-up cycle than the LMZ14203 output rail. The two resistors should be chosen based on the following ratio:

$$R_{ENT} / R_{ENB} = (V_{IN\ UVLO} / 1.18\ V) - 1 \quad (1)$$

The LMZ14203 demonstration and evaluation boards use 11.8 kΩ for R_{ENB} and 68.1 kΩ for R_{ENT} resulting in a rising UVLO of 8 V. This divider presents 6.25 V to the EN input when the divider input is raised to 42 V.

The EN pin is internally pulled up to VIN and can be left floating for always-on operation.

8.2.2.2.2 Output Voltage Selection

Output voltage is determined by a divider of two resistors connected between V_O and ground. The midpoint of the divider is connected to the FB input. The voltage at FB is compared to a 0.8V internal reference. In normal operation an ON-time cycle is initiated when the voltage on the FB pin falls below 0.8 V. The main MOSFET ON-time cycle causes the output voltage to rise and the voltage at the FB to exceed 0.8 V. As long as the voltage at FB is above 0.8 V, ON-time cycles will not occur.

The regulated output voltage determined by the external divider resistors R_{FBT} and R_{FBB} is:

$$V_O = 0.8\ V \times (1 + R_{FBT} / R_{FBB}) \quad (2)$$

Rearranging terms; the ratio of the feedback resistors for a desired output voltage is:

$$R_{FBT} / R_{FBB} = (V_O / 0.8\ V) - 1 \quad (3)$$

These resistors should be chosen from values in the range of 1 kΩ to 10 kΩ.

For V_O = 0.8 V the FB pin can be connected to the output directly so long as an output preload resistor remains that draws more than 20 uA. Converter operation requires this minimum load to create a small inductor ripple current and maintain proper regulation when no load is present.

A feed-forward capacitor is placed in parallel with R_{FBT} to improve load step transient response. Its value is usually determined experimentally by load stepping between DCM and CCM conduction modes and adjusting for best transient response and minimum output ripple.

A table of values for R_{FBT} , R_{FBB} , C_{FF} and R_{ON} is included in the applications schematic.

8.2.2.2.3 Soft-Start Capacitor Selection

Programmable soft-start permits the regulator to slowly ramp to its steady state operating point after being enabled, thereby reducing current inrush from the input supply and slowing the output voltage rise-time to prevent overshoot.

Upon turnon, after all UVLO conditions have been passed, an internal 8-uA current source begins charging the external soft-start capacitor. The soft-start time duration to reach steady-state operation is given by the formula:

$$t_{SS} = V_{REF} \times C_{SS} / Iss = 0.8\ V \times C_{SS} / 8\ uA \quad (4)$$

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This equation can be rearranged as follows:

$$C_{SS} = t_{SS} \times 8\ \mu A / 0.8\ V \quad (5)$$

Use of a 0.022-µF capacitor results in 2.2 ms soft-start duration. This is recommended as a minimum value.

As the soft-start input exceeds 0.8 V the output of the power stage will be in regulation. The soft-start capacitor continues charging until it reaches approximately 3.8 V on the SS pin. Voltage levels between 0.8 V and 3.8 V have no effect on other circuit operation. Note the following conditions will reset the soft-start capacitor by discharging the SS input to ground with an internal 200-µA current sink.

- The enable input being *pulled low*
- Thermal shutdown condition
- Overcurrent fault
- Internal V_{CC} UVLO (Approx 4-V input to V_{IN})

8.2.2.2.4 C_O Selection

None of the required C_O output capacitance is contained within the module. At a minimum, the output capacitor must meet the worst case minimum ripple current rating of 0.5 × $I_{LR\ P-P}$, as calculated in Equation 12 below. Beyond that, additional capacitance will reduce output ripple so long as the ESR is low enough to permit it. A minimum value of 10 µF is generally required. Experimentation will be required if attempting to operate with a minimum value. Ceramic capacitors or other low ESR types are recommended. See AN-2024 SNVA422 for more detail.

The following equation provides a good first pass approximation of C_O for load transient requirements:

$$C_O \geq I_{STEP} \times V_{FB} \times L \times V_{IN} / (4 \times V_O \times (V_{IN} - V_O) \times V_{OUT\text{-}TRAN}) \quad (6)$$

Solving:

$$C_O \geq 3\ A \times 0.8\ V \times 6.8\ \mu H \times 24\ V / (4 \times 3.3\ V \times (24\ V - 3.3\ V) \times 33\ mV) \geq 43\ \mu F \quad (7)$$

The LMZ14203 demonstration and evaluation boards are populated with a 100-uF 6.3-V X5R output capacitor. Locations for extra output capacitors are provided.

8.2.2.2.5 C_{IN} Selection

The LMZ14203 module contains an internal 0.47-µF input ceramic capacitor. Additional input capacitance is required external to the module to handle the input ripple current of the application. This input capacitance should be very close to the module. Input capacitor selection is generally directed to satisfy the input ripple current requirements rather than by capacitance value. Worst-case input ripple current rating is dictated by the equation:

$$I(C_{IN(RMS)}) \cong 1/2 \times I_O \times \sqrt{(D / 1 - D)}$$

where

- $D \cong V_O / V_{IN}$ (8)

(As a point of reference, the worst case ripple current will occur when the module is presented with full load current and when $V_{IN} = 2 \times V_O$).

Recommended minimum input capacitance is 10uF X7R ceramic with a voltage rating at least 25% higher than the maximum applied input voltage for the application. TI also recommends to pay attention to the voltage and temperature deratings of the capacitor selected. Note ripple current rating of ceramic capacitors may be missing from the capacitor data sheet and you may need to contact the capacitor manufacturer for this rating.

If the system design requires a certain minimum value of input ripple voltage ΔV_{IN} be maintained then the following equation may be used.

$$C_{IN} \geq I_O \times D \times (1-D) / (f_{SW\text{-}CCM} \times \Delta V_{IN}) \quad (9)$$

If ΔV_{IN} is 1% of V_{IN} for a 24-V input to 3.3-V output application this equals 240 mV and f_{SW} = 400 kHz.

$C_{IN} \geq 3\ A \times 3.3\ V / 24\ V \times (1 - 3.3\ V / 24\ V) / (400000 \times 0.240\ V)$

$\geq 3.7\ \mu F$

Additional bulk capacitance with higher ESR may be required to damp any resonant effects of the input capacitance and parasitic inductance of the incoming supply lines.

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8.2.2.2.6 Discontinuous Conduction and Continuous Conduction Mode Selection

Operating frequency in DCM can be calculated as follows:

$$f_{SW(DCM)} \cong V_O \times (V_{IN}\text{-}1) \times 6.8\ \mu H \times 1.18 \times 10^{20} \times I_O / ((V_{IN} - V_O) \times R_{ON}^2) \quad (10)$$

In CCM, current flows through the inductor through the entire switching cycle and never falls to zero during the OFF-time. The switching frequency remains relatively constant with load current and line voltage variations. The CCM operating frequency can be calculated using Equation 7 above.

Following is a comparison pair of waveforms of the showing both CCM (upper) and DCM operating modes.

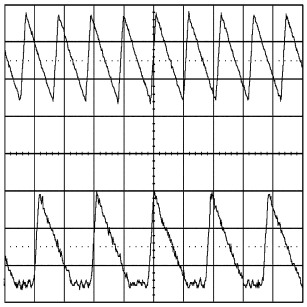


Figure 25. CCM and DCM Operating Modes V_{IN} = 24 V, V_O = 3.3 V, I_O = 3 A/0.4 A 2 µs/div

The approximate formula for determining the DCM/CCM boundary is as follows:

$$I_{DCB} \cong V_O \times (V_{IN} - V_O) / (2 \times 6.8\ \mu H \times f_{SW(CCM)} \times V_{IN}) \quad (11)$$

Following is a typical waveform showing the boundary condition.

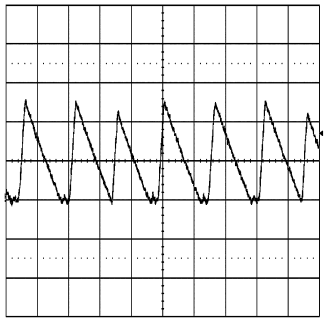


Figure 26. Transition Mode Operation V_{IN} = 24 V, V_O = 3.3 V, I_O = 0.5 A 2 µs/div

The inductor internal to the module is 6.8 µH. This value was chosen as a good balance between low and high input voltage applications. The main parameter affected by the inductor is the amplitude of the inductor ripple current (I_{LR}). I_{LR} can be calculated with:

$$I_{LR\ P\text{-}P} = V_O \times (V_{IN} - V_O) / (6.8\mu H \times f_{SW} \times V_{IN})$$

where

- V_{IN} is the maximum input voltage and f_{SW} is determined from Equation 13. (12)

If the output current I_O is determined by assuming that $I_O = I_L$, the higher and lower peak of I_{LR} can be determined. Be aware that the lower peak of I_{LR} must be positive if CCM operation is required.

8.2.2.2.7 R_{ON} Resistor Selection

Many designs will begin with a desired switching frequency in mind. For that purpose the following equation can be used.

$$f_{SW(CCM)} \cong V_O / (1.3 \times 10^{-10} \times R_{ON}) \quad (13)$$

This can be rearranged as

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$$R_{ON} \cong V_O / (1.3 \times 10^{-10} \times f_{SW(CCM)}) \quad (14)$$

The selection of RON and $f_{SW(CCM)}$ must be confined by limitations in the ON-time and OFF-time for the *COT Control Circuit Overview* section.

The ON-time of the LMZ14203 timer is determined by the resistor R_{ON} and the input voltage V_{IN}. It is calculated as follows:

$$t_{ON} = (1.3 \times 10^{-10} \times R_{ON}) / V_{IN} \quad (15)$$

The inverse relationship of t_{ON} and V_{IN} gives a nearly constant switching frequency as V_{IN} is varied. R_{ON} should be selected such that the ON-time at maximum V_{IN} is greater than 150 ns. The ON-timer has a limiter to ensure a minimum of 150 ns for t_{ON}. This limits the maximum operating frequency, which is governed by the following equation:

$$f_{SW(MAX)} = V_O / (V_{IN(MAX)} \times 150 \text{ ns}) \quad (16)$$

This equation can be used to select R_{ON} if a certain operating frequency is desired so long as the minimum ON-time of 150 ns is observed. The limit for R_{ON} can be calculated as follows:

$$R_{ON} \geq V_{IN(MAX)} \times 150 \text{ ns} / (1.3 \times 10^{-10}) \quad (17)$$

If R_{ON} calculated in Equation 14 is less than the minimum value determined in Equation 17 a lower frequency should be selected. Alternatively, $V_{IN(MAX)}$ can also be limited to keep the frequency unchanged.

NOTE

The minimum OFF-time of 260 ns limits the maximum duty ratio. Larger R_{ON} (lower F_{SW}) should be selected in any application requiring large duty ratio.

8.2.3 Application Curves

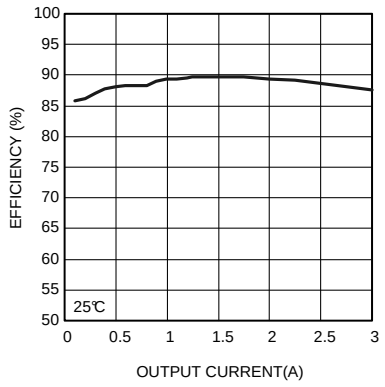


Figure 27. Efficiency V_{IN} = 24 V V_{OUT} = 5.0 V

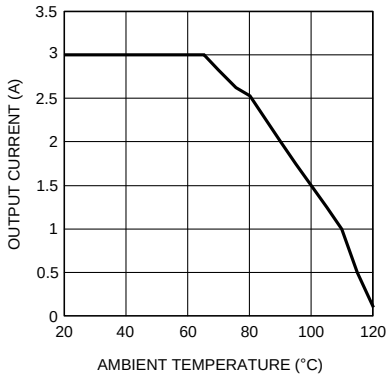


Figure 28. Thermal Derating Curve V_{IN} = 24 V, V_{OUT} = 5.0 V

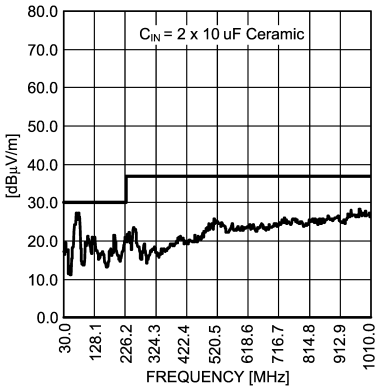


Figure 29. Radiated Emissions (EN 55022 Class B) From Evaluation Board

9 Power Supply Recommendations

The LMZ14203 device is designed to operate from an input voltage supply range between 4.5 V and 42 V. This input supply should be well regulated and able to withstand maximum input current and maintain a stable voltage. The resistance of the input supply rail should be low enough that an input current transient does not cause a high enough drop at the LMZ14203 supply voltage that can cause a false UVLO fault triggering and system reset. If the input supply is located more than a few inches from the LMZ14203, additional bulk capacitance may be required in addition to the ceramic bypass capacitors. The amount of bulk capacitance is not critical, but a 47-μF or 100-μF electrolytic capacitor is a typical choice.

10 Layout

10.1 Layout Guidelines

PCB layout is an important part of DC-DC converter design. Poor board layout can disrupt the performance of a DC-DC converter and surrounding circuitry by contributing to EMI, ground bounce and resistive voltage drop in the traces. These can send erroneous signals to the DC-DC converter resulting in poor regulation or instability. Good layout can be implemented by following a few simple design rules.

1. **Minimize area of switched current loops.**

   From an EMI reduction standpoint, it is imperative to minimize the high di/dt paths during PCB layout. The high current loops that do not overlap have high di/dt content that will cause observable high frequency noise on the output pin if the input capacitor (Cin1) is placed at a distance away from the LMZ14203. Therefore place C_{IN1} as close as possible to the LMZ14203 VIN and GND exposed pad. This will minimize the high di/dt area and reduce radiated EMI. Additionally, grounding for both the input and output capacitor should consist of a localized top side plane that connects to the GND exposed pad (EP).

2. **Have a single point ground.**

   The ground connections for the feedback, soft-start, and enable components should be routed to the GND pin of the device. This prevents any switched or load currents from flowing in the analog ground traces. If not properly handled, poor grounding can result in degraded load regulation or erratic output voltage ripple behavior. Provide the single point ground connection from pin 4 to EP.

3. **Minimize trace length to the FB pin.**

   Both feedback resistors, R_{FBT} and R_{FBB}, and the feed forward capacitor C_{FF}, should be close to the FB pin. Since the FB node is high impedance, maintain the copper area as small as possible. The trace are from R_{FBT}, R_{FBB}, and C_{FF} should be routed away from the body of the LMZ14203 to minimize noise.

4. **Make input and output bus connections as wide as possible.**

   This reduces any voltage drops on the input or output of the converter and maximizes efficiency. To optimize voltage accuracy at the load, ensure that a separate feedback voltage sense trace is made to the load. Doing so will correct for voltage drops and provide optimum output accuracy.

5. **Provide adequate device heat-sinking.**

   Use an array of heat-sinking vias to connect the exposed pad to the ground plane on the bottom PCB layer. If the PCB has a plurality of copper layers, these thermal vias can also be employed to make connection to inner layer heat-spreading ground planes. For best results use a 6 × 6 via array with minimum via diameter of 8 mils thermal vias spaced 59 mils (1.5 mm). Ensure enough copper area is used for heat-sinking to keep the junction temperature below 125°C.

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10.2 Layout Example

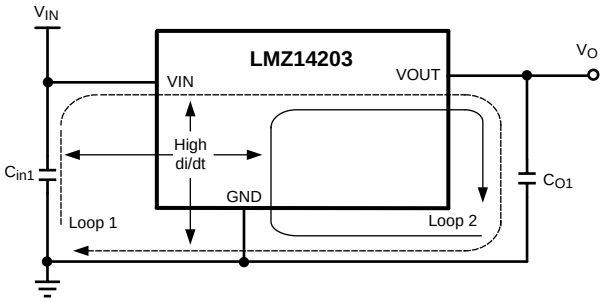


Figure 30. Minimize Area of Current Loops in Buck Module

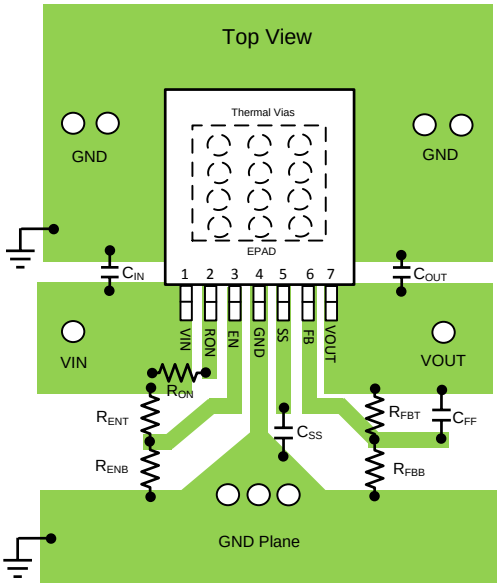


Figure 31. PCB Layout Guide

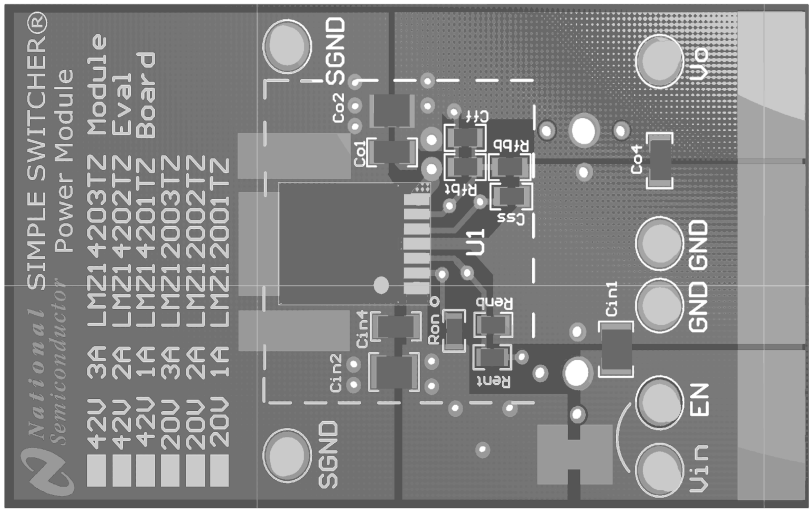


Figure 32. EVM Board Layout - Top View

Layout Example (continued)

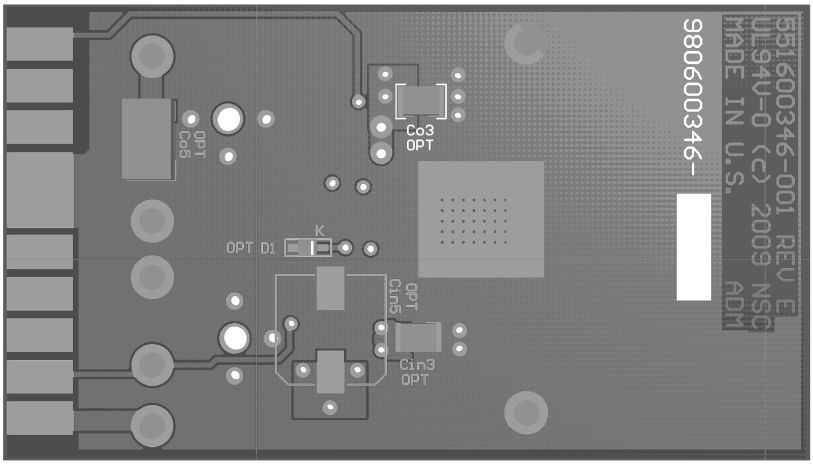


Figure 33. EVM Board Layout - Bottom View

10.3 Power Dissipation and Board Thermal Requirements

For the design case of V_{IN} = 24 V, V_O = 3.3 V, I_O = 3 A, $T_{AMB(MAX)}$ = 85°C , and $T_{JUNCTION}$ = 125°C, the device must see a thermal resistance from case to ambient of:

$$R_{\theta CA} < (T_{J\text{-}MAX} - T_{AMB(MAX)}) / P_{IC\text{-}LOSS} - R_{\theta JC} \quad (18)$$

Given the typical thermal resistance from junction to case to be 1.9°C/W. Use the 85°C power dissipation curves in the *Typical Characteristics* section to estimate the $P_{IC\text{-}LOSS}$ for the application being designed. In this application it is 2.25 W.

$R_{\theta CA} < (125 – 85) / 2.25\ W – 1.9 = 15.8$

To reach $R_{\theta CA}$ = 15.8, the PCB is required to dissipate heat effectively. With no airflow and no external heat, a good estimate of the required board area covered by 1 oz. copper on both the top and bottom metal layers is:

$$\text{Board Area_cm}^2 > 500°C \times \text{cm}^2/W / R_{\theta CA} \quad (19)$$

As a result, approximately 31.5 square cm of 1 oz copper on top and bottom layers is required for the PCB design. The PCB copper heat sink must be connected to the exposed pad. Approximately thirty six, 8-mil thermal vias spaced 59 mils (1.5 mm) apart must connect the top copper to the bottom copper. For an example of a high thermal performance PCB layout, refer to the Evaluation Board application note AN-2024 SNVA422.

10.4 Power Module SMT Guidelines

The recommendations below are for a standard module surface mount assembly

- Land Pattern – Follow the PCB land pattern with either soldermask defined or non-soldermask defined pads
- Stencil Aperture
  - For the exposed die attach pad (DAP), adjust the stencil for approximately 80% coverage of the PCB land pattern
  - For all other I/O pads use a 1:1 ratio between the aperture and the land pattern recommendation
- Solder Paste – Use a standard SAC Alloy such as SAC 305, type 3 or higher
- Stencil Thickness – 0.125 mm to 0.15 mm
- Reflow - Refer to solder paste supplier recommendation and optimized per board size and density
- Refer to AN SNAA214 for Reflow information.
- Maximum number of reflows allowed is one

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Power Module SMT Guidelines (continued)

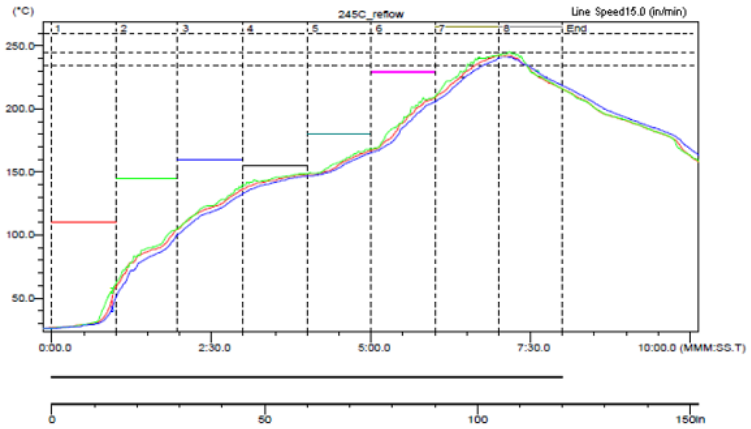


Figure 34. Sample Reflow Profile

Table 3. Sample Reflow Profile Table

Probe	Max Temp (°C)	Reached Max Temp	Time Above 235°C	Reached 235°C	Time Above 245°C	Reached 245°C	Time Above 260°C	Reached 260°C
#1	242.5	6.58	0.49	6.39	0.00	–	0.00	–
#2	242.5	7.10	0.55	6.31	0.00	7.10	0.00	–
#3	241.0	7.09	0.42	6.44	0.00	–	0.00	–

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11 デバイスおよびドキュメントのサポート

11.1 WEBENCH®ツールによるカスタム設計

ここをクリックすると、WEBENCH® Power Designerにより、LMZ14203を使用するカスタム設計を作成できます。

1. 最初に、入力電圧(V_{IN})、出力電圧(V_{OUT})、出力電流(I_{OUT})の要件を入力します。
2. オプティマイザのダイヤルを使用して、効率、占有面積、コストなどの主要なパラメータについて設計を最適化します。
3. 生成された設計を、テキサス・インスツルメンツが提供する他のソリューションと比較します。

WEBENCH Power Designerでは、カスタマイズされた回路図と部品リストを、リアルタイムの価格と部品の在庫情報と併せて参照できます。

ほとんどの場合、次の操作を実行可能です。

- 電気的なシミュレーションを実行し、重要な波形と回路の性能を確認する。
- 熱シミュレーションを実行し、基板の熱特性を把握する。
- カスタマイズされた回路図やレイアウトを、一般的なCADフォーマットでエクスポートする。
- 設計のレポートをPDFで印刷し、同僚と設計を共有する。

WEBENCHツールの詳細は、www.ti.com/WEBENCHでご覧になれます。

11.2 デバイス・サポート

11.2.1 開発サポート

WEBENCHソフトウェアは、反復設計手順を使用し、コンポーネントの包括的なデータベースにアクセスします。詳細については、www.ti.com/webenchをご覧ください。

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11.3 ドキュメントのサポート

11.3.1 関連資料

このセクションでは、追加のドキュメント・サポートを紹介します。

- *『LMZ1およびLMZ2パワー・モジュールの設計の概要』*、SNAA214
- *『LMZ14203 SIMPLE SWITCHERパワー・モジュール用の反転アプリケーション』*、SNVA425
- *『評価ボード・アプリケーション・ノートAN-2024』*、SNVA422
- *『ハンダ付けの絶対最大定格』*、SNOA549

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11.5 コミュニティ・リソース

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設計サポート ***TIの設計サポート*** **役に立つE2Eフォーラムや、設計サポート・ ツールをすばやく見つけることができます。技術サポート用の連絡先情報も参照できます。**

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11.8 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。この情報は、そのデバイスについて利用可能な最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LMZ14203TZ-ADJ/NO.A	Active	Production	TO-PMOD (NDW) | 7	250 | SMALL T&R	Yes	SN	Level-3-245C-168 HR	-40 to 125	LMZ14203 TZ-ADJ
LMZ14203TZ-ADJ/NOPB	Active	Production	TO-PMOD (NDW) | 7	250 | SMALL T&R	Yes	SN	Level-3-245C-168 HR	-40 to 125	LMZ14203 TZ-ADJ
LMZ14203TZE-ADJ/NO.A	Active	Production	TO-PMOD (NDW) | 7	45 | TUBE	Yes	SN	Level-3-245C-168 HR	-40 to 125	LMZ14203 TZ-ADJ
LMZ14203TZE-ADJ/NOPB	Active	Production	TO-PMOD (NDW) | 7	45 | TUBE	Yes	SN	Level-3-245C-168 HR	-40 to 125	LMZ14203 TZ-ADJ
LMZ14203TZX-ADJ/NO.A	Active	Production	TO-PMOD (NDW) | 7	500 | LARGE T&R	Yes	SN	Level-3-245C-168 HR	-40 to 125	LMZ14203 TZ-ADJ
LMZ14203TZX-ADJ/NOPB	Active	Production	TO-PMOD (NDW) | 7	500 | LARGE T&R	Yes	SN	Level-3-245C-168 HR	-40 to 125	LMZ14203 TZ-ADJ

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

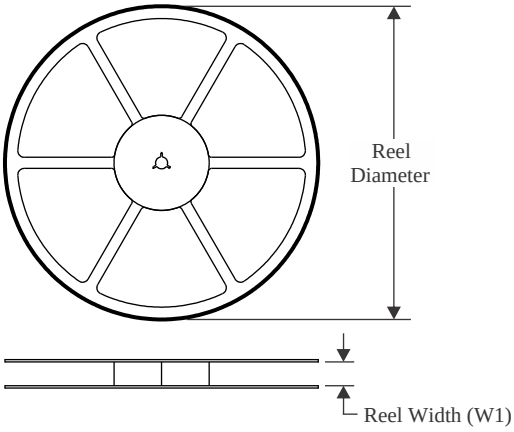
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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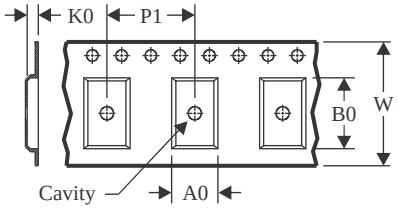
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TAPE AND REEL INFORMATION

REEL DIMENSIONS

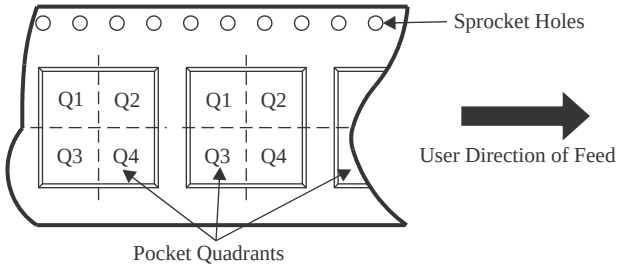


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

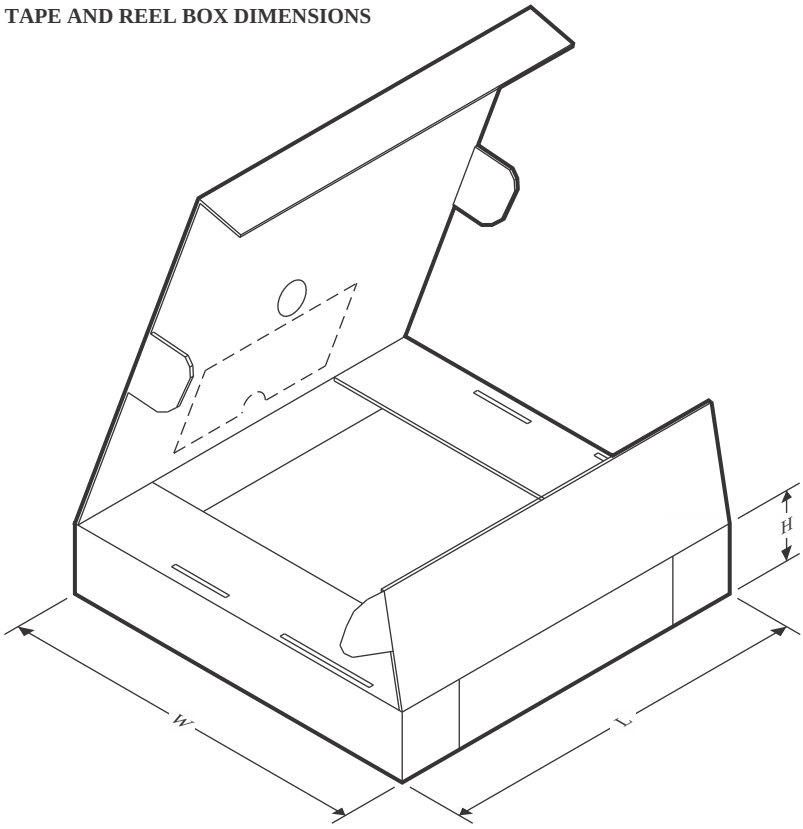
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMZ14203TZ-ADJ/NOPB	TO-PMOD	NDW	7	250	330.0	24.4	10.6	14.22	5.0	16.0	24.0	Q2
LMZ14203TZX-ADJ/NOPB	TO-PMOD	NDW	7	500	330.0	24.4	10.6	14.22	5.0	16.0	24.0	Q2

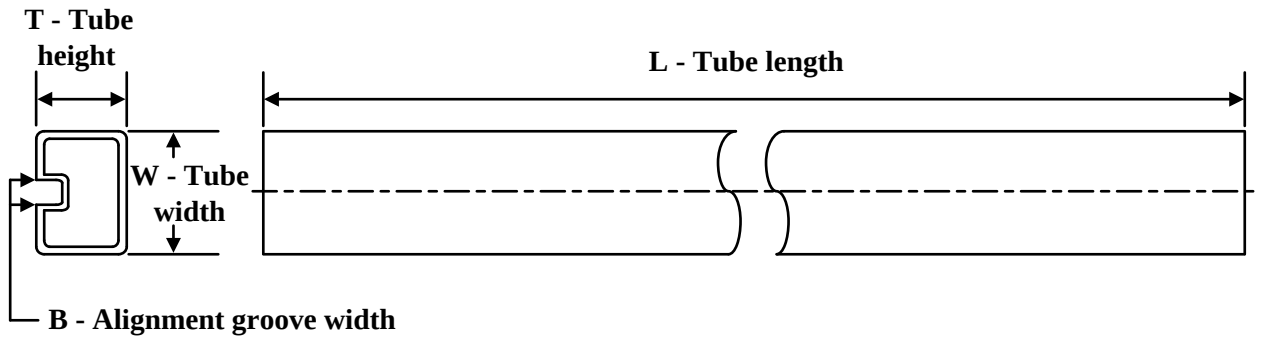
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMZ14203TZ-ADJ/NOPB	TO-PMOD	NDW	7	250	356.0	356.0	45.0
LMZ14203TZX-ADJ/NOPB	TO-PMOD	NDW	7	500	356.0	356.0	45.0

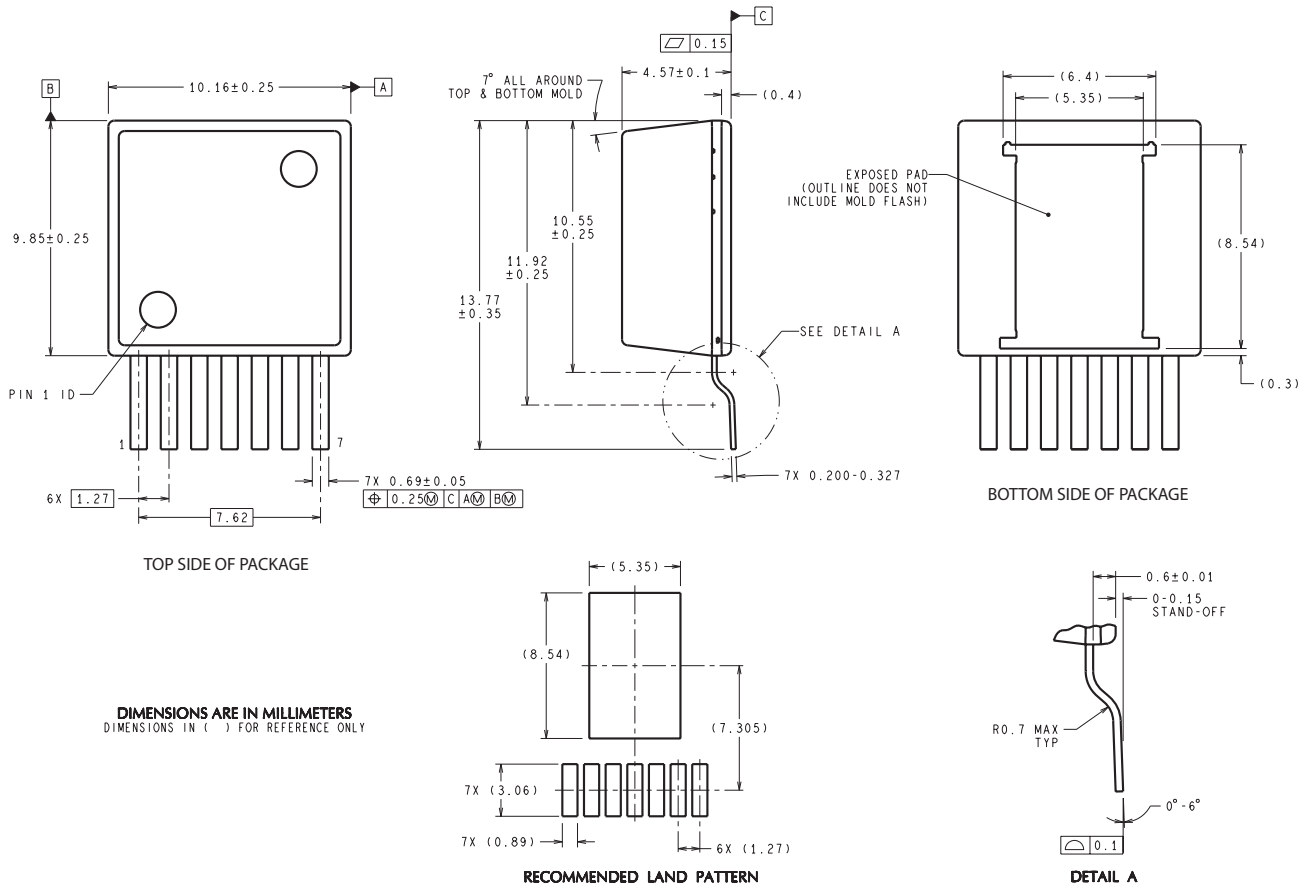
TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
LMZ14203TZE-ADJ/NO.A	NDW	TO-PMOD	7	45	502	17	6700	8.4
LMZ14203TZE-ADJ/NOPB	NDW	TO-PMOD	7	45	502	17	6700	8.4

NDW0007A



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