参考資料

Texas Instruments

LMZ30606
JAJSBU9B – JULY 2013 – REVISED APRIL 2018

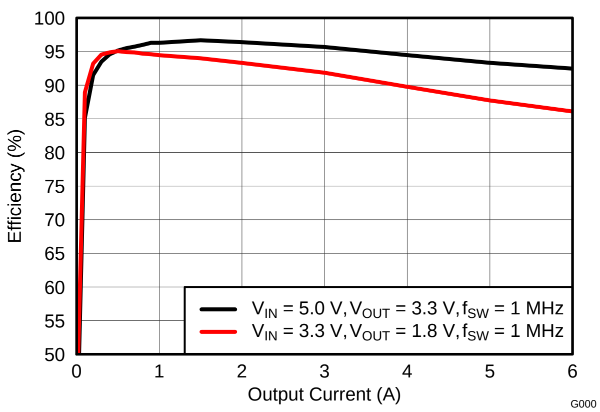
LMZ30606 6A、2.95V～6V入力、QFNパッケージのパワー・モジュール

1 特長

- 小さな占有面積で低プロファイルの設計を可能にする完全な統合電源ソリューション
- 9mm×11mm×2.8mmのパッケージ
  - LMZ30602およびLMZ30604とピン互換
- 最高96%の効率
- 出力電圧を0.8V～3.6Vの広い範囲で設定可能、リファレンス精度±1%
- 可変スイッチング周波数(500kHz～2MHz)
- 外部クロックに同期
- 調整可能なスロー・スタート
- 出力電圧シーケンシング/トラッキング
- パワー・グッド出力
- 低電圧誤動作防止(UVLO)をプログラム可能
- 出力過電流保護
- 過熱保護機能
- 動作温度範囲: -40℃～85℃
- 強化された熱特性: 12℃/W
- EN55022 Class Bの放射要件に準拠
  - シールド付きインダクタを内蔵
- WEBENCH® Power Designerにより、LMZ30606を使用するカスタム設計を作成

2 アプリケーション

- ブロードバンドおよび通信インフラストラクチャ
- 自動試験機器/医療用機器
- Compact PCI、PCI Express、PXI Express
- DSPおよびFPGAのポイント・オブ・ロード・アプリケーション
- 高密度分散電源システム



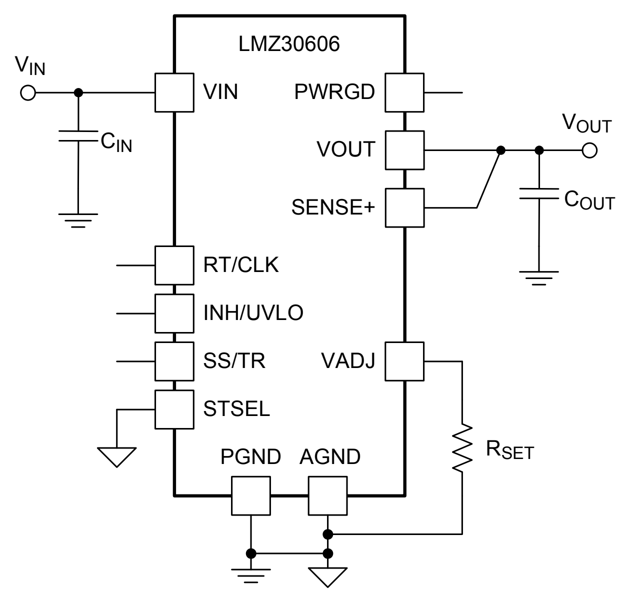
3 概要

LMZ30606 SIMPLE SWITCHER®パワー・モジュールは、使いやすい統合型パワー・ソリューションで、6AのDC/DCコンバータとパワーMOSFET、シールド付きインダクタ、パッシブ部品を組み合わせて、低プロファイルのQFNパッケージに実装しています。外部部品は3個しか使用せず、ループ補償や磁気部品の選択プロセスも不要になります。

9mm×11mm×2.8mmのQFNパッケージはプリント基板にハンダ付けしやすく、小型のポイント・オブ・ロード設計で、90%を超える効率、優れた消費電力、接合部から周囲へ12℃/Wの熱インピーダンスを実現できます。このデバイスは、周囲温度85℃において無気流でも、6Aの定格出力電流を完全に供給できます。

LMZ30606は、ディスクリートPOL設計と同等の柔軟性および機能セットを備え、高性能DSPおよびFPGAへの電力供給に最適です。先進のパッケージング技術により、標準のQFN実装/試験手法に対応した、堅牢で信頼性の高い電源ソリューションを実現できます。

アプリケーション概略図



English Data Sheet: SNVS995

Table 1. Ordering Information

For the most current package and ordering information, see the Package Option Addendum at the end of this datasheet, or see the TI website at www.ti.com.

4 Specifications

4.1 Absolute Maximum Ratings[1]

over operating temperature range (unless otherwise noted)

			VALUE MIN	VALUE MAX	UNIT
Input Voltage	VIN, PWRGD		–0.3	7	V
	INH/UVLO, RT/CLK		–0.3	3.3	V
	SS/TR, STSEL, VADJ		–0.3	3	V
	SENSE+	VADJ rating must also be met	-0.3	V_{OUT}	V
Output Voltage	PH		–0.6	7	V
	PH 10 ns, transient		–2	7	V
	VOUT		-0.6	VIN	V
V_{DIFF} (GND to exposed thermal pad)			–0.2	0.2	V
Source Current	RT/CLK, INH/UVLO			±100	µA
	PH			Current Limit	A
Sink Current	PH			Current Limit	A
	SS/TR			±100	µA
	PWRGD			10	mA
Operating Junction Temperature			–40	125[2]	°C
Storage Temperature, T_{stg}			–65	150	°C
Peak Reflow Case Temperature[3]				250[4]	°C
Maximum Number of Reflows Allowed[3]				3[4]	
Mechanical Shock	Mil-STD-883D, Method 2002.3, 1 msec, 1/2 sine, mounted			1500	G
Mechanical Vibration	Mil-STD-883D, Method 2007.2, 20-2000Hz			20	G

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) See the temperature derating curves in the Typical Characteristics section for thermal information.
(3) For soldering specifications, refer to the Soldering Requirements for BQFN Packages application note.
(4) Devices with a date code prior to week 14 2018 (1814) have a peak reflow case temperature of 240°C with a maximum of one reflow.

4.2 Thermal Information

THERMAL METRIC[1]		LMZ30606 RKG39 39 PINS	UNIT
θ_{JA}	Junction-to-ambient thermal resistance[2]	12	°C/W
ψ_{JT}	Junction-to-top characterization parameter[3]	2.2	°C/W
ψ_{JB}	Junction-to-board characterization parameter[4]	9.7	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics (SPRA953) application report.
(2) The junction-to-ambient thermal resistance, θ_{JA}, applies to devices soldered directly to a 100 mm x 100 mm double-sided PCB with 1 oz. copper and natural convection cooling. Additional airflow reduces θ_{JA}.
(3) The junction-to-top characterization parameter, ψ_{JT}, estimates the junction temperature, T_J, of a device in a real system, using a procedure described in JESD51-2A (sections 6 and 7). $T_J = \psi_{JT} * Pdis + T_T$; where Pdis is the power dissipated in the device and T_T is the temperature of the top of the device.
(4) The junction-to-board characterization parameter, ψ_{JB}, estimates the junction temperature, T_J, of a device in a real system, using a procedure described in JESD51-2A (sections 6 and 7). $T_J = \psi_{JB} * Pdis + T_B$; where Pdis is the power dissipated in the device and T_B is the temperature of the board 1mm from the device.

4.3 Electrical Characteristics

Over -40°C to 85°C free-air temperature, VIN = 3.3 V, V_{OUT} = 1.8 V, I_{OUT} = 6A,
C_{IN1} = 47 µF ceramic, C_{IN2} = 220 µF poly-tantalum, C_{OUT1} = 47 µF ceramic, C_{OUT2} = 100 µF poly-tantalum (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
I_{OUT}	Output current	T_A = 85°C, natural convection		0		6	A
V_{IN}	Input voltage range	Over I_{OUT} range		2.95[1]		6	V
UVLO	VIN Undervoltage lockout	VIN = increasing			3.05	3.135	V
		VIN = decreasing		2.5	2.75		
$V_{OUT(adj)}$	Output voltage adjust range	Over I_{OUT} range		0.8		3.6	V
V_{OUT}	Set-point voltage tolerance	T_A = 25°C, I_{OUT} = 0A				±1.0% [2]	
	Temperature variation	-40°C ≤ T_A ≤ +85°C, I_{OUT} = 0A			±0.3%		
	Line regulation	Over VIN range, T_A = 25°C, I_{OUT} = 0A			±0.1%		
	Load regulation	Over I_{OUT} range, T_A = 25°C			±0.1%		
	Total output voltage variation	Includes set-point, line, load, and temperature variation				±1.5% [2]	
η	Efficiency	VIN = 5 V, I_O = 3 A	V_{OUT} = 3.3V, f_{SW} = 1 MHz		96%		
			V_{OUT} = 2.5V, f_{SW} = 1 MHz		94%		
			V_{OUT} = 1.8V, f_{SW} = 1 MHz		92%		
			V_{OUT} = 1.5V, f_{SW} = 1 MHz		90%		
			V_{OUT} = 1.2V, f_{SW} =750 kHz		89%		
			V_{OUT} = 1.0V, f_{SW} = 650 kHz		87%		
			V_{OUT} = 0.8V, f_{SW} = 650 kHz		85%		
		VIN = 3.3V, I_O = 3 A	V_{OUT} = 1.8V, f_{SW} = 1 MHz		92%		
			V_{OUT} = 1.5V, f_{SW} = 1 MHz		90%		
			V_{OUT} = 1.2V, f_{SW} = 750 kHz		89%		
			V_{OUT} = 1.0V, f_{SW} = 650 kHz		87%		
			V_{OUT} = 0.8V, f_{SW} = 650 kHz		85%		
	Output voltage ripple	20 MHz bandwith			10		mV_{PP}
I_{LIM}	Overcurrent threshold				9		A
	Transient response	1.0 A/µs load step from 1.5A to 4.5A	Recovery time		80		µs
			V_{OUT} over/undershoot		120		mV
V_{INH-H}	Inhibit Control	Inhibit High Voltage			1.25	Open [3]	V
V_{INH-L}		Inhibit Low Voltage		–0.3		1.0	
$I_{I(stby)}$	Input standby current	INH pin to AGND			70	100	µA
Power Good	PWRGD Thresholds	V_{OUT} rising	Good		93%		
			Fault		109%		
		V_{OUT} falling	Fault		91%		
			Good		107%		
	PWRGD Low Voltage	I(PWRGD) = 0.33 mA				0.3	V
f_{SW}	Switching frequency	Over VIN and I_{OUT} ranges, RT/CLK pin OPEN		400	500	600	kHz
f_{CLK}	Synchronization frequency	CLK Control		500		2000	kHz
V_{CLK-H}	CLK High-Level Threshold			2.2		3.3	V
V_{CLK-L}	CLK Low-Level Threshold			-0.3		0.4	V
CLK_PW	CLK Pulse Width			75[4]			ns
	Thermal Shutdown	Thermal shutdown			170		°C
		Thermal shutdown hysteresis			20		°C

(1) The minimum VIN depends on V_{OUT} and the switching frequency. Please refer to Table 9 for operating limits.
(2) The stated limit of the set-point voltage tolerance includes the tolerance of both the internal voltage reference and the internal adjustment resistor. The overall output voltage tolerance will be affected by the tolerance of the external R_{SET} resistor.
(3) This control pin has an internal pullup. Do not place an external pull-up resistor on this pin. If this pin is left open circuit, the device operates when input power is applied. A small low-leakage MOSFET is recommended for control. See the application section for further guidance.
(4) The maximum synchronization clock pulse width is dependant on VIN, V_{OUT}, and the synchronization frequency. See the Synchronization (CLK) section for more information.

Electrical Characteristics (continued)

Over -40°C to 85°C free-air temperature, VIN = 3.3 V, V_{OUT} = 1.8 V, I_{OUT} = 6A,
C_{IN1} = 47 µF ceramic, C_{IN2} = 220 µF poly-tantalum, C_{OUT1} = 47 µF ceramic, C_{OUT2} = 100 µF poly-tantalum (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
C_{IN}	External input capacitance	Ceramic	47 (5)			µF
		Non-ceramic		220(5)		
C_{OUT}	External output capacitance	Ceramic	47 (6)	150	650(7)	µF
		Non-ceramic		100(6)	2000(7)	
		Equivalent series resistance (ESR)			25	mΩ

(5) A minimum of 47µF of ceramic capacitance is required across the input for proper operation. Locate the capacitor close to the device. An additional 220µF of bulk capacitance is recommended. See Table 6 for more details.
(6) The amount of required output capacitance varies depending on the output voltage (see Table 5). The amount of required capacitance must include at least 47µF of ceramic capacitance. Locate the capacitance close to the device. Adding additional capacitance close to the load improves the response of the regulator to load transients. See Table 5 and Table 6 for more details.
(7) When using both ceramic and non-ceramic output capacitance, the combined maximum must not exceed 2200µF.

4.4 Package Specifications

LMZ30606		UNIT
Weight		0.85 grams
Flammability	Meets UL 94 V-O	
MTBF Calculated reliability	Per Bellcore TR-332, 50% stress, T_A = 40°C, ground benign	32.8 MHrs

5 Device Information

FUNCTIONAL BLOCK DIAGRAM

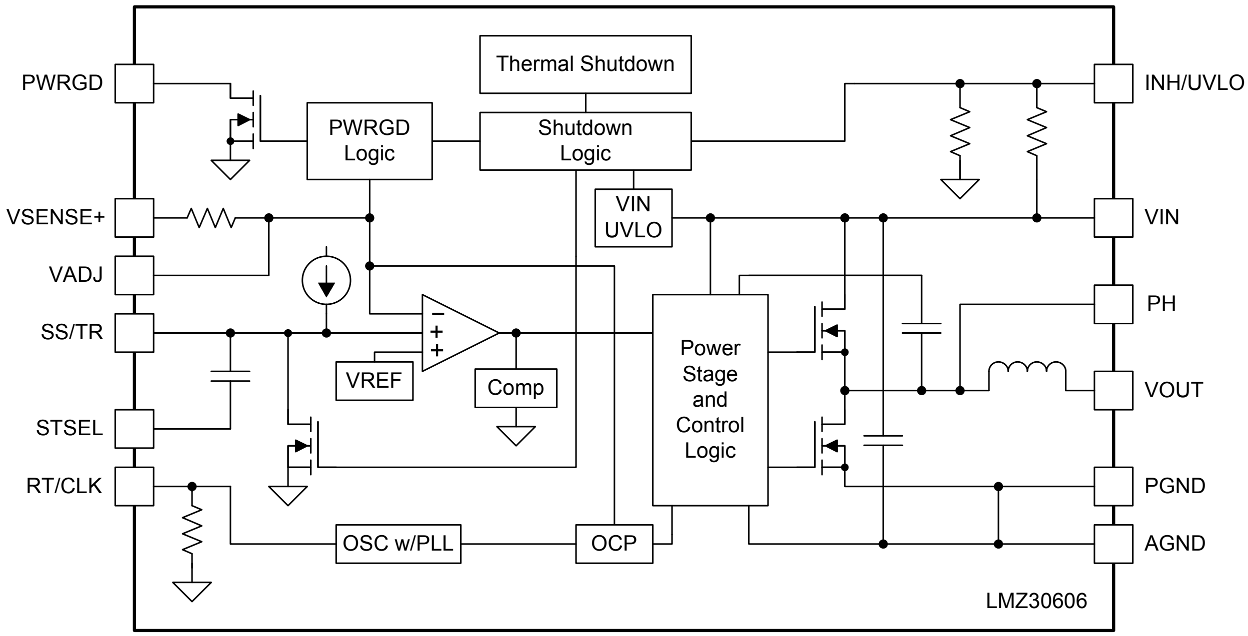
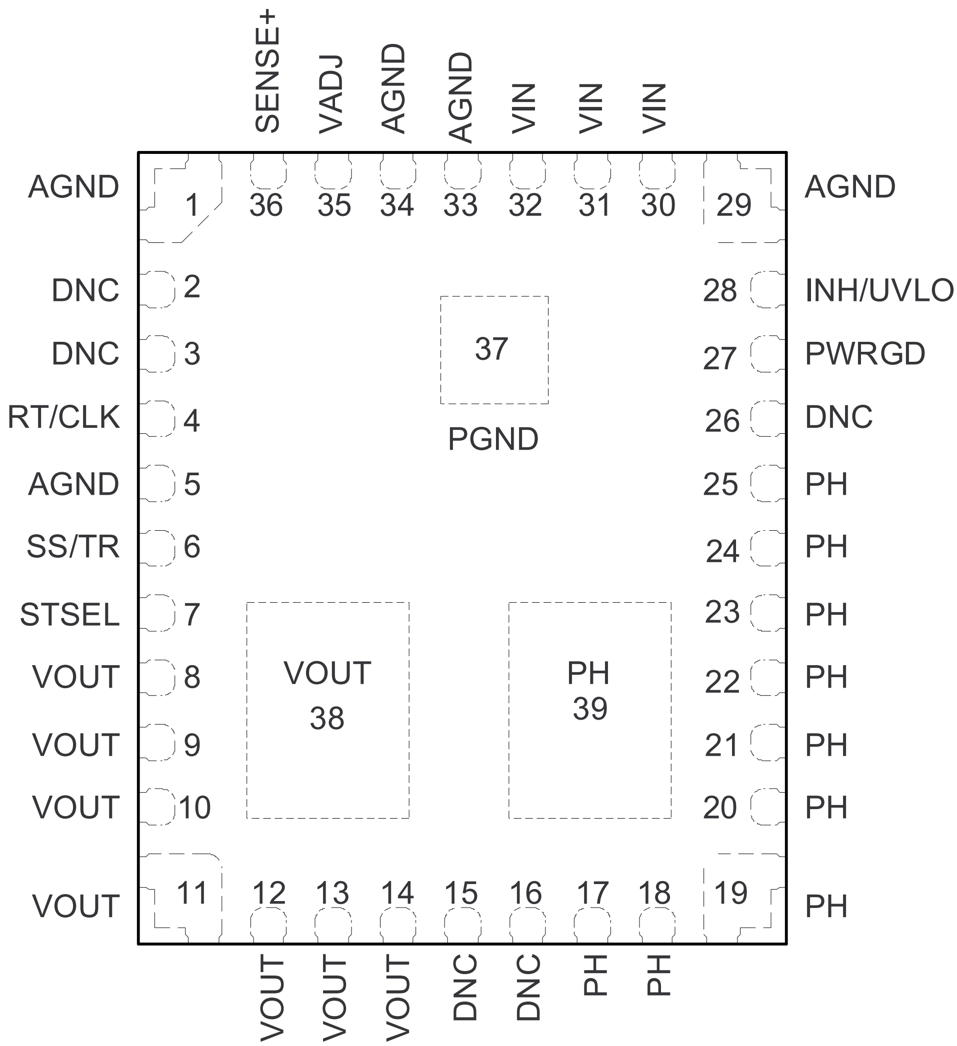


Table 2. PIN DESCRIPTIONS

TERMINAL		DESCRIPTION
NAME	NO.	
AGND	1	Zero VDC reference for the analog control circuitry. These pins should be connected directly to the PCB analog ground plane. Not all pins are connected together internally. All pins must be connected together externally with a copper plane or pour directly under the module. Connect the AGND copper area to the PGND copper area at a single point; directly at the pin 37 PowerPAD using multiple vias. See the recommended layout in Figure 36.
	5	
	29	
	33	
	34	
PowerPAD (PGND)	37	This pad provides both an electrical and thermal connection to the PCB. This pad should be connected directly to the PCB power ground plane using multiple vias for good electrical and thermal performance. The same vias should also be used to connect to the PCB analog ground plane. See the recommended layout in Figure 36.
DNC	2	Do Not Connect. Do not connect these pins to AGND, to another DNC pin, or to any other voltage. These pins are connected to internal circuitry. Each pin must be soldered to an isolated pad.
	3	
	15	
	16	
	26	
INH/UVLO	28	Inhibit and UVLO adjust pin. Use an open drain or open collector output logic to control the INH function. A resistor between this pin and AGND adjusts the UVLO voltage.
PH	17	Phase switch node. These pins should be connected by a small copper island under the device for thermal relief. Do not connect any external component to this pin or tie it to a pin of another function.
	18	
	19	
	20	
	21	
	22	
	23	
	24	
	25	
	39	
PWRGD	27	Power good fault pin. Asserts low if the output voltage is out of tolerance. A pull-up resistor is required.
RT/CLK	4	This pin automatically selects between RT mode and CLK mode. An external timing resistor adjusts the switching frequency of the device. In CLK mode, the device synchronizes to an external clock.
SENSE+	36	Remote sense connection. Connect this pin to VOUT at the load for improved regulation. This pin must be connected to VOUT at the load, or at the module pins.
SS/TR	6	Slow-start and tracking pin. Connecting an external capacitor to this pin adjusts the output voltage rise time. A voltage applied to this pin allows for tracking and sequencing control.
STSEL	7	Slow-start or track feature select. Connect this pin to AGND to enable the internal SS capacitor with a SS interval of approximately 1.1 ms. Leave this pin open to enable the TR feature.
VADJ	35	Connecting a resistor between this pin and AGND sets the output voltage above the 0.8V default voltage.
VIN	30	The positive input voltage power pins, which are referenced to PGND. Connect external input capacitance between these pins and the PGND plane, close to the device.
	31	
	32	
VOUT	8	Output voltage. Connect output capacitors between these pins and the PGND plane, close to the device.
	9	
	10	
	11	
	12	
	13	
	14	
	38	

RKG PACAKGE
39 PINS
(TOP VIEW)



6 Typical Characteristics (VIN = 5 V)

The electrical characteristic data has been developed from actual products tested at 25°C. This data is considered typical for the converter. Applies to Figure 1, Figure 2, and Figure 3. The temperature derating curves represent the conditions at which internal components are at or below the manufacturer's maximum operating temperatures. Derating limits apply to devices soldered directly to a 100 mm × 100 mm double-sided PCB with 1 oz. copper. Applies to Figure 4.

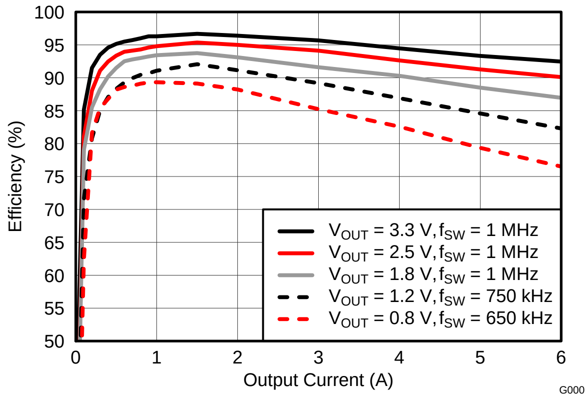


Figure 1. Efficiency vs. Output Current

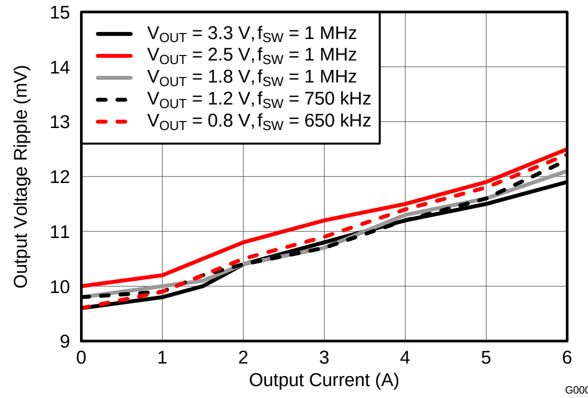


Figure 2. Voltage Ripple vs. Output Current

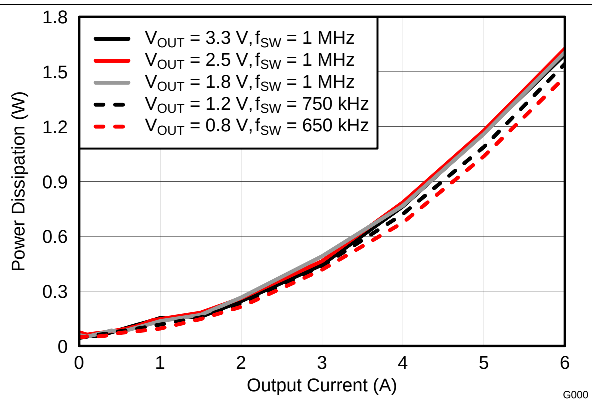


Figure 3. Power Dissipation vs. Output Current

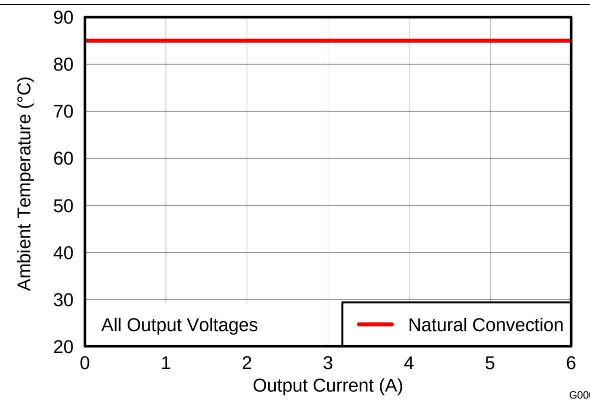


Figure 4. Safe Operating Area

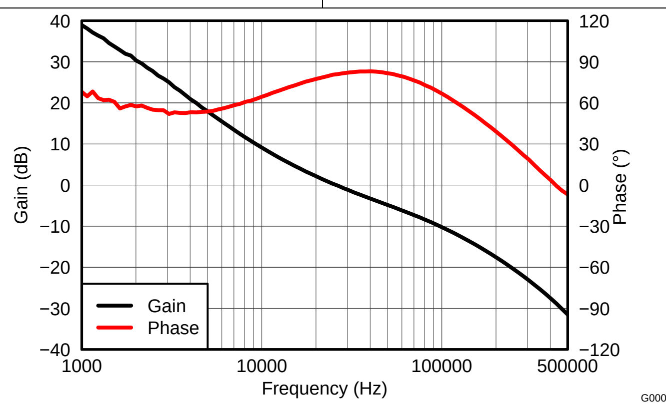


Figure 5. V_{OUT}= 1.8 V, I_{OUT}= 6 A, C_{OUT1}= 47 µF ceramic, C_{OUT2}= 100 µF POSCAP, f_{SW}= 1 MHz

7 Typical Characteristics (VIN = 3.3 V)

The electrical characteristic data has been developed from actual products tested at 25°C. This data is considered typical for the converter. Applies to Figure 6, Figure 7, and Figure 8. The temperature derating curves represent the conditions at which internal components are at or below the manufacturer's maximum operating temperatures. Derating limits apply to devices soldered directly to a 100 mm × 100 mm double-sided PCB with 1 oz. copper. Applies to Figure 9.

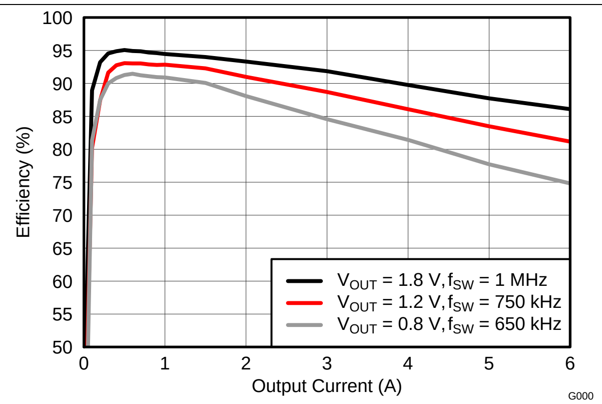


Figure 6. Efficiency vs. Output Current

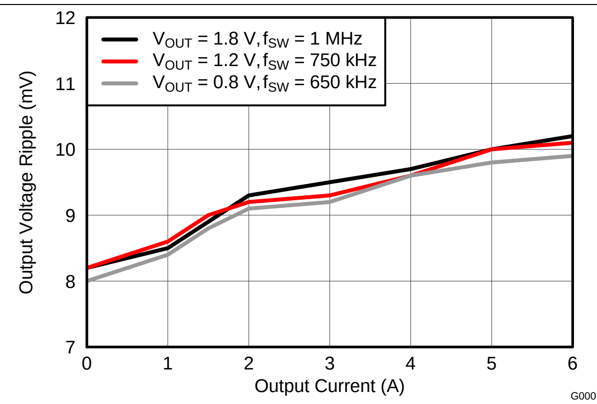


Figure 7. Voltage Ripple vs. Output Current

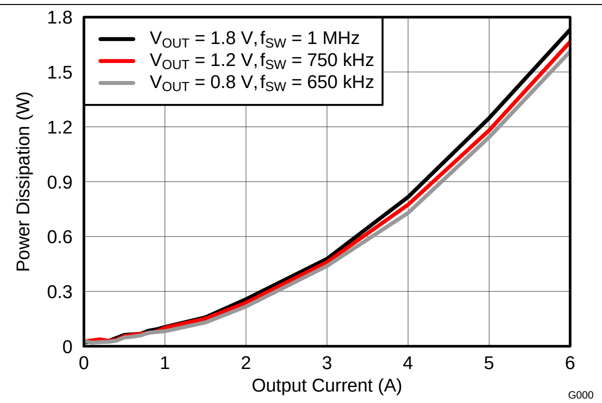


Figure 8. Power Dissipation vs. Output Current

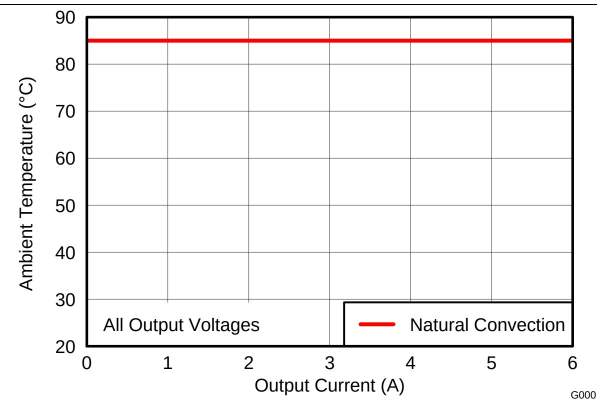


Figure 9. Safe Operating Area

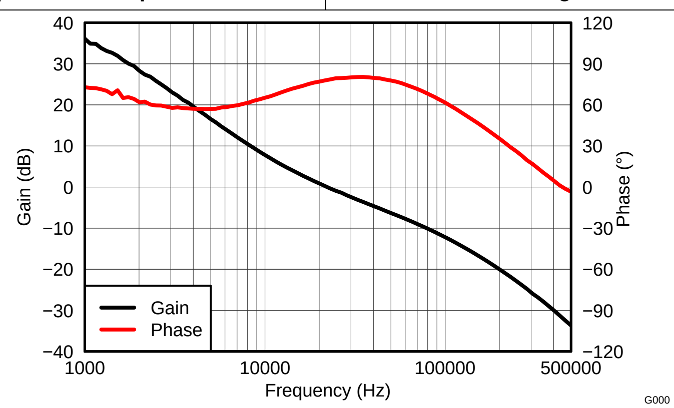


Figure 10. V_{OUT}= 1.8 V, I_{OUT}= 6 A, C_{OUT1}= 47 µF ceramic, C_{OUT2}= 100 µF POSCAP, f_{SW}= 1 MHz

8 Application Information

8.1 Adjusting the Output Voltage

The VADJ control sets the output voltage of the LMZ30606. The output voltage adjustment range is from 0.8V to 3.6V. The adjustment method requires the addition of R_{SET}, which sets the output voltage, the connection of SENSE+ to VOUT, and in some cases R_{RT} which sets the switching frequency. The R_{SET} resistor must be connected directly between the VADJ (pin 35) and AGND (pin 33 & 34). The SENSE+ pin (pin 36) must be connected to VOUT either at the load for improved regulation or at VOUT of the module. The R_{RT} resistor must be connected directly between the RT/CLK (pin 4) and AGND (pins 33 & 34).

Table 3 gives the standard external R_{SET} resistor for a number of common bus voltages, along with the recommended R_{RT} resistor for that output voltage.

Table 3. Standard R_{SET} Resistor Values for Common Output Voltages

RESISTORS	OUTPUT VOLTAGE V_{OUT} (V)					
	0.8	1.2	1.5	1.8	2.5	3.3
R_{SET} (kΩ)	open	2.87	1.65	1.15	0.673	0.459
R_{RT} (kΩ)	1200	715	348	348	348	348

For other output voltages, the value of the required resistor can either be calculated using the following formula, or simply selected from the range of values given in Table 4.

$$R_{SET} = \frac{1.43}{\left(\left(\frac{V_{OUT}}{0.799}\right) - 1\right)} \ (k\Omega) \tag{1}$$

Table 4. Standard R_{SET} Resistor Values

V_{OUT} (V)	R_{SET} (kΩ)	R_{RT} (kΩ)	f_{SW} (kHz)	V_{OUT} (V)	R_{SET} (kΩ)	R_{RT} (kΩ)	f_{SW} (kHz)
0.8	open	1200	650	2.3	0.768	348	1000
0.9	11.8	1200	650	2.4	0.715	348	1000
1.0	5.83	1200	650	2.5	0.673	348	1000
1.1	3.83	1200	650	2.6	0.634	348	1000
1.2	2.87	715	750	2.7	0.604	348	1000
1.3	2.32	715	750	2.8	0.576	348	1000
1.4	1.91	715	750	2.9	0.549	348	1000
1.5	1.65	348	1000	3.0	0.523	348	1000
1.6	1.43	348	1000	3.1	0.499	348	1000
1.7	1.27	348	1000	3.2	0.475	348	1000
1.8	1.15	348	1000	3.3	0.459	348	1000
1.9	1.05	348	1000	3.4	0.442	348	1000
2.0	0.953	348	1000	3.5	0.422	348	1000
2.1	0.845	348	1000	3.6	0.412	348	1000
2.2	0.825	348	1000				

8.2 Capacitor Recommendations for theLMZ30606 Power Supply

8.2.1 Capacitor Technologies

8.2.1.1 Electrolytic, Polymer-Electrolytic Capacitors

When using electrolytic capacitors, high-quality, computer-grade electrolytic capacitors are recommended. Polymer-electrolytic type capacitors are recommended for applications where the ambient operating temperature is less than 0°C. The Sanyo OS-CON capacitor series is suggested due to the lower ESR, higher rated surge, power dissipation, ripple current capability, and small package size. Aluminum electrolytic capacitors provide adequate decoupling over the frequency range of 2 kHz to 150 kHz, and are suitable when ambient temperatures are above 0°C.

8.2.1.2 Ceramic Capacitors

The performance of aluminum electrolytic capacitors is less effective than ceramic capacitors above 150 kHz. Multilayer ceramic capacitors have a low ESR and a resonant frequency higher than the bandwidth of the regulator. They can be used to reduce the reflected ripple current at the input as well as improve the transient response of the output.

8.2.1.3 Tantalum, Polymer-Tantalum Capacitors

Polymer-tantalum type capacitors are recommended for applications where the ambient operating temperature is less than 0°C. The Sanyo POSCAP series and Kemet T530 capacitor series are recommended rather than many other tantalum types due to their lower ESR, higher rated surge, power dissipation, ripple current capability, and small package size. Tantalum capacitors that have no stated ESR or surge current rating are not recommended for power applications.

8.2.2 Input Capacitor

The LMZ30606 requires a minimum input capacitance of 47 μF of ceramic capacitance. An additional 220 μF polymer-tantalum capacitor is recommended for applications with transient load requirements. The combined ripple current rating of the input capacitors must be at least 3000 mArms. Table 6 includes a preferred list of capacitors by vendor. For applications where the ambient operating temperature is less than 0°C, an additional 1 μF, X5R or X7R ceramic capacitor placed between VIN and AGND is recommended.

8.2.3 Output Capacitor

The required output capacitance is determined by the output voltage of the LMZ30606. See Table 5 for the amount of required capacitance. The required output capacitance must include at least one 47 µF ceramic capacitor. For applications where the ambient operating temperature is less than 0°C, an additional 100 µF polymer-tantalum capacitor is recommended. When adding additional non-ceramic bulk capacitors, low-ESR devices like the ones recommended in Table 6 are required. The required capacitance above the minimum is determined by actual transient deviation requirements. See Table 7 for typical transient response values for several output voltage, input voltage and capacitance combinations. Table 6 includes a preferred list of capacitors by vendor.

Table 5. Required Output Capacitance

V_{OUT} RANGE (V)		MINIMUM REQUIRED C_{OUT} (µF)
MIN	MAX	
0.8	< 1.8	147 (1)
1.8	< 3.3	100 (2)
3.3	3.6	47 (2)

(1) Minimum required must include at least 1 x 47 µF ceramic capacitor plus 1 x 100 µF polymer-tantalum capacitor.
(2) Minimum required must include at least 47 µF of ceramic capacitance.

Table 6. Recommended Input/Output Capacitors[1]

VENDOR	SERIES	PART NUMBER	CAPACITOR CHARACTERISTICS		
			WORKING VOLTAGE (V)	CAPACITANCE (µF)	ESR [2] (mΩ)
Murata	X5R	GRM32ER61C476K	16	47	2
TDK	X5R	C3225X5R0J107M	6.3	100	2
Murata	X5R	GRM32ER60J107M	6.3	100	2
TDK	X5R	C3225X5R0J476K	6.3	47	2
Murata	X5R	GRM32ER60J476M	6.3	47	2
Sanyo	POSCAP	10TPE220ML	10	220	25
Kemet	T520	T520V107M010ASE025	10	100	25
Sanyo	POSCAP	6TPE100MPB	6.3	100	25
Sanyo	POSCAP	2R5TPE220M7	2.5	220	7
Kemet	T530	T530D227M006ATE006	6.3	220	6
Kemet	T530	T530D337M006ATE010	6.3	330	10
Sanyo	POSCAP	2TPF330M6	2.0	330	6
Sanyo	POSCAP	6TPE330MFL	6.3	330	15

(1) **Capacitor Supplier Verification**
Please verify availability of capacitors identified in this table.
RoHS, Lead-free and Material Details
Please consult capacitor suppliers regarding material composition, RoHS status, lead-free status, and manufacturing process requirements.
(2) Maximum ESR @ 100kHz, 25°C.

8.3 Transient Response

Table 7. Output Voltage Transient Response

C_{IN1} = 1 x 47 µF CERAMIC, C_{IN2} = 220 µF POLYMER-TANTALUM

V_{OUT} (V)	V_{IN} (V)	C_{OUT1} Ceramic	C_{OUT2} BULK	VOLTAGE DEVIATION (mV)		RECOVERY TIME (µs)
				2 A LOAD STEP, (1 A/µs)	3 A LOAD STEP, (1 A/µs)	
0.8	3.3	47 µF	330 µF	35	45	60
		47 µF	470 µF	30	40	60
	5	47 µF	330 µF	30	40	60
		47 µF	470 µF	25	35	60
1.2	3.3	47 µF	330 µF	45	65	60
		47 µF	470 µF	40	60	60
	5	47 µF	330 µF	40	65	60
		47 µF	470 µF	35	60	60
1.8	3.3	47 µF	220 µF	65	90	70
		47 µF	330 µF	60	85	70
	5	47 µF	220 µF	60	85	70
		47 µF	330 µF	50	75	70
2.5	5	3x 47 µF	-	95	150	70
		3x 47 µF	100 µF	85	125	70
3.3	5	3x 47 µF	-	120	180	70
		3x 47 µF	100 µF	100	150	70

8.3.1 Transient Waveforms

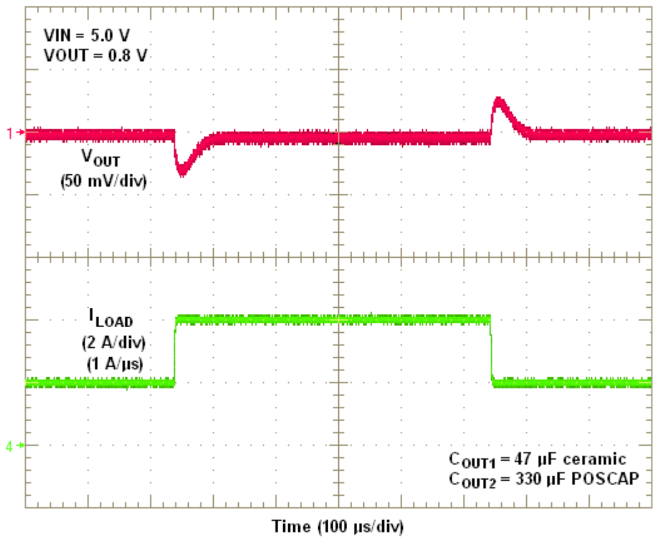


Figure 11. VIN = 5V, VOUT = 0.8V, 2A Load Step

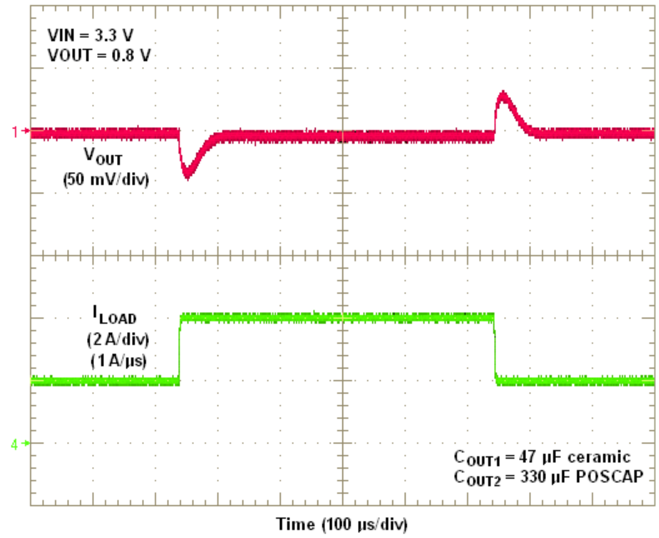


Figure 12. VIN = 3.3V, VOUT = 0.8V, 2A Load Step

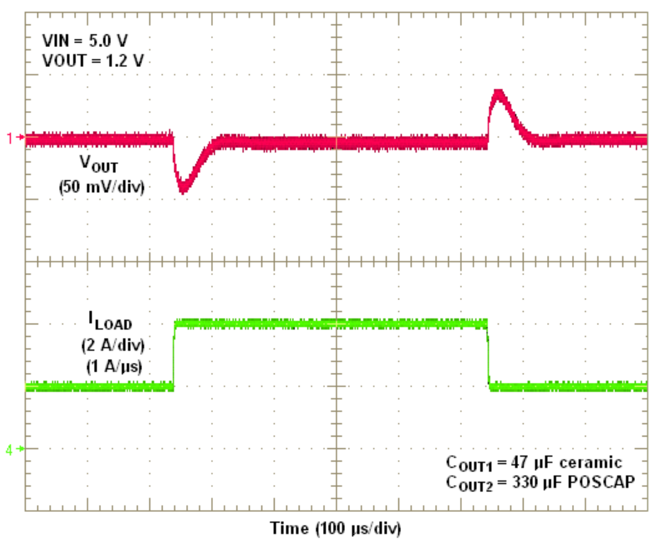


Figure 13. VIN = 5V, VOUT = 1.2V, 2A Load Step

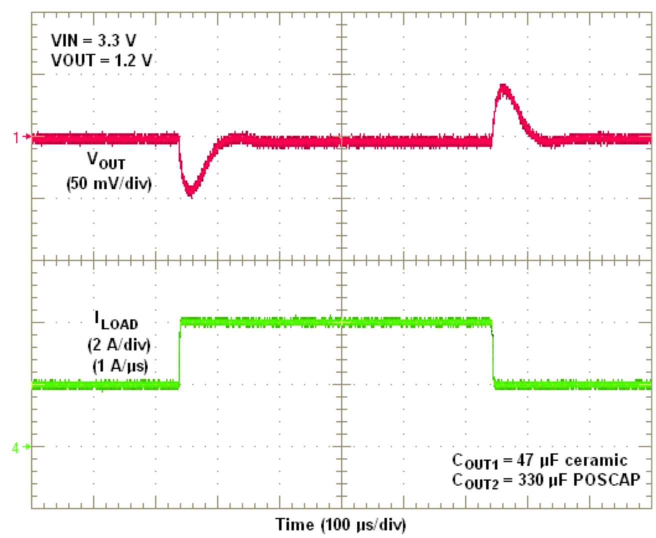


Figure 14. VIN = 3.3V, VOUT = 1.2V, 2A Load Step

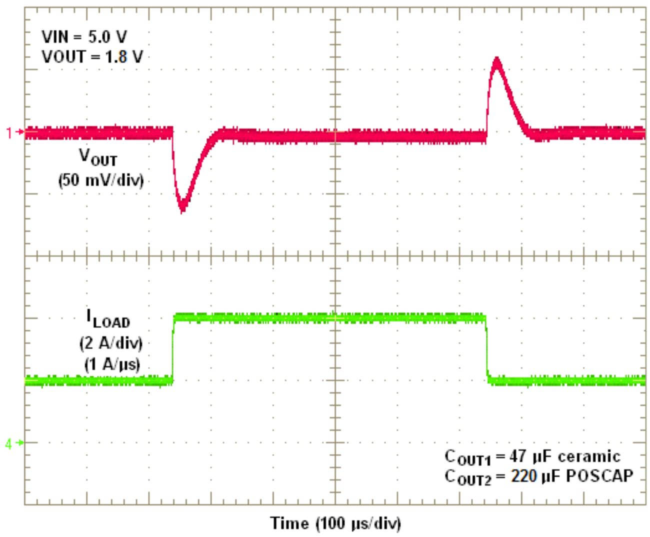


Figure 15. VIN = 5V, VOUT = 1.8V, 2A Load Step

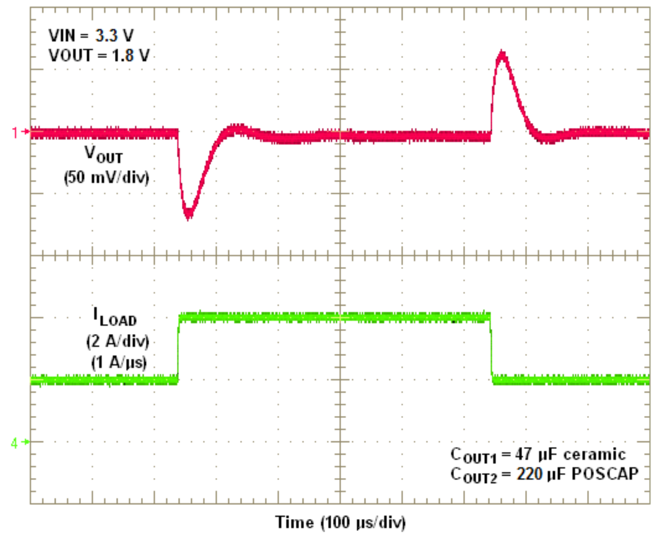


Figure 16. VIN = 3.3V, VOUT = 1.8V, 2A Load Step

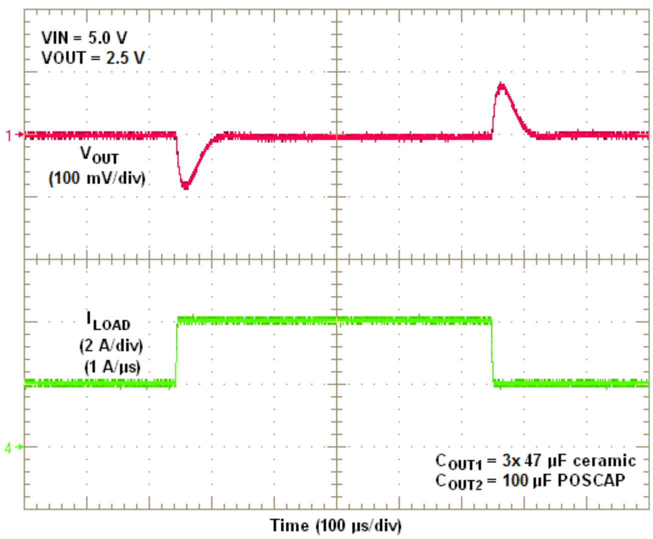


Figure 17. VIN = 5V, VOUT = 2.5V, 2A Load Step

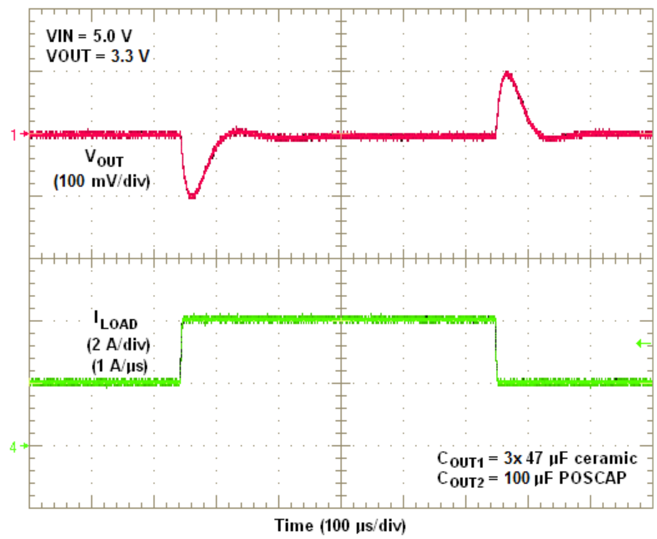


Figure 18. VIN = 5V, VOUT = 3.3V, 2A Load Step

8.4 Application Schematics

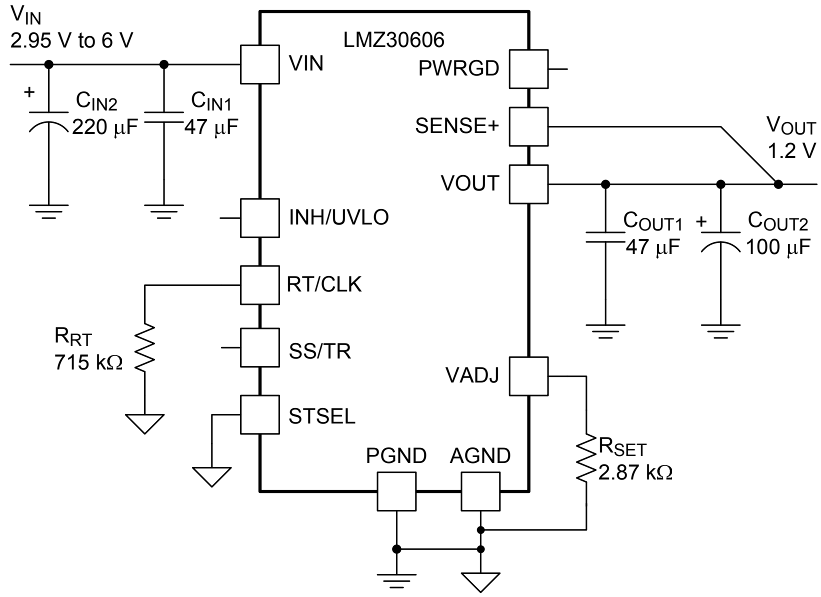


Figure 19. Typical Schematic
VIN = 2.95 V to 6.0 V, VOUT = 1.2 V

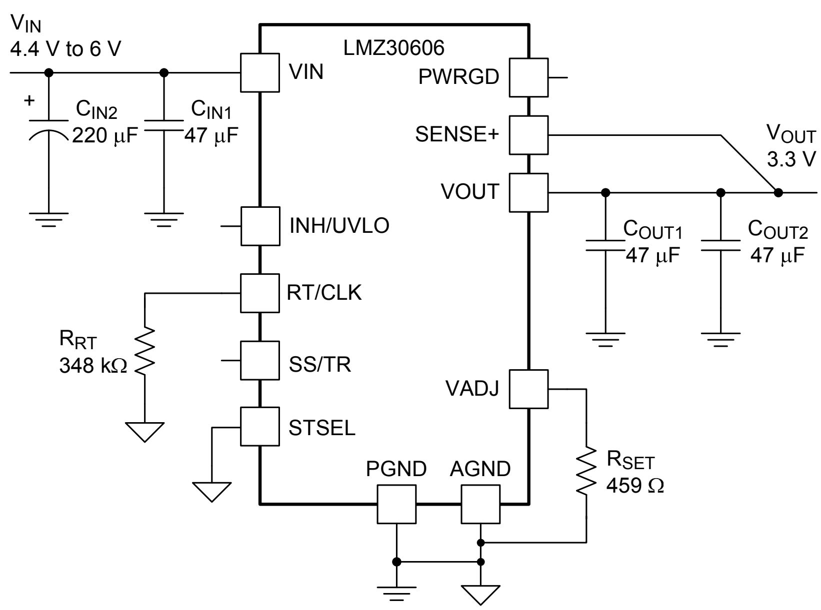


Figure 20. Typical Schematic
VIN = 4.4 V to 6.0 V, VOUT = 3.3 V

8.5 Custom Design With WEBENCH® Tools

Click here to create a custom design using the LMZ30606 device with the WEBENCH® Power Designer.

1. Start by entering the input voltage (V_{IN}), output voltage (V_{OUT}), and output current (I_{OUT}) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance
- Run thermal simulations to understand board thermal performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

8.6 Power Good (PWRGD)

The PWRGD pin is an open drain output. Once the voltage on the SENSE+ pin is between 93% and 107% of the set voltage, the PWRGD pin pull-down is released and the pin floats. The recommended pull-up resistor value is between 10 kΩ and 100 kΩ to a voltage source that is 6 V or less. The PWRGD pin is in a defined state once VIN is greater than 1.2 V, but with reduced current sinking capability. The PWRGD pin achieves full current sinking capability once the VIN pin is above 2.95V. Figure 21 shows the PWRGD waveform during power-up. The PWRGD pin is pulled low when the voltage on SENSE+ is lower than 91% or greater than 109% of the nominal set voltage. Also, the PWRGD pin is pulled low if the input UVLO or thermal shutdown is asserted, or if the INH pin is pulled low.

8.7 Power-Up Characteristics

When configured as shown in the front page schematic, the LMZ30606 produces a regulated output voltage following the application of a valid input voltage. During the power-up, internal soft-start circuitry slows the rate that the output voltage rises, thereby limiting the amount of in-rush current that can be drawn from the input source. The soft-start circuitry introduces a short time delay from the point that a valid input voltage is recognized. Figure 21 shows the start-up waveforms for a LMZ30606, operating from a 5-V input and with the output voltage adjusted to 1.8 V. The waveform is measured with a 3-A constant current load.

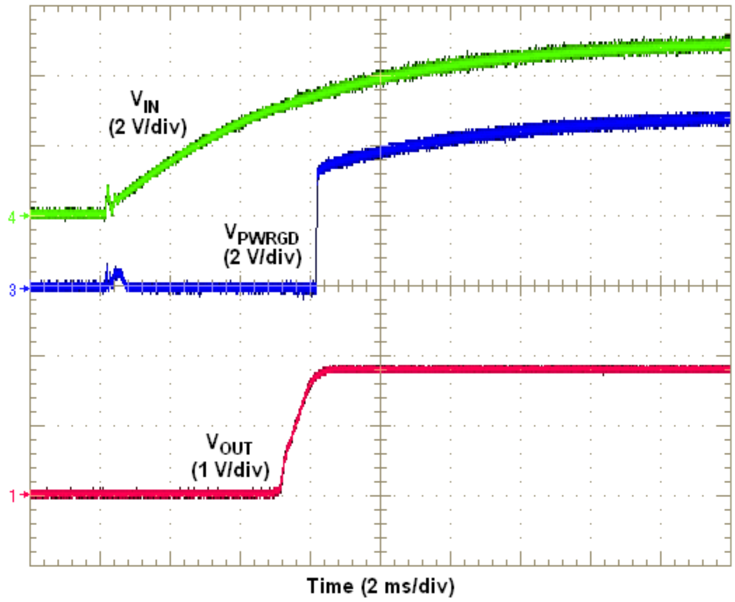


Figure 21. Start-Up Waveforms

8.8 Remote Sense

The SENSE+ pin must be connected to V_{OUT} at the load, or at the device pins.

Connecting the SENSE+ pin to V_{OUT} at the load improves the load regulation performance of the device by allowing it to compensate for any I-R voltage drop between its output pins and the load. An I-R drop is caused by the high output current flowing through the small amount of pin and trace resistance. This should be limited to a maximum of 300 mV.

NOTE

The remote sense feature is not designed to compensate for the forward drop of nonlinear or frequency dependent components that may be placed in series with the converter output. Examples include OR-ing diodes, filter inductors, ferrite beads, and fuses. When these components are enclosed by the SENSE+ connection, they are effectively placed inside the regulation control loop, which can adversely affect the stability of the regulator.

8.9 Output On/Off Inhibit (INH)

The INH pin provides electrical on/off control of the device. Once the INH pin voltage exceeds the threshold voltage, the device starts operation. If the INH pin voltage is pulled below the threshold voltage, the regulator stops switching and enters low quiescent current state.

The INH pin has an internal pull-up current source, allowing the user to float the INH pin for enabling the device. If an application requires controlling the INH pin, use an open drain/collector device, or a suitable logic gate to interface with the pin. Do not place an external pull-up resistor on this pin. Figure 22 shows the typical application of the inhibit function.

Turning Q1 on applies a low voltage to the inhibit control (INH) pin and disables the output of the supply, as shown in Figure 23. If Q1 is turned off, the supply executes a soft-start power-up sequence, as shown in Figure 24. The waveforms were measured with a 3-A constant current load.

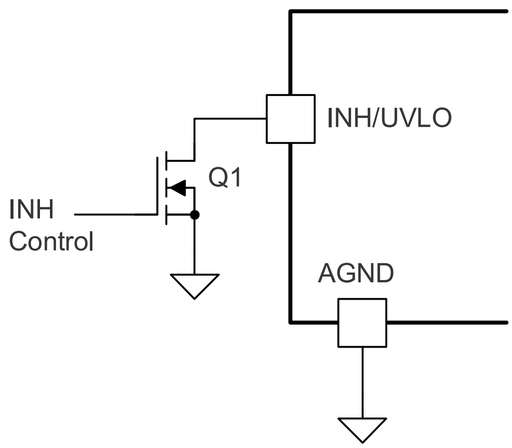


Figure 22. Typical Inhibit Control

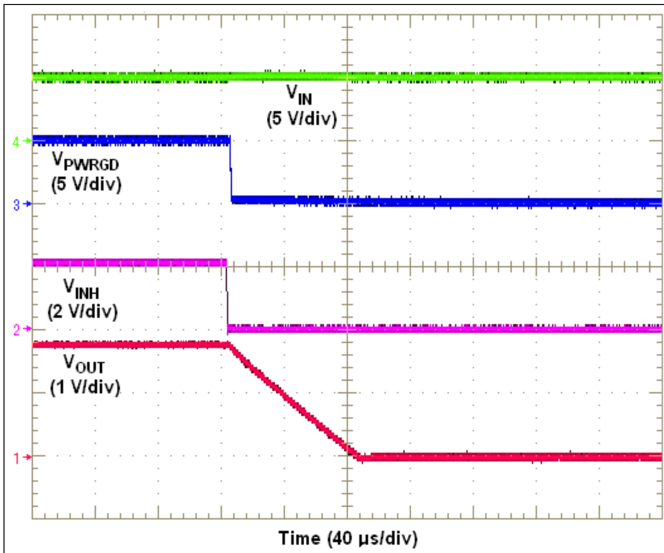


Figure 23. Inhibit Turn-Off

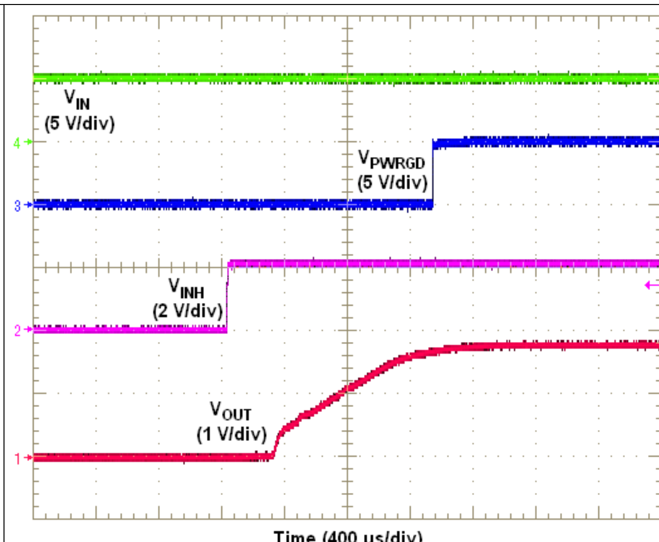


Figure 24. Inhibit Turn-On

8.10 Slow Start (SS/TR)

Connecting the STSEL pin to AGND and leaving SS/TR pin open enables the internal SS capacitor with a slow start interval of approximately 1.1 ms. Adding additional capacitance between the SS pin and AGND increases the slow start time. Table 8 shows an additional SS capacitor connected to the SS/TR pin and the STSEL pin connected to AGND. See Table 8 below for SS capacitor values and timing interval.

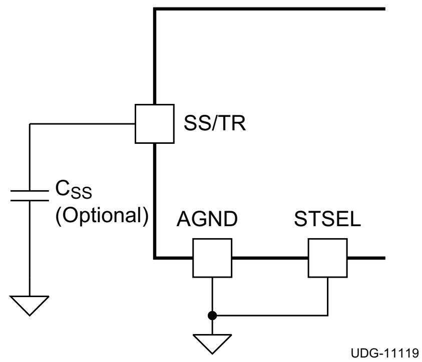


Figure 25. Slow-Start Capacitor (C_{SS}) and STSEL Connection

Table 8. Slow-Start Capacitor Values and Slow-Start Time

C_{SS} (pF)	open	2200	4700	10000	15000	22000	25000
SS Time (msec)	1.1	1.9	2.8	4.6	6.4	8.8	9.8

8.11 Overcurrent Protection

For protection against load faults, the LMZ30606 uses current limiting. The device is protected from overcurrent conditions by cycle-by-cycle current limiting and frequency foldback. During an overcurrent condition the output current is limited and the output voltage is reduced, as shown in Figure 26. When the overcurrent condition is removed, the output voltage returns to the established voltage, as shown in Figure 27.

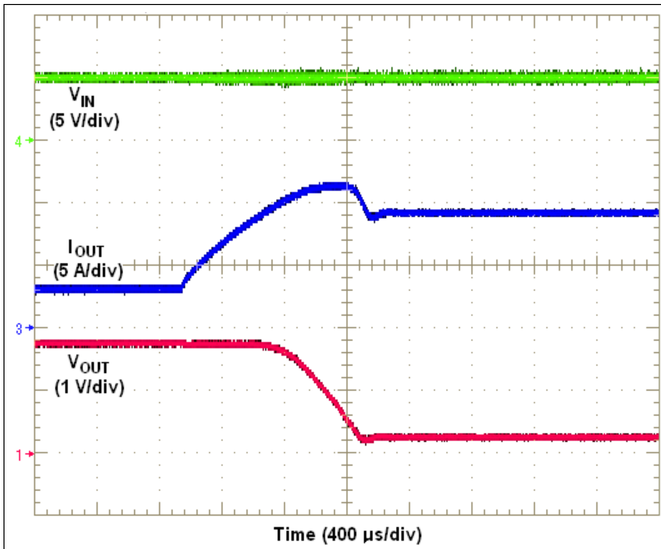


Figure 26. Overcurrent Limiting

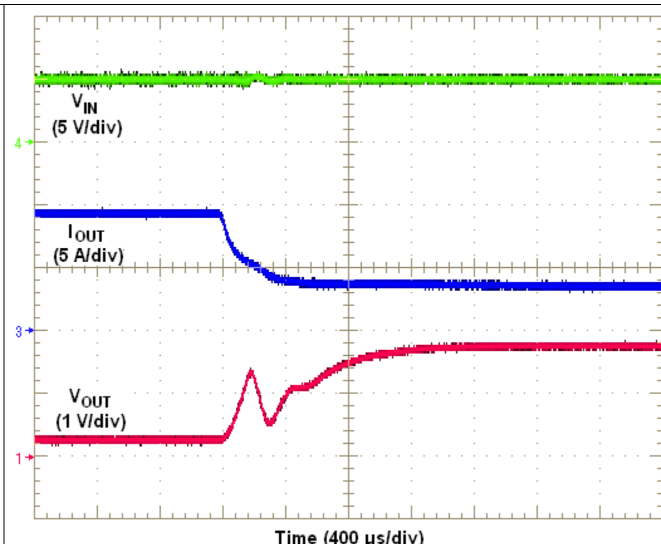


Figure 27. Removal of Overcurrent Condition

8.12 Synchronization (CLK)

An internal phase locked loop (PLL) has been implemented to allow synchronization between 500 kHz and 2 MHz, and to easily switch from RT mode to CLK mode. To implement the synchronization feature, connect a square wave clock signal to the RT/CLK pin with a minimum pulse width of 75 ns. The maximum clock pulse width must be calculated using Equation 2. The clock signal amplitude must transition lower than 0.4 V and higher than 2.2 V. The start of the switching cycle is synchronized to the falling edge of RT/CLK pin. Applications requiring both RT mode and CLK mode, configure the device as shown in Figure 28.

Before the external clock is present, the device works in RT mode and the switching frequency is set by the RT resistor (R_{RT}). When the external clock is present, the CLK mode overrides the RT mode. The device switches from RT mode to CLK mode and the RT/CLK pin becomes high impedance as the PLL starts to lock onto the frequency of the external clock. The device will lock to the external clock frequency approximately 15 µs after a valid clock signal is present. It is not recommended to switch from CLK mode back to RT mode because the internal switching frequency drops to a lower frequency before returning to the switching frequency set by the RT resistor.

$$CLK\_PW_{MAX} = \frac{0.75 \times \left(1 - \frac{V_{OUT}}{V_{IN(min)}}\right)}{f_{SW}} \quad (2)$$

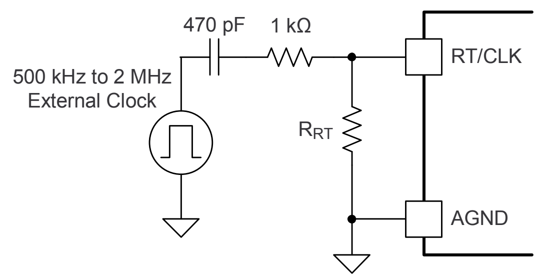


Figure 28. CLK/RT Configuration

Select the synchronization frequency based on the output voltages of the devices being synchronized. Table 9 shows the allowable V_{OUT} range for a given switching frequency when operating from a typical 5 V bus and a typical 3.3 V bus. For the most optimal solution, synchronize to a frequency in the center of the allowable frequency range. For example, an application requires synchronizing three LMZ30606 devices with output voltages of 1.2V, 1.8V, and 3.3V, all powered from VIN = 5V. Table 9 shows that all three output voltages can be synchronized to any frequency between 600 kHz to 1 MHz. For the most optimal solution, choose 800 kHz as the sychronization frequency. (Values included in the table are based on a resistive load.)

Table 9. Synchronization Frequency vs Output Voltage

SYNCHRONIZATION FREQUENCY (kHz)	R_{RT} (kΩ)	VIN = 5V (+/- 10%) V_{OUT} RANGE (V)		VIN = 3.3V (+/- 5%) V_{OUT} RANGE (V)	
		MIN	MAX	MIN	MAX
500	open	0.8	1.8	0.8	2.5
550	3400	0.8	2.2	0.8	2.5
600	1800	0.8	3.3	0.8	2.5
650	1200	0.8	3.6	0.8	2.5
700	887	0.8	3.6	0.8	2.5
750	715	0.9	3.6	0.8	2.5
800	590	0.9	3.6	0.8	2.5
850	511	1.0	3.6	0.8	2.5
900	442	1.0	3.6	0.8	2.5
950	392	1.1	3.6	0.8	2.5
1000	348	1.1	3.6	0.8	2.5
1250	232	1.4	3.6	0.9	2.4
1500	174	1.7	3.5	1.1	2.3
1750	137	2.0	3.4	1.3	2.3

Table 9. Synchronization Frequency vs Output Voltage (continued)

SYNCHRONIZATION FREQUENCY (kHz)	R_{RT} (kΩ)	VIN = 5V (+/- 10%)		VIN = 3.3V (+/- 5%)	
		V_{OUT} RANGE (V)		V_{OUT} RANGE (V)	
		MIN	MAX	MIN	MAX
2000	113	2.2	3.3	1.4	2.2

8.13 Sequencing (SS/TR)

Many of the common power supply sequencing methods can be implemented using the SS/TR, INH and PWRGD pins. The sequential method is illustrated in Figure 29 using two LMZ30606 devices. The PWRGD pin of the first device is coupled to the INH pin of the second device which enables the second power supply once the primary supply reaches regulation. Figure 30 shows sequential turn-on waveforms of two LMZ30606 devices.

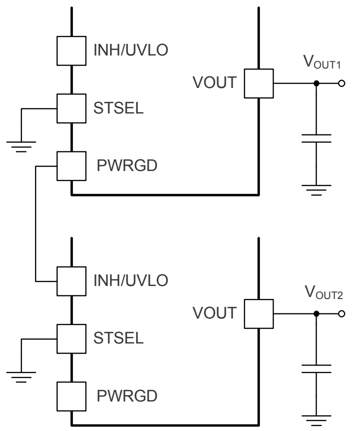


Figure 29. Sequencing Schematic

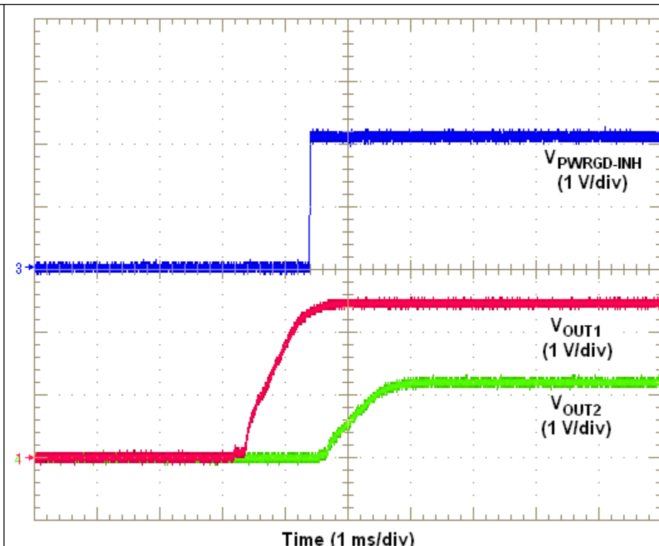


Figure 30. Sequencing Waveforms

Simultaneous power supply sequencing can be implemented by connecting the resistor network of R1 and R2 shown in Figure 31 to the output of the power supply that needs to be tracked or to another voltage reference source. Figure 32 shows simultaneous turn-on waveforms of two LMZ30606 devices. Use Equation 3 and Equation 4 to calculate the values of R1 and R2.

$$R1 = \frac{(V_{OUT2} \times 12.6)}{0.799} \ (k\Omega) \quad (3)$$

$$R2 = \frac{0.799 \times R1}{(V_{OUT2} - 0.799)} \ (k\Omega) \quad (4)$$

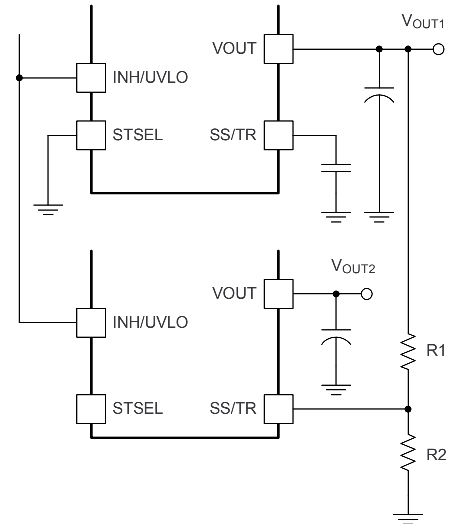


Figure 31. Simultaneous Tracking Schematic

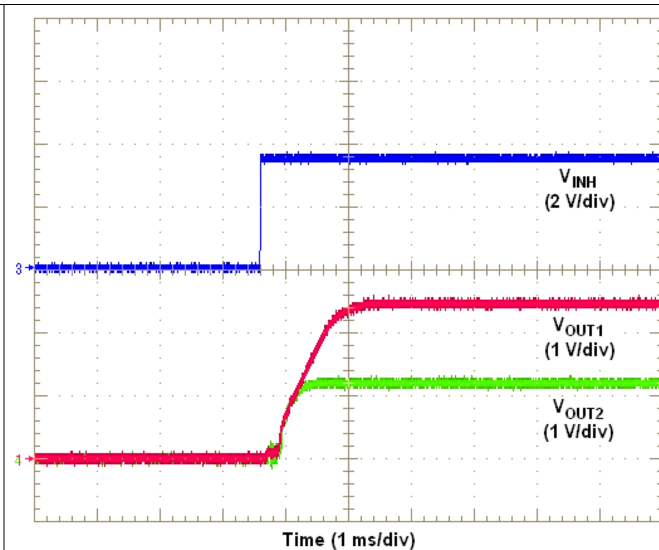


Figure 32. Simultaneous Tracking Waveforms

8.14 Programmable Undervoltage Lockout (UVLO)

The LMZ30606 implements internal UVLO circuitry on the VIN pin. The device is disabled when the VIN pin voltage falls below the internal VIN UVLO threshold. The internal VIN UVLO rising threshold is 3.135 V(max) with a typical hysteresis of 300 mV.

If an application requires a higher UVLO threshold on the VIN pin, the UVLO pin can be configured as shown in Figure 33. Table 10 lists standard values for R_{UVLO} to adjust the VIN UVLO voltage up.

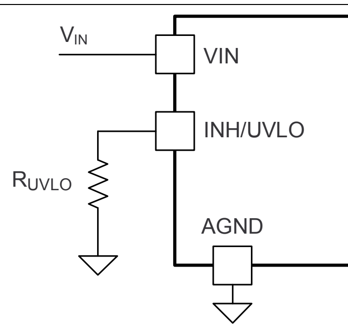


Figure 33. Adjustable VIN UVLO

Table 10. Standard Resistor values for Adjusting VIN UVLO

VIN UVLO (V) (typ)	3.25	3.5	3.75	4.0	4.25	4.5	4.75
R_{UVLO} (kΩ)	294	133	86.6	63.4	49.9	42.2	35.7
Hysteresis (mV)	325	335	345	355	365	375	385

8.15 Thermal Shutdown

The internal thermal shutdown circuitry forces the device to stop switching if the junction temperature exceeds 170°C typically. The device reinitiates the power up sequence when the junction temperature drops below 150°C typically.

8.16 EMI

The LMZ30606 is compliant with EN55022 Class B radiated emissions. Figure 34 and Figure 35 show typical examples of radiated emissions plots for the LMZ30606 operating from 5V and 3.3V respectively. Both graphs include the plots of the antenna in the horizontal and vertical positions.

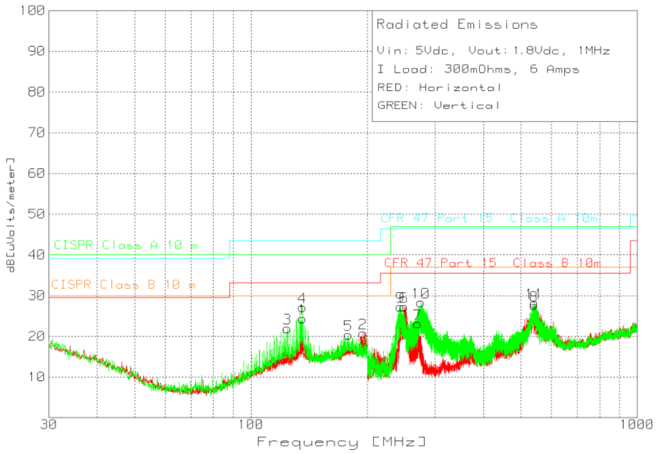


Figure 34. Radiated Emissions 5-V Input, 1.8-V Output, 6-A Load (EN55022 Class B)

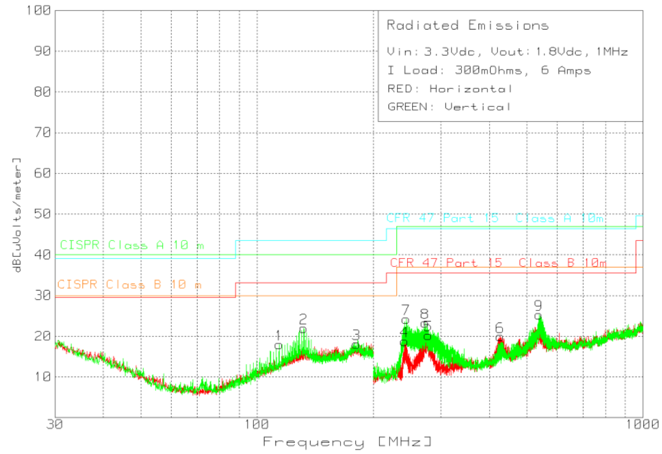


Figure 35. Radiated Emissions 3.3-V Input, 1.8-V Output, 6-A Load (EN55022 Class B)

8.17 Layout Considerations

To achieve optimal electrical and thermal performance, an optimized PCB layout is required. Figure 36, shows a typical PCB layout. Some considerations for an optimized layout are:

- Use large copper areas for power planes (VIN, VOUT, and PGND) to minimize conduction loss and thermal stress.
- Place ceramic input and output capacitors close to the module pins to minimize high frequency noise.
- Locate additional output capacitors between the ceramic capacitor and the load.
- Place a dedicated AGND copper area beneath the LMZ30606.
- Connect the AGND and PGND copper area at one point; directly at the pin 37 PowerPad using multiple vias.
- Place R_{SET}, R_{RT}, and C_{SS} as close as possible to their respective pins.
- Use multiple vias to connect the power planes to internal layers.

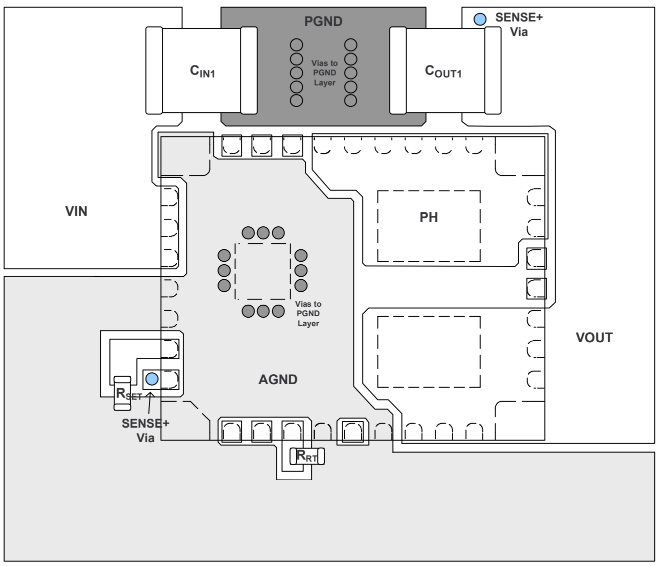


Figure 36. Typical Top-Layer Recommended Layout

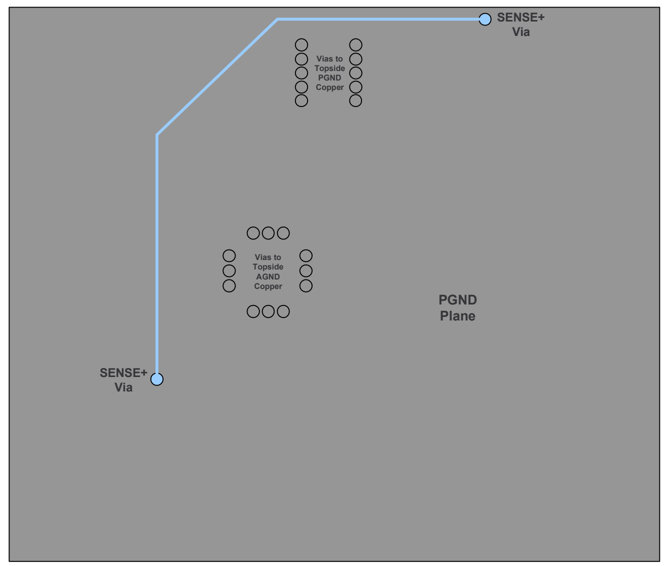


Figure 37. Typical PGND-Layer Recommended Layout

9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (June 2017) to Revision B	Page
• LMZ30606用のWEBENCH®設計リンクを追加	1
• Increased the peak reflow temperature and maximum number of reflows to JEDEC specifications for improved manufacturability	2
• 「デバイスおよびドキュメントのサポート」セクションを追加	26
• 「メカニカル、パッケージ、および注文情報」セクションを追加	27

Changes from Original (July 2013) to Revision A	Page
• Added peak reflow and maximum number of reflows information	2

10 デバイスおよびドキュメントのサポート

10.1 デバイス・サポート

10.1.1 開発サポート

10.1.1.1 WEBENCH®ツールによるカスタム設計

ここをクリックすると、WEBENCH® Power Designerにより、LMZ30606デバイスを使用するカスタム設計を作成できます。

1. 最初に、入力電圧(V_{IN})、出力電圧(V_{OUT})、出力電流(I_{OUT})の要件を入力します。
2. オプティマイザのダイヤルを使用して、効率、占有面積、コストなどの主要なパラメータについて設計を最適化します。
3. 生成された設計を、テキサス・インスツルメンツが提供する他のソリューションと比較します。

WEBENCH Power Designerでは、カスタマイズされた回路図と部品リストを、リアルタイムの価格と部品の在庫情報と併せて参照できます。

ほとんどの場合、次の操作を実行可能です。

- 電気的なシミュレーションを実行し、重要な波形と回路の性能を確認する。
- 熱シミュレーションを実行し、基板の熱特性を把握する。
- カスタマイズされた回路図やレイアウトを、一般的なCADフォーマットでエクスポートする。
- 設計のレポートをPDFで印刷し、同僚と設計を共有する。

WEBENCHツールの詳細は、www.ti.com/WEBENCHでご覧になれます。

10.2 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、ti.comのデバイス製品フォルダを開いてください。右上の隅にある「*通知を受け取る*」をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

10.3 コミュニティ・リソース

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™オンライン・コミュニティ ***TIのE2E（Engineer-to-Engineer）***コミュニティ。エンジニア間の共同作業を促進するために開設されたものです。e2e.ti.comでは、他のエンジニアに質問し、知識を共有し、アイディアを検討して、問題解決に役立てることができます。

設計サポート ***TIの設計サポート*** 役に立つE2Eフォーラムや、設計サポート・ツールをすばやく見つけることができます。技術サポート用の連絡先情報も参照できます。

10.4 商標

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10.5 静電気放電に関する注意事項

すべての集積回路は、適切なESD保護方法を用いて、取扱いと保存を行うようにして下さい。

静電気放電はわずかな性能の低下から完全なデバイスの故障に至るまで、様々な損傷を与えます。高精度の集積回路は、損傷に対して敏感であり、極めてわずかなパラメータの変化により、デバイスに規定された仕様に適合しなくなる場合があります。

10.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

11 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。この情報は、そのデバイスについて利用可能な最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LMZ30606RKGR	Active	Production	B1QFN (RKG) | 39	500 | LARGE T&R	Exempt	NIPDAU	Level-3-250C-168 HR	-40 to 85	(54618, LMZ30606)
LMZ30606RKGT	Active	Production	B1QFN (RKG) | 39	250 | SMALL T&R	Exempt	NIPDAU	Level-3-250C-168 HR	-40 to 85	(54618, LMZ30606)
LMZ30606RKGTG4	Active	Production	B1QFN (RKG) | 39	250 | SMALL T&R	Yes	NIPDAU	Level-3-250C-168 HR	-40 to 125	LMZ30606
LMZ30606RKGTG4.B	Active	Production	B1QFN (RKG) | 39	250 | SMALL T&R	Yes	NIPDAU	Level-3-250C-168 HR	-40 to 125	LMZ30606

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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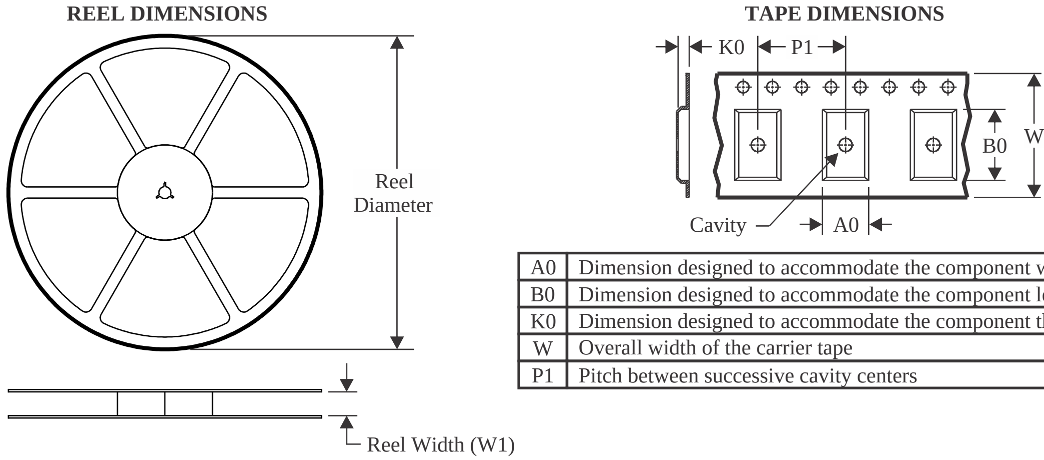
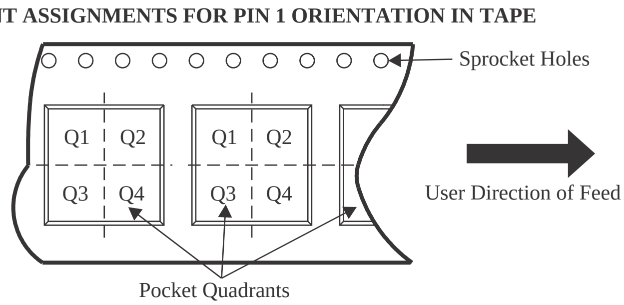
TAPE AND REEL INFORMATION

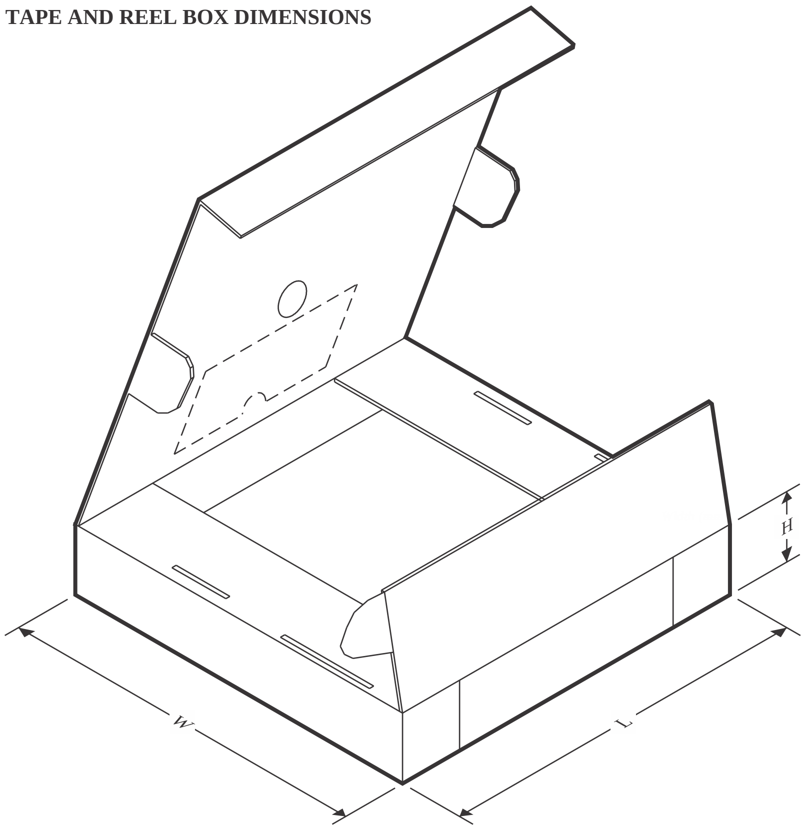


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers



*All dimensions are nominal

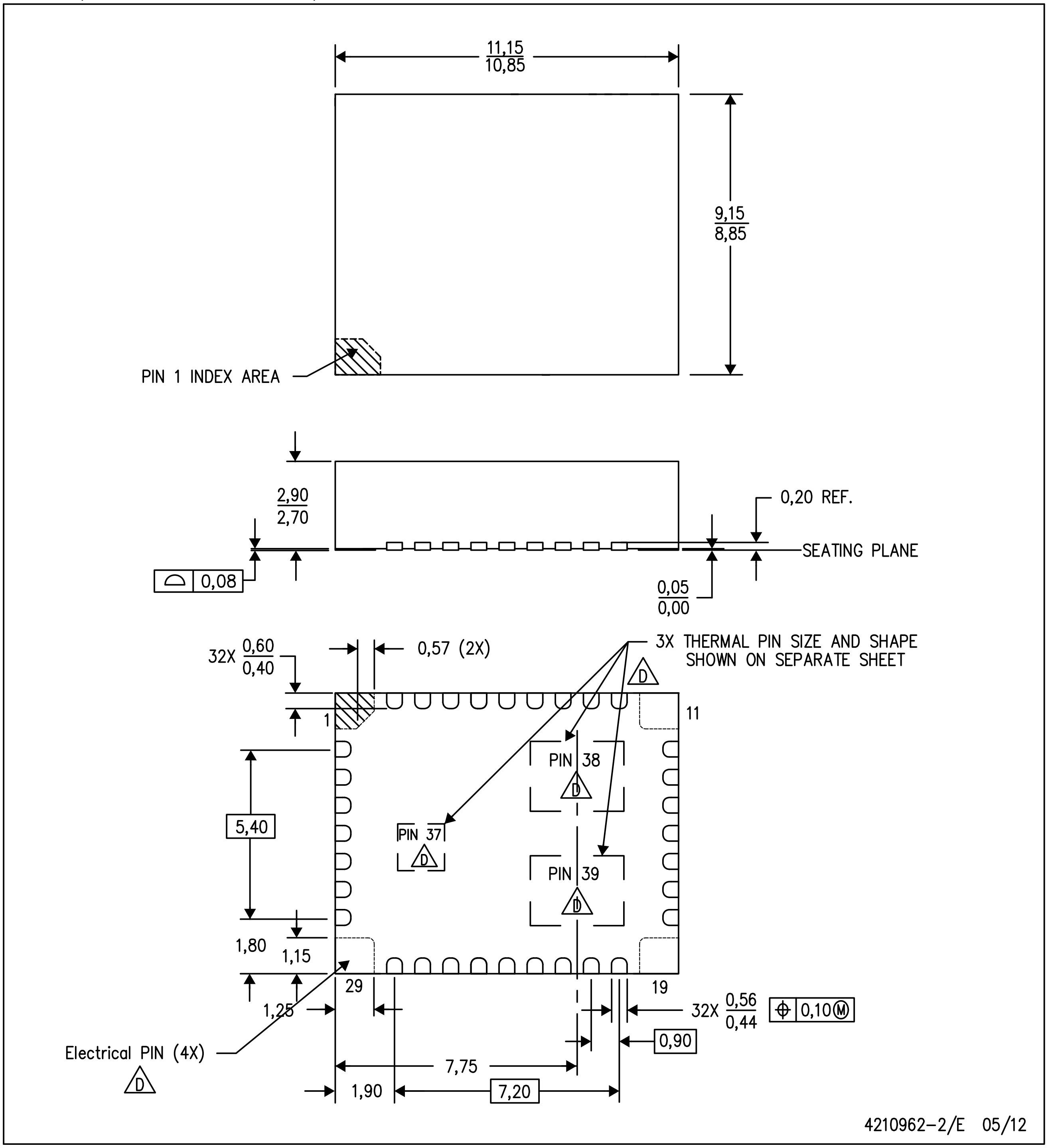
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMZ30606RKGR	B1QFN	RKG	39	500	330.0	24.4	9.35	11.35	3.1	16.0	24.0	Q1
LMZ30606RKGT	B1QFN	RKG	39	250	330.0	24.4	9.35	11.35	3.1	16.0	24.0	Q1
LMZ30606RKGTG4	B1QFN	RKG	39	250	330.0	24.4	9.35	11.35	3.1	16.0	24.0	Q1



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMZ30606RKGR	B1QFN	RKG	39	500	383.0	353.0	58.0
LMZ30606RKGT	B1QFN	RKG	39	250	383.0	353.0	58.0
LMZ30606RKGTG4	B1QFN	RKG	39	250	383.0	353.0	58.0

RKG (R–PB1QFN–N39) PLASTIC QUAD FLATPACK NO–LEAD



4210962–2/E 05/12

NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
- B. This drawing is subject to change without notice.
- C. Quad Flatpack, No–leads (QFN) package configuration.
- D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
- E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
- F. The package thermal performance may be enhanced by bonding the thermal pad to an external thermal plane.

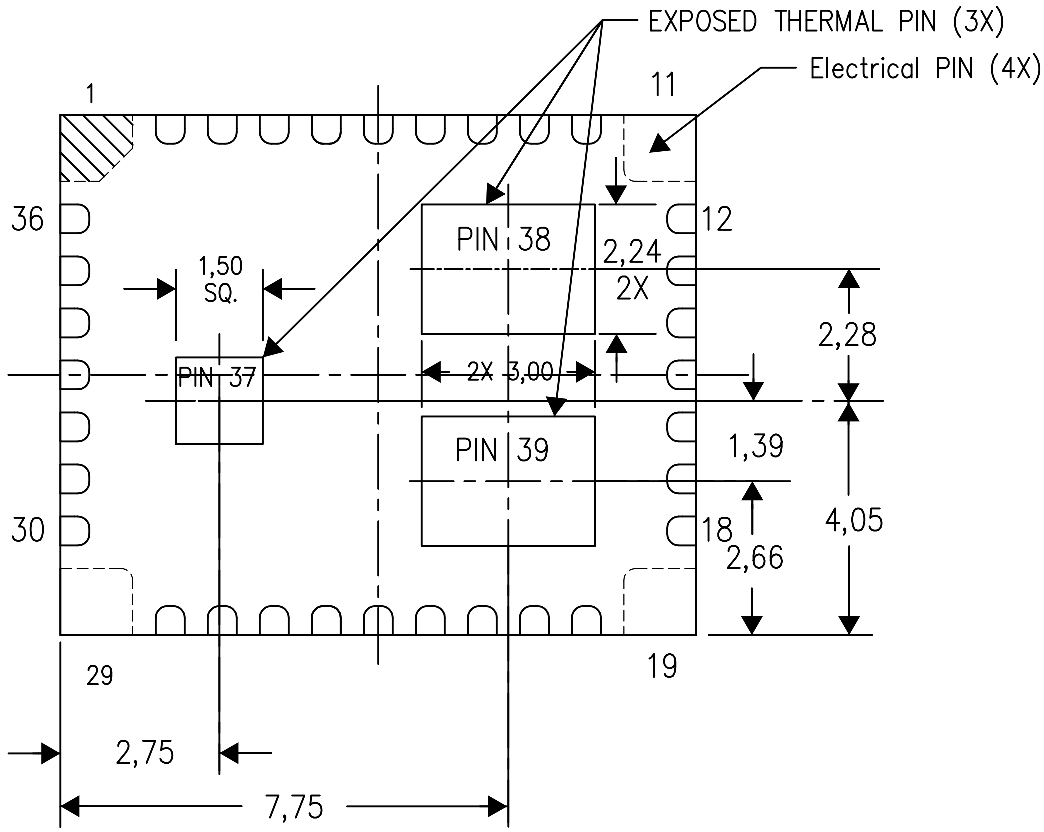
RKG (R–PQFN–N39) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

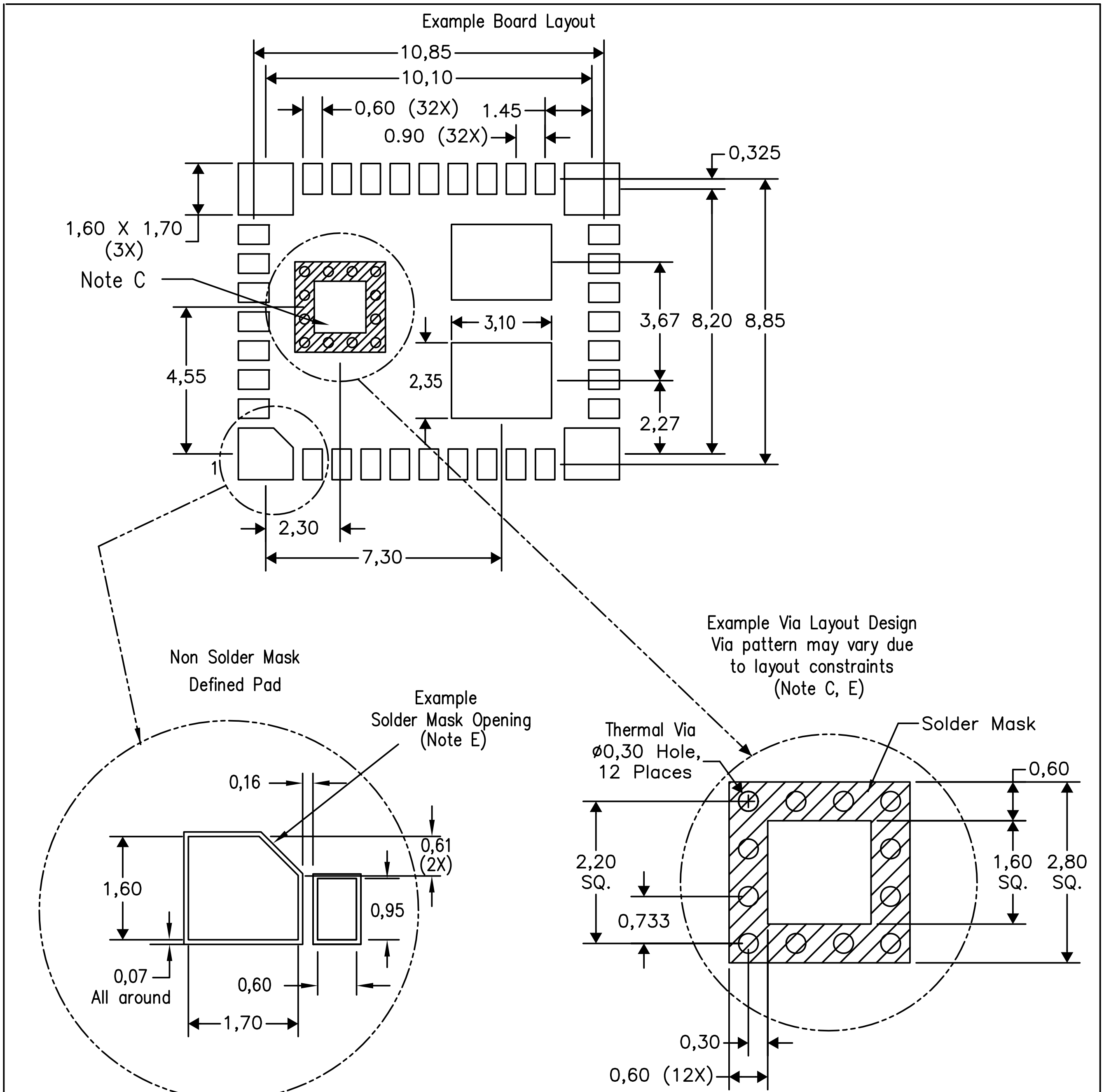
Exposed Thermal Pad Dimensions

Thermal Pad Tolerance: ±0.10mm

4211170–2/D 01/15

NOTE: A. All linear dimensions are in millimeters

RKG (S-PB1QFN-N39) PLASTIC QUAD FLATPACK NO-LEAD



4211194-2/D 08/15

NOTES: A. All linear dimensions are in millimeters.

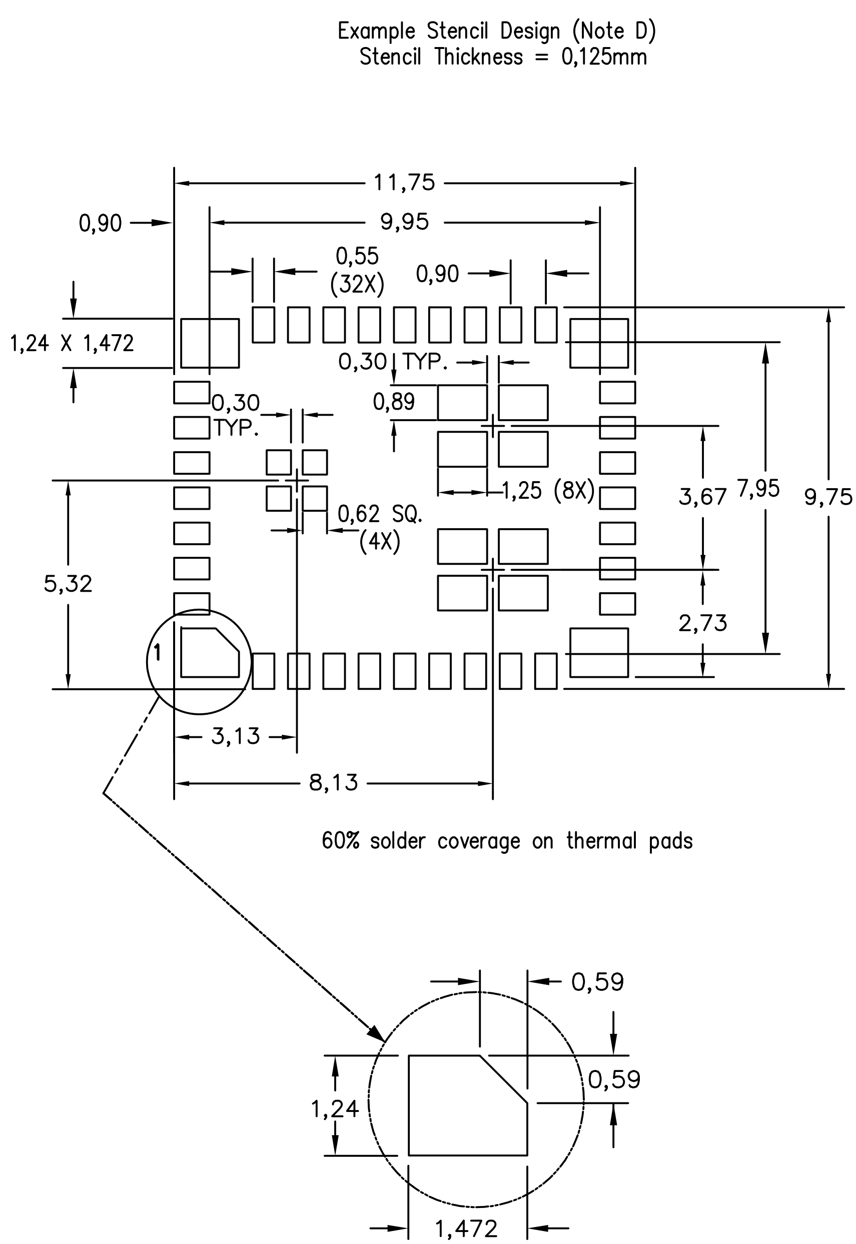
B. This drawing is subject to change without notice.

C. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat-Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http: //www.ti.com>.

D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.

E. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

RKG (S-PB1QFN-N39) PLASTIC QUAD FLATPACK NO-LEAD



4211194-3/D 08/15

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat-Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http: //www.ti.com>.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
E. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

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