LMZ34202 4.5V～42V入力、2A電源モジュール

1 特長

- 小さな占有面積で低プロファイルの設計を可能にする完全な統合電源ソリューション
- 10mm×10mm×4.3mmのパッケージ
- 広い出力電圧調整範囲(2.5V～7.5V)
- 可変スイッチング周波数(200kHz～1MHz)
- 外部クロックに同期
- 自動PFMモードによる軽負荷時の高効率
- ソフトスタート時間を設定可能
- 出力電圧シーケンシング/トラッキング
- パワー・グッド出力
- 低電圧誤動作防止(UVLO)をプログラム可能
- 過熱時のサーマル・シャットダウン保護機能
- 過電流保護機能(ヒカップ・モード)
- プリバイアス出力によるスタートアップ
- 動作温度範囲: -40℃～105℃
- 強化された熱特性: 14℃/W
- EN55022 Class Bの放射要件に準拠
  - シールド付きインダクタを内蔵
- WEBENCH® Power Designerにより、LMZ34202を使用するカスタム設計を作成

2 アプリケーション

- 産業用およびモータ制御
- 自動テスト機器
- 医療用およびイメージング機器
- 高密度の電源システム

3 概要

LMZ34202電源モジュールは使いやすい統合電源で、2AのDC-DCコンバータと、シールド付きインダクタおよびパッシブ部品が、薄型のQFNパッケージに内蔵されています。この総合的な電源ソリューションは、わずか3個の外付け部品で動作し、特定の設計要件に応じて主要なパラメータを変更する機能もあります。

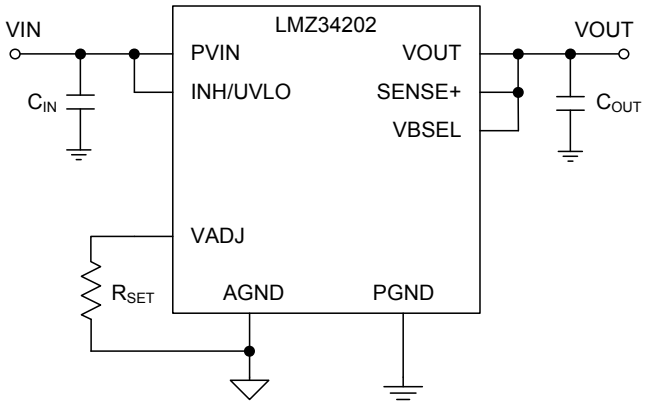
QFNパッケージはプリント基板へ簡単にハンダ付けでき、245℃までのリフロー・プロファイルが可能で、消費電力特性が非常に優れています。LMZ34202は柔軟で、多くの機能を持ち、広範なデバイスとシステムの電源として理想的です。

製品情報(1)

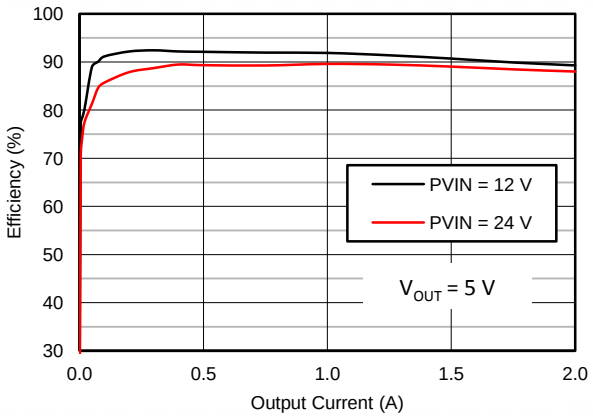
デバイス番号	パッケージ	本体サイズ
LMZ34202	QFN (43)	10.00mm×10.00mm

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。

アプリケーション概略図



効率と出力電流との関係



英語版のTI製品についての情報を翻訳したこの資料は、製品の概要を確認する目的で便宜的に提供しているものです。該当する正式な英語版の最新情報は、www.ti.comで閲覧でき、その内容が常に優先されます。TIでは翻訳の正確性および妥当性につきましては一切保証いたしません。実際の設計などの前には、必ず最新版の英語版をご参照くださいますようお願いいたします。

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4 改訂履歴

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Revision B (April 2018) から **Revision C** に変更 **Page**

- 「*絶対最大定格*」表に合わせてリフローの許容値を「260℃まで」から「245℃まで」に 変更 ... 1
- TIリファレンス・デザインの上端のナビゲータ 追加 ... 1

Revision A (June 2017) から **Revision B** に変更 **Page**

- LMZ34202のWEBENCH®設計リンク 追加 ... 1
- Increased the peak reflow temperature and maximum number of reflows to JEDEC specifications for improved manufacturability ... 5

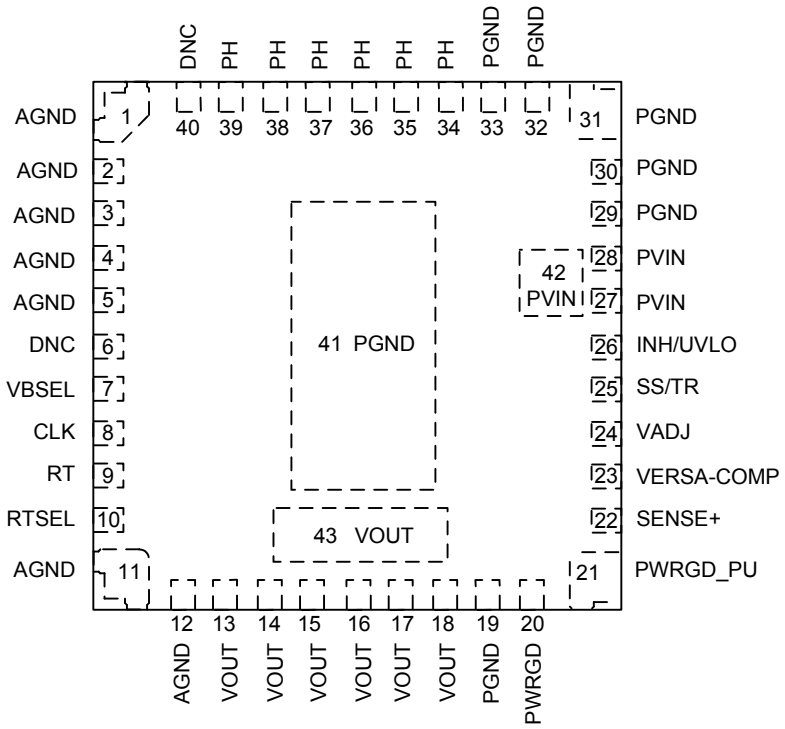
2016年3月発行のものから更新 **Page**

- Added peak reflow and maximum number of reflows information ... 5

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5 Pin Configuration and Functions

RVQ Package
43-Pin QFN
(Top View)



Pin Functions

PIN		TYPE (1)	DESCRIPTION
NAME	NO.		
AGND	1, 2, 3, 4, 5, 11, 12	G	Zero volt reference for the analog control circuitry. All of these pins are not connected together internal to the device and must be connected to one another externally using an analog ground plane on the PCB. Pins 11 and 12 are internally connected to the PGND of the device at a single point. The analog ground plane of the PCB should allow only analog ground currents to flow through these pins.
CLK	8	I	Synchronization input to synchronize the device to an external clock. Connect this pin to AGND if not used.
DNC	6, 40	-	Do Not Connect. Do not connect these pins to AGND, to another DNC pin, or to any other voltage. These pins are connected to internal circuitry. Each pin must be soldered to an isolated pad.
INH/UVLO	26	I	Inhibit and UVLO adjust pin. Use an open drain or open collector device to control the inhibit function. A resistor divider between this pin, AGND, and PVIN adjusts the UVLO voltage. Connect this pin to PVIN if not used.
PGND	19, 29, 30, 31, 32, 33, 41	G	This is the return current path for the power stage of the device. Connect these pins to the input source, the load, and to the bypass capacitors associated with PVIN and VOUT using power ground planes on the PCB. Pad 41 should be connected to the ground planes using multiple vias for good thermal performance.
PH	34, 35, 36, 37, 38, 39	O	Phase switch node. Do not place any external components on these pins or tie them to a pin of another function.
PVIN	27, 28, 42	I	Power input voltage. These pins supply all of the power to the device. Connect these pins to the input source and connect external bypass capacitors between these pins and PGND close to the device.
PWRGD	20	O	Power Good flag pin. This open drain output asserts low if the output voltage is more than approximately ±10% out of regulation. This pin is internally connected to an uncommitted 100k pull-up resistor that can be pulled up to a user-defined voltage applied to the PWRGD_PU pin.

(1) G = Ground, I = Input, O = Output

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Pin Functions (continued)

PIN		TYPE (1)	DESCRIPTION
NAME	NO.		
PWRGD_PU	21	I	An internal 100 k pull-up resistor is connected between this pin and the PWRGD pin. If use of this internal pull-up resistor is desired, connect this pin to an appropriate voltage source that is less than or equal to 12 V. If unused, leave this pin floating.
RT	9	I	This pin is connected to internal frequency setting circuitry which sets the default switching frequency to 500 kHz. An external resistor can be connected from this pin to AGND to adjust the switching frequency. Refer to application section in datasheet.
RTSEL	10	I	This pin can be used to adjust the switching frequency to 1 MHz without the need for an external resistor. Connect this pin to AGND to adjust the frequency to 1 MHz. Otherwise, leave this pin floating.
SENSE+	22	I	Remote sense connection. This pin must be connected to VOUT at the load or at the device pins. Connect the pin to VOUT at the load for improved regulation.
SS/TR	25	I	soft-start and tracking pin. Connecting an external capacitor to this pin adjusts the output voltage soft-start ramp above its 4.1 ms default setting. A voltage applied to this pin allows for tracking and sequencing control.
VADJ	24	I	Connecting a resistor between this pin and AGND adjusts the output voltage.
VBSEL	7	I	Selectable internal bias supply. For output voltages ≥ 4.5 V, connect this pin to VOUT. For output voltages < 4.5 V, connect this pin to AGND.
VERSA-COMP	23	I	Connects to internal compensation network. This pin can be left floating or connected to the VADJ pin to select the proper compensation depending on the output voltage.
VOUT	13, 14, 15, 16, 17, 18, 43	O	Output voltage. These pins are connected to the internal output inductor. Connect these pins to the output load and connect external bypass capacitors between these pins and PGND close to the device.

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Input voltage	PVIN, INH/UVLO	–0.3	50	V
	VOUT, SENSE+, VBSEL	–0.3	30(2)	V
	VADJ, VERSA-COMP, RT, RTSEL, SS/TR	–0.3	3.6	V
	PWRGD, PWRGD_PU	–0.3	15	V
	CLK	–0.3	5.5	V
Output voltage	PH	–0.3	50	V
Operating junction temperature(3)		–40	125	°C
Storage temperature, T_{stg}		–65	150	°C
Peak Reflow Case Temperature(4)			245(5)	°C
Maximum Number of Reflows Allowed(4)			3(5)	
Mechanical shock	Mil-STD-883D, Method 2002.3, 1 msec, 1/2 sine, mounted		1500	G
Mechanical vibration	Mil-STD-883D, Method 2007.2, 20-2000Hz		20	G

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The maximum voltage that can be applied to these pins is 30 V or PVIN, whichever is less.
(3) See temperature derating curves in the Typical Characteristics section for thermal information.
(4) For soldering specifications, refer to the Soldering Requirements for BQFN Packages application note.
(5) Devices with a date code prior to week 14 2018 (1814) have a peak reflow case temperature of 240°C with a maximum of one reflow.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±1000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
P_{VIN}	Input voltage	4.5		42	V
V_{OUT}	Output voltage	2.5		7.5	V
f_{SW}	Switching frequency	300		1000	kHz
T_A	Operating ambient temperature	–40		105	°C

6.4 Thermal Information

THERMAL METRIC(1)		LMZ34202 RVQ (QFN) 43 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	14	°C/W
ψ_{JT}	Junction-to-top characterization parameter	2.6	°C/W
ψ_{JB}	Junction-to-board characterization parameter	9	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

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6.5 Electrical Characteristics

Over –40°C to +105°C free-air temperature, PV_{IN} = 24 V, V_{OUT} = 5 V, I_{OUT} = I_{OUT} max, f_{sw} = 500 kHz, $C_{IN}1$ = 1 × 10-µF, 100-V 1210 ceramic, $C_{IN}2$ = 1 × 100-µF 100-V electrolytic bulk, and C_{OUT} = 3 × 47-µF, 16-V 1210 ceramic (unless otherwise noted).

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
INPUT VOLTAGE (PV_{IN})							
PV_{IN}	Input voltage range	Over I_{OUT} range		4.5(1)		42	V
UVLO	PV_{IN} undervoltage lockout	PV_{IN} increasing			3.2	3.8	V
		PV_{IN} decreasing			2.8		V
OUTPUT VOLTAGE							
$V_{OUT\ (ADJ)}$	Output voltage adjust range	Over I_{OUT} range		2.5		7.5	V
V_{OUT}	Set-point voltage tolerance	T_A = 25°C, I_{OUT} = 200 mA			±0.7	±1.5(2)	%
	Temperature variation	-40°C ≤ T_A ≤ 105°C, I_{OUT} = 0 A			±0.9		%
	Line regulation	T_A = 25°C, Over PV_{IN} range, I_{OUT} = 300 mA			±0.1		%
	Load regulation	T_A = 25°C, I_{OUT} = 300 mA to I_{OUT} max			±0.3		%
	Total output voltage variation	Includes set-point, line, load, and temperature			±2		%
V_{OUT} ripple	Output voltage ripple	20-MHz Bandwidth			10		mV/pp
OUTPUT CURRENT							
I_{OUT}	Output current	T_A = 105°C, natural convection		0		1.5	A
I_{OUT}	Output current	T_A = 105°C, 200LFM		0		2	A
I_{OUT}	Output current	T_A = 95°C, natural convection		0		2	A
I_{LIM}	Overcurrent threshold				2.5		A
PERFORMANCE							
η	Efficiency	PV_{IN} = 12 V, I_{OUT} = 1 A	V_{OUT} = 7.5 V; f_{SW} = 400 kHz		95		%
			V_{OUT} = 5 V; f_{SW} = 200 kHz		93		%
			V_{OUT} = 5 V; f_{SW} = 500 kHz		92		%
			V_{OUT} = 3.3 V; f_{SW}= 200 kHz		90		%
			V_{OUT} = 2.5 V; f_{SW} = 200 kHz		87		%
		PV_{IN} = 24 V, I_{OUT} = 1 A	V_{OUT} = 7.5 V; f_{SW} = 400 kHz		92		%
			V_{OUT} = 5 V; f_{SW}= 250 kHz		90		%
			V_{OUT} = 5 V; f_{SW}= 500 kHz		88		%
			V_{OUT} = 3.3 V; f_{SW} = 250 kHz		86		%
			V_{OUT} = 2.5 V; f_{SW} = 250 kHz		81		%
	Transient response	I_{OUT} = 50% load step 1 A/µs slew rate	Recovery time		100		µs
			Over/Undershoot		2		%
SLOW START							
T_{SS}	Internal slow start time	SS/TR pin open			4.1		ms
INHIBIT							
V_{INH} (high)	Inhibit control	Precision inhibit level		2.00	2.1	2.42	V
V_{INH} (low)		Inhibit turn-off hysteresis			-0.294		V
I_I (shutdown)	Input shutdown supply current	INH/UVLO pin conected to AGND			2.4	6.2(3)	µA
POWER GOOD (PWRGD)							
V_{PWRGD}	PWRGD thresholds	V_{OUT} rising	Good		95		%
			Fault		110		%
		V_{OUT} falling	Fault		90		%
			Good		105		%

(1) The minimum PV_{IN} is 4.5 V or (V_{OUT} / 0.75), whichever is greater. For V_{OUT} = 3.3 V, the minimum PV_{IN} is 4.75 V when I_{OUT} > 1.5 A.
(2) The stated limit of the set-point voltage tolerance includes the tolerance of both the internal voltage reference and the internal adjustment resistor. The overall output voltage tolerance will be affected by the tolerance of the external R_{SET} resistor.
(3) Guaranteed by design. Not production tested.

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Electrical Characteristics (continued)

Over –40°C to +105°C free-air temperature, PV_{IN} = 24 V, V_{OUT} = 5 V, I_{OUT} = I_{OUT} max, f_{sw} = 500 kHz, $C_{IN}1$ = 1 × 10-µF, 100-V 1210 ceramic, $C_{IN}2$ = 1 × 100-µF 100-V electrolytic bulk, and C_{OUT} = 3 × 47-µF, 16-V 1210 ceramic (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
THERMAL SHUTDOWN						
$T_{SHUTDOWN}$	Thermal shutdown	Shutdown Temperature		160		°C
		Hysteresis		10		°C
INPUT/OUTPUT CAPACITANCE						
C_{IN}	External input capacitance	ceramic	10(4)			µF
		non-ceramic		100		µF
C_{OUT}	External output capacitance	Ceramic	64(5)		See(6)	µF
		Non-ceramic		100	See(6)	µF
		ceramic + non-ceramic			See(6)	µF
		Equivalent series resistance (ESR)			20	mΩ

(4) The specified minimum ceramic input capacitance represents the standard capacitance value. The actual effective capacitance after considering the effects of DC bias and temperature variation should be ≥ 4.7 µF.
(5) The amount of required output capacitance varies depending on the output voltage (see Output Capacitor Selection). The minimum required output capacitance must be comprised of ceramic capacitance. The amount of required ceramic capacitance represents the standard capacitance value. Locate the capacitance close to the device. Adding additional ceramic or non-ceramic capacitance close to the load improves the response of the regulator to load transients.
(6) The maximum allowable output capacitance varies depending on the output voltage (see Output Capacitor Selection).

6.6 Switching Characteristics

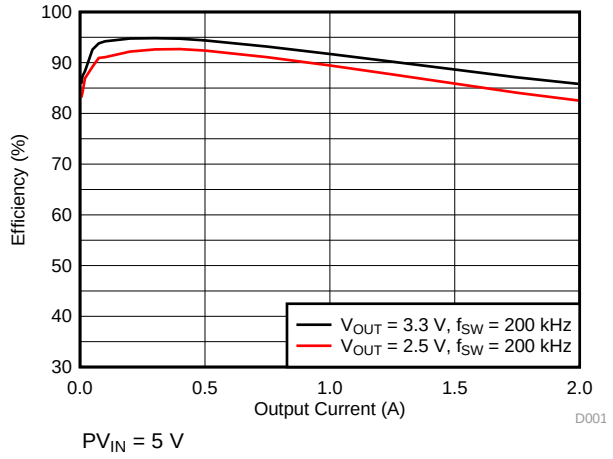
over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{SW}	Switching frequency	RT and RTSEL pins open	410	500	590	kHz
f_{CLK}	CLK Control	Synchronization frequency	200		1000	kHz
V_{CLK-H}		CLK high level	2		5.5	V
V_{CLK-L}		CLK low level			0.4	V
D_{CLK}		CLK duty cycle	10%	50%	90%	

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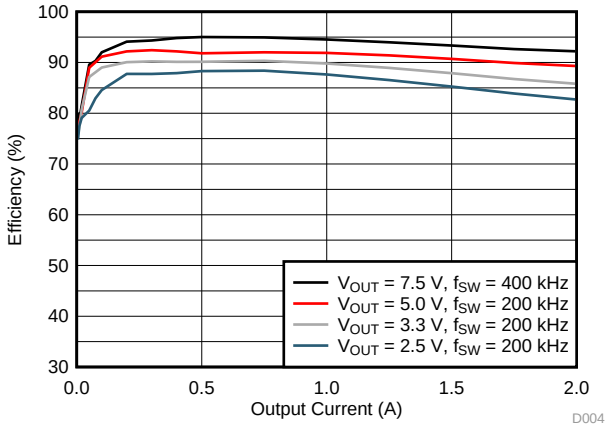
6.7 Typical Characteristics

T_A = 25°C, unless otherwise noted.



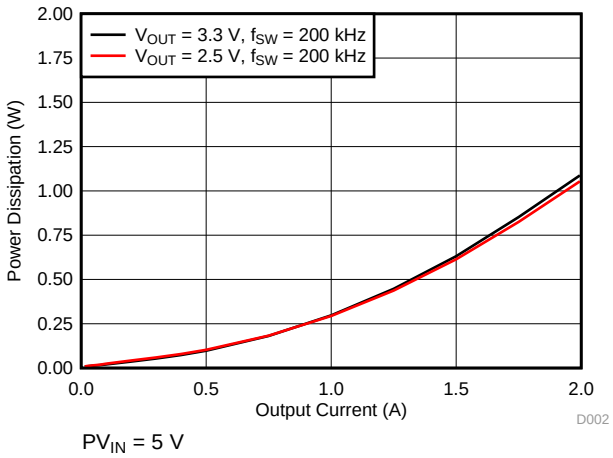
PV_{IN} = 5 V

図 1. Efficiency vs Output Current



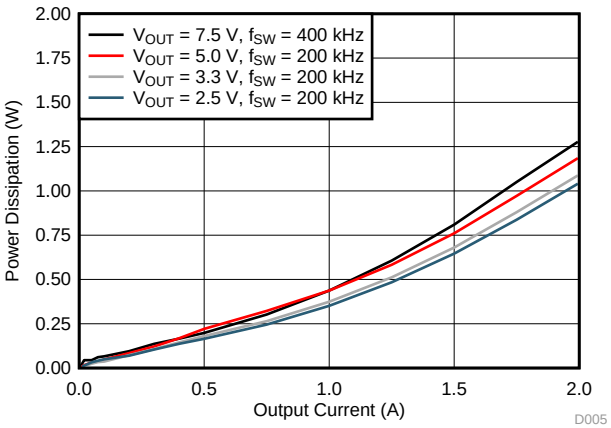
PV_{IN} = 12 V

図 2. Efficiency vs Output Current



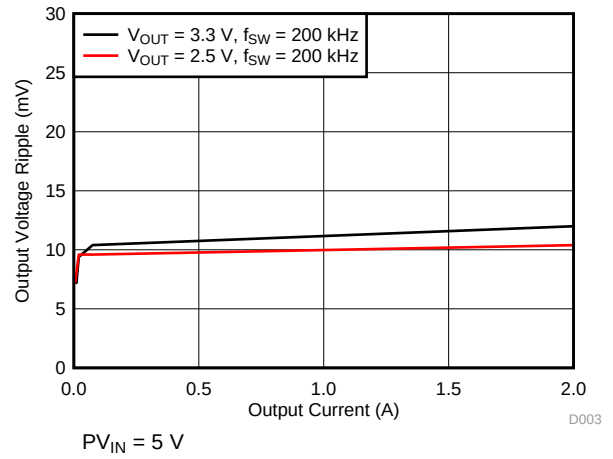
PV_{IN} = 5 V

図 3. Power Dissipation vs Output Current



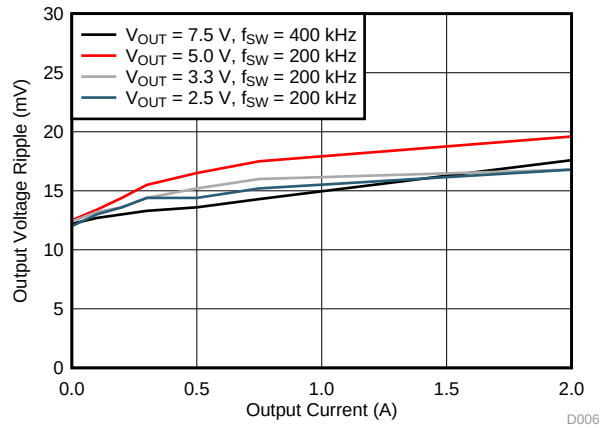
PV_{IN} = 12 V

図 4. Power Dissipation vs Output Current



PV_{IN} = 5 V

図 5. Voltage Ripple vs Output Current



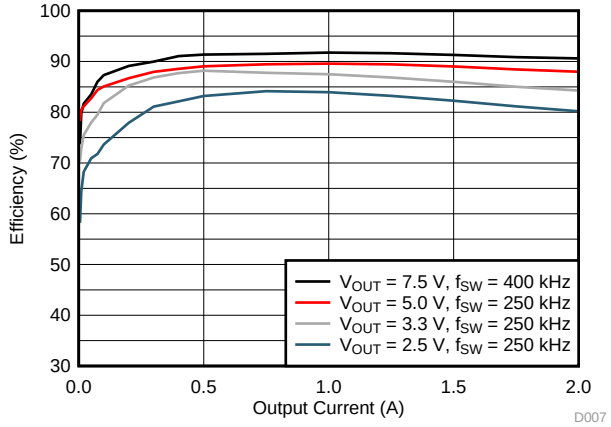
PV_{IN} = 12 V

図 6. Voltage Ripple vs Output Current

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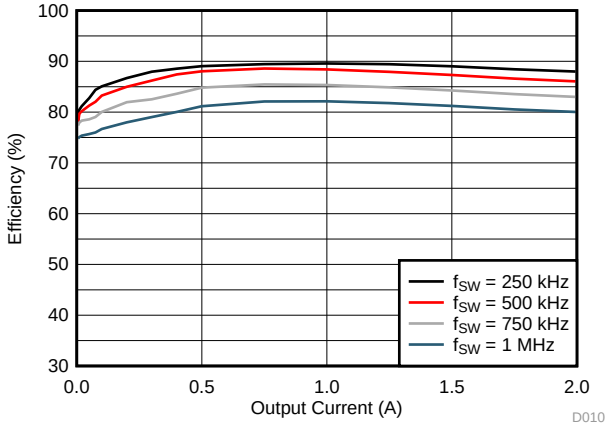
Typical Characteristics (continued)

T_A = 25°C, unless otherwise noted.



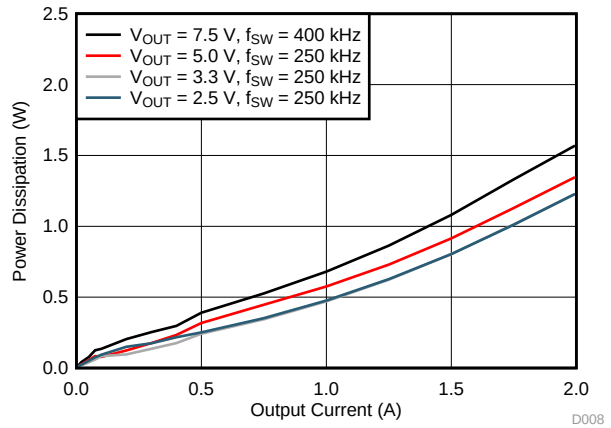
PV_{IN} = 24 V

図 7. Efficiency vs Output Current



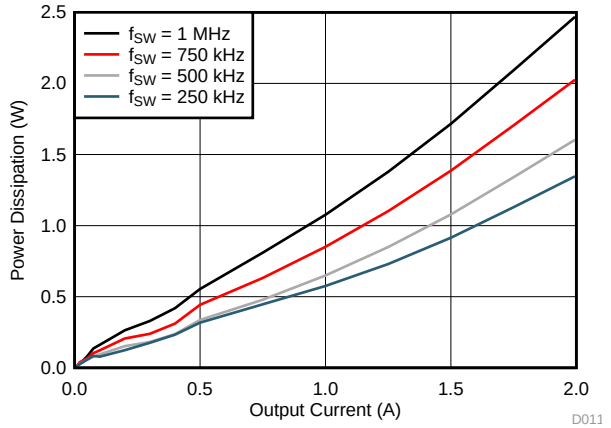
PV_{IN} = 24 V
V_{OUT} = 5 V over frequency range

図 8. Efficiency vs Output Current



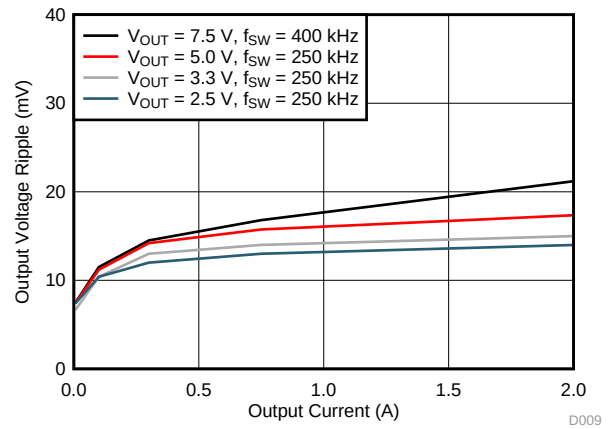
PV_{IN} = 24 V

図 9. Power Dissipation vs Output Current



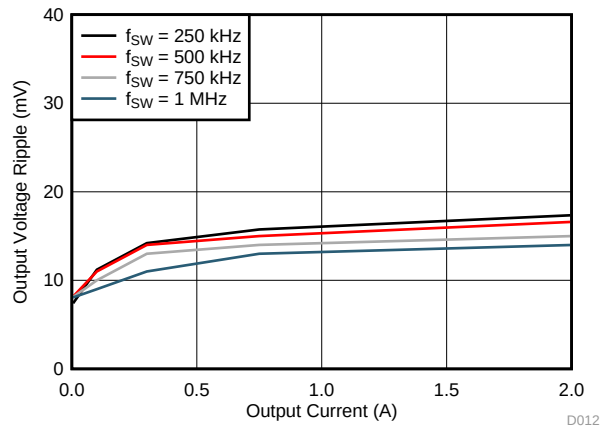
PV_{IN} = 24 V
V_{OUT} = 5 V over frequency range

図 10. Power Dissipation vs Output Current



PV_{IN} = 24 V

図 11. Voltage Ripple vs Output Current



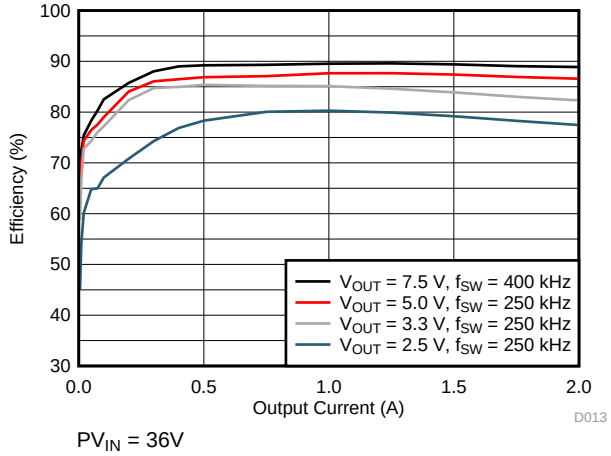
PV_{IN} = 24 V
V_{OUT} = 5 V over frequency range

図 12. Voltage Ripple vs Output Current

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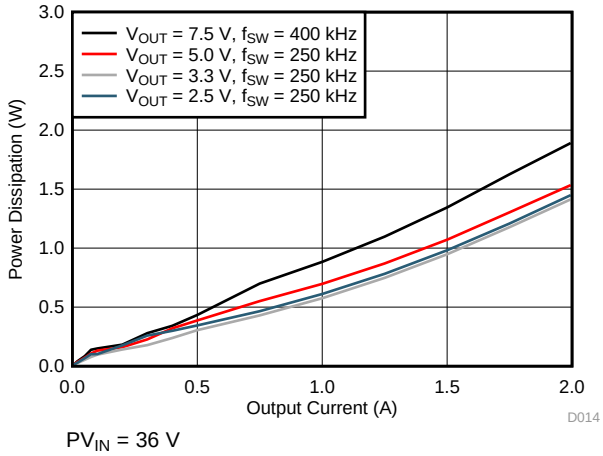
Typical Characteristics (continued)

T_A = 25°C, unless otherwise noted.



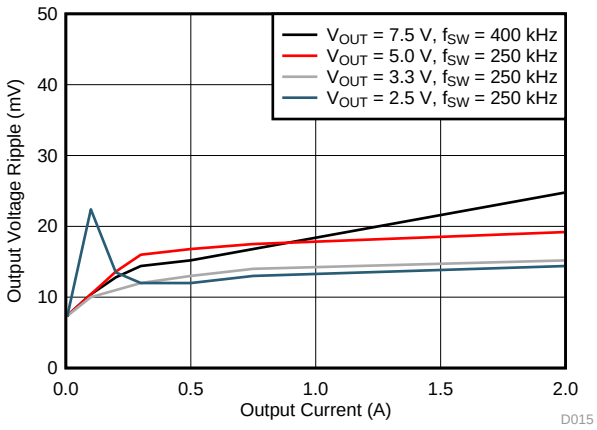
PV_{IN} = 36V

図 13. Efficiency vs Output Current



PV_{IN} = 36 V

図 14. Power Dissipation vs Output Current



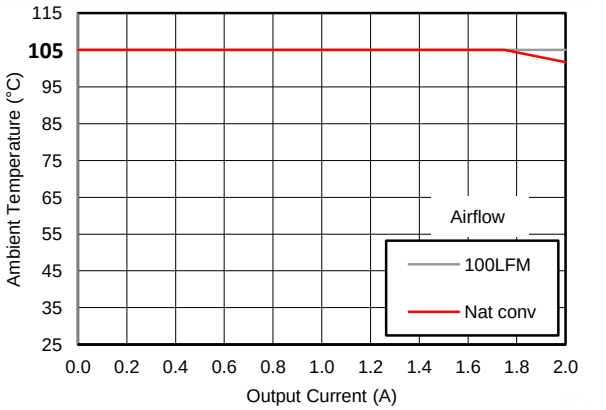
PV_{IN} = 36 V

図 15. Voltage Ripple vs Output Current

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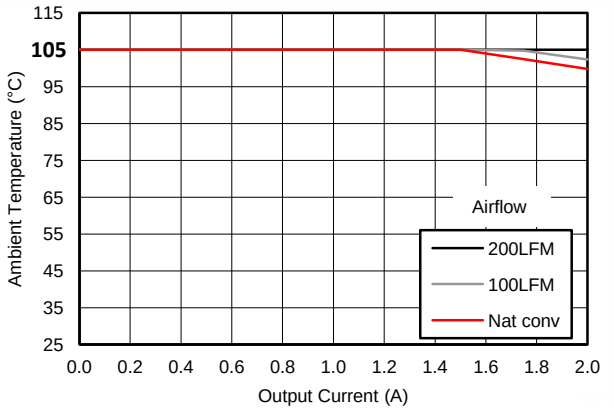
6.8 Typical Characteristics (Thermal Derating)

The temperature derating curves represent the conditions at which internal components are at or below the manufacturer's maximum operating temperatures. Derating limits apply to devices soldered directly to a 50 mm × 100 mm, 4-layer PCB with 2 oz. copper.



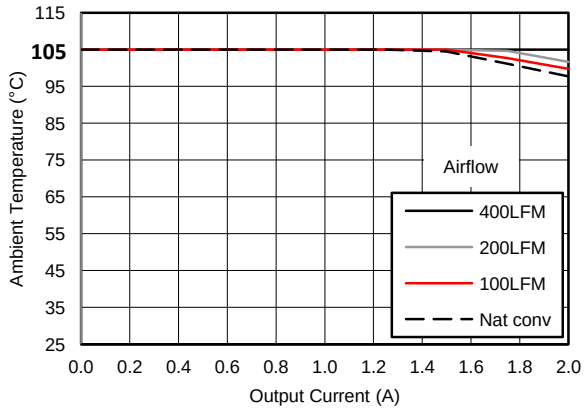
PV_{IN} = 24 V V_{OUT} = 3.3 V f_{SW} = 250 kHz

図 16. Safe Operating Area



PV_{IN} = 24 V V_{OUT} = 5 V f_{SW} = 250 kHz

図 17. Safe Operating Area



PV_{IN} = 24 V V_{OUT} = 7.5 V f_{SW} = 400 kHz

図 18. Safe Operating Area

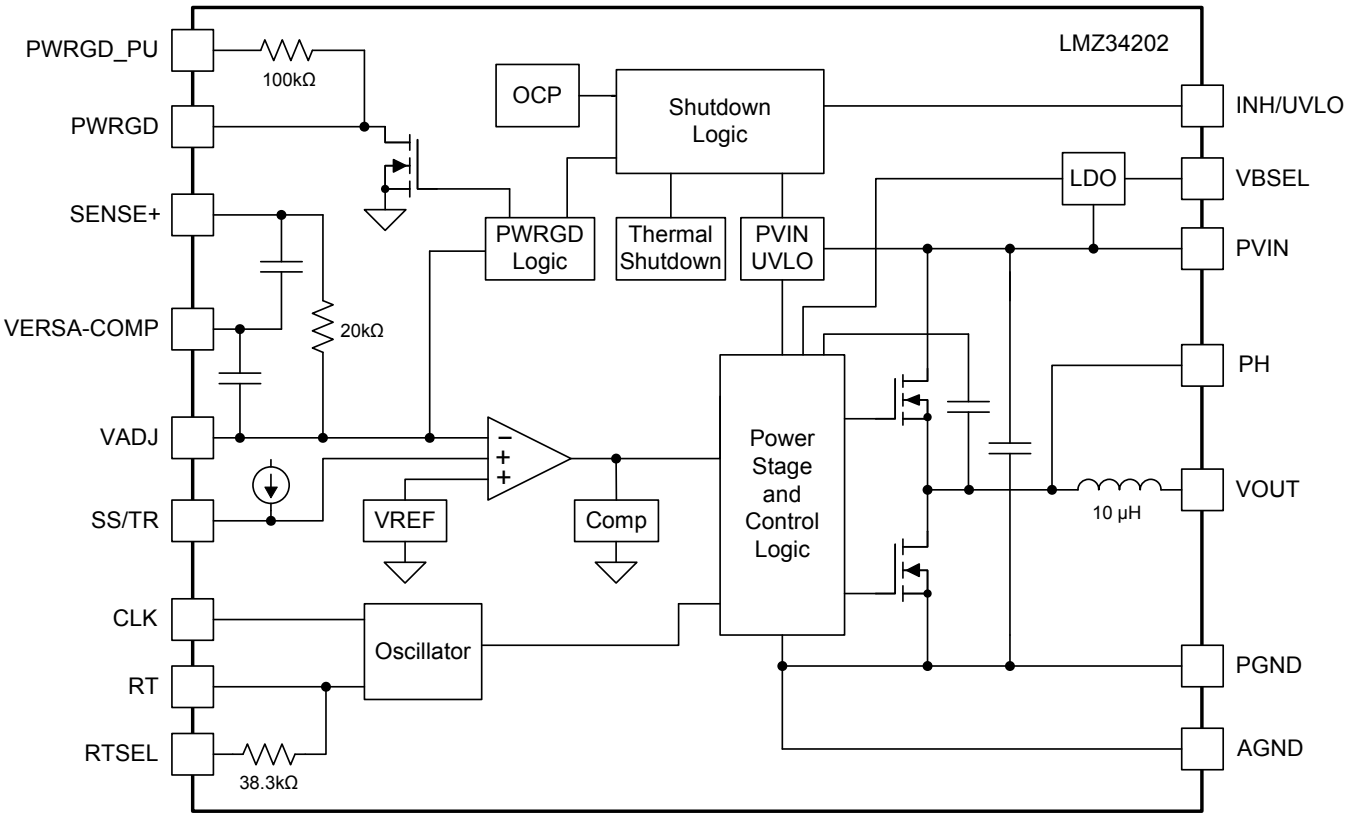
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7 Detailed Description

7.1 Overview

The LMZ34202 is a full featured 42-V input, 2-A, synchronous step down converter with PWM, MOSFETs, inductor, and control circuitry integrated into a low-profile, overmolded package. This device enables small designs by integrating all but the input and output capacitors, while still leaving the ability to adjust key parameters to meet specific design requirements. The LMZ34202 provides a 3× output voltage range of 2.5 V to 7.5 V. A single external resistor is used to adjust the output voltage to the desired output. The switching frequency is also adjustable by using an external resistor or a synchronization pulse to accommodate various input and output voltage conditions and to optimize efficiency. The device provides accurate voltage regulation for a variety of loads by using an internal voltage reference that is 2% accurate over temperature. Input under-voltage lockout is internally set at 3.2 V, but can be adjusted upward using a resistor divider on the INH/UVLO pin of the device. The INH/UVLO pin can also be pulled low to put the device in standby mode to reduce input quiescent current. The device provides a power good signal to indicate when the output is within ±5% of its nominal voltage. Thermal shutdown and current limit features protect the device during an overload condition. Automatic PFM mode improves light-load efficiency. A 43-pin, QFN, package that includes exposed bottom pads provides a thermally enhanced solution for space-constrained applications.

7.2 Functional Block Diagram



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7.3 Feature Description

7.3.1 Adjusting the Output Voltage

The VADJ pin sets the output voltage of the LMZ34202. The output voltage adjustment range is from 2.5 V to 7.5 V. The switching frequency range for any output voltage must be determined from 表 4 or 表 5. The adjustment method requires the addition of R_{SET}, which sets the output voltage, and the connection of SENSE+ to VOUT. The R_{SET} resistor must be connected directly between the VADJ (pin 24) and AGND. The SENSE+ pin (pin 22) must be connected to VOUT either at the load for improved regulation or at VOUT of the device. 表 1 lists the standard external R_{SET} resistor for a number of common bus voltages.

表 1. Standard R_{SET} Resistor Values for Common Output Voltages

	OUTPUT VOLTAGE V_{OUT} (V)				
	2.5	**3.3**	**5.0**	**6.0**	**7.5**
R_{SET} (kΩ)	13.7	8.87	5.11	4.02	3.09

For other output voltages, the value of the required resistor can either be calculated using the following formula, or simply selected from the range of values given in 表 2.

$$R_{SET} = \frac{20}{\left[\left(\frac{V_{OUT}}{1.011}\right) - 1\right]} \text{ (k}\Omega\text{)} \quad (1)$$

表 2. Standard R_{SET} Resistor Values

V_{OUT} (V)	R_{SET} (kΩ)		V_{OUT} (V)	R_{SET} (kΩ)
2.5	13.7		5.1	4.99
2.6	12.7		5.2	4.87
2.7	11.8		5.3	4.75
2.8	11.3		5.4	4.64
2.9	10.7		5.5	4.53
3.0	10.2		5.6	4.42
3.1	9.76		5.7	4.32
3.2	9.31		5.8	4.22
3.3	8.87		5.9	4.12
3.4	8.45		6.0	4.02
3.5	8.06		6.1	3.97
3.6	7.87		6.2	3.92
3.7	7.50		6.3	3.83
3.8	7.32		6.4	3.74
3.9	6.98		6.5	3.65
4.0	6.81		6.6	3.61
4.1	6.49		6.7	3.57
4.2	6.34		6.8	3.48
4.3	6.19		6.9	3.40
4.4	5.90		7.0	3.36
4.5	5.76		7.1	3.32
4.6	5.62		7.2	3.24
4.7	5.49		7.3	3.20
4.8	5.36		7.4	3.16
4.9	5.23		7.5	3.09
5.0	5.11			

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7.3.2 Switching Frequency (RT)

The switching frequency range of the LMZ34202 is 200 kHz to 1 MHz. Not all PV_{IN}, V_{OUT}, and I_{OUT} conditions can be set to all of the frequencies in this range. See Recommended Operating Range for the allowable operating ranges. The switching frequency can easily be set one of three ways. First, leaving the RT pin (pin 9) and RTSEL pin (pin 10) floating (OPEN) allows operation at the default switching frequency of 500 kHz. Also, connecting the RTSEL pin to AGND while floating the RT pin, sets the switching frequency to 1 MHz. The option is also available to set the switching frequency to any frequency in the range of 200 kHz to 1 MHz, by connecting a resistor (R_{RT}) between the RT pin and AGND, while floating the RTSEL pin. See 表 3 for standard resistor values for setting the switching frequency or use 式 2 to calculate R_{RT} for other switching frequencies.

表 3. Switching Frequency R_{RT} Values

Switching Frequency	R_{RT} (kΩ)
250 kHz	158
500 kHz	78.7 or (RT pin OPEN, RTSEL pin OPEN)
750 kHz	53.6
1 MHz	38.3 or (RT pin OPEN, RTSEL pin to AGND)

$$R_{RT} = \frac{40200}{Fsw(kHz)} - 0.6 \ \ (k\Omega) \tag{2}$$

7.3.3 Recommended Operating Range

表 4 and 表 5 below show the allowable switching frequencies for a given range of output voltages. Reference 表 4 for applications where the maximum output current is 1.75 A or less. Reference 表 5 for applications that the output current is greater than 1.75 A. Notice that applications requiring less than 1.75 A can operate over a much wider range of switching frequencies. For the most efficient solution, always operate at the lowest allowable frequency.

表 4. Switching Frequency vs Output Voltage
Output Current ≤ 1.75 A

V_{OUT} RANGE (V)	SWITCHING FREQUENCY RANGE (kHz)					
	PVIN = 12 V		PVIN = 24 V		PVIN = 36 V	
	MIN	MAX	MIN	MAX	MIN	MAX
2.5 - 3.5 V	200	1000	200	600	200	400
>3.5 - 4.5 V	200	1000	200	850	200	550
>4.5 - 5.5 V	200	1000	200	1000	200	750
>5.5 - 6.5 V	300	1000	200	1000	200	1000
>6.5 - 7.5 V	300	900	300	1000	300	950

表 5. Switching Frequency vs Output Voltage
Output Current > 1.75 A

V_{OUT} RANGE (V)	SWITCHING FREQUENCY RANGE (kHz)					
	PVIN = 12 V		PVIN = 24 V		PVIN = 36 V	
	MIN	MAX	MIN	MAX	MIN	MAX
2.5 - 3.5 V	200	450	200	500	200	400
>3.5 - 4.5 V	200	500	200	600	200	550
>4.5 - 5.5 V	200	500	200	650	200	700
>5.5 - 6.5 V	300	500	250	700	250	800
>6.5 - 7.5 V	300	400	300	750	300	800

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7.3.4 Synchronization (CLK)

The LMZ34202 switching frequency can also be synchronized to an external clock from 200 kHz to 1 MHz. Not all PV_{IN}, V_{OUT}, and I_{OUT} conditions can be set to all of the frequencies in this range. See *Recommended Operating Range* for the allowable operating ranges.

To implement the synchronization feature, connect a clock signal to the CLK pin with a duty cycle between 10% and 90%. The clock signal amplitude must transition lower than 0.4 V and higher than 2.0 V. The start of the switching cycle is synchronized to the rising edge of CLK pin. Before the external clock is present the device operates in RT mode and the switching frequency is set by R_{RT} resistor. Select R_{RT} to set the frequency close to the external synchronization frequency. When the external clock is present, the CLK mode overrides the RT mode. If the external clock is removed or fails at logic high or low, the LMZ34202 will switch at the frequency programmed by the R_{RT} resistor after a time-out period. Connect the CLK pin (pin 8) to AGND if not used.

7.3.5 Output Capacitor Selection

The minimum required and maximum output capacitance of the LMZ34202 is a function of the output voltage as shown in 表 6. Additionally, the output voltage will determine the Versa-Comp configuration (see VERSA-COMP Pin Configurations), which is also included in 表 6. The capacitance values listed in 表 6 are the specified capacitance values. The effects of DC bias and temperature variation must be considered when using ceramic capacitance. For ceramic capacitors, package size, voltage rating, and dielectric material will contribute to differences between the specified value and the actual effective value of the capacitance. $C_{OUT(min)}$ must be comprised of ceramic type capacitors. Additional capacitance, not exceeding $C_{OUT(max)}$, may be ceramic type or low-ESR polymer type. See 表 7 for a preferred list of output capacitors by vendor.

表 6. Required Output Capacitance

V_{OUT} (V)	MINIMUM REQUIRED C_{OUT} (µF) (1) (2)	MAXIMUM C_{OUT} (µF) (2)	Versa-Comp Connection
2.5	64	350	Leave OPEN
3.3	64	350	Connect to VADJ
5.0	64	350	Connect to VADJ
6.0	64	200	Connect to VADJ
7.5	100	200	Connect to VADJ

(1) Minimum required output capacitance must be comprised of ceramic capacitance.
(2) C_{OUT} values represent specified capacitance values.

表 7. Recommended Output Capacitors(1)

VENDOR	SERIES	PART NUMBER	CAPACITOR CHARACTERISTICS		
			WORKING VOLTAGE (V)	CAPACITANCE(2) (µF)	ESR(3) (mΩ)
TDK	X5R	C3225X5R1C106K	16	10	2
Murata	X5R	GRM32ER61C106K	16	10	2
TDK	X5R	C3225X5R1C226M	16	22	2
Murata	X5R	GRM32ER61C226K	16	22	2
TDK	X5R	C3225X5R1A476M	10	47	2
Murata	X5R	GRM32ER61C476K	16	47	3
TDK	X5R	C3225X5R0J107M	6.3	100	2
Murata	X5R	GRM32ER60J107M	6.3	100	2
Murata	X5R	GRM32ER61A107M	10	100	2
Kemet	X5R	C1210C107M4PAC7800	16	100	2
Panasonic	POSCAP	6TPE100MI	6.3	100	18
Panasonic	POSCAP	6TPF220M9L	6.3	220	9
Panasonic	POSCAP	6TPE220ML	6.3	220	12

(1) **Capacitor Supplier Verification, RoHS, Lead-free and Material Details**
Consult capacitor suppliers regarding availability, material composition, RoHS and lead-free status, and manufacturing process requirements for any capacitors identified in this table.
(2) Specified capacitance values.
(3) Maximum ESR @ 100kHz, 25°C.

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7.3.6 VERSA-COMP Pin Configurations

The versa-comp feature of the LMZ34202 allows a simple method to adjust the internal compensation network to provide the optimized phase and gain margin based on the output voltage. This easy-to-use feature requires no external components and is implemented by the simple configuration of two adjacent pins on the module.

The versa-comp feature must be configured in one of two ways; VERSA-COMP pin left OPEN or VERSA-COMP pin tied to VADJ. The output voltage determines the appropriate Versa-Comp pin configuration. 表 8 lists the Versa-Comp configuration. 図 19 shows the two possible Versa-Comp pin configurations.

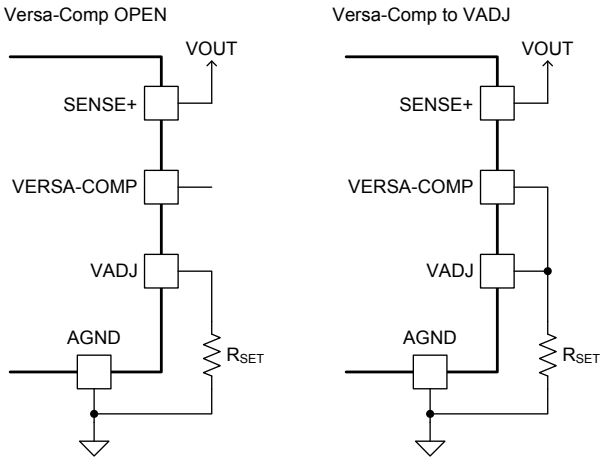


図 19. Versa-Comp Configurations

表 8. VERSA-COMP Pin Configurations

V_{OUT} RANGE (V)		VERSA-COMP PIN CONFIGURATION
MIN	MAX	
2.5	< 3.0	OPEN
3.0	7.5	Connect to VADJ

7.3.7 Input Capacitor Selection

The LMZ34202 requires a ceramic capacitor with a minimum effective input capacitance of 4.7 µF. Use only high-quality ceramic type X5R or X7R capacitors with sufficient voltage rating. An additional 100 µF of non-ceramic capacitance is recommended for applications with transient load requirements. The voltage rating of input capacitors must be greater than the maximum input voltage. To compensate the derating of ceramic capactors, a voltage rating of twice the maximum input voltage is recommended. At worst case, when operating at 50% duty cycle and maximum load, the combined ripple current rating of the input capacitors must be at least 1.0 Arms. 表 9 includes a preferred list of capacitors by vendor.

表 9. Recommended Input Capacitors(1)

VENDOR	SERIES	PART NUMBER	CAPACITOR CHARACTERISTICS		
			WORKING VOLTAGE (V)	CAPACITANCE (2) (µF)	ESR (3) (mΩ)
TDK	X5R	C3225X5R1H106K	50	10	3
Murata	X7R	GRM32ER71H106K	50	10	2
Murata	X7R	GRM32ER71J106K	63	10	2
Panasonic	ZA	EEHZA1H101P	50	100	28
Panasonic	ZA	EEHZA1J560P	63	56	30

(1) **Capacitor Supplier Verification, RoHS, Lead-free and Material Details**
Consult capacitor suppliers regarding availability, material composition, RoHS and lead-free status, and manufacturing process requirements for any capacitors identified in this table.
(2) Specified capacitance values
(3) Maximum ESR @ 100kHz, 25°C.

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7.3.8 Output On/Off Inhibit (INH/UVLO)

The INH/UVLO pin provides on and off control of the device. The INH input provides a precise 2.1 V rising threshold to allow direct logic drive or connection to a voltage divider from a higher voltage source such as PV_{IN}. Once the INH/UVLO pin voltage exceeds the threshold voltage, the device starts operation. The INH input also incorporates 300 mV (typ) of hysteresis resulting in a falling threshold of 1.8 V. If the INH/UVLO pin voltage is pulled below the threshold voltage, the regulator stops switching and enters low quiescent current state. The INH/UVLO pin cannot be open circuit or floating. The simplest way to enable the operation of the LMZ34202 is to connect the INH/UVLO pin to PVIN pin directly as shown in 図 20. This connection allows the LMZ34202 device to restart when PV_{IN} is again within the operation range.

If an application requires controlling the INH/UVLO pin, either drive it directly with a logic input or use an open drain and collector device to interface with the pin and place a 100-kΩ resistor between this pin and PVIN pin as shown in 図 21. When turning Q1 on applies a low voltage to the inhibit control (INH/UVLO) pin and disables the output of the supply, shown in 図 22. If Q1 is turned off, the supply executes a soft-start power-up sequence, as shown in 図 23.

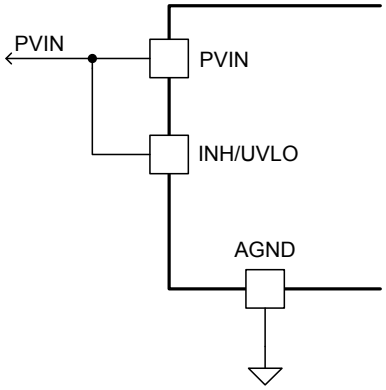


図 20. Enabling the Device

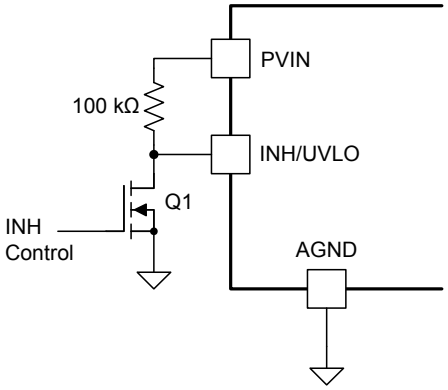


図 21. Typical Inhibit Control

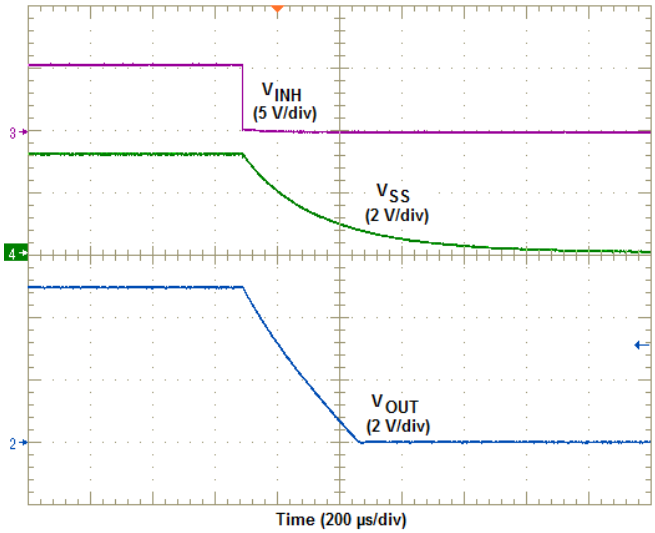


図 22. Inhibit Turn-Off

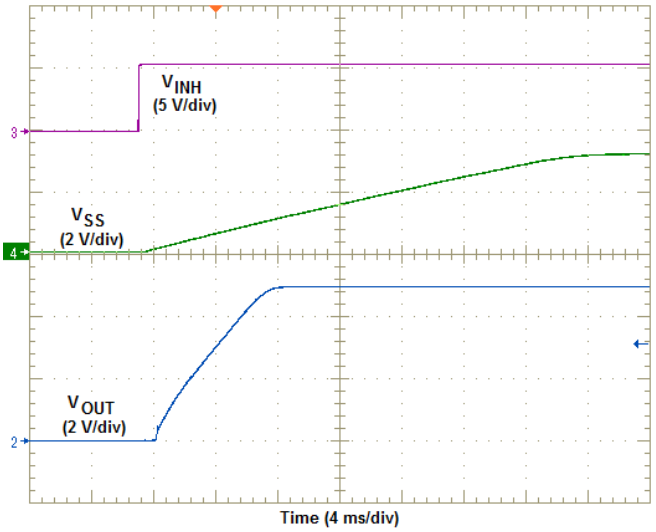


図 23. Inhibit Turn-On

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7.3.9 Under Voltage Lockout (UVLO)

The LMZ34202 device has an internal UVLO circuit which prevents the device from operating until the PV_{IN} voltage exceeds the UVLO threshold, (3.2 V (typ)). The device will begin switching and the output voltage will begin to rise once PV_{IN} exceeds the threshold, however PV_{IN} must be greater than (V_{OUT}/0.75) in order to for V_{OUT} to regulate at the set-point voltage.

Applications may require a higher UVLO threshold to prevent early turn-on, for sequencing requirements, or to prevent input current draw at lower input voltages. An external resistor divider can be added to the INH/UVLO pin to adjust the UVLO threshold higher. The external resistor divider can be configured as shown in 図 24. 表 10 lists standard values for R_{UVLO1} and R_{UVLO2} to adjust the UVLO voltage higher.

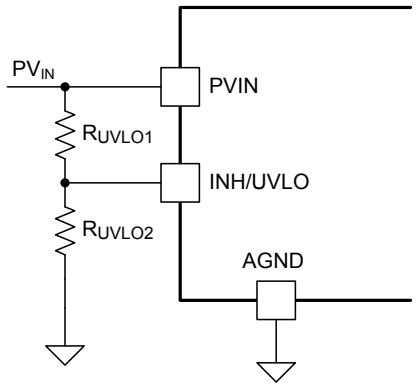


図 24. Adjustable PVIN UVLO

表 10. Resistor Values for Adjusting PVIN UVLO

PVIN UVLO (V)	4.5	10	15	20	25	30
R_{UVLO1} (kΩ)	100	100	100	100	100	100
R_{UVLO2} (kΩ)	46.4	21.0	14.0	10.5	8.45	6.98

7.3.10 Remote Sense

The SENSE+ pin must be connected to V_{OUT} at the load, or at the device pins.

Connecting the SENSE+ pin to V_{OUT} at the load improves the load regulation performance of the device by allowing it to compensate for any I-R voltage drop between its output pins and the load. An I-R drop is caused by the high output current flowing through the small amount of pin and trace resistance. This should be limited to a maximum of 300 mV.

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The remote sense feature is not designed to compensate for the forward drop of nonlinear or frequency dependent components that may be placed in series with the converter output. Examples include OR-ing diodes, filter inductors, ferrite beads, and fuses. When these components are enclosed by the SENSE+ connection, they are effectively placed inside the regulation control loop, which can adversely affect the stability of the regulator.

7.3.11 VBSEL

The VBSEL pin allows the user to select the input source of the internal bias circuitry to improve efficiency. For output voltages ≥ 4.5 V, connect this pin to VOUT. For output voltages < 4.5 V, connect this pin to AGND.

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7.3.12 Soft-Start (SS/TR)

Leaving SS/TR pin open enables the internal slow start time interval of approximately 4.1 ms. Adding additional capacitance between the SS pin and AGND increases the slow start time. Increasing the slow start time will reduce inrush current seen by the input source and reduce the current seen by the device when charging the output capacitors. To avoid the activation of current limit and ensure proper start-up, the SS capacitor may need to be increased when operating near the maximum output capacitance limit.

See 表 11 below for SS capacitor values and timing interval.

表 11. Soft-Start Capacitor Values and Soft-Start Time

C_{SS} (nF)	open	15	22	33	47
SS Time (ms)	4.1	7	10	15	20

7.3.13 Power Good (PWRGD) and Pull-up (PWRGD_PU)

The PWRGD pin is an open drain output. Once the voltage on the SENSE+ pin is between 95% and 105% of the set voltage, the PWRGD pin pull-down is released and the pin floats. The recommended pullup resistor value is between 10 kΩ and 100-kΩ to a voltage source that is 12 V or less. The LMZ34202 has an internal 100-kΩ between the PWRGD pin (pin 20) and the PWRGD_PU pin (pin 21). Connect the PWRGD_PU pin to an external voltage source to avoid using an external pullup resistor. The PWRGD pin is pulled low when the voltage on SENSE+ is lower than 90% or greater than 110% of the nominal set voltage.

7.3.14 Overcurrent Protection

For protection against load faults, the LMZ34202 incorporates output overcurrent protection. Applying a load that exceeds the regulator's overcurrent threshold causes the output to shut down when the output voltage falls below the PWRGD threshold. Following shutdown, the module periodically attempts to recover by initiating a soft-start power-up as shown in 図 25. This is described as a hiccup mode of operation, whereby the module continues in a cycle of successive shutdown and power up until the load fault is removed. During this period, the average current flowing into the fault is significantly reduced which reduces power dissipation. Once the fault is removed, the module automatically recovers and returns to normal operation as shown in 図 26.

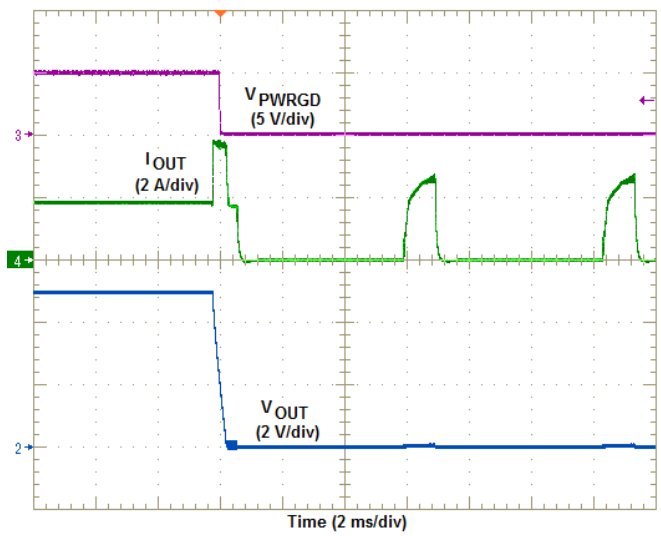


図 25. Overcurrent Limiting

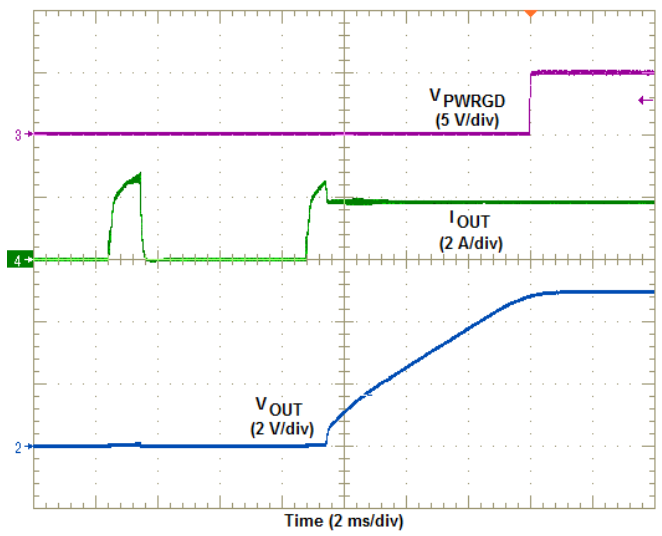


図 26. Removal of Overcurrent

7.3.15 Thermal Shutdown

The internal thermal shutdown circuitry forces the device to stop switching if the junction temperature exceeds 160°C typically. The device reinitiates the power up sequence when the junction temperature drops below 150°C typically.

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7.4 Device Functional Modes

7.4.1 Active Mode

The LMZ34202 is in Active Mode when PVIN is above the UVLO threshold and the INH/UVLO pin voltage is above the INH high threshold. The simplest way to enable the LMZ34202 is to connect the INH/UVLO terminal to PVIN. This allows self start-up of the LMZ34202 when the input voltage is in the operation range: 4.5 V to 42 V.

7.4.2 Light Load Operation

At light load, the LMZ34202 operates in pulse skip mode to improve efficiency and decrease power dissipation by reducing switching losses and gate drive losses. In light load operation (PFM mode), the output voltage can rise slightly above the set-point specification. To avoid this behavior, a 300-mA load is required on the output.

7.4.3 Shutdown Mode

The INH/UVLO pin provides electrical ON and OFF control for the LMZ34202. When the INH/UVLO pin voltage is below the INH threshold, the device is in shutdown mode. In shutdown mode the stand-by current is 2.4 μA typically with PV_{IN} = 24 V. The LMZ34202 also employs under voltage lock out protection. If PV_{IN} is below the UVLO level, the output of the regulator turns off.

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8 Application and Implementation

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Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The LMZ34202 is a synchronous step down DC-DC power module. It is used to convert a higher DC voltage to a lower DC voltage with a maximum output current of 2 A. The following design procedure can be used to select components for the LMZ34202. Alternately, the WEBENCH® software may be used to generate complete designs. When generating a design, the WEBENCH software utilizes an iterative design procedure and accesses comprehensive databases of components.

8.2 Typical Application

8.2.1 Minimum External Component Application

The LMZ34202 requires only a few external components to convert from a wide input voltage supply range to a wide range of output voltages. 図 27 shows a basic LMZ34202 schematic with only the minimum required components.

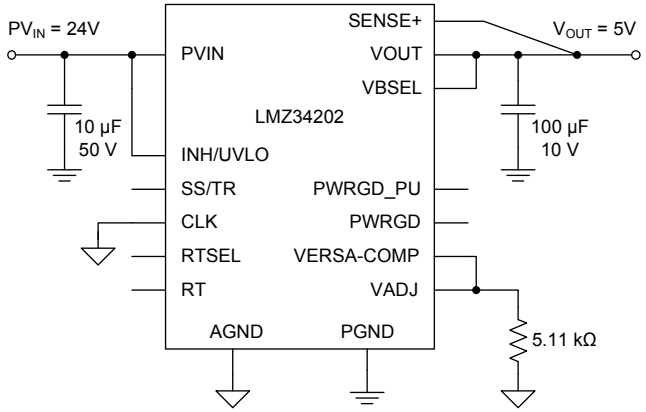


図 27. LMZ34202 Minimum External Component Application

8.2.1.1 Design Requirements

For this design example, use the parameters listed in 表 12 and follow the design procedures below.

表 12. Design Example Parameters

DESIGN PARAMETER	VALUE
Input Voltage PV_{IN}	24 V typical
Output Voltage V_{OUT}	5.0 V
Output Current Rating	2 A
Operating Frequency	500 kHz

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8.2.1.2 Detailed Design Procedure

8.2.1.2.1 Custom Design With WEBENCH® Tools

Click here to create a custom design using the LMZ34202 device with the WEBENCH® Power Designer.

1. Start by entering the input voltage (V_{IN}), output voltage (V_{OUT}), and output current (I_{OUT}) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance
- Run thermal simulations to understand board thermal performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

8.2.1.2.2 Output Voltage Set-Point

The output voltage of the LMZ34202 device is externally adjustable using a single resistor (R_{SET}). Select the value of R_{SET} from 表 2 or calculate using 式 3:

$$R_{SET} = \frac{20}{\left[\left(\frac{V_{OUT}}{1.011}\right) - 1\right]} \ (k\Omega) \tag{3}$$

Knowing the desired output voltage is 5 V, the R_{SET} value can then be calculated using 式 3 or selected from 表 2. The formula yields a value of 5.07 kΩ. Choose the closest available value of 5.11 kΩ for R_{SET}.

8.2.1.2.3 RT and RTSEL

The default switching frequency of the LMZ34202 is set to 500 kHz by leaving the RT pin open and the RTSEL pin open. The switching frequency of this application is 500-kHz, therefore no additional resistor is required to set the switching frequency. If another frequency is desired, use 表 3 to select the required resistor value.

8.2.1.2.4 VERSA-COMP

The Versa-Comp feature of the LMZ34202 configures the internal compensation based on the output voltage. From 表 8, the required Versa-Comp configuration for a 5-V output is to connect the VERSA-COMP pin to the VADJ pin.

8.2.1.2.5 VBSEL

The VBSEL pin allows the user to select the input source of the internal bias circuitry to improve efficiency. For output voltages ≥ 4.5 V, connect this pin to VOUT. For output voltages < 4.5 V, connect this pin to AGND.

8.2.1.2.6 Input Capacitors

For this design, a 10-µF, X7R dielectric ceramic capacitor rated for 50 V is used for the input decoupling capacitor. The effective capacitance at 24 V is 5.7 µF, the equivalent series resistance (ESR) is approximately 3 mΩ, and the current-rating is 5 A.

8.2.1.2.7 Output Capacitors

The minimum required output capacitance for a 5 V output is 64 µF of ceramic capacitance. For this design, a 100 µF, X5R dielectric ceramic capacitor rated for 10 V is used for the output capacitor.

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8.2.1.3 Application Curves

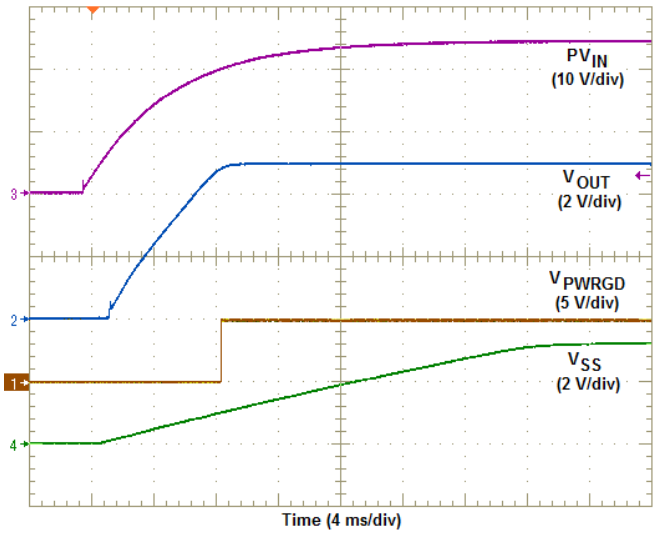


図 28. Start-up Waveforms

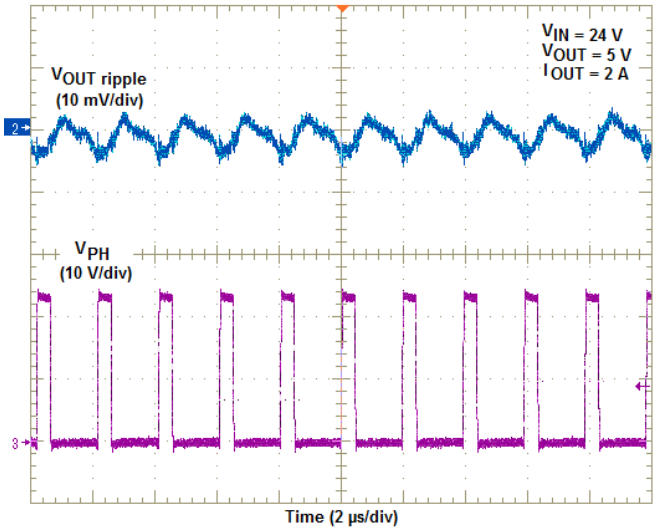


図 29. Output Ripple and PH Node Waveforms

8.2.2 INH Control Application

図 30 shows a more typical use schematic which makes use of the INH control, Versa-Comp, SS, PWRGD and PWRGD_PU features, along with adjusting the switching frequency with an external resistor. Setting these additional features is descibed below.

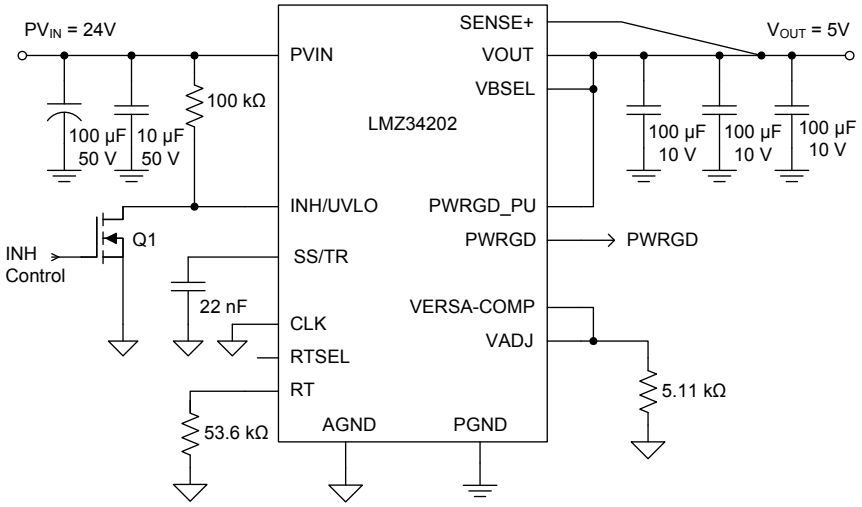


図 30. LMZ34202 Typical Schematic

8.2.2.1 Design Requirements

For this design example, use the parameters listed in 表 13 as the input parameters. For the complete design procedures start with the procedures for the basic application above as well as the procedures listed below.

表 13. Design Example Parameters

DESIGN PARAMETER	VALUE
Input Voltage PV_{IN}	24 V typical
Output Voltage V_{OUT}	5.0 V
Output Current Rating	2 A

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表 13. Design Example Parameters (continued)

DESIGN PARAMETER	VALUE
Operating Frequency	750 kHz
Inhibit Control	Yes
Power Good Signal	Yes
Slow Start Time	10 ms
Output Capacitance	300 µF

8.2.3 Detailed Design Procedure

8.2.3.1 Switching Frequency

To adjust the switching frequency place a resistor between the RT pin (pin 9) and AGND. Refer to 表 3 to select the required value for R_{RT} resistor. To set the switching frequency to 750 kHz, the value for R_{RT} is 53.6 kΩ, selected from 表 3.

8.2.3.2 Power Good

The PWRGD pin is an open drain output. The LMZ34202 includes an internal 100 kΩ pullup resistor between the PWRGD pin and the PWRGD_PU pin. Connecting the PWRGD_PU pin to a pullup voltage allows use of the PWRGD signal without adding an additional component. In this example, the 5-V output is used as the pullup voltage.

8.2.3.3 Inhibit Control

To control the turn ON and OFF of the LMZ34202, an open-drain and collector device is recommended. The open-drain and collector device must be rated for the maximum voltage applied to PVIN. A pull-up resistor is required between the INH/UVLO pin and PVIN. Place a 100-kΩ resistor between the INH/UVLO pin and the PVIN pin.

8.2.3.4 VERSA-COMP

The Versa-Comp feature of the LMZ34202 configures the internal compensation based on the output voltage. From 表 8, the required Versa-Comp configuration for a 5-V output is to connect the VERSA-COMP pin to the VADJ pin.

8.2.3.5 VBSEL

The VBSEL pin allows the user to select the input source to the internal power circuitry to improve efficiency. For output voltages ≥ 4.5 V, connect this pin to VOUT. For output voltages < 4.5 V, connect this pin to AGND.

8.2.3.6 Soft-Start Capacitors

When the SS/TRK pin remains floating the LMZ34202 implements a typical soft-start time of 4.1 ms. In order to increase the slow start time, an external slow start capacitor, C_{SS} must be placed between the SS/TRK pin and AGND. Select a value for C_{SS} from 表 11.

For the desired soft-start time of 10 ms, a soft-start capacitor value of 22 nF is selected from 表 11.

8.2.3.7 Input Capacitors

For this design, a 10-µF ceramic capacitor plus a 100-µF aluminum electrolytic capacitor, both rated for 50 V are used for the input decoupling capacitors.

8.2.3.8 Output Capacitors

The maximum allowable output capacitance for a 5-V output is 350 µF of capacitance. At least 64 µF of capacitance must be ceramic type. For this design, 3× 100-µF, X5R dielectric ceramic capacitors rated for 10 V are used for the output capacitors.

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9 Power Supply Recommendations

The LMZ34202 is designed to operate from an input voltage supply range between 4.5 V and 42 V. This input supply should be well regulated and able to withstand maximum input current and maintain a stable voltage. The resistance of the input supply rail should be low enough that an input current transient does not cause a high enough drop at the LMZ34202 supply voltage that can cause a false UVLO fault triggering and system reset.

If the input supply is located more than a few inches from the LMZ34202 additional bulk capacitance may be required in addition to the ceramic bypass capacitors. The typical amount of bulk capacitance is 47 µF or the typical amount of electrolytic capacitance is 100 µF.

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10 Layout

The performance of any switching power supply depends as much upon the layout of the PCB as the component selection. The following guidelines will help users design a PCB with the best power conversion performance, thermal performance, and minimized generation of unwanted EMI.

10.1 Layout Guidelines

To achieve optimal electrical and thermal performance, an optimized PCB layout is required. 図 31 thru 図 34, shows a typical PCB layout. Some considerations for an optimized layout are:

- Use large copper areas for power planes (PVIN, VOUT, and PGND) to minimize conduction loss and thermal stress.
- Place ceramic input and output capacitors close to the device pins to minimize high frequency noise.
- Locate additional output capacitors between the ceramic capacitor and the load.
- Keep AGND and PGND separate from one another. The connection is made internal to the device.
- Place R_{SET}, R_{RT}, and C_{SS} as close as possible to their respective pins.
- Use multiple vias to connect the power planes to internal layers.

10.2 Layout Example

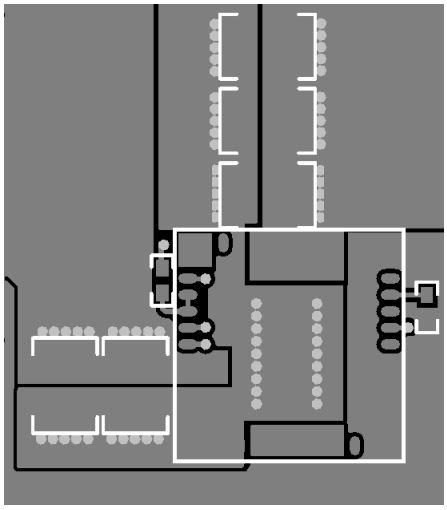


図 31. Typical Top-Layer Layout

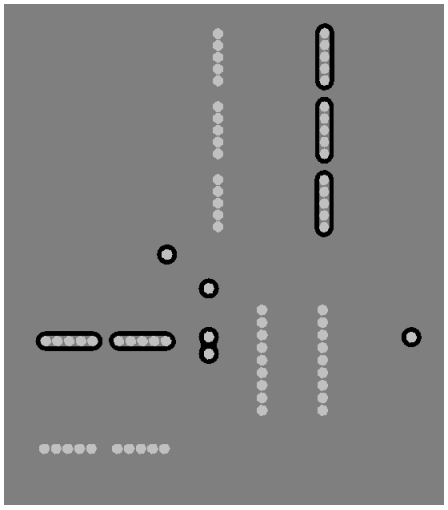


図 32. Typical Layer-2 Layout

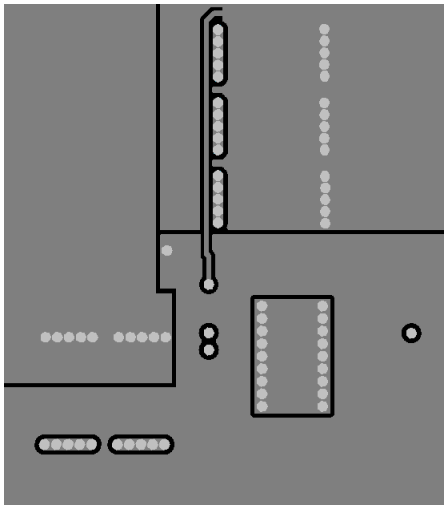


図 33. Typical Layer-3 Layout

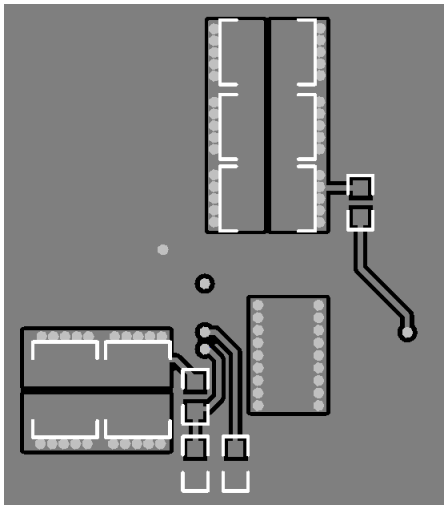


図 34. Typical Bottom-Layer Layout

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10.3 EMI

The LMZ34202 is compliant with EN55022 Class B radiated emissions. 図 35 図 36 show typical examples of radiated emissions plots for the LMZ34202 operating from 24 V. Both graphs include the plots of the antenna in the horizontal and vertical positions.

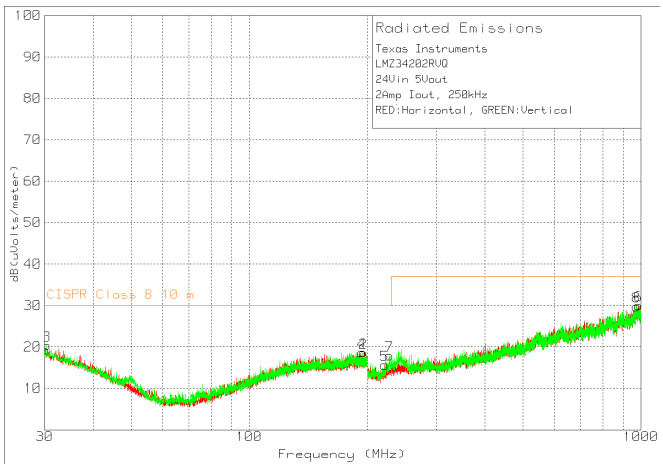


図 35. Radiated Emissions (EN55022 Class B)
24-V Input, 5-V Output, 2-A Load, 250 kHz

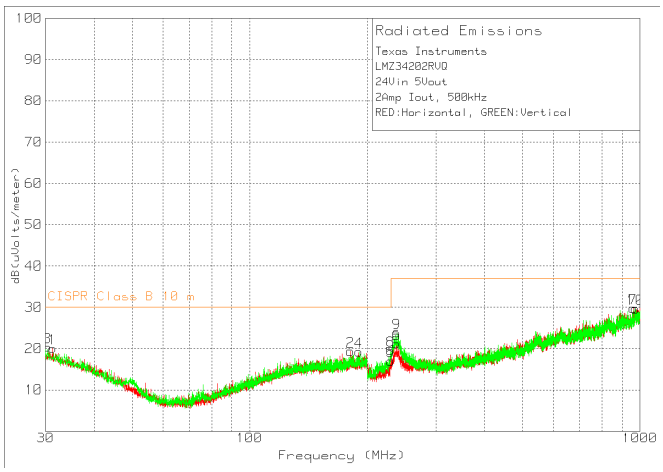


図 36. Radiated Emissions (EN55022 Class B)
24-V Input, 5-V Output, 2-A Load, 500 kHz

11 デバイスおよびドキュメントのサポート

11.1 デバイス・サポート

11.1.1 開発サポート

11.1.1.1 WEBENCH®ツールによるカスタム設計

ここをクリックすると、WEBENCH® Power Designerにより、LMZ34202を使用するカスタム設計を作成できます。

1. 最初に、入力電圧(V_{IN})、出力電圧(V_{OUT})、出力電流(I_{OUT})の要件を入力します。
2. オプティマイザのダイヤルを使用して、効率、占有面積、コストなどの主要なパラメータについて設計を最適化します。
3. 生成された設計を、テキサス・インスツルメンツが提供する他の方式と比較します。

WEBENCH Power Designerでは、カスタマイズされた回路図と部品リストを、リアルタイムの価格と部品の在庫情報と併せて参照できます。

通常、次の操作を実行可能です。

- 電気的なシミュレーションを実行し、重要な波形と回路の性能を確認する。
- 熱シミュレーションを実行し、基板の熱特性を把握する。
- カスタマイズされた回路図やレイアウトを、一般的なCADフォーマットで出力する。
- 設計のレポートをPDFで印刷し、設計を共有する。

WEBENCHツールの詳細は、www.ti.com/WEBENCHでご覧になれます。

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設計サポート ***TIの設計サポート*** **役に立つE2Eフォーラムや、設計サポート・ ツールをすばやく見つけることができます。技術サポート用の連絡先情報も参照できます。**

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11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。これらの情報は、指定のデバイスに対して提供されている最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LMZ34202RVQR	Active	Production	B3QFN (RVQ) | 43	500 | LARGE T&R	Exempt	NIPDAU	Level-3-245C-168 HR	-40 to 105	LMZ34202
LMZ34202RVQR.A	Active	Production	B3QFN (RVQ) | 43	500 | LARGE T&R	Exempt	NIPDAU	Level-3-245C-168 HR	-40 to 105	LMZ34202
LMZ34202RVQT	Active	Production	B3QFN (RVQ) | 43	250 | SMALL T&R	Yes	NIPDAU	Level-3-245C-168 HR	-40 to 105	LMZ34202
LMZ34202RVQT.A	Active	Production	B3QFN (RVQ) | 43	250 | SMALL T&R	Yes	NIPDAU	Level-3-245C-168 HR	-40 to 105	LMZ34202

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

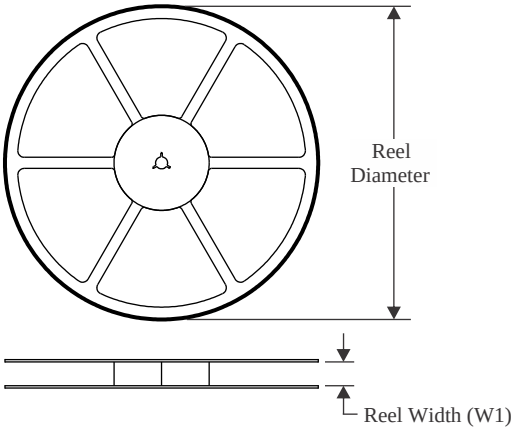
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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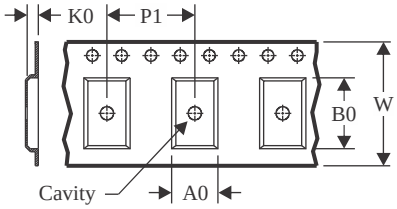
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TAPE AND REEL INFORMATION

REEL DIMENSIONS

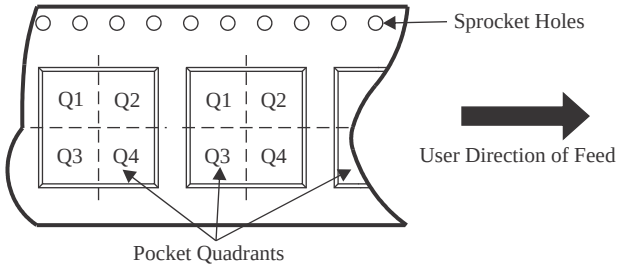


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

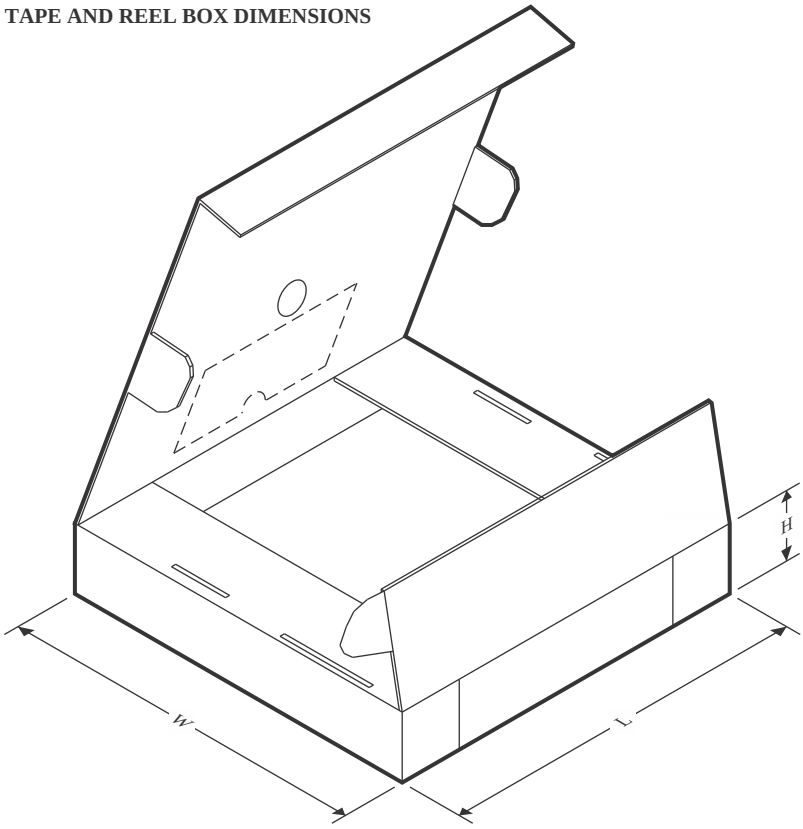
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMZ34202RVQR	B3QFN	RVQ	43	500	330.0	24.4	10.35	10.35	4.6	16.0	24.0	Q2
LMZ34202RVQT	B3QFN	RVQ	43	250	330.0	24.4	10.35	10.35	4.6	16.0	24.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

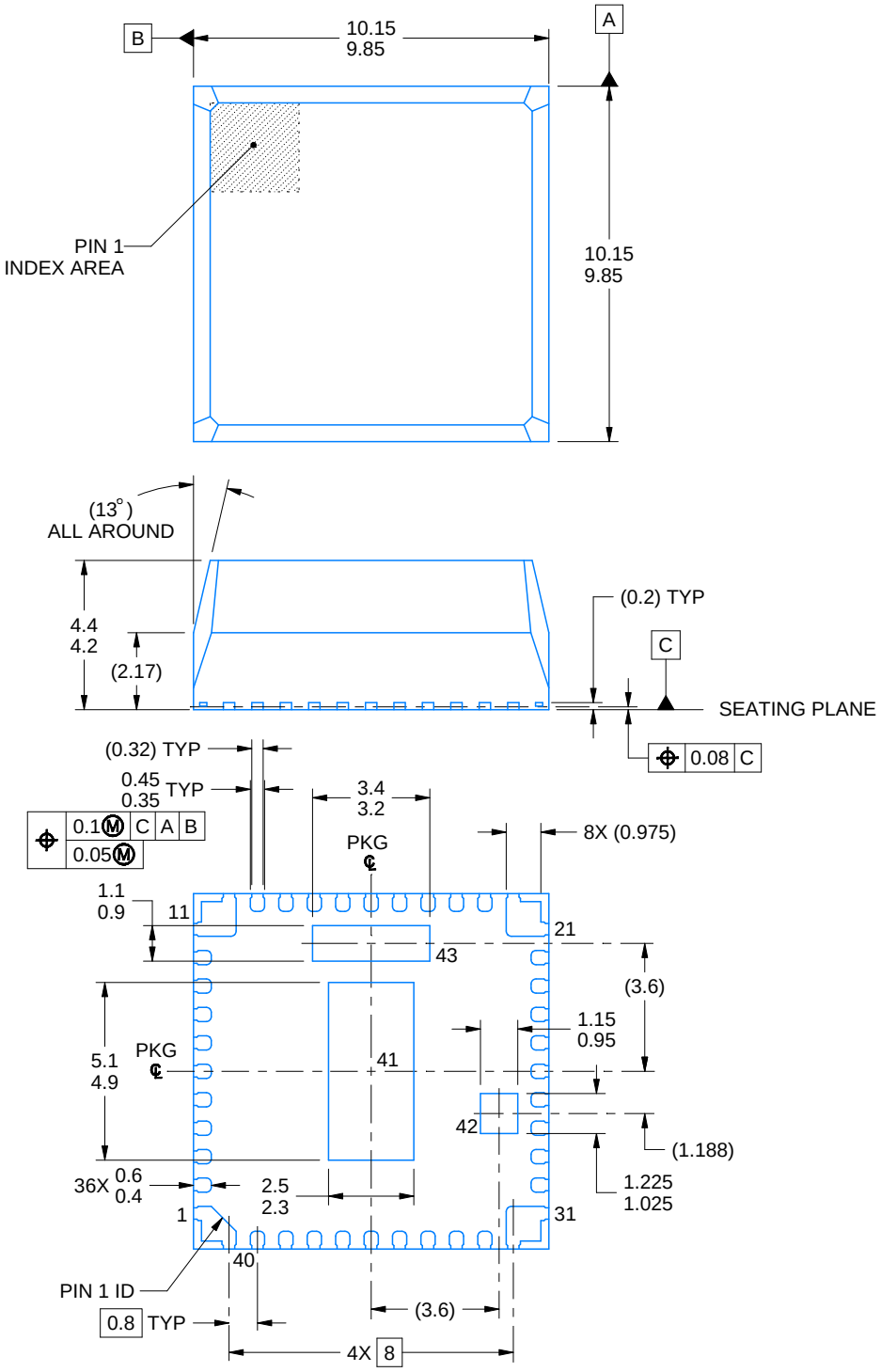
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMZ34202RVQR	B3QFN	RVQ	43	500	383.0	353.0	58.0
LMZ34202RVQT	B3QFN	RVQ	43	250	383.0	353.0	58.0

PACKAGE OUTLINE

RVQ0043A

B3QFN - 4.4mm max height

PLASTIC QUAD FLATPACK - NO LEAD



4226463/A 02/2021

NOTES:

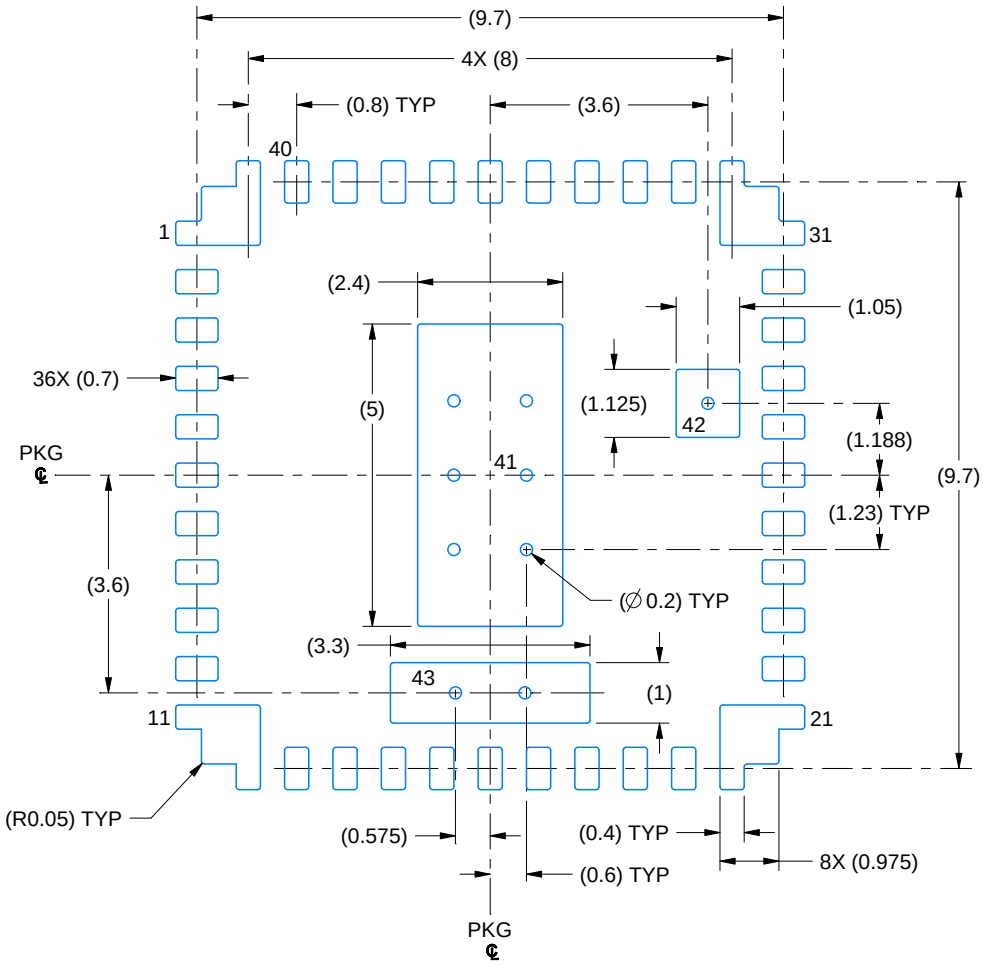
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pads must be soldered to the printed circuit board for optimal thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

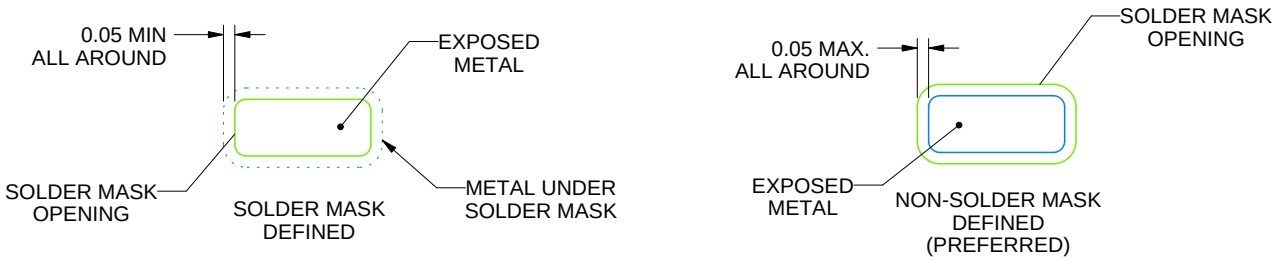
RVQ0043A

B3QFN - 4.4mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X

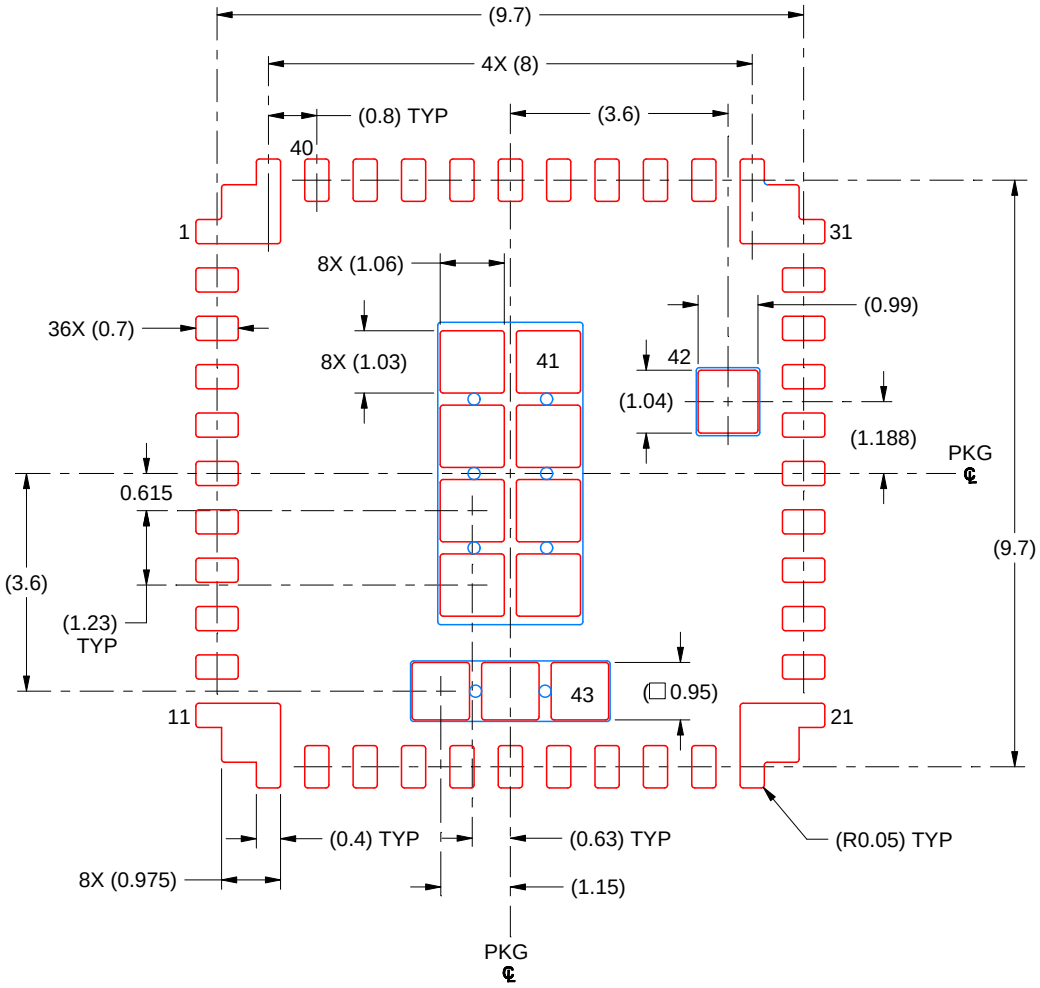


SOLDER MASK DETAIL

4226463/A 02/2021

NOTES: (continued)

4. This package designed to be soldered to a thermal pads on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm STENCIL THICKNESS

EXPOSED PAD 41:
73% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

EXPOSED PAD 42:
87% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

EXPOSED PAD 43:
82% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:8X

4226463/A 02/2021

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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