TEXAS INSTRUMENTS
LMZM33602
JAJSEO9D – DECEMBER 2017 – REVISED AUGUST 2020

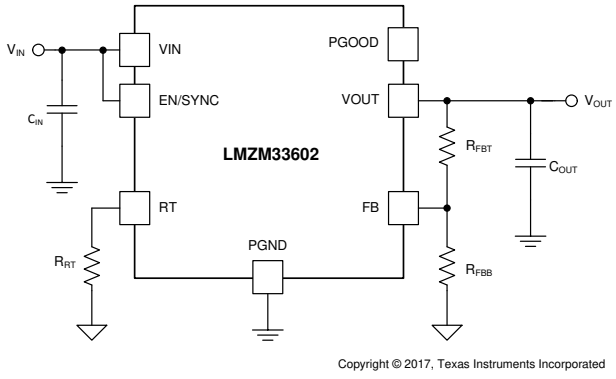
LMZM33602 4V～36V 入力、2A、QFN パッケージの電源モジュール

1 特長

- 完全に統合された電源ソリューション
  - 外部部品点数はわずか 4 個
  - 100mm^2 未満の小さなソリューション・サイズ
- 9mm × 7mm × 4mm の QFN パッケージ
  - すべてのピンにパッケージの周囲からアクセス可能
  - 3A の LMZM33603 とピン互換
- 入力電圧範囲：4V～36V
- 出力電圧範囲：1V～18V
- 最大 95% の効率
- 200kHz～1.2MHz の調整可能なスイッチング周波数
- 外部クロックに同期可能
- パワー・グッド出力
- EN55011 Class B 放射 EMI 標準に合致
- 動作時の IC 接合部温度範囲：–40℃～+125℃
- 動作時の周囲温度範囲：–40℃～+105℃
- WEBENCH® Power Designer により、LMZM33602 を使用するカスタム設計を作成

2 アプリケーション

- ファクトリ / ビルディング・オートメーション
- スマート・グリッド / エネルギー
- 産業用
- 医療用
- 防衛
- 反転出力アプリケーション



概略回路図

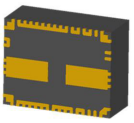
3 概要

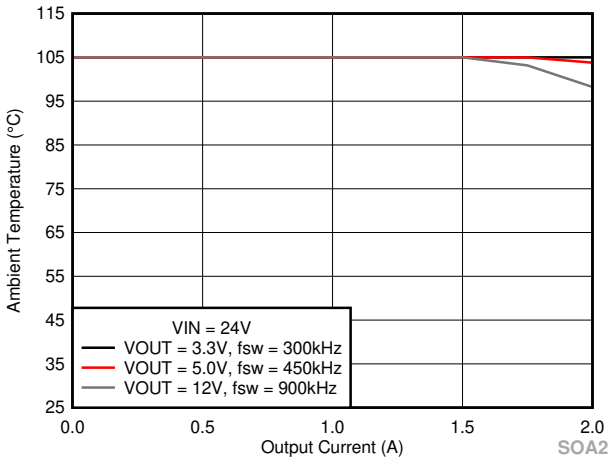
LMZM33602 パワー・モジュールは、2A の降圧型 DC/DC コンバータをパワー MOSFET、シールド付きインダクタ、およびパッシブ部品とともに低プロファイルのパッケージに実装した、使いやすい集積電源ソリューションです。わずか 4 個の外付け部品で電源ソリューションを構築でき、設計においてループ補償や磁気部品の選択が不要になります。

9mm × 7mm × 4mm の 18 ピン QFN パッケージは、プリント基板に簡単にハンダ付けでき、コンパクトで薄型のポイント・オブ・ロード (POL) 設計が可能です。LMZM33602 はパワー・グッド、プログラム可能な UVLO、プリバイアス・スタートアップ、過電流および過熱保護などの完全な機能セットを備えているため、広範なアプリケーションの電源として非常に優れたデバイスです。

製品情報

デバイス番号	パッケージ	本体サイズ (公称)
LMZM33602	QFN (18)	9.00mm × 7.00mm





安全動作領域

英語版の TI 製品についての情報を翻訳したこの資料は、製品の概要を確認する目的で便宜的に提供しているものです。該当する正式な英語版の最新情報は、www.ti.com で閲覧でき、その内容が常に優先されます。TI では翻訳の正確性および妥当性につきましては一切保証いたしません。実際の設計などの前には、必ず最新版の英語版をご参照くださいますようお願いいたします。

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4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision C (March 2018) to Revision D (August 2020) — **Page**

- 文書全体にわたって表、図、相互参照の採番方法を更新 ... 1
- Updated Storage temperature range in *Absolute Maximum Ratings* ... 4

Changes from Revision B (February 2018) to Revision C (March 2018) — **Page**

- Added *セクション 9.4* section ... 24

Changes from Revision A (February 2018) to Revision B (February 2018) — **Page**

- 量産データのデータシートの初版 ... 1

Changes from Revision * (December 2017) to Revision A (January 2018) — **Page**

- SNVA800 アプリケーション・レポートへのリンクを記載した新しい「*アプリケーション*」セクションを追加。編集上の細かい更新。 ... 1
- Added sentence re: inverting buck-boost topology to *セクション 8.1* ... 20

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5 Pin Configuration and Functions

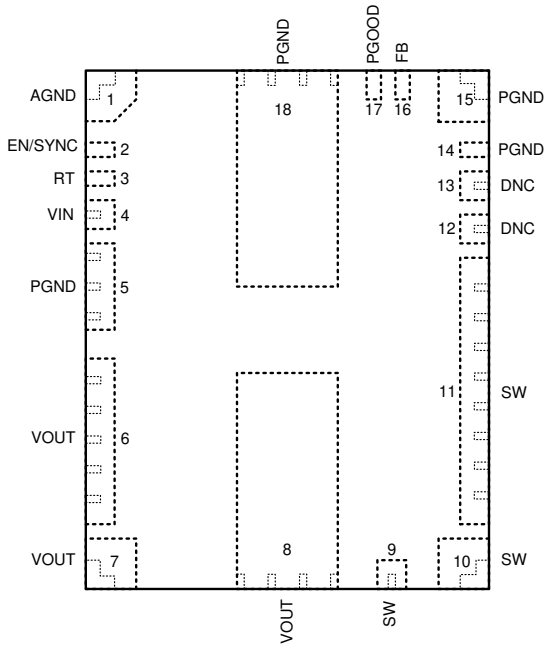


図 5-1. RLR Package 18-Pin QFN Top View

Pin Functions

PIN		TYPE	DESCRIPTION
NO.	NAME		
1	AGND	G	Analog ground. Zero voltage reference for internal references and logic. Do not connect this pin to PGND; the connection is made internal to the device. See the *セクション Layout* of the data sheet for a recommended layout.
2	EN/SYNC	I	EN - Enable input to regulator. High = On, Low = Off. Can be connected to VIN. Do not float. This pin can be used to set the input undervoltage lockout with two resistors. See *セクション 7.3.9*. SYNC - The internal oscillator can be synchronized to an external clock via AC-coupling. See *セクション 7.3.5* for details.
3	RT	I	An external timing resistor connected between this pin and AGND adjusts the switching frequency of the device. If left open, the default switching frequency is 400 kHz.
4	VIN	I	Input supply voltage. Connect external input capacitors between this pin and PGND.
5, 14, 15, 18	PGND	G	Power ground. This is the return current path for the power stage of the device. Connect pin 5 to the input source, the load, and to the bypass capacitors associated with VIN and VOUT using power ground planes on the PCB. **Pins 14 and 15 are not connected to PGND internal to the device and must be connected to PGND at pad 18.** Connect pad 18 to the power ground planes using multiple vias for good thermal performance. See *セクション Layout* of the data sheet for a recommended layout.
6, 7, 8	VOUT	O	Output voltage. These pins are connected to the internal output inductor. Connect these pins to the output load and connect external bypass capacitors between these pins and PGND.
9, 10, 11	SW	O	Switch node. Connect these pins to a small copper island under the device for thermal relief. Do not place any external component on these pins or tie them to a pin of another function.
12, 13	DNC	—	Do not connect. **Each pin must be soldered to an isolated pad**. These pins connect to internal circuitry. Do not connect these pins to one another, AGND, PGND, or any other voltage.
16	FB	I	Feedback input. Connect the center point of the feedback resistor divider to this pin. Connect the upper resistor (R_{FBT}) of the feedback divider to V_{OUT} at the desired point of regulation. Connect the lower resistor (R_{FBB}) of the feedback divider to AGND.
17	PGOOD	O	Open drain output for power-good flag. Use a 10-kΩ to 100-kΩ pullup resistor to logic rail or other DC voltage no higher than 12 V.

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6 Specifications

6.1 Absolute Maximum Ratings

Over operating ambient temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Input voltage	VIN	–0.3	42	V
	EN/SYNC	–5.5	V_{IN} + 0.3	V
	PGOOD	–0.3	15	V
	FB, RT	–0.3	4.5	V
Output voltage	SW	–1	V_{IN} + 0.3	V
	SW (< 10-ns transients)	–5	42	V
	VOUT	–0.3	V_{IN}	V
Sink current	PGOOD		3	mA
Mechanical shock	Mil-STD-883D, Method 2002.3, 1 msec, 1/2 sine, mounted		500	G
Mechanical vibration	Mil-STD-883D, Method 2007.2, 20 to 2000 Hz		20	G
Operating IC junction temperature, T_J (2)		–40	125	°C
Operating ambient temperature, T_A (2)		–40	105	°C
Storage temperature, T_{stg}		–55	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) The ambient temperature is the air temperature of the surrounding environment. The junction temperature is the temperature of the internal power IC when the device is powered. Operating below the maximum ambient temperature, as shown in the safe operating area (SOA) curves in the typical characteristics sections, ensures that the maximum junction temperature of any component inside the module is never exceeded.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2500	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±750	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

Over operating ambient temperature range (unless otherwise noted)

	MIN	MAX	UNIT
Input voltage, V_{IN}	4(1)	36	V
Output voltage, V_{OUT}	1	18	V
EN/SYNC voltage	–5	VIN	V
PGOOD pullup voltage, V_{PGOOD}	–0.3	12	V
PGOOD sink current, I_{PGOOD}		1	mA
Output current, I_{OUT}	0	2	A
Operating ambient temperature, T_A	–40	105	°C

(1) For output voltages ≤ 5 V, the recommended minimum V_{IN} is 4 V or (V_{OUT} + 1.5 V), whichever is greater. For output voltages > 5 V, the recommended minimum V_{IN} is (1.3 × V_{OUT}). See *Voltage Dropout* for information on voltage dropout.

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6.4 Thermal Information

THERMAL METRIC[1]		LMZM33602 RLR (QFN) 18 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance[2]	18.9	°C/W
ψ_{JT}	Junction-to-top characterization parameter[3]	2.0	°C/W
ψ_{JB}	Junction-to-board characterization parameter[4]	6.2	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report, SPRA953.
(2) The junction-to-ambient thermal resistance, $R_{\theta JA}$, applies to devices soldered directly to a 63 mm × 63 mm, 4-layer PCB with 2 oz. copper and natural convection cooling. Additional airflow reduces $R_{\theta JA}$.
(3) The junction-to-top board characterization parameter, ψ_{JT}, estimates the junction temperature, T_J, of a device in a real system, using a procedure described in JESD51-2A (section 6 and 7). $T_J = \psi_{JT} \times Pdis + T_T$; where Pdis is the power dissipated in the device and T_T is the temperature of the top of the device.
(4) The junction-to-board characterization parameter, ψ_{JB}, estimates the junction temperature, T_J, of a device in a real system, using a procedure described in JESD51-2A (sections 6 and 7). $T_J = \psi_{JB} \times Pdis + T_B$; where Pdis is the power dissipated in the device and T_B is the temperature of the board 1mm from the device.

6.5 Electrical Characteristics

Over –40°C to +105°C ambient temperature, V_{IN} = 24 V, V_{OUT} = 5 V, I_{OUT} = I_{OUT} maximum, f_{sw} = 450 kHz (unless otherwise noted); C_{IN1} = 2 × 4.7-µF, 50-V, 1210 ceramic; C_{IN2} = 100-µF, 50-V, electrolytic; C_{OUT} = 4 × 22-µF, 25-V, 1210 ceramic. Minimum and maximum limits are specified through production test or by design. Typical values represent the most likely parametric norm and are provided for reference only.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
INPUT VOLTAGE (V_{IN})							
V_{IN}	Input voltage	Over I_{OUT} range		4[1]		36	V
UVLO	V_{IN} undervoltage lockout	V_{IN} increasing		3.3	3.6	3.9	V
		V_{IN} decreasing		3	3.3	3.5	V
I_{SHDN}	Shutdown supply current	V_{EN} = 0 V, V_{IN} = 12 V			2	4	µA
OUTPUT VOLTAGE (V_{OUT})							
$V_{OUT(ADJ)}$	Output voltage adjust	Over I_{OUT} range		1		18	V
$V_{OUT(Ripple)}$	Output voltage ripple	20-MHz bandwidth			10		mV
FEEDBACK							
V_{FB}	Feedback voltage[2]	T_A = 25°C, I_{OUT} = 0 A		0.985	1	1.015	V
		Over V_{IN} range, –40°C ≤ T_J ≤ 125°C, I_{OUT} = 0 A		0.98	1	1.02	V
	Load regulation	Over I_{OUT} range, T_A = 25°C			0.04%		
I_{FB}	Feedback leakage current	V_{FB} = 1 V			10		nA
CURRENT							
I_{OUT}	Output current	Natural convection, T_A = 25°C		0		2	A
	Overcurrent threshold				3.6		A
PERFORMANCE							
η	Efficiency	V_{IN} = 24 V, I_{OUT} = 1 A	V_{OUT} = 12 V, f_{SW} = 900 kHz		94%		
			V_{OUT} = 5 V, f_{SW} = 450 kHz		90%		
			V_{OUT} = 3.3 V, f_{SW} = 300 kHz		88%		
		V_{IN} = 12 V, I_{OUT} = 1 A	V_{OUT} = 5 V, f_{SW} = 450 kHz		93%		
			V_{OUT} = 3.3 V, f_{SW} = 300 kHz		91%		
			V_{OUT} = 2.5 V, f_{SW} = 250 kHz		89%		
	Transient response	25% to 75% load step 1 A/µs slew rate	Over/undershoot		90		mV
			Recovery time		55		µs

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Over –40°C to +105°C ambient temperature, V_{IN} = 24 V, V_{OUT} = 5 V, I_{OUT} = I_{OUT} maximum, f_{sw} = 450 kHz (unless otherwise noted); C_{IN1} = 2 × 4.7-µF, 50-V, 1210 ceramic; C_{IN2} = 100-µF, 50-V, electrolytic; C_{OUT} = 4 × 22-µF, 25-V, 1210 ceramic. Minimum and maximum limits are specified through production test or by design. Typical values represent the most likely parametric norm and are provided for reference only.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SOFT START						
T_{SS}	Internal soft start time			6		ms
THERMAL						
T_{SHDN}	Thermal shutdown	Shutdown temperature		170		°C
		Hysteresis		15		°C
ENABLE (EN)						
V_{EN-H}	EN rising threshold		1.4	1.55	1.7	V
V_{EN-HYS}	EN hysteresis voltage			0.4		V
I_{EN}	EN Input leakage current	V_{IN} = 4 V to 36 V, V_{EN} = 2 V		10	100	nA
		V_{IN} = 4 V to 36 V, V_{EN} = 36 V			1	µA
POWER GOOD (PGOOD)						
V_{PGOOD}	PGOOD thresholds	V_{OUT} rising (good)	92%	94%	96.5%	
		V_{OUT} rising (fault)	104%	107%	110%	
		V_{OUT} falling hysteresis		1.5%		
	Minimum V_{IN} for valid PGOOD	50-µA pullup, V_{EN} = 0 V, T_A = 25°C			1.5	V
	PGOOD low voltage	0.5-mA pullup, V_{EN} = 0 V			0.4	V
CAPACITANCE						
C_{IN}	External input capacitance	Ceramic type	9.4(3)			µF
		Non-ceramic type		47(3)		µF
C_{OUT}	External output capacitance		min(4)		max(5)	µF

(1) See *Voltage Dropout* for information on voltage dropout.
(2) The overall output voltage tolerance will be affected by the tolerance of the external R_{FBT} and R_{FBB} resistors.
(3) A minimum of 9.4 µF (2 × 4.7 µF) ceramic input capacitance is required for proper operation. An additional 47 µF of bulk capacitance is recommended for applications with transient load requirements. See the *Input Capacitors* section of the datasheet for further guidance.
(4) The minimum amount of required output capacitance varies depending on the output voltage (see *Output Capacitor Selection*). A minimum amount of ceramic output capacitance is required. Locate the capacitance close to the device. Adding additional ceramic or non-ceramic capacitance close to the load improves the response of the regulator to load transients.
(5) The maximum allowable output capacitance varies depending on the output voltage (see *Output Capacitor Selection*).

6.6 Switching Characteristics

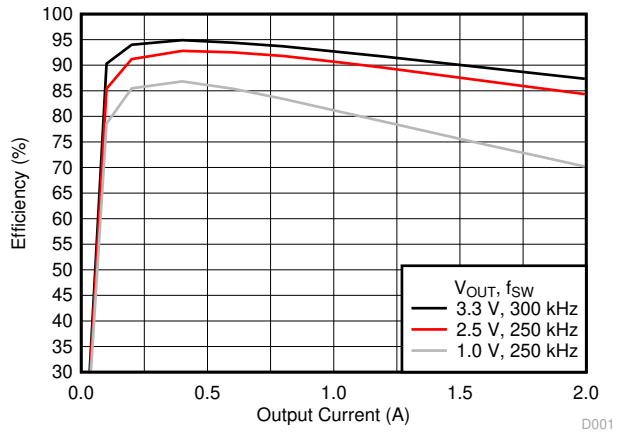
Over operating ambient temperature range (unless otherwise noted)
Minimum and maximum limits are specified through production test or by design. Typical values represent the most likely parametric norm, and are provided for reference only.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
FREQUENCY (RT) and SYNCHRONIZATION (EN/SYNC)						
f_{SW}	Default switching frequency	RT pin = open	340	400	460	kHz
	Switching frequency range		200		1200	kHz
V_{SYNC}	Peak-to-peak amplitude of SYNC clock AC signal (measured at SYNC pin)		2.8		5.5	V
T_{S-MIN}	Minimum SYNC ON/OFF time			100		ns

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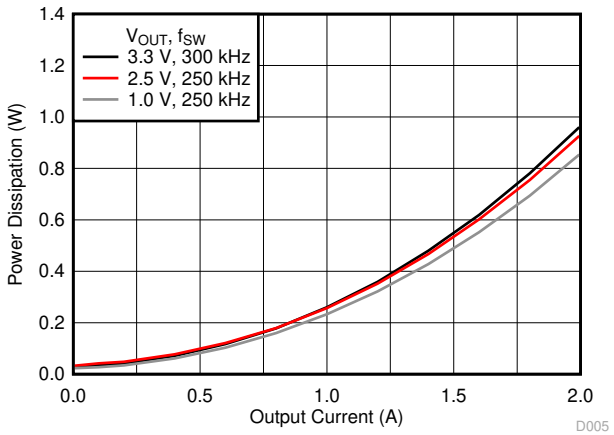
6.7 Typical Characteristics (V_{IN} = 5 V)

The typical characteristic data has been developed from actual products tested at 25°C. This data is considered typical for the device.



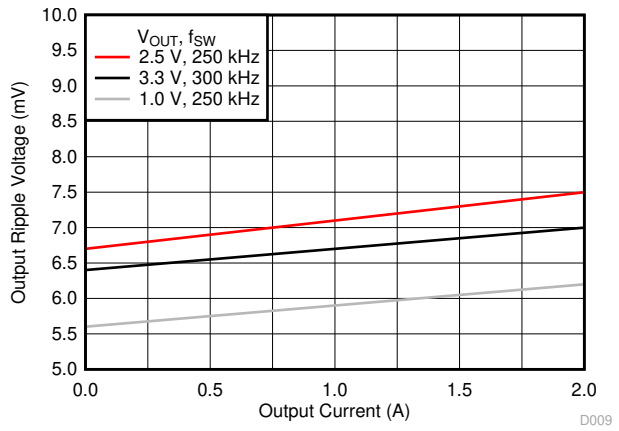
V_{IN} = 5 V

図 6-1. Efficiency vs Output Current



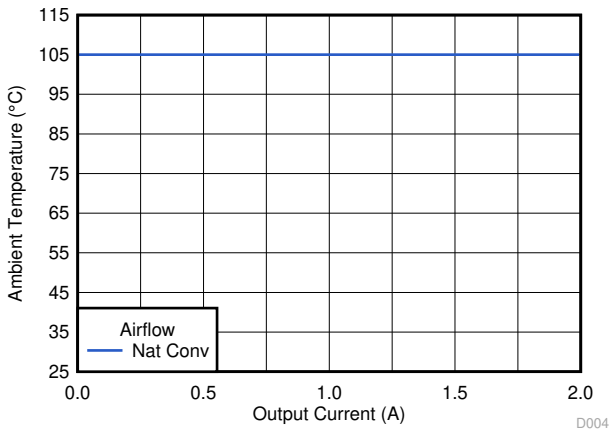
V_{IN} = 5 V

図 6-2. Power Dissipation vs Output Current



V_{IN} = 5 V C_{OUT} = 4 × 22 µF, 25 V, 1210 ceramic

図 6-3. Voltage Ripple vs Output Current



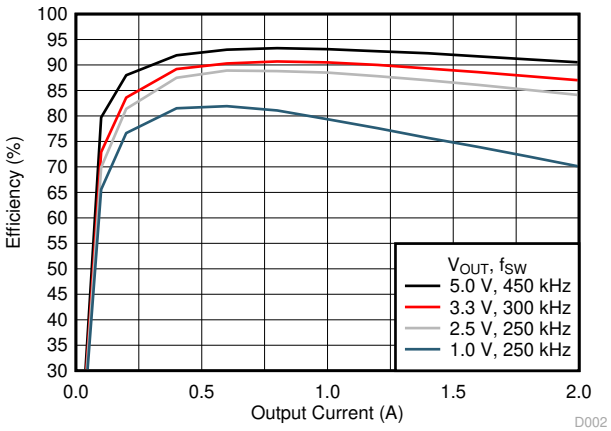
V_{IN} = 5 V All V_{OUT}

図 6-4. Safe Operating Area

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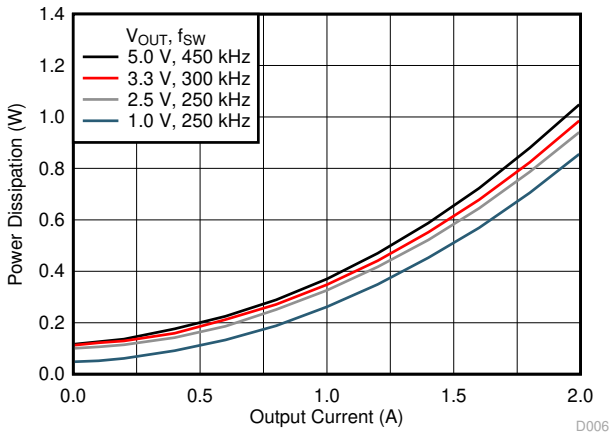
6.8 Typical Characteristics (V_{IN} = 12 V)

The typical characteristic data has been developed from actual products tested at 25°C. This data is considered typical for the device.



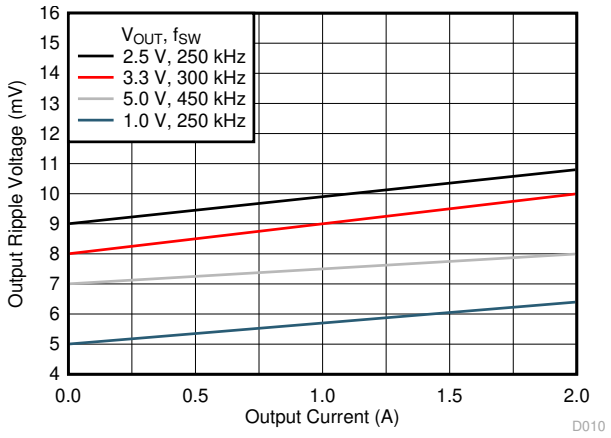
V_{IN} = 12 V

図 6-5. Efficiency vs Output Current



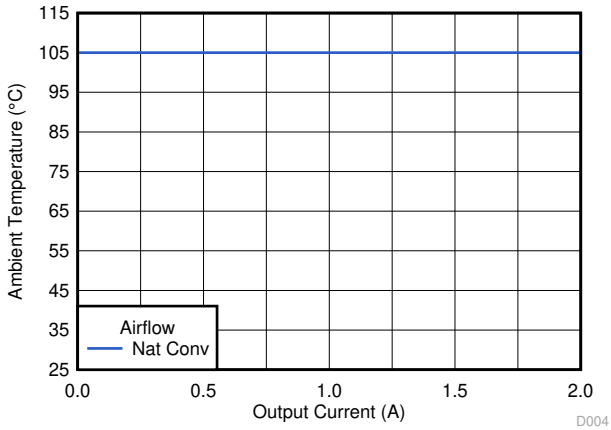
V_{IN} = 12 V

図 6-6. Power Dissipation vs Output Current



V_{IN} = 12 V C_{OUT} = 4 × 22 µF, 25 V, 1210 ceramic

図 6-7. Voltage Ripple vs Output Current



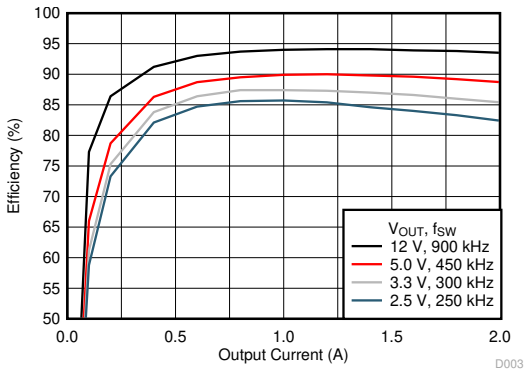
V_{IN} = 12 V V_{OUT} = 5 V f_{SW} = 450 kHz

図 6-8. Safe Operating Area

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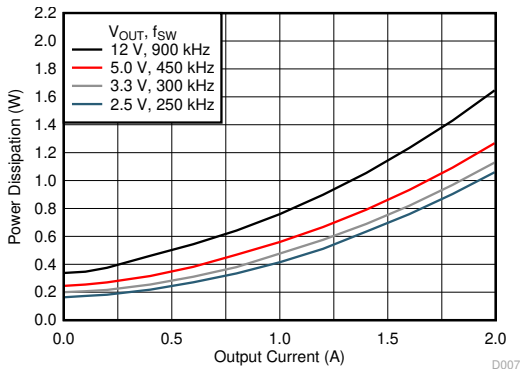
6.9 Typical Characteristics (V_{IN} = 24 V)

The typical characteristic data has been developed from actual products tested at 25°C. This data is considered typical for the device.



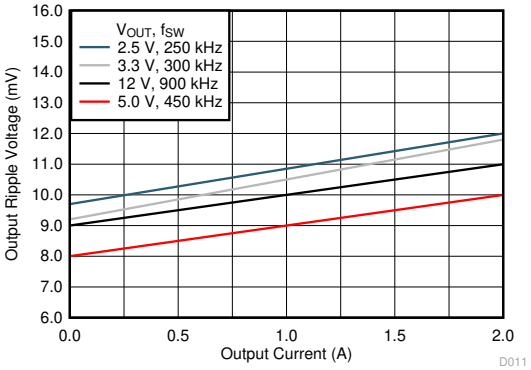
V_{IN} = 24 V

図 6-9. Efficiency vs Output Current



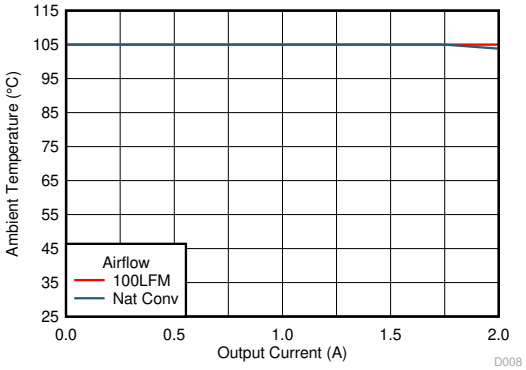
V_{IN} = 24 V

図 6-10. Power Dissipation vs Output Current



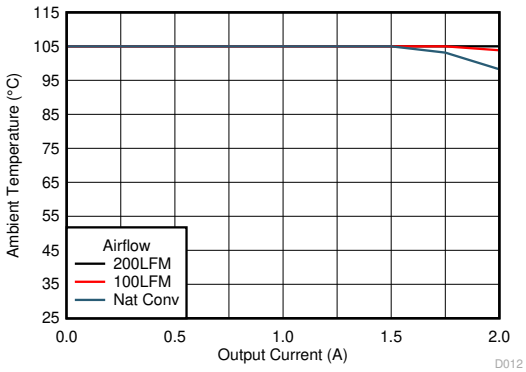
V_{IN} = 24 V C_{OUT} = 4 × 22 µF, 25 V, 1210 ceramic

図 6-11. Voltage Ripple vs Output Current



V_{IN} = 24 V V_{OUT} = 5 V f_{SW} = 450 kHz

図 6-12. Safe Operating Area



V_{IN} = 24 V V_{OUT} = 12 V f_{SW} = 900 kHz

図 6-13. Safe Operating Area

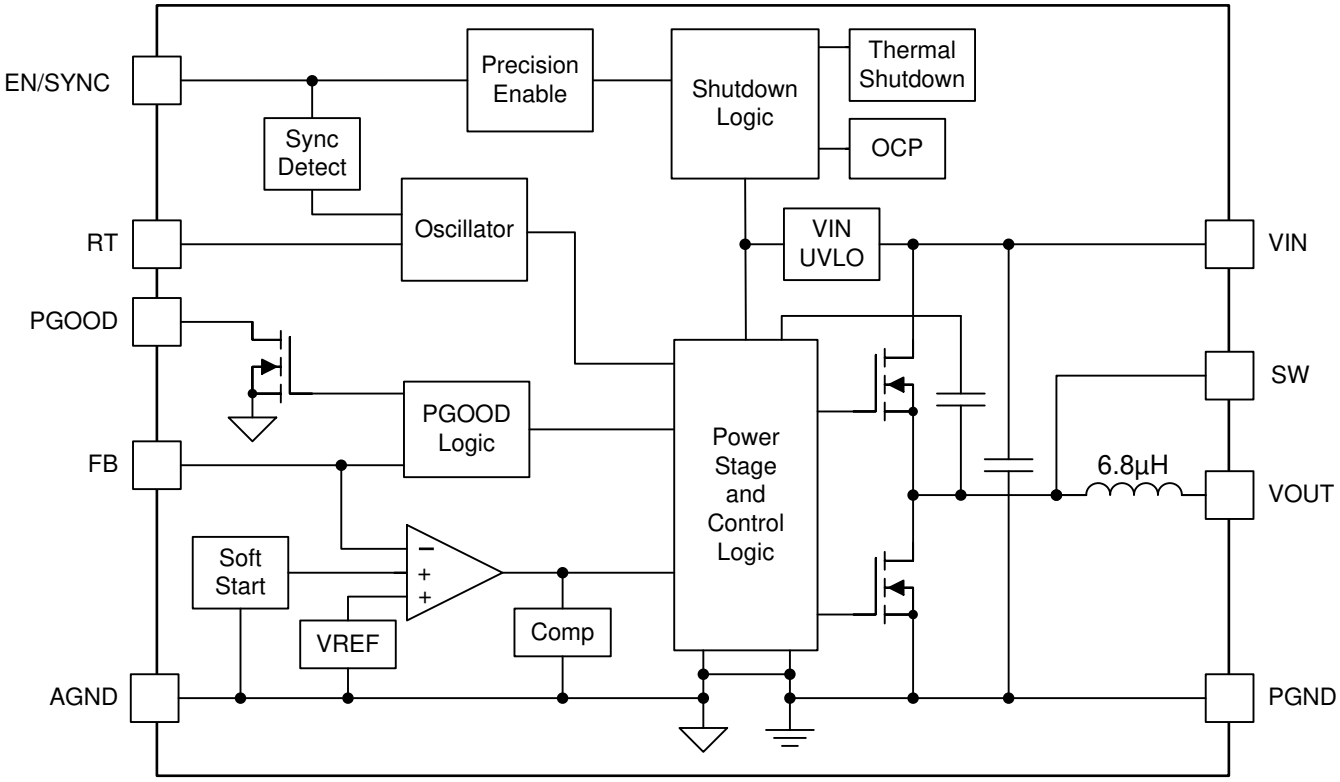
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7 Detailed Description

7.1 Overview

The LMZM33602 is a full-featured, 36-V input, 2-A, synchronous step-down converter with PWM, MOSFETs, shielded inductor, and control circuitry integrated into a low-profile, overmolded package. The device integration enables small designs, while providing the ability to adjust key parameters to meet specific design requirements. The LMZM33602 provides an output voltage range of 1 V to 18 V. An external resistor divider is used to adjust the output voltage to the desired value. The switching frequency can also be adjusted, by either an external resistor or a sync signal, which allows the LMZM33602 to accommodate a variety of input and output voltage conditions as well as optimize efficiency. The device provides accurate voltage regulation over a wide load range by using a precision internal voltage reference. Input undervoltage lockout is internally set at 3.6 V (typical), but can be adjusted upward using a resistor divider on the EN/SYNC pin of the device. The EN/SYNC pin can also be pulled low to put the device into standby mode to reduce input quiescent current. A power-good signal is provided to indicate when the output is within its nominal voltage range. Thermal shutdown and current limit features protect the device during an overload condition. An 18-pin, QFN package that includes exposed bottom pads provides a thermally enhanced solution for space-constrained applications.

7.2 Functional Block Diagram



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7.3 Feature Description

7.3.1 Adjusting the Output Voltage

A resistor divider connected to the FB pin (pin 16) programs the output voltage of the LMZM33602. The output voltage adjustment range is from 1 V to 18 V. 図 7-1 shows the feedback resistor connections for setting the output voltage. The recommended value of R_{FBB} is 10 kΩ. The value for R_{FBT} can be calculated using 式 1. Depending on the output voltage, a feedforward capacitor, C_{FF}, can be required for optimum transient performance. 表 7-1 lists the standard external R_{FBT} and C_{FF} values for several output voltages between 2.5 V and 18 V. 表 7-2 lists the values for output voltages below 2.5 V. Additionally, 表 7-1 and 表 7-2 include the recommended switching frequency (F_{SW}), the frequency setting resistor (R_{RT}), and the minimum and maximum output capacitance for each of the output voltages listed.

For designs with R_{FBB} other than 10 kΩ, adjust C_{FF} and R_{FBT} such that (C_{FF} × R_{FBT}) is unchanged and adjust R_{FBT} such that (R_{FBT} / R_{FBB}) is unchanged.

$$R_{FBT} = 10 \times (V_{OUT} - 1)(k\Omega) \quad (1)$$

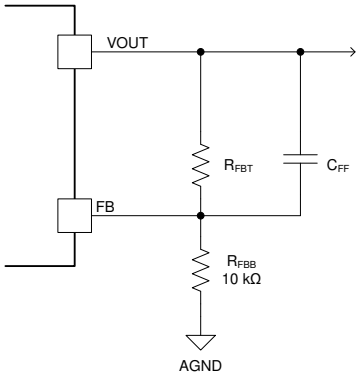


図 7-1. Setting the Output Voltage

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表 7-1. Required Component Values (V_{OUT} ≥ 2.5 V)

V_{OUT} (V)	R_{FBT} (kΩ)(3)	C_{FF} (pF)	f_{SW} (kHz)	R_{RT} (kΩ)	$C_{OUT(min)}$ (µF)(1)	$C_{OUT(max)}$ (µF)(2)
2.5	15.0	220	250	162	150	400
3.3	23.2	150	300	133	88	300
5	40.2	100	450	88.7	66	200
6	49.9	68	550	71.5	54	160
7.5	64.9	47	650	60.4	40	130
9	80.6	47	700	56.2	36	110
12	110	open	900	44.2	22	80
13.5	124	open	1000	39.2	22	75
15	140	open	1100	35.7	20	65
18	169	open	1200	33.2	16	55

(1) For output voltages ≥ 2.5 V, the minimum required output capactiance must be comprised of **ceramic** type and account for DC bias and temperature derating.
(2) The maximum output capactiance must include the required ceramic $C_{OUT(min)}$. Additional capacitance, may be ceramic type, low-ESR polymer type, or a combination of the two.
(3) R_{FBB} = 10.0 kΩ

表 7-2. Required Component Values (V_{OUT} < 2.5 V)

V_{OUT} (V)	R_{FBT} (kΩ)(1)	C_{FF} (pF)	F_{SW} (kHz)	R_{RT} (kΩ)	C_{OUT}
1 to 2.5	See 式 1	open	250	162	150-µF ceramic + 470-µF polymer

(1) R_{FBB} = 10 kΩ. For V_{OUT} = 1 V, R_{FBB}= open and R_{FBT} = 0 Ω.

7.3.2 Feedforward Capacitor, C_{FF}

The LMZM33602 is internally compensated to be stable over the operating frequency and output voltage range. However, depending on the output voltage, an additional feedforward capacitor can be required. TI recommends an external feedforward capacitor, C_{FF}, be placed in parallel with the top resistor divider, R_{FBT} for optimum transient performance. The value for C_{FF} can be calculated using Equation 2.

$$C_{FF} = \frac{1000}{4\pi\left(\frac{8.32}{V_{OUT} \times C_{OUT}}\right) \times R_{FBT}} (pF) \quad (2)$$

where

- C_{OUT} is the value after derating in µF
- R_{FBT} is in kΩ

Refer to 表 7-1 for the recommended C_{FF} value for several output voltages.

7.3.3 Voltage Dropout

Voltage dropout is the difference between the input voltage and output voltage that is required to maintain output voltage regulation while providing the rated output current.

To ensure the LMZM33602 maintains output voltage regulation at the recommended switching frequency, over the operating temperature range, the following requirements apply:

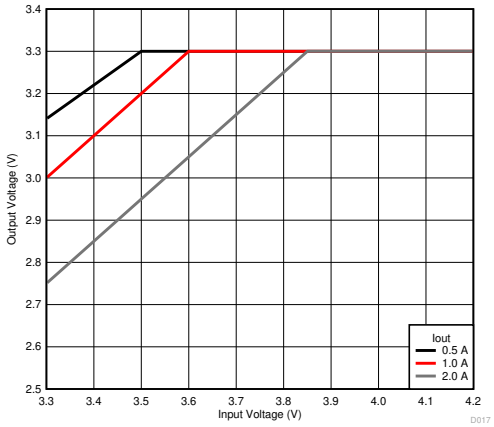
For output voltages ≤ 5 V, the minimum V_{IN} is 4 V or (V_{OUT} + 1.5 V), whichever is greater.

For output voltages > 5 V, the minimum V_{IN} is (1.3 × V_{OUT}).

However, if fixed switching frequency operation is not required, the LMZM33602 operates in a frequency foldback mode when the dropout voltage is less than the recommendations above. Frequency foldback reduces the switching frequency to allow the output voltage to maintain regulation as input voltage decreases. 図 7-2 through 図 7-7 show typical dropout voltage and frequency foldback curves for 3.3-V, 5-V, and 12-V outputs at T_A

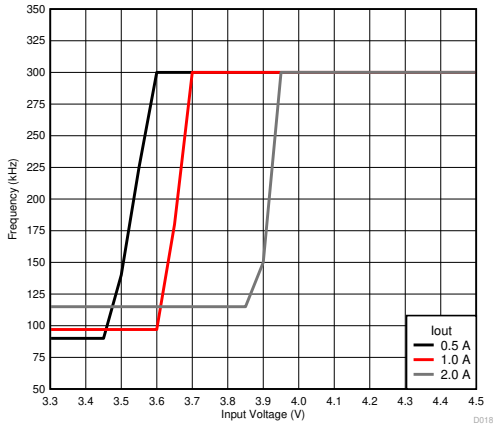
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= 25°C. (Note: As ambient temperature increases, dropout voltage and frequency foldback occur at higher input voltage.)



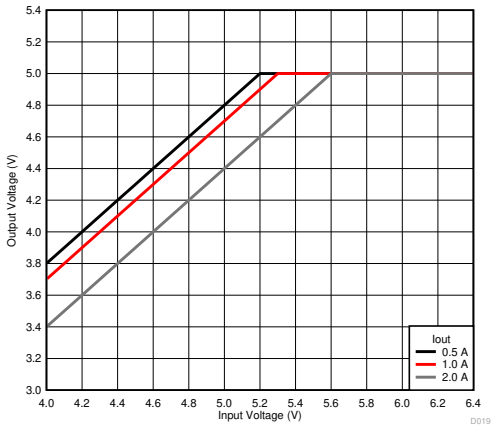
V_{OUT} = 3.3 V f_{SW} = 300 kHz

図 7-2. Voltage Dropout



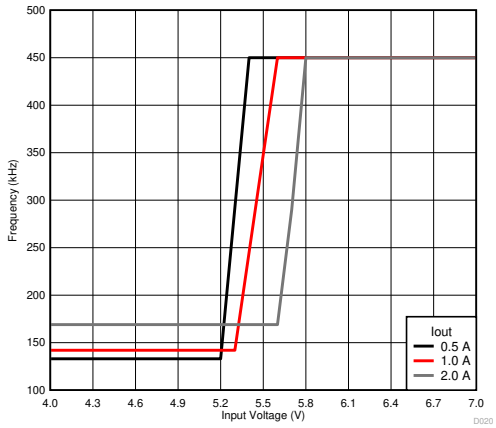
V_{OUT} = 3.3 V f_{SW} = 300 kHz

図 7-3. Frequency Foldback



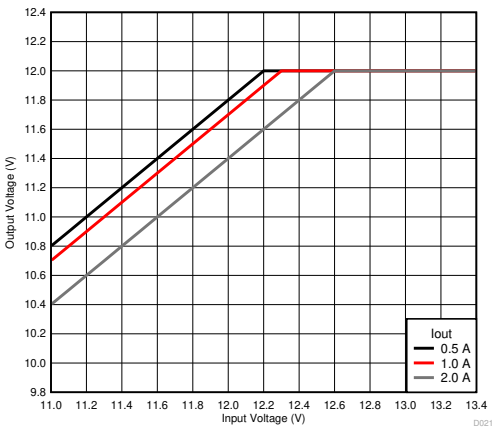
V_{OUT} = 5 V f_{SW} = 450 kHz

図 7-4. Voltage Dropout



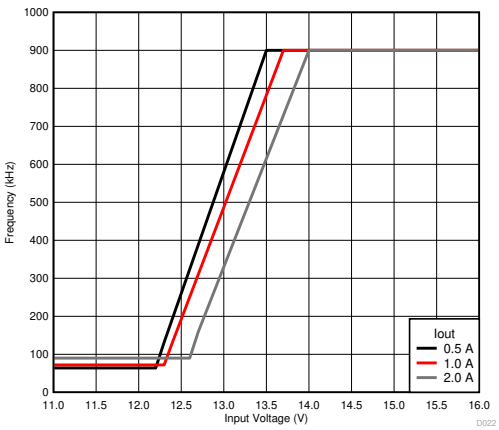
V_{OUT} = 5 V f_{SW} = 450 kHz

図 7-5. Frequency Foldback



V_{OUT} = 12 V f_{SW} = 900 kHz

図 7-6. Voltage Dropout



V_{OUT} = 12 V f_{SW} = 900 kHz

図 7-7. Frequency Foldback

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7.3.4 Switching Frequency (RT)

The switching frequency range of the LMZM33602 is 200 kHz to 1.2 MHz. The switching frequency can easily be set by connecting a resistor (R_{RT}) between the RT pin and AGND. Additionally, the RT pin can be left floating and the LMZM33602 will operate at 400 kHz default switching frequency. Use Equation 3 to calculate the R_{RT} value for a desired frequency or simply select from 表 7-3.

The switching frequency must be selected based on the output voltage setting of the device and the operating input voltage. See 表 7-3 for R_{RT} resistor values and the allowable output voltage range for a given switching frequency for three common input voltages.

$$R_{RT} = \left(\frac{40200}{f_{SW}\,(kHz)} \right) - 0.6\,(k\Omega) \tag{3}$$

表 7-3. Switching Frequency vs Output Voltage

SWITCHING FREQUENCY (kHz)	R_{RT} RESISTOR (kΩ)	V_{IN} = 5 V (±5%)		V_{IN} = 12 V (±5%)		V_{IN} = 24 V (±5%)	
		V_{OUT} RANGE (V)		V_{OUT} RANGE (V)		V_{OUT} RANGE (V)	
		MIN	MAX	MIN	MAX	MIN	MAX
200	200	1	3.4	1	5.5	1	6.2
250	158	1	3.5	1	6.2	1	10.6
300	133	1	3.5	1	6.8	1	10.6
350	113	1	3.5	1	7.4	1	10.7
400	100 or (RT pin open)	1	3.5	1	7.9	1	11.4
450	88.7	1	3.5	1	8.4	1.2	12.1
500	78.7	1	3.5	1	8.9	1.3	12.8
550	71.5	1	3.4	1	9.3	1.4	13.4
600	66.5	1	3.4	1	9.5	1.6	14.1
650	60.4	1	3.4	1	9.4	1.7	14.6
700	56.2	1	3.3	1	9.3	1.8	15.2
750	52.3	1	3.3	1	9.2	2.0	15.8
800	49.9	1	3.3	1	9.1	2.1	16.3
850	46.4	1	3.2	1.1	9.0	2.2	16.8
900	44.2	1	3.2	1.2	9.0	2.3	17.3
950	41.2	1	3.2	1.2	8.9	2.5	17.8
1000	39.2	1	3.1	1.3	8.8	2.6	18
1050	37.4	1	3.1	1.4	8.7	2.7	18
1100	35.7	1	3.1	1.4	8.6	2.9	18
1150	34.0	1	3	1.5	8.5	3	18
1200	33.2	1	3	1.6	8.5	3.1	18

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7.3.5 Synchronization (SYNC)

The LMZM33602 switching frequency can also be synchronized to an external clock from 200 kHz to 1.2 MHz. To implement the synchronization feature, couple an AC signal to the EN/SYNC pin (pin 2) with a peak-to-peak amplitude of at least 2.8 V, not to exceed 5.5 V. The minimum SYNC clock ON and OFF time must be longer than 100ns. The AC signal must be coupled through a small capacitor (1 nF) as shown in 図 7-8. R_{ENT} is required for this synchronization circuit, but R_{ENB} is not required if an external UVLO adjustment is not needed.

Before the external clock is present, or when a valid clock signal is removed, the device works in RT mode and the switching frequency is set by R_{RT} resistor. Select R_{RT} so that it sets the frequency close to the external synchronization frequency. When the external clock is present, the SYNC mode overrides the RT mode.

The synchronization frequency must be selected based on the output voltages of the devices being synchronized. 表 7-3 shows the allowable frequencies for a given range of output voltages. For the most efficient solution, always select the lowest allowable frequency.

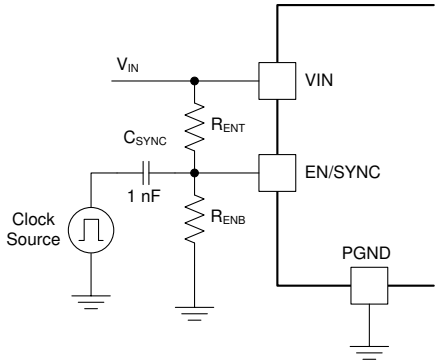


図 7-8. AC Coupled SYNC Signal

7.3.6 Input Capacitors

The LMZM33602 requires a minimum input capacitance of 9.4 µF (2 × 4.7 µF) of ceramic type. High-quality, ceramic-type X5R or X7R capacitors with sufficient voltage rating are recommended. TI recommends an additional 100 µF of non-ceramic capacitance for applications with transient load requirements. The voltage rating of input capacitors must be greater than the maximum input voltage.

表 7-4. Recommended Input Capacitors

VENDOR	SERIES	PART NUMBER	CAPACITOR CHARACTERISTICS		
			WORKING VOLTAGE (V)	CAPACITANCE (2) (µF)	ESR(1) (mΩ)
Murata	X7R	GRM32ER71H475KA88L	50	4.7	2
TDK	X5R	C3225X5R1H106K250AB	50	10	3
Murata	X7R	GRM32ER71H106KA12	50	10	2
TDK	X7R	C3225X7R1H106M250AB	50	10	3
Panasonic	ZA	EEHZA1H101P	50	100	28

(1) Maximum ESR @ 100 kHz, 25°C.
(2) Standard capacitance values

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7.3.7 Output Capacitors

The LMZM33602 minimum and maximum output capacitance listed in 表 7-1 and 表 7-2 represents the amount of *effective* capacitance. The effects of DC bias and temperature variation must be considered when using ceramic capacitance. For ceramic capacitors, the package size, voltage rating, and dielectric material will contribute to differences between the standard rated value and the actual effective value of the capacitance.

When adding additional capacitance, above $C_{OUT(min)}$, the capacitance can be ceramic type, low-ESR polymer type, or a combination of the two. See 表 7-5 for a preferred list of output capacitors by vendor.

表 7-5. Recommended Output Capacitors

VENDOR	SERIES	PART NUMBER(1)	CAPACITOR CHARACTERISTICS		
			WORKING VOLTAGE (V)	CAPACITANCE (3) (µF)	ESR(2) (mΩ)
Murata	X7R	GRM32ER71E226KE15L	25	22	2
TDK	X5R	C3225X5R0J476K	6.3	47	2
Murata	X5R	GRM32ER61C476K	16	47	3
TDK	X5R	C3225X5R0J107M	6.3	100	2
Murata	X5R	GRM32ER60J107M	6.3	100	2
Murata	X5R	GRM32ER61A107M	10	100	2
Kemet	X5R	C1210C107M4PAC7800	16	100	2
Panasonic	POSCAP	6TPE100MI	6.3	100	18
Panasonic	POSCAP	6TPE150MF	6.3	150	15
Panasonic	POSCAP	10TPF150ML	10	150	15
Panasonic	POSCAP	6TPF220M9L	6.3	220	9
Panasonic	POSCAP	6TPE220ML	6.3	220	12
Panasonic	POSCAP	4TPF330ML	4	330	12
Panasonic	POSCAP	6TPF330M9L	6.3	330	9
Panasonic	POSCAP	6TPE470MAZU	6.3	470	35

(1) **Capacitor Supplier Verification , RoHS, Lead-free and Material Details** Consult capacitor suppliers regarding availability, material composition, RoHS and lead-free status, and manufacturing process requirements for any capacitors identified in this table.
(2) Maximum ESR @ 100 kHz, 25°C.
(3) Standard capacitance values.

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7.3.8 Output On/Off Enable (EN)

The voltage on the EN/SYNC pin provides electrical ON/OFF control of the device. Once the EN pin voltage exceeds the threshold voltage, the device starts operation. If the EN pin voltage is pulled below the threshold voltage, the regulator stops switching and enters low quiescent current state.

The EN pin cannot be open circuit or floating. The simplest way to enable the operation of the LMZM33602 is to connect the EN pin to VIN directly as shown in 図 7-9. This allows self-start-up of the LMZM33602 when VIN is within the operation range.

If an application requires controlling the EN pin, an external logic signal can be used to drive EN/SYNC pin as shown in 図 7-10. Applications using an open drain/collector device to interface with this pin require a pullup resistor to a voltage above the enable threshold.

図 7-11 and 図 7-12 show typical turn-ON and turn-OFF waveforms using the enable control.

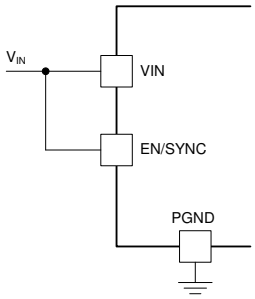


図 7-9. Enabling the Device

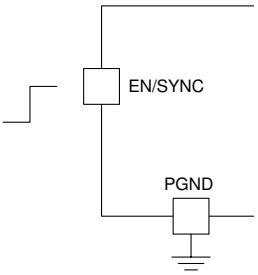


図 7-10. Typical Enable Control

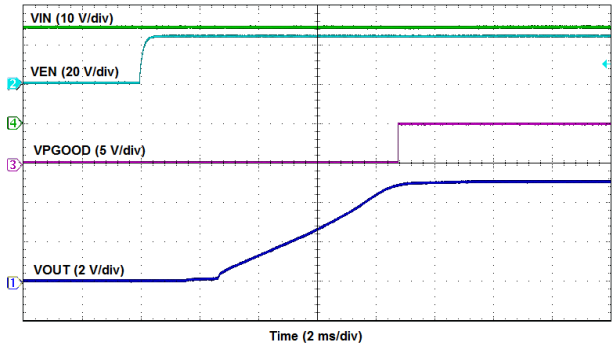


図 7-11. Enable Turn-ON

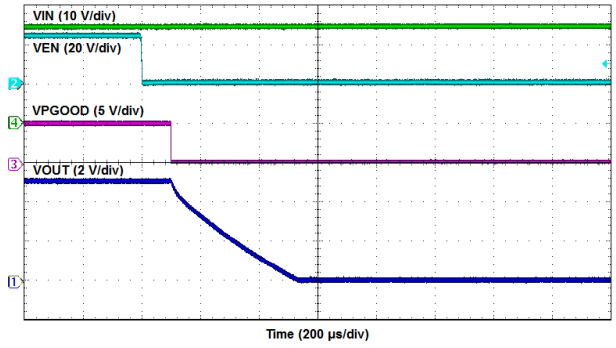


図 7-12. Enable Turn-OFF

7.3.9 Programmable Undervoltage Lockout (UVLO)

The LMZM33602 implements internal UVLO circuitry on the VIN pin. The device is disabled when the VIN pin voltage falls below the internal VIN UVLO threshold. The internal VIN UVLO rising threshold is 3.9 V (maximum) with a typical hysteresis of 300 mV.

If an application requires a higher UVLO threshold, a resistor divider can be placed on the EN/SYNC pin as shown in 図 7-13. 表 7-6 lists recommended resistor values for R_{ENT} and R_{ENB} to adjust the ULVO voltage.

To ensure proper start-up and reduce input current surges, the UVLO threshold must be set to at least (V_{OUT} + 1.5 V) for output voltages ≤ 5 V and at least (1.3 × V_{OUT}) for output voltages > 5 V. TI recommends to set the UVLO threshold to approximately 80% to 85% of the minimum expected input voltage.

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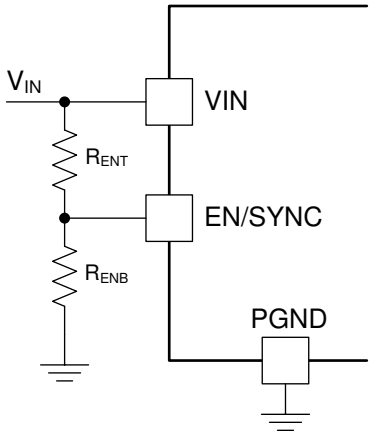


図 7-13. Adjustable UVLO

表 7-6. Resistor Values for Adjusting UVLO

VIN UVLO (V)	6.5	10	15	20	25	30
R_{ENT} (kΩ)	100	100	100	100	100	100
R_{ENB} (kΩ)	35.7	20.5	12.7	9.31	7.32	6.04

7.3.10 Power Good (PGOOD)

The LMZM33602 has a built-in power-good signal (PGOOD) which indicates whether the output voltage is within its regulation range. The PGOOD pin is an open-drain output that requires a pullup resistor to a nominal voltage source of 12 V or less. The maximum recommended PGOOD sink current is 1 mA. A typical pullup resistor value is between 10 kΩ and 100 kΩ.

Once the output voltage rises above 94% of the set voltage, the PGOOD pin rises to the pullup voltage level. The PGOOD pin is pulled low when the output voltage drops lower than 92.5% or rises higher than 107% of the nominal set voltage. See 図 7-14 for typical power-good thresholds.

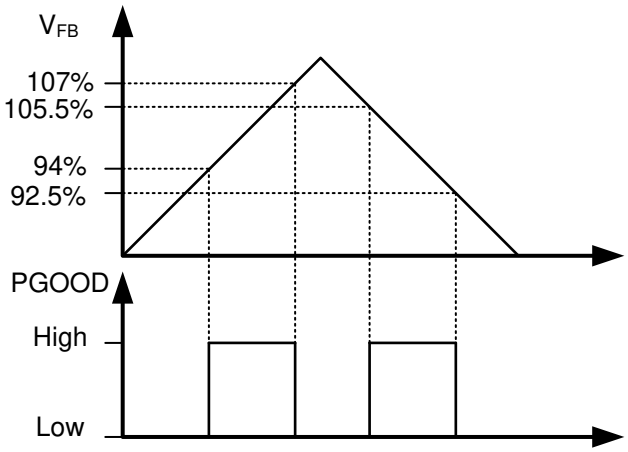


図 7-14. Power Good Flag

7.3.11 Overcurrent Protection (OCP)

The LMZM33602 is protected from overcurrent conditions. Hiccup mode is activated if a fault condition persists to prevent overheating. In hiccup mode, the regulator is shut down and kept off for 10 ms typical before the LMZM33602 tries to start again. If overcurrent or short-circuit fault condition still exist, hiccup repeats until the fault condition is removed. Hiccup mode reduces power dissipation under severe overcurrent conditions, and prevents overheating and potential damage to the device. Once the fault is removed, the module automatically recovers and returns to normal operation as shown in 図 7-16.

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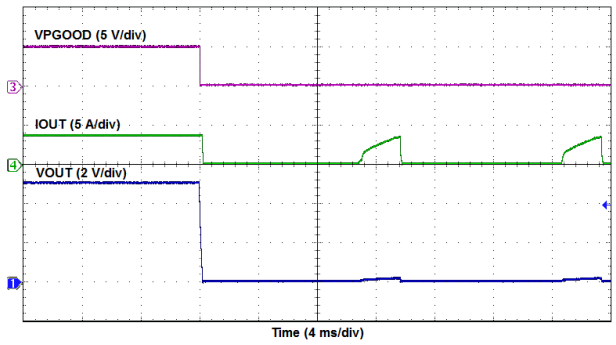


図 7-15. Overcurrent Limiting

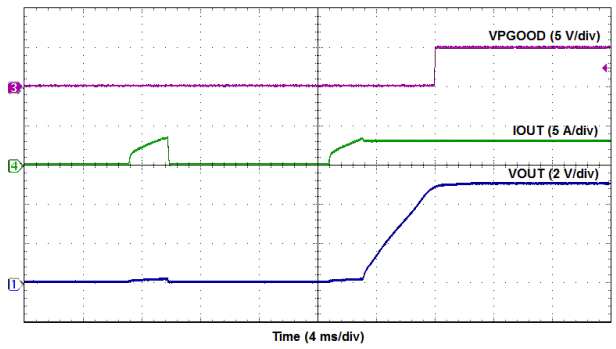


図 7-16. Removal of Overcurrent

7.3.12 Thermal Shutdown

The internal thermal shutdown circuitry forces the device to stop switching if the junction temperature exceeds 170°C typically. The device reinitiates the power up sequence when the junction temperature drops below 155°C typically.

7.4 Device Functional Modes

7.4.1 Active Mode

The LMZM33602 is in active mode when VIN is above the UVLO threshold and the EN/SYNC pin voltage is above the EN high threshold. The simplest way to enable the LMZM33602 is to connect the EN/SYNC pin to VIN. This allows self start-up of the LMZM33602 when the input voltage is in the operation range: 4 V to 36 V. In active mode, the LMZM33602 is in continuous conduction mode (CCM) with fixed switching frequency.

7.4.2 Shutdown Mode

The EN/SYNC pin provides electrical ON and OFF control for the LMZM33602. When the EN/SYNC pin voltage is below the EN low threshold, the device is in shutdown mode. In shutdown mode the standby current is 2 µA typical. The LMZM33602 also employs input UVLO protection. If VIN is below the UVLO level, the output of the regulator is turned off.

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8 Application and Implementation

Note

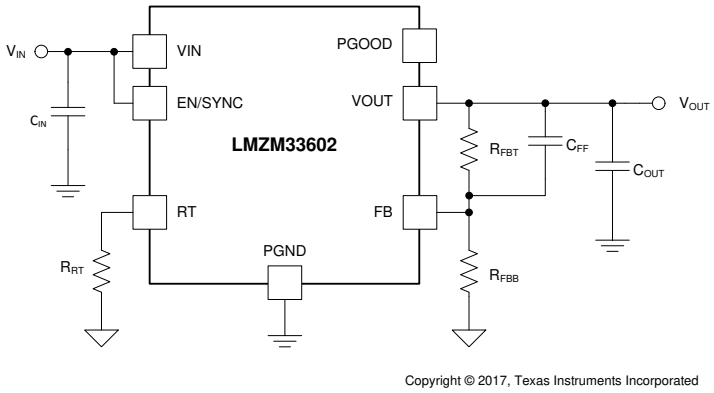
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8.1 Application Information

The LMZM33602 is a synchronous, step-down, DC-DC power module. It is used to convert a higher DC voltage to a lower DC voltage with a maximum output current of 2 A. The LMZM33602 can be configured in an inverting buck-boost (IBB) topology with the output voltage inverted or negative with respect to ground. For more details, see TI Application Report *Inverting Application for the LMZM33602/03*. The following design procedure can be used to select components for the LMZM33602. Alternately, the WEBENCH® software may be used to generate complete designs. When generating a design, the WEBENCH® software utilizes an iterative design procedure and accesses comprehensive databases of components. See www.ti.com for more details.

8.2 Typical Application

The LMZM33602 only requires a few external components to convert from a wide input voltage supply range to a wide range of output voltages. 図 8-1 shows a basic LMZM33602 schematic with only the minimum required components.



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図 8-1. LMZM33602 Typical Schematic

8.2.1 Design Requirements

For this design example, use the parameters listed in 表 8-1 as the input parameters and follow the design procedures in *セクション 8.2.2*.

表 8-1. Design Example Parameters

DESIGN PARAMETER	VALUE
Input voltage V_{IN}	24 V typical
Output voltage V_{OUT}	5 V
Output current rating	2 A
Operating frequency	450 kHz

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8.2.2 Detailed Design Procedure

8.2.2.1 Custom Design With WEBENCH® Tools

Click here to create a custom design using the LMZM33602 device with the WEBENCH® Power Designer.

1. Start by entering the input voltage (V_{IN}), output voltage (V_{OUT}), and output current (I_{OUT}) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance
- Run thermal simulations to understand board thermal performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

8.2.2.2 Output Voltage Setpoint

The output voltage of the LMZM33602 device is externally adjustable using a resistor divider. The recommended value of R_{FBB} is 10.0 kΩ. The value for R_{FBT} can be selected from 表 7-6 or calculated using Equation 4:

$$R_{FBT} = 10 \times (V_{OUT} - 1)(k\Omega) \quad (4)$$

For the desired output voltage of 5.0 V, the formula yields a value of 40 kΩ. Choose the closest available value of 40.2 kΩ for R_{FBT}.

8.2.2.3 Feedforward Capacitor (C_{FF})

TI recommends placing an external feedforward capacitor, C_{FF} in parallel with the top resistor divider, R_{FBT} for optimum transient performance. The value for C_{FF} can be calculated using Equation 2 or selected from 表 7-1. The recommended C_{FF} value for 5-V application is 100 pF.

8.2.2.4 Setting the Switching Frequency

The recommended switching frequency for a 5-V application is 450 kHz. To set the swtiching frequency to 450 kHz, a 88.7-kΩ R_{RT} resistor is required.

8.2.2.5 Input Capacitors

The LMZM33602 requires a minimum input capacitance of 10 µF (or 2 × 4.7 µF) ceramic type. High-quality ceramic type X5R or X7R capacitors with sufficient voltage rating are recommended. An additional 100 µF of non-ceramic capacitance is recommended for applications with transient load requirements. The voltage rating of input capacitors must be greater than the maximum input voltage.

For this design, a 10-µF, 50-V, ceramic capacitor was selected.

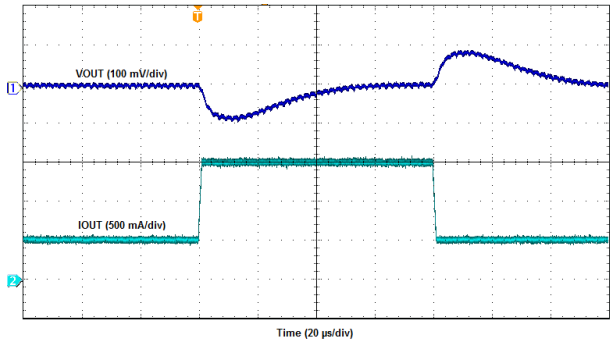
8.2.2.6 Output Capacitor Selection

The LMZM33602 requires a minimum amount of output capacitance for proper operation. The minimum amount of required output varies depending on the output voltage. See 表 7-1 for the required output capacitance.

For this design example, four 22-µF, 25-V ceramic capacitors are used.

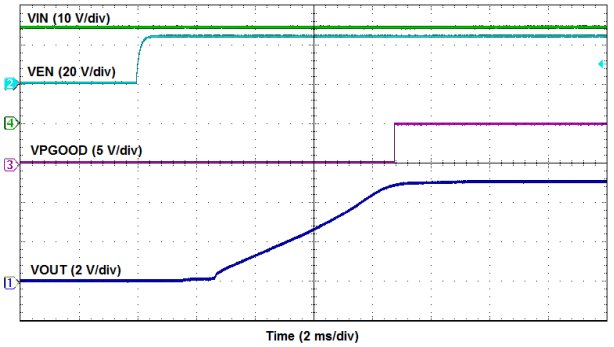
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8.2.2.7 Application Curves



V_{IN} = 24 V V_{OUT} = 5 V I_{OUT} = 0.5 A to 1 A
C_{OUT} = 4 × 22 µF Slew rate: 1 A/µs

図 8-2. Transient Response



V_{IN} = 24 V V_{OUT} = 5 V C_{OUT} = 4 × 22 µF

図 8-3. Enable Turn-on

Power Supply Recommendations

The LMZM33602 is designed to operate from an input voltage supply range between 4 V and 36 V. This input supply must be well regulated and able to withstand maximum input current and maintain a stable voltage. The resistance of the input supply rail must be low enough that an input current transient does not cause a high enough drop at the LMZM33602 supply voltage that can cause a false UVLO fault triggering and system reset.

If the input supply is located more than a few inches from the LMZM33602 additional bulk capacitance may be required in addition to the ceramic bypass capacitors. The typical amount of bulk capacitance is a 100-µF electrolytic capacitor.

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Layout

The performance of any switching power supply depends as much upon the layout of the PCB as the component selection. The following guidelines will help users design a PCB with the best power conversion performance, optimal thermal performance, and minimized generation of unwanted EMI.

9.1 Layout Guidelines

To achieve optimal electrical and thermal performance, an optimized PCB layout is required. 図 9-1 through 図 9-4 show a typical PCB layout. Some considerations for an optimized layout are:

- Use large copper areas for power planes (VIN, VOUT, and PGND) to minimize conduction loss and thermal stress.
- **Connect PGND pins 14 and 15 directly to pin 18 using thick copper traces.**
- Connect the SW pins together using a small copper island under the device for thermal relief.
- Place ceramic input and output capacitors close to the device pins to minimize high frequency noise.
- Locate additional output capacitors between the ceramic capacitor and the load.
- Keep AGND and PGND separate from one another.
- Place R_{FBT}, R_{FBB}, R_{RT}, and C_{FF} as close as possible to their respective pins.
- Use multiple vias to connect the power planes to internal layers.

9.2 Layout Examples

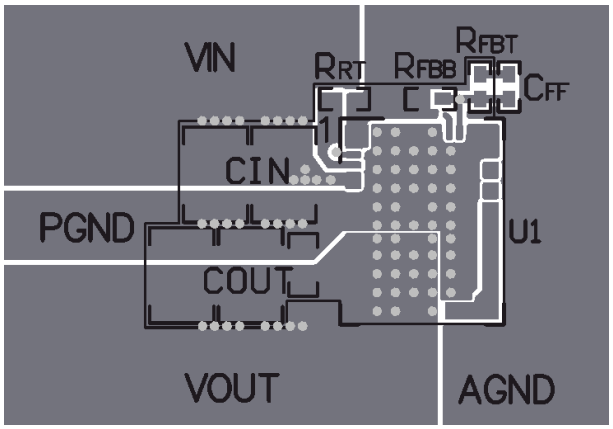


図 9-1. Typical Top-Layer Layout

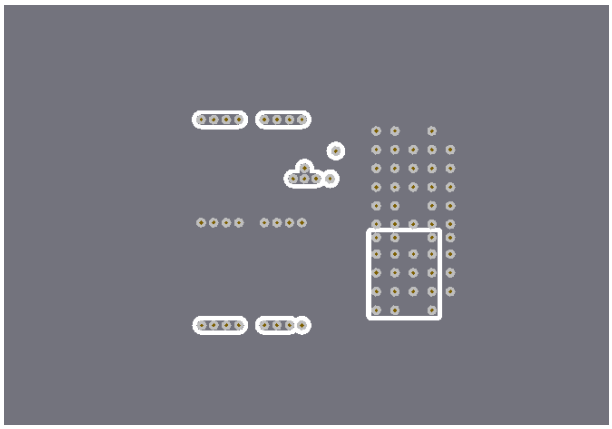


図 9-2. Typical Layer-2 Layout

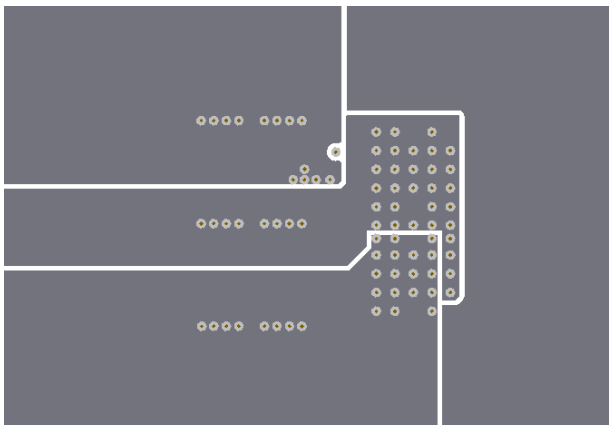


図 9-3. Typical Layer 3 Layout

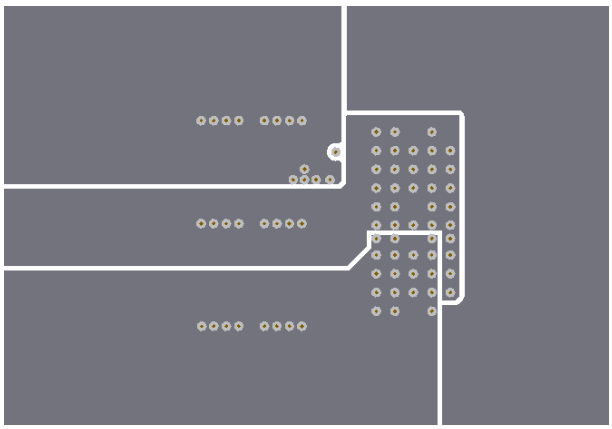


図 9-4. Typical Bottom-Layer Layout

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9.3 Theta JA versus PCB Area

The amount of PCB copper effects the thermal performance of the device. 図 9-5 shows the effects of copper area on the junction-to-ambient thermal resistance ($R_{\theta JA}$) of the LMZM33602. The junction-to-ambient thermal resistance is plotted for a 2-layer PCB and a 4-layer PCB with PCB area from 16 cm^2 to 49 cm^2.

To determine the required copper area for an application:

1. Determine the maximum power dissipation of the device in the application by referencing the power dissipation graphs in *セクション 6.7* to *セクション 6.9*.
2. Calculate the maximum θ_{JA} using Equation 5 and the maximum ambient temperature of the application.

$$\theta_{JA} = \frac{(125^{\circ}C - T_{A(max)})}{P_{D(max)}} \ (^{\circ}C/W) \tag{5}$$

3. Reference 図 9-5 to determine the minimum required PCB area for the application conditions.

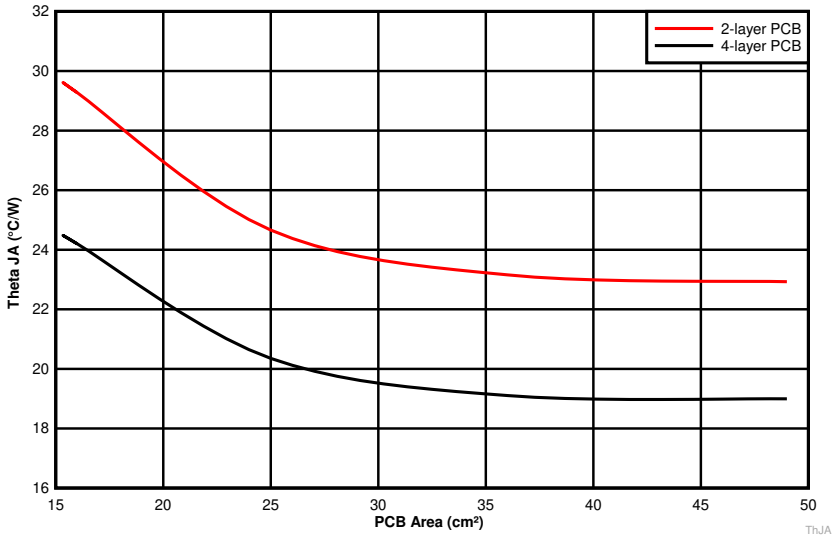


図 9-5. θ_{JA} vs PCB Area

9.4 EMI

The LMZM33602 is compliant with EN55011 Class B radiated emissions. 図 9-6, 図 9-7, and 図 9-8 show typical examples of radiated emissions plots for the LMZM33602. The graphs include the plots of the antenna in the horizontal and vertical positions.

9.4.1 EMI Plots

EMI plots were measured using the standard LMZM33602EVM with no input filter.

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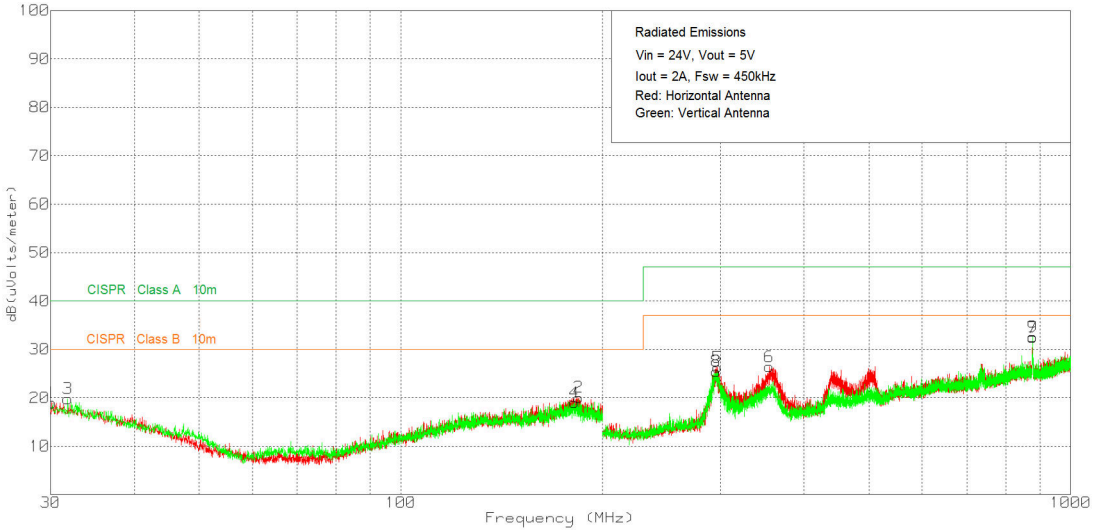


図 9-6. Radiated Emissions 24-V Input, 5-V Output, 2-A Load (EN55011 Class B)

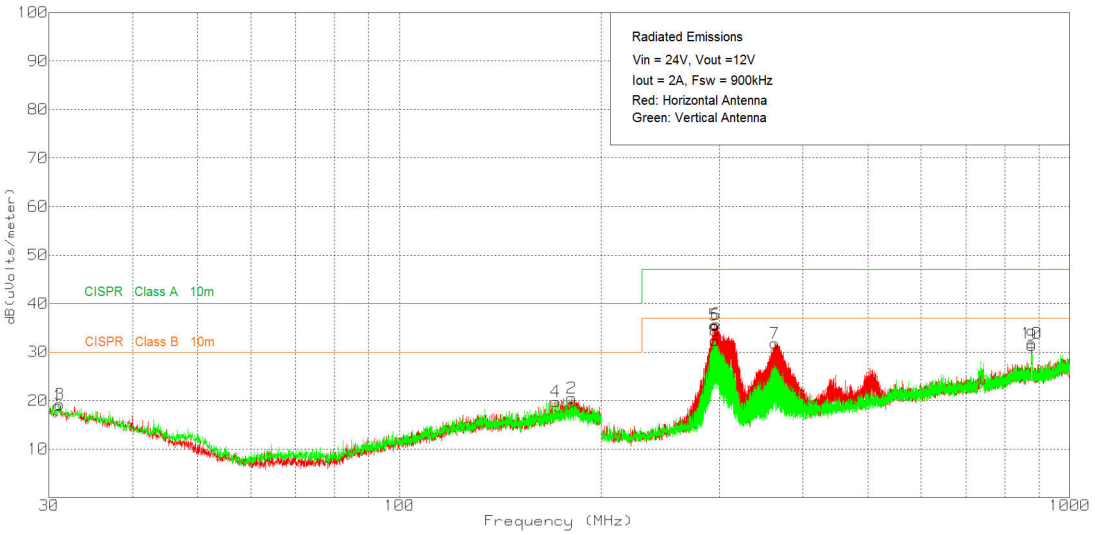


図 9-7. Radiated Emissions 24-V Input, 12-V Output, 2-A Load (EN55011 Class B)

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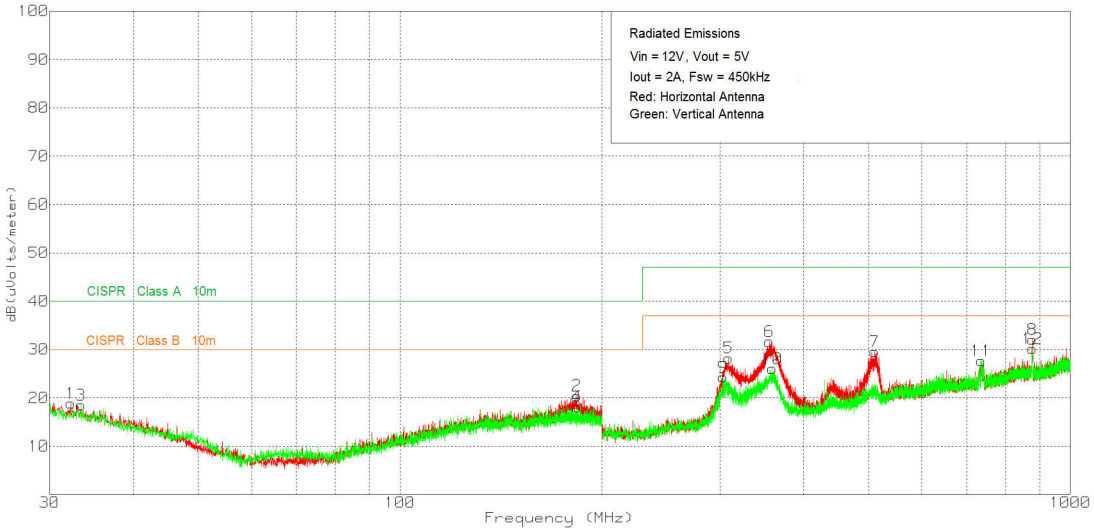


図 9-8. Radiated Emissions 12-V Input, 5-V Output, 2-A Load (EN55011 Class B)

9.5 Package Specifications

LMZM33602		VALUE	UNIT
Weight		0.74	grams
Flammability	Meets UL 94 V-O		
MTBF Calculated Reliability	Per Bellcore TR-332, 50% stress, T_A = 40°C, ground benign	98.0	MHrs

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9 Device and Documentation Support

9.1 Device Support

9.1.1 Development Support

9.1.1.1 Custom Design With WEBENCH® Tools

Click here to create a custom design using the LMZM33602 device with the WEBENCH® Power Designer.

1. Start by entering the input voltage (V_{IN}), output voltage (V_{OUT}), and output current (I_{OUT}) requirements.
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The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

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- Run thermal simulations to understand board thermal performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

9.2 Documentation Support

9.2.1 Related Documentation

For related documentation see the following:

TI Application Report *Inverting Application for the LMZM33602/03*

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9.6 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.7 用語集

TI 用語集　　この用語集には、用語や略語の一覧および定義が記載されています。

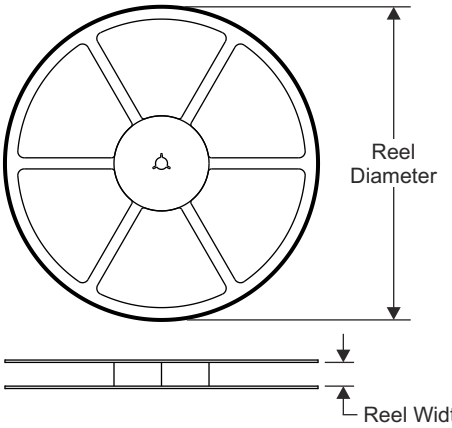
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Mechanical, Packaging, and Orderable Information

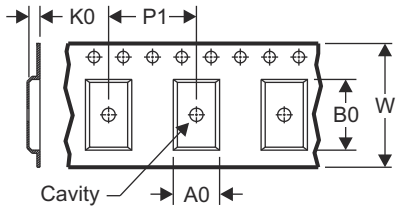
The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

10.1 Tape and Reel Information

REEL DIMENSIONS

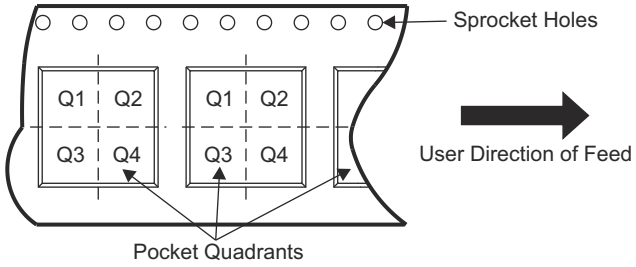


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

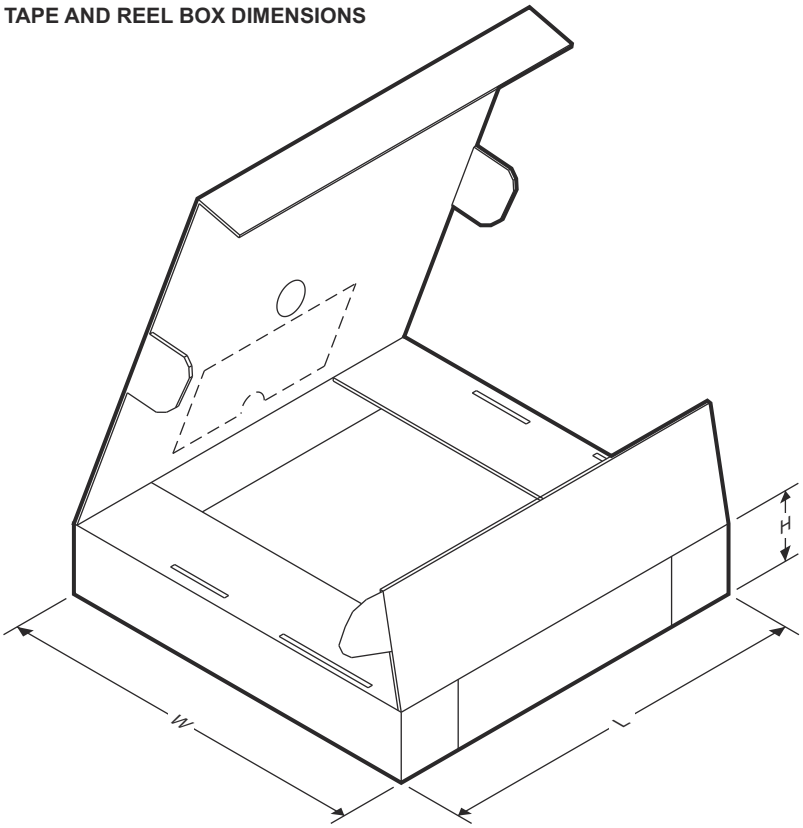
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMZM33602RLRR	B3QFN	RLR	18	500	330.0	24.4	7.35	9.35	4.35	12.0	24.0	Q1

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TAPE AND REEL BOX DIMENSIONS



Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMZM33602RLRR	B3QFN	RLR	18	500	383.0	353.0	58.0

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LMZM33602RLRR	Active	Production	B3QFN (RLR) | 18	500 | LARGE T&R	Yes	NIPDAU	Level-3-250C-168 HR	-40 to 105	LMZM33602
LMZM33602RLRR.A	Active	Production	B3QFN (RLR) | 18	500 | LARGE T&R	Yes	NIPDAU	Level-3-250C-168 HR	-40 to 105	LMZM33602
LMZM33602RLRRG4	Active	Production	B3QFN (RLR) | 18	500 | LARGE T&R	Yes	NIPDAU	Level-3-250C-168 HR	-40 to 105	LMZM33602
LMZM33602RLRRG4.A	Active	Production	B3QFN (RLR) | 18	500 | LARGE T&R	Yes	NIPDAU	Level-3-250C-168 HR	-40 to 105	LMZM33602
LMZM33602RLRRG4.B	Active	Production	B3QFN (RLR) | 18	500 | LARGE T&R	Yes	NIPDAU	Level-3-250C-168 HR	-40 to 105	LMZM33602

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

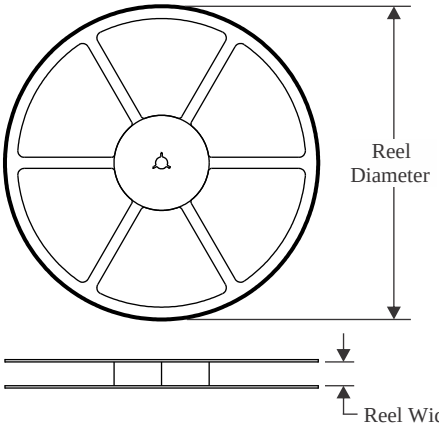
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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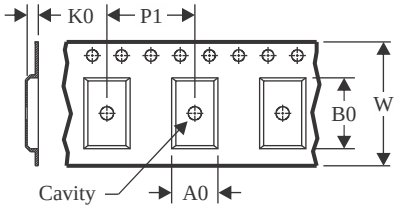
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TAPE AND REEL INFORMATION

REEL DIMENSIONS

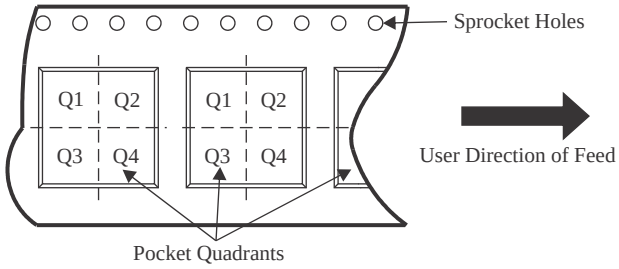


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

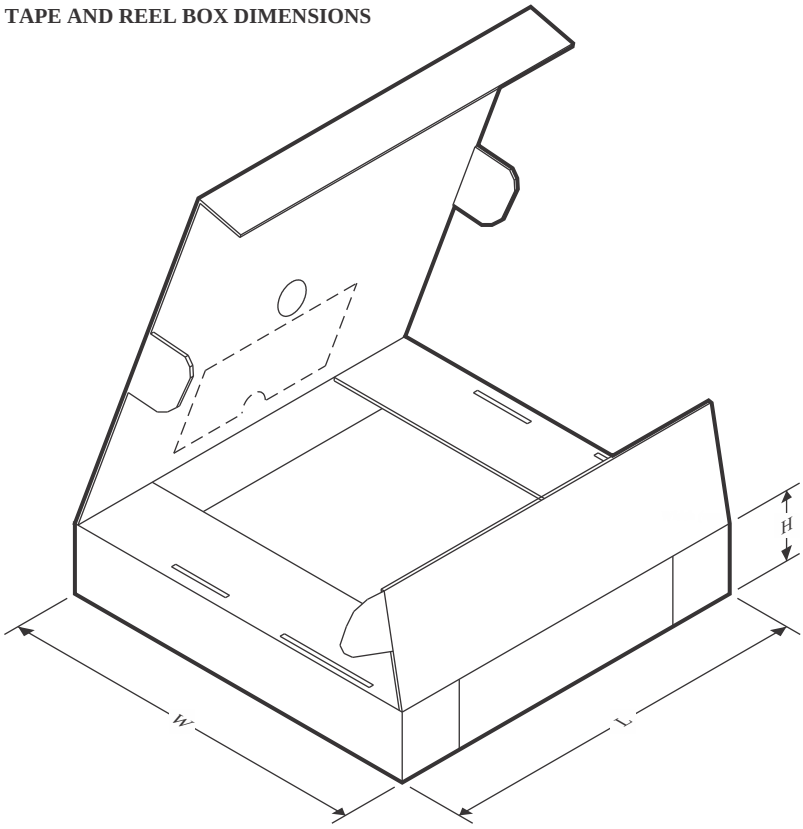
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMZM33602RLRR	B3QFN	RLR	18	500	330.0	24.4	7.35	9.35	4.35	12.0	24.0	Q1
LMZM33602RLRRG4	B3QFN	RLR	18	500	330.0	24.4	7.35	9.35	4.35	12.0	24.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

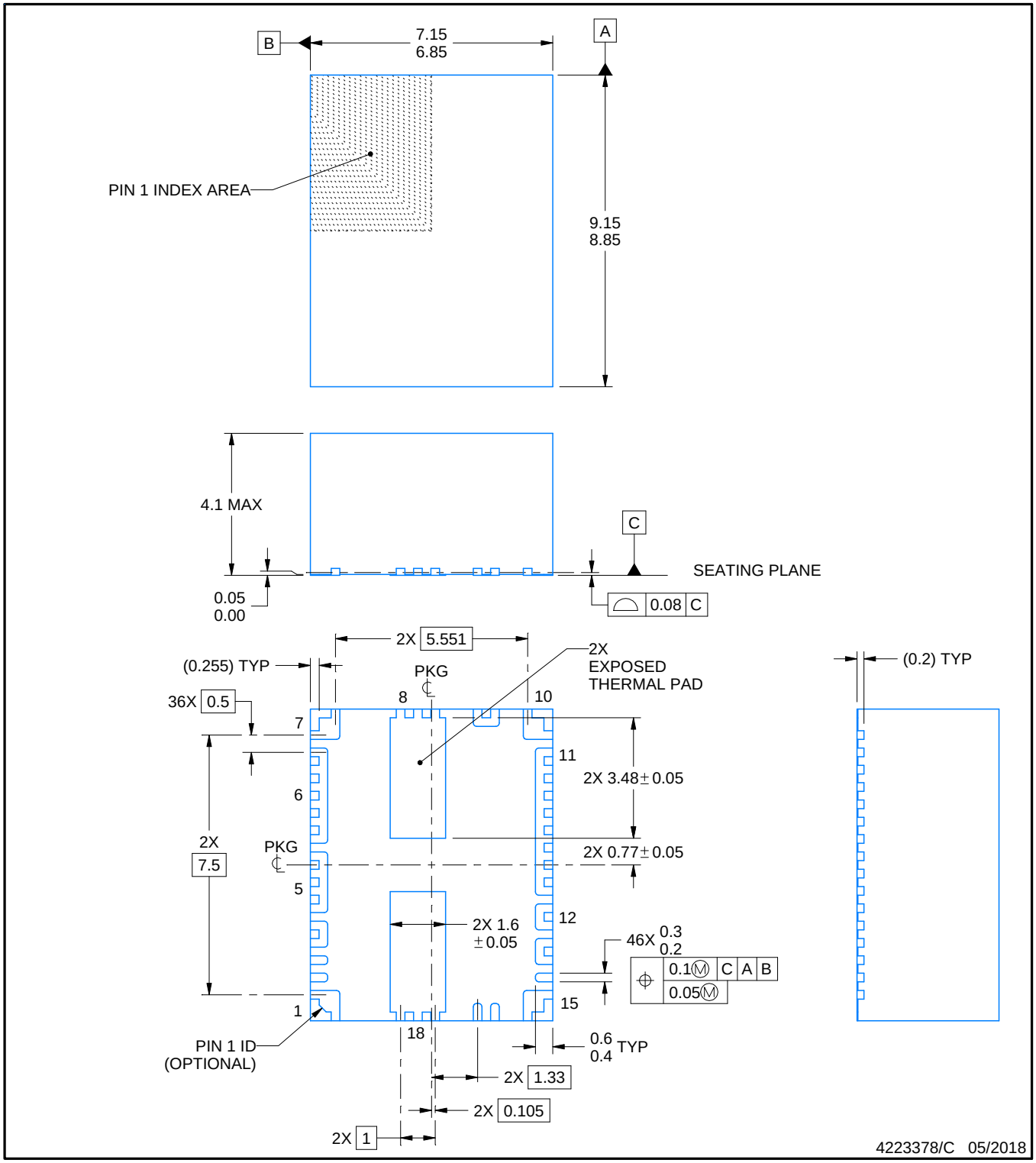
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMZM33602RLRR	B3QFN	RLR	18	500	383.0	353.0	58.0
LMZM33602RLRRG4	B3QFN	RLR	18	500	383.0	353.0	58.0

RLR0018A

PACKAGE OUTLINE

B3QFN - 4.1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES:

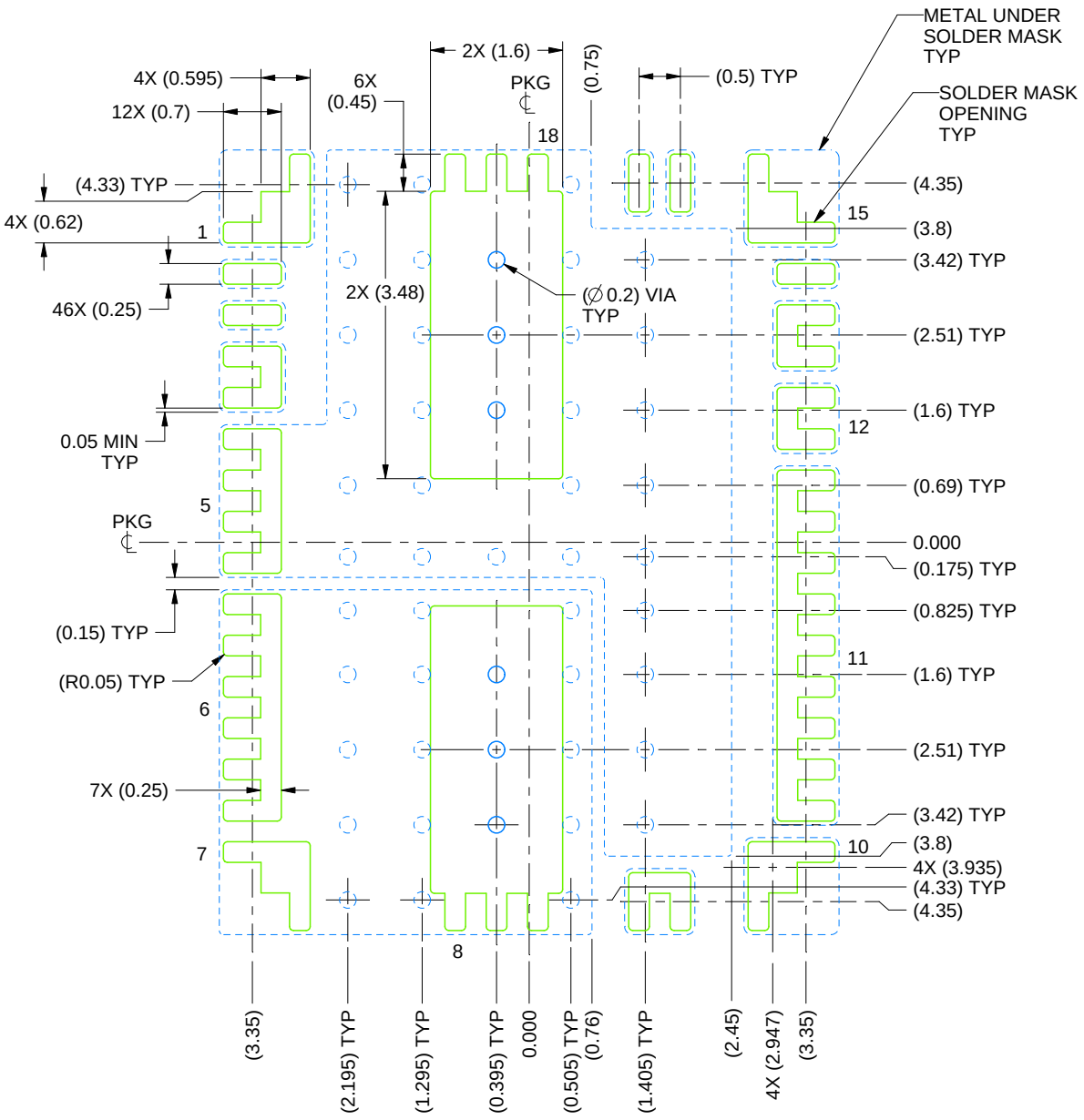
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pads must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

RLR0018A

B3QFN - 4.1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

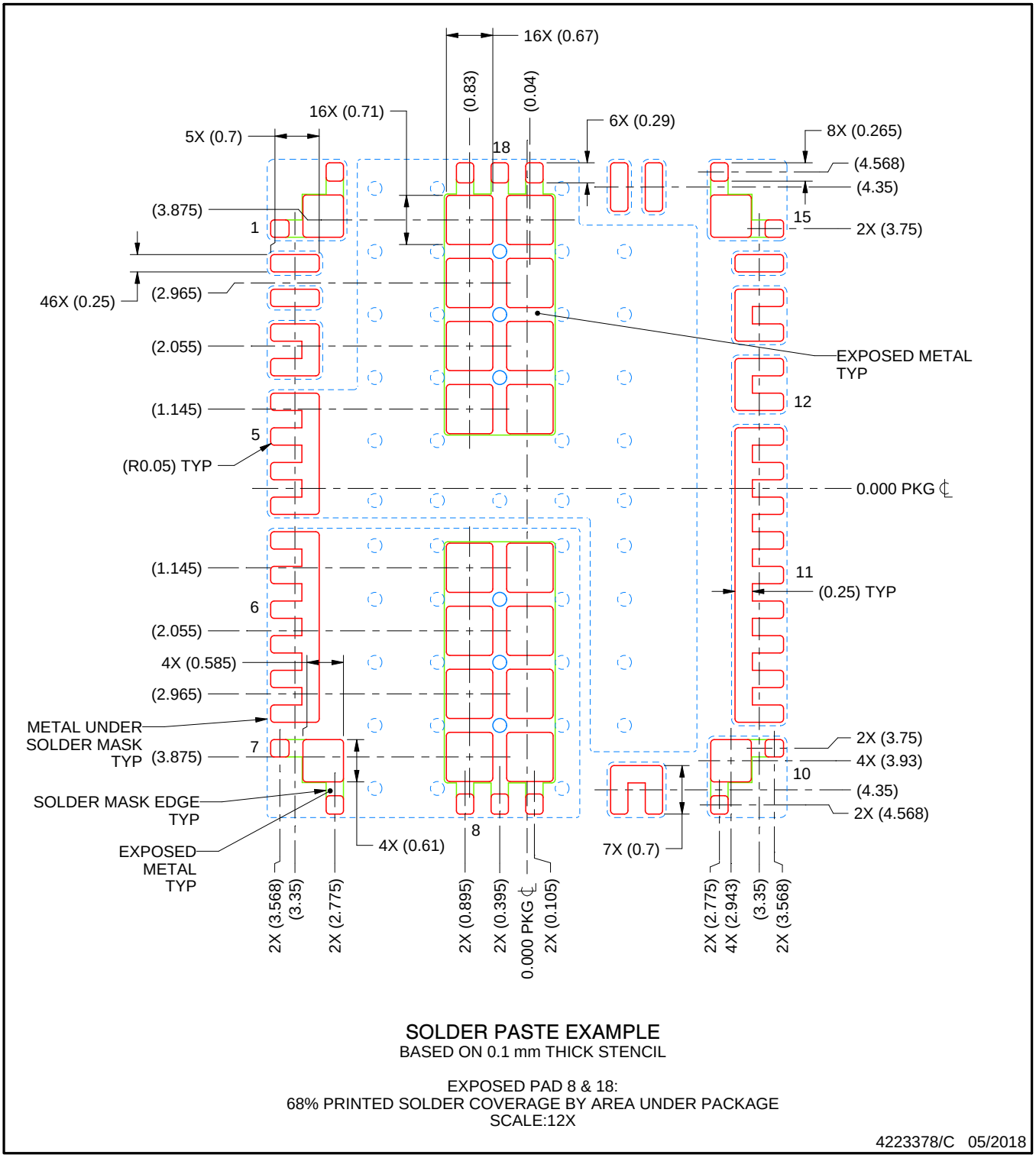


LAND PATTERN EXAMPLE
SOLDER MASK DEFINED
SCALE: 12X

4223378/C 05/2018

NOTES: (continued)

4. This package designed to be soldered to a thermal pads on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL

EXPOSED PAD 8 & 18:
68% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:12X

4223378/C 05/2018

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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