LP2954/LP2954A 5V/可変型マイクロパワーLDO

1 特長

- 5V出力で全動作温度範囲にわたって精度1.2%(Aグレード)
- 1.23V～29Vの可変出力電圧のバージョンが利用可能(LP2954IMおよびLP2954AIM)
- 出力電流250mAを保証
- 非常に低い静止電流
- 低ドロップアウト電圧
- バッテリ逆極性保護
- 非常に優れたラインおよび負荷のレギュレーション
- 非常に低い温度ドリフト係数
- 電流および熱の制限
- LM2940およびLM340とピン互換(5Vバージョンのみ)
- 可変出力バージョンには、出力ドロップを警告するERRORフラグとロジック制御シャットダウン機能が付加

2 アプリケーション

- 高効率のリニア・レギュレータ
- 低ドロップアウトのバッテリ駆動レギュレータ

3 概要

LP2954は5Vのマイクロパワー LDOで、静止電流が非常に低く(1mA負荷時に標準値90μA)、ドロップアウト電圧も非常に低い(軽負荷時に標準値60mV、250mA負荷電流時に470mV)製品です。

ドロップアウト時にも静止電流はわずかしか増大しないため(標準値120μA)、バッテリ駆動時間が延長されます。

5V固定出力電圧のLP2954は、3ピンTO-220およびDDPAK/TO-263パッケージで利用できます。可変出力のLP2954は、8ピンのスモール・アウトラインSOICパッケージで供給されます。可変出力バージョンは抵抗回路も備えており、ピン・ストラップにより1.23V～29Vの任意の電圧に出力を設定できます。

INピンにバッテリの逆極性保護を実装しています。

優れたラインおよび負荷のレギュレーション(標準値0.04%)と、非常に低い出力温度ドリフト係数から、LP2954は低消費電力の基準電圧に適しています。

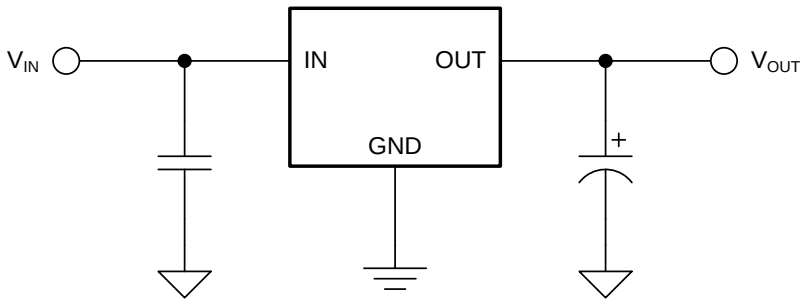
室温だけでなく、動作温度範囲の全体にわたって出力精度が保証されています。

製品情報(1)

型番	パッケージ	本体サイズ(公称)
LP2954	SOIC (8)	4.90mm×3.91mm
	DDPAK/TO-263 (3)	10.18mm×8.41mm
	TO-220 (3)	14.986mm×10.16mm

(1) 提供されているすべてのパッケージについては、巻末の注文情報を参照してください。

概略回路図



英語版のTI製品についての情報を翻訳したこの資料は、製品の概要を確認する目的で便宜的に提供しているものです。該当する正式な英語版の最新情報は、www.ti.comで閲覧でき、その内容が常に優先されます。TIでは翻訳の正確性および妥当性につきましては一切保証いたしません。実際の設計などの前には、必ず最新版の英語版をご参照くださいますようお願いいたします。

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4 改訂履歴

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Revision D (March 2013) から **Revision E** に変更 **Page**

- 「電圧レギュレータ」から「LDO」へ 変更 ... 1
- 「*デバイス情報*」および「*ピン構成および機能*」セクション、「*ESD定格*」表、「*熱に関する情報*」セクション、「*機能説明*」セクション、「*デバイスの機能モード*」セクション、「*アプリケーションと実装*」セクション、「*電源に関する推奨事項*」セクション、「*レイアウト*」セクション、「*デバイスおよびドキュメントのサポート*」セクション、「*メカニカル、パッケージ、および注文情報*」セクション、およびTI Designs用の上端のナビゲーションアイコンを 追加 ... 1
- Changed $R_{\theta JA}$ value for DDPAK/TO-263 from "73°C/W" to "44.3°C/W"; TO-220 from "60°C/W" to "80.3°C/W"; SOIC from "160°C/W" to "105.0°C/W". These values were in former FN 3 to *Abs Max* table ... 4
- Added *Power Dissipation* ... 15
- Added *Estimating Junction Temperature* ... 15

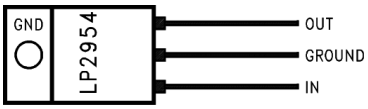
Revision C (March 2013) から **Revision D** に変更 **Page**

- Changed layout of National Semiconductor data sheet to TI format ... 18

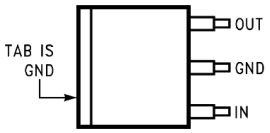
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5 Pin Configuration and Functions

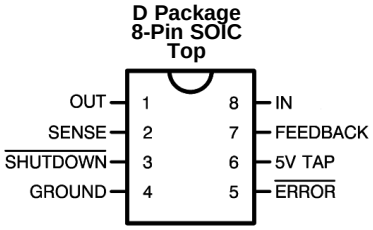
NDE Package
3-Pin TO-220
Front View



KTT Package
3-Pin DDPAK/TO-263
Front View



D Package
8-Pin SOIC
Top



Pin Functions

PIN				I/O	DESCRIPTION
NAME	NDE	KTT	D		
$\overline{\text{ERROR}}$	—	—	5	O	Error output
FEEDBACK	—	—	7	I	Voltage feedback input
IN	1	1	8	I	Unregulated input voltage
GND	2	2	4	—	Ground
OUT	3	3	1	O	Regulated output voltage. This pin requires an output capacitor to maintain stability. See *Detailed Design Procedure* for output capacitor details
SENSE	—	—	2	I	Output voltage sense
$\overline{\text{SHUTDOWN}}$	—	—	3	I	Disable device
5V TAP	—	—	6	O	Internal resistor divider

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)(2)

	MIN	MAX	UNIT
Input supply voltage	–20	30	V
Power dissipation(1)	Internally Limited		
Storage temperature, T_{stg}	–65	150	°C

(1) At elevated temperatures, device power dissipation must be derated based on package thermal resistance and heat sink values (if a heat sink is used). If power dissipation causes the junction temperature to exceed specified limits, the device goes into thermal shutdown.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/Distributors for availability and specifications.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	NOM	MAX	UNIT
Operating junction temperature	–40		125	°C

6.4 Thermal Information

THERMAL METRIC(1)		LP2954, LP2954A			UNIT
		KTT (DDPAK/TO-263)	NDE (TO-220)	D (SOIC)	
		3 PINS	3 PINS	8 PINS	
$R_{\theta JA}$(2)	Junction-to-ambient thermal resistance, High-K	44.3	80.3(3)	105.0	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	44.8	38.6	47.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	23.8	73.1	45.8	°C/W
ψ_{JT}	Junction-to-top characterization parameter	10.6	13.5	6.2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	22.7	73.1	45.2	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	1.0	0.9	—	°C/W

(1) For more information about traditional and new thermal metrics, see *Semiconductor and IC Package Thermal Metrics*.
(2) Thermal resistance value $R_{\theta JA}$ is based on the EIA/JEDEC High-K printed circuit board defined by *JESD51-7 - High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages.*
(3) The TO-220 (NDE) package is vertically mounted in center of JEDEC High-K test board (JESD 51-7) with no additional heat sink. This is a through-hole package; this is NOT a surface mount package.

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6.5 Electrical Characteristics

Limits are specified by production testing or correlation techniques using standard Statistical Quality Control (SQC) methods. Unless otherwise noted: T_J = 25°C, V_{IN} = 6 V, I_L = 1 mA, C_L = 2.2 µF

PARAMETER		TEST CONDITIONS	LP2954AI			LP2954I			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V_O	Output voltage(1)		4.975	5	5.025	4.95	5	5.05	V
		−40°C to 125°C	4.94		5.06	4.9		5.1	
		1 mA ≤ I_L ≤ 250 mA		5			5		
		1 mA ≤ I_L ≤ 250 mA −40°C to 125°C	4.93		5.07	4.88		5.12	
$\Delta V_O/\Delta T$	Output voltage temperature coefficient	See(2), –40°C ≤ T_J ≤ 125°C		20	100		20	150	ppm/°C
$\Delta V_O/V_O$	Line regulation	V_{IN} = 6 V to 30 V		0.03%	0.1%		0.03%	0.2%	
		V_{IN} = 6 V to 30 V –40°C ≤ T_J ≤ 125°C			0.2%			0.3%	
$\Delta V_O/V_O$	Load regulation	I_L = 1 to 250 mA I_L = 0.1 to 1 mA(3)		0.04%	0.16%		0.04%	0.2%	
		I_L = 1 to 250 mA I_L = 0.1 to 1 mA –40°C ≤ T_J ≤ 125°C			0.2%			0.3%	
$V_{IN} – V_O$	Dropout voltage(4)	I_L = 1 mA		60	100		60	100	mV
		I_L = 1 mA –40°C ≤ T_J ≤ 125°C			150			150	
		I_L = 50 mA		240	300		240	300	
		I_L = 50 mA, –40°C ≤ T_J ≤ 125°C			420			420	
		I_L = 100 mA		310	400		310	400	
		I_L = 100 mA –40°C ≤ T_J ≤ 125°C			520			520	
		I_L = 250 mA		470	600		470	600	
		I_L = 250 mA –40°C ≤ T_J ≤ 125°C			800			800	
I_{GND}	Ground pin current(5)	I_L = 1 mA		90	150		90	150	µA
		I_L = 1 mA –40°C ≤ T_J ≤ 125°C			180			180	
		I_L = 50 mA		1.1	2		1.1	2	mA
		I_L = 50 mA –40°C ≤ T_J ≤ 125°C			2.5			2.5	
		I_L = 100 mA		4.5	6		4.5	6	
		I_L = 100 mA –40°C ≤ T_J ≤ 125°C			8			8	
		I_L = 250 mA		21	28		21	28	
		I_L = 250 mA –40°C ≤ T_J ≤ 125°C			33			33	
I_{GND}	Ground pin current at dropout(5)	V_{IN} = 4.5 V		120	170		120	170	µA
		V_{IN} = 4.5 V –40°C ≤ T_J ≤ 125°C			210			210	

(1) When used in dual-supply systems where the regulator load is returned to a negative supply, the output voltage must be diode-clamped to ground.
(2) Output voltage temperature coefficient is defined as the worst-case voltage change divided by the total temperature range.
(3) Regulation is measured at constant junction temperature using low duty cycle pulse testing. Parts are tested separately for load regulation in the load ranges 0.1 mA to 1 mA and 1 mAto 250 mA. Changes in output voltage due to heating effects are covered by the thermal regulation specification.
(4) Dropout voltage is defined as the input-to-output differential at which the output voltage drops 100 mV below the value measured with a 1-V differential.
(5) GND pin current is the regulator quiescent current. The total current drawn from the source is the sum of the load current plus the GND pin current.

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Electrical Characteristics (continued)

Limits are specified by production testing or correlation techniques using standard Statistical Quality Control (SQC) methods. Unless otherwise noted: T_J = 25°C, V_{IN} = 6 V, I_L = 1 mA, C_L = 2.2 µF

PARAMETER		TEST CONDITIONS	LP2954AI			LP2954I			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
I_{LIMIT}	Current limit	V_O = 0 V		380	500		380	500	mA
		V_O = 0 V –40°C ≤ T_J ≤ 125°C			530			530	
$\Delta V_O/\Delta P_D$	Thermal regulation	See(6)		0.05	0.2		0.05	0.2	%/W
e_n	Output noise 10 Hz to 100 kHz	I_L = 100 mA, C_L = 2.2 µF		400			400		μV_{RMS}
		I_L = 100 mA, C_L = 33 µF		260			260		
		I_L = 100 mA, C_L = 33 µF(7)		80			80		
ADDITIONAL SPECIFICATIONS FOR THE ADJUSTABLE DEVICE (LP2954AIM and LP2954IM)									
V_{REF}	Reference voltage	See(8)	1.215	1.23	1.245	1.205	1.23	1.255	V
		See(8) –40°C ≤ T_J ≤ 125°C	1.205		1.255	1.19		1.27	
$\Delta V_{REF}/V_{REF}$	Reference voltage line regulation	V_{IN}= 2.5 V to $V_{O(NOM)}$ + 1 V		0.03%	0.1%		0.03%	0.2%	
		V_{IN}= 2.5 V to $V_{O(NOM)}$ +1 V to 30 V(9)(8)–40°C ≤ T_J ≤ 125°C			0.2%			0.4%	
$\Delta V_{REF}/\Delta T$	Reference voltage temperature coefficient	See(2) –40°C ≤ T_J ≤ 125°C		20					ppm/°C
$I_{B(FB)}$	Feedback pin bias current			20	40		20	40	nA
		–40°C ≤ T_J ≤ 125°C			60			60	
I_{GND}	Ground pin current at shutdown(5)	$V_{\overline{SHUTDOWN}}$ ≤ 1.1 V		105	140		105	140	µA
$I_{O(SINK)}$	Output OFF pulldown current	See(10)	30			30			mA
		See(10) –40°C ≤ T_J ≤ 125°C	20			20			
DROPOUT DETECTION COMPARATOR									
I_{OH}	Output HIGH leakage current	V_{OH} = 30 V		0.01	1		0.01	1	µA
		V_{OH} = 30 V, –40°C ≤ T_J ≤ 125°C			2			2	
V_{OL}	Output LOW voltage	V_{IN} = $V_{O(NOM)}$ − 0.5 V $I_{O(COMP)}$ = 400 µA –40°C ≤ T_J ≤ 125°C		150	250		150	250	mV
					400			400	
$V_{THR(MAX)}$	Upper threshold voltage	See(11)	–80	–60	–35	–80	–60	–35	mV
		See(11) –40°C ≤ T_J ≤ 125°C	–95		–25	–95		–25	
$V_{THR(MIN)}$	Lower threshold voltage	See(11)	–110	–85	–55	–110	–85	–55	mV
		See(11) –40°C ≤ T_J ≤ 125°C	–160		–40	–160		–40	
HYST	Hysteresis	See(11)		15			15		mV

(6) Thermal regulation is defined as the change in output voltage at a time T after a change in power dissipation is applied, excluding load or line regulation effects. Specifications are for 200-mA load pulse at V_{IN} = 20 V (3-W pulse) for T = 10 ms.
(7) Connect a 0.1-µF capacitor from the OUT pin to the FEEDBACK pin.
(8) $V_{REF} \le V_{OUT} \le (V_{IN} - 1\ V)$, 2.3 V ≤ V_{IN} ≤ 30 V, 100 µA ≤ I_L ≤ 250 mA.
(9) Two separate tests are performed, one covering V_{IN} = 2.5 V to $V_{O(NOM)}$ + 1 V and the other test for V_{IN} = 2.5 V to $V_{O(NOM)}$ + 1 V to 30 V.
(10) $V_{\overline{SHUTDOWN}}$ ≤ 1.1 V, V_{OUT} = $V_{O(NOM)}$.
(11) Comparator thresholds are expressed in terms of a voltage differential at the FEEDBACK pin below the nominal reference voltage measured at V_{IN} = $V_{O(NOM)}$ + 1 V. To express these thresholds in terms of output voltage change, multiply by the error amplifier gain, which is V_{OUT}/V_{REF} = (R1 + R2) / R2.

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Electrical Characteristics (continued)

Limits are specified by production testing or correlation techniques using standard Statistical Quality Control (SQC) methods. Unless otherwise noted: T_J = 25°C, V_{IN} = 6 V, I_L = 1 mA, C_L = 2.2 µF

PARAMETER		TEST CONDITIONS	LP2954AI			LP2954I			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
SHUTDOWN INPUT									
V_{OS}	Input offset voltage	(Referred to V_{REF})	−7.5	±3	7.5	−7.5	±3	7.5	mV
		(Referred to V_{REF}), –40°C ≤ T_J ≤ 125°C	–10		10	–10		10	
HYST	Hysteresis			6			6		mV
I_B	Input bias current	$V_{IN(\overline{SHUTDOWN})}$ = 0 V to 5 V	–30	10	30	–30	10	30	nA
		$V_{IN(\overline{SHUTDOWN})}$ = 0 V to 5 V, –40°C ≤ T_J ≤ 125°C	–50		50	–50		50	

6.6 Typical Characteristics

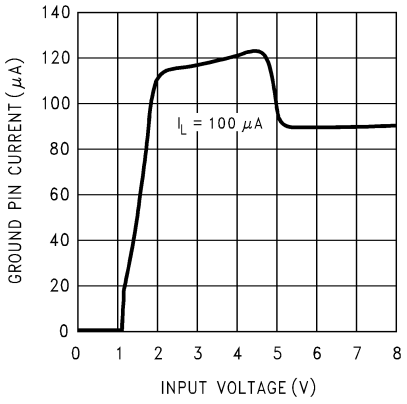


Figure 1. Quiescent Current

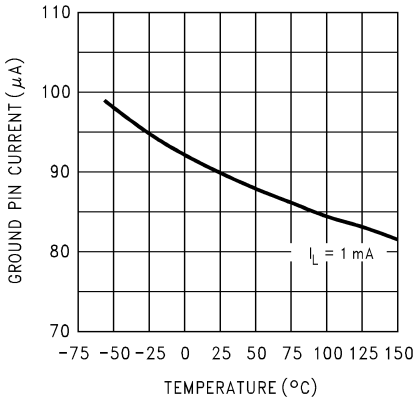


Figure 2. Quiescent Current

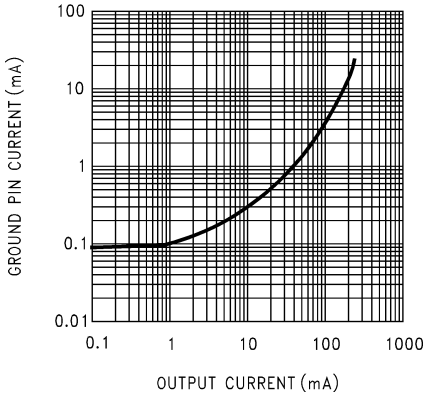


Figure 3. Ground Pin Current vs Load

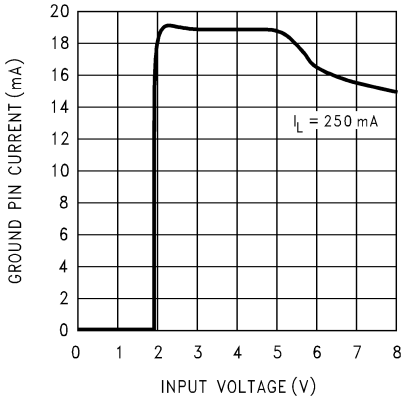


Figure 4. Ground Pin Current

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Typical Characteristics (continued)

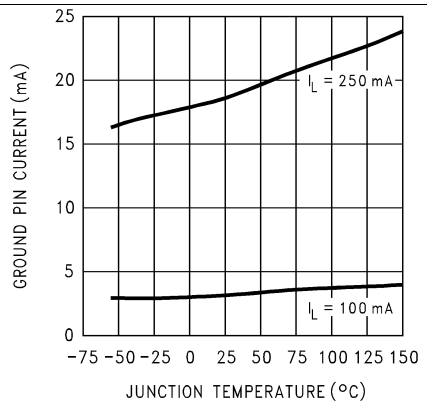


Figure 5. Ground Pin Current

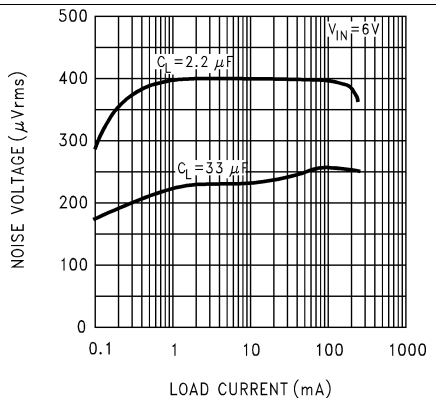


Figure 6. Output Noise Voltage

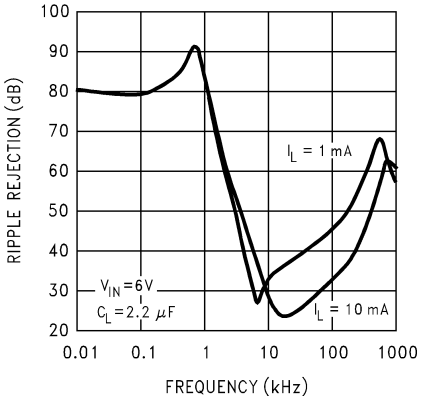


Figure 7. Ripple Rejection

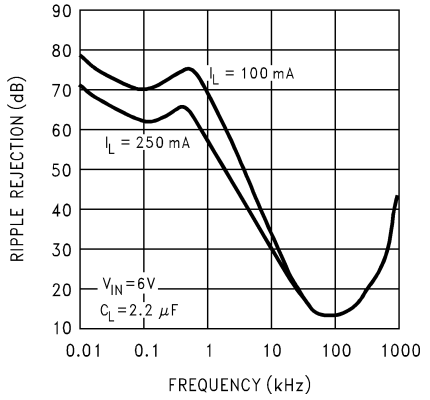


Figure 8. Ripple Rejection

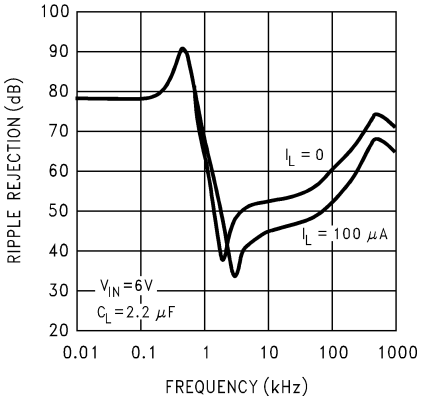


Figure 9. Ripple Rejection

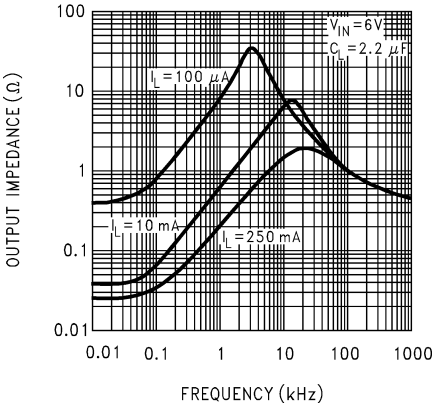


Figure 10. Output Impedance

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Typical Characteristics (continued)

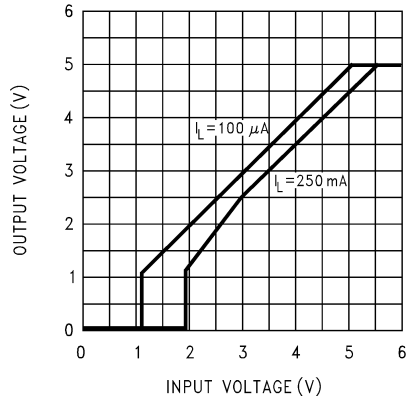


Figure 11. Dropout Characteristics

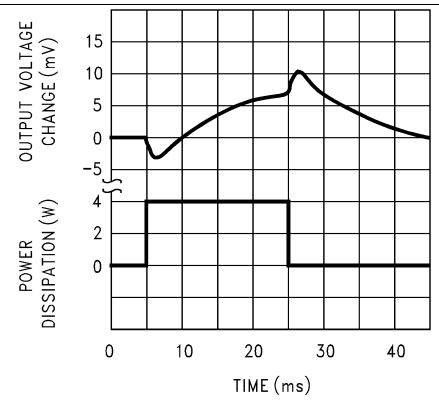


Figure 12. Thermal Response

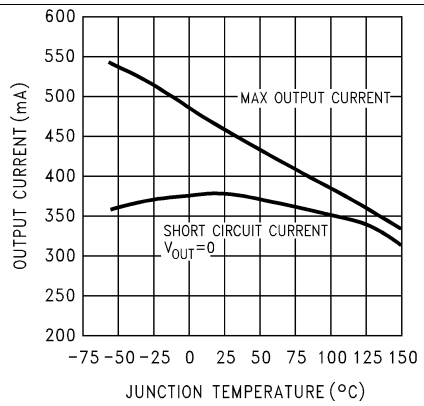


Figure 13. Short-Circuit Output Current and Maximum Output Current

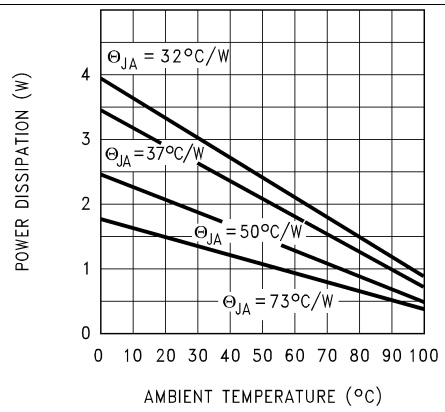


Figure 14. Maximum Power Dissipation (DDPAK/TO-263)

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7 Detailed Description

7.1 Overview

The LP2954 is a 5-V micropower LDO with very low quiescent current (90 μA typical at 1-mA load) and very low dropout voltage (typically 60 mV at light loads and 470 mV at 250-mA load current).

7.2 Functional Block Diagrams

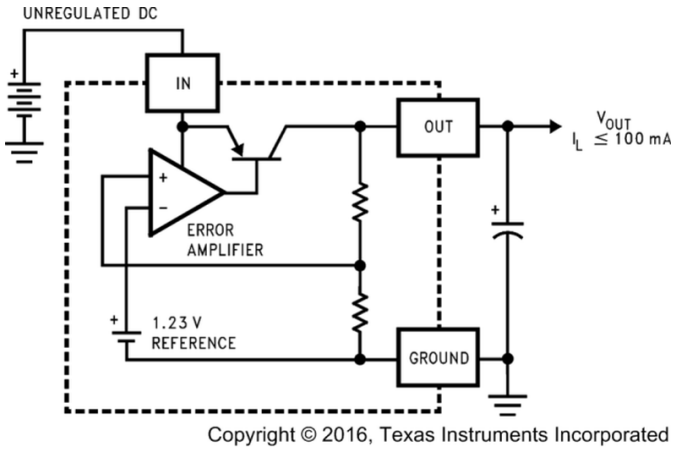


Figure 15. LP2954 TO-220 and TO-263 Functional Block Diagram

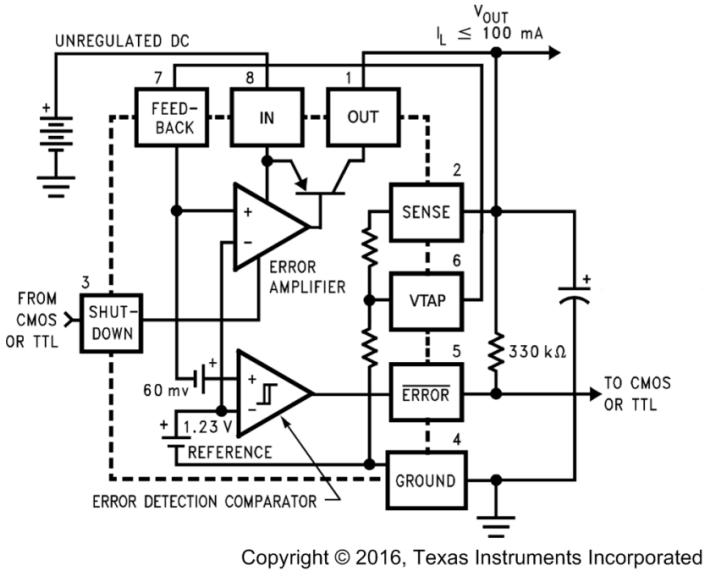


Figure 16. LP2954 SOIC Functional Block Diagram

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7.3 Feature Description

7.3.1 Dropout Voltage

The dropout voltage of the regulator is defined as the minimum input-to-output voltage differential required for the output voltage to stay within 100 mV of the output voltage measured with a 1-V differential. The dropout voltages for various values of load current are listed under *Electrical Characteristics*.

If the regulator is powered from a rectified AC source with a capacitive filter, the minimum AC line voltage and maximum load current must be used to calculate the minimum voltage at the input of the regulator. The minimum input voltage, *including AC ripple on the filter capacitor*, must not drop below the voltage required to keep the LP2954 in regulation. It is also advisable to verify operating at *minimum* operating ambient temperature, because the increasing ESR of the filter capacitor makes this a worst-case test for dropout voltage due to increased ripple amplitude.

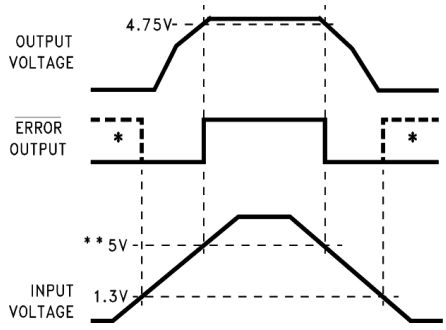
7.3.2 Dropout Detection Comparator

This comparator produces a logic LOW whenever the output falls out of regulation by more than about 5%. The 5% value is from the comparators built-in offset of 60 mV divided by the 1.23-V reference. The 5% low trip level remains constant regardless of the programmed output voltage. An out-of-regulation condition can result from low input voltage, current limiting, or thermal limiting.

Figure 17 gives a timing diagram showing the relationship between the output voltage, the $\overline{\text{ERROR}}$ output, and input voltage as the input voltage is ramped up and down to a regulator programmed for 5-V output. The $\overline{\text{ERROR}}$ signal becomes low at about 1.3-V input. It goes high at about 5-V input, where the output equals 4.75 V. Because the dropout voltage is load dependent, the *input* voltage trip points vary with load current. The *output* voltage trip point does not vary.

The comparator has an open-collector output which requires an external pullup resistor. This resistor may be connected to the regulator output or some other supply voltage. Using the regulator output prevents an invalid HIGH on the comparator output which occurs if it is pulled up to an external voltage while the regulator input voltage is reduced below 1.3 V. In selecting a value for the pullup resistor note that, while the output can sink 400 μA, this current adds to battery drain. Suggested values range from 100 kΩ to 1 MΩ. This resistor is not required if the output is unused.

When $V_{IN} \leq 1.3$ V, the $\overline{\text{ERROR}}$ pin becomes a high impedance, allowing the error flag voltage to rise to its pullup voltage. Using V_{OUT} as the pullup voltage (rather than an external 5-V source) keeps the error flag voltage below 1.2 V (typical) in this condition. The user may wish to divide down the error flag voltage using equal-value resistors (10 kΩ suggested) to ensure a low-level logic signal during any fault condition, while still allowing a valid high logic level during normal operation.



* In shutdown mode, $\overline{\text{ERROR}}$ goes high if it has been pulled up to an external supply. To avoid this invalid response, pull up to regulator output.
** Exact value depends on dropout voltage. (See *Dropout Voltage*)

Figure 17. $\overline{\text{ERROR}}$ Output Timing

7.3.3 Output Isolation

The regulator output can be left connected to an active voltage source (such as a battery) with the regulator input power turned off, *as long as the regulator ground pin is connected to ground*. If the ground pin is left floating, *damage to the regulator can occur* if the output is pulled up by an external voltage source.

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Feature Description (continued)

7.3.4 Reducing Output Noise

In reference applications it may be advantageous to reduce the AC noise present on the output. One method is to reduce regulator bandwidth by increasing output capacitance. This is relatively inefficient, because large increases in capacitance are required to get significant improvement.

Noise can be reduced more effectively by a bypass capacitor placed across R1 (refer to Figure 19). The formula for selecting the capacitor to be used is:

$$C_B = 1 / 2\pi R1 \times 20\ Hz \quad (1)$$

This gives a value of about 0.1 μF. When this is used, the output capacitor must be 6.8 μF (or greater) to maintain stability. The 0.1-μF capacitor reduces the high frequency gain of the circuit to unity, lowering the output noise from 260 μV to 80 μV using a 10-Hz to 100-kHz bandwidth. Also, noise is no longer proportional to the output voltage, so improvements are more pronounced at high output voltages.

7.4 Device Functional Modes

7.4.1 Shutdown Input

A logic-level signal shuts off the regulator output when a LOW (< 1.2 V) is applied to the $\overline{\text{SHUTDOWN}}$ input.

To prevent possible mis-operation, the $\overline{\text{SHUTDOWN}}$ input must be actively terminated. If the input is driven from open-collector logic, a pullup resistor (TI recommends 20 kΩ to 100 kΩ) must be connected from the $\overline{\text{SHUTDOWN}}$ input to the regulator input.

If the $\overline{\text{SHUTDOWN}}$ input is driven from a source that actively pulls high and low (like an operational amplifier), the pullup resistor is not required, but may be used.

If the shutdown function is not to be used, the cost of the pullup resistor can be saved by simply tying the $\overline{\text{SHUTDOWN}}$ input directly to the regulator input.

IMPORTANT: Because the *Absolute Maximum Ratings* state that the $\overline{\text{SHUTDOWN}}$ input cannot go more than 0.3 V below ground, the reverse-battery protection feature that protects the regulator input is sacrificed if the $\overline{\text{SHUTDOWN}}$ input is tied directly to the regulator input.

If reverse-battery protection is required in an application, the pullup resistor between the $\overline{\text{SHUTDOWN}}$ input and the regulator input must be used. The recommended 20 kΩ to 100 kΩ provides adequate protection of the $\overline{\text{SHUTDOWN}}$ pin during negative voltage transitions at the IN pin.

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8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The LP2954-N is a linear voltage regulator operating from 2.3 V to 30 V on the input and regulated output voltage of 5 V with typical 0.5% accuracy (LP2954AI) and 250 mA maximum output current. For linear voltage regulator the efficiency is defined by the ratio of output voltage to input voltage (efficiency = V_{OUT}/V_{IN}). To achieve high efficiency, the dropout voltage ($V_{IN} – V_{OUT}$) must be as small as possible, thus requiring a very low dropout LDO. Successfully implementing an LDO in an application depends on the application requirements. If the requirements are simply input voltage and output voltage, compliance specifications (such as internal power dissipation or stability) must be verified to ensure a solid design. If timing, start-up, noise, PSRR, or any other transient specification is required, the design becomes more challenging.

8.2 Typical Application

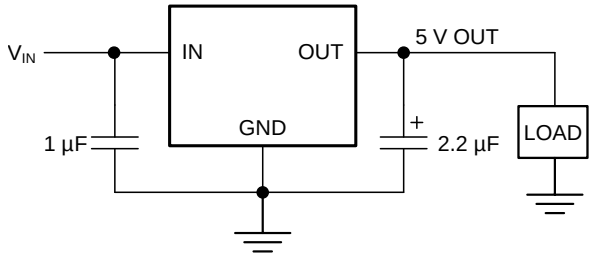


Figure 18. LP2954 Typical Application

8.2.1 Design Requirements

For typical LDO applications, use the parameters listed in Table 1.

Table 1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage	2.5 V to 30 V
Output voltage	1.23 V to 29 V
Output current	250 mA (maximum)
RMS noise, 10 Hz to100 kHz	260 μV_{RMS}

8.2.2 Detailed Design Procedure

8.2.2.1 External Capacitors

A 2.2 µF (or greater) capacitor is *required* between the OUT pin and GND to assure stability (refer to Figure 20). Without this capacitor, the device may oscillate. Most types of tantalum or aluminum electrolytic capacitors work here. Film-type capacitors work, but are more expensive. Many aluminum electrolytics contain electrolytes which freeze at −30°C, which requires the use of solid tantalums below −25°C. The important parameters of the capacitor are an equivalent series resistance (ESR) of about 5 Ω or less and a resonant frequency above 500 kHz (the ESR may increase by a factor of *20* or *30* as the temperature is reduced from 25°C to −30°C). The value of this capacitor may be increased without limit. At lower values of output current, less output capacitance is required for stability. The capacitor can be reduced to 0.68 µF for currents below 10 mA or 0.22 µF for currents below 1 mA.

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Place a 1-μF capacitor from the IN pin to GND if there is more than 10 inches of wire between the input and the AC filter capacitor or if a battery input is used.

Programming the output for voltages below 5 V runs the error amplifier at lower gains requiring more output capacitance for stability. At 3.3-V output, a minimum of 4.7 μF is required. For the worst case condition of 1.23-V output and 250 mA of load current, a 6.8-μF (or larger) capacitor must be used.

Stray capacitance to the FEEDBACK pin can cause instability. This problem is most likely to appear when using high value external resistors to set the output voltage. Adding a 100-pF capacitor between the OUT and FEEDBACK pins and increasing the output capacitance to 6.8 μF (or greater) solves the problem.

8.2.2.2 Minimum Load

When setting the output voltage using an external resistive divider, TI recommends a minimum current of 1 μA through the resistors to provide a minimum load.

It should be noted that a minimum load current is specified in several of the electrical characteristic test conditions, so this value must be used to obtain correlation on these tested limits. The part is parametrically tested down to 100 μA, but is functional with no load.

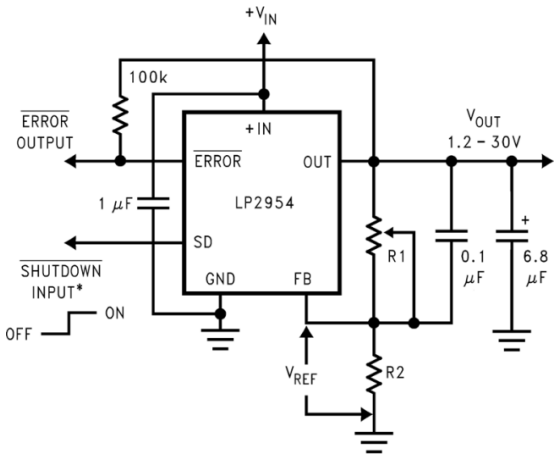
8.2.2.3 Programming The Output Voltage

The SOIC version of the LP2954 regulator may be pin strapped for 5-V operation using its internal resistive divider by tying the OUT and SENSE pins together and also tying the FEEDBACK and 5V TAP pins together.

Alternatively, it may be programmed for any voltage between the 1.23-V reference and the 30-V maximum rating using an external pair of resistors (see Figure 19). The complete equation for the output voltage is:

$$V_{OUT} = V_{REF} \times (1 + R1 / R2) + (I_{FB} \times R1) \quad (2)$$

where V_{REF} is the 1.23-V reference and I_{FB} is the FEEDBACK pin bias current (−20 nA typical). The minimum recommended load current of 1 μA sets an upper limit of 1.2 MΩ on the value of R2 in cases where the regulator must work with no load (see *Minimum Load*). I_{FB} produces a typical 2% error in V_{OUT} which can be eliminated at room temperature by trimming R1. For better accuracy, choosing R2 = 100 kΩ reduces this error to 0.17% while increasing the resistor program current to 12 μA. Because the typical quiescent current is 120 μA, this added current is negligible.



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*Drive with TTL-low to shutdown

Figure 19. Adjustable Regulator

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8.2.2.4 Power Dissipation

Knowing the device power dissipation and proper sizing of the thermal plane connected to the tab or pad is critical to ensuring reliable operation. Device power dissipation depends on input voltage, output voltage, and load conditions and can be calculated with Equation 3.

$$P_{D(MAX)} = (V_{IN(MAX)} - V_{OUT}) \times I_{OUT} \quad (3)$$

Power dissipation can be minimized, and greater efficiency can be achieved, by using the lowest available voltage drop option that would still be greater than the dropout voltage (V_{DO}). However, keep in mind that higher voltage drops result in better dynamic (that is, PSRR and transient) performance.

Power dissipation and junction temperature are most often related by the junction-to-ambient thermal resistance ($R_{\theta JA}$) of the combined PCB and device package and the temperature of the ambient air (T_A), according to Equation 4 or Equation 5:

$$T_{J(MAX)} = T_{A(MAX)} + (R_{\theta JA} \times P_{D(MAX)}) \quad (4)$$

$$P_{D(MAX)} = (T_{J(MAX)} - T_{A(MAX)}) / R_{\theta JA} \quad (5)$$

Unfortunately, this $R_{\theta JA}$ is highly dependent on the heat-spreading capability of the particular PCB design, and therefore varies according to the total copper area, copper weight, and location of the planes. The $R_{\theta JA}$ recorded in *Thermal Information* is determined by the specific EIA/JEDEC JESD51-7 standard for PCB and copper-spreading area, and is to be used only as a relative measure of package thermal performance. For a well-designed thermal layout, $R_{\theta JA}$ is actually the sum of the package junction-to-case (bottom) thermal resistance ($R_{\theta JCbot}$) plus the thermal resistance contribution by the PCB copper area acting as a heat sink.

8.2.2.5 Estimating Junction Temperature

The EIA/JEDEC standard recommends the use of psi (Ψ) thermal characteristics to estimate the junction temperatures of surface mount devices on a typical PCB board application. These characteristics are not true thermal resistance values, but rather package specific thermal characteristics that offer practical and relative means of estimating junction temperatures. These psi metrics are determined to be significantly independent of copper-spreading area. The key thermal characteristics (Ψ_{JT} and Ψ_{JB}) are given in *Thermal Information* and are used in accordance with Equation 6 or Equation 7.

$$T_{J(MAX)} = T_{TOP} + (\Psi_{JT} \times P_{D(MAX)})$$

where

- $P_{D(MAX)}$ is explained in Equation 5
- T_{TOP} is the temperature measured at the center-top of the device package. (6)

$$T_{J(MAX)} = T_{BOARD} + (\Psi_{JB} \times P_{D(MAX)})$$

where

- $P_{D(MAX)}$ is explained in Equation 5.
- T_{BOARD} is the PCB surface temperature measured 1-mm from the device package and centered on the package edge. (7)

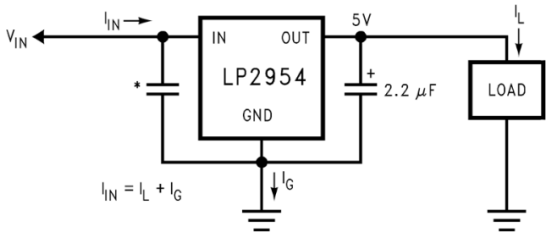
For more information about the thermal characteristics Ψ_{JT} and Ψ_{JB}, *Semiconductor and IC Package Thermal Metrics*; for more information about measuring T_{TOP} and T_{BOARD}, see *Using New Thermal Metrics*; and for more information about the EIA/JEDEC JESD51 PCB used for validating $R_{\theta JA}$, see *Thermal Characteristics of Linear and Logic Packages Using JEDEC PCB Designs*. These application notes are available at www.ti.com.

8.2.2.6 Heatsinking the TO-220 Package

A heat sink may be required with the LP2954IT depending on the maximum power dissipation and maximum ambient temperature of the application. Under all possible operating conditions, the junction temperature must be within the range specified under *Recommended Operating Conditions*.

To determine if a heat sink is required, the maximum power dissipated by the regulator, $P_{(MAX)}$, must be calculated. It is important to remember that if the regulator is powered from a transformer connected to the AC line, the *maximum specified AC input voltage* must be used (because this produces the maximum DC input voltage to the regulator). Figure 20 shows the voltages and currents that are present in the circuit. The formula for calculating the power dissipated in the regulator is also shown in Figure 20.

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*See *External Capacitors*

$P_D = (((V_{IN} – V_{OUT}) \times I_{OUT}) + (V_{IN} \times I_G))$

Figure 20. Basic 5-V Regulator Circuit

The next parameter which must be calculated is the maximum allowable temperature rise, $T_{R(MAX)}$. This is calculated by using the formula:

$$T_{R(MAX)} = T_{J(MAX)} - T_{A(MAX)}$$

where

- $T_{J(MAX)}$ is the maximum allowable junction temperature
- $T_{A(MAX)}$ is the maximum ambient temperature (8)

Using the calculated values for $T_{R(MAX)}$ and $P_{(MAX)}$, the required value for junction-to-ambient thermal resistance, $R_{\theta JA}$, can now be found:

$$R_{\theta JA} = T_{R(MAX)} / P_{(MAX)} \quad (9)$$

If the calculated value is 60°C/W *or higher* , the regulator may be operated without an external heat sink. If the calculated value is *below* 60°C/W, an external heatsink is required. The required thermal resistance for this heat sink can be calculated using the formula:

$$R_{\theta HA} = R_{\theta JA} - R_{\theta JC(bot)} - R_{\theta CH}$$

where

- $R_{\theta JC(bot)}$ is the junction-to-case thermal resistance, which is specified as 0.9°C/W maximum for the LP2954IT
- $R_{\theta CH}$ is the case-to-heat-sink thermal resistance, which is dependent on the interfacing material (if used). For details and typical values in Table 2 and Table 3.
- $R_{\theta(H-A)}$ is the heatsink-to-ambient thermal resistance. It is this specification (listed on the heat-sink manufacturers data sheet) which defines the effectiveness of the heat sink. The heat sink selected must have a thermal resistance which is *equal to or lower* than the value of $R_{\theta HA}$ calculated from the above listed formula. (10)

Table 2. Typical Values of Case-To-Heatsink Thermal Resistance ($R_{\theta CH}$) (Data from Aavid Engineering)

	UNIT (C°/W)
Silicone grease	1
Dry interface	1.3
Mica with grease	1.4

Table 3. Typical Values Of Case-To-Heatsink Thermal Resistance ($R_{\theta CH}$) (Data from Thermalloy)

	UNIT (C°/W)
Thermasil III	1.3
Thermasil II	1.5
Thermalfilm (0.002) with grease	2.2

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8.2.3 Application Curves

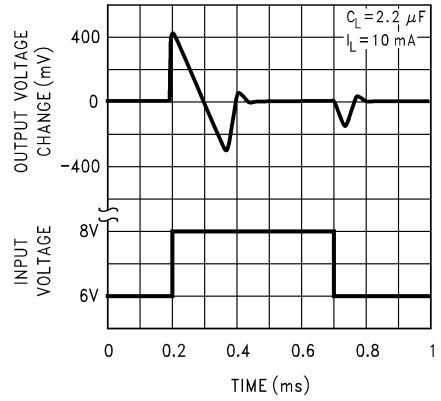


Figure 21. Line Transient Response

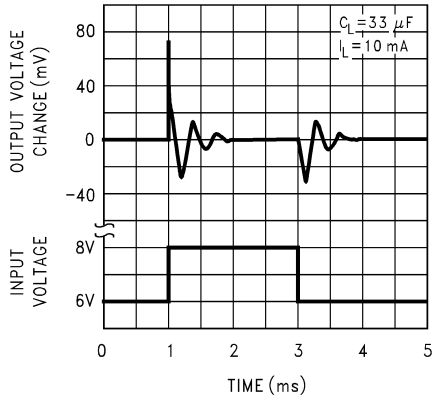


Figure 22. Line Transient Response

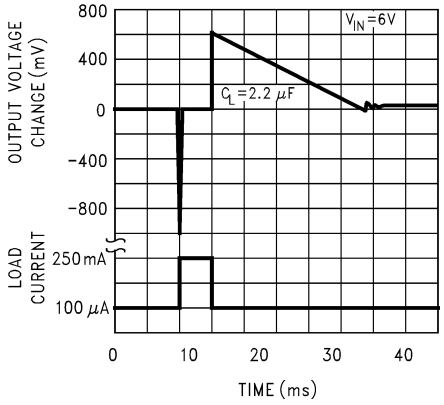


Figure 23. Load Transient Response

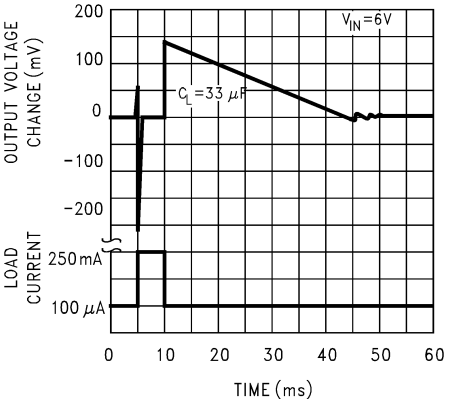


Figure 24. Load Transient Response

9 Power Supply Recommendations

The LP2954 is designed to operate from a minimum input voltage supply of either 2.5 V or $V_{OUT(NOM)}$ + 1 V, whichever is higher. The maximum input supply voltage is 30 V, but may be limited by thermal dissipation of the selected package. The input voltage range provides adequate headroom in order for the device to have a regulated output. This input supply must be well regulated. If the input supply is noisy, additional input capacitors with low ESR can help. improve the output noise performance.

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10 Layout

10.1 Layout Guidelines

For best overall performance, place all the circuit components on the same side of the circuit board and as near as practical to the respective LDO pin connections. Place ground return connections to the input and output capacitor, and to the LDO ground pin as close as possible to each other, connected by a wide, component-side, copper surface. The use of vias and long traces to create LDO circuit connections is strongly discouraged and negatively affects system performance. This grounding and layout scheme minimizes inductive parasitic, and thereby reduces load-current transients, minimizes noise, and increases circuit stability.

TI also recommends a ground reference plane and is either embedded in the PCB itself or located on the bottom side of the PCB opposite the components. This reference plane serves to assure accuracy of the output voltage, shield noise, and behaves similar to a thermal plane to spread heat from the LDO device. In most applications, this ground plane is necessary to meet thermal requirements.

10.2 Layout Example

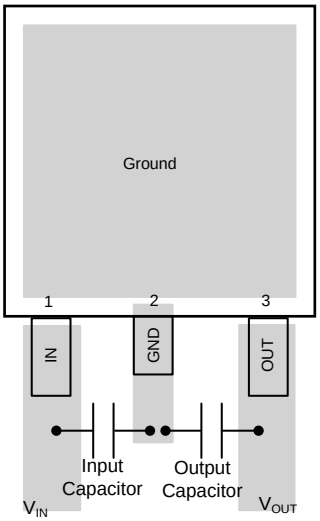


Figure 25. LP2954 TO-263 Board Layout

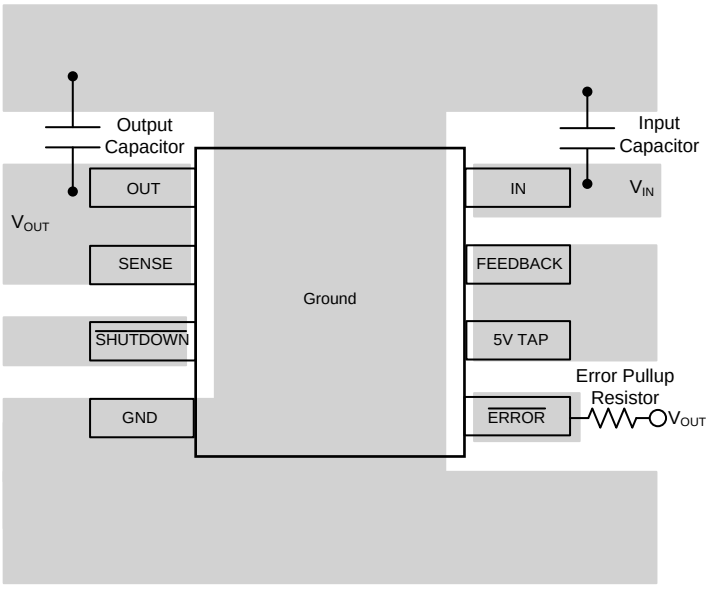


Figure 26. LP2954 SOIC Board Layout

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11 デバイスおよびドキュメントのサポート

11.1 関連資料

詳細情報については、以下を参照してください。

- *『半導体およびICパッケージの熱指標』*
- *『新しい温度指標の使用』*
- *『JEDEC PCB設計を使用するリニアおよびロジック・パッケージの熱特性』*

11.2 関連リンク

表 4 に、クイック・アクセス・リンクの一覧を示します。カテゴリには、技術資料、サポートおよびコミュニティ・リソース、ツールとソフトウェア、およびサンプル注文またはご購入へのクイック・アクセスが含まれます。

表 4. 関連リンク

製品	プロダクト・フォルダ	サンプルとご購入	技術資料	ツールとソフトウェア	サポートとコミュニティ
LP2954	ここをクリック	ここをクリック	ここをクリック	ここをクリック	ここをクリック
LP2954A	ここをクリック	ここをクリック	ここをクリック	ここをクリック	ここをクリック

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11.4 コミュニティ・リソース

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

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Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

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11.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

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12 メカニカル、パッケージ、および注文情報

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LP2954AIM/NOPB	Active	Production	SOIC (D) | 8	95 | TUBE	Yes	SN	Level-1-260C-UNLIM	-40 to 125	LP295 4AIM
LP2954AIM/NOPB.B	Active	Production	SOIC (D) | 8	95 | TUBE	Yes	SN	Level-1-260C-UNLIM	-40 to 125	LP295 4AIM
LP2954AIMX/NOPB	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	LP295 4AIM
LP2954AIMX/NOPB.B	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	LP295 4AIM
LP2954AIS/NOPB	Active	Production	DDPAK/ TO-263 (KTT) | 3	45 | TUBE	ROHS Exempt	SN	Level-3-245C-168 HR	-40 to 125	LP2954AIS
LP2954AIS/NOPB.B	Active	Production	DDPAK/ TO-263 (KTT) | 3	45 | TUBE	ROHS Exempt	SN	Level-3-245C-168 HR	-40 to 125	LP2954AIS
LP2954AISX/NOPB	Active	Production	DDPAK/ TO-263 (KTT) | 3	500 | LARGE T&R	ROHS Exempt	SN	Level-3-245C-168 HR	-40 to 125	LP2954AIS
LP2954AISX/NOPB.B	Active	Production	DDPAK/ TO-263 (KTT) | 3	500 | LARGE T&R	ROHS Exempt	SN	Level-3-245C-168 HR	-40 to 125	LP2954AIS
LP2954AIT/NOPB	NRND	Production	TO-220 (NDE) | 3	45 | TUBE	Yes	SN	Level-1-NA-UNLIM	-40 to 125	LP2954AIT
LP2954AIT/NOPB.B	NRND	Production	TO-220 (NDE) | 3	45 | TUBE	Yes	SN	Level-1-NA-UNLIM	-40 to 125	LP2954AIT
LP2954IM/NOPB	Active	Production	SOIC (D) | 8	95 | TUBE	Yes	SN	Level-1-260C-UNLIM	-40 to 125	LP29 54IM
LP2954IM/NOPB.B	Active	Production	SOIC (D) | 8	95 | TUBE	Yes	SN	Level-1-260C-UNLIM	-40 to 125	LP29 54IM
LP2954IMX/NOPB	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	LP29 54IM
LP2954IMX/NOPB.B	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	LP29 54IM
LP2954IS/NOPB	Active	Production	DDPAK/ TO-263 (KTT) | 3	45 | TUBE	ROHS Exempt	SN	Level-3-245C-168 HR	-40 to 125	LP2954IS
LP2954IS/NOPB.B	Active	Production	DDPAK/ TO-263 (KTT) | 3	45 | TUBE	ROHS Exempt	SN	Level-3-245C-168 HR	-40 to 125	LP2954IS
LP2954ISX/NOPB	Active	Production	DDPAK/ TO-263 (KTT) | 3	500 | LARGE T&R	ROHS Exempt	SN	Level-3-245C-168 HR	-40 to 125	LP2954IS

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LP2954ISX/NOPB.B	Active	Production	DDPAK/ TO-263 (KTT) | 3	500 | LARGE T&R	ROHS Exempt	SN	Level-3-245C-168 HR	-40 to 125	LP2954IS
LP2954IT/NOPB	Active	Production	TO-220 (NDE) | 3	45 | TUBE	Yes	SN	Level-1-NA-UNLIM	-40 to 125	LP2954IT
LP2954IT/NOPB.B	Active	Production	TO-220 (NDE) | 3	45 | TUBE	Yes	SN	Level-1-NA-UNLIM	-40 to 125	LP2954IT

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

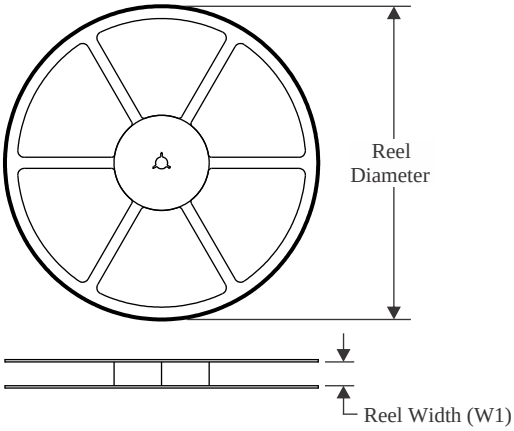
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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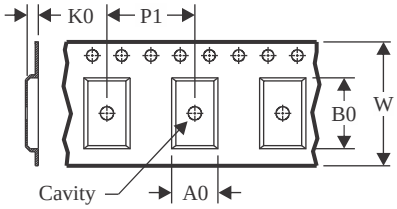
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

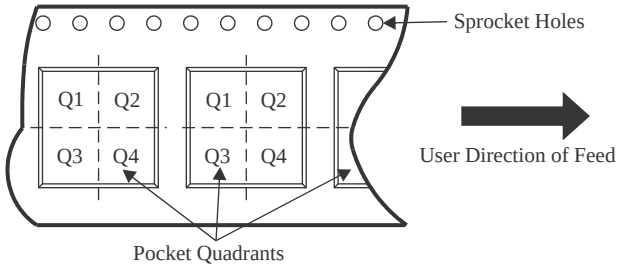


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

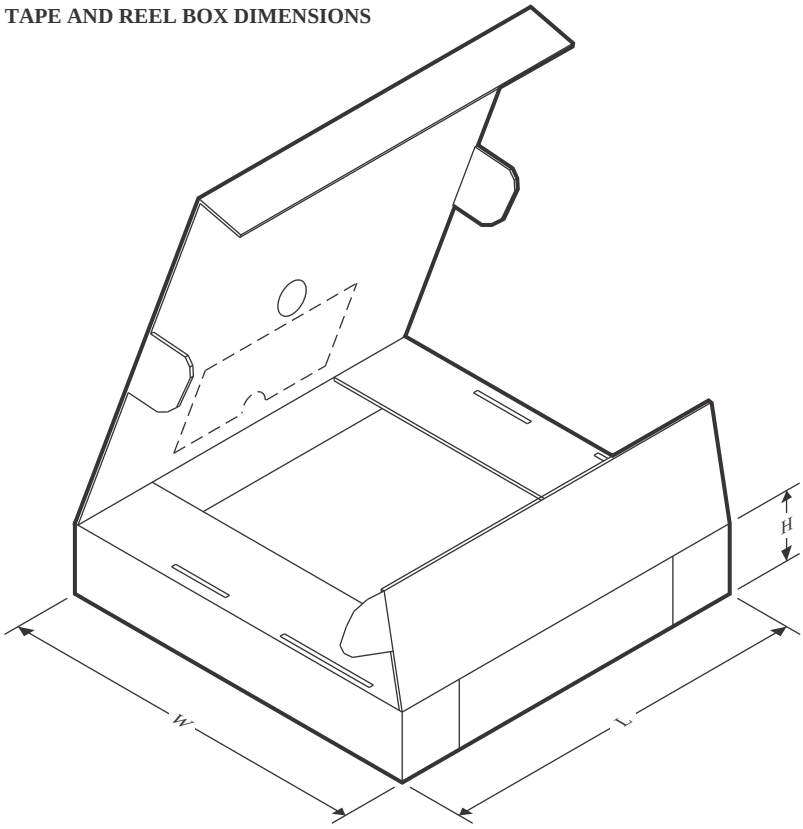
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LP2954AIMX/NOPB	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LP2954AISX/NOPB	DDPAK/ TO-263	KTT	3	500	330.0	24.4	10.75	14.85	5.0	16.0	24.0	Q2
LP2954IMX/NOPB	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LP2954ISX/NOPB	DDPAK/ TO-263	KTT	3	500	330.0	24.4	10.75	14.85	5.0	16.0	24.0	Q2

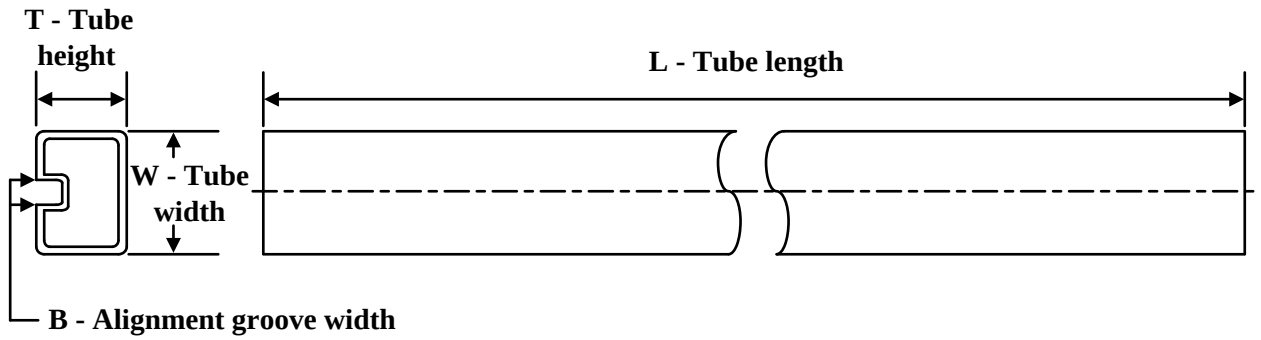
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

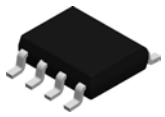
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LP2954AIMX/NOPB	SOIC	D	8	2500	367.0	367.0	35.0
LP2954AISX/NOPB	DDPAK/TO-263	KTT	3	500	356.0	356.0	45.0
LP2954IMX/NOPB	SOIC	D	8	2500	367.0	367.0	35.0
LP2954ISX/NOPB	DDPAK/TO-263	KTT	3	500	356.0	356.0	45.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
LP2954AIM/NOPB	D	SOIC	8	95	495	8	4064	3.05
LP2954AIM/NOPB.B	D	SOIC	8	95	495	8	4064	3.05
LP2954AIS/NOPB	KTT	TO-263	3	45	502	25	8204.2	9.19
LP2954AIS/NOPB.B	KTT	TO-263	3	45	502	25	8204.2	9.19
LP2954AIT/NOPB	NDE	TO-220	3	45	502	33	6985	4.06
LP2954AIT/NOPB.B	NDE	TO-220	3	45	502	33	6985	4.06
LP2954IM/NOPB	D	SOIC	8	95	495	8	4064	3.05
LP2954IM/NOPB.B	D	SOIC	8	95	495	8	4064	3.05
LP2954IS/NOPB	KTT	TO-263	3	45	502	25	8204.2	9.19
LP2954IS/NOPB.B	KTT	TO-263	3	45	502	25	8204.2	9.19
LP2954IT/NOPB	NDE	TO-220	3	45	502	33	6985	4.06
LP2954IT/NOPB.B	NDE	TO-220	3	45	502	33	6985	4.06

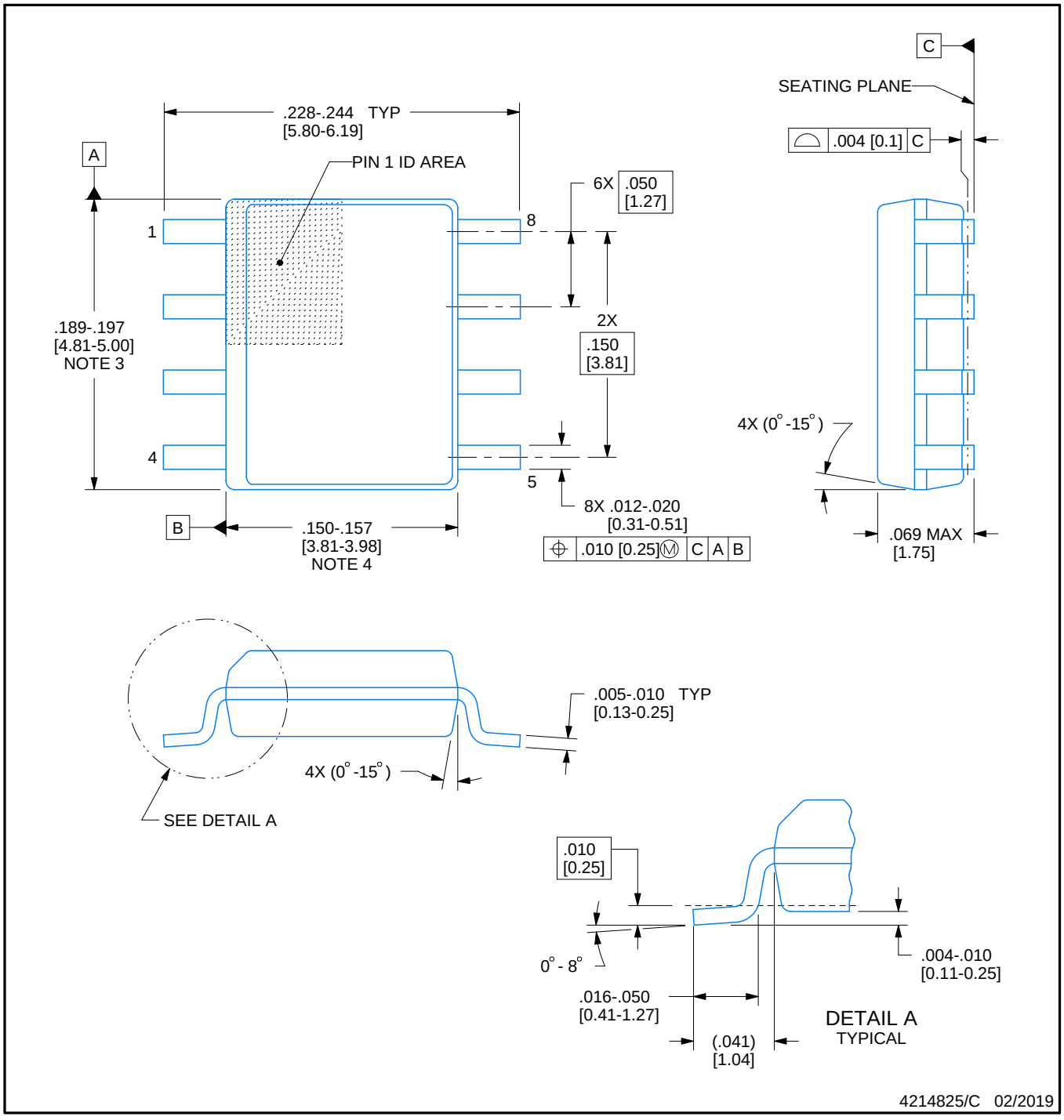


PACKAGE OUTLINE

D0008A

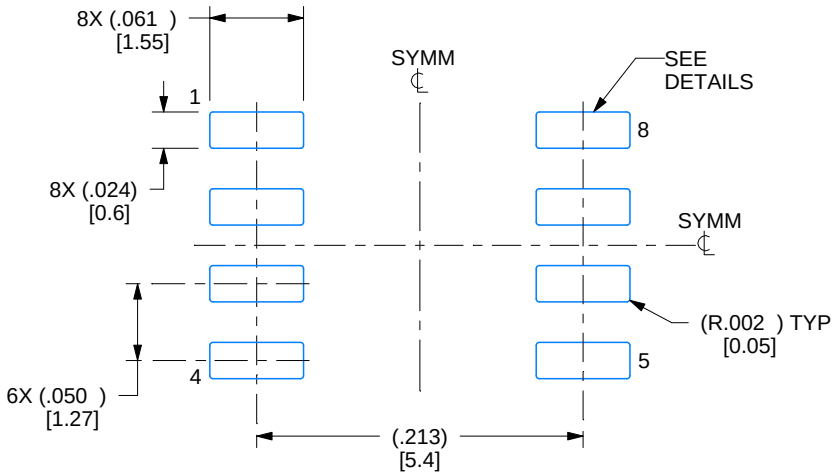
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

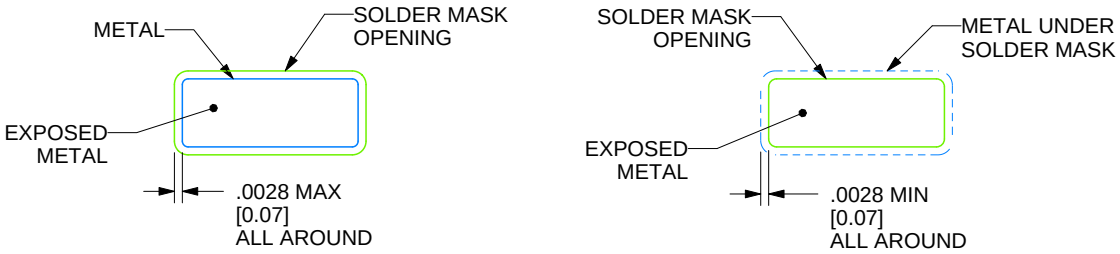


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

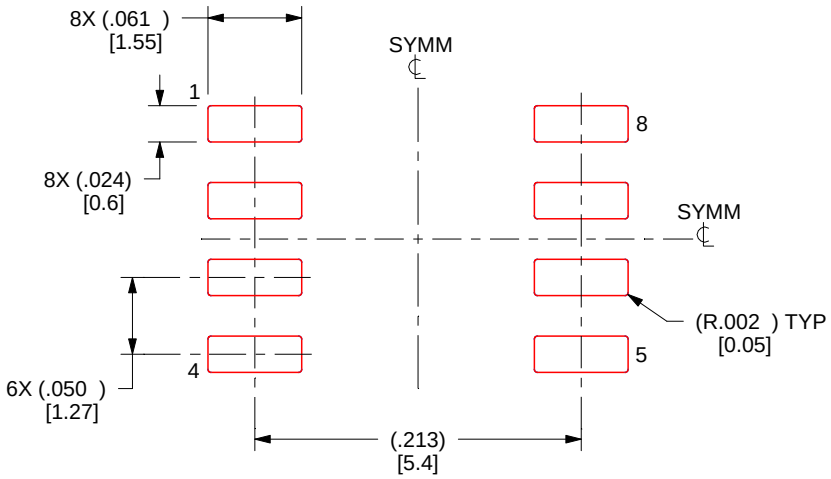
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



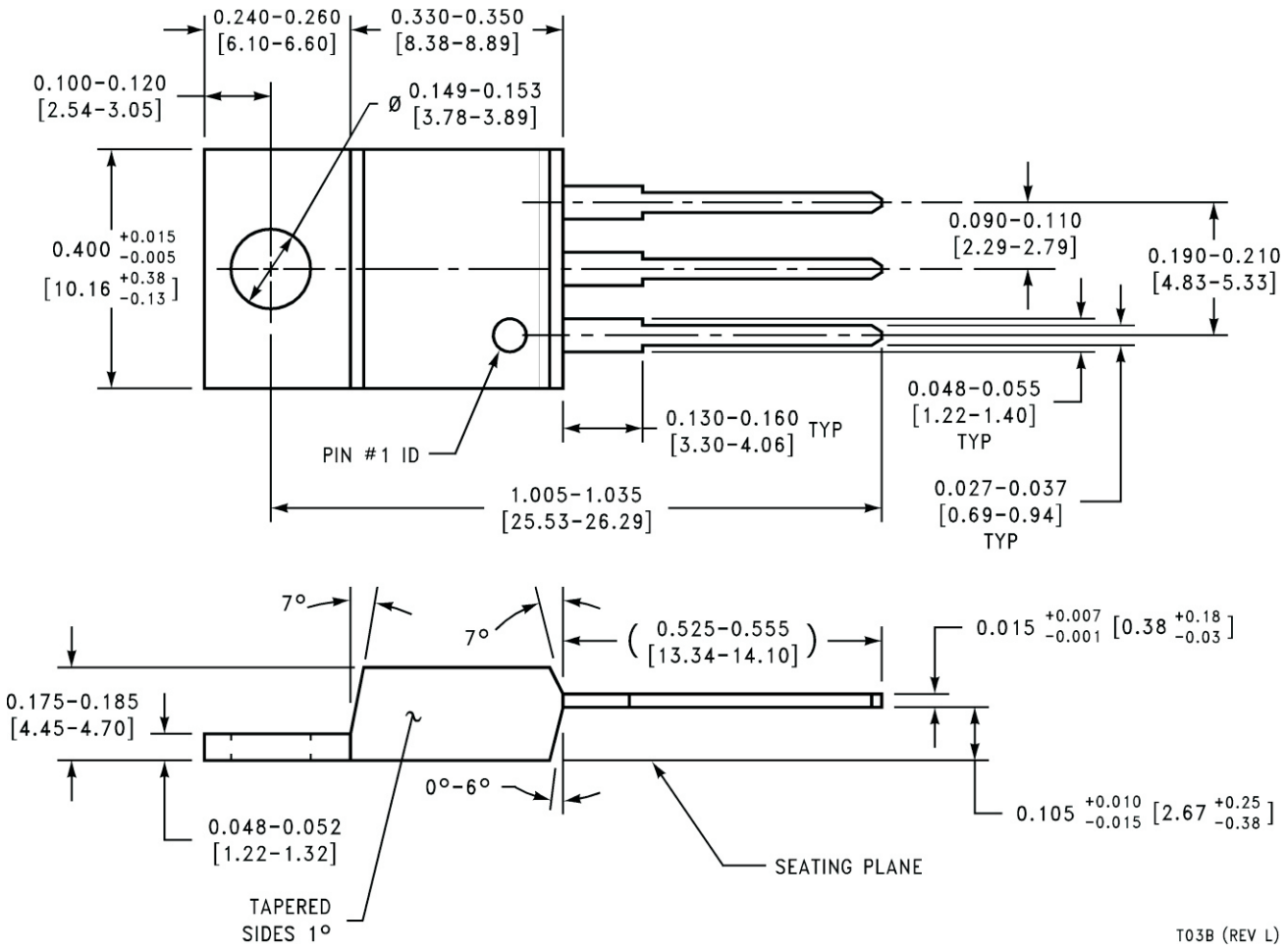
SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

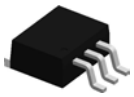
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

NDE0003B


0.240-0.260
[6.10-6.60]
0.330-0.350
[8.38-8.89]
0.100-0.120
[2.54-3.05]
Ø 0.149-0.153
[3.78-3.89]
0.400 +0.015 -0.005
[10.16 +0.38 -0.13]
0.090-0.110
[2.29-2.79]
0.190-0.210
[4.83-5.33]
PIN #1 ID
0.130-0.160 TYP
[3.30-4.06]
0.048-0.055
[1.22-1.40]
TYP
1.005-1.035
[25.53-26.29]
0.027-0.037
[0.69-0.94]
TYP
7°
7°
(0.525-0.555
[13.34-14.10])
0.015 +0.007 -0.001 [0.38 +0.18 -0.03]
0.175-0.185
[4.45-4.70]
0°-6°
0.105 +0.010 -0.015 [2.67 +0.25 -0.38]
0.048-0.052
[1.22-1.32]
SEATING PLANE
TAPERED
SIDES 1°
T03B (REV L)

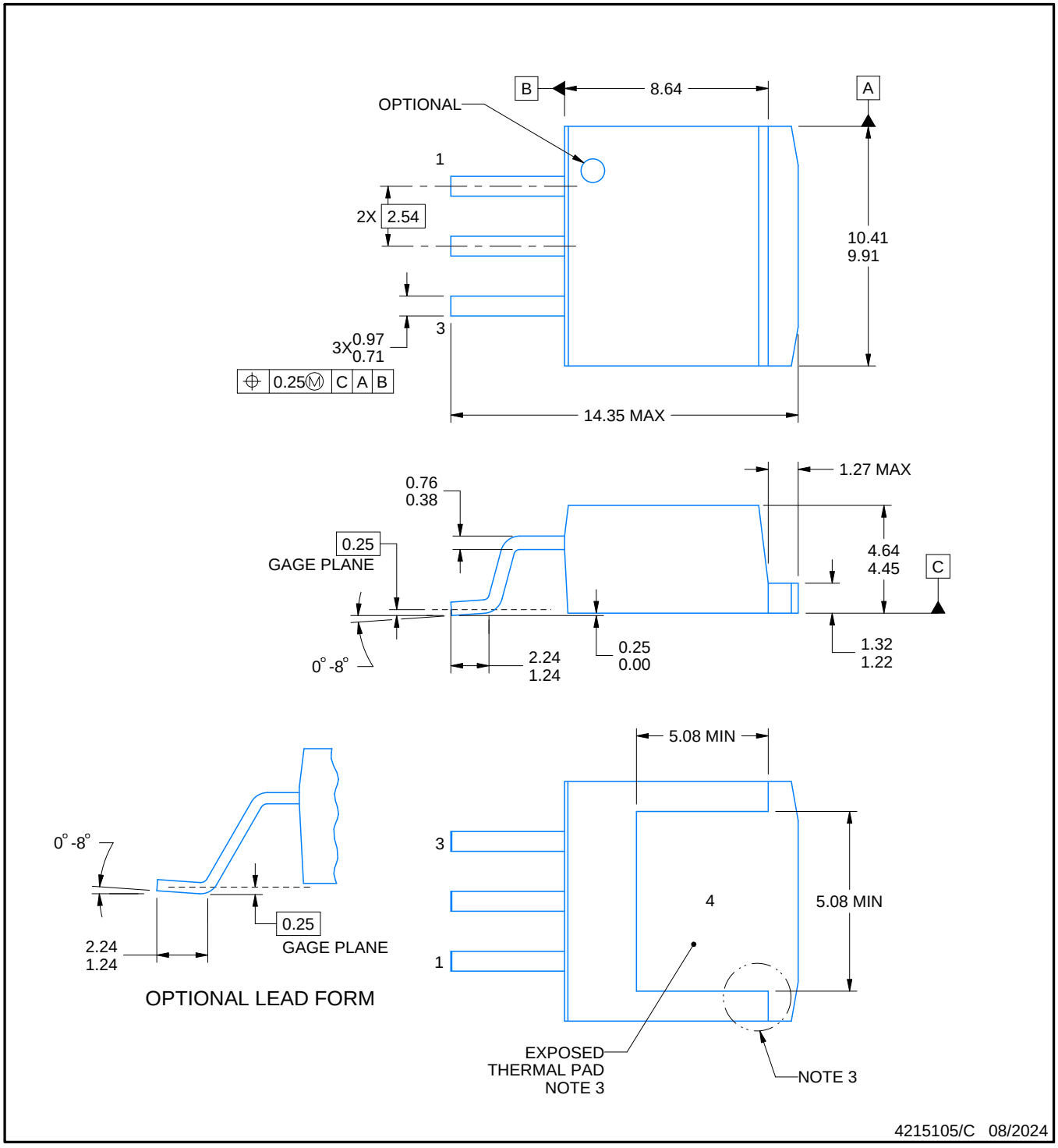
KTT0003B



PACKAGE OUTLINE

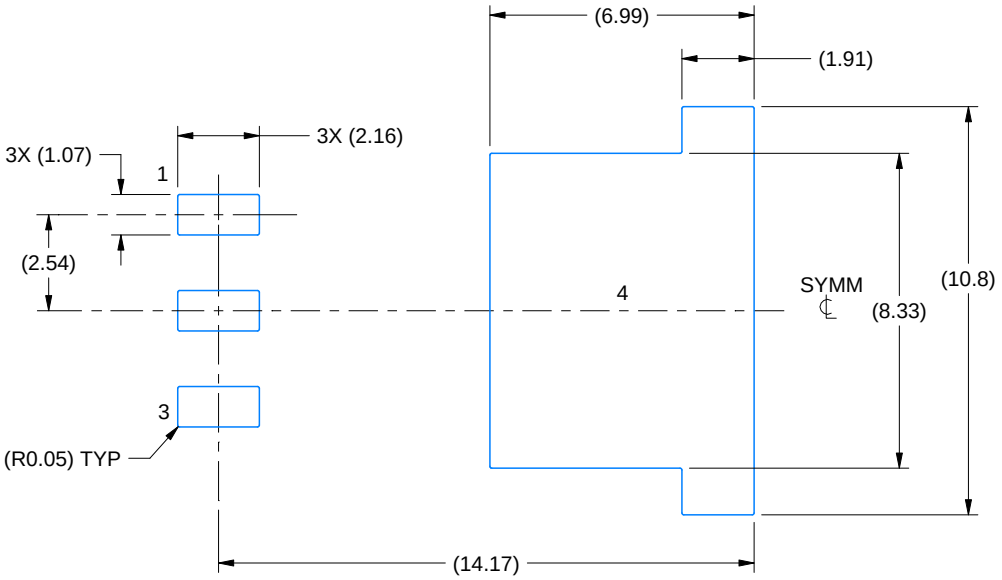
TO-263 - 4.83 mm max height

TRANSISTOR OUTLINE

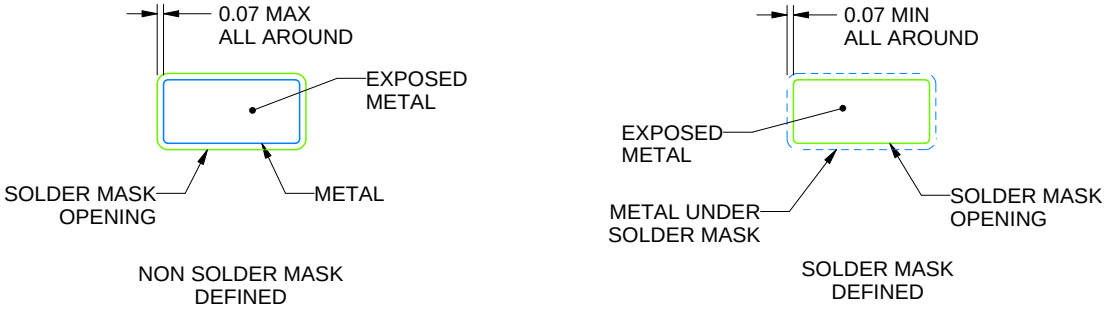


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Features may not exist and shape may vary per different assembly sites.
4. Reference JEDEC registration TO-263, except minimum lead thickness and minimum exposed pad length.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:5X

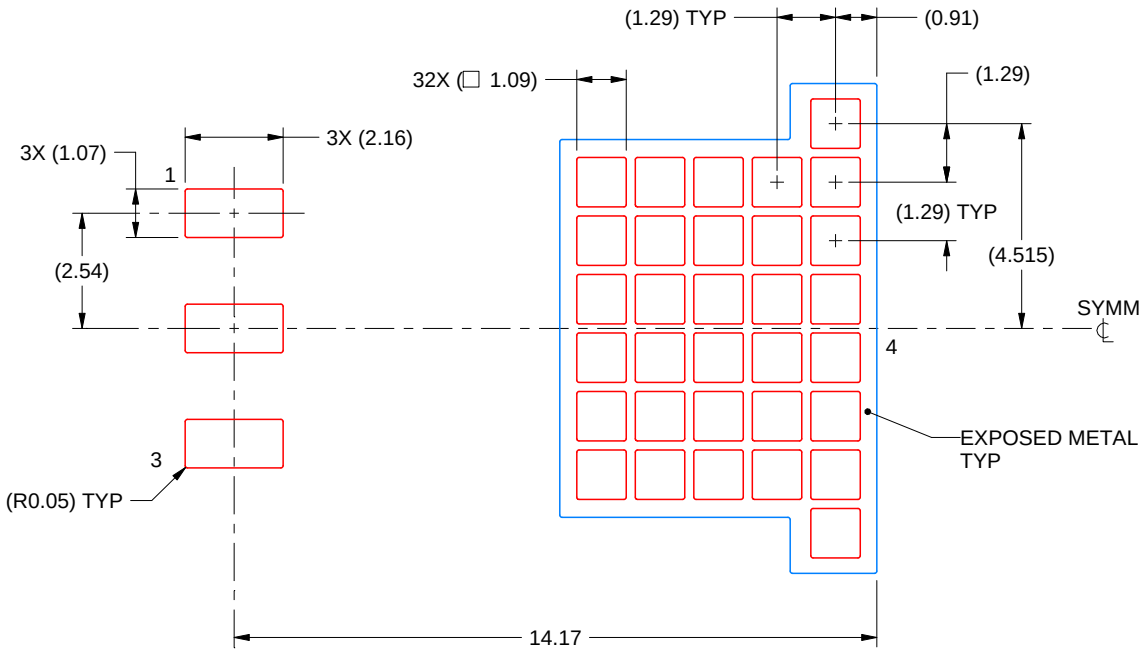


SOLDER MASK DETAILS

4215105/C 08/2024

NOTES: (continued)

5. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002(www.ti.com/lit/slm002) and SLMA004 (www.ti.com/lit/slma004).
6. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
60% PRINTED SOLDER COVERAGE BY AREA
SCALE:6X

4215105/C 08/2024

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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最終更新日：2025 年 10 月