LP3943 16 チャネル RGB、白色 LED ドライバ 独立 SMBUS/I²C ストリング制御付き

1 特長

- パワーオン リセット内蔵
- アクティブ Low のリセット
- 内部高精度発振回路
- 可変調光レート (6.25ms～1.6s、160Hz～0.625Hz)
- 16 個の LED ドライバ (複数の状態をプログラム可能: オン、オフ、入力、および指定されたレートでの調光)
- 16 個のオープン ドレイン出力、LED あたり 25mA まで駆動可能

2 アプリケーション

- 携帯電話用にカスタマイズされた点滅 LED ライト
- 携帯用アプリケーション
- デジタル カメラ
- 表示灯
- 汎用 I/O エクスパンダ
- 玩具

3 概要

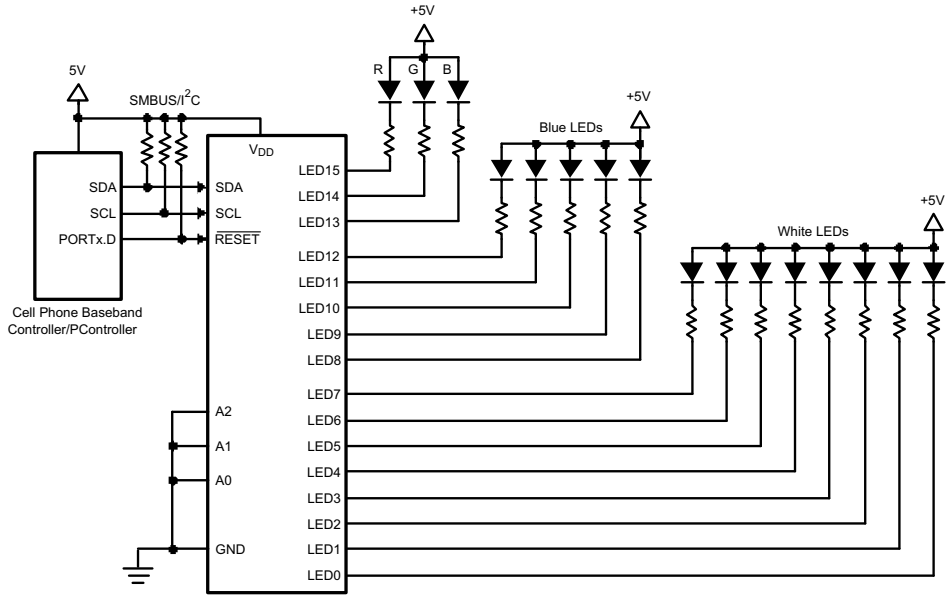
LP3943 は、16 個の LED を独立して駆動できる統合デバイスです。このデバイスは高精度の発振器も内蔵しており、各 LED を駆動するために必要なすべてのタイミングを供給します。2 つのプリスケーラ レジスタおよび 2 つの PWM レジスタにより、多用途なデューティ サイクル制御が可能です。LP3943 は、必要に応じて SMBUS/I²C アプリケーションで LED を調光する機能を備えており、バスのトラフィックを削減できます。

従来の 74LS594/5 などのシリアル シフト レジスタを使用する調光 LED は、シリアル バス上で大量のトラフィックを必要とします。しかし、LP3943 で必要なことは、各出力ピンの周波数とデューティ サイクルの設定だけです。その後は、ホストからの 1 つのコマンドだけで、各オープン ドレイン出力をオンまたはオフ状態に切り替えたり、あるいは、プログラム済みの周波数とデューティ サイクルでオン オフを繰り返したりできます。最大出力シンク電流は、ピンあたり 25mA、パッケージあたり 200mA です。LED の制御に使用されていないポートは、汎用入出力の拡張に使用できます。

製品情報 (1)

部品番号	パッケージ	本体サイズ (公称)
LP3943	WQFN (24)	4.00mm × 4.00mm

(1) 利用可能なすべてのパッケージについては、データシートの末尾にある注文情報を参照してください。



代表的なアプリケーション回路

このリソースの元の言語は英語です。翻訳は概要を便宜的に提供するもので、自動化ツール (機械翻訳) を使用していることがあり、TI では翻訳の正確性および妥当性につきましては一切保証いたしません。実際の設計などの前には、ti.com で必ず最新の英語版をご参照くださいますようお願いいたします。

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4 Pin Configuration and Functions

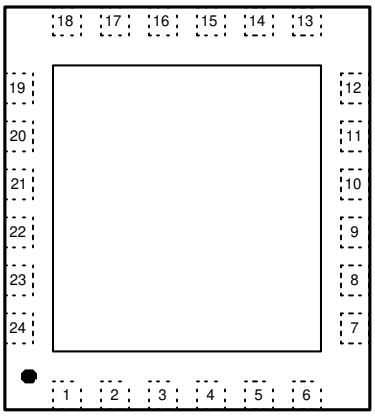

図 4-1. RTW Package 24-Pin WQFN With Exposed Pad Top View

Pin Functions

PIN		I/O	DESCRIPTION
NUMBER	NAME		
1	LED0	Output	Output of LED0 Driver
2	LED1	Output	Output of LED1 Driver
3	LED2	Output	Output of LED2 Driver
4	LED3	Output	Output of LED3 Driver
5	LED4	Output	Output of LED4 Driver
6	LED5	Output	Output of LED5 Driver
7	LED6	Output	Output of LED6 Driver
8	LED7	Output	Output of LED7 Driver
9	GND	Ground	Ground
10	LED8	Output	Output of LED8 Driver
11	LED9	Output	Output of LED9 Driver
12	LED10	Output	Output of LED10 Driver

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PIN		I/O	DESCRIPTION
NUMBER	NAME		
13	LED11	Output	Output of LED11 Driver
14	LED12	Output	Output of LED12 Driver
15	LED13	Output	Output of LED13 Driver
16	LED14	Output	Output of LED14 Driver
17	LED15	Output	Output of LED15 Driver
18	$\overline{RST}$	Input	Active Low Reset Input
19	SCL	Input	Clock Line for I^2C Interface
20	SDA	Input/Output	Serial Data Line for I^2C Interface
21	VDD	Power	Power Supply
22	A0	Input	Address Input 0
23	A1	Input	Address Input 1
24	A2	Input	Address Input 2
—	Exposed Pad	—	Tie internally to GND pin.

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5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1) (2) (3)

	MIN	MAX	UNIT
V_{DD}	–0.5	6	V
A0, A1, A2, SCL, SDA, $\overline{RST}$ (Collectively called digital pins)		6	V
Voltage on LED pins	V_{SS} − 0.5	6	V
Junction temperature		150	°C
Power dissipation(4)		400	mW
Storage temperature	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under セクション 5.3. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to the potential at the GND pin.
(3) If Military/Aerospace specified devices are required, contact the Texas Instruments Sales Office/ Distributors for availability and specifications.
(4) The part cannot dissipate more than 400 mW.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	
		Machine model	±200	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)(1) (2)

	MIN	NOM	MAX	UNIT
V_{DD}	2.3		5.5	V
Junction temperature	–40		125	°C
Operating ambient temperature	–40		85	°C

(1) *Absolute Maximum Ratings* are limits beyond which damage to the device might occur. *Recommended Operating Conditions* are conditions under which operation of the device is ensured. *Recommended Operating Conditions* do not imply ensured performance limits. For verified performance limits and associated test conditions, see セクション 5.5.
(2) All voltages are with respect to the potential at the GND pin.

5.4 Thermal Information

THERMAL METRIC(1)		LP3943 RTW (WQFN) 24 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	45.0	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	41.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	22.4	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.5	°C/W
ψ_{JB}	Junction-to-board characterization parameter	22.5	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	3.7	°C/W

(1) For more information about traditional and new thermal metrics, see *Semiconductor and IC Package Thermal Metrics*.

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5.5 Electrical Characteristics

Unless otherwise noted, V_{DD} = 5.5V. Typical values and limits apply for T_J = 25°C. Minimum and maximum limits apply over the entire junction temperature range for operation, T_J = −40°C to +125°C.(1)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLY						
V_{DD}	Supply voltage		2.3	5	5.5	V
I_Q	Supply current	No load		350	550	µA
		Standby		2	5	
ΔI_Q	Additional standby current	V_{DD} = 5.5V, every LED pin at 4.3V			2	mA
V_{POR}	Power-On Reset voltage			1.8	1.96	V
t_w	Reset pulse width			10		ns
LED						
V_{IL}	Low level input voltage		−0.5		0.8	V
V_{IH}	High level input voltage		2		5.5	V
I_{OL}	Low level output current(2)	V_{OL} = 0.4V, V_{DD} = 2.3V	9			mA
		V_{OL} = 0.4V, V_{DD} = 3V	12			
		V_{OL} = 0.4V, V_{DD} = 5V	15			
		V_{OL} = 0.7V, V_{DD} = 2.3V	15			
		V_{OL} = 0.7V, V_{DD} = 3V	20			
		V_{OL} = 0.7V, V_{DD} = 5V	25			
I_{LEAK}	Input leakage current	V_{DD} = 3.6V, V_{IN} = 0V or V_{DD}	−1		1	µA
$C_{I/O}$	Input/output capacitance	See(3)		2.6	5	pF
ALL DIGITAL PINS (EXCEPT SCL AND SDA PINS)						
V_{IL}	LOW level input voltage		−0.5		0.8	V
V_{IH}	HIGH level input voltage		2		5.5	V
I_{LEAK}	Input leakage current		−1		1	µA
C_{IN}	Input capacitance	V_{IN} = 0V(3)		2.3	5	pF
I²C INTERFACE (SCL AND SDA PINS)						
V_{IL}	LOW level input voltage		–0.5		$0.3V_{DD}$	V
V_{IH}	HIGH level input voltage		$0.7V_{DD}$		5.5	V
V_{OL}	LOW level output voltage		0		$0.2V_{DD}$	V
I_{OL}	LOW level output current	V_{OL} = 0.4V	3	6.5		mA
$I_{Q_SCL/SDA}$	SCL/SDA to VDD capable current			100		µA
f_{CLK}	Clock frequency				400	kHz

(1) Limits are ensured. All electrical characteristics having room-temperature limits are tested during production with T_J = 25°C. All hot and cold limits are ensured by correlating the electrical characteristics to process and temperature variations and applying statistical process control.
(2) Each LED pin must not exceed 25 mA and each octal (LED0–LED7; LED8–LED15) must not exceed 100 mA. The package must not exceed a total of 200 mA.
(3) Verified by design.

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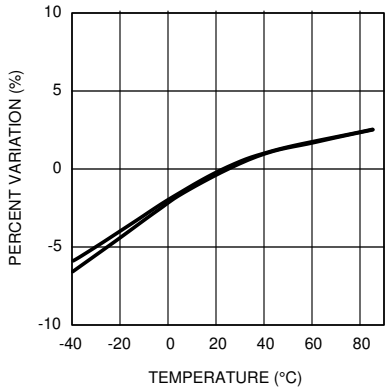
5.6 I²C Interface (SCL and SDA Pins) Timing Requirements

See(1)

		MIN	NOM	MAX	UNIT
t_{HOLD}	Hold time repeated START condition	0.6			µs
t_{CLK-LP}	CLK low period	1.3			µs
t_{CLK-HP}	CLK high period	0.6			µs
t_{SU}	Setup time repeated START condition	0.6			µs
$t_{DATA-HOLD}$	Data hold time	300			ns
$t_{DATA-SU}$	Data setup time	100			ns
t_{SU}	Setup time for STOP condition	0.6			µs
t_{TRANS}	Maximum pulse width of spikes that must be suppressed by the input filter of both DATA and CLK signals		50		ns

(1) All values verified by design.

5.7 Typical Characteristic



T_A = −40°C to +85°C V_{DD} = 2.3V to 3V

図 5-1. Frequency vs. Temperature

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6 Detailed Description

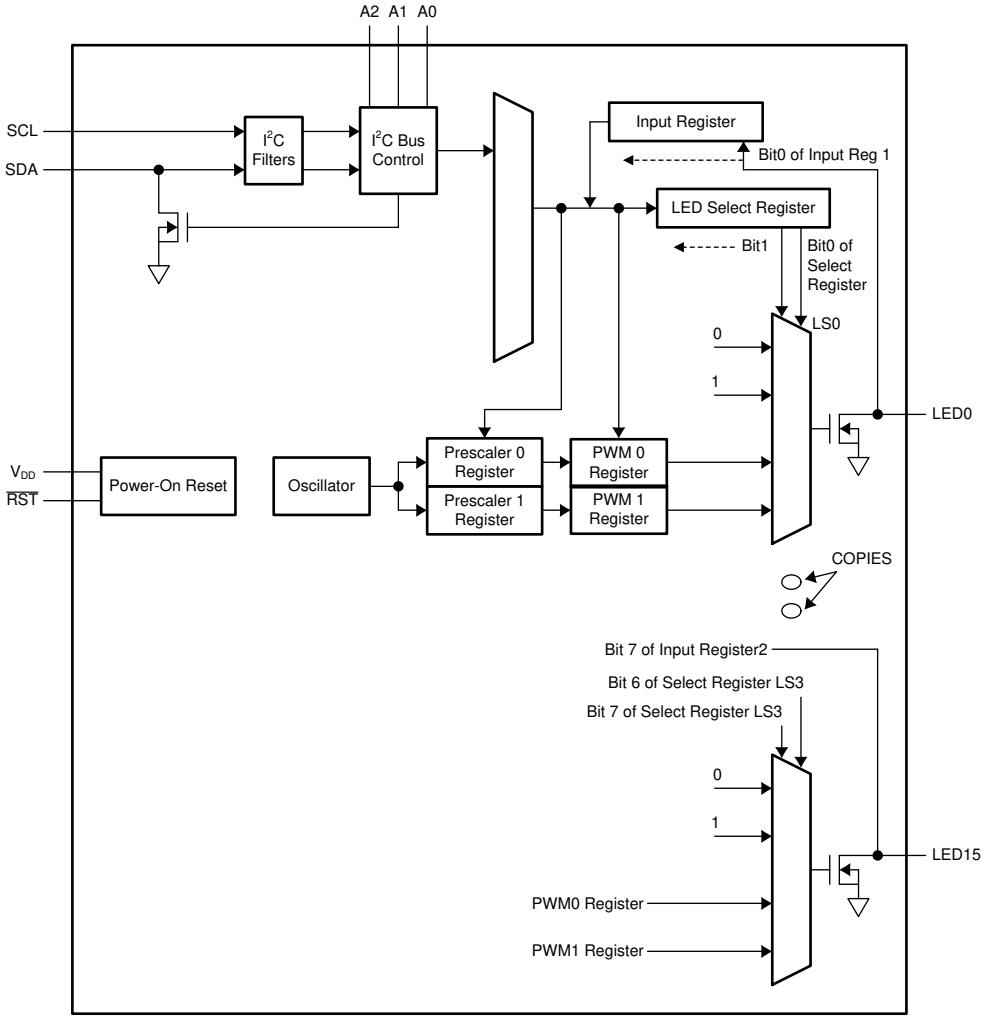
6.1 Overview

The LP3943 takes incoming data from the baseband controller and feeds them into several registers that control the frequency and the duty cycle of the LEDs. Two prescaler registers and two PWM registers provide two individual rates to dim or blink the LEDs (for more information on these registers, refer to 表 6-1). Each LED can be programmed in one of four states: ON, OFF, DIM0 rate, or DIM1 rate. Two read-only registers provide status on all 16 LEDs. The LP3943 can be used to drive RGB LEDs and/or single-color LEDs to create a colorful, entertaining, and informative setting. Alternatively, it can also drive RGB LED as a flashlight. This is particularly suitable for accessory functions in cellular phones and toys. Any LED pins not used to drive LED can be used for general purpose parallel input/output (GPIO) expansion.

The LP3943 is equipped with power-on reset that holds the chip in a reset state until V_{DD} reaches V_{POR} during power up. Once V_{POR} is achieved, the LP3943 comes out of reset and initializes itself to the default state.

To bring the LP3943 into reset, hold the $\overline{RST}$ pin LOW for a period of TW. This puts the chip into its default state. The LP3943 can only be programmed after $\overline{RST}$ signal is HIGH again.

6.2 Functional Block Diagram



6.3 Feature Description

Some of the features of the LP3943 device are:

1. 16 low-side switches to control the current in 16 strings of LEDs with a maximum of 25mA per switch or a maximum of 200mA total.
2. Programmable internal PWM dimming:
   a. Duty cycle control (8 bits). Any of the 16 current switches can be mapped to either PWM0 register or PWM1 register. Each register offers 8-bit PWM duty cycle control.
   b. PWM Frequency control (8 bits). Any of the 16 current switches can be mapped to either PSC0 register or PSC1 register. Each register offers 8-bit PWM frequency control from 0.625Hz to 160Hz.
3. $\overline{\text{RESET}}$ input.
4. Auto increment for I2C writes to reduce number of I2C clock pulses .
5. The LP3943 provides for an externally selectable I2C slave address via the ADR0, ADR1, and ADR2 inputs. See 図 6-3.

6.4 Device Functional Modes

1. Output set to high impedance. This is set by programming bits [B0 and B1] to 00 in the LS0, LS1, LS2, or LS3 registers (see Table 2)
2. Output set to ON state (current switch pulls low). This turns the LED on at the full current in the specified current switch bits [B0 and B1] set to 01 in the LS0, LS1, LS2, or LS3 registers (see 表 6-12).
3. Output set to toggle at the programmed PWM duty cycle and PWM frequency. This turns on or off the specified current switch at the programmed PWM frequency and duty cycle. Each current switch is mapped to either of the PWM0/PSC0 or PWM1/PSC1 pairs by setting [B0 and B1] to 10 or 11 in the LS0, LS1, LS2, or LS3 registers (see 表 6-12).

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6.5 Programming

6.5.1 I²C Data Validity

The data on SDA line must be stable during the HIGH period of the clock signal (SCL). In other words, state of the data line can only be changed when CLK is LOW.

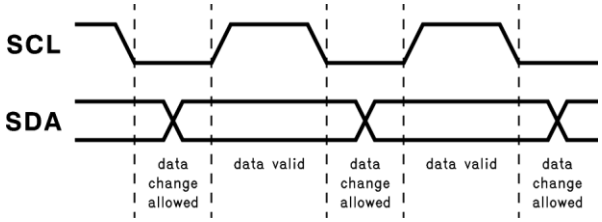


図 6-1. I²C Data Validity

6.5.2 I²C START and STOP Conditions

START and STOP bits classify the beginning and the end of the I²C session. START condition is defined as SDA signal transitioning from HIGH to LOW while SCL line is HIGH. STOP condition is defined as the SDA transitioning from LOW to HIGH while SCL is HIGH. The I²C master always generates START and STOP bits. The I²C bus is considered to be busy after START condition and free after STOP condition. During data transmission, I²C master can generate repeated START conditions. First START and repeated START conditions are equivalent, function-wise.

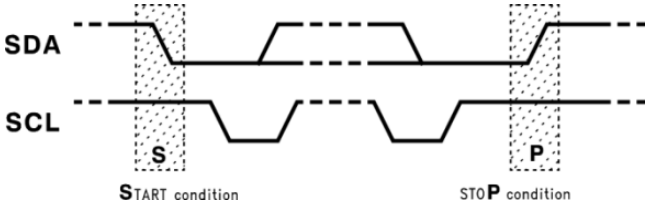


図 6-2. I²C START and STOP Conditions

6.5.3 Transferring Data

Every byte put on the SDA line must be eight bits long with the most significant bit (MSB) being transferred first. The number of bytes that can be transmitted per transfer is unrestricted. Each byte of data has to be followed by an acknowledge bit. The acknowledge related clock pulse is generated by the master. The transmitter releases the SDA line (HIGH) during the acknowledge clock pulse. The receiver must pull down the SDA line during the 9th clock pulse, signifying an acknowledge. A receiver which has been addressed must generate an acknowledge after each byte has been received.

After the START condition, a chip address is sent by the I²C master. This address is seven bits long followed by an eighth bit which is a data direction bit (R/W). The LP3943 hardwires bits 7 to 4 and leaves bits 3 to 1 selectable, as shown in 図 6-3. For the eighth bit, a 0 indicates a WRITE and a 1 indicates a READ. The LP3943 supports only a WRITE during chip addressing. The second byte selects the register to which the data is written. The third byte contains data to write to the selected register.

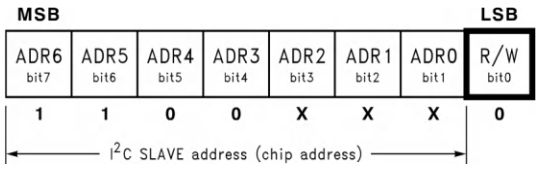
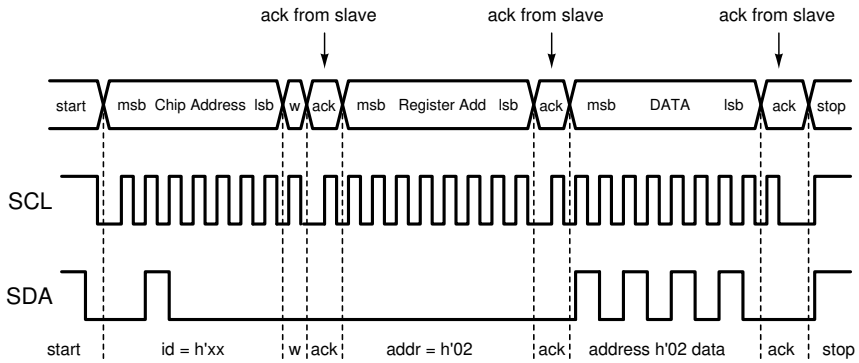


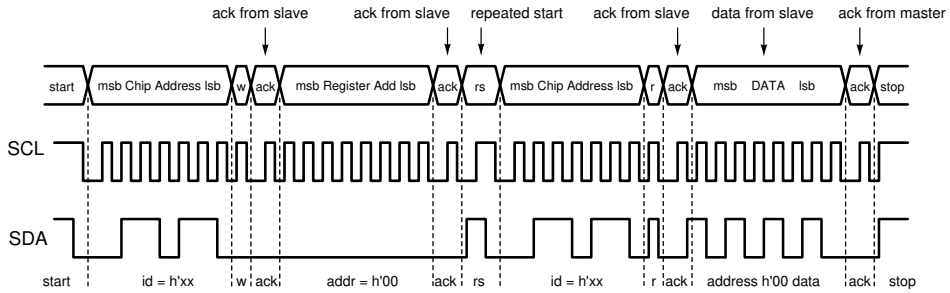
図 6-3. Chip Address Byte



w = write (SDA = 0) r = read (SDA = 1) ack = acknowledge (SDA pulled LOW by either master or slave) rs = repeated start xx = 60 to 67

図 6-4. LP3943 Register Write

However, if a READ function is to be accomplished, a WRITE function must precede the READ function, as shown in 図 6-5.



w = write (SDA = “0”) r = read (SDA = “1”) ack = acknowledge (SDA pulled LOW by either master or slave) rs = repeated start xx = 60 to 67

図 6-5. LP3943 Register Read

6.5.4 Auto Increment

Auto increment is a special feature supported by the LP3943 to eliminate repeated chip and register addressing when data are to be written to or read from registers in sequential order. The auto increment bit is inside the register address byte, as shown in 図 6-6. Auto increment is enabled when this bit is programmed to “1” and disabled when it is programmed to “0”.

Bits 5, 6 and 7 in the register address byte must always be zero.

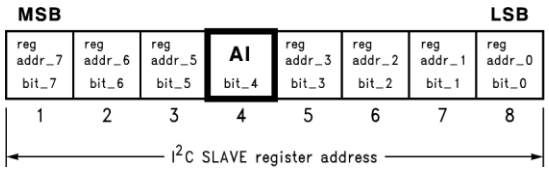


図 6-6. Register Address Byte

In the READ mode, when auto increment is enabled, I^2C master could receive any number of bytes from LP3943 without selecting chip address and register address again. Every time the I^2C master reads a register, the LP3943 increments the register address, and the next data register is read. When I^2C master reaches the last register (09H), the register address rolls over to 00H.

In the WRITE mode, when auto increment is enabled, the LP3943 increments the register address every time I^2C master writes to register. When the last register (09H register) is reached, the register address rolls over to

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02H, not 00H, because the first two registers in LP3943 are read-only registers. It is possible to write to the first two registers independently, and the LP3943 device will acknowledge, but the data is ignored.

If auto increment is disabled, and the I^{2}C master does not change register address, it continues to write data into the same register.

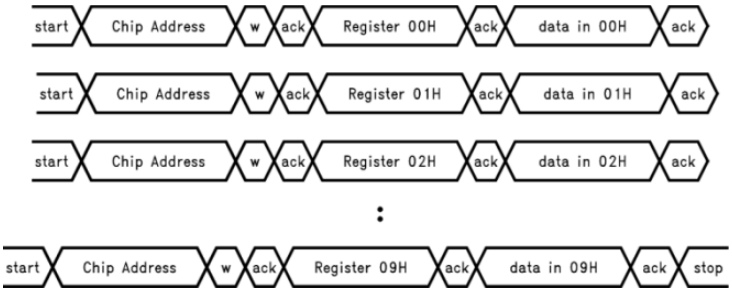

図 6-7. Programming With Auto Increment Disabled (in WRITE Mode)

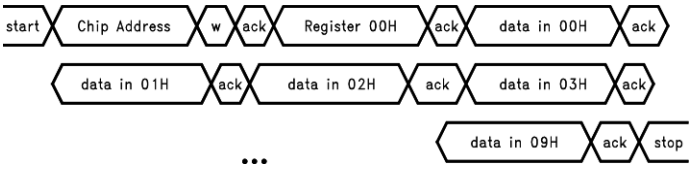

図 6-8. Programming With Auto Increment Enabled (in WRITE Mode)

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6.6 Register Maps

表 6-1. LP3943 Register Table

Address (Hex)	Register Name	Read/Write	Register Function
0x00	Input 1	Read Only	LED0–7 Input Register
0x01	Input 2	Read Only	LED8–15 Input Register
0x02	PSC0	R/W	Frequency Prescaler 0
0x03	PWM0	R/W	PWM Register 0
0x04	PSC1	R/W	Frequency Prescaler 1
0x05	PWM1	R/W	PWM Register 1
0x06	LS0	R/W	LED0–3 Selector
0x07	LS1	R/W	LED4–7 Selector
0x08	LS2	R/W	LED8–11 Selector
0x09	LS3	R/W	LED12–15 Selector

6.6.1 Binary Format for Input Registers (Read-only)—Address 0x00 and 0x01

表 6-2. Address 0x00

Bit #	7	6	5	4	3	2	1	0
Default value	X	X	X	X	X	X	X	X
	LED7	LED6	LED5	LED4	LED3	LED2	LED1	LED0

表 6-3. Address 0x01

Bit #	7	6	5	4	3	2	1	0
Default value	X	X	X	X	X	X	X	X
	LED15	LED14	LED13	LED12	LED11	LED10	LED9	LED8

6.6.2 Binary Format for Frequency Prescaler and PWM Registers — Address 0x02 to 0x05

表 6-4. Address 0x02 (PSC0)

Bit #	7	6	5	4	3	2	1	0
Default value	0	0	0	0	0	0	0	0

表 6-5. Address 0x03 (PWM0)

Bit #	7	6	5	4	3	2	1	0
Default value	1	0	0	0	0	0	0	0

表 6-6. Address 0x04 (PSC1)

Bit #	7	6	5	4	3	2	1	0
Default value	0	0	0	0	0	0	0	0

表 6-7. Address 0x05 (PWM1)

Bit #	7	6	5	4	3	2	1	0
Default value	1	0	0	0	0	0	0	0

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6.6.3 Binary Format for Selector Registers — Address 0x06 to 0x09

表 6-8. Address 0x06 (LS0)

Bit #	7	6	5	4	3	2	1	0
Default value	0	0	0	0	0	0	0	0
	B1	B0	B1	B0	B1	B0	B1	B0
	LED3		LED2		LED1		LED0	

表 6-9. Address 0x07 (LS1)

Bit #	7	6	5	4	3	2	1	0
Default value	0	0	0	0	0	0	0	0
	B1	B0	B1	B0	B1	B0	B1	B0
	LED7		LED6		LED5		LED4	

表 6-10. Address 0x08 (LS2)

Bit #	7	6	5	4	3	2	1	0
Default value	0	0	0	0	0	0	0	0
	B1	B0	B1	B0	B1	B0	B1	B0
	LED11		LED10		LED9		LED8	

表 6-11. Address 0x09 (LS3)

Bit #	7	6	5	4	3	2	1	0
Default value	0	0	0	0	0	0	0	0
	B1	B0	B1	B0	B1	B0	B1	B0
	LED15		LED14		LED13		LED12	

表 6-12. LED States With Respect To Values in B1 and B0

B1	B0	Function
0	0	Output Hi-Z (LED off)
0	1	Output LOW (LED on)
1	0	Output dims (DIM0 rate)
1	1	Output dims (DIM1 rate)

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Programming Example:

- Dim LEDs 0 to 7 at 1Hz at 25% duty cycle
- Dim LEDs 8 to 12 at 5Hz at 50% duty cycle
- Set LEDs 13, 14 and 15 off
- Step 1: Set PSC0 to achieve DIM0 of 1 s
- Step 2: Set PWM0 duty cycle to 25%
- Step 3: Set PSC1 to achieve DIM1 of 0.2 s
- Step 4: Set PWM1 duty cycle to 50%
- Step 5: Set LEDs 13, 14 and 15 off by loading the data into LS3 register
- Step 6: Set LEDs 0 to 7 to point to DIM0
- Step 7: Set LEDs 8 to 12 to point to DIM1

表 6-13. Programming Details

STEP	DESCRIPTION	REGISTER NAME	SET TO (HEX)
1	Set DIM0 = 1 s 1 = (PSC0 + 1)/160 PSC0 = 159	PSC0	0x09F
2	Set duty cycle to 25% Duty Cycle = PWM0/256 PWM0 = 64	PWM0	0x40
3	Set DIM1 = 0.2s 0.2 = (PSC1 + 1)/160 PSC1 = 31	PSC1	0x1F
4	Set duty cycle to 50% Duty Cycle = PWM1/256 PWM1 = 128	PWM1	0x80
5	LEDs 13, 14 and 15 off Output = HIGH	LS3	0x03
6	LEDs 0 to 7 Output = DIM0	LS0, LS1	LS0 = 0xAA LS1 = 0xAA
7	LEDs 8 to 12 Output = DIM1	LS2, LS3	LS2 = 0xFF LS3 = 0x03

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Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

1 Application Information

The LP3943 is a 16-channel LED controller which has 16 low-side current switches. Each switch can control the LED current in its respective LED or LEDs by modulating its duty cycle and frequency.

2 Typical Application

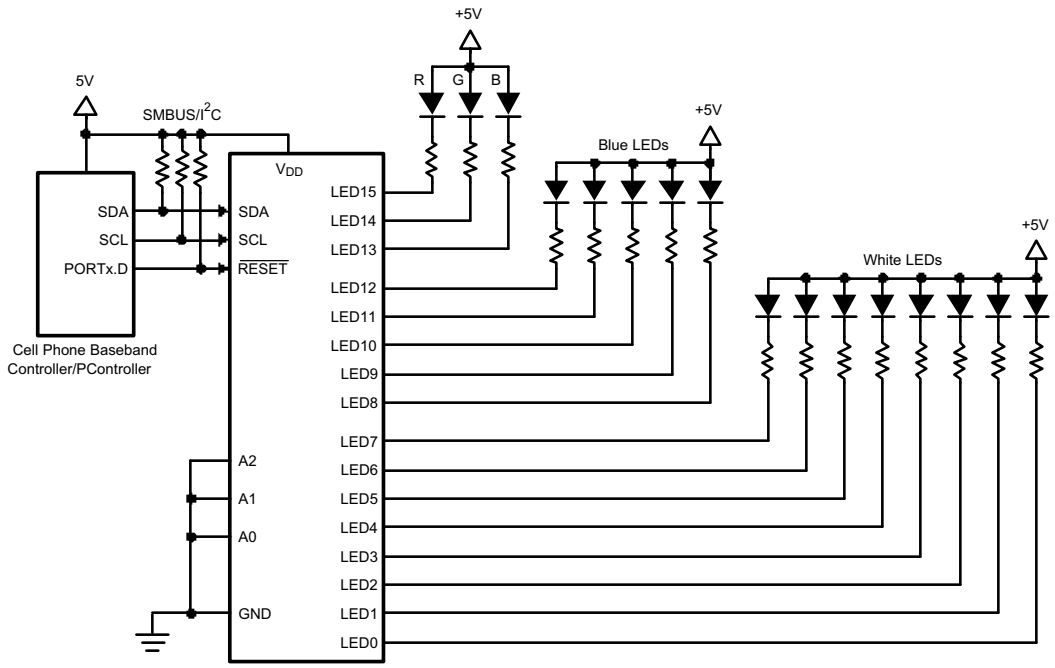

図 7-1. LP3943 Typical Application

2.1 Design Requirements

For typical RGB LED light-driver applications, use the parameters listed in 表 7-1.

表 7-1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Minimum input voltage	2.3 V
Typical output voltage	5 V
Output current	20 mA

2.2 Detailed Design Procedure

2.2.1 Reducing I_Q When LEDs are OFF

In many applications, the LEDs and the LP3943 share the same V_{DD}, as shown in 図 7-1. When the LEDs are off, the LED pins are at a lower potential than V_{DD}, causing extra supply current (ΔI_Q). To minimize this current, consider keeping the LED pins at a voltage equal to or greater than V_{DD}.

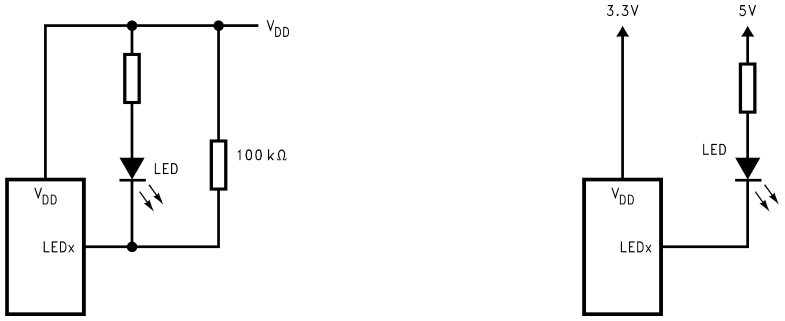

図 7-2. Methods to Reduce I_Q When LEDs are in OFF State

2.3 Application Curve

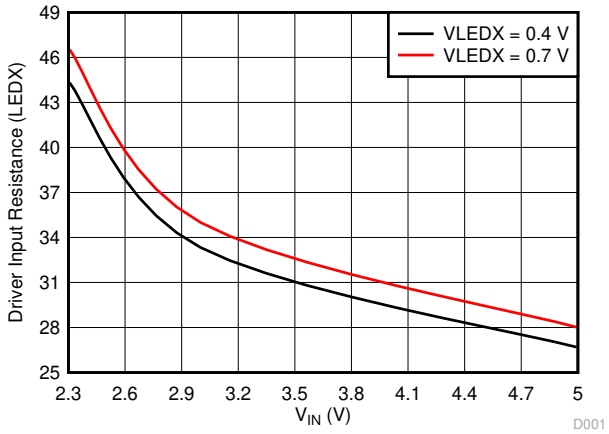

図 7-3. Typical LED Switch Resistance

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3 System Examples

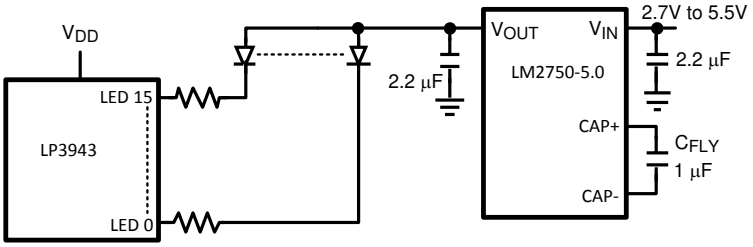

図 7-4. LP3943 With 5V Booster

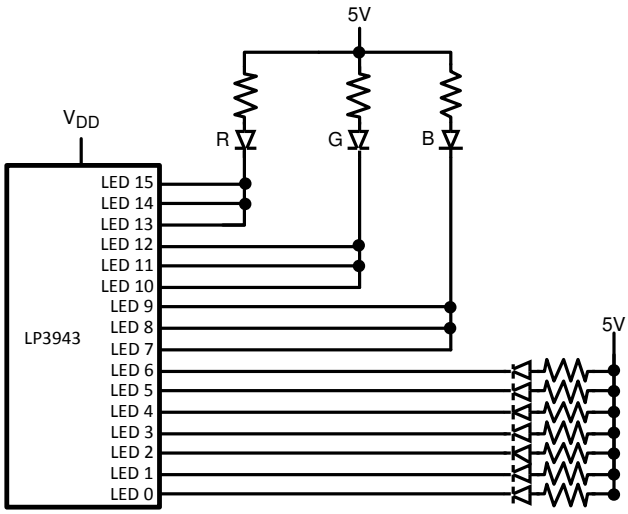

図 7-5. LP3943 Driving RGB LED as a Flash

4 Power Supply Recommendations

The LP3943 is designed to be powered from a 2.3V minimum to a 5.5V maximum supply input.

5 Layout

5.1 Layout Guidelines

The LP3943 layout is not critical, but TI recommends providing a noise-free supply input at V_{DD}. This typically would require a 1µF capacitor placed close to the VDD pin and ground.

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5.2 Layout Example

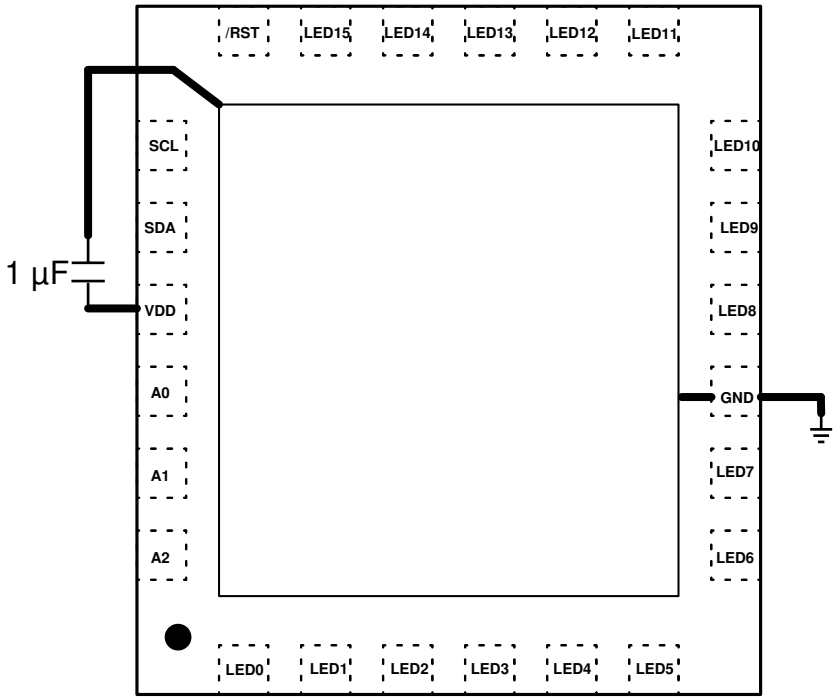

図 7-6. LP3943 Layout Example

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7 Device and Documentation Support

7.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

7.2 Community Resources

7.3 Trademarks

すべての商標は、それぞれの所有者に帰属します。

8 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision D (October 2016) to Revision E (October 2024)	Page
• Added SCL/SDA to VDD capable current parameter to the Electrical Characteristics table	4

Changes from Revision C (October 2015) to Revision D (October 2016)	Page
• SEO キーワードを追加するためにタイトルの表現を変更	1
• Changed $R_{\theta JA}$ value from "37°C/W" to "45.0°C/W"; add additional thermal values	4

Changes from Revision B (September 2013) to Revision C (October 2015)	Page
• 「製品情報」セクション、「ピン構成および機能」セクション、「ESD 定格」表、「機能説明」セクション、「デバイスの機能モード」セクション、「アプリケーションと実装」セクション、「電源に関する推奨事項」セクション、「レイアウト」セクション、「デバイスおよびドキュメントのサポート」セクション、「メカニカル、パッケージ、および注文情報」セクションを追加	1

Changes from Revision A (April 2013) to Revision B (September 2013)	Page
• Changed layout of National Data Sheet to TI format; fixed format of Block Diagram	7

Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LP3943ISQ	Obsolete	Production	WQFN (RTW) | 24	-	-	Call TI	Call TI	-40 to 85	3943SQ
LP3943ISQ/NOPB	Active	Production	WQFN (RTW) | 24	1000 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	3943SQ
LP3943ISQ/NOPB.A	Active	Production	WQFN (RTW) | 24	1000 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	3943SQ
LP3943ISQX/NOPB	Active	Production	WQFN (RTW) | 24	4500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	3943SQ
LP3943ISQX/NOPB.A	Active	Production	WQFN (RTW) | 24	4500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	3943SQ

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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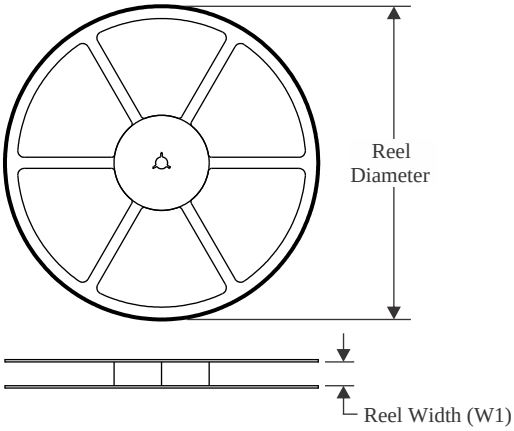
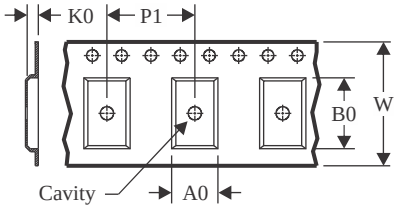
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

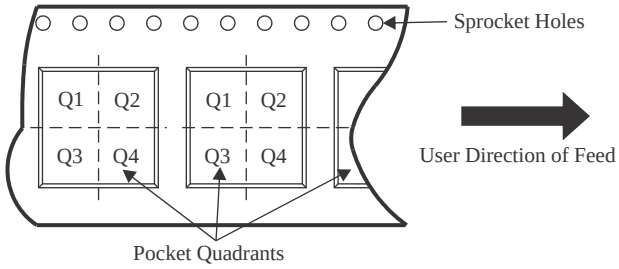


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

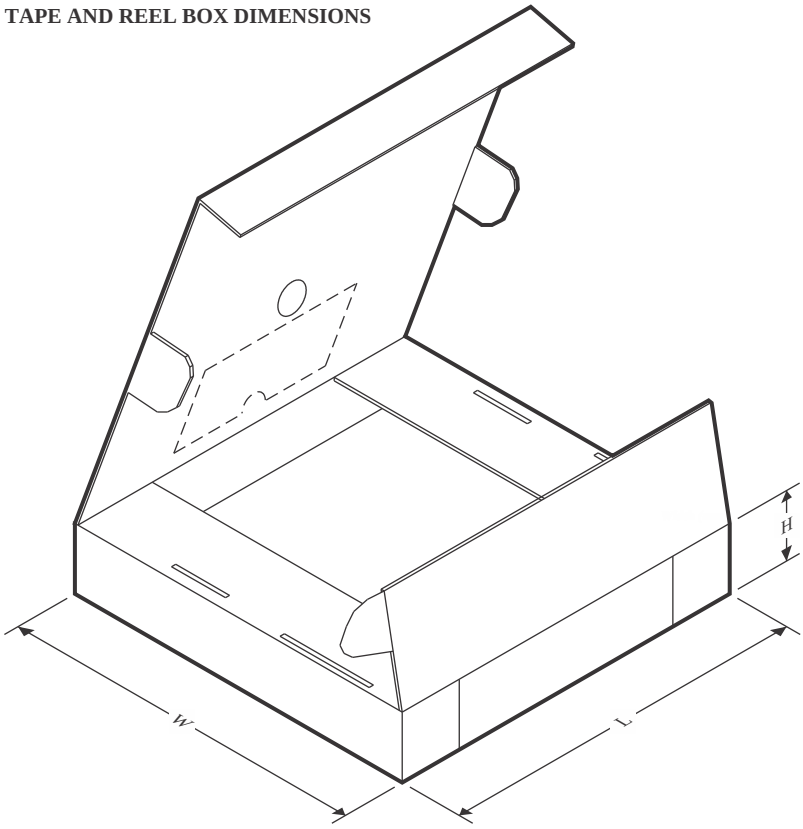
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LP3943ISQ/NOPB	WQFN	RTW	24	1000	177.8	12.4	4.3	4.3	1.3	8.0	12.0	Q1
LP3943ISQX/NOPB	WQFN	RTW	24	4500	330.0	12.4	4.3	4.3	1.3	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

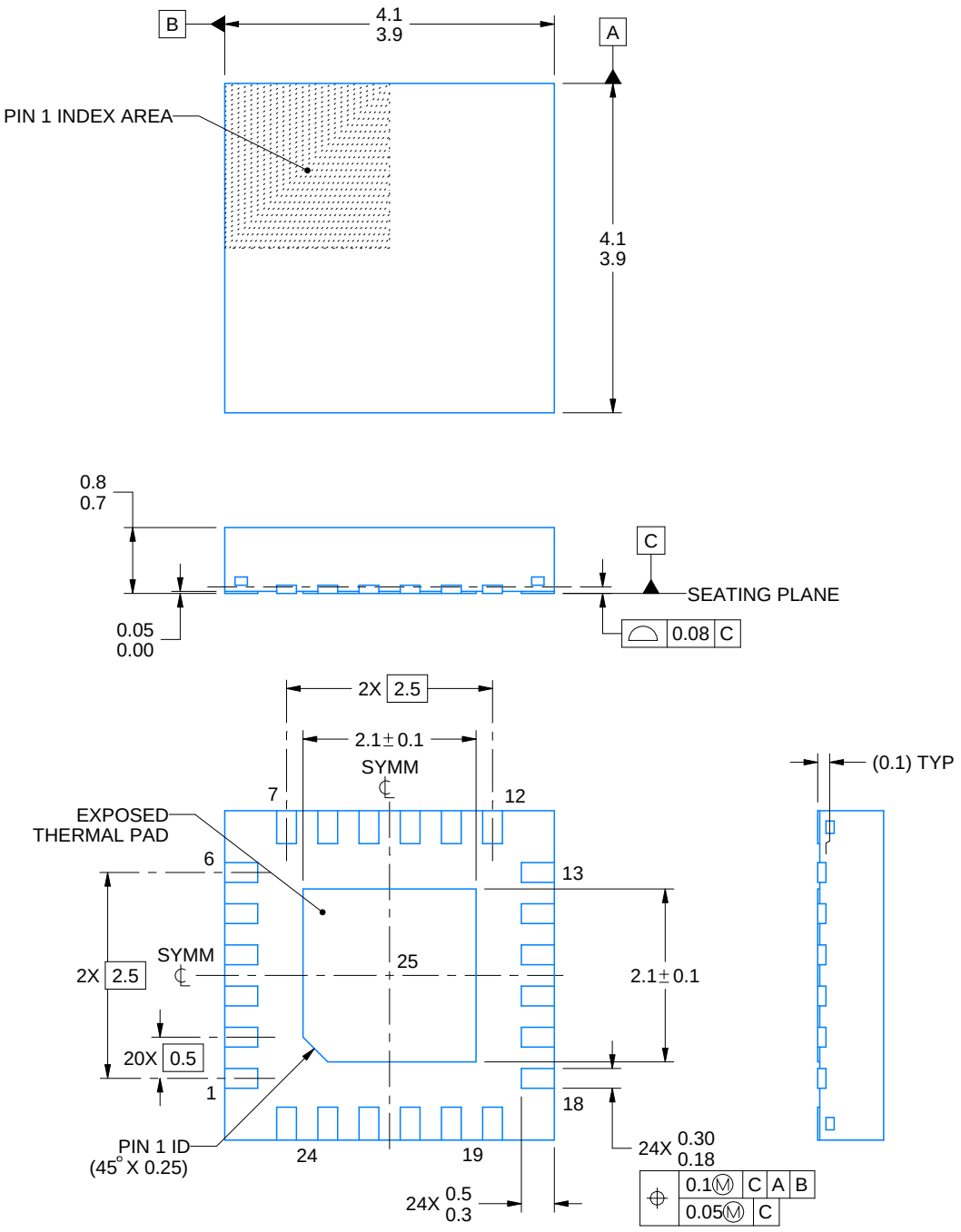
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LP3943ISQ/NOPB	WQFN	RTW	24	1000	208.0	191.0	35.0
LP3943ISQX/NOPB	WQFN	RTW	24	4500	367.0	367.0	35.0

PACKAGE OUTLINE

RTW0024C

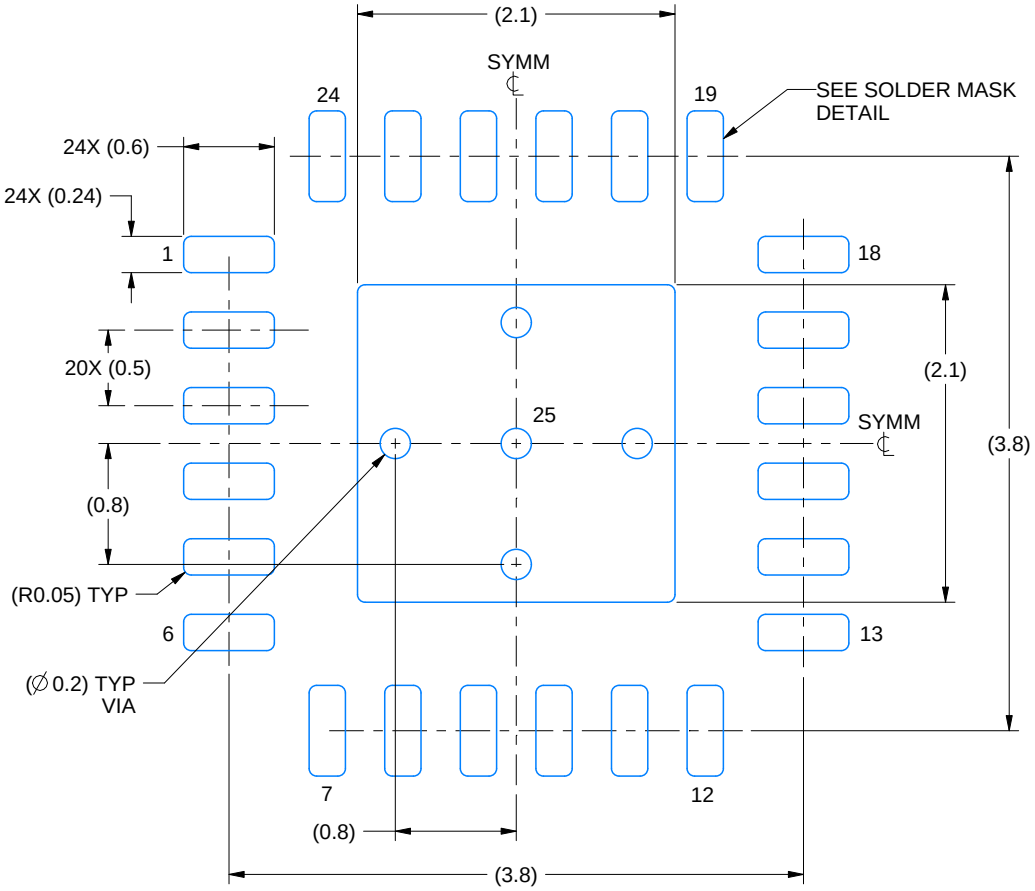
WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

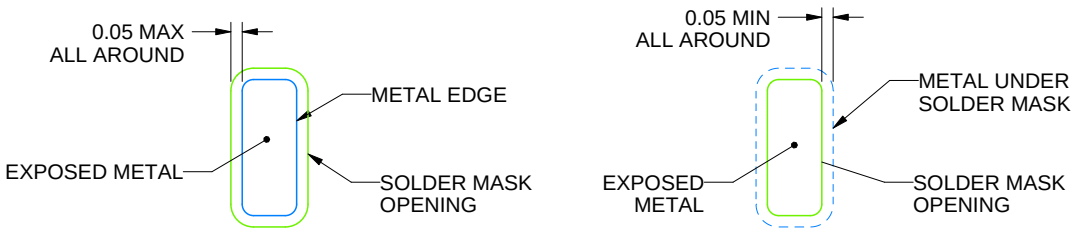


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X



SOLDER MASK DETAILS

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NOTES: (continued)

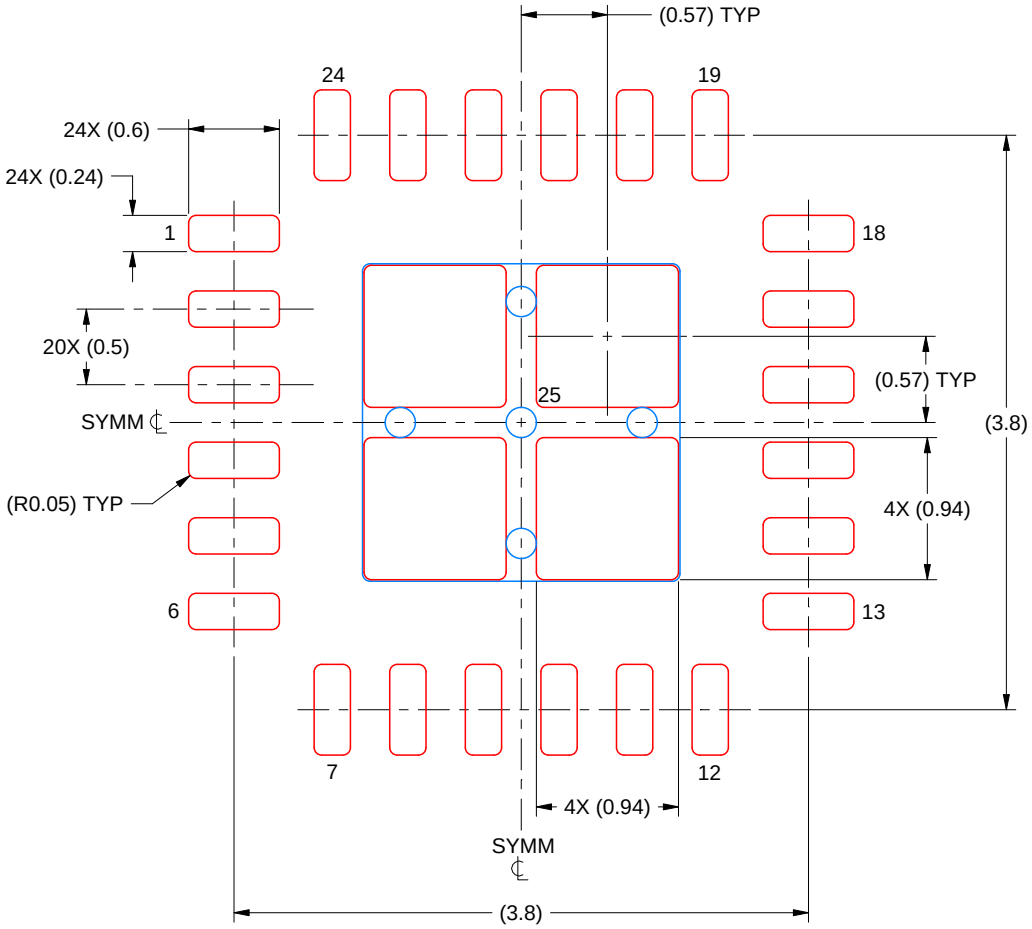
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

RTW0024C

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 20X

EXPOSED PAD 25
80% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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最終更新日：2025 年 10 月