LV5144 95V、デューティ・サイクル範囲の広い同期整流降圧 DC/DC コントローラ

1 特長

- – デバイス温度グレード 1:-40℃～+125℃の周囲温度範囲
- 多用途の同期整流式降圧 DC/DC コントローラ
  - 6V～95V の広い入力電圧範囲
  - 接合部温度:125℃ (最大値)
  - フィードバック精度 ±1% の 0.8V 基準電圧
  - 0.8V～60V の可変出力電圧
  - 45ns の $t_{ON(min)}$ により高い V_{IN}/V_{OUT} 比を実現
  - 145ns の $t_{OFF(min)}$ により低ドロップアウトを実現
  - ロスレス $R_{DS(on)}$ またはシャント電流センシング
  - CISPR 11 および CISPR 32 Class B EMI 要件に対して最適化
- 100kHz～1MHz のスイッチング周波数
  - SYNC In および SYNC Out 機能
  - ダイオード・エミュレーションまたは FPWM を選択可能
- 標準の V_{TH} MOSFET 用の 7.5V ゲート・ドライバ
  - 14ns のアダプティブ・デッドタイム制御
  - 2.3A ソースおよび 3.5A シンク能力
- 本質的な保護機能による堅牢な設計
  - 可変出力電圧ソフト・スタート
  - ヒカップ・モードによる過電流保護
  - ヒステリシス付きの入力 UVLO
  - VCC とゲート駆動の UVLO 保護
  - 高精度のイネーブル入力とオープン・ドレインの PGOOD インジケータによるシーケンシングと制御
  - ヒステリシス付きのサーマル・シャットダウン保護
- 20 ピンのウェッタブル・フランク付き VQFN パッケージ

2 アプリケーション

- 無線インフラストラクチャ、クラウド・コンピューティング
- 産業用モータ駆動、試験 / 測定機器
- 個人用移動車両:電動バイク
- アセット追跡およびフリート管理システム
- 非絶縁型 PoE、IP カメラ
- 反転型昇降圧レギュレータ

3 概要

LV5144 95-V 同期整流降圧コントローラは、高い入力電圧の電源、または高い過渡電圧が発生する入力レールからのレギュレーションを行い、外部のサージ抑制コンポーネントの必要性を最小限に抑えます。ハイサイド・スイッチの最小のオン時間は 45ns で、大きな降圧率を使用できるため、48V 公称入力から低電圧レールへの直接降圧変換が可能になり、システムの複雑性と設計コストを下げることができます。LV5144 は最低 6V の入力電圧ディップ中も動作し、必要に応じて 100% に近いデューティ・サイクルで動作するため、高性能の産業用制御、ロボット、データ通信、RF アプリケーションに理想的です。

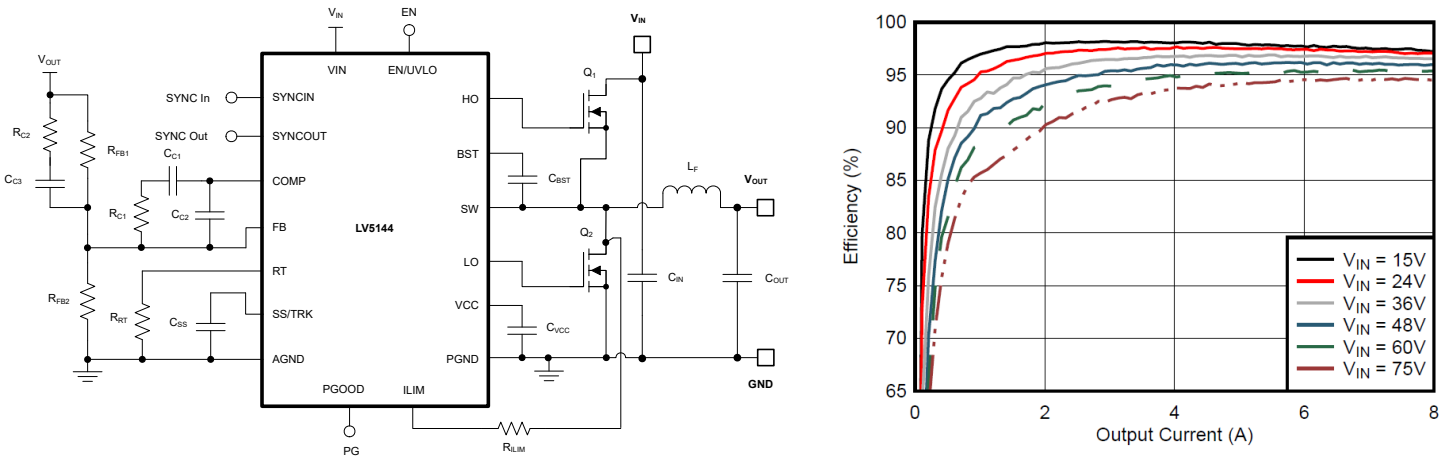
強制 PWM (FPWM) 動作によりスイッチング周波数変動が排除され、EMI が最小化されます。また、ユーザー選択のダイオード・エミュレーション機能により軽負荷の状況で消費電流が抑えられます。スイッチング周波数は最高 1MHz まで設定可能で、外部クロック・ソースと同期できるため、ノイズに敏感なアプリケーションでビート周波数を排除できます。

パッケージ情報

部品番号	パッケージ (1)	パッケージ・サイズ (2)
LV5144	RGY (VQFN、20)	4.50mm × 3.50mm

(1) 利用可能なすべてのパッケージについては、データシートの末尾にある注文情報を参照してください。
(2) パッケージ・サイズ (長さ×幅) は公称値であり、該当する場合はピンも含まれます。

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代表的なアプリケーション回路と効率特性、V_{OUT} = 12V、F_{SW} = 400kHz

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4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

DATE	REVISION	NOTES
August 2023	*	Initial Release

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5 概要 (続き)

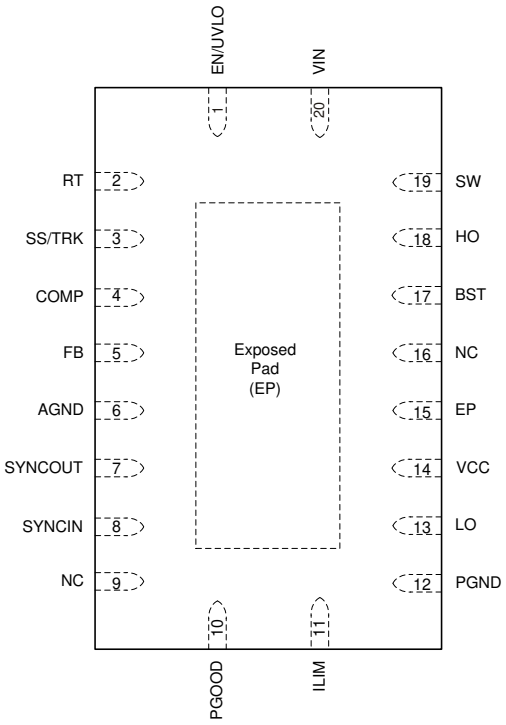
LV5144 ライン・フィードフォワード付き電圧モード・コントローラは、外部のハイサイドおよびローサイド N チャネル電力スイッチを、標準スレッショルドの MOSFET に適した、堅牢な 7.5V のゲート・ドライバで駆動します。適応型タイミングのゲート・ドライバと、ソース 2.3A、シンク 3.5A の能力から、スイッチング遷移時にボディ・ダイオードの導通が最小化され、スイッチング損失が低減し、高い入力電圧と高周波数で MOSFET を駆動するときの熱特性が改善されます。LV5144 はスイッチング・レギュレータの出力、または他の利用可能な電源で駆動できるため、さらに効率が向上します。

SYNCOUT での、内部発振器に対して 180° 位相がずれたクロック出力は、カスケードまたはマルチチャネルの電源で入力コンデンサのリップル電流と EMI フィルタのサイズを減らすため理想的です。LV5144 の追加機能として、構成可能なソフト・スタート、フォルト報告および出力監視用のオープン・ドレインのパワー・グッド・モニタ、プリバイアス負荷への単調スタートアップ、VCC バイアス電源レギュレータおよびブートストラップ・ダイオードの搭載、外部電源のトラッキング、可変のライン低電圧誤動作防止 (UVLO) を行うための高精度のヒステリシス付きイネーブル入力、ヒカップ・モードの過負荷保護、自動回復機能付きのサーマル・シャットダウン保護があります。

LV5144 コントローラは 4.5mm × 3.5mm の熱的に強化された 20 ピンの VQFN パッケージで供給され、高電圧ピンには追加のスペースを設け、ウェッタブル・フランクを採用してハンダ接合部フィレットの光学検査を容易に行えます。

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6 Pin Configuration and Functions



Connect Exposed Pad on bottom to AGND and PGND on the PCB.

図 6-1. 20-Pin VQFN With Wettable Flanks in RGY Package (Top View)

表 6-1. Pin Functions

PIN		I/O(1)	DESCRIPTION
NO.	NAME		
1	EN/UVLO	I	Enable input and undervoltage lockout programming pin. If the EN/UVLO voltage is below 0.4 V, the controller is in shutdown mode with all functions disabled. If the EN/UVLO voltage is greater than 0.4 V and less than 1.2 V, the regulator is in standby mode with the VCC regulator operational, the SS pin grounded, and no switching at the HO and LO outputs. If the EN/UVLO voltage is above 1.2 V, the SS/TRK voltage can ramp and pulse-width modulated gate-drive signals are delivered to the HO and LO pins. A 10-µA current source is enabled when EN/UVLO exceeds 1.2 V and flows through the external UVLO resistor divider to provide hysteresis. Hysteresis can be adjusted by varying the resistance of the external divider.
2	RT	I	Oscillator frequency adjust pin. The internal oscillator is programmed with a single resistor between RT and the AGND. TI recommends a maximum oscillator frequency of 1 MHz. An RT pin resistor is required even when using the SYNCIN pin to synchronize to an external clock.
3	SS/TRK	I	Soft start and voltage-tracking pin. An external capacitor and an internal 10-µA current source set the ramp rate of the error amplifier reference during start-up. When the SS/TRK pin voltage is less than 0.8 V, the SS/TRK voltage controls the noninverting input of the error amp. When the SS/TRK voltage exceeds 0.8 V, the amplifier is controlled by the internal 0.8-V reference. SS/TRK is discharged to ground during standby and fault conditions. After start-up, the SS/TRK voltage is clamped 115 mV above the FB pin voltage. If FB falls due to a load fault, SS/TRK is discharged to a level 115 mV above FB to provide a controlled recovery when the fault is removed. Voltage tracking can be implemented by connecting a low impedance reference between 0 V and 0.8 V to the SS/TRK pin. The 10-µA SS/TRK charging current flows into the reference and produces a voltage error if the impedance is not low. Connect a minimum capacitance from SS/TRK to AGND of 2.2 nF.
4	COMP	O	Low impedance output of the internal error amplifier. Connect the loop compensation network between the COMP pin and the FB pin.
5	FB	I	Feedback connection to the inverting input of the internal error amplifier. A resistor divider from the output to this pin sets the output voltage level. The regulation threshold at the FB pin is nominally 0.8 V.
6	AGND	P	Analog ground. Return for the internal 0.8-V voltage reference and analog circuits.

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表 6-1. Pin Functions (continued)

PIN		I/O(1)	DESCRIPTION
NO.	NAME		
7	SYNCOUT	O	Synchronization output. Logic output that provides a clock signal that is 180° out-of-phase with the high-side FET gate drive. Connect SYNCOUT of the primary LV5144 to the SYNCIN pin of a second LV5144 to operate two controllers at the same frequency with 180° interleaved high-side FET switch turn-on transitions. Note that the SYNCOUT pin does not provide 180° interleaving when the controller is operating from an external clock that is different from the free-running frequency set by the RT resistor.
8	SYNCIN	I	Dual function pin to provide an optional clock input and enable diode emulation by the low-side MOSFET. Connecting a clock signal to the SYNCIN pin synchronizes switching to the external clock. Diode emulation by the low-side MOSFET is disabled when the controller is synchronized to an external clock, and negative inductor current can flow in the low-side MOSFET with light loads. A continuous logic low state at the SYNCIN pin enables diode emulation to prevent reverse current flow in the inductor. Diode emulation results in discontinuous mode operation (DCM) at light loads, which improves efficiency. A logic high state at the SYNCIN pin disables diode emulation, producing forced-PWM (FPWM) operation. During soft start when SYNCIN is high or a clock signal is present, the LV5144 operates in diode emulation mode until the output is in regulation, then gradually increases the SW zero-cross threshold, resulting in a gradual transition from DCM to FPWM.
9	NC	—	No electrical connection
10	PGOOD	O	Power-good indicator. This pin is an open-drain output. A high state indicates that the voltage at the FB pin is within a specified tolerance window centered at 0.8 V.
11	ILIM	I	Current limit adjust and current sense comparator input. A current sourced from the ILIM pin through an external resistor programs the threshold voltage for valley current limiting. The opposite end of the threshold adjust resistor can be connected to either the drain of the low-side MOSFET for $R_{DS(on)}$ sensing or to a current sense resistor connected to the source of the low-side FET.
12	PGND	P	Power ground return pin for the low-side MOSFET gate driver. Connect directly to the source of the low-side MOSFET or the ground side of a shunt resistor.
13	LO	P	Low-side MOSFET gate drive output. Connect to the gate of the low-side synchronous rectifier FET through a short, low inductance path.
14	VCC	O	Output of the 7.5-V bias regulator. Locally decouple to PGND using a low-ESR/ESL capacitor located as close as possible to the controller. Controller bias can be supplied from an external supply that is greater than the internal VCC regulation voltage. Use caution when applying external bias to ensure that the applied voltage is not greater than the minimum V_{IN} voltage and does not exceed the VCC pin maximum operating rating. See the *Recommended Operating Conditions*.
15	EP	—	Pin is internally connected to exposed pad of the package. Connect to GND at the exposed pad to improve heat spreading.
16	NC	—	No electrical connection
17	BST	O	Bootstrap supply for the high-side gate driver. Connect to the bootstrap (boot) capacitor. The bootstrap capacitor supplies current to the high-side FET gate and must be placed as close as possible to controller. If an external bootstrap diode is used to reduce the time required to charge the bootstrap capacitor, connect the cathode of the diode to the BST pin and anode to VCC.
18	HO	P	High-side MOSFET gate drive output. Connect to the gate of the high-side MOSFET through a short, low inductance path.
19	SW	P	Switching node of the buck controller. Connect to the bootstrap capacitor, the source terminal of the high-side MOSFET, and the drain terminal of the low-side MOSFET using short, low inductance paths.
20	VIN	P	Supply voltage input for the VCC LDO regulator
—	EP	—	Exposed pad of the package. Electrically isolated. Solder to the system ground plane to reduce thermal resistance.

(1) P = Power, G = Ground, I = Input, O = Output

6.1 Wettable Flanks

100% automated visual inspection (AVI) post-assembly is typically required to meet requirements for high reliability and robustness. Standard quad-flat no-lead (VQFN) packages do not have solderable or exposed pins and terminals that are easily viewed. Therefore, visually determining whether or not the package is successfully soldered onto the printed-circuit board (PCB) is difficult. The wettable-flank process was developed to resolve the issue of side-lead wetting of leadless packaging. The LV5144 is assembled using a 20-pin VQFN package with wettable flanks to provide a visual indicator of solderability, which reduces the inspection time and manufacturing costs.

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7 Specifications

7.1 Absolute Maximum Ratings

Over the recommended operating junction temperature range of –40°C to 150°C (unless otherwise noted). Parameters are not tested.(1)

		MIN	MAX	UNIT
Input voltage	VIN	–0.3	100	V
	SW	–1	100	
	SW (20-ns transient)	–5	100	
	ILIM	–1	100	
	EN/UVLO	–0.3	100	
	VCC	–0.3	14	
	FB, COMP, SS/TRK, RT	–0.3	6	
	SYNCIN	–0.3	14	
Output voltage	BST	–0.3	110	V
	BST to VCC		100	
	BST to SW	–0.3	14	
Output voltage	VCC to BST (20-ns transient)		7	V
Output voltage	LO (20-ns transient)	–3		V
Output voltage	PGOOD	–0.3	14	V
Operating junction temperature, T_J		–40	125	°C
Storage temperature, T_{stg}		–55	125	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±2000	V
		Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002 (2)	±750	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

Over the recommended operating junction temperature range of –40°C to 150°C (unless otherwise noted). Parameters are not tested.

		MIN	NOM	MAX	UNIT
VIN	Input voltage	6		95	V
SW	SW voltage	–1		95	V
ILIM	ILIM voltage	–1		95	V
VCC	External VCC bias voltage	8		13	V
EN/UVLO	Enable voltage	0		95	V
BST	BST voltage	–0.3		105	V
BST to VCC	Pin-to-pin voltage difference			95	V
BST to SW	Pin-to-pin voltage difference	5		13	V
PGOOD	Pull-up voltage	0		13	V

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7.3 Recommended Operating Conditions (continued)

Over the recommended operating junction temperature range of –40°C to 150°C (unless otherwise noted). Parameters are not tested.

		MIN	NOM	MAX	UNIT
SYNCOUT	Source/sink currents	–1		1	mA
I-PGOOD	PGOOD sink current	0		2	mA
T_J	Operating junction temperature	–40		125	°C

7.4 Thermal Information

THERMAL METRIC[1]		20-PIN VQFN	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	36.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	28	
$R_{\theta JB}$	Junction-to-board thermal resistance	11.8	
Ψ_{JT}	Junction-to-top characterization parameter	0.4	
Ψ_{JB}	Junction-to-board characterization parameter	11.7	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	2.1	

(1) For more information about traditional and new thermal metrics, see the IC Package Thermal Metrics application report, SPRA953.

7.5 Electrical Characteristics

Typical values correspond to T_J = 25°C. Minimum and maximum limits apply over the –40°C to 150°C junction temperature range unless otherwise stated. V_{VIN} = 48 V, $V_{EN/UVLO}$ = 1.5 V, R_{RT} = 25 kΩ unless otherwise stated

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT SUPPLY						
V_{IN}	Operating input voltage range		6		95	V
I_{Q-RUN}	Operating input current, not switching	$V_{EN/UVLO}$ = 1.5 V, $V_{SS/TRK}$ = 0 V		2		mA
I_{Q-STBY}	Standby input current	$V_{EN/UVLO}$ = 1 V		2		mA
I_{Q-SHDN}	Shutdown input current	$V_{EN/UVLO}$ = 0 V, V_{VCC} < 1 V		20		µA
VCC REGULATOR						
V_{VCC}	VCC regulation voltage	$V_{SS/TRK}$ = 0 V, 9 V < V_{VIN} < 48 V, 0 mA < I_{VCC} < 20 mA		7.5		V
$V_{VCC-LDO}$	VIN to VCC dropout voltage	V_{VIN} = 6 V, $V_{SS/TRK}$ = 0 V, I_{VCC} = 20 mA		0.25	0.72	V
I_{SC-LDO}	VCC short-circuit current	$V_{SS/TRK}$ = 0 V, V_{VCC} = 0 V	40	50	70	mA
V_{VCC-UV}	VCC undervoltage threshold	VCC rising	4.8	4.93	5.2	V
$V_{VCC-UVH}$	VCC undervoltage hysteresis	Rising threshold – falling threshold		0.26		V
$V_{VCC-EXT}$	Minimum external bias voltage	Voltage required to disable VCC regulator	8			V
I_{VCC}	External VCC input current, not switching	$V_{SS/TRK}$ = 0 V, V_{VCC} = 13 V			2.3	mA
ENABLE AND INPUT UVLO						
V_{SHDN}	Shutdown to standby threshold	$V_{EN/UVLO}$ rising		0.42		V
$V_{SHDN-HYS}$	Shutdown threshold hysteresis	EN/UVLO Rising threshold – falling threshold		50		mV
V_{EN}	Standby to operating threshold	$V_{EN/UVLO}$ rising	1.164	1.2	1.236	V
I_{EN-HYS}	Standby to operating hysteresis current	$V_{EN/UVLO}$ = 1.5 V	9	10	11	µA
ERROR AMPLIFIER						

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7.5 Electrical Characteristics (continued)

Typical values correspond to T_J = 25°C. Minimum and maximum limits apply over the –40°C to 150°C junction temperature range unless otherwise stated. V_{VIN} = 48 V, $V_{EN/UVLO}$ = 1.5 V, R_{RT} = 25 kΩ unless otherwise stated

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{REF}	FB reference Voltage	FB connected to COMP	792	800	808	mV
$I_{FB-BIAS}$	FB input bias current	V_{FB} = 0.8 V, -40℃ to +125℃	–100		100	nA
$I_{FB-BIAS}$	FB input bias current	V_{FB} =0.8 V, T_J = +150℃	–200		200	nA
$V_{COMP-OH}$	COMP output high voltage	V_{FB} = 0 V, COMP sourcing 1 mA		5		V
$V_{COMP-OL}$	COMP output low voltage	COMP sinking 1 mA			0.3	V
AVOL	DC gain			94		dB
GBW	Unity gain bandwidth			6.5		MHz
SOFT-STARTand VOLTAGE TRACKING						
I_{SS}	SS/TRK capacitor charging current	$V_{SS/TRK}$ = 0 V	8.5	10	12	µA
R_{SS}	SS/TRK discharge FET resistance	$V_{EN/UVLO}$ = 1 V, $V_{SS/TRK}$ = 0.1 V		11		Ω
V_{SS-FB}	SS/TRK to FB offset	$V_{SS/TRK}$ – V_{FB}, V_{FB} = 0.8 V	–15	0	15	mV
$V_{SS-CLAMP}$	SS/TRK clamp voltage	V_{FB} = 0.8 V		0.115		V
POWER GOOD INDICATOR						
PG_{UTH}	FB upper threshold for PGOOD high to low	% of V_{REF}, V_{FB} rising		108		%
PG_{LTH}	FB lower threshold for PGOOD high to low	% of V_{REF}, V_{FB} falling		92		%
PG_{HYS_U}	PGOOD upper theshold hysteresis	% of V_{REF}		3		%
PG_{HYS_L}	PGOOD lower threshold hysteresis	% of V_{REF}		2		%
$T_{PG-RISE}$	PGOOD rising filter	FB to PGOOD rising edge		25		us
$T_{PG-FALL}$	PGOOD falling filter	FB to PGOOD falling edge		25		us
V_{PG-OL}	PGOOD low state output voltage	V_{FB} = 0.9 V, I_{PGOOD} = 2 mA			150	mV
I_{PG-OH}	PGOOD high state leakage current	V_{FB} = 0.8 V, V_{PGOOD} = 13 V, -40℃ to +150℃			400	nA
I_{PG-OH}	PGOOD high state leakage current	V_{FB} = 0.8 V, V_{PGOOD} = 13 V			400	nA
OSCILLATOR						
F_{SW1}	Oscilator frequency – 1	R_{RT} = 100 kΩ		100		kHz
F_{SW2}	Oscillator frequency – 2	R_{RT} = 25 kΩ		400		kHz
F_{SW3}	Oscillator frequency – 3	R_{RT} = 12.5 kΩ		780		kHz
SYNCHRONIZATION INPUT AND OUTPUT						
F_{SYNC}	SYNCIN external clock frequency range	% of nominal frequency set by R_{RT}	–20		50	%
$V_{SYNC-IH}$	SYNCIN input logic high		2			V
$V_{SYNC-IL}$	SYNCIN input logic low				0.8	V
$R_{SYNC-IN}$	SYNCIN input resistance	V_{SYNCIN} = 3 V		20		kΩ
$T_{SYNCI-PW}$	SYNCIN input minimum pulsewidth	Minimum high state or low state duration	50			ns
$V_{SYNCO-OH}$	SYNCOUT high-state output voltage	$I_{SYNCOUT}$ = –1 mA (sourcing current)	3			V
$V_{SYNCO-OL}$	SYNCOUT low-state output voltage	$I_{SYNCOUT}$ = 1 mA (sinking current)			0.4	V
$T_{SYNCOUT}$	Delay from HO rising to SYNCOUT leading edge	V_{SYNCIN} = 0 V, T_S = 1/F_{SW}, F_{SW} set by R_{RT}		T_S/2 – 140		ns
T_{SYNCIN}	Delay from SYNCIN rising to HO leading edge	50% to 50%		150		ns
GATE DRIVERS						
R_{HO-UP}	HO high state resistance, HO to BST	V_{BST} – V_{SW} = 7 V, I_{HO} = –100 mA		1.5		Ω

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7.5 Electrical Characteristics (continued)

Typical values correspond to T_J = 25°C. Minimum and maximum limits apply over the –40°C to 150°C junction temperature range unless otherwise stated. V_{VIN} = 48 V, $V_{EN/UVLO}$ = 1.5 V, R_{RT} = 25 kΩ unless otherwise stated

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$R_{HO-DOWN}$	HO low state resistance, HO to SW	$V_{BST} – V_{SW}$ = 7 V, I_{HO} = 100 mA		0.9		Ω
R_{LO-UP}	LO high state resistance, LO to VCC	$V_{BST} – V_{SW}$ = 7 V, I_{LO} = –100 mA		1.5		Ω
$R_{LO-DOWN}$	LO low state resistance, LO to PGND	$V_{BST} – V_{SW}$ = 7 V, I_{LO} = 100 mA		0.9		Ω
I_{HOH}, I_{LOH}	HO, LO source current	$V_{BST} – V_{SW}$ = 7 V, HO = SW, LO = AGND		2.3		A
I_{HOL}, I_{LOL}	HO, LO sink current	$V_{BST} – V_{SW}$ = 7 V, HO = BST, LO = VCC		3.5		A
T_{HO-TR}, T_{LO-TR}	HO, LO rise times	$V_{BST} – V_{SW}$ = 7 V, C_{LOAD} = 1 nF, 20% to 80%		7		ns
T_{HO-TF}, T_{LO-TF}	HO, LO fall times	$V_{BST} – V_{SW}$ = 7 V, C_{LOAD} = 1 nF, 80% to 20%		4		ns
T_{HO-DT}	HO turn-on deadtime	$V_{BST} – V_{SW}$ = 7 V, 50% to 50%		14		ns
T_{LO-DT}	LO turn-on deadtime	$V_{BST} – V_{SW}$ = 7 V, 50% to 50%		14		ns
BOOTSTRAP DIODE AND UNDER-VOLTAGE THRESHOLD						
$V_{BST-FWD}$	VCC to BST	VCC to BST, BST pin sourcing 20 mA		0.75	0.9	V
I_{Q-BST}	BST to SW quiescent current, not switching	$V_{SS/TRK}$ = 0 V, V_{SW} = 48 V, V_{BST} = 54 V		80		µA
V_{BST-UV}	BST to SW undervoltage detection	$V_{BST} – V_{SW}$ falling		3.4		V
$V_{BST-HYS}$	BST to SW undervoltage hysteresis	$V_{BST} – V_{SW}$ rising		0.42		V
PWM CONTROL						
$T_{ON(min)}$	Minimum controllable on-time	$V_{BST} – V_{SW}$ = 7 V, HO 50% to 50%		45		ns
$T_{OFF(min)}$	Minimum off-time	$V_{BST} – V_{SW}$ = 7 V, HO 50% to 50%		145		ns
DC_{100KHz}	Maximum duty cycle	F_{SW} = 100 kHz, 5.5 V < V_{VIN} < 60 V	98	99		%
DC_{400kHz}		F_{SW} = 400 kHz, 5.5 V < V_{VIN} < 60 V	90	94		%
$V_{RAMP(min)}$	RAMP valley voltage (COMP at 0% duty cycle)			300		mV
k_{FF}	PWM feedforward gain (V_{IN} / V_{RAMP})	5.5 V < V_{VIN} < 100 V		15		V / V
OVER CURRENT PROTECT (OCP) - VALLEY CURRENT LIMITING						
I_{RS}	ILIM source current, R_{SENSE} Mode	Low voltage detected at ILIM		100		µA
I_{RDSON}	ILIM source current, R_{DS-ON} mode	SW voltage detected at ILIM , T_J = 25°C	180	200	220	µA
I_{RSTC}	ILIM current tempco	R_{DS-ON} mode		4500		ppm/°C
$I_{RDSONTC}$	ILIM current tempco	R_{SENSE} mode		0		ppm/°C
$V_{ILIM-TH}$	ILIM comparator threshold at ILIM		–8	–2	3.5	mV
SHORT CIRCUIT PROTECTION (SCP) - DUTY CYCLE CLAMP						
$V_{CLAMP-OS}$	Clamp offset voltage - No current limiting	COMP to duty cycle clamp voltage		0.2 + V_{VIN}/75		V
$V_{CLAMP-MIN}$	Minimum duty cycle clamp voltage	Clamp voltage with continuous OCP		0.3 + V_{VIN}/150		V
HICCUP MODE FAULT PROTECTION						
$C_{HICC-DEL}$	Hiccup mode activation delay	Clock cycles with current limiting before off-time activated		128		cycles
C_{HICCUP}	Hiccup mode off time after activation	Clock cycles with no switching followed by SS/TRK release		8192		cycles
DIODE EMULATION / DCM OPERATION						
V_{ZCD-SS}	Zero-cross detect (ZCD) soft-start ramp	ZCD threshold measured at SW pin 50 cycles after first HO pulse		0		mV

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7.5 Electrical Characteristics (continued)

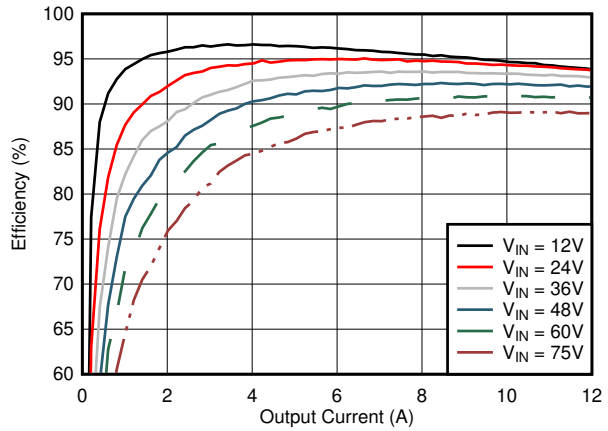
Typical values correspond to T_J = 25°C. Minimum and maximum limits apply over the –40°C to 150°C junction temperature range unless otherwise stated. V_{VIN} = 48 V, $V_{EN/UVLO}$ = 1.5 V, R_{RT} = 25 kΩ unless otherwise stated

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{ZCD-DIS}$	Zero-cross detect disable threshold	ZCD threshold measured at SW pin 1000 cycles after first HO pulse		200		mV
V_{DEM-TH}	Diode emulation zero-cross threshold	Measured at SW with V_{SW} rising		0		mV
THERMAL SHUTDOWN						
T_{SD}	Thermal shutdown threshold	T_J rising		175		°C
T_{SD-HYS}	Thermal shutdown hysteresis			20		°C
Switching Characteristics						
T_{HO-TR}, T_{LO-TR}	HO, LO rise times	V_{BST}-V_{SW} =7 V, C_{LOAD} =1 nF, 20% to 80%		7		ns
T_{HO-TF}, T_{LO-TF}	HO, fall times	V_{BST} -V_{SW} =7 V, C_{LOAD} =1 nF, 20% to 80%		4		ns
T_{HO-DT}	HO turnon dead time	V_{BST} - V_{SW} =7 V, LO off to HO on, 50% to 50%		14		ns

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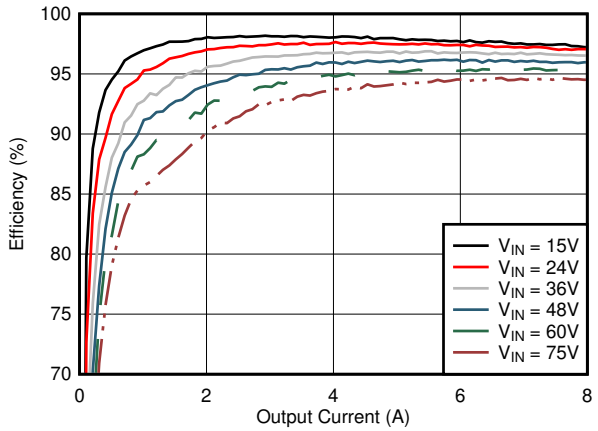
7.6 Typical Characteristics

V_{VIN} = 48 V, R_{RT} = 25 kΩ, SYNCIN tied to VCC, EN/UVLO tied to VIN (unless otherwise noted).



V_{OUT} = 5 V　　F_{SW} = 300 kHz
See 図 9-5　　R_{RT} = 33.2 kΩ

図 7-1. Efficiency vs Load, CCM



V_{OUT} = 12 V　　F_{SW} = 400 kHz
See 図 9-16　　R_{RT} = 24.9 kΩ

図 7-2. Efficiency vs Load, CCM

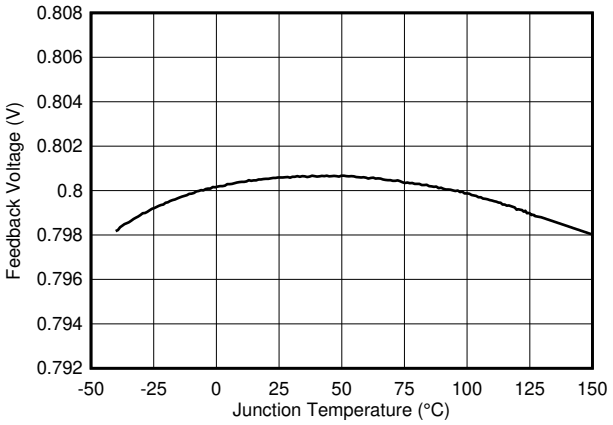


図 7-3. FB Voltage vs Junction Temperature

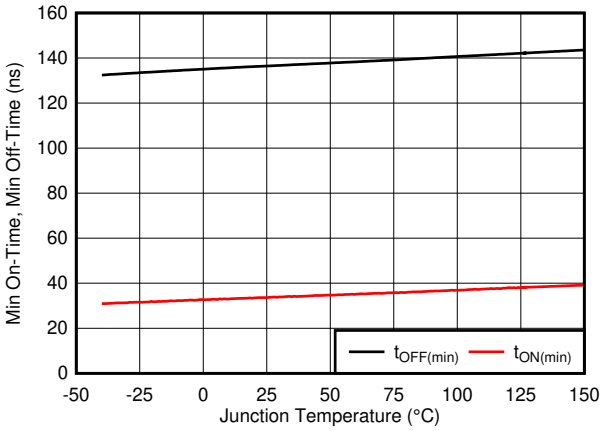
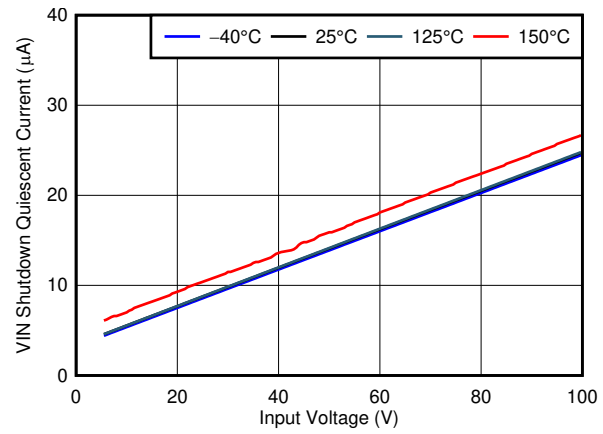
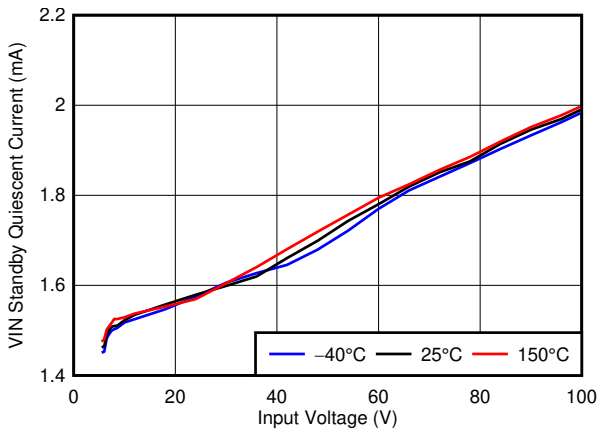


図 7-4. $t_{ON(min)}$ and $t_{OFF(min)}$ vs Junction Temperature



V_{SW} = 0 V　　$V_{EN/UVLO}$ = 0 V

図 7-5. I_{Q-SHD} vs Input Voltage



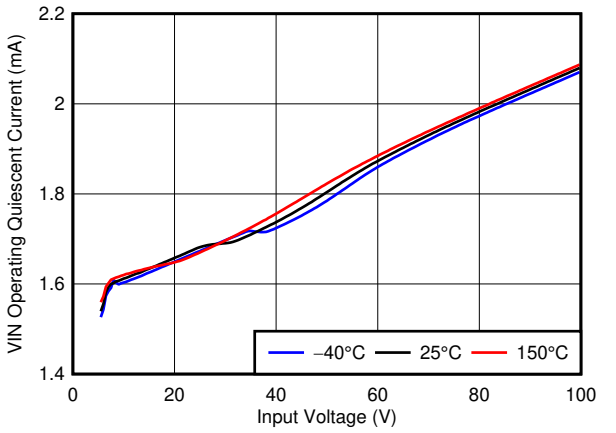
V_{SW} = 0 V　　$V_{EN/UVLO}$ = 1 V

図 7-6. $I_{Q-STANDBY}$ vs Input Voltage

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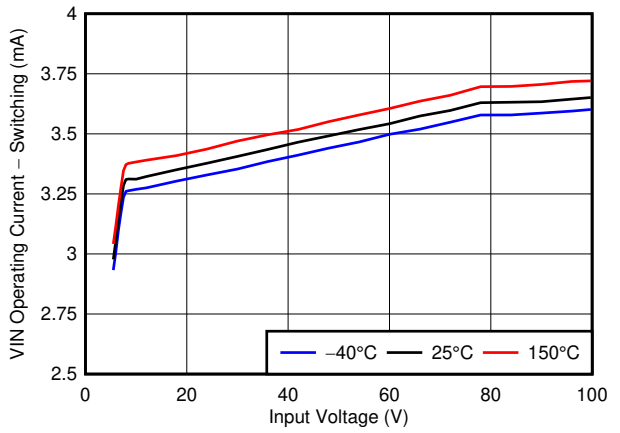
7.6 Typical Characteristics (continued)

V_{VIN} = 48 V, R_{RT} = 25 kΩ, SYNCIN tied to VCC, EN/UVLO tied to VIN (unless otherwise noted).



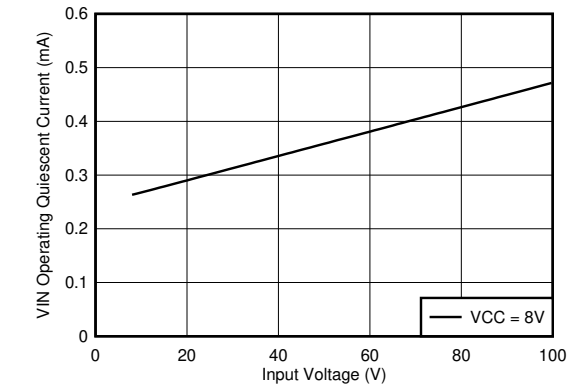
V_{SW} = 0 V $V_{EN/UVLO}$ = V_{VIN} $V_{SS/TRK}$ = 0 V

図 7-7. $I_{Q-OPERATING}$ (Nonswitching) vs Input Voltage



V_{SW} = 0 V HO, LO Open

図 7-8. $I_{Q-OPERATING}$ (Switching) vs Input Voltage



V_{SW} = 0 V V_{VCC} = V_{BST} = V_{ILIM} V_{FB} = 0 V

図 7-9. VIN Quiescent Current with External VCC Applied

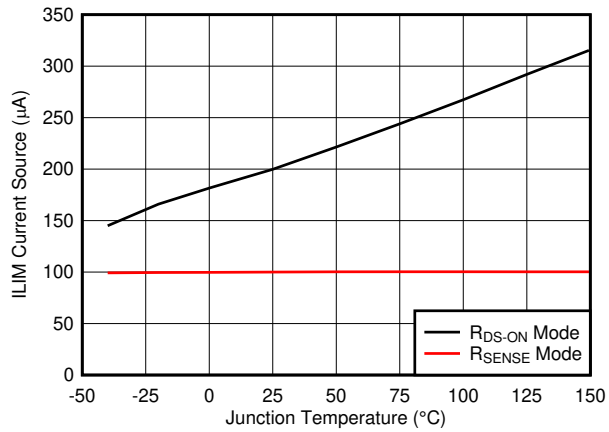
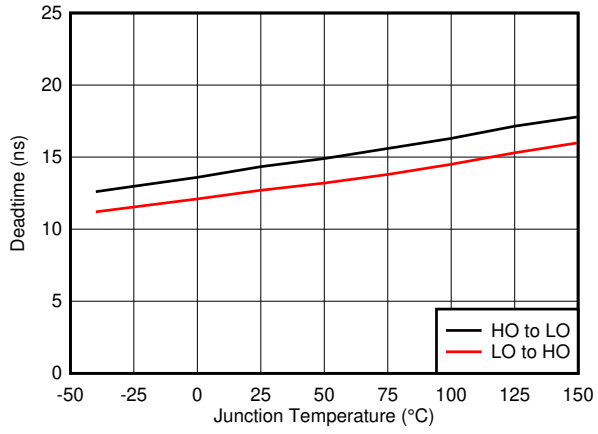


図 7-10. ILIM Current Source vs Junction Temperature



V_{SW} = 0 V

図 7-11. Deadtime vs Junction Temperature

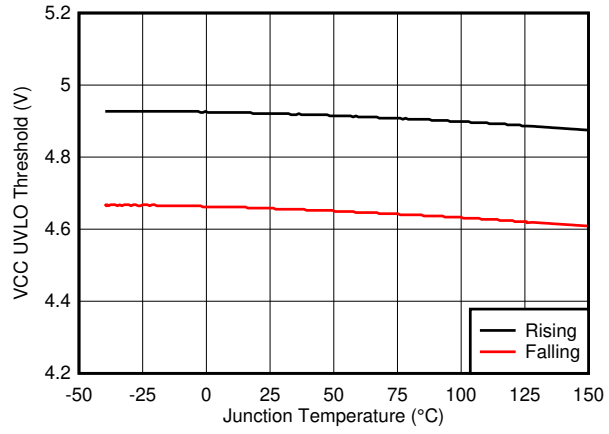


図 7-12. VCC UVLO Thresholds vs Junction Temperature

7.6 Typical Characteristics (continued)

V_{VIN} = 48 V, R_{RT} = 25 kΩ, SYNCIN tied to VCC, EN/UVLO tied to VIN (unless otherwise noted).

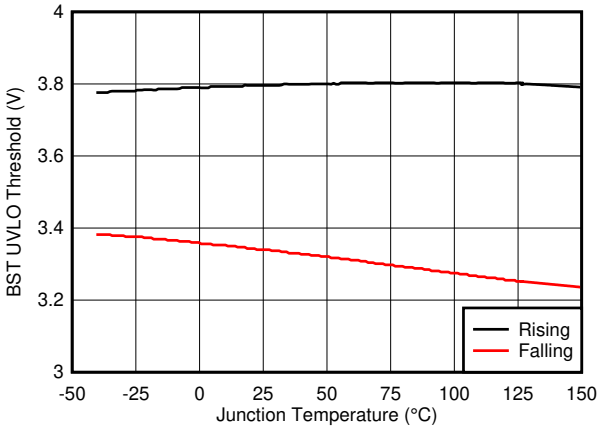


図 7-13. BST UVLO Thresholds vs Junction Temperature

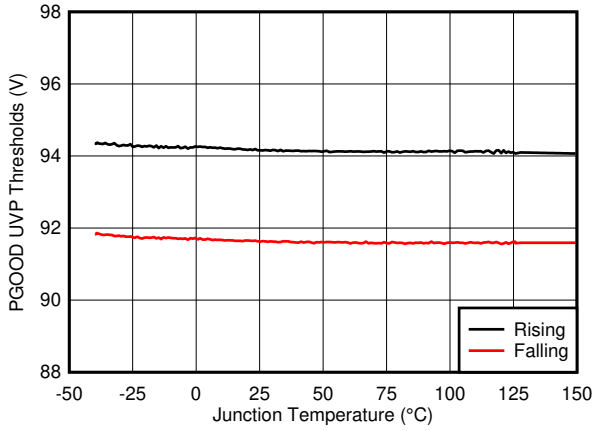


図 7-14. PGOOD UVP Thresholds vs Junction Temperature

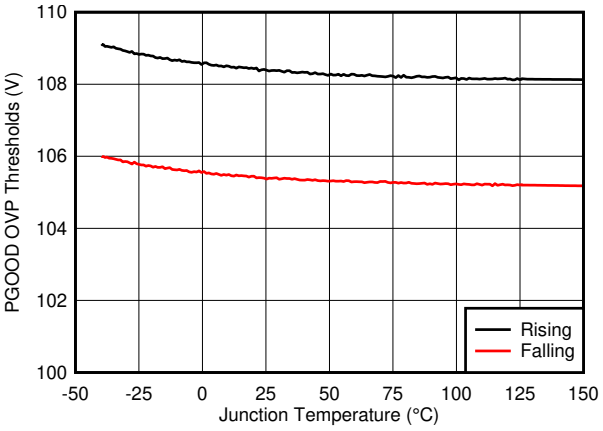


図 7-15. PGOOD OVP Thresholds vs Junction Temperature

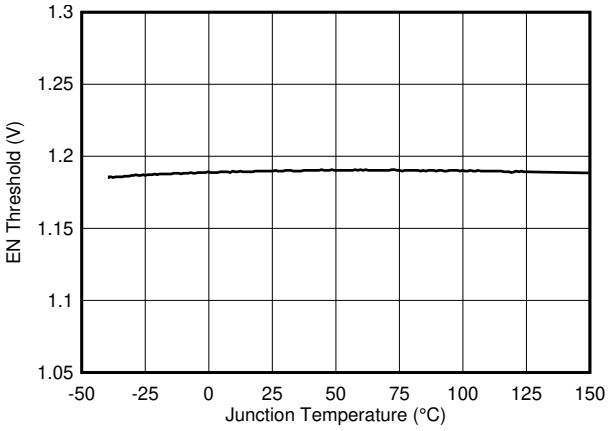


図 7-16. EN/UVLO Threshold vs Junction Temperature

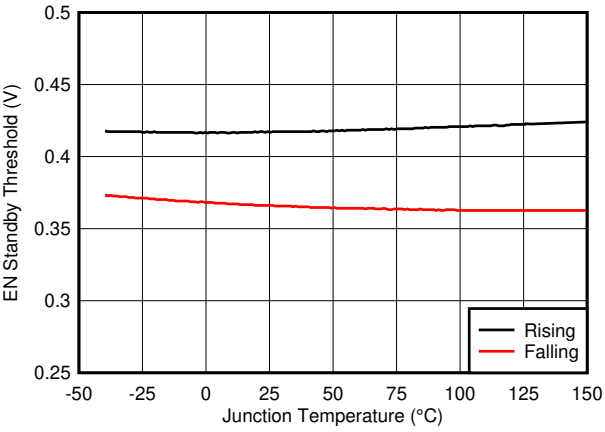
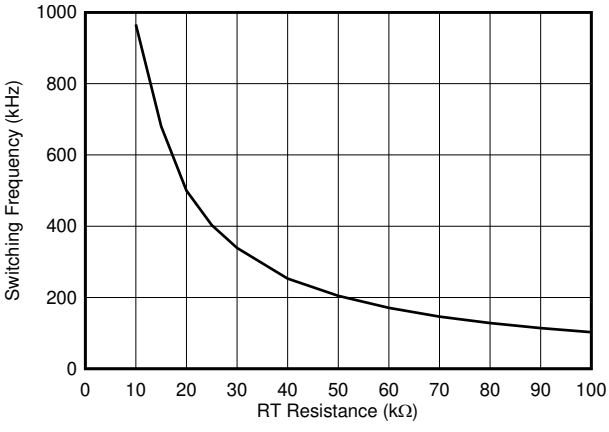


図 7-17. EN Standby Thresholds vs Junction Temperature



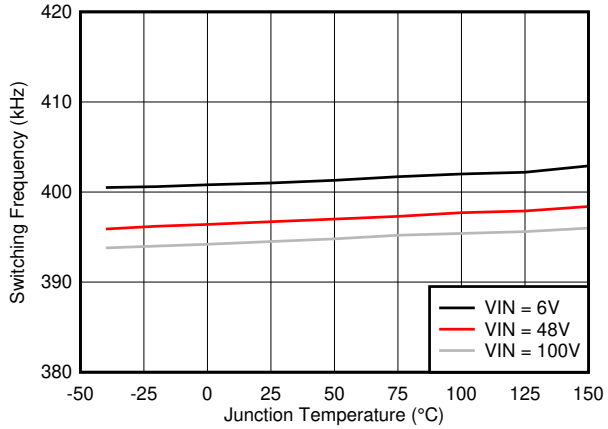
V_{SW} = 0 V

図 7-18. Oscillator Frequency vs RT Resistance

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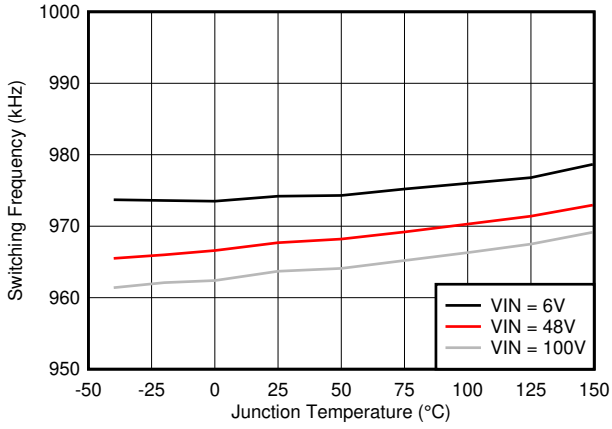
7.6 Typical Characteristics (continued)

V_{VIN} = 48 V, R_{RT} = 25 kΩ, SYNCIN tied to VCC, EN/UVLO tied to VIN (unless otherwise noted).



R_{RT} = 25 kΩ

図 7-19. Oscillator Frequency vs Junction Temperature



R_{RT} = 10 kΩ

図 7-20. Oscillator Frequency vs Junction Temperature

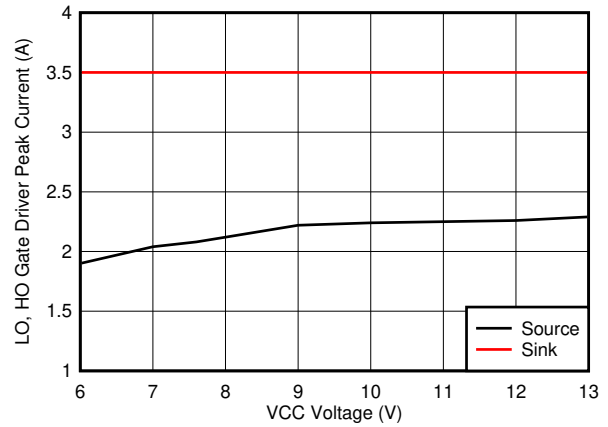


図 7-21. Gate Driver Peak Current vs VCC Voltage

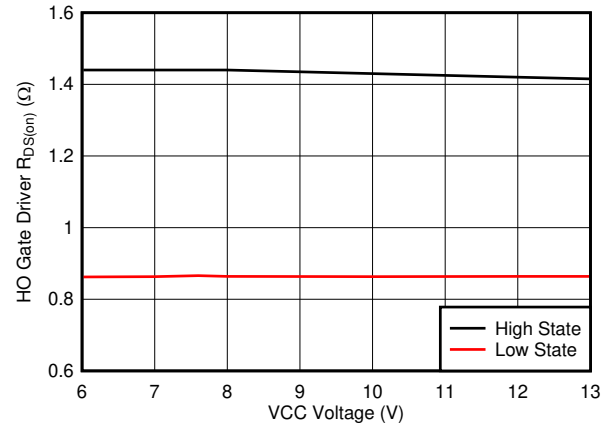


図 7-22. HO Driver Resistance vs VCC Voltage

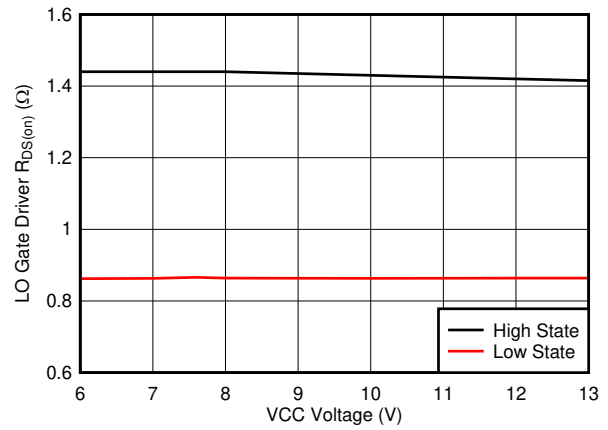
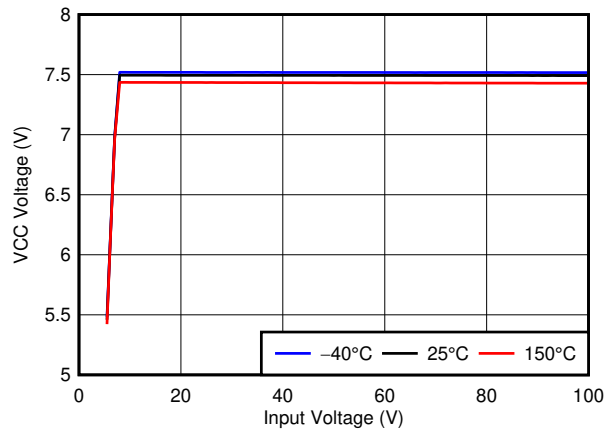


図 7-23. LO Driver Resistance vs VCC Voltage



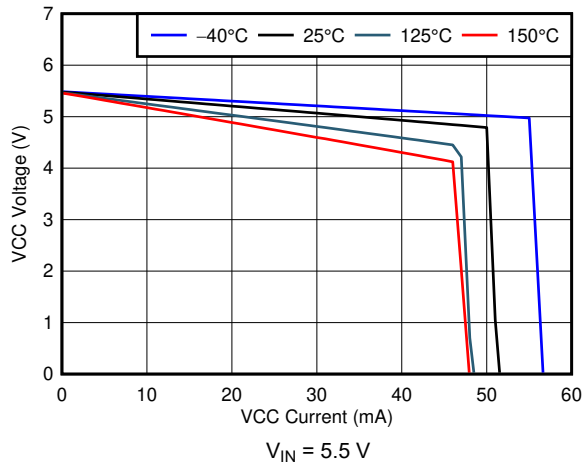
$V_{SS/TRK}$ = 0 V

図 7-24. VCC Voltage vs Input Voltage

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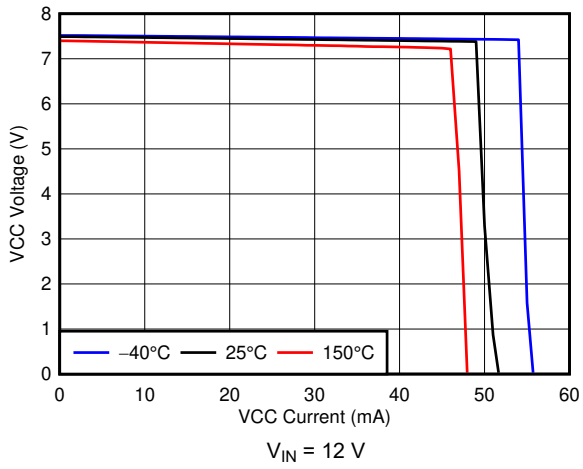
7.6 Typical Characteristics (continued)

V_{VIN} = 48 V, R_{RT} = 25 kΩ, SYNCIN tied to VCC, EN/UVLO tied to VIN (unless otherwise noted).



V_{IN} = 5.5 V

図 7-25. VCC vs ICC Characteristic



V_{IN} = 12 V

図 7-26. VCC vs ICC Characteristic

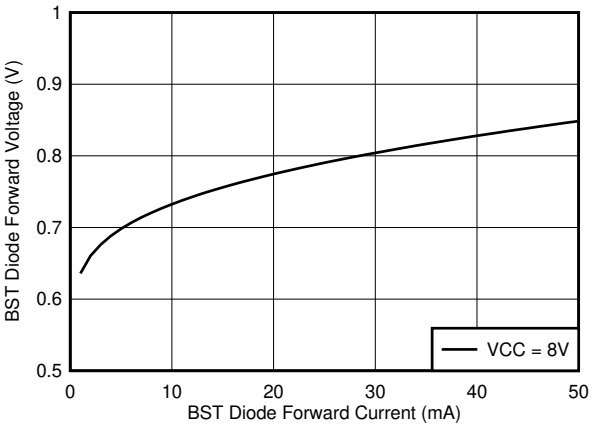


図 7-27. BST Diode Forward Voltage vs Current

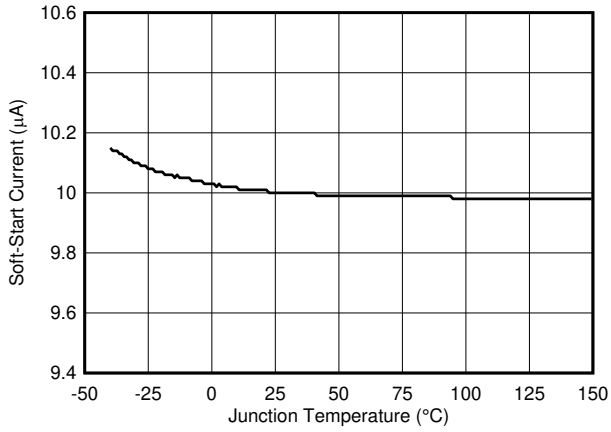


図 7-28. SS/TRK Current Source vs Junction Temperature

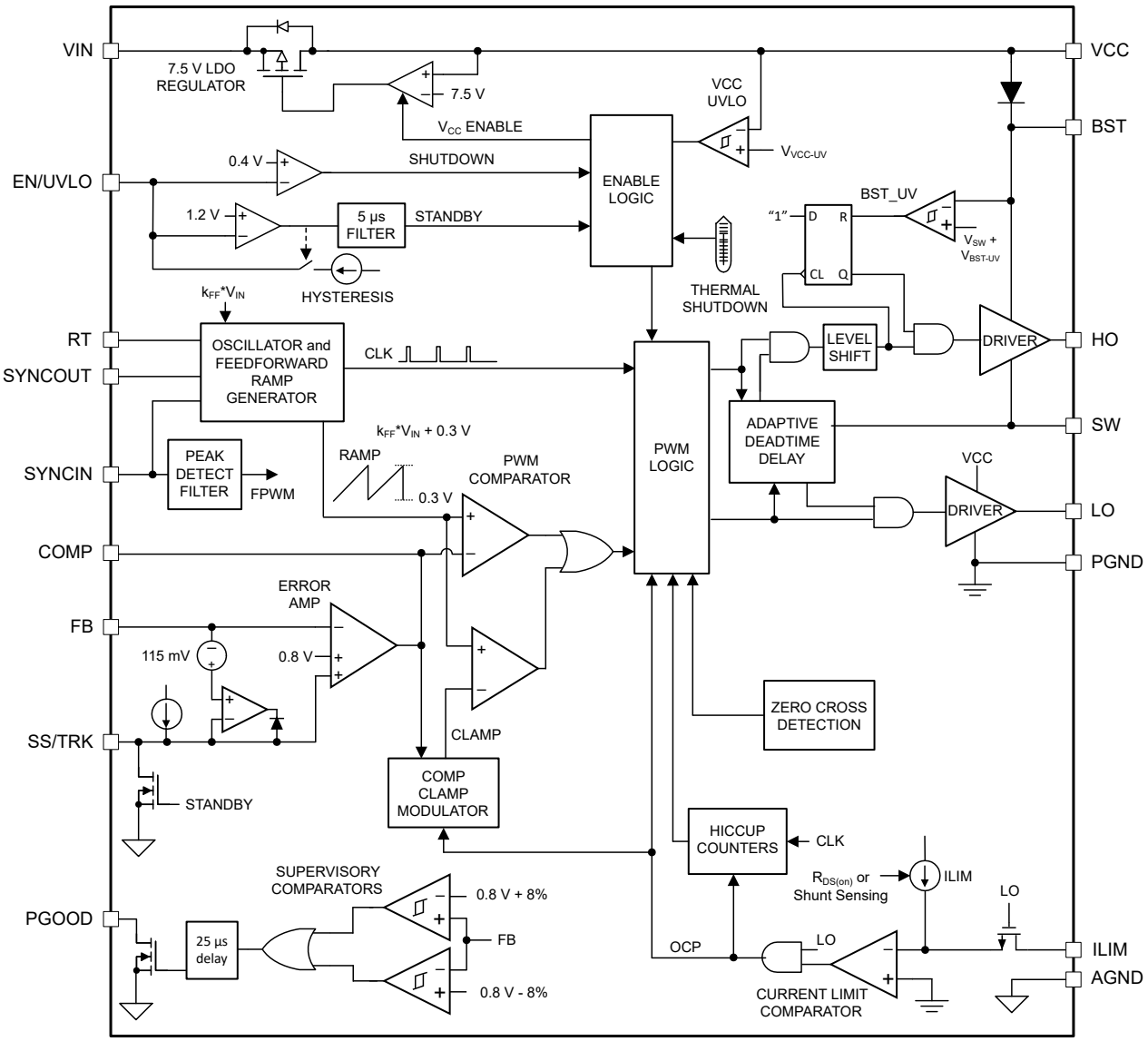
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8 Detailed Description

8.1 Overview

The LV5144 is a 95-V, synchronous, buck controller with all of the functions necessary to implement a high-efficiency step-down power supply. The output voltage range is from 0.8 V to 60 V. The voltage-mode control architecture uses input feedforward for excellent line transient response over a wide V_{IN} range. Voltage-mode control supports the wide duty cycle range for high input voltage and low dropout applications as well as when a high-voltage conversion ratio (for example, 10-to-1) is required. Current sensing for cycle-by-cycle current limit can be implemented with either the low-side FET $R_{DS(on)}$ or a current sense resistor. The operating frequency is programmable from 100 kHz to 1 MHz. The LV5144 drives external high-side and low-side NMOS power switches with robust 7.5-V gate drivers suitable for standard threshold MOSFETs. Adaptive dead-time control between the high-side and low-side drivers minimizes body diode conduction during switching transitions. An external bias supply can be connected to the VCC pin to improve efficiency in high-voltage applications. A user-selectable diode emulation feature enables DCM operation for improved efficiency and lower dissipation at light-load conditions.

8.2 Functional Block Diagram



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8.3 Feature Description

8.3.1 Input Range (V_{IN})

The LV5144 operational input voltage range is from 6 V to 95 V. The device is intended for step-down conversions from 12-V, 24-V, 48-V, 60-V, and 72-V unregulated, semiregulated, and fully-regulated supply rails. The application circuit in 図 8-1 shows all the necessary components to implement an LV5144-based wide-V_{IN} step-down regulator using a single supply. The LV5144 uses an internal LDO subregulator to provide a 7.5-V VCC bias rail for the gate drive and control circuits (assuming the input voltage is higher than 7.5 V plus the necessary subregulator dropout specification).

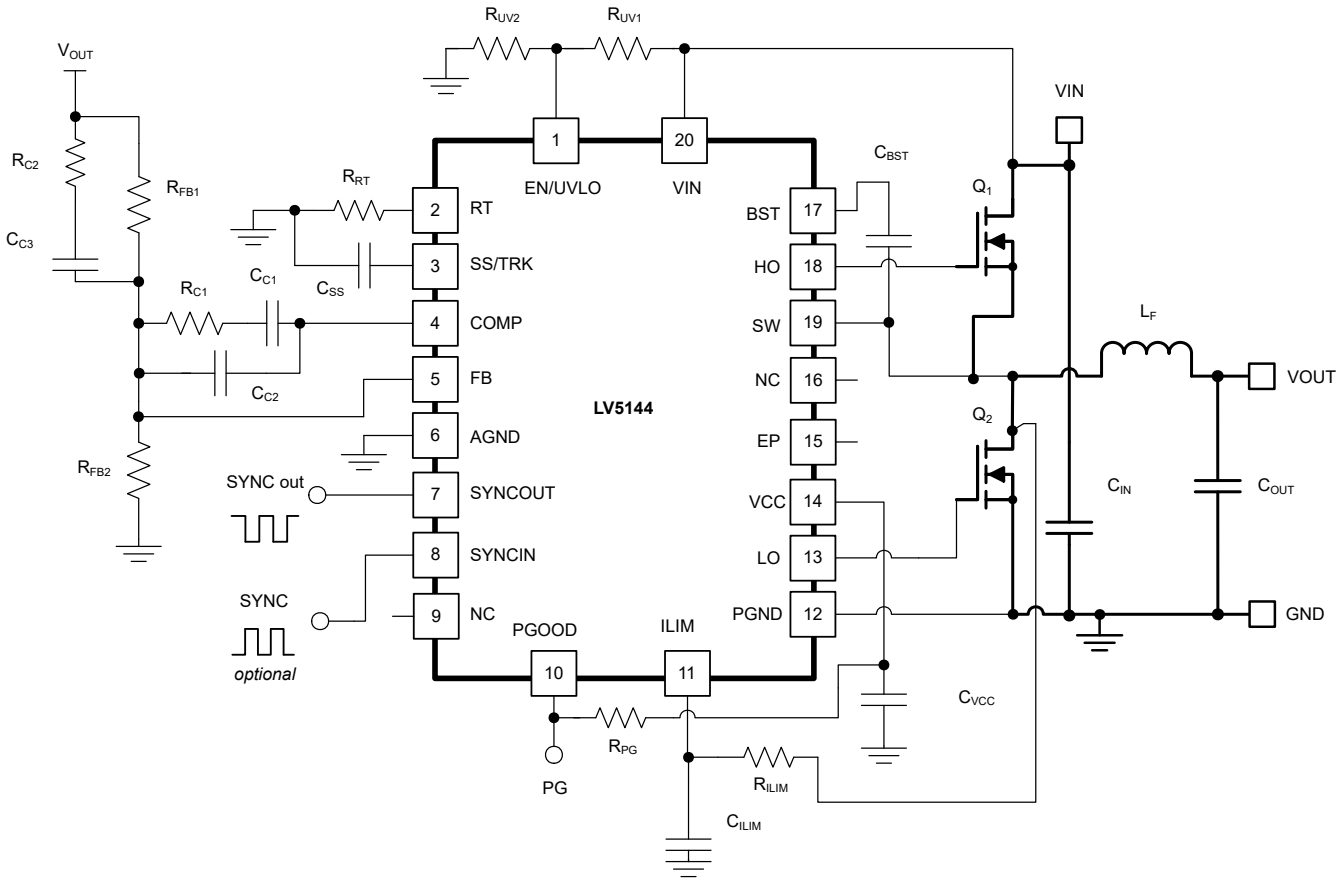


図 8-1. Schematic Diagram for VIN Operating Range of 6 V to 95 V

In high-voltage applications, take extra care to ensure the VIN pin does not exceed the absolute maximum voltage rating of 95 V during line or load transient events. Voltage ringing on the VIN pin that exceeds the values in the *Absolute Maximum Ratings* can damage the IC. Use high-quality ceramic input capacitors to minimize ringing. An RC filter from the input rail to the VIN pin (for example, 4.7 Ω and 0.1 µF) provides supplementary filtering at the VIN pin.

8.3.2 Output Voltage Setpoint and Accuracy (FB)

The reference voltage at the FB pin is set at 0.8 V with a feedback system accuracy over the full junction temperature range of ±1%. Junction temperature range for the device is –40°C to +125°C. While dependent on switching frequency and load current requirements, the LV5144 is generally capable of providing an output voltage in the range of 0.8 V to a maximum of 60 V or slightly less than V_{IN}, whichever is lower. The DC output voltage setpoint during normal operation is set by the feedback resistor network, R_{FB1} and R_{FB2}, connected to the output.

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8.3.3 High-Voltage Bias Supply Regulator (VCC)

The LV5144 contains an internal high-voltage VCC regulator that provides a bias supply for the PWM controller and its gate drivers for the external MOSFETs. The input pin (VIN) can be connected directly to an input voltage source up to 100 V. The output of the VCC regulator is set to 7.5 V. However, when the input voltage is below the VCC setpoint level, the VCC output tracks V_{IN} with a small voltage drop. Connect a ceramic decoupling capacitor between 1 µF and 5 µF from VCC to AGND for stability.

The VCC regulator output has a current limit of 40 mA (minimum). At power up, the regulator sources current into the capacitor connected to the VCC pin. When the VCC voltage exceeds its rising UVLO threshold of 4.93 V, the output is enabled (if EN/UVLO is above 1.2 V), and the soft-start sequence begins. The output remains active until the VCC voltage falls below its falling UVLO threshold of 4.67 V (typical) or if EN/UVLO goes to a standby or shutdown state.

Internal power dissipation of the VCC regulator can be minimized by connecting the output voltage or an auxiliary bias supply rail (up to 13 V) to VCC using a diode D_{VCC} as shown in 図 8-2. A diode in series with the input prevents reverse current flow from VCC to VIN if the input voltage falls below the external VCC rail.

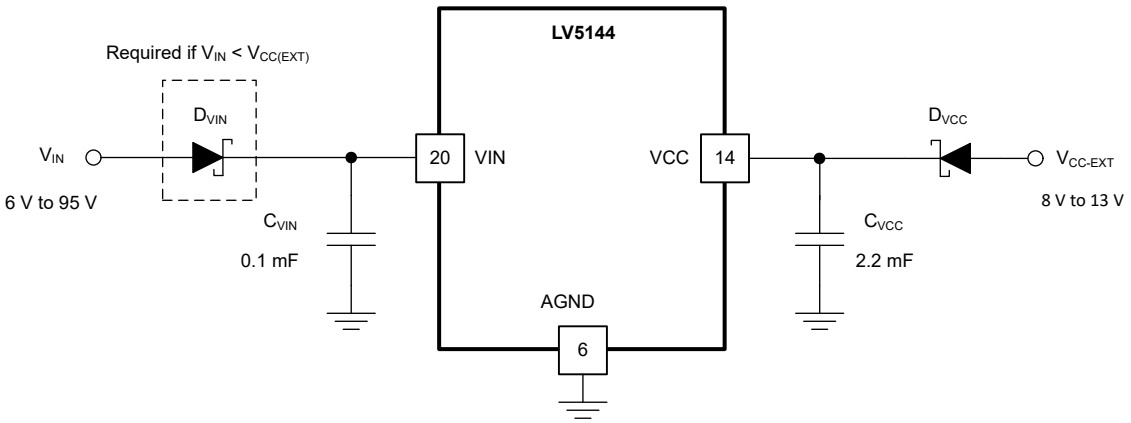


図 8-2. VCC Bias Supply Connection From VOUT or Auxiliary Supply

Note that a finite bias supply regulator dropout voltage exists and is manifested to a larger extent when driving high gate charge (Q_G) power MOSFETs at elevated switching frequencies. For example, at V_{VIN} = 6 V, the VCC voltage is 5.8 V with a DC operating current, I_{VCC}, of 20 mA. Such a low gate drive voltage can be insufficient to fully enhance the power MOSFETs. At the very least, MOSFET on-state resistance, $R_{DS(ON)}$, can increase at such low gate drive voltage.

Here are the main considerations when operating at input voltages below 7.5 V:

- Increased MOSFET $R_{DS(on)}$ at lower V_{GS}, leading to Increased conduction losses and reduced OCP setpoint
- Increased switching losses given the slower switching times when operating at lower gate voltages
- Restricted range of suitable power MOSFETs to choose from (MOSFETs with $R_{DS(on)}$ rated at V_{GS} = 4.5 V become mandatory)

8.3.4 Precision Enable (EN/UVLO)

The EN/UVLO input supports adjustable input undervoltage lockout (UVLO) with hysteresis programmed by the resistor values for application specific power-up and power-down requirements. EN/UVLO connects to a comparator-based input referenced to a 1.2-V bandgap voltage. An external logic signal can be used to drive the EN/UVLO input to toggle the output ON and OFF and for system sequencing or protection. The simplest way to enable the operation of the LV5144 is to connect EN/UVLO directly to VIN. This allows self start-up of the LV5144 when V_{CC} is within its valid operating range. However, many applications benefit from using a resistor divider R_{UV1} and R_{UV2} as shown in 図 8-3 to establish a precision UVLO level.

Use 式 1 and 式 2 to calculate the UVLO resistors given the required input turn-on and turn-off voltages.

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$$R_{UV1} = \frac{V_{IN(on)} - V_{IN(off)}}{I_{HYS}} \quad (1)$$

$$R_{UV2} = R_{UV1} \cdot \frac{V_{EN}}{V_{IN(on)} - V_{EN}} \quad (2)$$

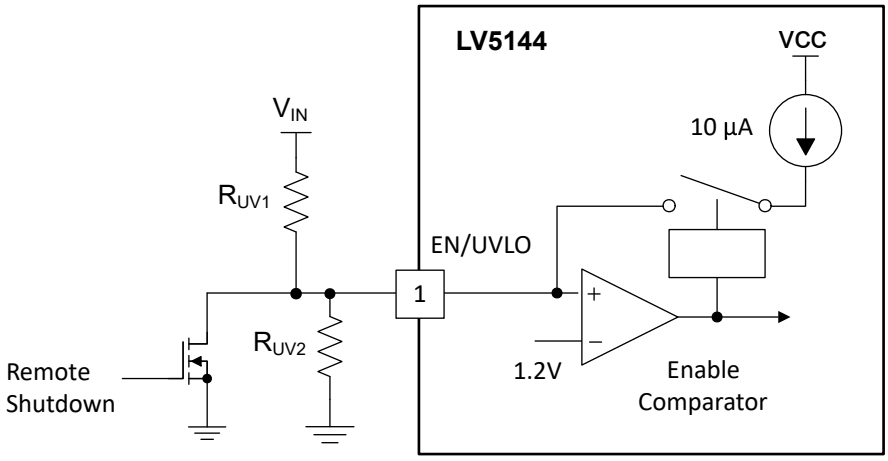


図 8-3. Programmable Input Voltage UVLO Turn-on and Turn-off

The LV5144 enters a low I_Q shutdown mode when EN/UVLO is pulled below approximately 0.4 V. The internal LDO regulator powers off and the internal bias supply rail collapses, shutting down the bias currents of the LV5144. The LV5144 operates in standby mode when the EN/UVLO voltage is between the hard shutdown and precision enable (standby) thresholds.

8.3.5 Power Good Monitor (PGOOD)

The LV5144 provides a PGOOD flag pin to indicate when the output voltage is within a regulation window. Use the PGOOD signal as shown in Primary-Secondary Sequencing Implementation Using PGOOD and EN/UVLOfor start-up sequencing of downstream converters, fault protection, and output monitoring. PGOOD is an open-drain output that requires a pullup resistor to a DC supply not greater than 13 V. The typical range of pullup resistance is 10 kΩ to 100 kΩ. If necessary, use a resistor divider to decrease the voltage from a higher voltage pullup rail.

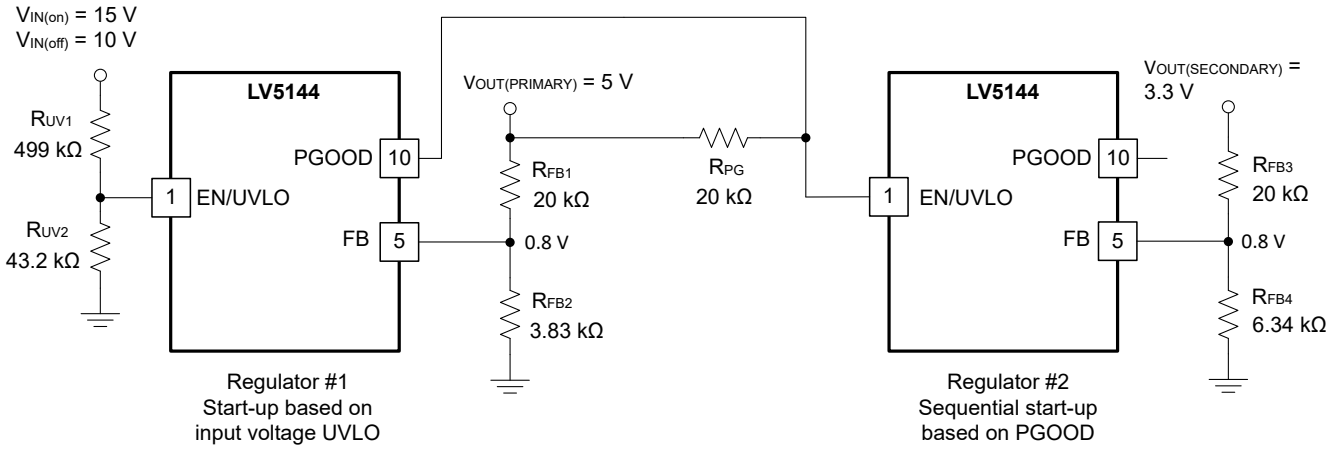


図 8-4. Primary-Secondary Sequencing Implementation Using PGOOD and EN/UVLO

When the FB voltage exceeds 94% of the internal reference V_{REF}, the internal PGOOD switch turns off and PGOOD can be pulled high by the external pullup. If the FB voltage falls below 92% of V_{REF}, the internal

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PGOOD switch turns on, and PGOOD is pulled low to indicate that the output voltage is out of regulation. Similarly, when the FB voltage exceeds 108% of V_{REF}, the internal PGOOD switch turns on, pulling PGOOD low. If the FB voltage subsequently falls below 105% of V_{REF}, the PGOOD switch is turned off and PGOOD is pulled high. PGOOD has a built-in deglitch delay of 25 µs.

8.3.6 Switching Frequency (RT, SYNCIN)

There are two options for setting the switching frequency, F_{SW}, of the LV5144, thus providing a power supply designer with a level of flexibility when choosing external components for various applications. To adjust the frequency, use a resistor from the RT pin to AGND, or synchronize the LV5144 to an external clock signal through the SYNCIN pin.

8.3.6.1 Frequency Adjust

Adjust the free-running switching frequency by using a resistor from the RT pin to AGND. The switching frequency range is from 100 kHz to 1 MHz. The frequency set resistance, R_{RT}, is governed by Equation 3. E96 standard-value resistors for common switching frequencies are given in 表 8-1.

$$R_{RT}\left[k\Omega\right] = \frac{10^4}{F_{SW}\left[kHz\right]} \tag{3}$$

表 8-1. Frequency Set Resistors

SWITCHING FREQUENCY (kHz)	FREQUENCY SET RESISTANCE (kΩ)
100	100
200	49.9
250	40.2
300	33.2
400	24.9
500	20
750	13.3
1000	10

8.3.6.2 Clock Synchronization

Apply an external clock synchronization signal to the LV5144 to synchronize switching in both frequency and phase. Requirements for the external clock SYNC signal are:

- Clock frequency range: 100 kHz to 1 MHz
- Clock frequency: –20% to +50% of the free-running frequency set by R_{RT}
- Clock maximum voltage amplitude: 13 V
- Clock minimum pulse width: 50 ns

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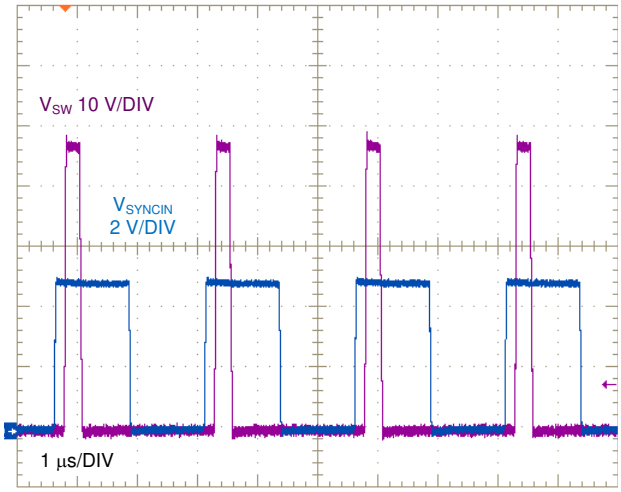


図 8-5. Typical 400-kHz SYNCIN and SW Voltage Waveforms

図 8-5 shows a clock signal at 400 kHz and the corresponding SW node waveform (V_{IN} = 48 V, V_{OUT} = 5 V, free-running frequency = 280 kHz). The SW voltage waveform is synchronized with respect to the rising edge of SYNCIN. The rising edge of the SW voltage is phase delayed relative to SYNCIN by approximately 100 ns.

8.3.7 Configurable Soft Start (SS/TRK)

After the EN/UVLO pin exceeds its rising threshold of 1.2 V, the LV5144 begins charging the output to the DC level dictated by the feedback resistor network. The LV5144 features an adjustable soft start (set by a capacitor from the SS/TRK pin to GND) that determines the charging time of the output. A 10-µA current source charges this soft-start capacitor. Soft start limits inrush current as a result of high output capacitance to avoid an overcurrent condition. Stress on the input supply rail is also reduced. The soft-start time, t_{SS}, for the output voltage to ramp to its nominal level is set by 式 4.

$$t_{SS} = \frac{C_{SS} \cdot V_{REF}}{I_{SS}} \tag{4}$$

where

- C_{SS} is the soft-start capacitance
- V_{REF} is the 0.8-V reference
- I_{SS} is the 10-µA current sourced from the SS/TRK pin

More simply, calculate C_{SS} using 式 5.

$$C_{SS}\left[nF\right] = 12.5 \cdot t_{SS}\left[ms\right] \tag{5}$$

The SS/TRK pin is internally clamped to V_{FB} + 115 mV to allow a soft start recovery from an overload event. The clamp circuit requires a soft-start capacitance greater than 2 nF for stability and has a current limit of approximately 2 mA.

8.3.7.1 Tracking

The SS/TRK pin also doubles as a tracking pin when primary-secondary power-supply tracking is required. This tracking is achieved by simply dividing down the output voltage of the primary with a simple resistor network. Coincident, ratiometric, and offset tracking modes are possible.

If an external voltage source is connected to the SS/TRK pin, the external soft-start capability of the LV5144 is effectively disabled. The regulated output voltage level is reached when the SS/TRK pin reaches the 0.8-V reference voltage level. It is the responsibility of the system designer to determine if an external soft-start

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capacitor is required to keep the device from entering current limit during a start-up event. Likewise, the system designer must also be aware of how fast the input supply ramps if the tracking feature is enabled.

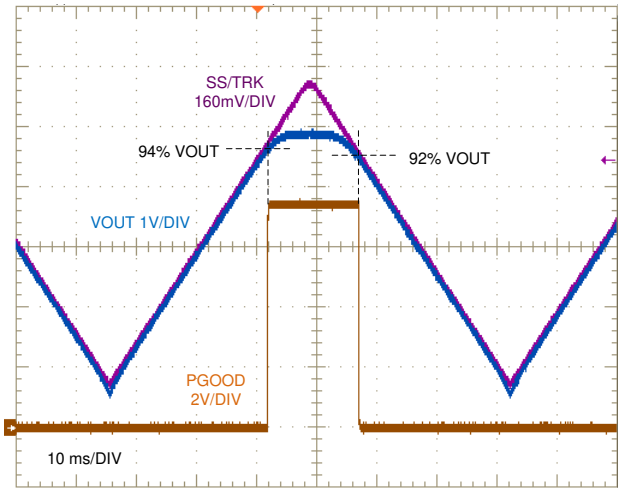


図 8-6. Typical Output Voltage Tracking and PGOOD Waveforms

図 8-6 shows a triangular voltage signal directly driving SS/TRK and the corresponding output voltage tracking response. Nominal output voltage here is 5 V, with oscilloscope channel scaling chosen such that the waveforms overlap during tracking. As expected, the PGOOD flag transitions at thresholds of 94% (rising) and 92% (falling) of the nominal output voltage setpoint.

Two practical tracking configurations, ratiometric and coincident, are shown in Tracking Implementation With Primary, Ratiometric Secondary, and Coincident Secondary Rails. The most common application is coincident tracking, used in core versus I/O voltage tracking in DSP and FPGA implementations. Coincident tracking forces the primary and secondary channels to have the same output voltage ramp rate until the secondary output reaches its regulated setpoint. Conversely, ratiometric tracking sets the output voltage of the secondary to a fraction of the output voltage of the primary during start-up.

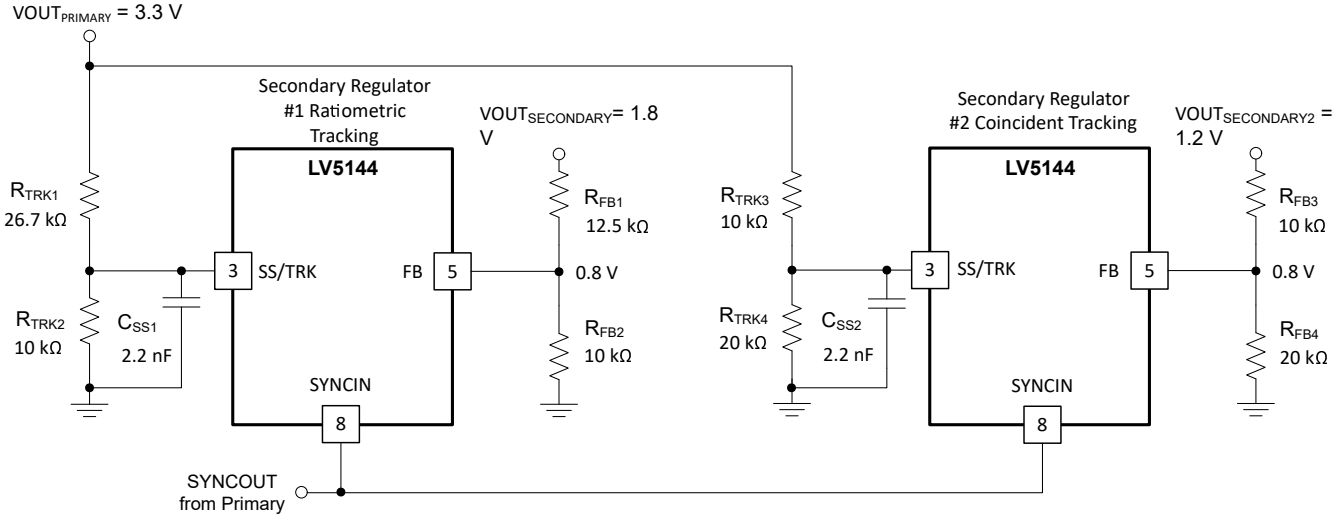


図 8-7. Tracking Implementation With Primary, Ratiometric Secondary, and Coincident Secondary Rails

For coincident tracking, connect the SS/TRK input of the secondary regulator to a resistor divider from the output voltage of the primary that is the same as the divider used on the FB pin of the secondary. In other words, simply select R_{TRK3} = R_{FB3} and R_{TRK4} = R_{FB4} as shown in Tracking Implementation With Primary, Ratiometric Secondary, and Coincident Secondary Rails. As the primary voltage rises, the secondary voltage rises identically

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(aside from the 80-mV offset from SS/TRK to FB when V_{FB} is below 0.8 V). Eventually, the secondary voltage reaches its regulation voltage, at which point the internal reference takes over the regulation while the SS/TRK input continues to 115 mV above FB, and no longer controls the output voltage.

In all cases, to ensure that the output voltage accuracy is not compromised by the SS/TRK voltage being too close to the 0.8-V reference voltage, the final value of the SS/TRK voltage of the secondary must be at least 100 mV above FB.

8.3.8 Voltage-Mode Control (COMP)

The LV5144 incorporates a voltage-mode control loop implementation with input voltage feedforward to eliminate the input voltage dependence of the PWM modulator gain. This configuration allows the controller to maintain stability throughout the entire input voltage operating range and provides optimal response to input voltage transient disturbances. The constant gain provided by the controller greatly simplifies loop compensation design because the loop characteristics remain constant as the input voltage changes, unlike a buck converter without voltage feedforward. An increase in input voltage is matched by a concomitant increase in ramp voltage amplitude to maintain constant modulator gain. The input voltage feedforward gain, k_{FF}, is 15, equivalent to the input voltage divided by the ramp amplitude, V_{IN}/V_{RAMP}. See セクション 9.1.3 for more detail.

8.3.9 Gate Drivers (LO, HO)

The LV5144 gate driver impedances are low enough to perform effectively in high output current applications where large die-size or paralleled MOSFETs with correspondingly large gate charge, Q_G, are used. Measured at V_{VCC} = 7.5 V, the low-side driver of the LV5144 has a low impedance pulldown path of 0.9 Ω to minimize the effect of dv/dt induced turn-on, particularly with low gate-threshold voltage MOSFETs. Similarly, the high-side driver has 1.5-Ω and 0.9-Ω pullup and pulldown impedances, respectively, for faster switching transition times, lower switching loss, and greater efficiency.

The high-side gate driver works in conjunction with an integrated bootstrap diode and external bootstrap capacitor, C_{BST}. When the low-side MOSFET conducts, the SW voltage is approximately at 0 V and C_{BST} is charged from VCC through the integrated boot diode. Connect a 0.1-µF or larger ceramic capacitor close to the BST and SW pins.

Furthermore, there is a proprietary adaptive dead-time control on both switching edges to prevent shoot-through and cross-conduction, minimize body diode conduction time, and reduce body diode reverse recovery losses.

8.3.10 Current Sensing and Overcurrent Protection (ILIM)

The LV5144 implements a lossless current sense scheme designed to limit the inductor current during an overload or short-circuit condition. 図 8-8 portrays the popular current sense method using the on-state resistance of the low-side MOSFET. Meanwhile, 図 8-9 shows an alternative implementation with current shunt resistor, R_S. The LV5144 senses the inductor current during the PWM off-time (when LO is high).

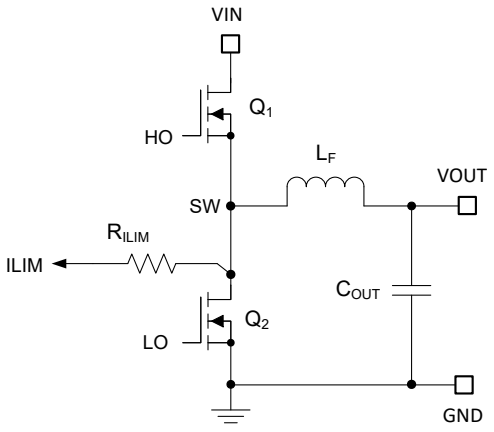


図 8-8. MOSFET $R_{DS(on)}$ Current Sensing

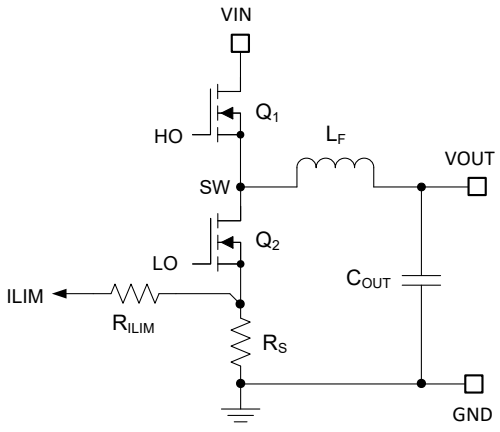


図 8-9. Shunt Resistor Current Sensing

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The ILIM pin of the LV5144 sources a reference current that flows in an external resistor, designated R_{ILIM}, to program of the current limit threshold. A current limit comparator on the ILIM pin prevents further SW pulses if the ILIM pin voltage goes below GND. 図 8-10 shows the implementation.

Resistor R_{ILIM} is tied to SW to use the $R_{DS(on)}$ of the low-side MOSFET as a sensing element (termed $R_{DS(on)}$ mode). Alternatively, R_{ILIM} is tied to a shunt resistor connected at the source of the low-side MOSFET (termed R_{SENSE} mode). The LV5144 detects the appropriate mode at start-up and sets the source current amplitude and temperature coefficient (TC) accordingly.

The ILIM current with R_{DS-ON} sensing is 200 µA at 27°C junction temperature and incorporates a TC of +4500 ppm/°C to generally track the $R_{DS(on)}$ temperature variation of the low-side MOSFET. Conversely, the ILIM current is a constant 100 µA in R_{SENSE} mode. This controls the valley of the inductor current during a steady-state overload at the output. Depending on the chosen mode, select the resistance of R_{ILIM} using Equation 6.

$$R_{ILIM} = \begin{cases} \dfrac{I_{OUT} - \Delta I_L/2}{I_{RDSON}} \cdot R_{DS(on)Q2}, & R_{DS(on)} \text{ sensing} \\ \dfrac{I_{OUT} - \Delta I_L/2}{I_{RS}} \cdot R_S, & \text{shunt sensing} \end{cases} \quad (6)$$

where

- ΔI_L is the peak-to-peak inductor ripple current
- $R_{DS(on)Q2}$ is the on-state resistance of the low-side MOSFET
- I_{RDSON} is the ILIM pin current in R_{DS-ON} mode
- R_S is the resistance of the current-sensing shunt element
- I_{RS} is the ILIM pin current in R_{SENSE} mode

Given the large voltage swings of ILIM in $R_{DS(on)}$ sensing mode, a capacitor designated C_{ILIM} connected from ILIM to PGND is essential to the operation of the valley current limit circuit. Choose this capacitance such that the time constant $R_{ILIM} \cdot C_{ILIM}$ is approximately 6 ns.

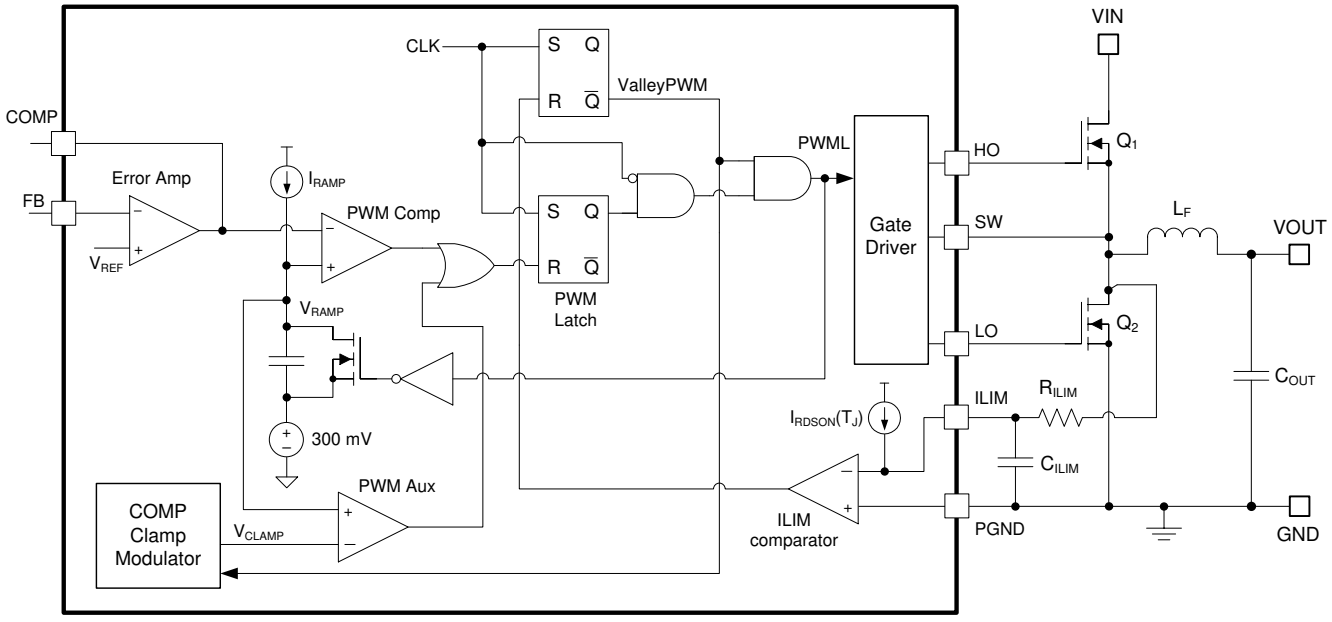


図 8-10. OCP Setpoint Defined by Current Source I_{RDSON} and Resistor R_{ILIM} in R_{DS-ON} Mode

Note that current sensing with a shunt component is typically implemented at lower output current levels to provide accurate overcurrent protection. Burdened by the unavoidable efficiency penalty, PCB layout, and

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additional cost implications, this configuration is not usually implemented in high-current applications (except where OCP setpoint accuracy and stability over the operating temperature range are critical specifications).

8.3.11 OCP Duty Cycle Limiter

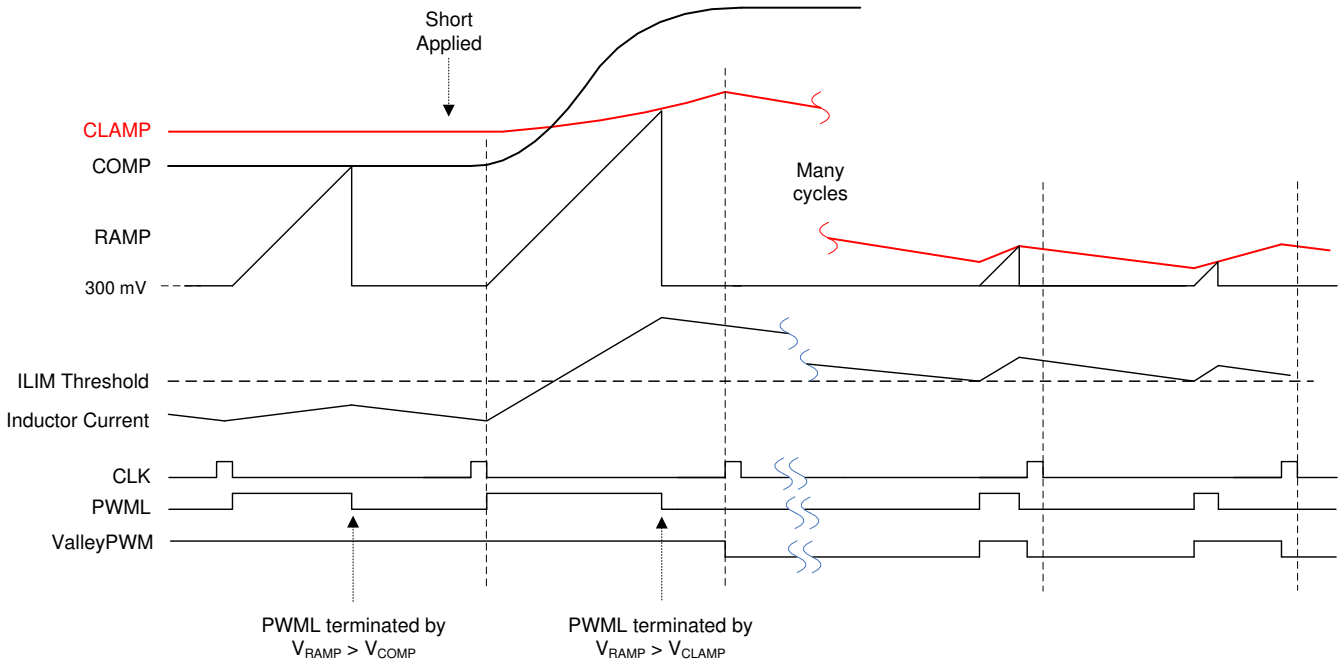


図 8-11. OCP Duty Cycle Limiting Waveforms

In addition to valley current limiting, the LV5144 uses a proprietary duty-cycle limiter circuit to reduce the PWM on-time during an overcurrent condition. As shown in 図 8-10, an auxiliary PWM comparator along with a modulated CLAMP voltage limits how quickly the on-time increases in response to a large step in the COMP voltage that typically occurs with a voltage-mode control loop architecture.

As depicted in 図 8-11, the CLAMP voltage, V_{CLAMP}, is normally regulated above the COMP voltage to provide adequate headroom during a response to a load-on transient. If the COMP voltage rises quickly during an overloaded or shorted output condition, the on-time pulse terminates, thereby limiting the on-time and peak inductor current. Moreover, the CLAMP voltage is reduced if additional valley current limit events occur, further reducing the average output current. If the overcurrent condition exists for 128 continuous clock cycles, a hiccup event is triggered and SS is pulled low for 8192 clock cycles before a soft-start sequence is initiated.

8.4 Device Functional Modes

8.4.1 Shutdown Mode

The EN/UVLO pin provides ON / OFF control for the LV5144. When the EN/UVLO voltage is below 0.37 V (typical), the device is in shutdown mode. Both the internal bias supply LDO and the switching regulator are off. The quiescent current in shutdown mode drops to 13.5 µA (typical) at V_{IN} = 48 V. The LV5144 also includes undervoltage protection of the internal bias LDO. If the internal bias supply voltage is below its UVLO threshold level, the switching regulator remains off.

8.4.2 Standby Mode

The internal bias supply LDO has a lower enable threshold than the switching regulator. When the EN/UVLO voltage exceeds 0.42 V (typical) and is below the precision enable threshold (1.2 V typically), the internal LDO is on and regulating. Switching action and output voltage regulation are disabled in standby mode.

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8.4.3 Active Mode

The LV5144 is in active mode when the VCC voltage is above its rising UVLO threshold of 5 V and the EN/UVLO voltage is above the precision EN threshold of 1.2 V. The simplest way to enable the LV5144 is to tie EN/UVLO to VIN. This allows self start-up of the LV5144 when the input voltage exceeds the VCC threshold plus the LDO dropout voltage from VIN to VCC.

8.4.4 Diode Emulation Mode

The LV5144 provides a diode emulation feature that can be enabled to prevent reverse (drain-to-source) current flow in the low-side MOSFET. When configured for diode emulation, the low-side MOSFET is switched off when reverse current flow is detected by sensing of the SW voltage using a zero-cross comparator. The benefit of this configuration is lower power loss at no-load and light-load conditions, the disadvantage being slower light-load transient response.

The diode emulation feature is configured with the SYNCIN pin. To enable diode emulation and thus achieve discontinuous conduction mode (DCM) operation at light loads, connect the SYNCIN pin to AGND or leave SYNCIN floating. If forced PWM (FPWM) continuous conduction mode (CCM) operation is desired, tie SYNCIN to VCC either directly or using a pullup resistor. Note that diode emulation mode is automatically engaged to prevent reverse current flow during a prebias start-up. A gradual change from DCM to CCM operation provides monotonic start-up performance.

8.4.5 Thermal Shutdown

The LV5144 includes an internal junction temperature monitor. If the temperature exceeds 175°C (typical), thermal shutdown occurs. When entering thermal shutdown, the device:

1. Turns off the high-side and low-side MOSFETs.
2. Pulls SS/TRK and PGOOD low.
3. Turns off the VCC regulator.
4. Initiates a soft-start sequence when the die temperature decreases by the thermal shutdown hysteresis of 20°C (typical).

This protection is a non-latching protection, and the device cycles into and out of thermal shutdown if the fault persists.

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9 Application and Implementation

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Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

9.1.1 Design and Implementation

9.1.2 Power Train Components

Comprehensive knowledge and understanding of the power train components are key to successfully completing a synchronous buck regulator design.

9.1.2.1 Inductor

For most applications, choose an inductance such that the inductor ripple current, ΔI_L, is between 30% and 40% of the maximum DC output current at nominal input voltage. Choose the inductance using Equation 7 based on a peak inductor current given by Equation 8.

$$L_F = \frac{V_{OUT}}{V_{IN}} \cdot \left(\frac{V_{IN} - V_{OUT}}{\Delta I_L \cdot F_{SW}} \right) \tag{7}$$

$$I_{L(peak)} = I_{OUT} + \frac{\Delta I_L}{2} \tag{8}$$

Check the inductor data sheet to ensure that the saturation current of the inductor is well above the peak inductor current of a particular design. Ferrite designs have very low core loss and are preferred at high switching frequencies, so design goals can then concentrate on copper loss and preventing saturation. Low inductor core loss is evidenced by reduced no-load input current and higher light-load efficiency. However, ferrite core materials exhibit a hard saturation characteristic and the inductance collapses abruptly when the saturation current is exceeded. This results in an abrupt increase in inductor ripple current, higher output voltage ripple, not to mention reduced efficiency and compromised reliability. Note that the saturation current of an inductor generally decreases as its core temperature increases. Of course, accurate overcurrent protection is key to avoiding inductor saturation.

9.1.2.2 Output Capacitors

Ordinarily, the output capacitor energy store of the regulator combined with the control loop response are prescribed to maintain the integrity of the output voltage within the dynamic (transient) tolerance specifications. The usual boundaries restricting the output capacitor in power management applications are driven by finite available PCB area, component footprint and profile, and cost. The capacitor parasitics—equivalent series resistance (ESR) and equivalent series inductance (ESL)—take greater precedence in shaping the load transient response of the regulator as the load step amplitude and slew rate increase.

The output capacitor, C_{OUT}, filters the inductor ripple current and provides a reservoir of charge for step-load transient events. Typically, ceramic capacitors provide extremely low ESR to reduce the output voltage ripple and noise spikes, while tantalum and electrolytic capacitors provide a large bulk capacitance in a relatively compact footprint for transient loading events.

Based on the static specification of peak-to-peak output voltage ripple denoted by ΔV_{OUT}, choose an output capacitance that is larger than that given by Equation 9.

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$$C_{OUT} \geq \frac{\Delta I_L}{8 \cdot F_{SW} \sqrt{\Delta V_{OUT}^2 - \left(R_{ESR} \cdot \Delta I_L\right)^2}} \quad (9)$$

図 9-1 conceptually illustrates the relevant current waveforms during both load step-up and step-down transitions. As shown, the large-signal slew rate of the inductor current is limited as the inductor current ramps to match the new load-current level following a load transient. This slew-rate limiting exacerbates the deficit of charge in the output capacitor, which must be replenished as rapidly as possible during and after the load step-up transient. Similarly, during and after a load step-down transient, the slew rate limiting of the inductor current adds to the surplus of charge in the output capacitor that must be depleted as quickly as possible.

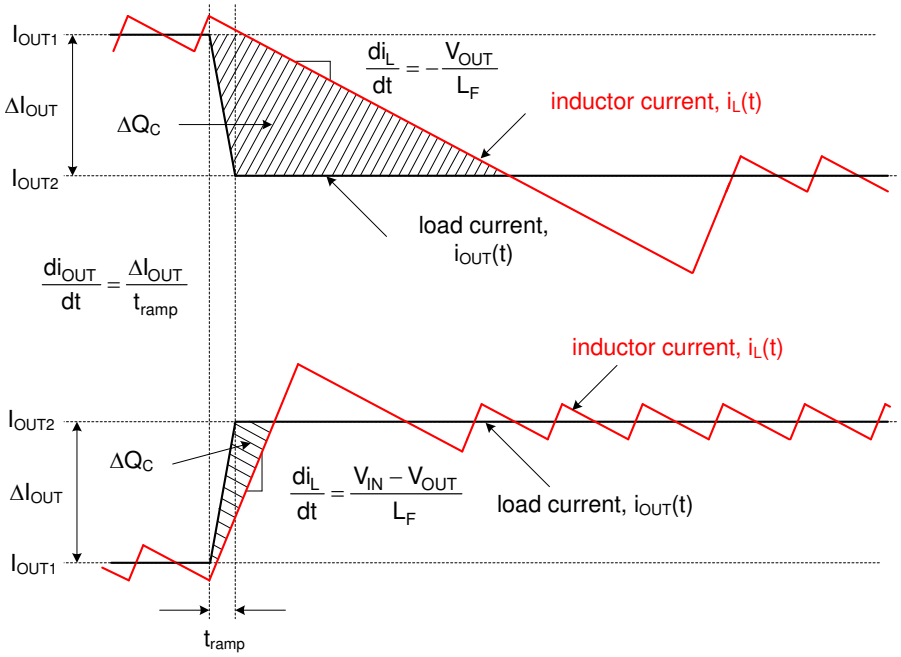


図 9-1. Load Transient Response Representation Showing C_{OUT} Charge Surplus or Deficit

In a typical regulator application of 48-V input to low output voltage (for example, 5 V), the load-off transient represents the worst case in terms of output voltage transient deviation. In that conversion ratio application, the steady-state duty cycle is approximately 10% and the large-signal inductor current slew rate when the duty cycle collapses to zero is approximately $-V_{OUT}/L$. Compared to a load-on transient, the inductor current takes much longer to transition to the required level. The surplus of charge in the output capacitor causes the output voltage to significantly overshoot. In fact, to deplete this excess charge from the output capacitor as quickly as possible, the inductor current must ramp below its nominal level following the load step. In this scenario, a large output capacitance can be advantageously employed to absorb the excess charge and limit the voltage overshoot.

To meet the dynamic specification of output voltage overshoot during such a load-off transient (denoted as $\Delta V_{OVERSHOOT}$ with step reduction in output current given by ΔI_{OUT}), the output capacitance must be larger than

$$C_{OUT} \geq \frac{L_F \cdot \Delta I_{OUT}^2}{\left(V_{OUT} + \Delta V_{OVERSHOOT}\right)^2 - V_{OUT}^2} \quad (10)$$

The ESR of a capacitor is provided in the manufacturer's data sheet either explicitly as a specification or implicitly in the impedance vs. frequency curve. Depending on type, size and construction, electrolytic capacitors have significant ESR, 5 mΩ and above, and relatively large ESL, 5 nH to 20 nH. PCB traces contribute some parasitic resistance and inductance as well. Ceramic output capacitors, on the other hand, have low ESR and ESL contributions at the switching frequency, and the capacitive impedance component dominates. However,

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depending on package and voltage rating of the ceramic capacitor, the effective capacitance can drop quite significantly with applied DC voltage and operating temperature.

Ignoring the ESR term in Equation 9 gives a quick estimation of the minimum ceramic capacitance necessary to meet the output ripple specification. One to four 47-µF, 10-V, X7R capacitors in 1206 or 1210 footprint is a common choice. Use Equation 10 to determine if additional capacitance is necessary to meet the load-off transient overshoot specification.

A composite implementation of ceramic and electrolytic capacitors highlights the rationale for paralleling capacitors of dissimilar chemistries yet complementary performance. The frequency response of each capacitor is accretive in that each capacitor provides desirable performance over a certain portion of the frequency range. While the ceramic provides excellent mid- and high-frequency decoupling characteristics with its low ESR and ESL to minimize the switching frequency output ripple, the electrolytic device with its large bulk capacitance provides low-frequency energy storage to cope with load transient demands.

9.1.2.3 Input Capacitors

Input capacitors are necessary to limit the input ripple voltage to the buck power stage due to switching-frequency AC currents. TI recommends using X5R or X7R dielectric ceramic capacitors to provide low impedance and high RMS current rating over a wide temperature range. To minimize the parasitic inductance in the switching loop, position the input capacitors as close as possible to the drain of the high-side MOSFET and the source of the low-side MOSFET. The input capacitor RMS current is given by Equation 11.

$$I_{CIN,rms} = \sqrt{D \cdot \left({I_{OUT}}^2 \cdot (1-D) + \frac{\Delta I_L^2}{12} \right)} \tag{11}$$

The highest input capacitor RMS current occurs at D = 0.5, at which point the RMS current rating of the capacitors must be greater than half the output current.

Ideally, the DC component of input current is provided by the input voltage source and the AC component by the input filter capacitors. Neglecting inductor ripple current, the input capacitors source current of amplitude (I_{OUT} − I_{IN}) during the D interval and sinks I_{IN} during the 1−D interval. Thus, the input capacitors conduct a square-wave current of peak-to-peak amplitude equal to the output current. It follows that the resultant capacitive component of AC ripple voltage is a triangular waveform. Together with the ESR-related ripple component, the peak-to-peak ripple voltage amplitude is given by Equation 12.

$$\Delta V_{IN} = \frac{I_{OUT} \cdot D \cdot (1-D)}{F_{SW} \cdot C_{IN}} + I_{OUT} \cdot R_{ESR} \tag{12}$$

The input capacitance required for a particular load current, based on an input voltage ripple specification of ΔV_{IN}, is given by Equation 13.

$$C_{IN} \geq \frac{D \cdot (1-D) \cdot I_{OUT}}{F_{SW} \cdot (\Delta V_{IN} - R_{ESR} \cdot I_{OUT})} \tag{13}$$

Low-ESR ceramic capacitors can be placed in parallel with higher valued bulk capacitance to provide optimized input filtering for the regulator and damping to mitigate the effects of input parasitic inductance resonating with high-Q ceramics. One bulk capacitor of sufficiently high current rating and two or three 2.2-µF 100-V X7R ceramic decoupling capacitors are usually sufficient. Select the input bulk capacitor based on its ripple current rating and operating temperature.

9.1.2.4 Power MOSFETs

The choice of power MOSFETs has significant impact on DC/DC regulator performance. A MOSFET with low on-state resistance, $R_{DS(on)}$, reduces conduction loss, whereas low parasitic capacitances enable faster transition times and reduced switching loss. Normally, the lower the $R_{DS(on)}$ of a MOSFET, the higher the gate charge and

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output charge (Q_G and Q_{OSS} respectively), and vice versa. As a result, the product $R_{DS(on)} \times Q_G$ is commonly specified as a MOSFET figure-of-merit. Low thermal resistance ensures that the MOSFET power dissipation does not result in excessive MOSFET die temperature.

The main parameters affecting power MOSFET selection in a LV5144 application are as follows:

- $R_{DS(on)}$ at V_{GS} = 7.5 V
- Drain-source voltage rating, BV_{DSS}, typically 60 V, 80 V, or 100 V, depending on maximum input voltage
- Gate charge parameters at V_{GS} = 7.5 V
- Output charge, Q_{OSS}, at the relevant input voltage
- Body diode reverse recovery charge, Q_{RR}
- Gate threshold voltage, $V_{GS(th)}$, derived from the Miller plateau evident in the Q_G versus V_{GS} plot in the MOSFET data sheet. With a Miller plateau voltage typically in the range of 2 V to 5 V, the 7.5-V gate drive amplitude of the LV5144 provides an adequately-enhanced MOSFET when on and a margin against Cdv/dt shoot-through when off.

The MOSFET-related power losses are summarized by the equations presented in 表 9-1, where suffixes 1 and 2 represent high-side and low-side MOSFET parameters, respectively. While the influence of inductor ripple current is considered, second-order loss modes, such as those related to parasitic inductances and SW node ringing, are not included. Consult the *LV5144 Quickstart Calculator* to assist with power loss calculations.

表 9-1. Buck Regulator MOSFET Power Losses

POWER LOSS MODE	HIGH-SIDE MOSFET	LOW-SIDE MOSFET
MOSFET conduction(2) (3)	$P_{cond1} = D \cdot \left({I_{OUT}}^2 + \frac{\Delta I_L^2}{12} \right) \cdot R_{DS(on)1}$	$P_{cond2} = D' \cdot \left({I_{OUT}}^2 + \frac{\Delta I_L^2}{12} \right) \cdot R_{DS(on)2}$
MOSFET switching	$P_{sw1} = \frac{V_{IN} \cdot F_{SW}}{2} \left[\left(I_{OUT} - \frac{\Delta I_L}{2} \right) \cdot t_R + \left(I_{OUT} + \frac{\Delta I_L}{2} \right) \cdot t_F \right]$	Negligible
MOSFET gate drive(1)	$P_{Gate1} = V_{CC} \cdot F_{SW} \cdot Q_{G1}$	$P_{Gate2} = V_{CC} \cdot F_{SW} \cdot Q_{G2}$
MOSFET output charge(4)	$P_{Coss} = F_{SW} \cdot \left(V_{IN} \cdot Q_{oss2} + E_{oss1} - E_{oss2} \right)$	
Body diode conduction	N/A	$P_{cond_{BD}} = V_F \cdot F_{SW} \left[\left(I_{OUT} + \frac{\Delta I_L}{2} \right) \cdot t_{dt1} + \left(I_{OUT} - \frac{\Delta I_L}{2} \right) \cdot t_{dt2} \right]$
Body diode reverse recovery(5)	$P_{RR} = V_{IN} \cdot F_{SW} \cdot Q_{RR2}$	

(1) Gate drive loss is apportioned based on the internal gate resistance of the MOSFET, externally-added series gate resistance and the relevant gate driver resistance of the LV5144.
(2) MOSFET $R_{DS(on)}$ has a positive temperature coefficient of approximately 4500 ppm/°C. The MOSFET junction temperature, T_J, and its rise over ambient temperature is dependent upon the device total power dissipation and its thermal impedance. When operating at or near minimum input voltage, ensure that the MOSFET $R_{DS(on)}$ is rated at V_{GS} = 4.5 V.
(3) D' = 1–D is the duty cycle complement.
(4) MOSFET output capacitances, C_{oss1} and C_{oss2}, are highly non-linear with voltage. These capacitances are charged losslessly by the inductor current at high-side MOSFET turn-off. During turn-on, however, a current flows from the input to charge C_{oss2} of the low-side MOSFET. E_{oss1}, the energy of C_{oss1}, is dissipated at turnon, but this is offset by the stored energy E_{oss2} on C_{oss2}.
(5) MOSFET body diode reverse recovery charge, Q_{RR}, depends on many parameters, particularly forward current, current transition speed, and temperature.

The high-side (control) MOSFET carries the inductor current during the PWM on-time (or D interval) and typically incurs most of the switching losses. It is therefore imperative to choose a high-side MOSFET that balances conduction and switching loss contributions. The total power dissipation in the high-side MOSFET is the sum of the losses due to conduction, switching (voltage-current overlap), output charge, and typically two-thirds of the net loss attributed to body diode reverse recovery.

The low-side (synchronous) MOSFET carries the inductor current when the high-side MOSFET is off (or 1–D interval). The low-side MOSFET switching loss is negligible as it is switched at zero voltage – current just commutates from the channel to the body diode or vice versa during the transition deadtimes. The LV5144, with

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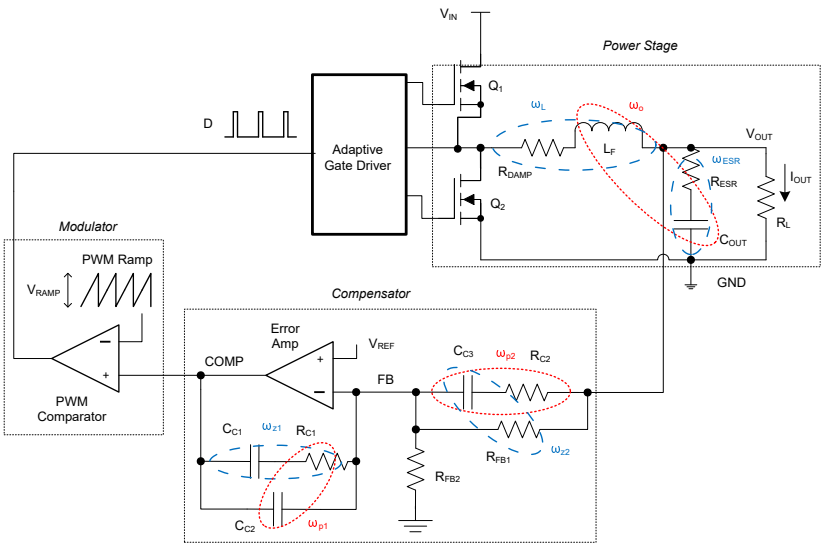
its adaptive gate drive timing, minimizes body diode conduction losses when both MOSFETs are off. Such losses scale directly with switching frequency.

In high step-down ratio applications, the low-side MOSFET carries the current for a large portion of the switching period. Therefore, to attain high efficiency, it is critical to optimize the low-side MOSFET for low $R_{DS(on)}$. In cases where the conduction loss is too high or the target $R_{DS(on)}$ is lower than available in a single MOSFET, connect two low-side MOSFETs in parallel. The total power dissipation of the low-side MOSFET is the sum of the losses due to channel conduction, body diode conduction, and typically one-third of the net loss attributed to body diode reverse recovery. The LV5144 is well suited to drive TI's portfolio of NexFET™ power MOSFETs.

9.1.3 Control Loop Compensation

The poles and zeros inherent to the power stage and compensator are respectively illustrated by red and blue dashed rings in the schematic embedded in 表 9-2. The compensation network typically employed with voltage-mode control is a Type-III circuit with three poles and two zeros. One compensator pole is located at the origin to realize high DC gain. The normal compensation strategy uses two compensator zeros to counteract the LC double pole, one compensator pole located to nullify the output capacitor ESR zero, with the remaining compensator pole located at one-half switching frequency to attenuate high frequency noise. The resistor divider network to FB determines the desired output voltage. Note that the lower feedback resistor, R_{FB2}, has no impact on the control loop from an AC standpoint because the FB node is the input to an error amplifier and is effectively at AC ground. Hence, the control loop is designed irrespective of output voltage level. The proviso here is the necessary output capacitance derating with bias voltage and temperature.

表 9-2. Buck Regulator Poles and Zeros



POWER STAGE POLES	POWER STAGE ZEROS	COMPENSATOR POLES	COMPENSATOR ZEROS
$\omega_o = \frac{1}{\sqrt{L_F \cdot C_{OUT}\left(\frac{1+R_{ESR}/R_L}{1+R_{ESR}/R_{DAMP}}\right)}} \cong \frac{1}{\sqrt{L_F \cdot C_{OUT}}}$ (1) (2)	$\omega_{ESR} = \frac{1}{R_{ESR} \cdot C_{OUT}}$	$\omega_{p1} = \frac{1}{R_{C1} \cdot (C_{C1} \parallel C_{C2})} \cong \frac{1}{R_{C1} \cdot C_{C2}}$	$\omega_{z1} = \frac{1}{R_{C1} \cdot C_{C1}}$
	$\omega_L = \frac{L_F}{R_{DAMP}}$	$\omega_{p2} = \frac{1}{R_{C2} \cdot C_{C3}}$	$\omega_{z2} = \frac{1}{(R_{FB1}+R_{C2}) \cdot C_{C3}}$

(1) R_{ESR} represents the ESR of the output capacitor C_{OUT}.

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(2) $R_{DAMP} = D \cdot R_{DS(on)high\text{-}side} + (1–D) \cdot R_{DS(on)\ low\text{-}side} + R_{DCR}$, shown as a lumped element in the schematic, represents the effective series damping resistance.

The small-signal open-loop response of a buck regulator is the product of modulator, power train and compensator transfer functions. The power stage transfer function can be represented as a complex pole pair associated with the output LC filter and a zero related to the ESR of the output capacitor. The DC (and low frequency) gain of the modulator and power stage is V_{IN}/V_{RAMP}. The gain from COMP to the average voltage at the input of the LC filter is held essentially constant by the PWM line feedforward feature of the LV5144 (15 V/V or 23.5 dB).

Complete expressions for small-signal frequency analysis are presented in 表 9-3. The transfer functions are denoted in normalized form. While the loop gain is of primary importance, a regulator is not specified directly by its loop gain but by its performance related characteristics, namely closed-loop output impedance and audio susceptibility.

表 9-3. Buck Regulator Small-Signal Analysis

TRANSFER FUNCTION	EXPRESSION
Open-loop transfer function	$T_v(s) = \frac{\hat{v}_{comp}(s)}{\hat{v}_o(s)} \cdot \frac{\hat{v}_o(s)}{\hat{d}(s)} \cdot \frac{\hat{d}(s)}{\hat{v}_{comp}(s)} = G_c(s) \cdot G_{vd}(s) \cdot F_M$
Duty-cycle-to-output transfer function	$G_{vd}(s) = \frac{\hat{v}_o(s)}{\hat{d}(s)}\Big\vert_{\substack{\hat{v}_{in}(s)=0 \\ \hat{i}_o(s)=0}} = V_{IN} \frac{1+\frac{s}{\omega_{ESR}}}{1+\frac{s}{Q_o\omega_o}+\frac{s^2}{\omega_o^2}}$
Compensator transfer function(1)	$G_c(s) = \frac{\hat{v}_{comp}(s)}{\hat{v}_o(s)} = K_{mid} \frac{\left(1+\frac{\omega_{z1}}{s}\right)\left(1+\frac{s}{\omega_{z2}}\right)}{\left(1+\frac{s}{\omega_{p1}}\right)\left(1+\frac{s}{\omega_{p2}}\right)}$
Modulator transfer function	$F_M = \frac{\hat{d}(s)}{\hat{v}_{comp}(s)} = \frac{1}{V_{RAMP}}$

(1) $K_{mid} = R_{C1}/R_{FB1}$ is the mid-band gain of the compensator. By expressing one of the compensator zeros in inverted zero format, the mid-band gain is denoted explicitly.

図 9-2 shows the open-loop response gain and phase. The poles and zeros of the system are marked with x and o symbols, respectively, and a + symbol indicates the crossover frequency. When plotted on a log (dB) scale, the open-loop gain is effectively the sum of the individual gain components from the modulator, power stage, and compensator (see 図 9-3). The open-loop response of the system is measured experimentally by breaking the loop, injecting a variable-frequency oscillator signal, and recording the ensuing frequency response using a network analyzer setup.

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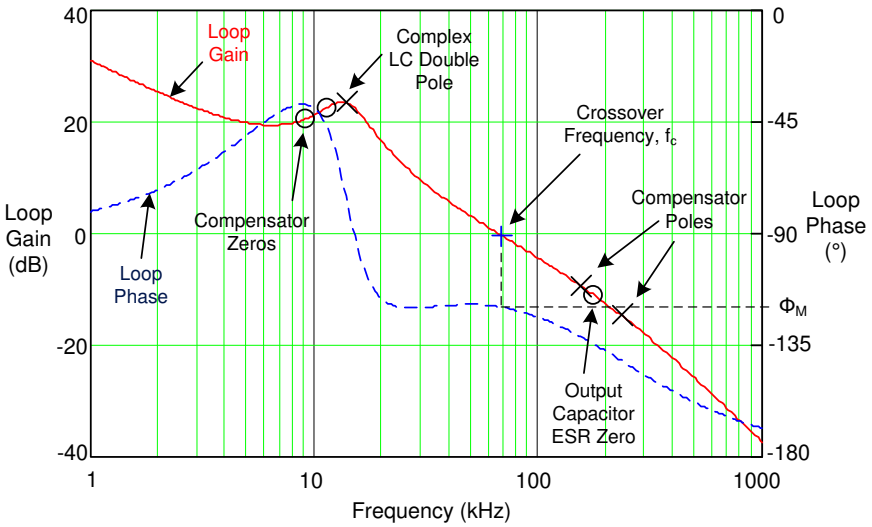


図 9-2. Typical Buck Regulator Loop Gain and Phase With Voltage-Mode Control

If the pole located at ω_{p1} cancels the zero located at ω_{ESR} and the pole at ω_{p2} is located well above crossover, the expression for the loop gain, $T_v(s)$ in 表 9-3, can be manipulated to yield the simplified expression given in 式 14.

$$T_v(s) = R_{C1} \cdot C_{C3} \cdot \frac{V_{IN}}{V_{RAMP}} \cdot \frac{\omega_o^2}{s} \tag{14}$$

Essentially, a multi-order system is reduced to a single-order approximation by judicious choice of compensator components. A simple solution for the crossover frequency (denoted as f_c in 図 9-2) with Type-III voltage-mode compensation is derived as shown in 式 15 and 式 16.

$$\omega_c = 2\pi \cdot f_c = \omega_o \cdot K_{mid} \cdot \frac{V_{IN}}{V_{RAMP}} \tag{15}$$

$$K_{mid} = \frac{f_c}{f_o} \cdot \frac{1}{k_{FF}} = \frac{R_{C1}}{R_{FB1}} \tag{16}$$

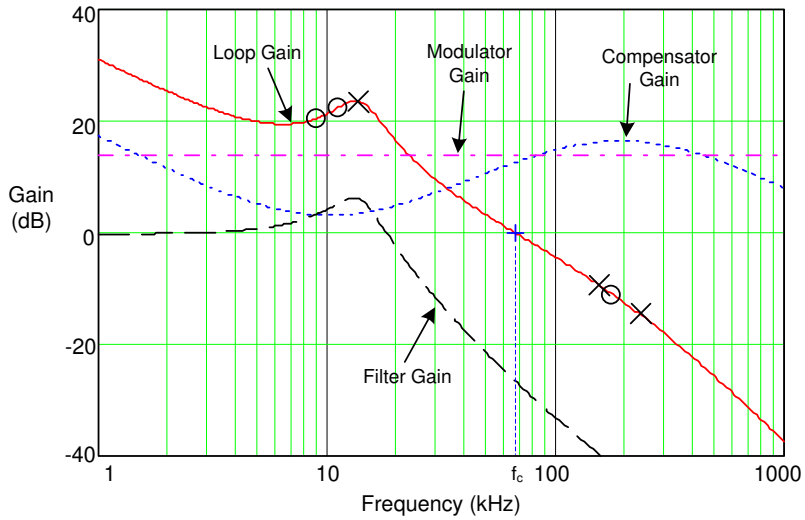


図 9-3. Buck Regulator Constituent Gain Components

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The loop crossover frequency is usually selected between one-tenth to one-fifth of switching frequency. Inserting an appropriate crossover frequency into Equation 16 gives a target for the mid-band gain of the compensator, K_{mid}. Given an initial value for R_{FB1}, R_{FB2} is then selected based on the desired output voltage. Values for R_{C1}, R_{C2}, C_{C1}, C_{C2}, and C_{C3} are calculated from the design expressions listed in 表 9-4, with the premise that the compensator poles and zeros are set as follows: $\omega_{z1} = 0.5 \cdot \omega_o$, $\omega_{z2} = \omega_o$, $\omega_{p1} = \omega_{SW}/2$, and $\omega_{p2} = \omega_{ESR}$.

表 9-4. Compensation Component Selection

RESISTORS	CAPACITORS
$R_{FB2} = \frac{R_{FB1}}{(V_{OUT}/V_{REF}) - 1}$	$C_{C1} = \frac{1}{\omega_{z1} \cdot R_{C1}}$
$R_{C1} = K_{mid} \cdot R_{FB1}$	$C_{C2} = \frac{1}{\omega_{p1} \cdot R_{C1}}$
$R_{C2} = \frac{1}{\omega_{p2} \cdot C_{C3}}$	$C_{C3} = \frac{1}{\omega_{z2} \cdot R_{FB1}}$

Referring to the bode plot in 図 9-2, the phase margin, indicated as φ_M, is the difference between the loop phase and –180° at crossover. A target of 50° to 70° for this parameter is considered ideal. Additional phase boost is dialed in by locating the compensator zeros at a frequency lower than the LC double pole. This helps mitigate the phase dip associated with the LC filter, particularly at light loads when the Q-factor is higher and the phase dip becomes especially prominent. The ramification of low phase in the frequency domain is an under-damped transient response in the time domain.

The power supply designer now has all the necessary expressions to optimally position the loop crossover frequency while maintaining adequate phase margin over the required line, load and temperature operating ranges. The *LV5144 Quickstart Calculator* is available to expedite these calculations and to adjust the bode plot as needed.

9.1.4 EMI Filter Design

Switching regulators exhibit negative input impedance, which is lowest at the minimum input voltage. An underdamped LC filter exhibits a high output impedance at the resonant frequency of the filter. For stability, the filter output impedance must be less than the absolute value of the converter input impedance.

$$Z_{IN} = \left| -\frac{V_{IN(min)}^2}{P_{IN}} \right| \tag{17}$$

The EMI filter design steps are as follows:

- Calculate the required attenuation of the EMI filter at the switching frequency, where C_{IN} represents the existing capacitance at the input of the switching converter.
- Input filter inductor L_{IN} is usually selected between 1 µH and 10 µH, but it can be lower to reduce losses in a high current design.
- Calculate input filter capacitor C_F.

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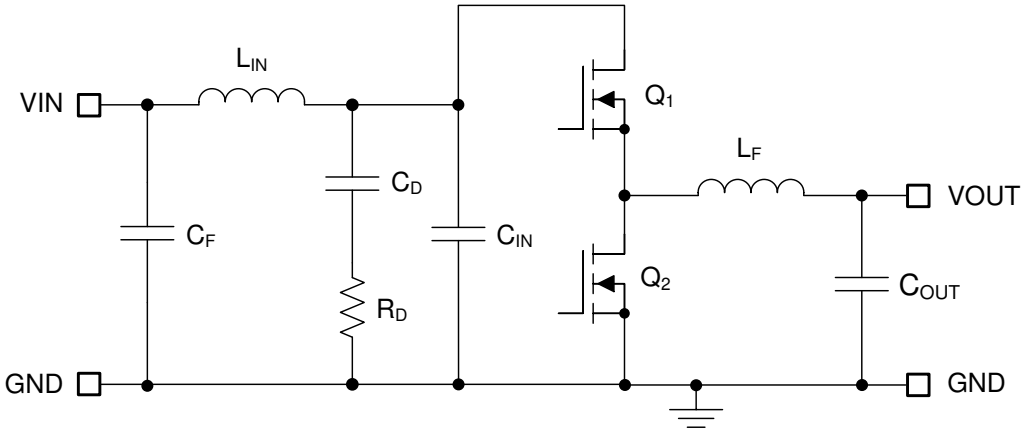


図 9-4. Buck Regulator With π-Stage EMI Filter

By calculating the first harmonic current from the Fourier series of the input current waveform and multiplying it by the input impedance (the impedance is defined by the existing input capacitor C_{IN}), a formula is derived to obtain the required attenuation as shown by Equation 18.

$$Attn = 20\log\left(\frac{I_{L(PEAK)}}{\pi^2 \cdot F_{SW} \cdot C_{IN}} \cdot \sin\left(\pi \cdot D_{MAX}\right) \cdot \frac{1}{1\,\mu V}\right) - V_{MAX} \tag{18}$$

where

- V_{MAX} is the noise specification in dBµV from the applicable EMI standard, for example CISPR 32 Class B
- C_{IN} is the existing input capacitance of the buck regulator
- D_{MAX} is the maximum duty cycle
- I_{PEAK} is the peak inductor current

For filter design purposes, the current at the input can be modeled as a square-wave. Determine the EMI filter capacitance C_F from Equation 19.

$$C_F = \frac{1}{L_{IN}}\left(\frac{10^{\frac{|Attn|}{40}}}{2\pi \cdot F_{SW}}\right)^2 \tag{19}$$

Adding an input filter to a switching regulator modifies the control-to-output transfer function. The output impedance of the filter must be sufficiently small such that the input filter does not significantly affect the loop gain of the buck converter. The impedance peaks at the filter resonant frequency. The resonant frequency of the filter is given by Equation 20.

$$f_{res} = \frac{1}{2\pi \cdot \sqrt{L_{IN} \cdot C_F}} \tag{20}$$

The purpose of R_D is to reduce the peak output impedance of the filter at the resonant frequency. Capacitor C_D blocks the DC component of the input voltage to avoid excessive power dissipation in R_D. Capacitor C_D must have lower impedance than R_D at the resonant frequency with a capacitance value greater than that of the input capacitor C_{IN}. This prevents C_{IN} from interfering with the cutoff frequency of the main filter. Added damping is needed when the output impedance of the filter is high at the resonant frequency (Q of filter formed by L_{IN} and C_{IN} is too high). An electrolytic capacitor C_D can be used for damping with a value given by Equation 21.

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$$C_D \geq 4 \cdot C_{IN} \quad (21)$$

Select the damping resistor R_D using Equation 22.

$$R_D = \sqrt{\frac{L_{IN}}{C_{IN}}} \quad (22)$$

9.2 Typical Applications

For step-by-step design procedure, circuit schematics, bill of materials, PCB files, simulation and test results of an LV5144-powered implementation, see *TI Designs* reference design library.

9.2.1 Design 1 – 12-A High-Efficiency Synchronous Buck DC/DC Regulator

図 9-5 shows the schematic diagram of a 5-V, 12-A buck regulator with a switching frequency of 300 kHz. In this example, the target efficiencies are 94% and 92% at input voltages of 24 V and 48 V, respectively. The input UVLO is set to turn on and off at 8 V and 7 V, respectively. The switching frequency is set by means of a synchronization input signal at 300 kHz, and the free-running switching frequency (in the event that the synchronization signal is removed) is set at 250 kHz by resistor R_{RT}. In terms of control loop performance, the target loop crossover frequency is 40 kHz with a phase margin greater than 50°. The output voltage soft-start time is 6 ms.

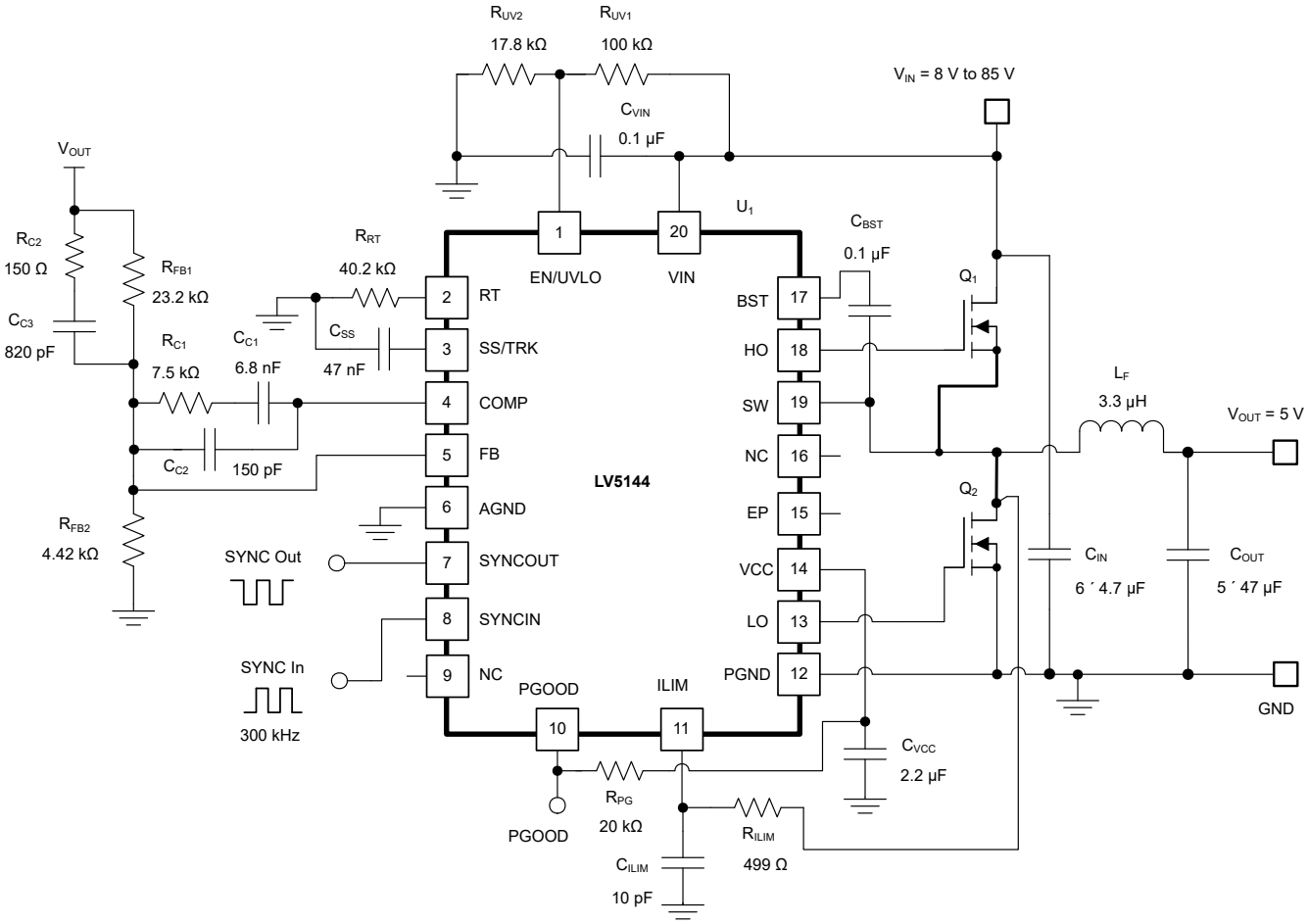


図 9-5. Application Circuit 1 With LV5144-Q1 48-V to 5-V, 12-A Buck Regulator at 300 kHz

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This and subsequent design examples are provided herein to showcase the LV5144 controller in several different applications. Depending on the source impedance of the input supply bus, an electrolytic capacitor can be required at the input to ensure stability, particularly at low input voltage and high output current operating conditions. See セクション 9.3 for more detail.

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9.2.1.1 Design Requirements

The intended input, output, and performance-related parameters pertinent to this design example are shown in 表 9-5.

表 9-5. Design Parameters

DESIGN PARAMETER	VALUE
Input voltage range (steady state)	8 V to 85 V
Input transient voltage (peak)	95 V
Output voltage and current	5 V, 12 A
Input voltage UVLO thresholds	8 V on, 7 V off
Switching frequency (SYNC in)	300 kHz
Output voltage regulation	±1%
Load transient peak voltage deviation	< 100 mV

9.2.1.2 Detailed Design Procedure

The selected buck converter powertrain components are cited in 表 9-6, and many of the components are available from multiple vendors. The MOSFETs in particular are chosen for both lowest conduction and switching power loss, as discussed in detail in セクション 9.1.2.4.

The current limit setpoint in this design is set at 19 A based on the resistor R_{ILIM} and the 6-mΩ $R_{DS(on)}$ of the low-side MOSFET (typical at T_J = 25°C and V_{GS} = 7.5 V). This design uses a low-DCR, metal-powder inductor, and all-ceramic output capacitor implementation.

表 9-6. List of Materials for Application Circuit 1

REFERENCE DESIGNATOR	QTY	SPECIFICATION	MANUFACTURER	PART NUMBER
C_{IN}	6	4.7 µF, 100 V, X7S, 1210, ceramic	TDK	CGA6M3X7S2A475K200
			Murata	GCM32DC72A475KE02L
			Taiyo Yuden	HMK325C7475MMHPE
C_{OUT}	5	47 µF, 6.3 V, X7R, 1210, ceramic	Murata	GCM32ER70J476KE19L
			Taiyo Yuden	JMK325B7476KMHTR
		47 µF, 6.3 V, X7S, 1210, ceramic	TDK	CGA6P1X7S0J476M
L_F	1	3.3 µH, 6.25 mΩ, 19 A, 10.85 × 10.0 × 5.2 mm	Cyntec	VCHA105D-3R3M
		3.3 µH, 5.8 mΩ, 28.6 A, 10.5 × 10.0 × 6.5 mm	TDK	SPM10065VTT-3R3M-D
		3.3 µH, 6.0 mΩ, 17 A, 10.9 × 10.0 × 6.0 mm	Panasonic	ETQP6M3R3YLC
Q_1	1	100 V, 22 mΩ, MOSFET, SON 5 × 6	Onsemi	NVMFS6B25NL
Q_2	1	100 V, 6 mΩ, MOSFET, SON 5 × 6	Onsemi	FDWS86068-F085
U_1	1	Wide V_{IN} synchronous buck controller	Texas Instruments	LV5144RGYR

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9.2.1.3 Application Curves

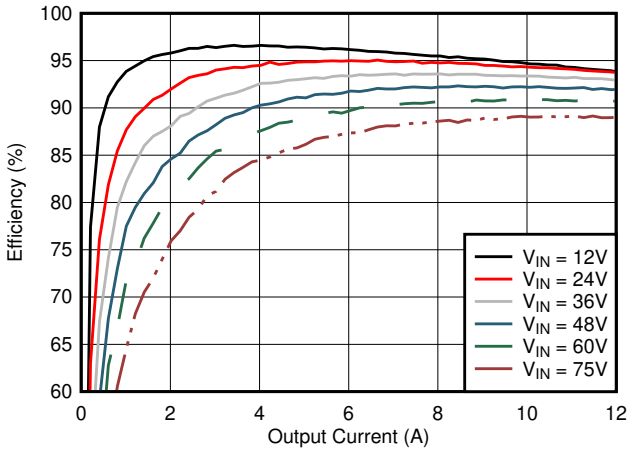
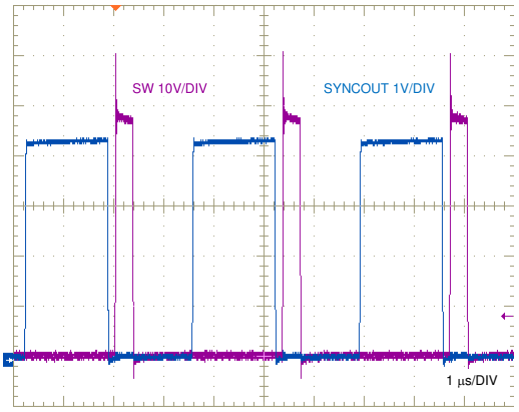
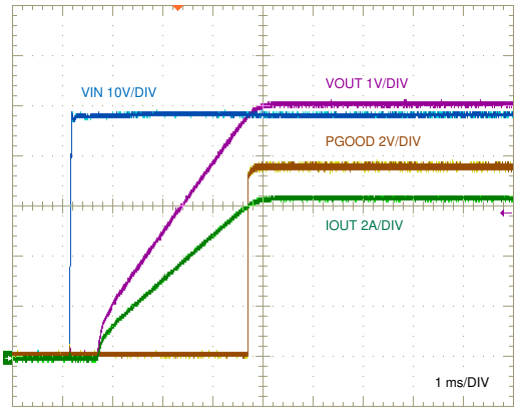


図 9-6. Efficiency and Power Loss vs I_{OUT} and V_{IN}



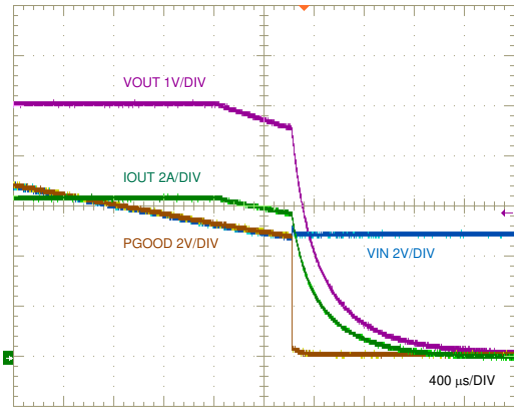
V_{IN} = 48 V I_{OUT} = 6 A

図 9-7. SYNCOUT and SW Node Voltages



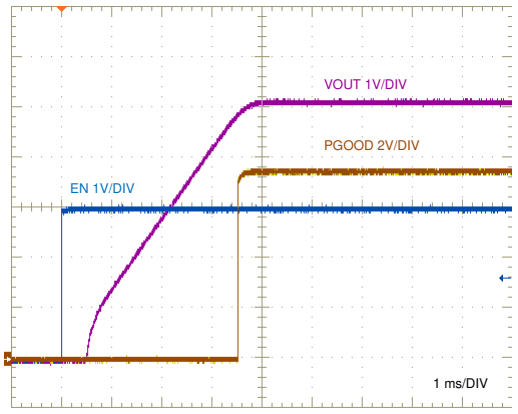
V_{IN} step to 48 V 0.8-Ω Load

図 9-8. Start-Up, Resistive Load



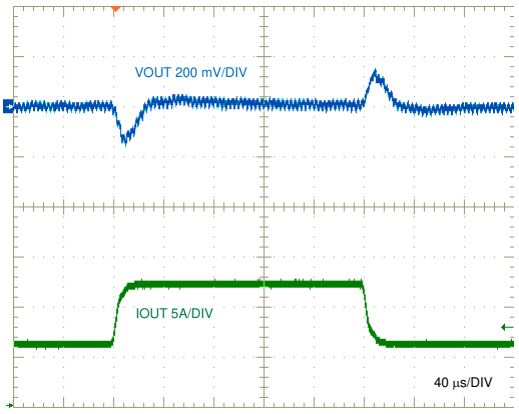
V_{IN} 48 V to 6 V 0.8-Ω Load

図 9-9. Shutdown Through UVLO



V_{IN} = 48 V 0.8-Ω Load

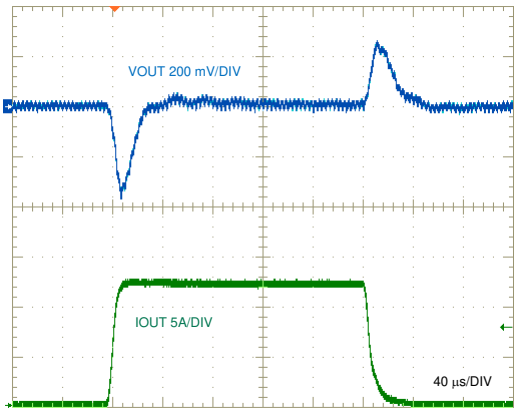
図 9-10. ENABLE ON, Resistive Load



V_{IN} = 48 V

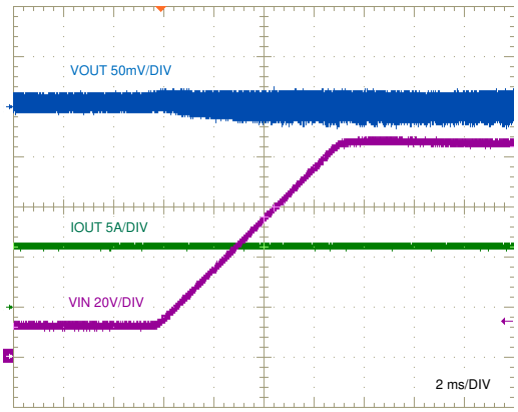
図 9-11. Load Transient Response, 6 A to 12 A to 6 A

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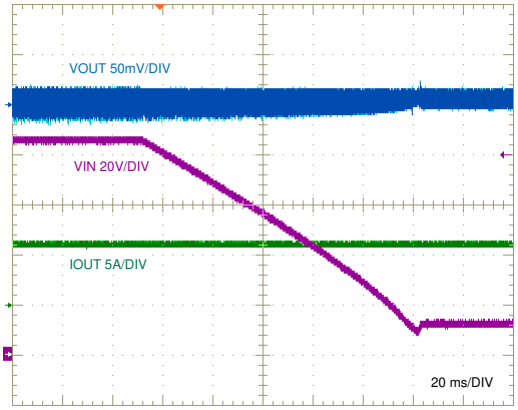
V_{IN} = 48 V

図 9-12. Load Transient Response, 0 A to 12 A to 0 A



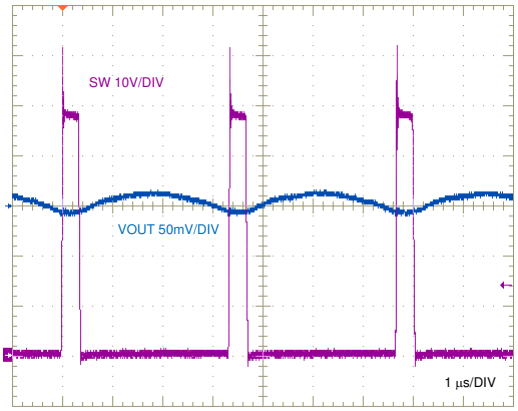
I_{OUT} = 6 A

図 9-13. Line Transient Response, 12 V to 85 V



I_{OUT} = 6 A

図 9-14. Line Transient Response, 85 V to 12 V



V_{IN} = 48 V I_{OUT} = 0 A

図 9-15. SW Node and Output Ripple Voltages

9.2.2 Design 2 – High Density, 12-V, 8-A Rail From 48-V Telecom Power

図 9-16 shows the schematic diagram of a 400-kHz, 12-V output, 8-A synchronous buck regulator intended for 48-V telecom applications.

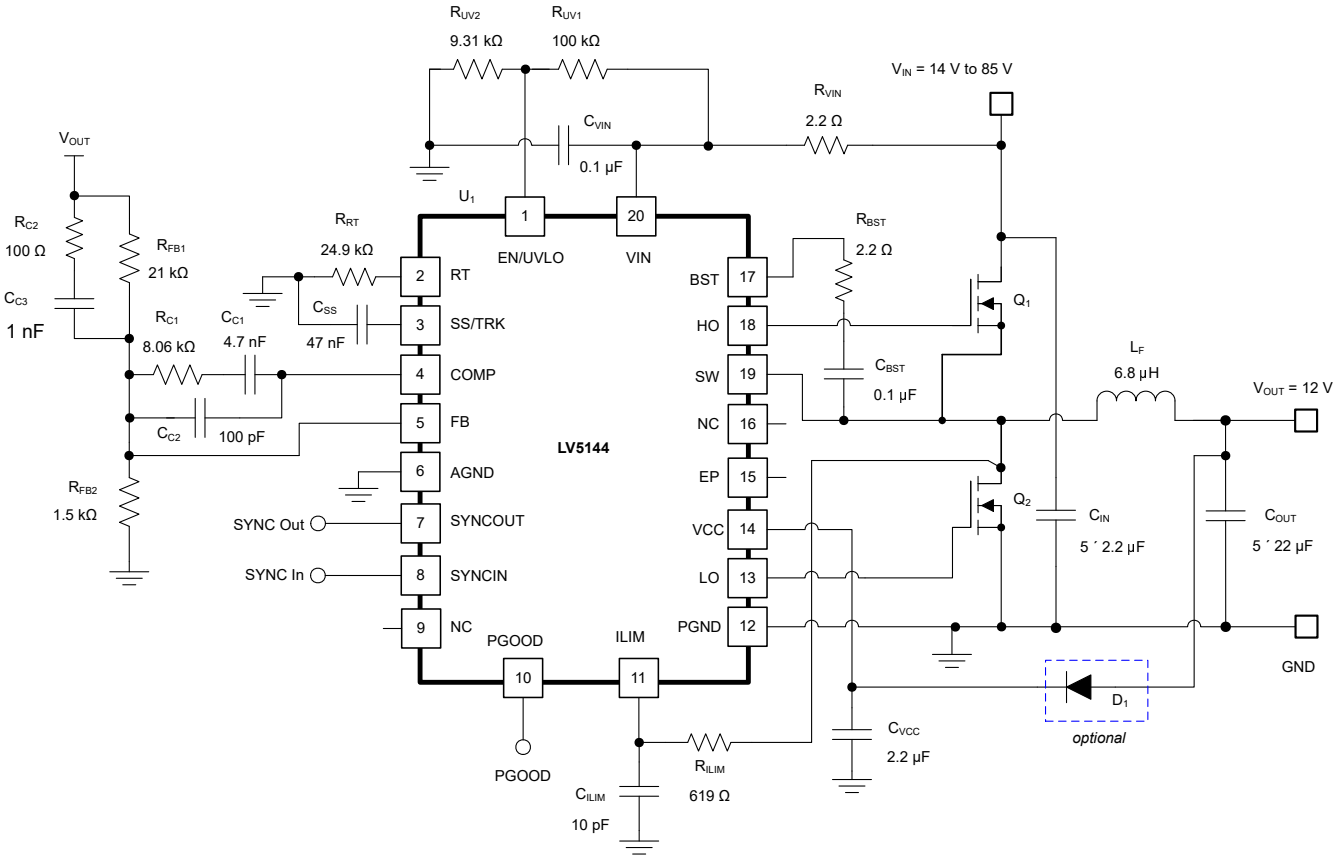


図 9-16. Application Circuit 2 With LV5144 48-V to 12-A Synchronous Buck Regulator at 400 kHz

9.2.2.1 Design Requirements

The required input, output, and performance parameters for this application example are shown in 表 9-7.

表 9-7. Design Parameters

DESIGN PARAMETER	VALUE
Input voltage range (steady state)	14 V to 85 V
Input transient voltage (peak)	90 V
Output voltage and current	12 V, 8 A
Input UVLO thresholds	14 V on, 13 V off
Switching frequency	400 kHz
Output voltage regulation	±1%
Load transient peak voltage deviation, 4-A load step	< 120 mV

9.2.2.2 Detailed Design Procedure

A high power density, high-efficiency regulator design uses 100-V power MOSFETs in SON 5-mm × 6-mm packages, together with a low-DCR inductor and all-ceramic capacitor design. The design occupies a footprint of 30 mm × 15 mm on a single-sided PCB. The overcurrent (OC) setpoint in this design is set at 12 A based on the resistor R_{ILIM} and the 10-mΩ $R_{DS(on)}$ of the low-side MOSFET (typical at T_J = 25°C and V_{GS} = 10 V). The 12-V output is connected to VCC through a diode, D1, to reduce IC bias power dissipation at high input voltages.

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The selected buck converter powertrain components are cited in 表 9-8, including power MOSFETs, buck inductor, input and output capacitors, and ICs. Using the *LV5144 Quickstart Calculator*, compensation components are selected based on a target loop crossover frequency of 40 kHz and phase margin greater than 55°. The output voltage soft-start time is 6 ms based on the selected soft-start capacitance, C_{SS}, of 47 nF.

表 9-8. List of Materials for Application Circuit 2

REFERENCE DESIGNATOR	QTY	SPECIFICATION	MANUFACTURER	PART NUMBER
C_{IN}	5	2.2 µF, 100 V, X7R, 1210, ceramic	TDK	CGA6N3X7R2A225K
			Taiyo Yuden	HMK325B7225KM-P
		2.2 µF, 100 V, X7S, 1206, ceramic	Murata	GCM31CC72A225KE02
C_{OUT}	5	22 µF, 25 V, X7R, 1210, ceramic	TDK	CGA6P3X7R1E226M
			Murata	GCM32EC71E226KE36
			Taiyo Yuden	TMK325B7226KMHT
L_F	1	6.8 µH, 12 mΩ, 13.3 A, 10.85 × 10.0 × 5.2 mm	Cyntec	VCHA105D-6R8MS6
		6.8 µH, 13.3 mΩ, 21.4 A, 10.5 × 10.0 × 6.5 mm	TDK	SPM10065VT-6R8M-D
Q_1	1	100 V, 22 mΩ, MOSFET, SON 5 × 6	Onsemi	NVMFS6B25NLT1G
Q_2	1	100 V, 10 mΩ, MOSFET, SON 5 × 6	Onsemi	NVMFS6B14NLT1G
U_1	1	Wide V_{IN} synchronous buck controller	Texas Instruments	LV5144RGYR

As shown in 図 9-16, a 2.2-Ω resistor in series with C_{BST} is used to slow the turn-on transition of the high-side MOSFET, reducing the spike amplitude and ringing of the SW node voltage and minimizing the possibility of Cdv/dt-induced shoot-through of the low-side MOSFET. If needed, place an RC snubber (for example, 2.2 Ω and 100 pF) close to the drain (SW node) and source (PGND) terminals of the low-side MOSFET to further attenuate any SW node voltage overshoot or ringing. Please refer to the application note *Reduce Buck Converter EMI and Voltage Stress by Minimizing Inductive Parasitics* for more detail.

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9.2.2.3 Application Curves

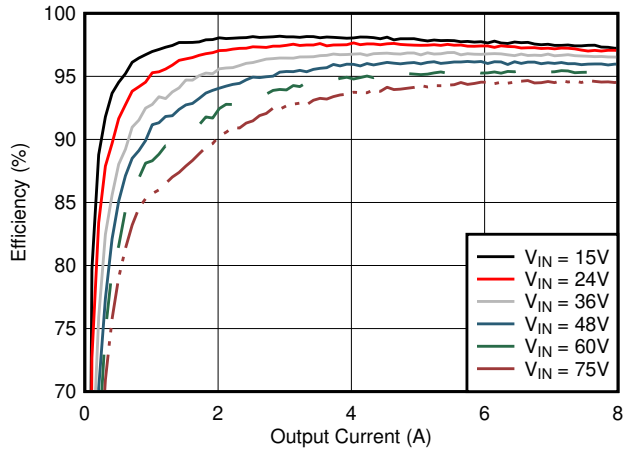
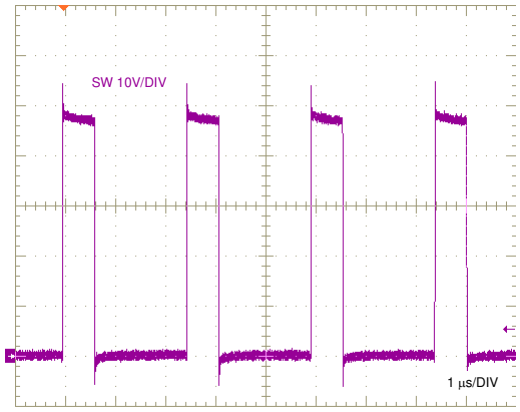
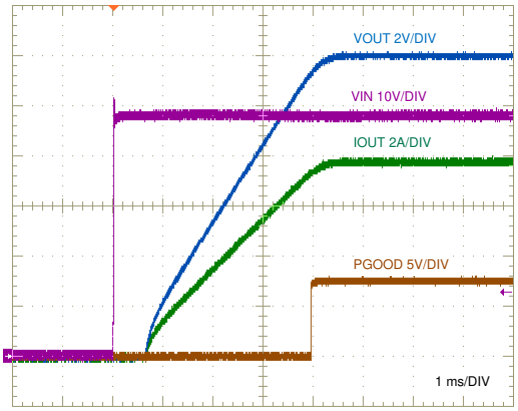


図 9-17. Efficiency vs I_{OUT} and V_{IN}



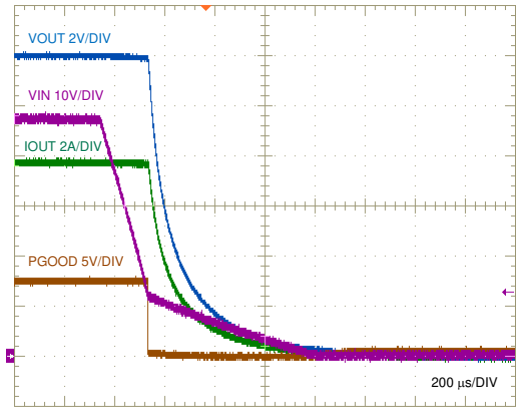
V_{IN} = 48 V I_{OUT} = 8 A

図 9-18. SW Node Voltages



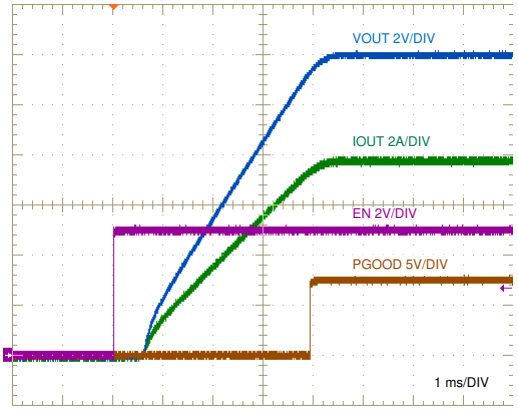
V_{IN} step to 48 V 1.5-Ω Load

図 9-19. Start-Up, 8-A Resistive Load



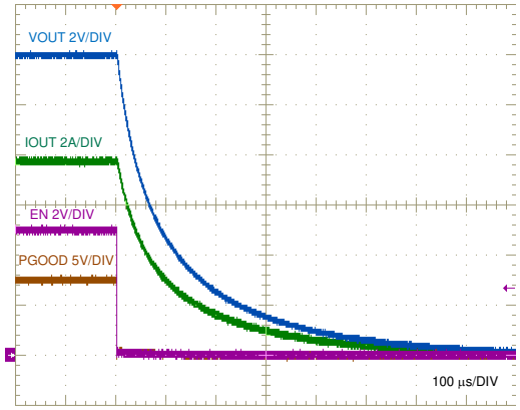
1.5-Ω Load

図 9-20. Shutdown By Input UVLO, 8-A Resistive Load



V_{IN} = 48 V 1.5-Ω Load

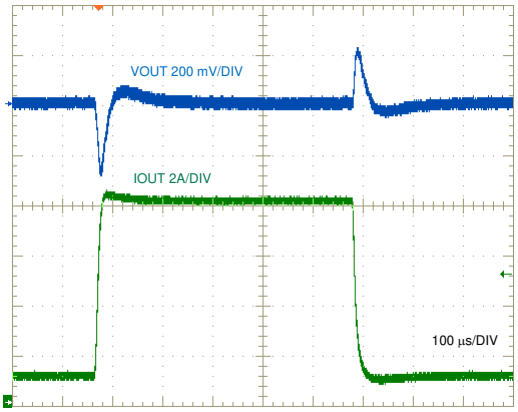
図 9-21. ENABLE ON, 10-A Resistive Load



V_{IN} = 48 V 1.5-Ω Load

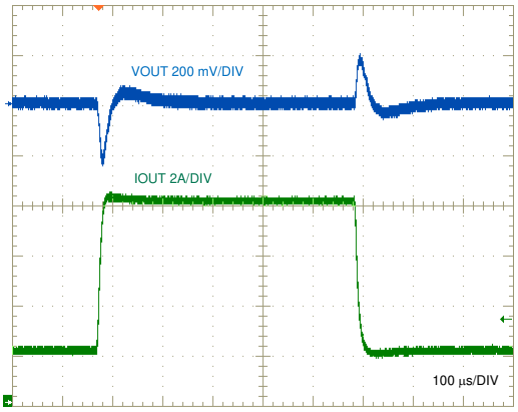
図 9-22. ENABLE OFF, 10-A Resistive Load

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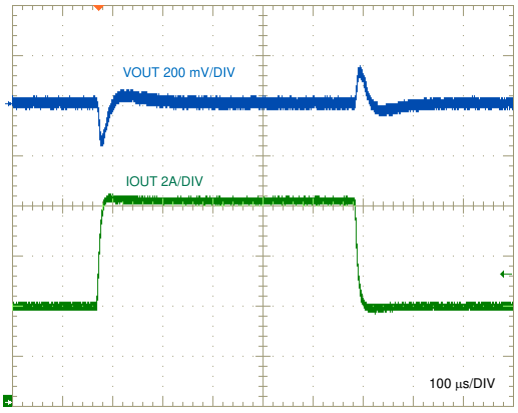
V_{IN} = 48 V

図 9-23. Load Transient Response, 1 A to 8 A to 1 A



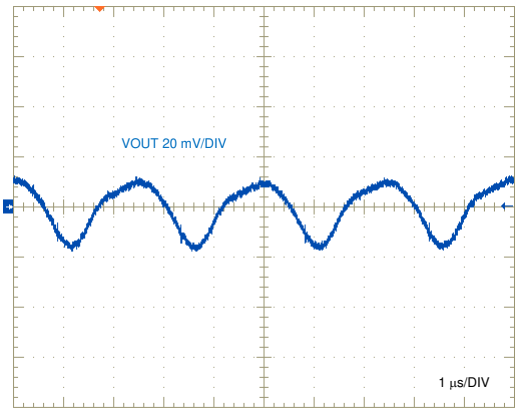
V_{IN} = 48 V

図 9-24. Load Transient Response, 2 A to 8 A to 2 A



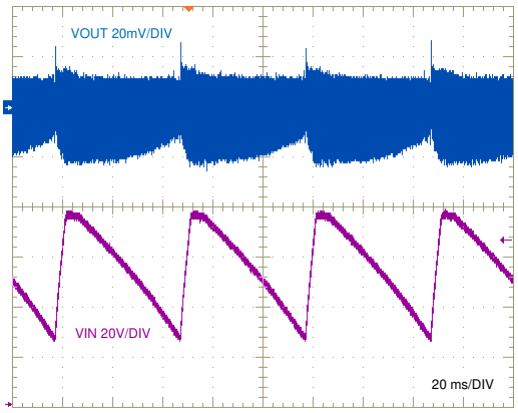
V_{IN} = 48 V

図 9-25. Load Transient Response, 4 A to 8 A to 4 A



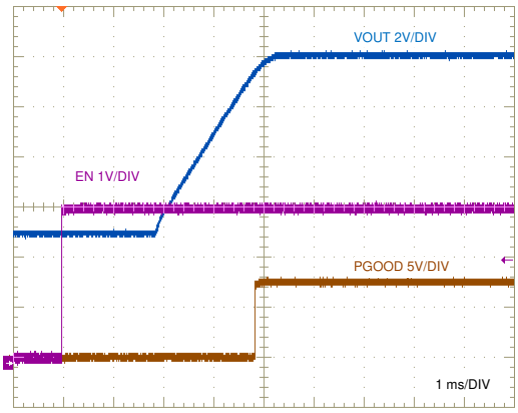
V_{IN} = 48 V I_{OUT} = 8 A

図 9-26. Output Voltage Ripple



I_{OUT} = 4 A

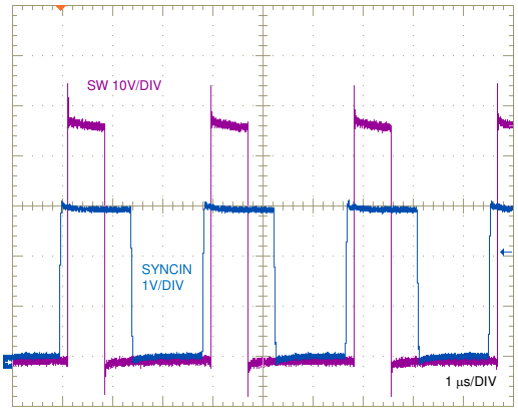
図 9-27. Repetitive Line Transients, 24 V to 75 V



V_{IN} = 48 V I_{OUT} = 0 A

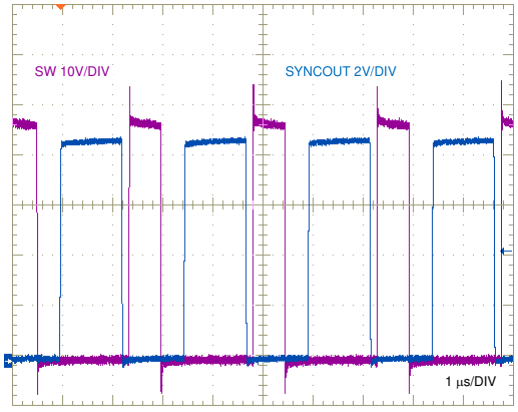
図 9-28. Pre-Biased Start-Up

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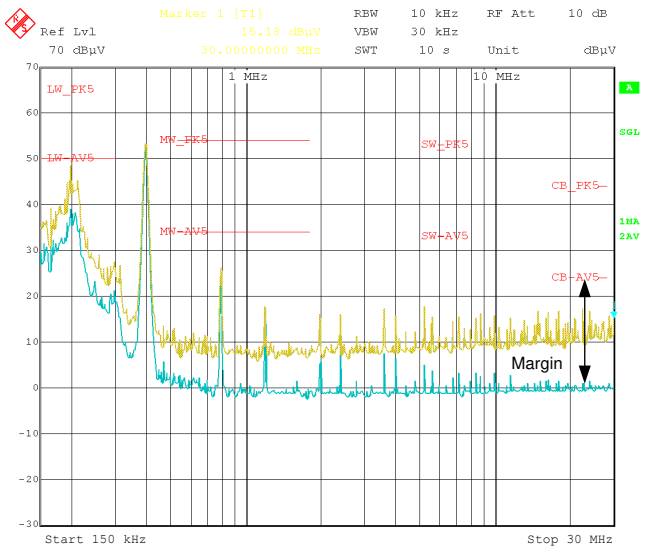
V_{IN} = 48 V F_{SW} = 350 kHz I_{OUT} = 8 A

図 9-29. SW Node and SYNCIN Voltages



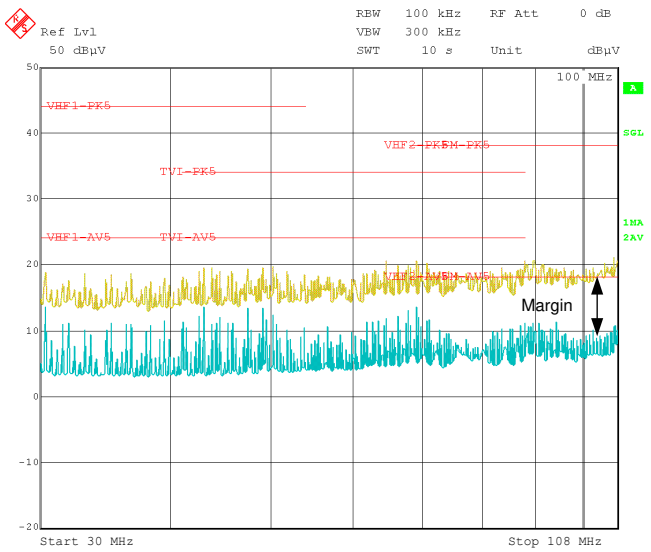
V_{IN} = 48 V I_{OUT} = 8 A

図 9-30. SW Node and SYNCOUT Voltages



V_{IN} = 48 V V_{OUT} = 12 V 6-A resistive load

図 9-31. CISPR 25 Class 5 Conducted EMI, 150 kHz to 30 MHz



V_{IN} = 48 V V_{OUT} = 12 V 6-A resistive load

図 9-32. CISPR 25 Class 5 Conducted EMI, 30 MHz to 108 MHz

9.3 Power Supply Recommendations

The LV5144 buck controller is designed to operate from a wide input voltage range from 5.5 V to 100 V. The characteristics of the input supply must be compatible with the *Absolute Maximum Ratings* and *Recommended Operating Conditions*. In addition, the input supply must be capable of delivering the required input current to the fully-loaded regulator. Estimate the average input current with 式 23.

$$I_{IN} = \frac{V_{OUT} \cdot I_{OUT}}{V_{IN} \cdot \eta} \tag{23}$$

where

- η is the efficiency

If the converter is connected to an input supply through long wires or PCB traces with a large impedance, take special care to achieve stable performance. The parasitic inductance and resistance of the input cables can have an adverse affect on converter operation. The parasitic inductance in combination with the low-ESR

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ceramic input capacitors form an underdamped resonant circuit. This circuit can cause overvoltage transients at VIN each time the input supply is cycled ON and OFF. The parasitic resistance causes the input voltage to dip during a load transient. If the regulator is operating close to the minimum input voltage, this dip can cause false UVLO fault triggering and a system reset. The best way to solve such issues is to reduce the distance from the input supply to the regulator and use an aluminum or tantalum input capacitor in parallel with the ceramics. The moderate ESR of the electrolytic capacitors helps to damp the input resonant circuit and reduce any voltage overshoots. A capacitance in the range of 10 µF to 47 µF is usually sufficient to provide input damping and helps to hold the input voltage steady during large load transients.

An EMI input filter is often used in front of the regulator that, unless carefully designed, can lead to instability as well as some of the effects mentioned above. The application report *Simple Success with Conducted EMI for DC-DC Converters* provides helpful suggestions when designing an input filter for any switching regulator.

9.4 Layout

9.4.1 Layout Guidelines

Proper PCB design and layout is important in a high-current, fast-switching circuits (with high current and voltage slew rates) to assure appropriate device operation and design robustness. As expected, certain issues must be considered before designing a PCB layout using the LV5144. The high-frequency power loop of the buck converter power stage is denoted by #1 in the shaded area of 図 9-33. The topological architecture of a buck converter means that particularly high di/dt current flows in the components of loop 1, and it becomes mandatory to reduce the parasitic inductance of this loop by minimizing its effective loop area. Also important is the gate drive loops of the low-side and high-side MOSFETs, denoted by 2 and 3, respectively, in 図 9-33.

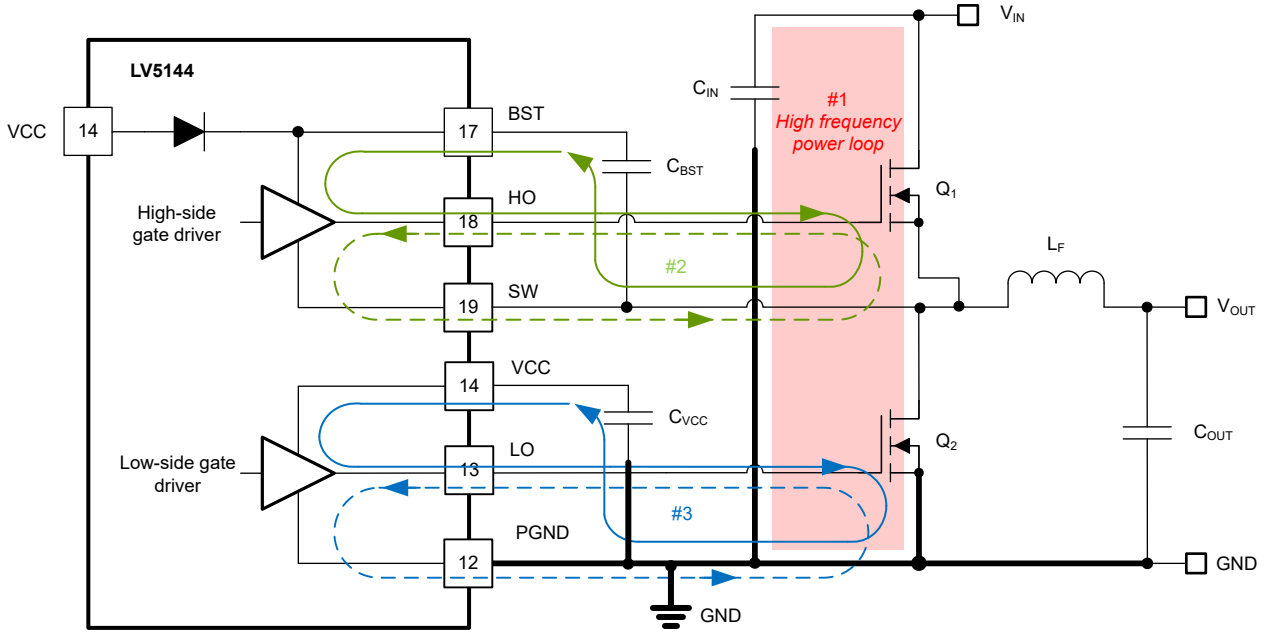


図 9-33. DC/DC Regulator Ground System With Power Stage and Gate Drive Circuit Switching Loops

9.4.1.1 Power Stage Layout

1. Input capacitors, output capacitors, and MOSFETs are the constituent components of the power stage of a buck regulator and are typically placed on the top side of the PCB (solder side). The benefits of convective heat transfer are maximized because of leveraging any system-level airflow. In a two-sided PCB layout, small-signal components are typically placed on the bottom side (component side). insert at least one inner plane, connected to ground, to shield and isolate the small-signal traces from noisy power traces and lines.
2. The DC/DC converter has several high-current loops. Minimize the area of these loops in order to suppress generated switching noise and parasitic loop inductance and optimize switching performance.

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- Loop #1: The most important loop to minimize the area of is the path from the input capacitor or capacitors through the high- and low-side MOSFETs, and back to the capacitor or capacitors through the ground connection. Connect the input capacitor or capacitors negative terminal close to the source of the low-side MOSFET (at ground). Similarly, connect the input capacitor or capacitors positive terminal close to the drain of the high-side MOSFET (at VIN). Refer to loop #1 of 図 9-33.
- Another loop, not as critical though as loop #1, is the path from the low-side MOSFET through the inductor and output capacitors, and back to source of the low-side MOSFET through ground. Connect the source of the low-side MOSFET and negative terminal of the output capacitor or capacitors at ground as close as possible.

3. The PCB trace defined as SW node, which connects to the source of the high-side (control) MOSFET, the drain of the low-side (synchronous) MOSFET and the high-voltage side of the inductor, must be short and wide. However, the SW connection is a source of injected EMI and thus must not be too large.
4. Follow any layout considerations of the MOSFETs as recommended by the MOSFET manufacturer, including pad geometry and solder paste stencil design.
5. The SW pin connects to the switch node of the power conversion stage and acts as the return path for the high-side gate driver. The parasitic inductance inherent to loop #1 in 図 9-33 and the output capacitance (C_{OSS}) of both power MOSFETs form a resonant circuit that induces high frequency (> 100 MHz) ringing on the SW node. The voltage peak of this ringing, if not controlled, can be significantly higher than the input voltage. Ensure that the peak ringing amplitude does not exceed the absolute maximum rating limit for the SW pin. In many cases, a series resistor and capacitor snubber network connected from the SW node to GND damps the ringing and decreases the peak amplitude. Provide provisions for snubber network components in the PCB layout. If testing reveals that the ringing amplitude at the SW pin is excessive, then include snubber components as needed.

9.4.1.2 Gate Drive Layout

The LV5144 high-side and low-side gate drivers incorporate short propagation delays, adaptive dead-time control and low-impedance output stages capable of delivering large peak currents with very fast rise and fall times to facilitate rapid turnon and turnoff transitions of the power MOSFETs. Very high di/dt can cause unacceptable ringing if the trace lengths and impedances are not well controlled.

Minimization of stray or parasitic gate loop inductance is key to optimizing gate drive switching performance, whether it be series gate inductance that resonates with MOSFET gate capacitance or common source inductance (common to gate and power loops) that provides a negative feedback component opposing the gate drive command, thereby increasing MOSFET switching times. The following loops are important:

- Loop 2: high-side MOSFET, Q_1. During the high-side MOSFET turnon, high current flows from the bootstrap (boot) capacitor through the gate driver and high-side MOSFET, and back to the negative terminal of the boot capacitor through the SW connection. Conversely, to turn off the high-side MOSFET, high current flows from the gate of the high-side MOSFET through the gate driver and SW, and back to the source of the high-side MOSFET through the SW trace. Refer to loop #2 of 図 9-33.
- Loop 3: low-side MOSFET, Q_2. During the low-side MOSFET turn-on, high current flows from the VCC decoupling capacitor through the gate driver and low-side MOSFET, and back to the negative terminal of the capacitor through ground. Conversely, to turn off the low-side MOSFET, high current flows from the gate of the low-side MOSFET through the gate driver and GND, and back to the source of the low-side MOSFET through ground. Refer to loop #3 of 図 9-33.

TI strongly recommends following circuit layout guidelines when designing with high-speed MOSFET gate drive circuits.

1. Connections from gate driver outputs, HO and LO, to the respective gate of the high-side or low-side MOSFET must be as short as possible to reduce series parasitic inductance. Use 0.65 mm (25 mils) or wider traces. Use a via or vias, if necessary, of at least 0.5 mm (20 mils) diameter along these traces. Route HO and SW gate traces as a differential pair from the LV5144 to the high-side MOSFET, taking advantage of flux cancellation.
2. Minimize the current loop path from the VCC and BST pins through their respective capacitors as these provide the high instantaneous current, up to 3.5 A, to charge the MOSFET gate capacitances. Specifically, locate the bootstrap capacitor, C_{BST}, close to the BST and SW pins of the LV5144 to minimize the area of

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loop #2 associated with the high-side driver. Similarly, locate the VCC capacitor, C_{VCC}, close to the VCC and PGND pins of the LV5144 to minimize the area of loop #3 associated with the low-side driver.

3. Placing a 2-Ω to 10-Ω resistor in series with the boot capacitor, as shown in 図 9-16, slows down the high-side MOSFET turn-on transition, serving to reduce the voltage ringing and peak amplitude at the SW node at the expense of increased MOSFET turn-on power loss.

9.4.1.3 PWM Controller Layout

With the proviso to locate the controller as close as possible to the MOSFETs to minimize gate driver trace runs, the components related to the analog and feedback signals, current limit setting, and temperature sense are considered in the following:

1. Separate power and signal traces, and use a ground plane to provide noise shielding.
2. Place all sensitive analog traces and components such as COMP, FB, RT, ILIM, and SS/TRK away from high-voltage switching nodes such as SW, HO, LO, or BST to avoid mutual coupling. Use an internal layer or layers as a ground plane or ground planes. Pay particular attention to shielding the feedback (FB) trace from power traces and components.
3. The upper feedback resistor can be connected directly to the output voltage sense point at the load device or the bulk capacitor at the converter side.
4. Connect the ILIM setting resistor from the drain of the low-side MOSFET to ILIM and make the connections as close as possible to the LV5144. The trace from the ILIM pin to the resistor must avoid coupling to a high-voltage switching net.
5. Minimize the loop area from the VCC and VIN pins through their respective decoupling capacitors to the GND pin. Locate these capacitors as close as possible to the LV5144.

9.4.1.4 Thermal Design and Layout

The useful operating temperature range of a PWM controller with integrated gate drivers and bias supply LDO regulator is greatly affected by:

- Average gate drive current requirements of the power MOSFETs
- Switching frequency
- Operating input voltage (affecting bias regulator LDO voltage drop and hence its power dissipation)
- Thermal characteristics of the package and operating environment

For a PWM controller to be useful over a particular temperature range, the package must allow for the efficient removal of the heat produced while keeping the junction temperature within rated limits. The LV5144 controller is available in a small 3.5-mm × 4.5-mm 20-pin VQFN (RGY) PowerPAD™ package to cover a range of application requirements. The thermal metrics of this package are summarized in Thermal Information. The application report *Semiconductor and IC Package Thermal Metrics* provides detailed information regarding the thermal information table.

The 20-pin VQFN package offers a means of removing heat from the semiconductor die through the exposed thermal pad at the base of the package. While the exposed pad of the package is not directly connected to any leads of the package, it is thermally connected to the substrate of the LV5144 device (ground). This allows a significant improvement in heat sinking, and it becomes imperative that the PCB is designed with thermal lands, thermal vias, and a ground plane to complete the heat removal subsystem. The exposed pad of the LV5144 is soldered to the ground-connected copper land on the PCB directly underneath the device package, reducing the thermal resistance to a very low value. Wide traces of the copper tying in the no-connect pins of the LV5144 (pins 9 and 16) and connection to this thermal land helps to dissipate heat.

Numerous vias with a 0.3-mm diameter connected from the thermal land to the internal and solder-side ground planes are vital to help dissipation. In a multi-layer PCB design, a solid ground plane is typically placed on the PCB layer below the power components. Not only does this provide a plane for the power stage currents to flow but it also represents a thermally conductive path away from the heat generating devices.

The thermal characteristics of the MOSFETs also are significant. The drain pad of the high-side MOSFET is normally connected to a VIN plane for heat sinking. The drain pad of the low-side MOSFET is tied to the SW plane, but the SW plane area is purposely kept relatively small to mitigate EMI concerns.

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9.4.1.5 Ground Plane Design

As mentioned previously, TI recommends using one or more of the inner PCB layers as a solid ground plane. A ground plane offers shielding for sensitive circuits and traces and also provides a quiet reference potential for the control circuitry. Connect the PGND pin to the system ground plane using an array of vias under the exposed pad. Also connect the PGND directly to the return terminals of the input and output capacitors. The PGND net contains noise at the switching frequency and can bounce because of load current variations. The power traces for PGND, VIN, and SW can be restricted to one side of the ground plane. The other side of the ground plane contains much less noise and is designed for sensitive analog trace routes.

9.4.2 Layout Example

図 9-34 shows an example PCB layout based on the *LV5144-Q1-EVM12V* design. The power component connections are made on the top layer with wide, copper-filled polygon areas. The SW connection from the power MOSFETs to the inductor is purposely kept at minimum area to reduce radiated EMI. A power ground plane is placed on layer 2 with 6 mil (0.15 mm) spacing to the top layer, see 図 9-35. As a result, the buck regulator hot loop has a small effective area based on this tightly-coupled GND plane directly underneath the MOSFETs.

The LV5144 controller is located close to the gate terminals of the MOSFETs such that the gate drive traces are routed short and direct. Refer to the *LV5144-Q1-EVM12V Evaluation Module User's Guide* for more detail.

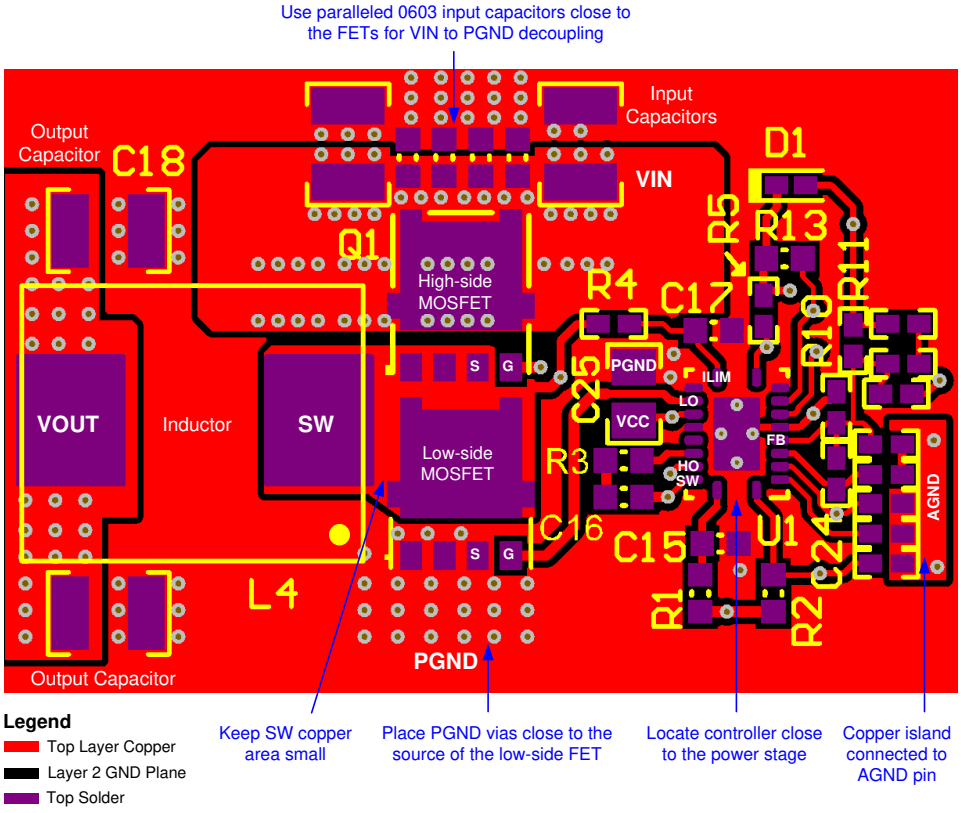
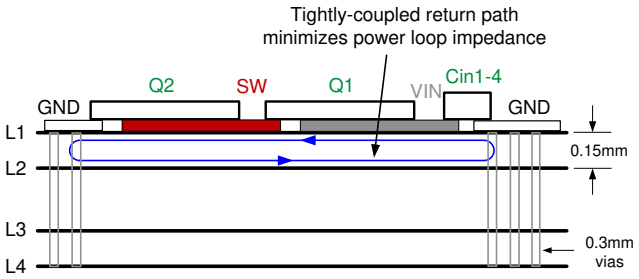


図 9-34. LV5144 Controller PCB Layout (Viewed From Top)

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注

See the *Improve High-current DC/DC Regulator Performance for Free with Optimized Power Stage Layout* application brief for more detail.

図 9-35. PCB Stack-up Diagram With Low L1-L2 Intra-layer Spacing

10 Device and Documentation Support

10.1 Device Support

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10.1.2 Development Support

With an input operating voltage as low as 3.5 V and up to 100 V as specified in 表 10-1, the LM(2)514x family of synchronous buck controllers from TI provides flexibility, scalability and optimized design size for a range of applications. These controllers enable DC/DC designs with high density, low EMI and increased flexibility. Available EMI mitigation features include dual-random spread spectrum (DRSS) or triangular spread spectrum (TRSS), split gate driver outputs for slew rate (SR) control, and integrated active EMI filtering (AEF).

表 10-1. Synchronous Buck DC/DC Controller Family

DC/DC CONTROLLER	SINGLE or DUAL	V_{IN} RANGE	CONTROL METHOD	GATE DRIVE VOLTAGE	SYNC OUTPUT	EMI MITIGATION
LM25148	Single	3.5 V to 42 V	Peak current mode	5 V	180° phase shift	DRSS
LM25149	Single	3.5 V to 42 V	Peak current mode	5 V	180° phase shift	AEF, DRSS
LM25141	Single	3.8 V to 42 V	Peak current mode	5 V	N/A	SR control, TRSS
LM5141	Single	3.8 V to 42 V	Peak current mode	5 V	N/A	SR control, TRSS
LM5143	Dual	3.5 V to 65 V	Peak current mode	5 V	90° phase shift	SR control, TRSS
LM25145	Single	6 V to 42 V	Voltage mode	7.5 V	180° phase shift	N/A
LM5145	Single	6 V to 75 V	Voltage mode	7.5 V	180° phase shift	N/A
LV5144	Single	5.5 V to 100 V	Voltage mode	7.5 V	180° phase shift	N/A

For development support see the following:

- For TI's reference design library, visit TI Designs
- To design a low-EMI power supply, review TI's comprehensive EMI Training Series
- TI Reference Designs:
  - *57W output synchronous buck converter for telecom reference design*
  - *10-A automotive pre-regulator reference design*
  - *10-A automotive pre-regulator reference design with extended input voltage range for trucks*
  - *20-A automotive pre-regulator reference design*
  - *20-A automotive pre-regulator reference design with extended input voltage range for trucks*
- Technical Articles:
  - *High-density PCB layout of DC/DC converters*
  - *Synchronous buck controller solutions support wide V_{IN} performance and flexibility*
  - *How to use slew rate for EMI control*
  - *How to reduce EMI and shrink power-supply size with an integrated active EMI filter*

10.2 Documentation Support

10.2.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *LV5144-Q1 EVM User's Guide*
- Texas Instruments, *LM5145 EVM User's Guide*
- Texas Instruments, *LM5143-Q1 Synchronous Buck Controller EVM* user's guide
- Texas Instruments, *LM5143-Q1 4-phase Buck Regulator Design for Automotive ADAS Applications* application note

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- Texas Instruments, *Reduce Buck Converter EMI and Voltage Stress by Minimizing Inductive Parasitics* analog design journal
- Texas Instruments, *AN-2162 Simple Success with Conducted EMI from DC-DC Converters* application note
- White Papers:
  - Texas Instruments, *Valuing Wide V_{IN}, Low-EMI Synchronous Buck Circuits for Cost-Effective, Demanding Applications*
  - Texas Instruments, *An Overview of Conducted EMI Specifications for Power Supplies*
  - Texas Instruments, *An Overview of Radiated EMI Specifications for Power Supplies*

10.2.1.1 PCB Layout Resources

- Texas Instruments, *Improve High-current DC/DC Regulator Performance for Free with Optimized Power Stage Layout* application brief
- Texas Instruments, *AN-1149 Layout Guidelines for Switching Power Supplies* application note
- Texas Instruments, *Constructing Your Power Supply – Layout Considerations*
- Technical Articles:
  - *High-Density PCB Layout of DC-DC Converters*

10.2.1.2 Thermal Design Resources

- Texas Instruments, *AN-2020 Thermal Design by Insight, Not Hindsight* application note
- Texas Instruments, *AN-1520 A Guide to Board Layout for Best Thermal Resistance for Exposed Pad Packages* application note
- Texas Instruments, *Semiconductor and IC Package Thermal Metrics* application note
- Texas Instruments, *Thermal Design Made Simple with LM43603 and LM43602* application note
- Texas Instruments, *PowerPAD™ Thermally Enhanced Package* application note
- Texas Instruments, *PowerPAD Made Easy* application brief
- Texas Instruments, *Using New Thermal Metrics* application note

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10.7 用語集

テキサス・インスツルメンツ用語集　　この用語集には、用語や略語の一覧および定義が記載されています。

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11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LV5144RGYR	Active	Production	VQFN (RGY) | 20	3000 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	LV5144
LV5144RGYR.A	Active	Production	VQFN (RGY) | 20	3000 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	LV5144

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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GENERIC PACKAGE VIEW

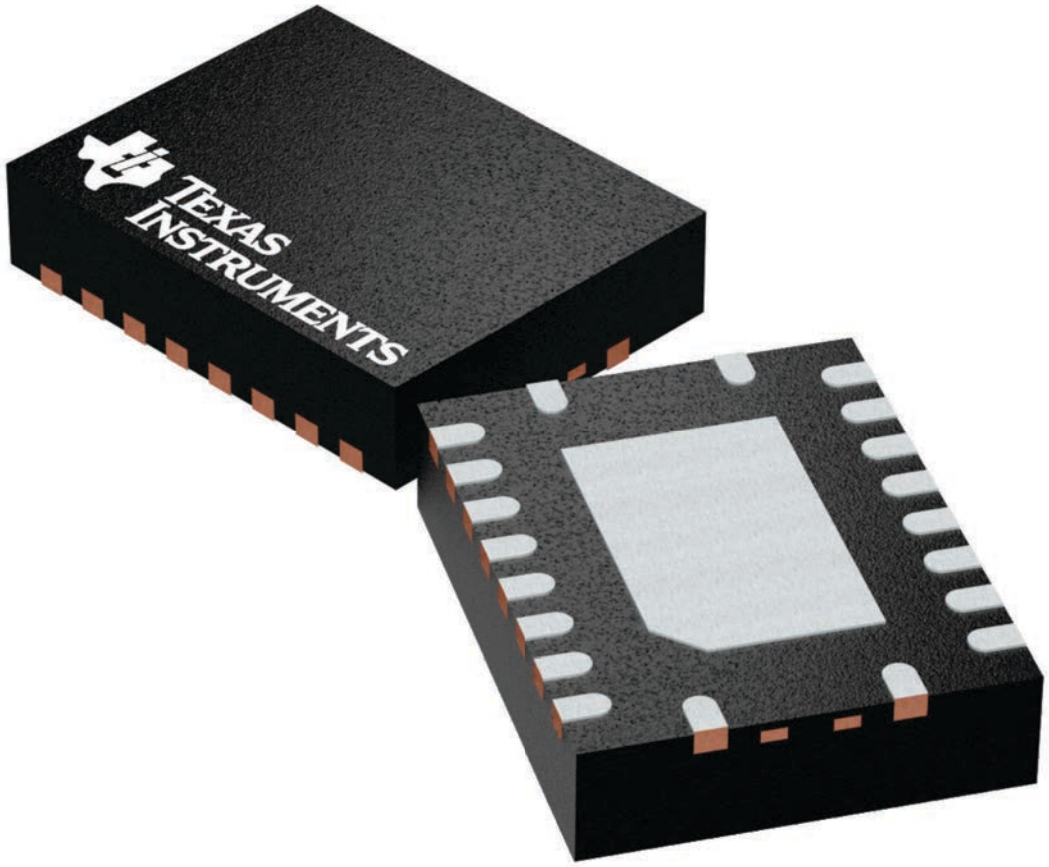
RGY 20

VQFN - 1 mm max height

3.5 x 4.5, 0.5 mm pitch

PLASTIC QUAD FGLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4225264/A

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