MAX232 デュアル EIA-232 ドライバ / レシーバ

1 特長

- TIA/EIA-232-F および ITU 勧告 V.28 適合またはそれを上回る性能
- 1µF チャージ ポンプコンデンサを使用して 5V 単一電源で動作
- 最大 120kbit/s で動作
- 2 つのドライバと 2 つのレシーバ
- ±30V の入力レベル
- 低い消費電流:8mA (代表値)
- JESD 22 を上回る ESD 保護
  - 2000V、人体モデル (A114-A)
- MAX202 デバイスを使用すれば、ESD (15kV HBM) の改善および 0.1µF チャージポンプコンデンサによるアップグレードが可能です。

2 アプリケーション

- TIA/EIA-232-F
- バッテリ駆動システム
- 端末
- モデム
- コンピュータ

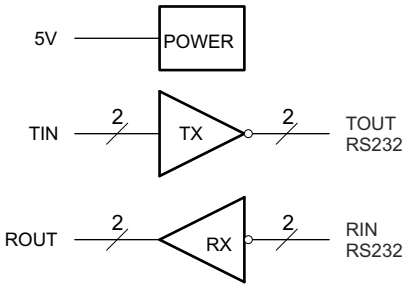
3 概要

MAX232 デバイスは、5V 単一電源から TIA/EIA-232-F の電圧レベルを供給する容量性電圧発生器を内蔵したデュアル ドライバ / レシーバです。各レシーバは、TIA/EIA-232-F の入力を 5V の TTL/CMOS レベルに変換します。これらのレシーバは、標準スレッショルドが 1.3V、標準ヒステリシスが 0.5V で、±30V の入力を受け入れます。各ドライバは、TTL/CMOS 入力レベルを TIA/EIA-232-F レベルに変換します。

パッケージ情報

部品番号	パッケージ (1)	パッケージ サイズ(2)
MAX232	SOIC (16)	9.9mm × 6mm
	SOIC (16)	10.4mm × 10.3mm
	PDIP (16)	19.3mm × 9mm
	SOP (16)	10.2mm × 7.8 mm

(1) 詳細については、セクション 11 を参照してください。
(2) パッケージ サイズ (長さ × 幅) は公称値であり、該当する場合はピンも含まれます。



概略回路図

このリソースの元の言語は英語です。翻訳は概要を便宜的に提供するもので、自動化ツール (機械翻訳) を使用していることがあり、TI では翻訳の正確性および妥当性につきましては一切保証いたしません。実際の設計などの前には、ti.com で必ず最新の英語版をご参照くださいますようお願いいたします。

Table of Contents

1 特長.....1
2 アプリケーション.....1
3 概要.....1
4 Pin Configuration and Functions.....3
5 Specifications.....4
5.1 Absolute Maximum Ratings(1).....4
5.2 ESD Ratings.....4
5.3 Recommended Operating Conditions.....4
5.4 Thermal Information.....4
5.5 Electrical Characteristics, Device.....5
5.6 Electrical Characteristics, Driver.....5
5.7 Electrical Characteristics, Receiver.....5
5.8 Switching Characteristics.....5
5.9 Typical Characteristics.....6
6 Parameter Measurement Information.....7
7 Detailed Description.....9
7.1 Overview.....9
7.2 Functional Block Diagram.....9
7.3 Feature Description.....9
7.4 Device Functional Modes.....9
8 Application and Implementation.....10
8.1 Application Information.....10
8.2 Typical Application.....10
8.3 Power Supply Recommendations.....11
8.4 Layout.....11
9 Device and Documentation Support.....12
9.1 Receiving Notification of Documentation Updates.....12
9.2 サポート・リソース.....12
9.3 Trademarks.....12
9.4 静電気放電に関する注意事項.....12
9.5 用語集.....12
10 Revision History.....12
11 Mechanical, Packaging, and Orderable Information.....12

Copyright © 2024 Texas Instruments Incorporated

4 Pin Configuration and Functions

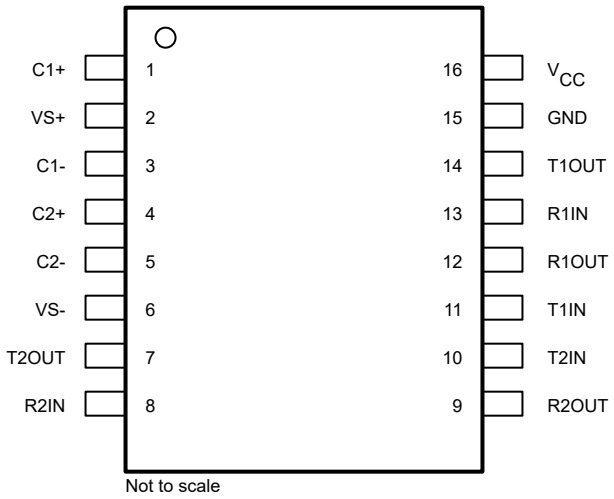


図 4-1. MAX232: D, DW, N or NS Package
MAX232I: D, DW, or N Package
(Top View)

表 4-1. Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
C1+	1	—	Positive lead of C1 capacitor
VS+	2	O	Positive charge pump output for storage capacitor only
C1-	3	—	Negative lead of C1 capacitor
C2+	4	—	Positive lead of C2 capacitor
C2-	5	—	Negative lead of C2 capacitor
VS-	6	O	Negative charge pump output for storage capacitor only
T2OUT	7	O	RS232 line data output (to remote RS232 system)
R2IN	8	I	RS232 line data input (from remote RS232 system)
R2OUT	9	O	Logic data output (to UART)
T2IN	10	I	Logic data input (from UART)
T1IN	11	I	Logic data input (from UART)
R1IN	13	I	RS232 line data input (from remote RS232 system)
T1OUT	14	O	RS232 line data output (to remote RS232 system)
GND	15	—	Ground
V_{CC}	16	—	Supply Voltage, Connect to external 5V power supply

Copyright © 2024 Texas Instruments Incorporated

5 Specifications

5.1 Absolute Maximum Ratings(1)

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CC}	Input Supply voltage range(2)		–0.3	6	V
V_{S+}	Positive output supply voltage range		V_{CC} – 0.3	15	V
$V_{S–}$	Negative output supply voltage range		–0.3	–15	V
V_I	Input voltage range	T1IN, T2IN	–0.3	V_{CC} + 0.3	V
		R1IN, R2IN		±30	
V_O	Output voltage range	T1OUT, T2OUT	$V_{S–}$ – 0.3	V_{S+} + 0.3	V
		R1OUT, R2OUT	–0.3	V_{CC} + 0.3	
	Short-circuit duration	T1OUT, T2OUT	Unlimited		
T_J	Operating virtual junction temperature			150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to network GND.

5.2 ESD Ratings

			MIN	MAX	UNIT
T_{stg}	Storage temperature range		-65	150	°C
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	0	2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	0	1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		4.5	5	5.5	V
V_{IH}	High-level input voltage (T1IN,T2IN)		2			V
V_{IL}	Low-level input voltage (T1IN, T2IN)				0.8	V
R1IN, R2IN	Receiver input voltage				±30	V
T_A	Operating free-air temperature	MAX232	0		70	°C
		MAX232I	–40		85	

5.4 Thermal Information

THERMAL METRIC(1)		SOIC (D)	SOIC wide (DW)	PDIP (N)	SOP (NS)	UNIT
		16 PINS	16 PINS	16 PINS	16 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	84.6	71.7	60.6	88.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	43.5	37.6	48.1	46.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	43.2	36.8	40.6	50.7	°C/W
ψ_{JT}	Junction-to-top characterization parameter	10.4	13.3	27.5	13.5	°C/W
ψ_{JB}	Junction-to-board characterization parameter	42.8	36.4	40.3	50.3	°C/W

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report (SPRA953).

Copyright © 2024 Texas Instruments Incorporated

5.5 Electrical Characteristics, Device

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see 図 8-1)

PARAMETER		TEST CONDITIONS(2)	MIN	TYP(1)	MAX	UNIT
I_{CC}	Supply current	V_{CC} = 5.5V, all outputs open, T_A = 25°C		8	10	mA

(1) All typical values are at V_{CC} = 5V, and T_A = 25°C.
(2) Test conditions are C1–C4 = 1µF at V_{CC} = 5V ± 0.5V

5.6 Electrical Characteristics, Driver

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER			TEST CONDITIONS(2)	MIN	TYP(1)	MAX	UNIT
V_{OH}	High-level output voltage	T1OUT, T2OUT	R_L = 3kΩ to GND	5	7		V
V_{OL}	Low-level output voltage(2)	T1OUT, T2OUT	R_L = 3kΩ to GND		–7	–5	V
r_O	Output resistance	T1OUT, T2OUT	V_{S+} = $V_{S–}$ = 0, V_O = ±2V	300			Ω
I_{OS} (3)	Short-circuit output current	T1OUT, T2OUT	V_{CC} = 5.5V, V_O = 0V		±10		mA
I_{IS}	Short-circuit input current	T1IN, T2IN	V_I = 0			200	µA

(1) All typical values are at V_{CC} = 5V, T_A = 25°C.
(2) The algebraic convention, in which the least-positive (most negative) value is designated minimum, is used in this data sheet for logic voltage levels only.
(3) Not more than one output should be shorted at a time.

5.7 Electrical Characteristics, Receiver

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER			TEST CONDITIONS(3)	MIN	TYP(1)	MAX	UNIT
V_{OH}	High-level output voltage	R1OUT, R2OUT	I_{OH} = –1mA	3.5			V
V_{OL}	Low-level output voltage(2)	R1OUT, R2OUT	I_{OL} = 3.2mA			0.4	V
V_{IT+}	Receiver positive-going input threshold voltage	R1IN, R2IN	V_{CC} = 5V, T_A = 25°C		1.7	2.4	V
$V_{IT–}$	Receiver negative-going input threshold voltage	R1IN, R2IN	V_{CC} = 5V, T_A = 25°C	0.8	1.2		V
V_{hys}	Input hysteresis voltage	R1IN, R2IN	V_{CC} = 5V	0.2	0.5	1	V
r_I	Receiver input resistance	R1IN, R2IN	V_{CC} = 5V, T_A = 25°C	3	5	7	kΩ

(1) All typical values are at V_{CC} = 5V, T_A = 25°C.
(2) The algebraic convention, in which the least-positive (most negative) value is designated minimum, is used in this data sheet for logic voltage levels only.
(3) Test conditions are C1–C4 = 1µF at V_{CC} = 5V ± 0.5V.

5.8 Switching Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS(1)	MIN	TYP(1)	MAX	UNIT
SR	Driver slew rate	RL = 3kΩ to 7kΩ, see 図 6-2			30	V/µs
SR(t)	Driver transition region slew rate	see 図 6-3		3		V/µs
	Data rate	One TOUT switching		120		kbit/s
$t_{PLH®)}$	Receiver propagation delay time, low- to high-level output	TTL load, see 図 6-1		500		ns
$t_{PHL®)}$	Receiver propagation delay time, high- to low-level output	TTL load, see 図 6-1		500		ns

(1) Test conditions are C1–C4 = 1µF at V_{CC} = 5V ± 0.5V.

Copyright © 2024 Texas Instruments Incorporated

5.9 Typical Characteristics

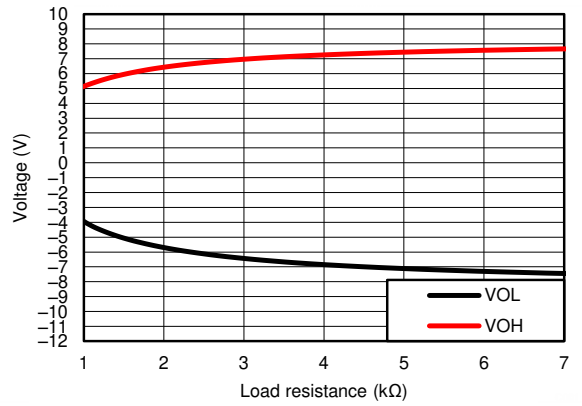


図 5-1. TOUT VOH & VOL vs Load Resistance, Both Drivers Loaded

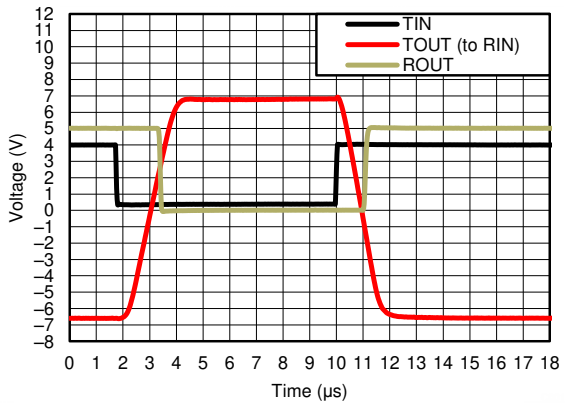
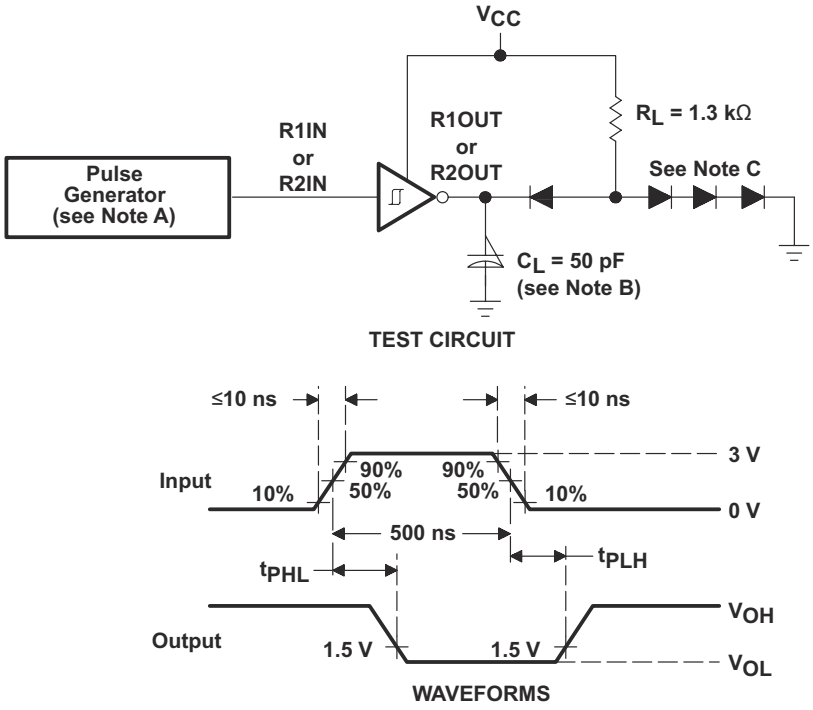


図 5-2. Driver to Receiver Loopback Timing Waveform

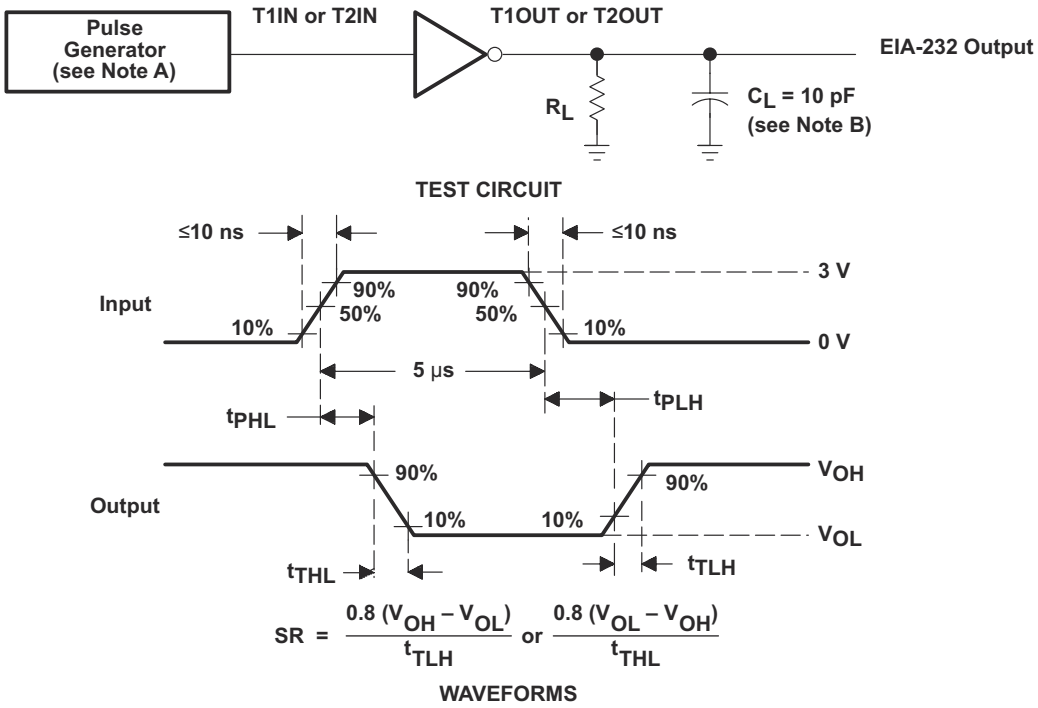
Copyright © 2024 Texas Instruments Incorporated

6 Parameter Measurement Information



A. The pulse generator has the following characteristics: Z_O = 50Ω, duty cycle ≤ 50%.
B. C_L includes probe and jig capacitance.
C. All diodes are 1N3064 or equivalent.

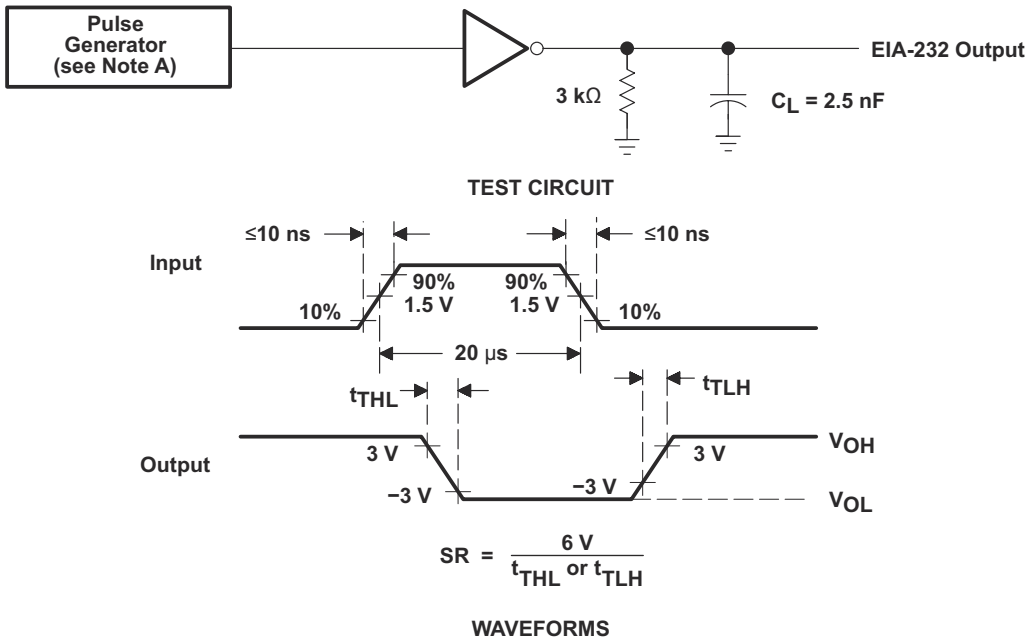
図 6-1. Receiver Test Circuit and Waveforms for t_{PHL} and t_{PLH} Measurements



A. The pulse generator has the following characteristics: Z_O = 50Ω, duty cycle ≤ 50%.

B. C_L includes probe and jig capacitance.

図 6-2. Driver Test Circuit and Waveforms for t_{PHL} and t_{PLH} Measurements (5µs Input)



A. The pulse generator has the following characteristics: Z_O = 50Ω, duty cycle ≤ 50%.

図 6-3. Test Circuit and Waveforms for t_{THL} and t_{TLH} Measurements (20µs Input)

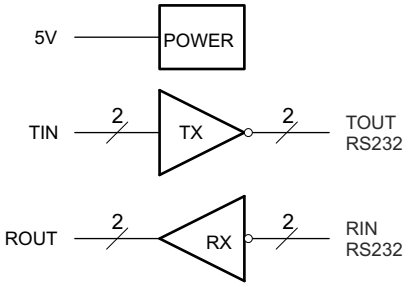
Copyright © 2024 Texas Instruments Incorporated

7 Detailed Description

7.1 Overview

The MAX232 device is a dual driver/receiver that includes a capacitive voltage generator using four capacitors to supply TIA/EIA-232-F voltage levels from a single 5-V supply. Each receiver converts TIA/EIA-232-F inputs to 5-V TTL/CMOS levels. These receivers have a typical threshold of 1.3 V, a typical hysteresis of 0.5 V, and can accept ±30-V inputs. Each driver converts TTL/CMOS input levels into TIA/EIA-232-F levels. The driver, receiver, and voltage-generator functions are available as cells in the Texas Instruments LinASIC™ library. Outputs are protected against shorts to ground.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Power

The power block increases and inverts the 5V supply for the RS232 driver using a charge pump that requires four 1µF external capacitors.

7.3.2 RS232 Driver

Two drivers interface standard logic level to RS232 levels. Internal pull up resistors on TIN inputs ensures a high input when the line is high impedance.

7.3.3 RS232 Receiver

Two receivers interface RS232 levels to standard logic levels. An open input will result in a high output on ROUT.

7.4 Device Functional Modes

7.4.1 V_{CC} powered by 5V

The device will be in normal operation.

7.4.2 V_{CC} unpowered

When MAX232 is unpowered, it can be safely connected to an active remote RS232 device.

7.4.3 Function Tables

表 7-1. Each Driver

INPUT(1)	OUTPUT
T_{IN}	T_{OUT}
L	H
H	L

(1) H = high level, L = low level, X = irrelevant, Z = high impedance

表 7-2. Each Receiver

INPUTS(1)	OUTPUT
R_{IN}	R_{OUT}
L	H
H	L
Open	H

(1) H = high level, L = low level, X = irrelevant, Z = high impedance (off), Open = disconnected input or connected driver off

8 Application and Implementation

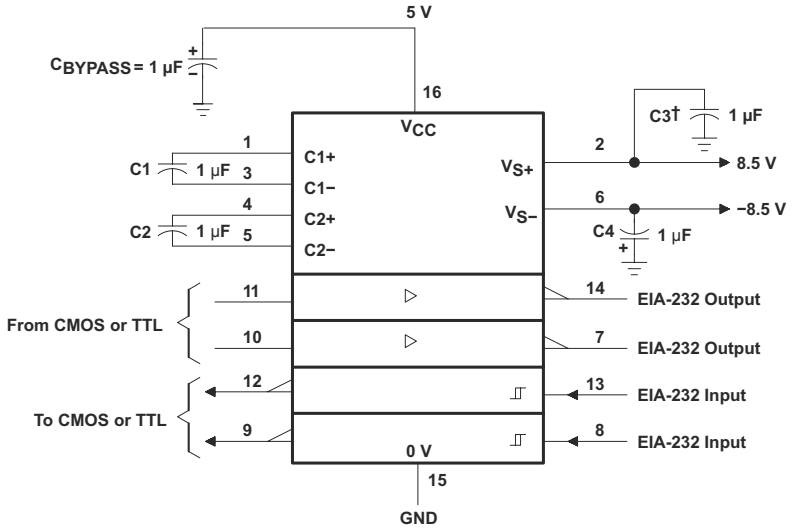
注

以下のアプリケーション情報は、TI の製品仕様に含まれるものではなく、TI ではその正確性または完全性を保証いたしません。個々の目的に対する製品の適合性については、お客様の責任で判断していただくことになります。また、お客様は自身の設計実装を検証しテストすることで、システムの機能を確認する必要があります。

8.1 Application Information

For proper operation add capacitors as shown in 図 8-1. Pins 9 through 12 connect to UART or general purpose logic lines. EIA-232 lines will connect to a connector or cable.

8.2 Typical Application



† C3 can be connected to V_{CC} or GND.

NOTES: A. Resistor values shown are nominal.

B. Nonpolarized ceramic capacitors are acceptable. If polarized tantalum or electrolytic capacitors are used, they should be connected as shown. In addition to the 1-µF capacitors shown, the MAX202 can operate with 0.1-µF capacitors.

図 8-1. Typical Operating Circuit

8.2.1 Design Requirements

- V_{CC} minimum is 4.5V and maximum is 5.5V.
- Maximum recommended bit rate is 120kbps.

8.2.2 Detailed Design Procedure

Use 1uF tantalum or ceramic capacitors.

Copyright © 2024 Texas Instruments Incorporated

8.2.3 Application Curves

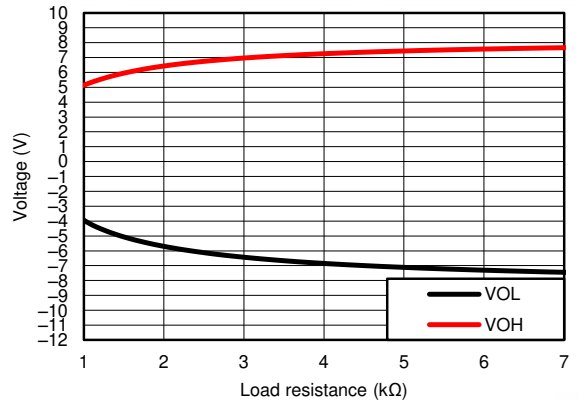


図 8-2. TOUT VOH & VOL vs Load Resistance, Both Drivers Loaded

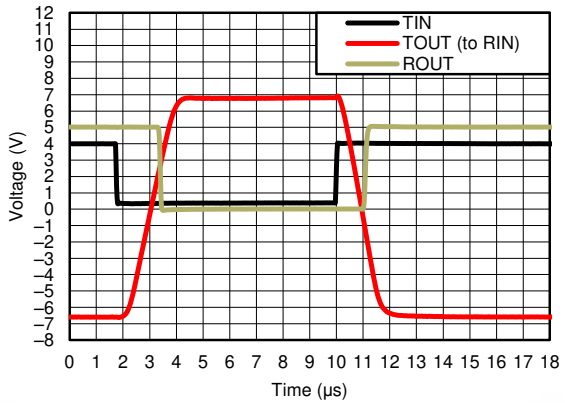


図 8-3. Driver to Receiver Loopback Timing Waveform

8.3 Power Supply Recommendations

The V_{CC} voltage should be connected to the same power source used for logic device connected to TIN pins. V_{CC} should be between 4.5V and 5.5V.

8.4 Layout

8.4.1 Layout Guidelines

Keep the external capacitor traces short. This is more important on C1 and C2 nodes that have the fastest rise and fall times.

8.4.2 Layout Example

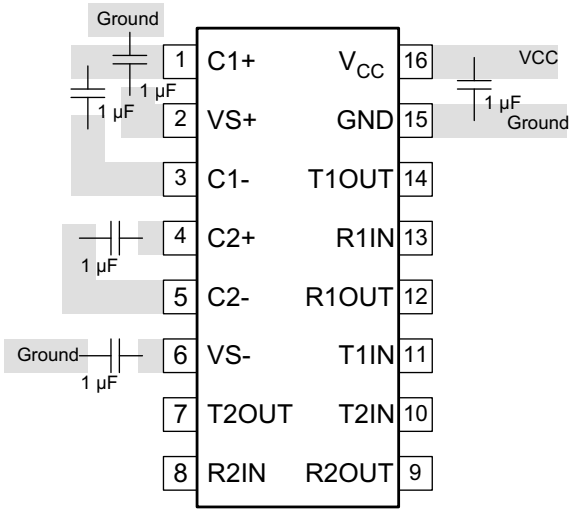


図 8-4. Layout Schematic

9 Device and Documentation Support

9.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.2 サポート・リソース

テキサス・インスツルメンツ E2E™ サポート・フォーラムは、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計で必要な支援を迅速に得ることができます。

リンクされているコンテンツは、各寄稿者により「現状のまま」提供されるものです。これらはテキサス・インスツルメンツの仕様を構成するものではなく、必ずしもテキサス・インスツルメンツの見解を反映したものではありません。テキサス・インスツルメンツの使用条件を参照してください。

9.3 Trademarks

テキサス・インスツルメンツ E2E™ is a trademark of Texas Instruments.
すべての商標は、それぞれの所有者に帰属します。

9.4 静電気放電に関する注意事項



この IC は、ESD によって破損する可能性があります。テキサス・インスツルメンツは、IC を取り扱う際には常に適切な注意を払うことを推奨します。正しい ESD 対策をとらないと、デバイスを破損するおそれがあります。

ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

9.5 用語集

テキサス・インスツルメンツ用語集　　この用語集には、用語や略語の一覧および定義が記載されています。

10 Revision History

Changes from Revision M (November 2004) to Revision N (February 2024)	Page
• Changed the Handling Ratings table to the *ESD Ratings* table	4
• Changed the *Thermal Information* table	4

Changes from Revision L (March 2004) to Revision M (November 2014)	Page
• 「注文情報」表を削除。	1
• 「取り扱い定格」の表、「機能説明」セクション、「デバイスの機能モード」セクション、「アプリケーションと実装」セクション、「電源に関する推奨事項」セクション、「レイアウト」セクション、「デバイスおよびドキュメントのサポート」セクション、「メカニカル、パッケージ、および注文情報」セクションを追加。	1
• 「製品情報」表を「パッケージ情報」表に変更	1
• Moved T_{stg} to Handling Ratings table	4

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser based versions of this data sheet, refer to the left hand navigation.

Copyright © 2024 Texas Instruments Incorporated

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
MAX232D	Obsolete	Production	SOIC (D) | 16	-	-	Call TI	Call TI	0 to 70	MAX232
MAX232DR	Active	Production	SOIC (D) | 16	2500 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	0 to 70	MAX232
MAX232DR.A	Active	Production	SOIC (D) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	MAX232
MAX232DR.B	Active	Production	SOIC (D) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	MAX232
MAX232DRG4	Obsolete	Production	SOIC (D) | 16	-	-	Call TI	Call TI	0 to 70	MAX232
MAX232DW	Obsolete	Production	SOIC (DW) | 16	-	-	Call TI	Call TI	0 to 70	MAX232
MAX232DWG4	Obsolete	Production	SOIC (DW) | 16	-	-	Call TI	Call TI	0 to 70	
MAX232DWR	Obsolete	Production	SOIC (DW) | 16	-	-	Call TI	Call TI	0 to 70	
MAX232DWRG4	Obsolete	Production	SOIC (DW) | 16	-	-	Call TI	Call TI	0 to 70	
MAX232ID	Obsolete	Production	SOIC (D) | 16	-	-	Call TI	Call TI	-40 to 85	MAX232I
MAX232IDR	Active	Production	SOIC (D) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	MAX232I
MAX232IDR.A	Active	Production	SOIC (D) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	MAX232I
MAX232IDR.B	Active	Production	SOIC (D) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	MAX232I
MAX232IDW	Obsolete	Production	SOIC (DW) | 16	-	-	Call TI	Call TI	-40 to 85	
MAX232IDWR	Active	Production	SOIC (DW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	MAX232I
MAX232IDWR.A	Active	Production	SOIC (DW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	MAX232I
MAX232IDWR.B	Active	Production	SOIC (DW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	MAX232I
MAX232IDWRG4	Obsolete	Production	SOIC (DW) | 16	-	-	Call TI	Call TI	-40 to 85	
MAX232IN	Obsolete	Production	PDIP (N) | 16	-	-	Call TI	Call TI	-40 to 85	MAX232IN
MAX232N	Active	Production	PDIP (N) | 16	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	MAX232N
MAX232N.A	Active	Production	PDIP (N) | 16	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	MAX232N
MAX232N.B	Active	Production	PDIP (N) | 16	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	MAX232N
MAX232NE4	Active	Production	PDIP (N) | 16	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	MAX232N
MAX232NSR	Active	Production	SOP (NS) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	MAX232
MAX232NSR.A	Active	Production	SOP (NS) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	MAX232
MAX232NSR.B	Active	Production	SOP (NS) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	MAX232

(1) **Status:** For more details on status, see our product life cycle.

(2) Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

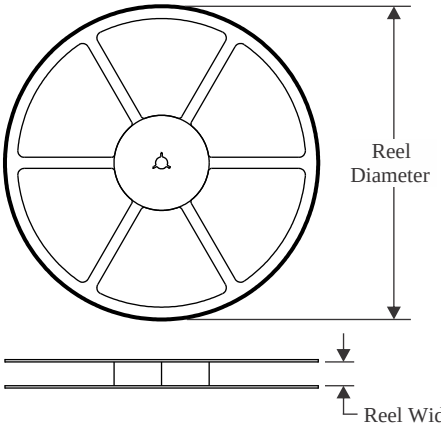
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

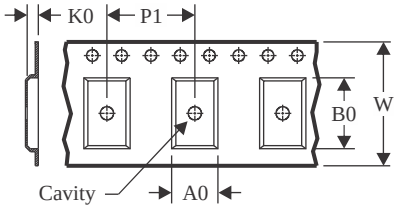
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

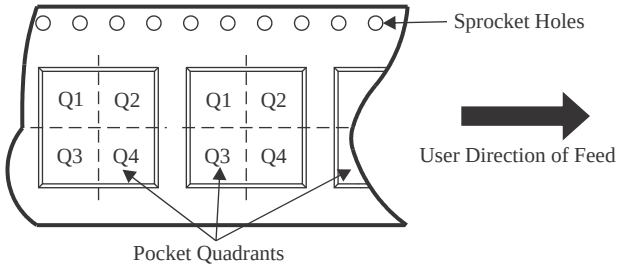


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

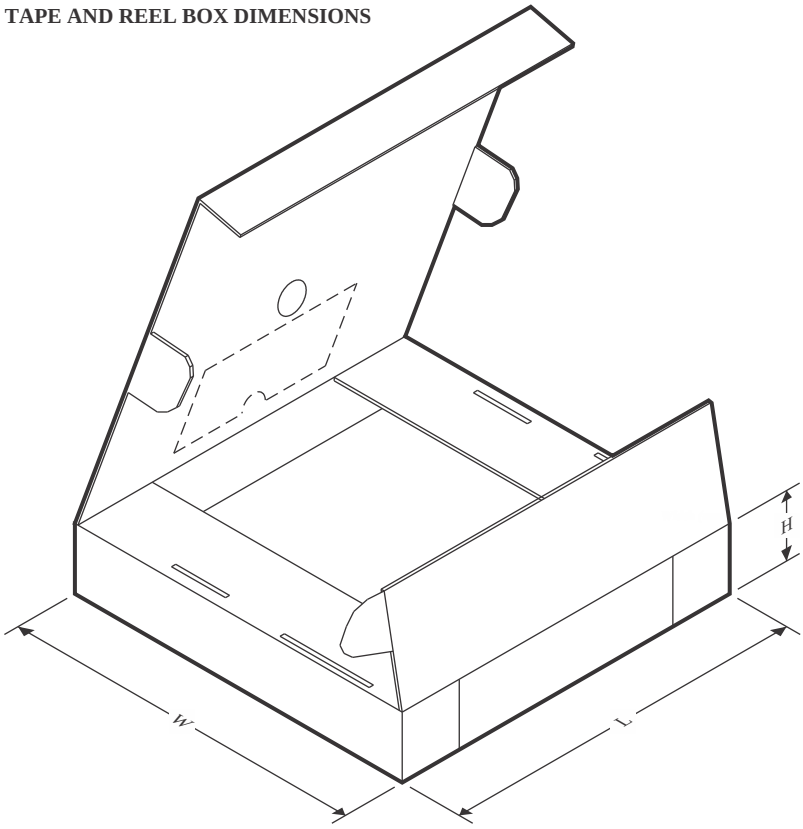
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
MAX232DR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
MAX232DR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
MAX232IDR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
MAX232IDR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
MAX232IDWR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
MAX232NSR	SOP	NS	16	2000	330.0	16.4	8.1	10.4	2.5	12.0	16.0	Q1

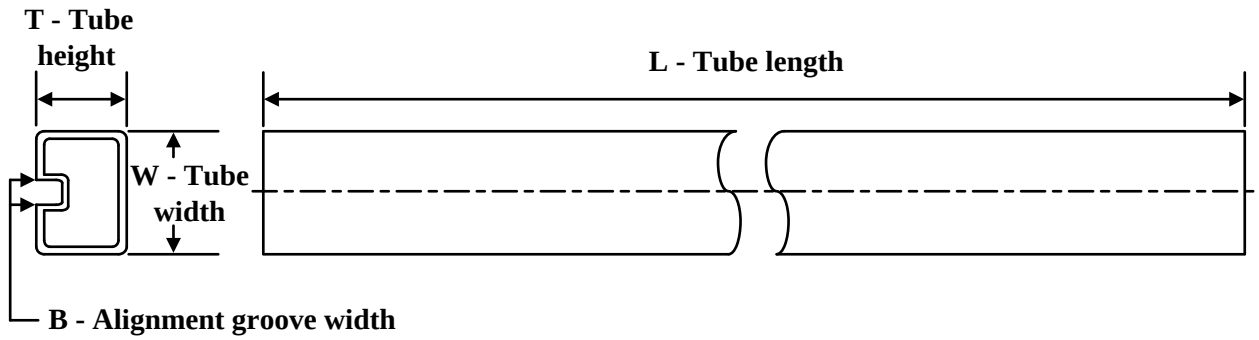
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

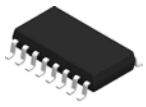
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
MAX232DR	SOIC	D	16	2500	333.2	345.9	28.6
MAX232DR	SOIC	D	16	2500	340.5	336.1	32.0
MAX232IDR	SOIC	D	16	2500	340.5	336.1	32.0
MAX232IDR	SOIC	D	16	2500	353.0	353.0	32.0
MAX232IDWR	SOIC	DW	16	2000	350.0	350.0	43.0
MAX232NSR	SOP	NS	16	2000	353.0	353.0	32.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
MAX232N	N	PDIP	16	25	506	13.97	11230	4.32
MAX232N.A	N	PDIP	16	25	506	13.97	11230	4.32
MAX232N.B	N	PDIP	16	25	506	13.97	11230	4.32
MAX232NE4	N	PDIP	16	25	506	13.97	11230	4.32

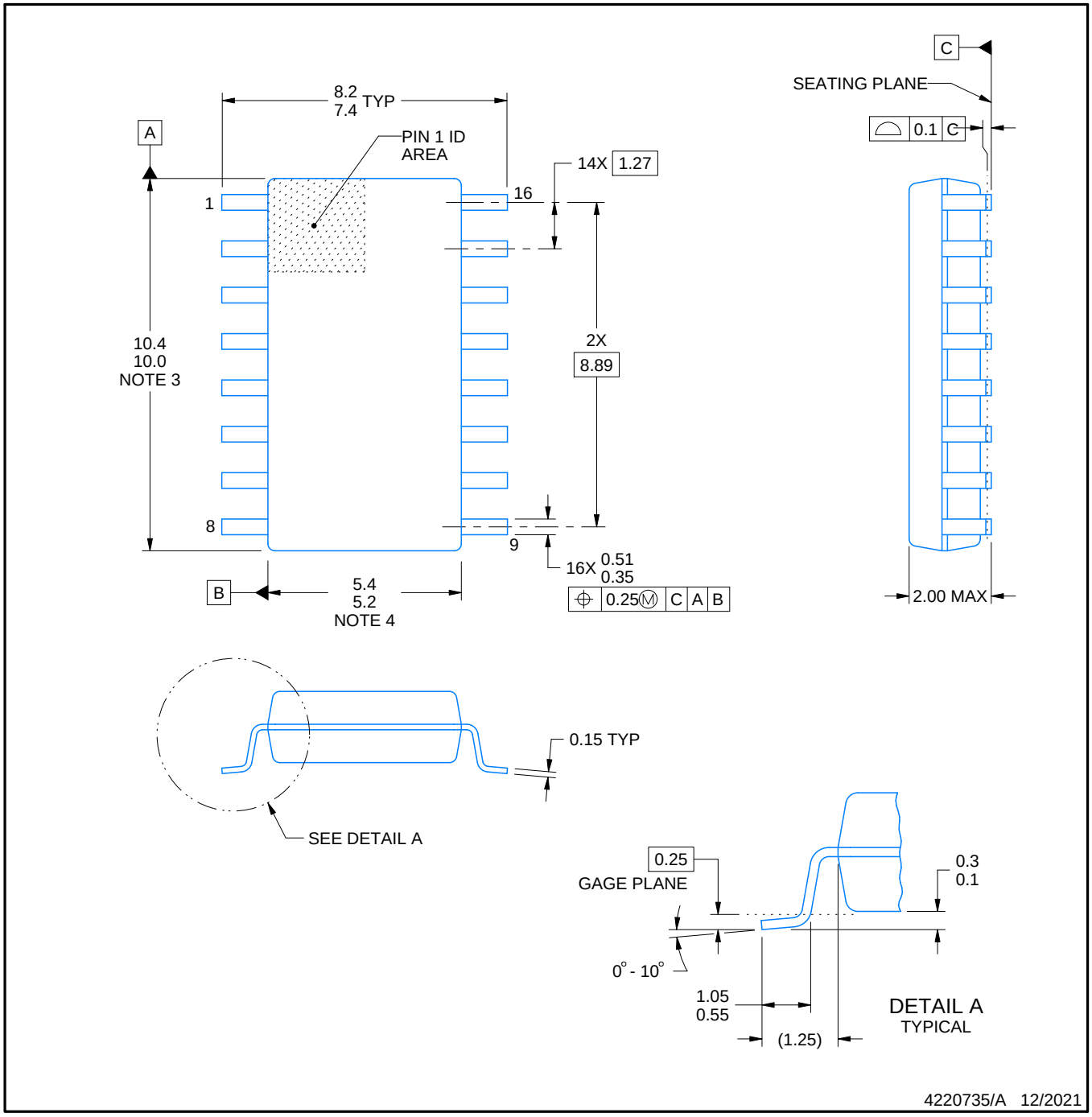


PACKAGE OUTLINE

NS0016A

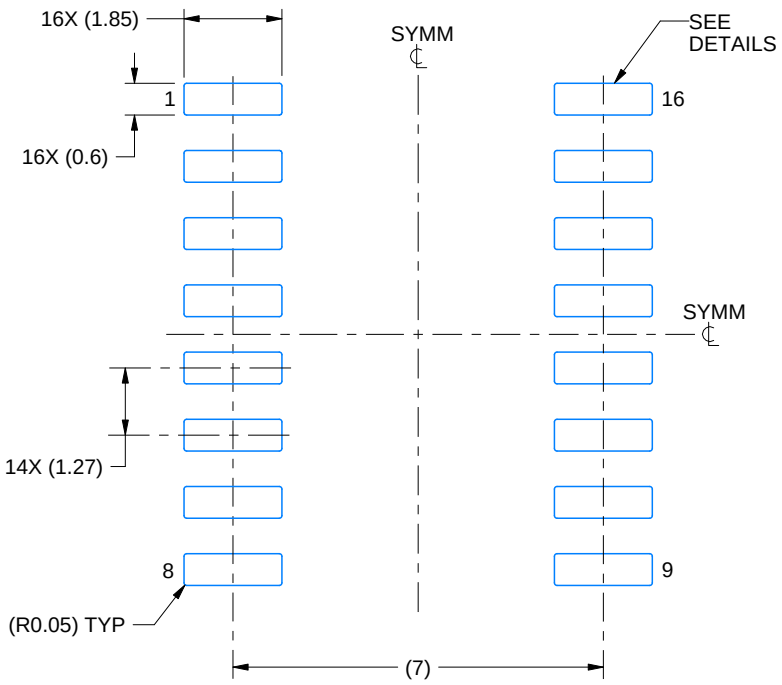
SOP - 2.00 mm max height

SOP

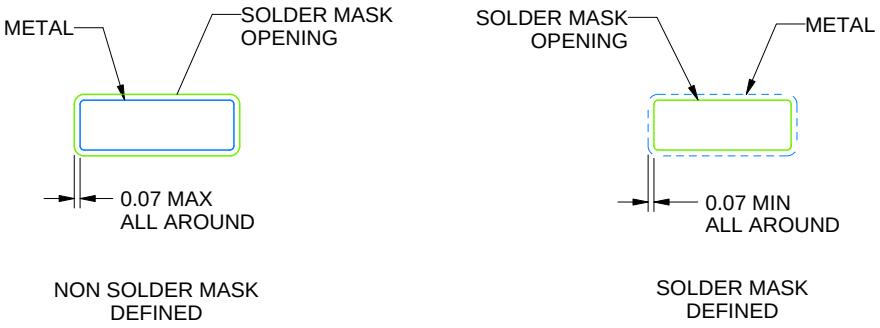


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.



LAND PATTERN EXAMPLE
SCALE:7X



NON SOLDER MASK
DEFINED

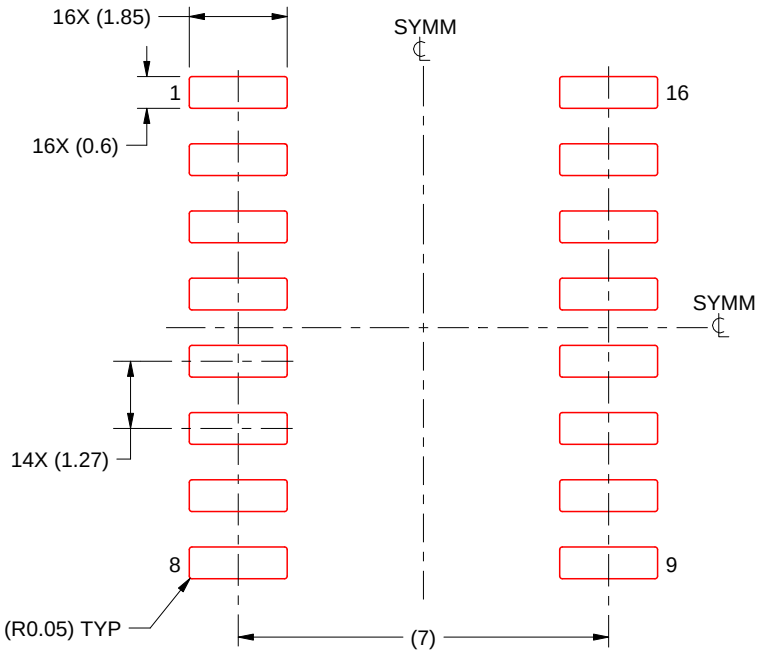
SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4220735/A 12/2021

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



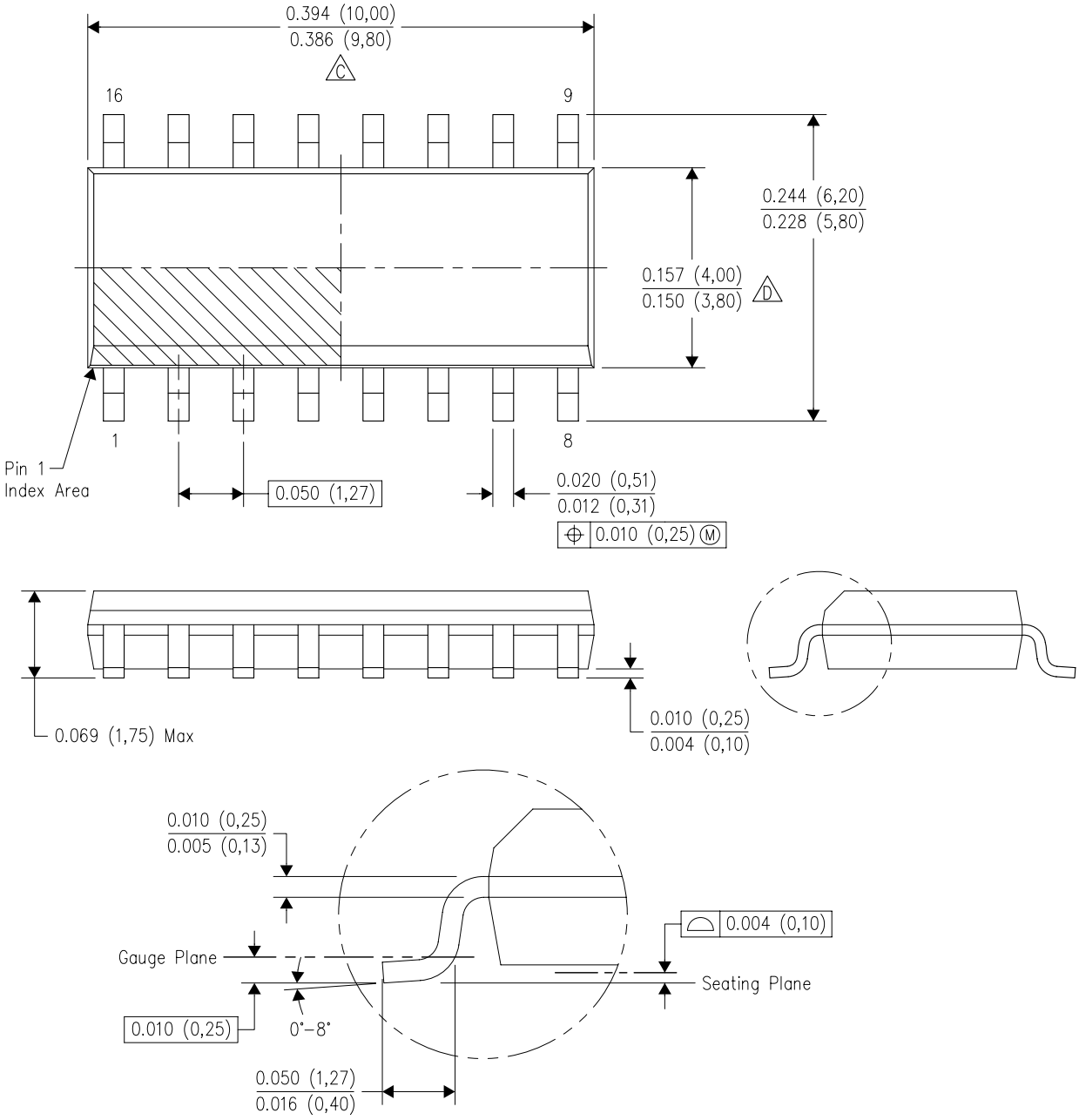
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:7X

4220735/A 12/2021

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

D (R–PDSO–G16) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AC.

GENERIC PACKAGE VIEW

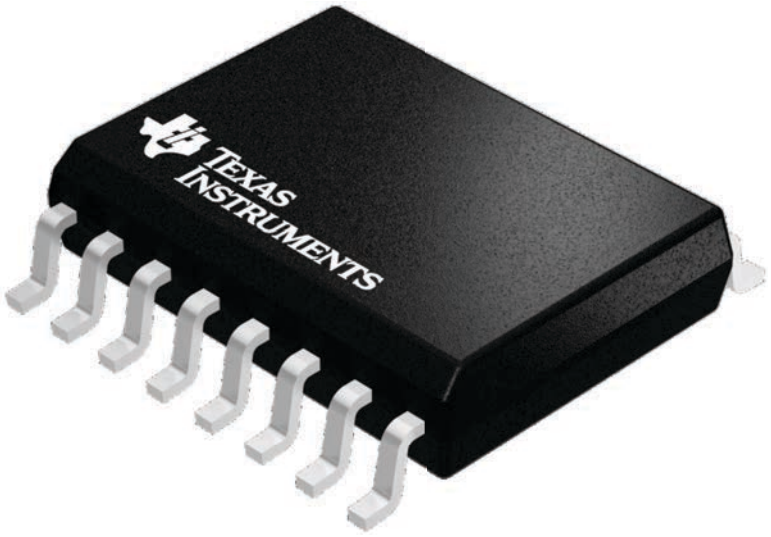
DW 16

SOIC - 2.65 mm max height

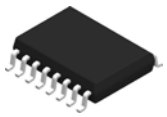
7.5 x 10.3, 1.27 mm pitch

SMALL OUTLINE INTEGRATED CIRCUIT

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4224780/A

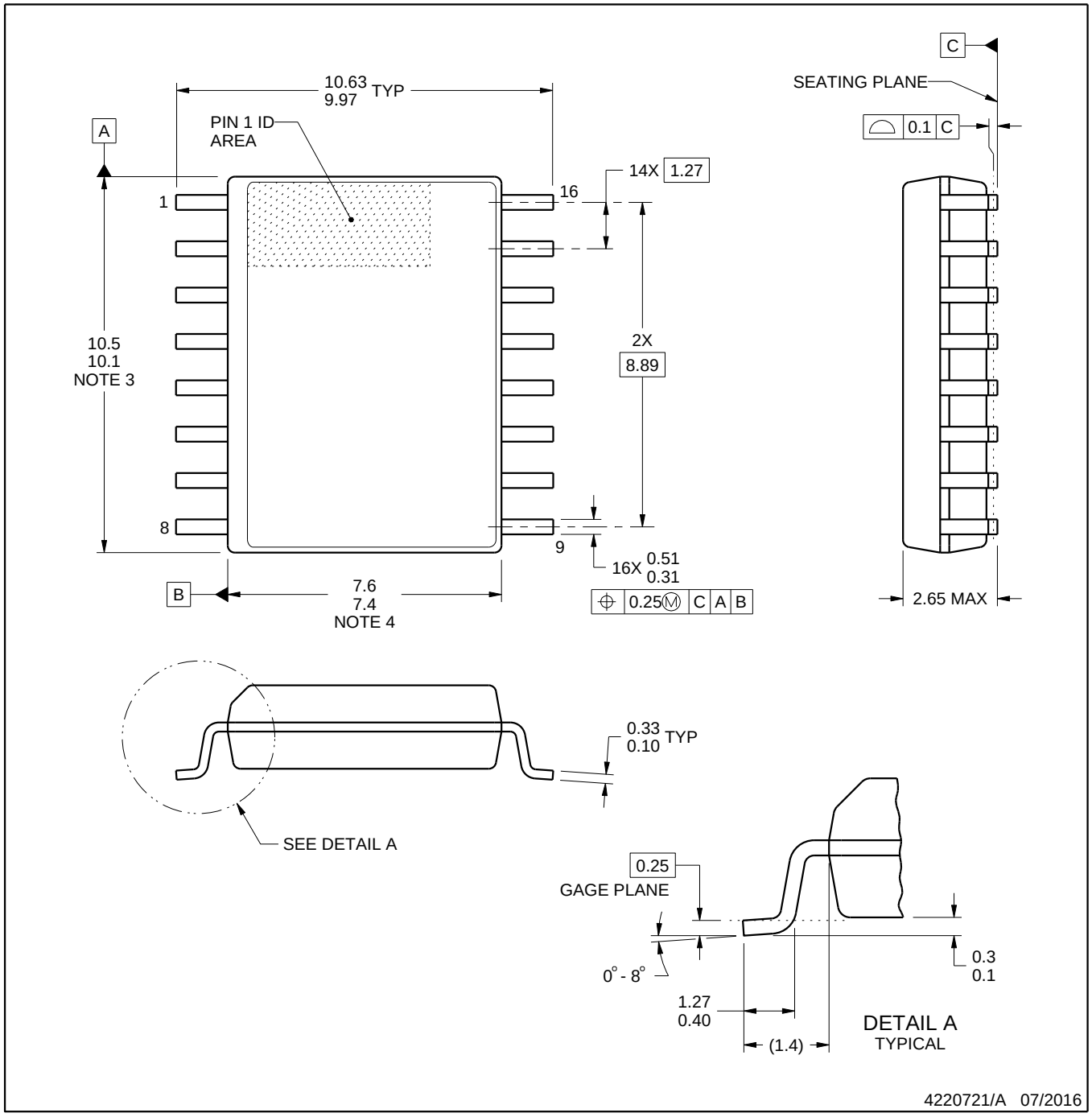


PACKAGE OUTLINE

DW0016A

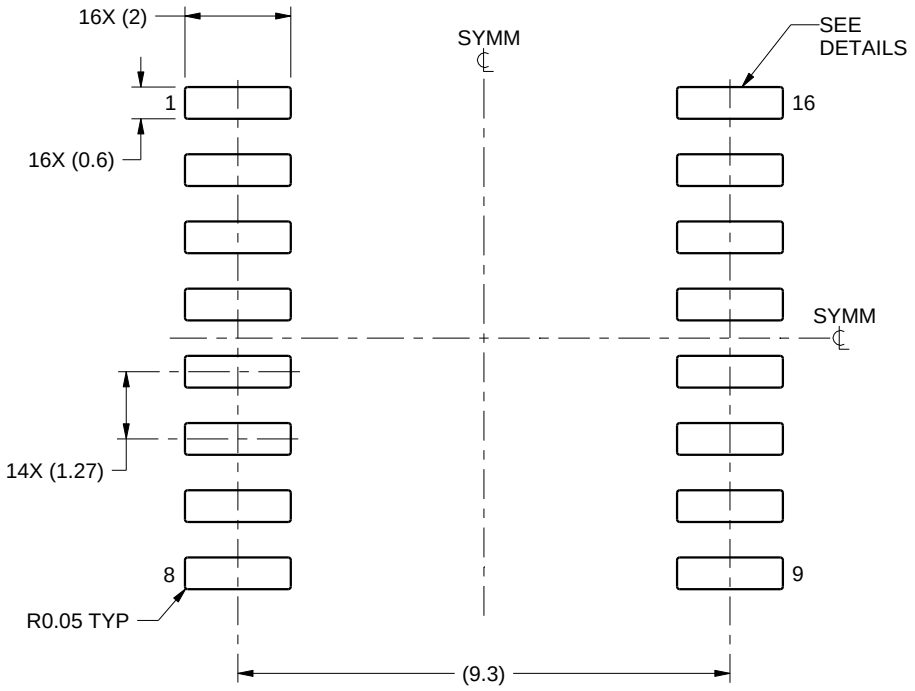
SOIC - 2.65 mm max height

SOIC

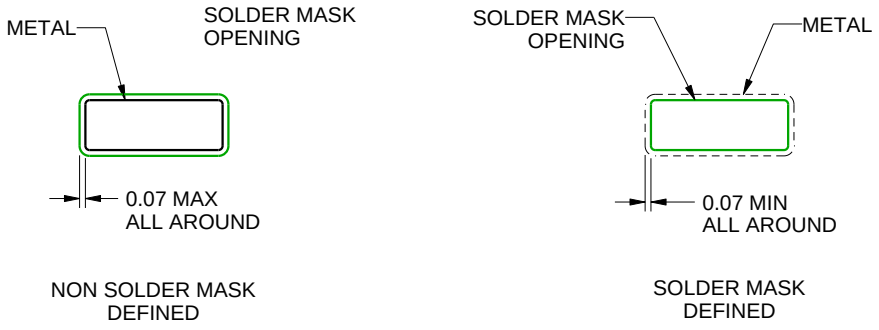


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.
5. Reference JEDEC registration MS-013.



LAND PATTERN EXAMPLE
SCALE:7X

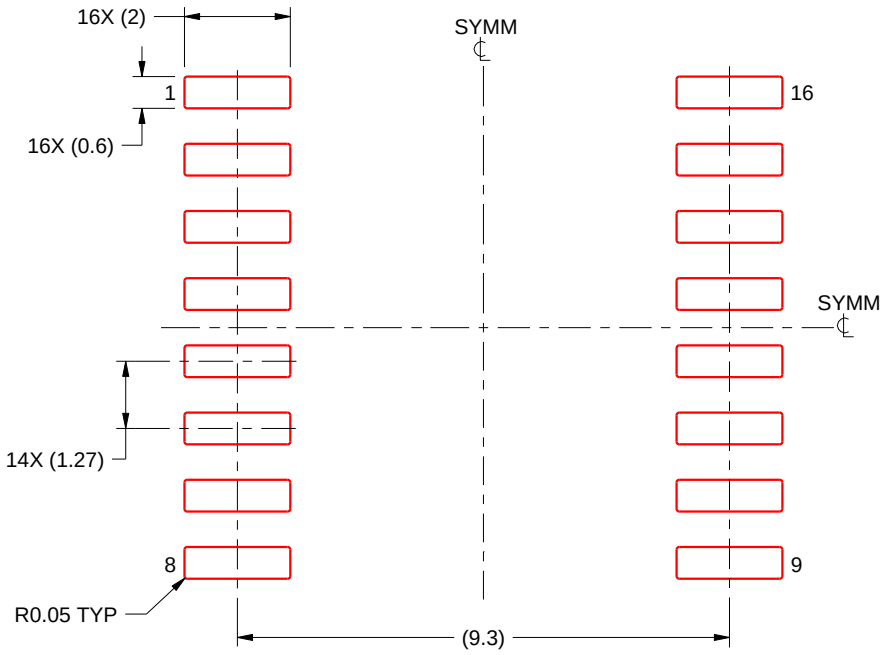


SOLDER MASK DETAILS

4220721/A 07/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:7X

4220721/A 07/2016

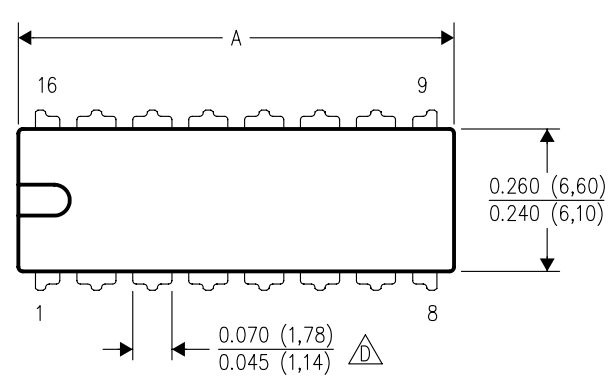
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

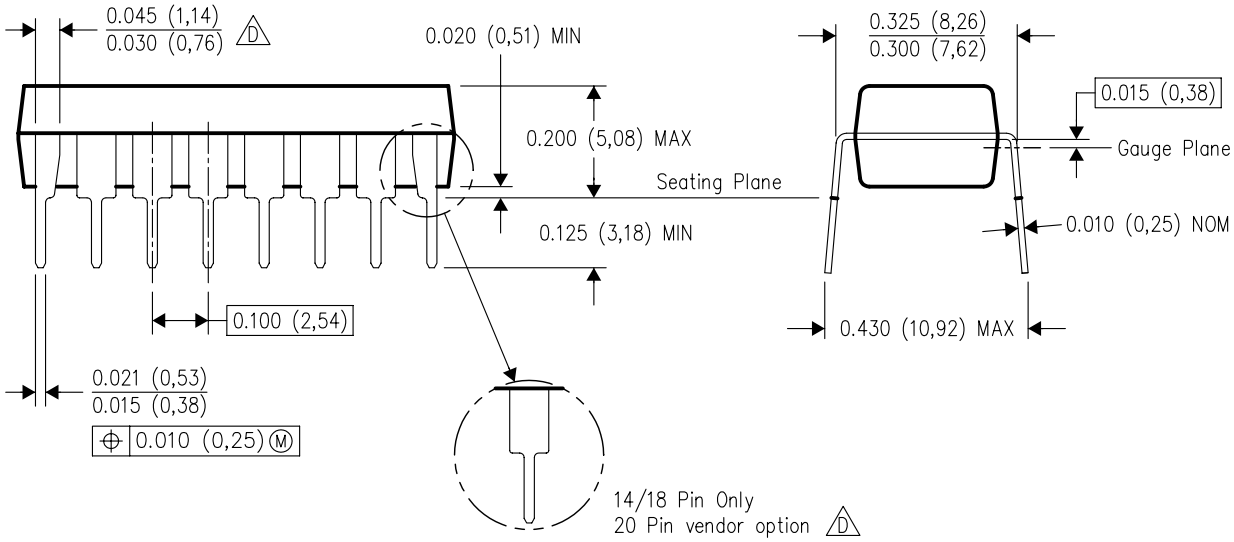
N (R–PDIP–T**)

PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN



DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD



4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

重要なお知らせと免責事項

TI は、技術データと信頼性データ (データシートを含みます)、設計リソース (リファレンス デザインを含みます)、アプリケーションや設計に関する各種アドバイス、Web ツール、安全性情報、その他のリソースを、欠陥が存在する可能性のある「現状のまま」提供しており、商品性および特定目的に対する適合性の黙示保証、第三者の知的財産権の非侵害保証を含むいかなる保証も、明示的または黙示的にかかわらず拒否します。

これらのリソースは、TI 製品を使用する設計の経験を積んだ開発者への提供を意図したものです。(1) お客様のアプリケーションに適した TI 製品の選定、(2) お客様のアプリケーションの設計、検証、試験、(3) お客様のアプリケーションに該当する各種規格や、その他のあらゆる安全性、セキュリティ、規制、または他の要件への確実な適合に関する責任を、お客様のみが単独で負うものとします。

上記の各種リソースは、予告なく変更される可能性があります。これらのリソースは、リソースで説明されている TI 製品を使用するアプリケーションの開発の目的でのみ、TI はその使用をお客様に許諾します。これらのリソースに関して、他の目的で複製することや掲載することは禁止されています。TI や第三者の知的財産権のライセンスが付与されている訳ではありません。お客様は、これらのリソースを自身で使用した結果発生するあらゆる申し立て、損害、費用、損失、責任について、TI およびその代理人を完全に補償するものとし、TI は一切の責任を拒否します。

TI の製品は、 TI の販売条件 、 TI の総合的な品質ガイドライン 、 ti.com または TI 製品などに関連して提供される他の適用条件に従い提供されます。TI がこれらのリソースを提供することは、適用される TI の保証または他の保証の放棄の拡大や変更を意味するものではありません。 TI がカスタム、またはカスタマー仕様として明示的に指定していない限り、TI の製品は標準的なカタログに掲載される汎用機器です。

お客様がいかなる追加条項または代替条項を提案する場合も、TI はそれらに異議を唱え、拒否します。

Copyright © 2026, Texas Instruments Incorporated

最終更新日：2025 年 10 月