



MCP629x 10MHz、レール・ツー・レール・オペアンプ

1 特長

- ゲイン帯域幅積：標準値 10MHz
- 動作電源電圧範囲：2.4V～5.5V
- レール・ツー・レール入出力
- 低い入力バイアス電流：1pA
- 低い静止電流：0.6mA
- 入力電圧ノイズ：f = 10kHz において 8.7nV/√Hz
- 内部 RF および EMI フィルタ
- 拡張温度範囲：-40℃～125℃
- ユニティ・ゲイン安定
- 抵抗性の開ループ出力インピーダンスにより、大きな容量性負荷で簡単に安定

2 アプリケーション

- パワー・モジュール
- 煙感知器
- HVAC：暖房、換気、空調
- バッテリー駆動のアプリケーション
- センサ信号コンディショニング
- フォトダイオード・アンプ
- アナログ・フィルタ
- 医療用計測装置
- ノートPCおよびPDA
- バーコード・スキャナ
- オーディオ・レシーバ
- 車載インフォテインメント

3 概要

MCP6291 (シングル)、MCP6292 (デュアル)、および MCP6294 (クワッド) デバイスは、汎用の低消費電力オペアンプのファミリを構成しています。レール・ツー・レールの入出力スイング、低い静止電流 (標準値 600μA/ch) と 10MHz の広い帯域幅、および低いノイズ (10kHz で 8.7nV/√Hz) から、このファミリはコストと性能のバランスを必要とする各種のアプリケーションにおいて魅力的な選択肢です。入力バイアス電流が低いため、このファミリはソースのインピーダンスが高いアプリケーションで使用できます。

MCP629xは堅牢に設計されており、ユニティ・ゲイン安定、RFIおよびEMI除去フィルタの内蔵、オーバードライブ状態で位相反転が発生しない、高い静電放電(ESD)保護 (4kV HBM) という特長から、回路設計者が簡単に使用できます。

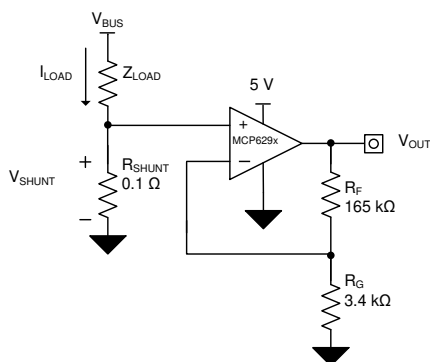
MCP629x ファミリは、拡張温度範囲の -40℃～125℃ で動作します。このファミリの電源電圧範囲は2.4V～5.5V です。

製品情報⁽¹⁾

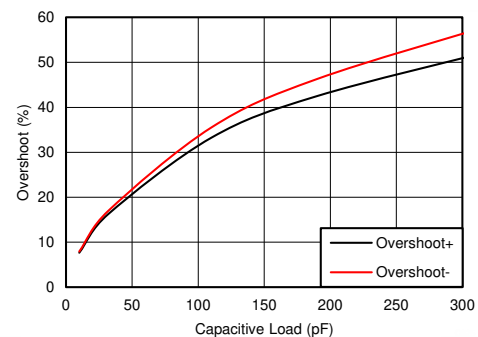
型番	パッケージ	本体サイズ(公称)
MCP6291	SOT-23 (5)	1.60mm × 2.90mm
	SC70 (5)	1.25mm×2.00mm
MCP6292	SOIC (8)	3.91mm×4.90mm
	VSSOP (8)	3.00mm×3.00mm
	SOT-23 (8)	1.60mm × 2.90mm
MCP6294	SOIC (14)	8.65mm×3.91mm
	TSSOP (14)	4.40mm×5.00mm

(1) 提供されているすべてのパッケージについては、データシートの末尾にある注文情報を参照してください。

ローサイドのモータ制御



小信号のオーバーシュートと負荷容量との関係



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4 改訂履歴

Revision C (January 2019) から Revision D に変更

•	データシートに SOT-23 (8) (DDF) パッケージを追加	1
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Revision B (April 2018) から Revision C に変更

•	「製品情報」表から SOT-23 パッケージのプレビュー版表記を削除	1
•	「製品情報」表に SC70 パッケージを追加	1
•	Added DCK package information to <i>Device Comparison Table</i>	4
•	Deleted DBV package preview notation from <i>Pin Configuration and Functions</i> section	5
•	Added DCK package drawing and pin functions to <i>Pin Configuration and Functions</i> section	5
•	Added DBV (SOT-23) and DCK (SC70) thermal information	8

Revision A (October 2017) から Revision B に変更

•	Added DGK package to <i>Thermal Information</i> table	9
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2017年7月発行のものから更新

•	「製品情報」表から MCP6291 の SC70、SOT-553、SOIC パッケージを削除	1
•	「製品情報」表から MCP6292 の WSON および VSSOP (10) パッケージを削除	1
•	「製品情報」表の MCP6294 の 14ピン SOIC パッケージをプレビューから量産データに変更	1
•	Deleted DCK, DRL, DSG, RTE and 8-pin D packages from <i>Device Comparison</i> table	4
•	Deleted DRL (SOT-533) package from MCP6291 pinout image and table in <i>Pin Configuration and Functions</i> section	5
•	Deleted MCP6291 DCK (SC70) and D (SOIC) package pinout drawings and pin information from <i>Pin Configuration and Functions</i> section	5
•	Deleted MCP6292 DSG (WSON) and DGS (VSSOP) package pinout drawings and pin table information in <i>Pin Configuration and Functions</i> section	6

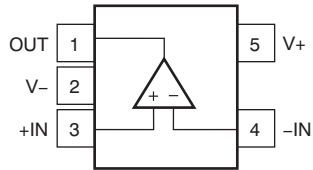
• Deleted package preview note from MCP6294 pinout drawing in <i>Pin Configuration and Functions</i> section	7
• Added MCP6294 <i>Thermal Information</i> table	9

5 Device Comparison Table

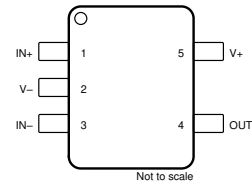
DEVICE	NO. OF CHANNELS	PACKAGE LEADS					
		DBV	DCK	D	DGK	PW	DDF
MCP6291	1	5	5	—	—	—	—
MCP6292	2	—	—	8	8	—	8
MCP6294	4	—	—	14	—	14	—

6 Pin Configuration and Functions

**MCP6291 DBV Package
5-Pin SOT-23
Top View**



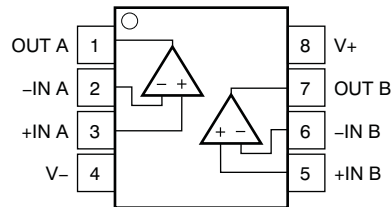
**MCP6291 DCK Package
5-Pin SC70
Top View**



Pin Functions: MCP6291

NAME	PIN NO.		I/O	DESCRIPTION
	SOT-23 (DBV)	SC70 (DCK)		
–IN	4	3	I	Inverting input
+IN	3	1	I	Noninverting input
OUT	1	4	O	Output
V–	2	8	—	Negative (lowest) supply or ground (for single-supply operation)
V+	5	5	—	Positive (highest) supply

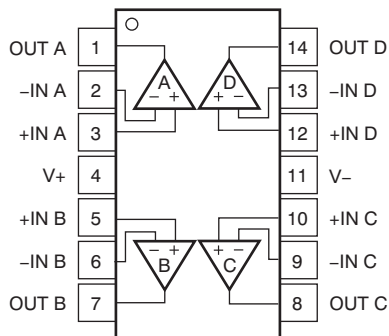
**MCP6292 D, DGK, DDF Packages
8-Pin SOIC, VSSOP
Top View**



Pin Functions: MCP6292

PIN		I/O	DESCRIPTION
NAME	NO.		
-IN A	2	I	Inverting input, channel A
+IN A	3	I	Noninverting input, channel A
-IN B	6	I	Inverting input, channel B
+IN B	5	I	Noninverting input, channel B
OUT A	1	O	Output, channel A
OUT B	7	O	Output, channel B
V-	4	—	Negative (lowest) supply or ground (for single-supply operation)
V+	8	—	Positive (highest) supply

**MCP6294 D, PW Packages
14-Pin SOIC, TSSOP
Top View**



Pin Functions: MCP6294

PIN		I/O	DESCRIPTION
NAME	NO.		
-IN A	2	I	Inverting input, channel A
+IN A	3	I	Noninverting input, channel A
-IN B	6	I	Inverting input, channel B
+IN B	5	I	Noninverting input, channel B
-IN C	9	I	Inverting input, channel C
+IN C	10	I	Noninverting input, channel C
-IN D	13	I	Inverting input, channel D
+IN D	12	I	Noninverting input, channel D
OUT A	1	O	Output, channel A
OUT B	7	O	Output, channel B
OUT C	8	O	Output, channel C
OUT D	14	O	Output, channel D
V-	11	—	Negative (lowest) supply or ground (for single-supply operation)
V+	4	—	Positive (highest) supply

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature (unless otherwise noted)⁽¹⁾

			MIN	MAX	UNIT
Supply voltage			6		V
Signal input pins	Voltage ⁽²⁾	Common-mode	(V–) – 0.5	(V+) + 0.5	V
		Differential	(V+) – (V–) + 0.2		
	Current ⁽²⁾		–10	10	mA
Output short-circuit ⁽³⁾			Continuous		mA
Specified, T _A			–40	125	°C
Junction, T _J			150		°C
Storage, T _{stg}			–65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) Input pins are diode-clamped to the power-supply rails. Current limit input signals that can swing more than 0.5 V beyond the supply rails to 10 mA or less.
- (3) Short-circuit to ground, one amplifier per package.

7.2 ESD Ratings

over operating free-air temperature range (unless otherwise noted)

			VALUE	UNIT
V _(ESD)	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	±4000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾	±1500	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V _S	Supply voltage	2.4	5.5	V
	Specified temperature	–40	125	°C

7.4 Thermal Information: MCP6291

THERMAL METRIC ⁽¹⁾		MCP6291		UNIT
		DBV (SOT-23)	DCK (SC70)	
		5 PINS	5 PINS	
R _{θJA}	Junction-to-ambient thermal resistance	221.7	263.3	°C/W
R _{θJC(top)}	Junction-to-case(top) thermal resistance	144.7	75.5	°C/W
R _{θJB}	Junction-to-board thermal resistance	49.7	51.0	°C/W
ψ _{JT}	Junction-to-top characterization parameter	26.1	1.0	°C/W
ψ _{JB}	Junction-to-board characterization parameter	49.0	50.3	°C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

7.5 Thermal Information: MCP6292

THERMAL METRIC ⁽¹⁾		MCP6292			UNIT
		D (SOIC)	DGK (VSSOP)	DDF (SOT-23)	
		8 PINS	8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	157.6	201.2	184.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	104.6	85.7	112.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	99.7	122.9	99.9	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	55.6	21.2	18.7	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	99.2	121.4	99.3	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

7.6 Thermal Information: MCP6294

THERMAL METRIC ⁽¹⁾		MCP6294		UNIT
		D (SOIC)	PW (TSSOP)	
		14 PINS	14 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	106.9	135.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case(top) thermal resistance	64	64	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	63	79	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	25.9	15.7	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	62.7	78.4	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

7.7 Electrical Characteristics: V_S (Total Supply Voltage) = $(V_+) - (V_-) = 2.4\text{ V to }5.5\text{ V}$

at $T_A = 25^\circ\text{C}$, $R_L = 10\text{ k}\Omega$ connected to $V_S / 2$, $V_{CM} = V_S / 2$, and $V_{OUT} = V_S / 2$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFFSET VOLTAGE						
V _{OS}	Input offset voltage	V _S = 5 V		±0.3	±3	mV
		V _S = 5 V, T _A = −40°C to 125°C			±5	
dV _{OS} /dT	Drift	V _S = 5 V, T _A = −40°C to 125°C		±1.1		μV/°C
PSRR	Power-supply rejection ratio	V _S = 2.4 V – 5.5 V, V _{CM} = (V−)		±7		μV/V
	Channel separation, DC	At DC		100		dB
INPUT VOLTAGE RANGE						
V _{CM}	Common-mode voltage range	V _S = 2.4 V to 5.5 V	(V−) − 0.1		(V+) + 0.1	V
CMRR	Common-mode rejection ratio	V _S = 5.5 V (V−) − 0.1 V < V _{CM} < (V+) − 1.4 V T _A = −40°C to 125°C	80	103		dB
		V _S = 5.5 V V _{CM} = −0.1 V to 5.6 V T _A = −40°C to 125°C	57	87		
		V _S = 2.4 V (V−) − 0.1 V < V _{CM} < (V+) − 1.4 V T _A = −40°C to 125°C		88		
		V _S = 2.4 V V _{CM} = −0.1 V to 1.9 V T _A = −40°C to 125°C		81		
INPUT BIAS CURRENT						
I _B	Input bias current			±1		pA
I _{OS}	Input offset current			±0.05		pA
NOISE						
E _n	Input voltage noise (peak-to-peak)	V _S = 5 V, f = 0.1 Hz to 10 Hz		4.77		μV _{PP}
e _n	Input voltage noise density	V _S = 5 V, f = 10 kHz, R _L = 10 kΩ		8.7		nV/√Hz
		V _S = 5 V, f = 1 kHz, R _L = 10 kΩ		16		
i _n	Input current noise density	f = 1 kHz		10		fA/√Hz
INPUT CAPACITANCE						
C _{ID}	Differential			2		pF
C _{IC}	Common-mode			4		pF
OPEN-LOOP GAIN						
A _{OL}	Open-loop voltage gain	V _S = 2.4 V (V−) + 0.04 V < V _O < (V+) − 0.04 V R _L = 10 kΩ		100		dB
		V _S = 5.5 V (V−) + 0.05 V < V _O < (V+) − 0.05 V R _L = 10 kΩ	104	130		
		V _S = 2.4 V (V−) + 0.06 V < V _O < (V+) − 0.06 V R _L = 2 kΩ		100		
		V _S = 5.5 V (V−) + 0.15 V < V _O < (V+) − 0.15 V R _L = 2 kΩ		130		
FREQUENCY RESPONSE						
GBP	Gain bandwidth product	V _S = 5 V, G = 1		10		MHz
Φ _m	Phase margin	V _S = 5 V, G = 1		55		°
SR	Slew rate	V _S = 5 V, G = 1		6.5		V/μs
t _S	Settling time	To 0.1%, V _S = 5 V, 2-V step , G = 1 C _L = 100 pF		0.5		μs
		To 0.01%, V _S = 5 V, 2-V step , G = 1 C _L = 100 pF		1		
t _{OR}	Overload recovery time	V _S = 5 V V _{IN} × gain > V _S		0.2		μs

Electrical Characteristics: V_S (Total Supply Voltage) = (V+) – (V–) = 2.4 V to 5.5 V (continued)

 at $T_A = 25^\circ\text{C}$, $R_L = 10\text{ k}\Omega$ connected to $V_S / 2$, $V_{CM} = V_S / 2$, and $V_{OUT} = V_S / 2$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
THD + N Total harmonic distortion + noise ⁽¹⁾	$V_S = 5\text{ V}$ $V_O = 1\text{ V}_{RMS}$ $G = 1$, $f = 1\text{ kHz}$		0.0008%		
OUTPUT					
V_O Voltage output swing from supply rails	$V_S = 5.5\text{ V}$, $R_L = 10\text{ k}\Omega$			15	mV
	$V_S = 5.5\text{ V}$, $R_L = 2\text{ k}\Omega$			50	
I_{SC} Short-circuit current	$V_S = 5\text{ V}$		± 50		mA
Z_O Open-loop output impedance	$V_S = 5\text{ V}$, $f = 10\text{ MHz}$		100		Ω
POWER SUPPLY					
I_Q Quiescent current per amplifier	$V_S = 5.5\text{ V}$, $I_O = 0\text{ mA}$		600	1300	μA

(1) Third-order filter; bandwidth = 80 kHz at –3 dB.

7.8 Typical Characteristics

at $T_A = 25^\circ\text{C}$, $V_S = 5.5\text{ V}$, $R_L = 10\text{ k}\Omega$ connected to $V_S / 2$, $V_{CM} = V_S / 2$, and $V_{OUT} = V_S / 2$ (unless otherwise noted)

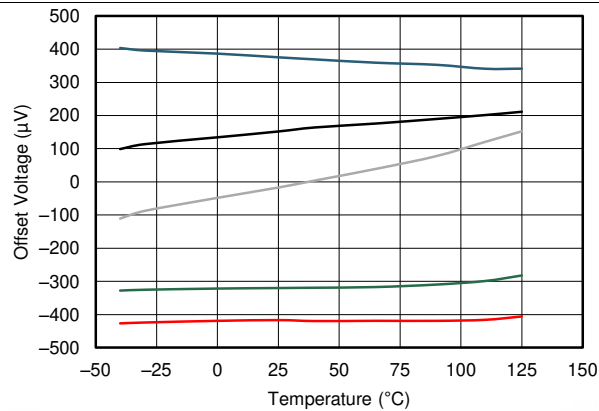


图 1. Offset Voltage vs Temperature

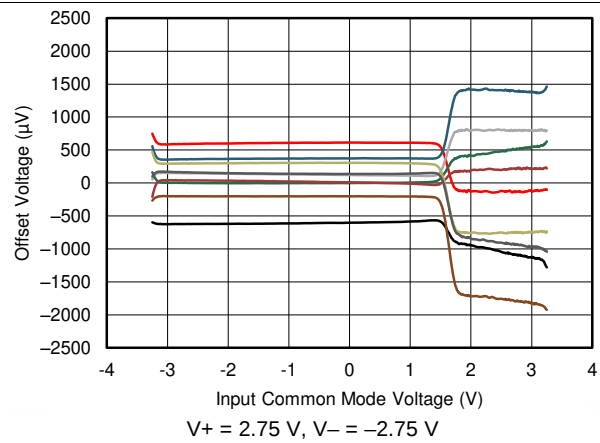


图 2. Offset Voltage vs Common-Mode Voltage

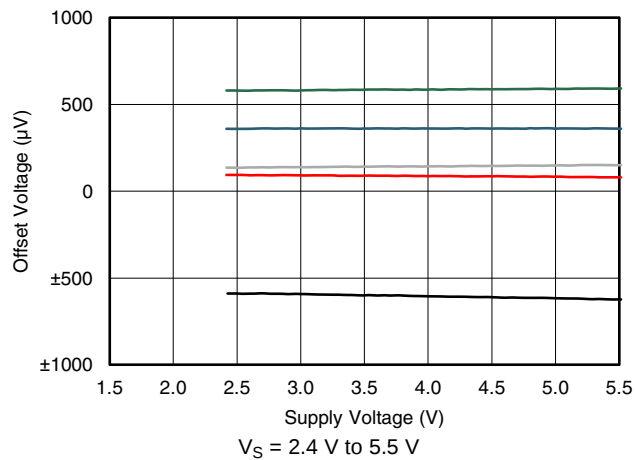


图 3. Offset Voltage vs Power Supply

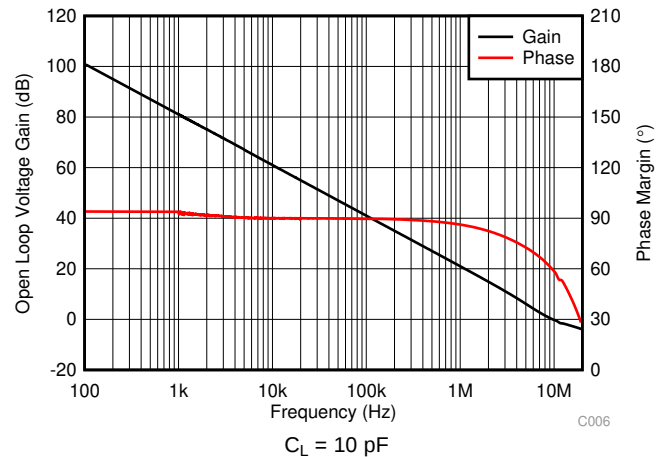


图 4. Open-Loop Gain and Phase vs Frequency

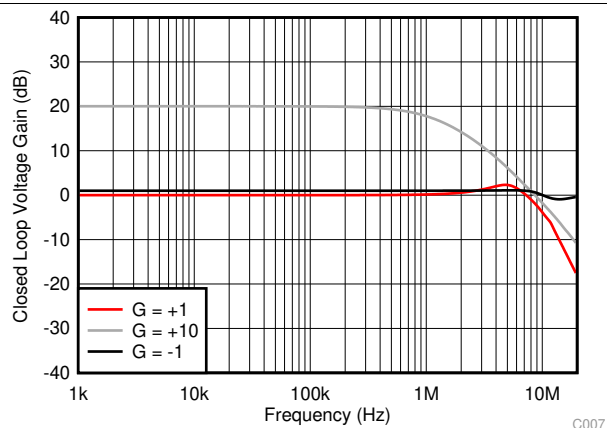


图 5. Closed-Loop Gain vs Frequency

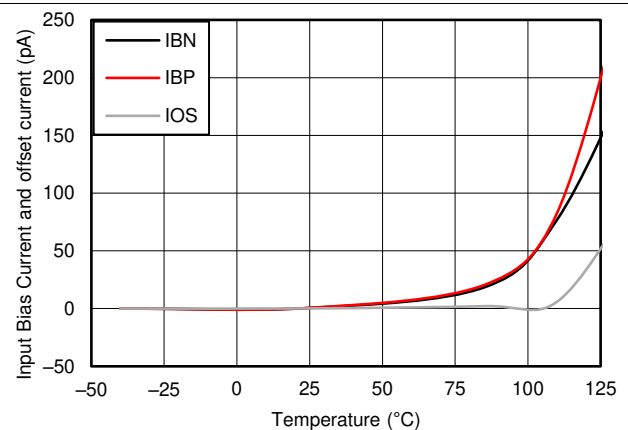


图 6. Input Bias Current vs Temperature

Typical Characteristics (continued)

at $T_A = 25^\circ\text{C}$, $V_S = 5.5\text{ V}$, $R_L = 10\text{ k}\Omega$ connected to $V_S / 2$, $V_{CM} = V_S / 2$, and $V_{OUT} = V_S / 2$ (unless otherwise noted)

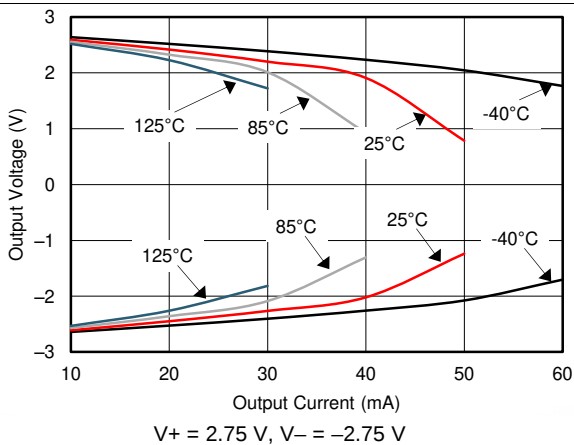


Figure 7. Output Voltage Swing vs Output Current

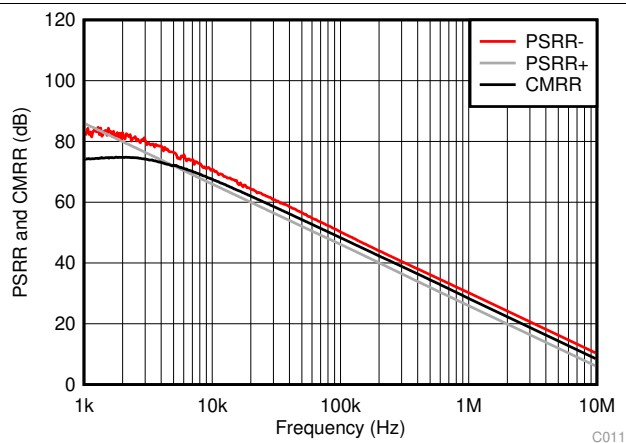


Figure 8. CMRR and PSRR vs Frequency (Referred to Input)

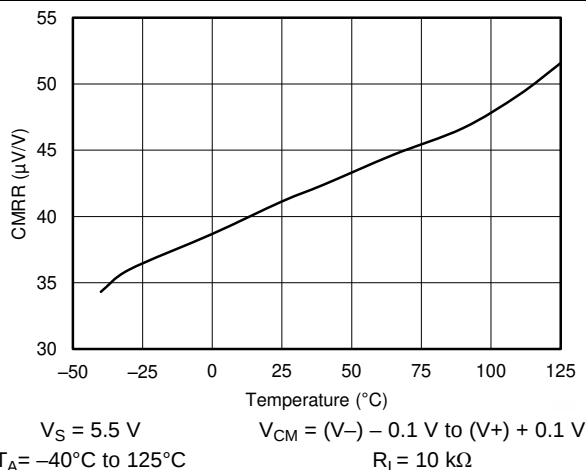


Figure 9. CMRR vs Temperature

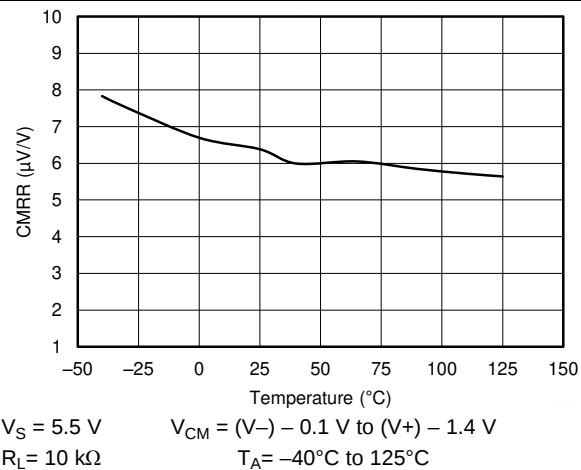


Figure 10. CMRR vs Temperature

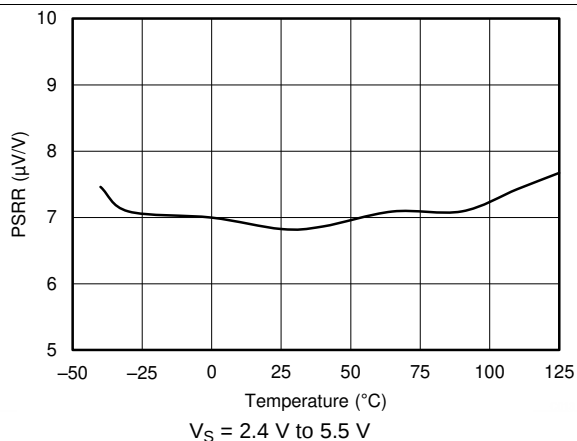


Figure 11. PSRR vs Temperature

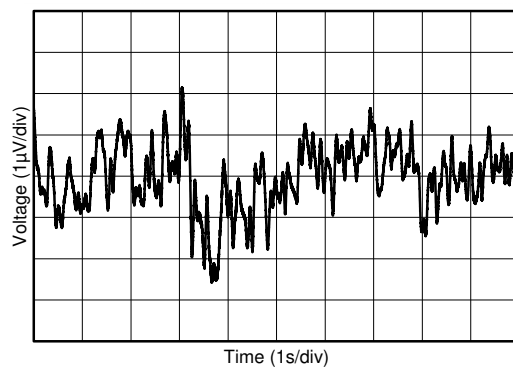


Figure 12. 0.1-Hz to 10-Hz Input Voltage Noise

Typical Characteristics (continued)

at $T_A = 25^\circ\text{C}$, $V_S = 5.5\text{ V}$, $R_L = 10\text{ k}\Omega$ connected to $V_S / 2$, $V_{CM} = V_S / 2$, and $V_{OUT} = V_S / 2$ (unless otherwise noted)

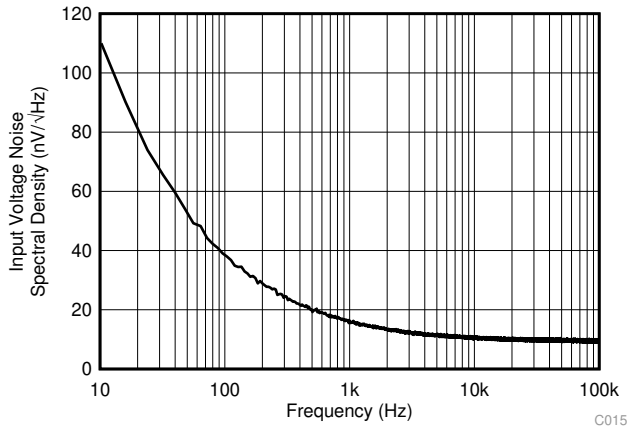


FIG 13. Input Voltage Noise Spectral Density vs Frequency

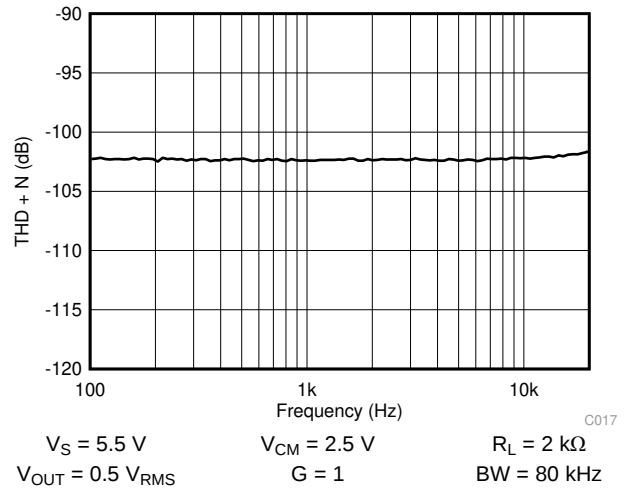


FIG 14. THD + N vs Frequency

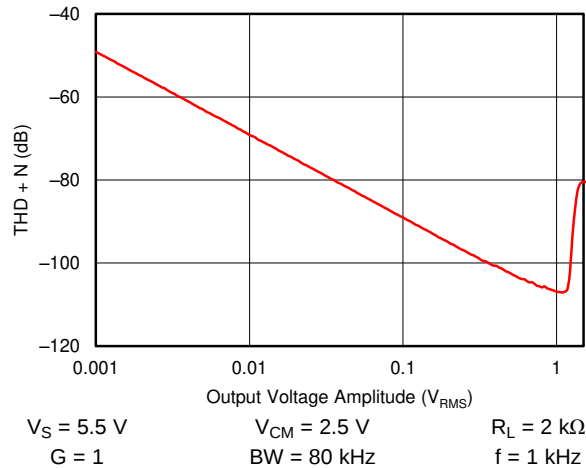


FIG 15. THD + N vs Amplitude

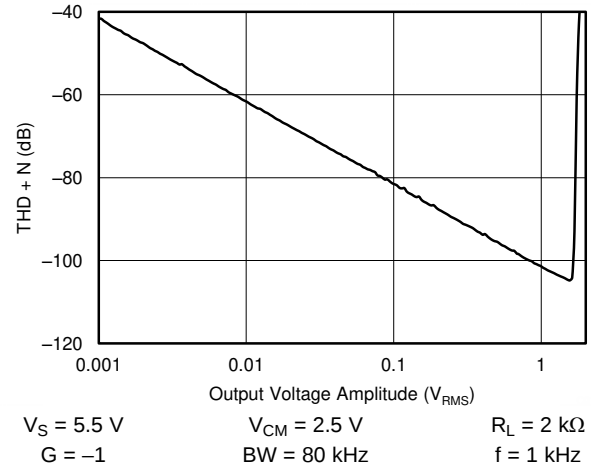


FIG 16. THD + N vs Amplitude

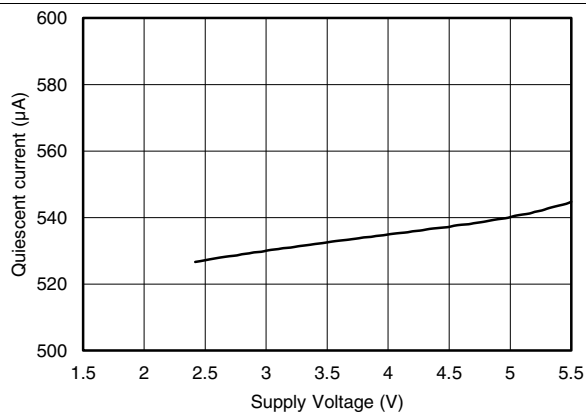


FIG 17. Quiescent Current vs Supply Voltage

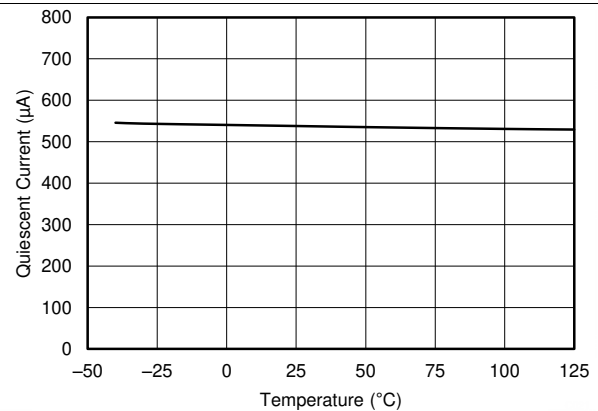


FIG 18. Quiescent Current vs Temperature

Typical Characteristics (continued)

at $T_A = 25^\circ\text{C}$, $V_S = 5.5\text{ V}$, $R_L = 10\text{ k}\Omega$ connected to $V_S / 2$, $V_{CM} = V_S / 2$, and $V_{OUT} = V_S / 2$ (unless otherwise noted)

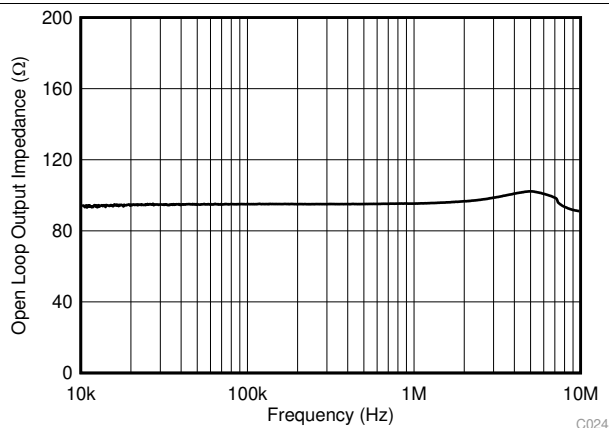
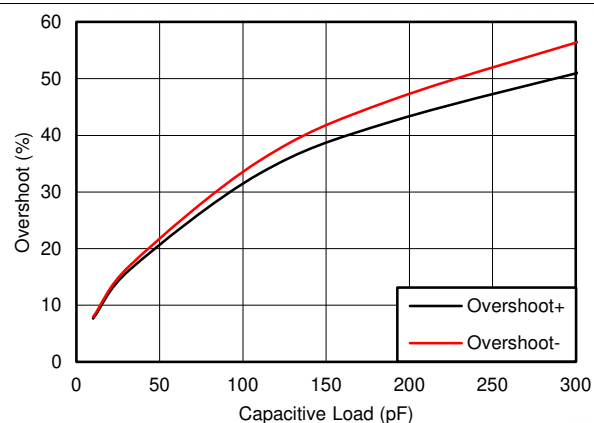
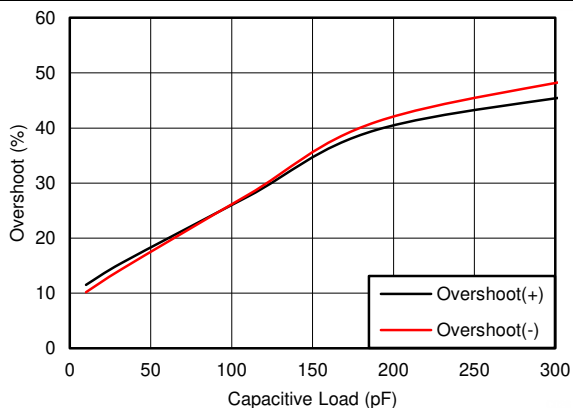


FIG 19. Open-Loop Output Impedance vs Frequency



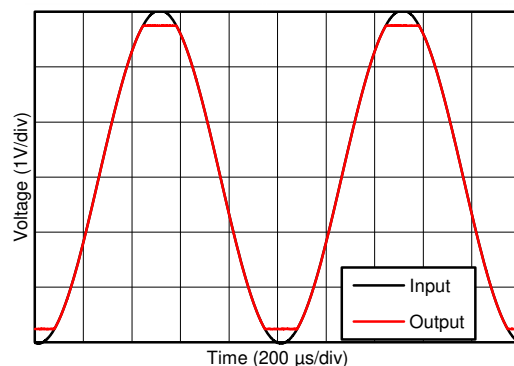
$V_+ = 2.75\text{ V}$ $V_- = -2.75\text{ V}$ $G = 1\text{ V/V}$
 $R_L = 10\text{ k}\Omega$ $V_{OUT}\text{ step} = 100\text{ mV}_{p-p}$

FIG 20. Small-Signal Overshoot vs Load Capacitance



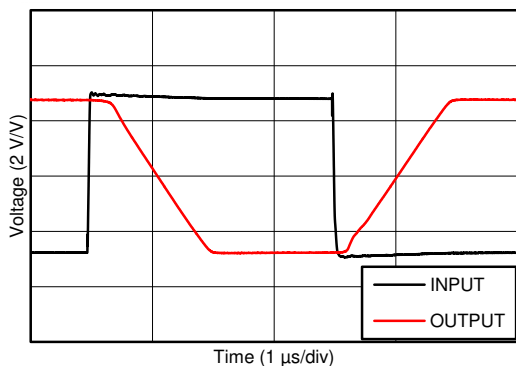
$V_+ = 2.75\text{ V}$ $V_- = -2.75\text{ V}$ $G = -1\text{ V/V}$
 $R_L = 10\text{ k}\Omega$ $V_{OUT}\text{ step} = 100\text{ mV}_{p-p}$

FIG 21. Small-Signal Overshoot vs Load Capacitance



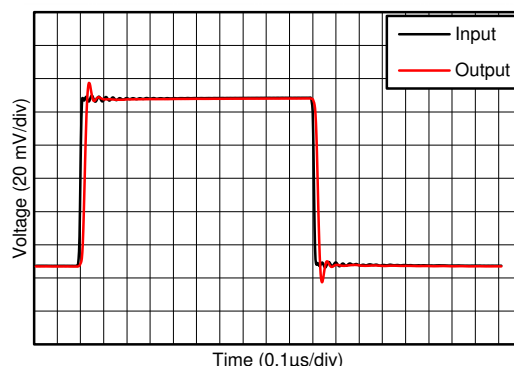
$V_+ = 2.75\text{ V}$, $V_- = -2.75\text{ V}$

FIG 22. No Phase Reversal



$V_+ = 2.75\text{ V}$ $V_- = -2.75\text{ V}$ $G = -10\text{ V/V}$

FIG 23. Overload Recovery

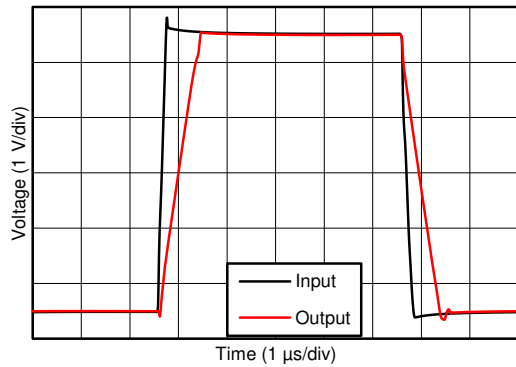


$V_+ = 2.75\text{ V}$ $V_- = -2.75\text{ V}$ $G = 1\text{ V/V}$

FIG 24. Small-Signal Step Response

Typical Characteristics (continued)

at $T_A = 25^\circ\text{C}$, $V_S = 5.5\text{ V}$, $R_L = 10\text{ k}\Omega$ connected to $V_S / 2$, $V_{CM} = V_S / 2$, and $V_{OUT} = V_S / 2$ (unless otherwise noted)



$V_+ = 2.75\text{ V}$ $V_- = -2.75\text{ V}$ $C_L = 100\text{ pF}$
 $G = 1\text{ V/V}$

FIG 25. Large-Signal Step Response

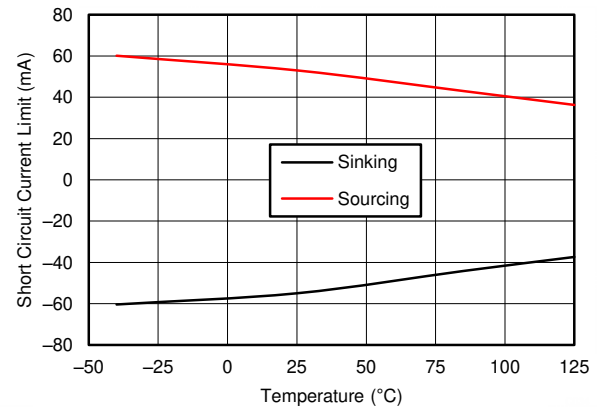


FIG 26. Short-Circuit Current vs Temperature

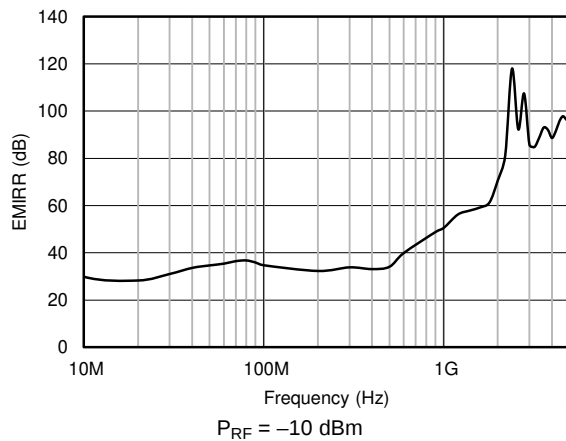


FIG 27. Electromagnetic Interference Rejection Ratio Referred to Noninverting Input (EMIRR+) vs Frequency

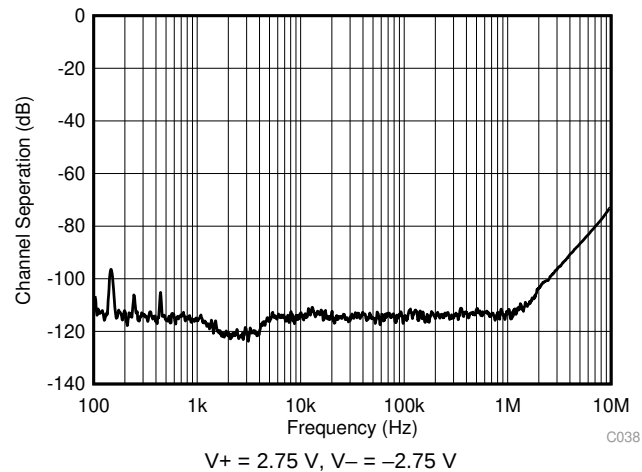


FIG 28. Channel Separation vs Frequency

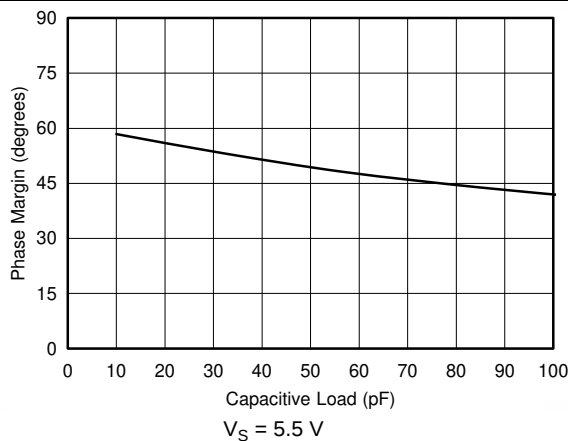


FIG 29. Phase Margin vs Capacitive Load

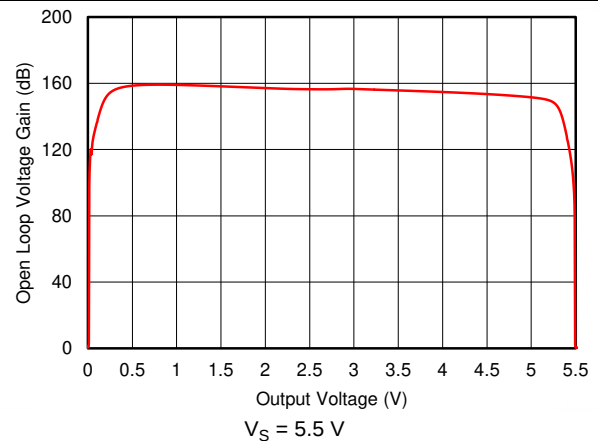


FIG 30. Open Loop Voltage Gain vs Output Voltage

Typical Characteristics (continued)

at $T_A = 25^\circ\text{C}$, $V_S = 5.5\text{ V}$, $R_L = 10\text{ k}\Omega$ connected to $V_S / 2$, $V_{CM} = V_S / 2$, and $V_{OUT} = V_S / 2$ (unless otherwise noted)

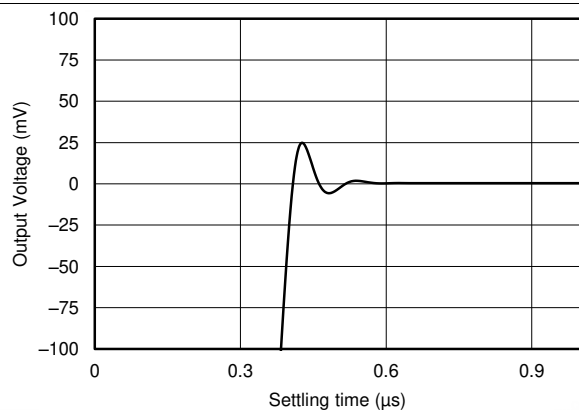


FIG 31. Large Signal Settling Time (Positive)

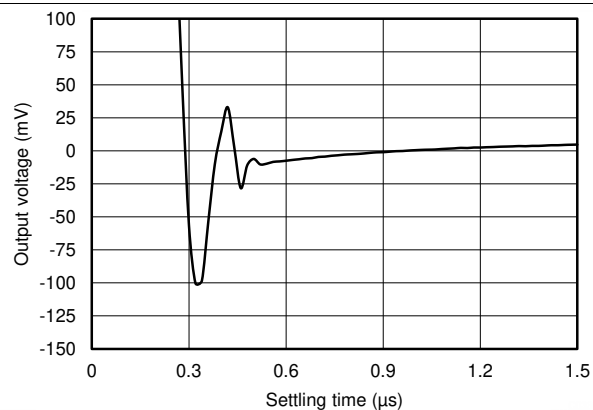


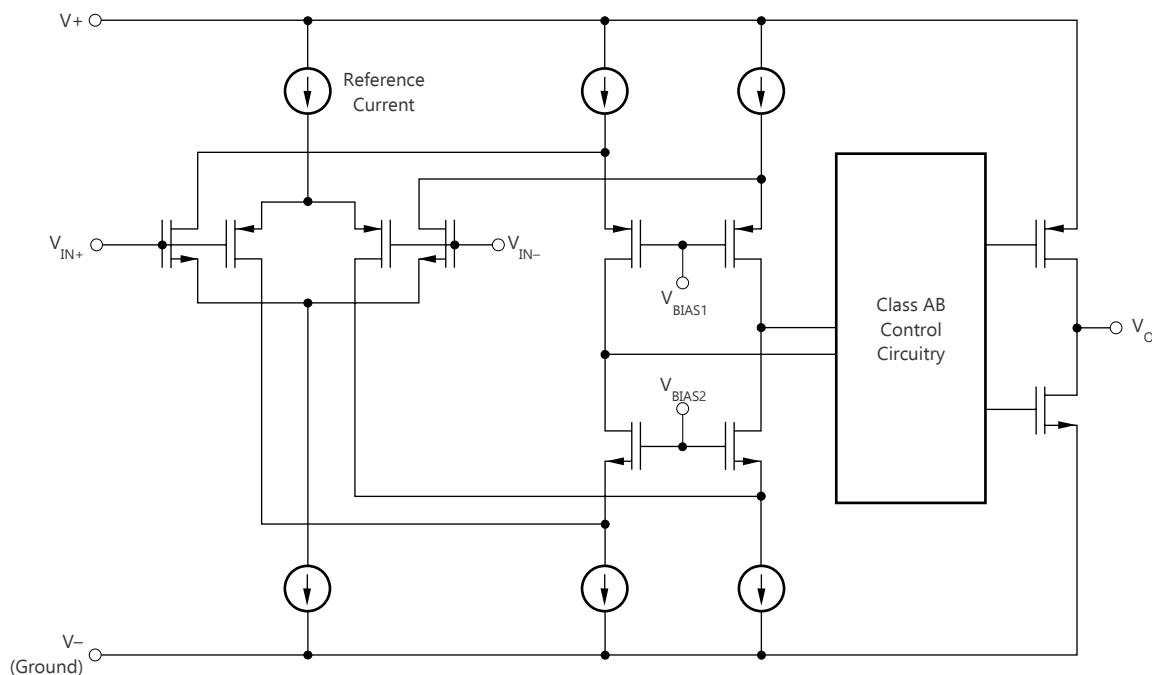
FIG 32. Large Signal Settling Time (Negative)

8 Detailed Description

8.1 Overview

The MCP629x series is a family of low-power, rail-to-rail input and output op amps. These devices operate from 2.4 V to 5.5 V, are unity-gain stable, and are designed for a wide range of general-purpose applications. The input common-mode voltage range includes both rails and allows the MCP629x series to be used in any single-supply application. Rail-to-rail input and output swing significantly increases dynamic range in low-supply applications and are designed for driving sampling analog-to-digital converters (ADCs).

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Rail-to-Rail Input

The input common-mode voltage range of the MCP629x family extends 100 mV beyond the supply rails for the full supply voltage range of 2.4 V to 5.5 V. This performance is achieved with a complementary input stage: an N-channel input differential pair in parallel with a P-channel differential pair, as the [Functional Block Diagram](#) shows. The N-channel pair is active for input voltages close to the positive rail, typically $(V+) - 1.4\text{ V}$ to 100 mV above the positive supply, whereas the P-channel pair is active for inputs from 100 mV below the negative supply to approximately $(V+) - 1.4\text{ V}$. There is a small transition region, typically $(V+) - 1.2\text{ V}$ to $(V+) - 1\text{ V}$, in which both pairs are on. This 200-mV transition region can vary up to 200 mV with process variation. Thus, the transition region (with both stages on) can range from $(V+) - 1.4\text{ V}$ to $(V+) - 1.2\text{ V}$ on the low end, and up to $(V+) - 1\text{ V}$ to $(V+) - 0.8\text{ V}$ on the high end. Within this transition region, PSRR, CMRR, offset voltage, offset drift, and THD can degrade compared to device operation outside this region.

8.3.2 Rail-to-Rail Output

Designed as a low-power, low-voltage operational amplifier, the MCP629x series delivers a robust output drive capability. A class AB output stage with common-source transistors achieves full rail-to-rail output swing capability. For resistive loads of 10 k Ω , the output swings to within 15 mV of either supply rail, regardless of the applied power-supply voltage. Different load conditions change the ability of the amplifier to swing close to the rails.

8.3.3 Overload Recovery

Overload recovery is defined as the time required for the operational amplifier output to recover from a saturated state to a linear state. The output devices of the operational amplifier enter a saturation region when the output voltage exceeds the rated operating voltage, because of the high input voltage or the high gain. After the device enters the saturation region, the charge carriers in the output devices require time to return to the linear state. After the charge carriers return to the linear state, the device begins to slew at the specified slew rate. Therefore, the propagation delay (in case of an overload condition) is the sum of the overload recovery time and the slew time. The overload recovery time for the MCP629x series is approximately 200 ns.

8.4 Device Functional Modes

The MCP629x family has a single functional mode. These devices are powered on as long as the power-supply voltage is between 2.4 V ($\pm 1.2\text{ V}$) and 5.5 V ($\pm 2.75\text{ V}$).

9 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The MCP629x series features 10-MHz bandwidth and 6.5-V/ μ s slew rate with only 600 μ A of supply current per channel, providing good AC performance at low power consumption. DC applications are well served with a low input noise voltage of 8.7 nV / $\sqrt{\text{Hz}}$ at 10 kHz, low input bias current, and a typical input offset voltage of 0.3 mV.

9.2 Typical Application

Figure 33 shows the MCP629x configured in a low-side, motor-control application.

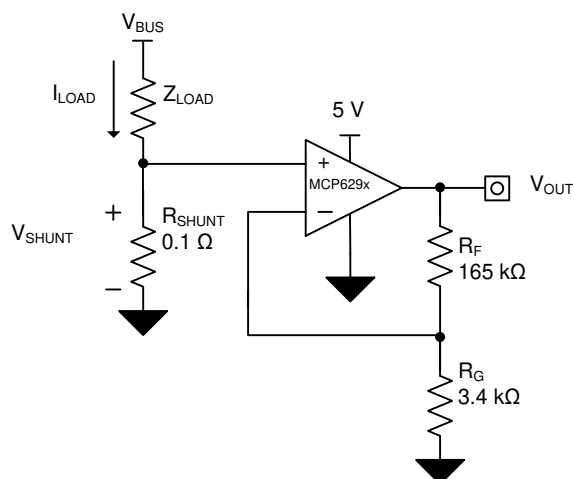


Figure 33. MCP629x in a Low-Side, Motor-Control Application

9.2.1 Design Requirements

The design requirements for this design are:

- Load current: 0 A to 1 A
- Output voltage: 4.95 V
- Maximum shunt voltage: 100 mV

Typical Application (continued)

9.2.2 Detailed Design Procedure

The transfer function of the circuit in [Figure 33](#) is shown in [Equation 1](#).

$$V_{OUT} = I_{LOAD} \times R_{SHUNT} \times \text{Gain} \quad (1)$$

The load current (I_{LOAD}) produces a voltage drop across the shunt resistor (R_{SHUNT}). The load current is set from 0 A to 1 A. To keep the shunt voltage below 100 mV at maximum load current, the largest shunt resistor is defined using [Equation 2](#).

$$R_{SHUNT} = \frac{V_{SHUNT_MAX}}{I_{LOAD_MAX}} = \frac{100\text{mV}}{1\text{A}} = 100\text{m}\Omega \quad (2)$$

Using [Equation 2](#), R_{SHUNT} is 100 m Ω . The voltage drop produced by I_{LOAD} and R_{SHUNT} is amplified by the MCP629x to produce an output voltage of roughly 0 V to 4.95 V. The gain needed by the MCP629x to produce the necessary output voltage is calculated using [Equation 3](#):

$$\text{Gain} = \frac{(V_{OUT_MAX} - V_{OUT_MIN})}{(V_{IN_MAX} - V_{IN_MIN})} \quad (3)$$

Using [Equation 3](#), the required gain is calculated to be 49.5 V/V, which is set with resistors R_F and R_G . [Equation 4](#) is used to size the resistors, R_F and R_G , to set the gain of the MCP629x to 49.5 V/V.

$$\text{Gain} = 1 + \frac{(R_F)}{(R_G)} \quad (4)$$

Choosing R_F as 165 k Ω and R_G as 3.4 k Ω provides a combination that equals roughly 49.5 V/V. [Figure 34](#) shows the measured transfer function of the circuit shown in [Figure 33](#).

9.2.3 Application Curve

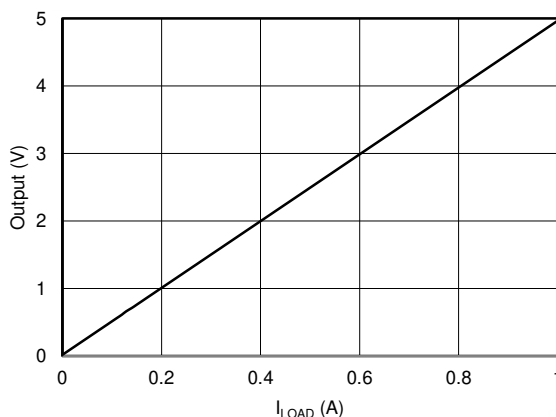


Figure 34. Low-Side, Current-Sense Transfer Function

10 Power Supply Recommendations

The MCP629x series is specified for operation from 2.4 V to 5.5 V (± 1.2 V to ± 2.75 V); many specifications apply from -40°C to 125°C . The [Typical Characteristics](#) section presents parameters that can exhibit significant variance with regard to operating voltage or temperature.

注意

Supply voltages larger than 6 V can permanently damage the device; see the [Absolute Maximum Ratings](#) table.

Place 0.1- μF bypass capacitors close to the power-supply pins to reduce errors coupling in from noisy or high-impedance power supplies. For more detailed information on bypass capacitor placement, see the [Layout Example](#) section.

10.1 Input and ESD Protection

The MCP629x series incorporates internal ESD protection circuits on all pins. For input and output pins, this protection primarily consists of current-steering diodes connected between the input and power-supply pins. These ESD protection diodes provide in-circuit, input overdrive protection, as long as the current is limited to 10-mA, as stated in the [Absolute Maximum Ratings](#) table. [Figure 35](#) shows how a series input resistor is added to the driven input to limit the input current. The added resistor contributes thermal noise at the amplifier input and the value must be kept to a minimum in noise-sensitive applications.

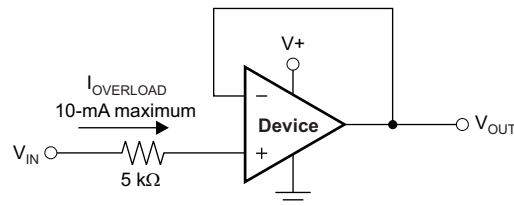


Figure 35. Input Current Protection

11 Layout

11.1 Layout Guidelines

For best operational performance of the device, use good printed-circuit board (PCB) layout practices, including:

- Noise can propagate into analog circuitry through the power pins of the circuit as a whole and of op amp itself. Bypass capacitors reduce the coupled noise by providing low-impedance power sources local to the analog circuitry.
 - Connect low-ESR, 0.1- μ F ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from V+ to ground is applicable for single-supply applications.
- Separate grounding for analog and digital portions of circuitry is one of the simplest and most-effective methods of noise suppression. One or more layers on multilayer PCBs are usually devoted to ground planes. A ground plane helps distribute heat and reduces electromagnetic interference (EMI) noise pickup. Make sure to physically separate digital and analog grounds, paying attention to the flow of the ground current. For more detailed information, see [Circuit Board Layout Techniques](#).
- To reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If these traces cannot be kept separate, crossing the sensitive trace perpendicular is much better as opposed to in parallel with the noisy trace.
- Place the external components as close to the device as possible. As shown in [Figure 37](#), keeping RF and RG close to the inverting input minimizes parasitic capacitance on the inverting input.
- Keep the length of input traces as short as possible. Always remember that the input traces are the most sensitive part of the circuit.
- Consider a driven, low-impedance guard ring around the critical traces. A guard ring can significantly reduce leakage currents from nearby traces that are at different potentials.
- Cleaning the PCB following board assembly is recommended for best performance.
- Any precision integrated circuit can experience performance shifts resulting from moisture ingress into the plastic package. Following any aqueous PCB cleaning process, baking the PCB assembly is recommended to remove moisture introduced into the device packaging during the cleaning process. A low-temperature, post-cleaning bake at 85°C for 30 minutes is sufficient for most circumstances.

11.2 Layout Example

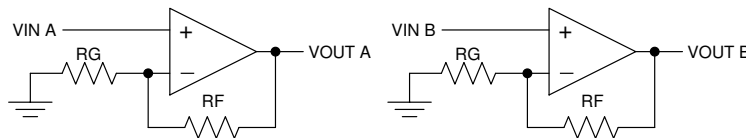


Figure 36. Schematic Representation for Figure 37

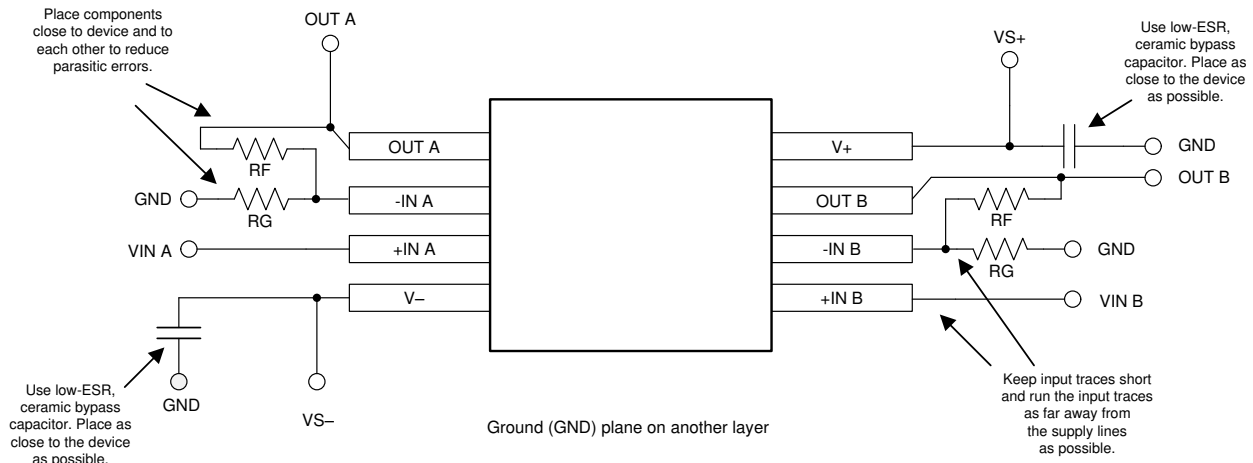


Figure 37. Layout Example

12 デバイスおよびドキュメントのサポート

12.1 ドキュメントのサポート

12.1.1 関連資料

関連資料については、以下を参照してください。

『[基板のレイアウト技法](#)』、SLOA089

12.2 関連リンク

次の表に、クイック・アクセス・リンクを示します。カテゴリには、技術資料、サポートおよびコミュニティ・リソース、ツールとソフトウェア、およびご注文へのクイック・アクセスが含まれます。

表 1. 関連リンク

製品	プロダクト・フォルダ	ご注文はこちら	技術資料	ツールとソフトウェア	サポートとコミュニティ
MCP6291	ここをクリック	ここをクリック	ここをクリック	ここをクリック	ここをクリック
MCP6292	ここをクリック	ここをクリック	ここをクリック	ここをクリック	ここをクリック
MCP6294	ここをクリック	ここをクリック	ここをクリック	ここをクリック	ここをクリック

12.3 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、[ti.com](#)のデバイス製品フォルダを開いてください。右上の「アラートを受け取る」をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

12.4 コミュニティ・リソース

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

12.5 商標

E2E is a trademark of Texas Instruments.

All other trademarks are the property of their respective owners.

12.6 静電気放電に関する注意事項



すべての集積回路は、適切なESD保護方法を用いて、取扱いと保存を行うようにして下さい。

静電気放電はわずかな性能の低下から完全なデバイスの故障に至るまで、様々な損傷を与えます。高精度の集積回路は、損傷に対して敏感であり、極めてわずかなパラメータの変化により、デバイスに規定された仕様に適合しなくなる場合があります。

12.7 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。この情報は、そのデバイスについて利用可能な最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
MCP6291IDBVR	Active	Production	SOT-23 (DBV) 5	3000 LARGE T&R	Yes	NIPDAU SN	Level-1-260C-UNLIM	-40 to 125	1U3F
MCP6291IDBVR.A	Active	Production	SOT-23 (DBV) 5	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1U3F
MCP6291IDBVRG4	Active	Production	SOT-23 (DBV) 5	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1U3F
MCP6291IDBVRG4.A	Active	Production	SOT-23 (DBV) 5	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1U3F
MCP6291IDCKR	Active	Production	SC70 (DCK) 5	3000 LARGE T&R	Yes	POST-PLAT AG SPOT SN	Level-2-260C-1 YEAR	-40 to 125	1EL
MCP6291IDCKR.A	Active	Production	SC70 (DCK) 5	3000 LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	1EL
MCP6292IDDFR	Active	Production	SOT-23-THIN (DDF) 8	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	M292
MCP6292IDDFR.A	Active	Production	SOT-23-THIN (DDF) 8	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	M292
MCP6292IDGKR	Active	Production	VSSOP (DGK) 8	2500 LARGE T&R	Yes	NIPDAU SN NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	M292
MCP6292IDGKR.A	Active	Production	VSSOP (DGK) 8	2500 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	M292
MCP6292IDGKT	Active	Production	VSSOP (DGK) 8	250 SMALL T&R	Yes	NIPDAU SN NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	M292
MCP6292IDGKT.A	Active	Production	VSSOP (DGK) 8	250 SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	M292
MCP6292IDR	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	MC6292
MCP6292IDR.A	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	MC6292
MCP6294IDR	Active	Production	SOIC (D) 14	2500 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	MCP6294D
MCP6294IDR.A	Active	Production	SOIC (D) 14	2500 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	MCP6294D
MCP6294IPWR	Active	Production	TSSOP (PW) 14	2000 LARGE T&R	Yes	NIPDAU SN	Level-2-260C-1 YEAR	-40 to 125	MCP6294
MCP6294IPWR.A	Active	Production	TSSOP (PW) 14	2000 LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	MCP6294
MCP6294IPWT	Active	Production	TSSOP (PW) 14	250 SMALL T&R	Yes	NIPDAU SN	Level-2-260C-1 YEAR	-40 to 125	MCP6294
MCP6294IPWT.A	Active	Production	TSSOP (PW) 14	250 SMALL T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	MCP6294

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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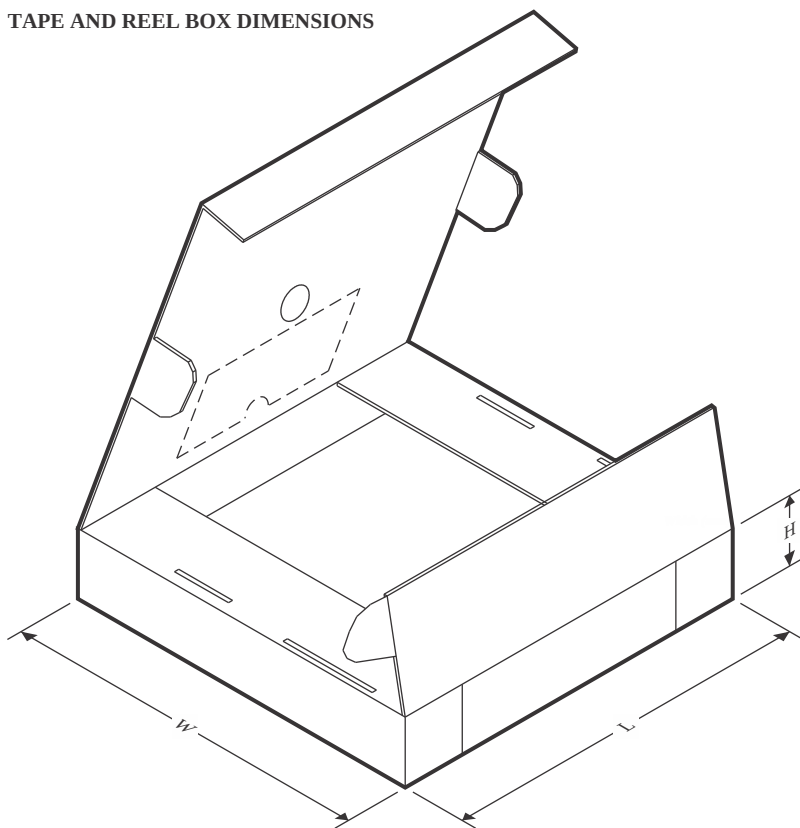
TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
MCP6291IDBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
MCP6291IDBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
MCP6291IDBVRG4	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
MCP6291IDCKR	SC70	DCK	5	3000	178.0	8.4	2.25	2.45	1.2	4.0	8.0	Q3
MCP6292IDDFR	SOT-23-THIN	DDF	8	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
MCP6292IDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
MCP6292IDGKT	VSSOP	DGK	8	250	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
MCP6292IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
MCP6294IDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
MCP6294IPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
MCP6294IPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
MCP6294IPWT	TSSOP	PW	14	250	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
MCP6291IDBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
MCP6291IDBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
MCP6291IDBVRG4	SOT-23	DBV	5	3000	210.0	185.0	35.0
MCP6291IDCKR	SC70	DCK	5	3000	208.0	191.0	35.0
MCP6292IDDFR	SOT-23-THIN	DDF	8	3000	210.0	185.0	35.0
MCP6292IDGKR	VSSOP	DGK	8	2500	356.0	356.0	36.0
MCP6292IDGKT	VSSOP	DGK	8	250	353.0	353.0	32.0
MCP6292IDR	SOIC	D	8	2500	353.0	353.0	32.0
MCP6294IDR	SOIC	D	14	2500	353.0	353.0	32.0
MCP6294IPWR	TSSOP	PW	14	2000	353.0	353.0	32.0
MCP6294IPWR	TSSOP	PW	14	2000	366.0	364.0	50.0
MCP6294IPWT	TSSOP	PW	14	250	353.0	353.0	32.0



SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.

EXAMPLE BOARD LAYOUT

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

4214839/K 08/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/K 08/2024

NOTES: (continued)

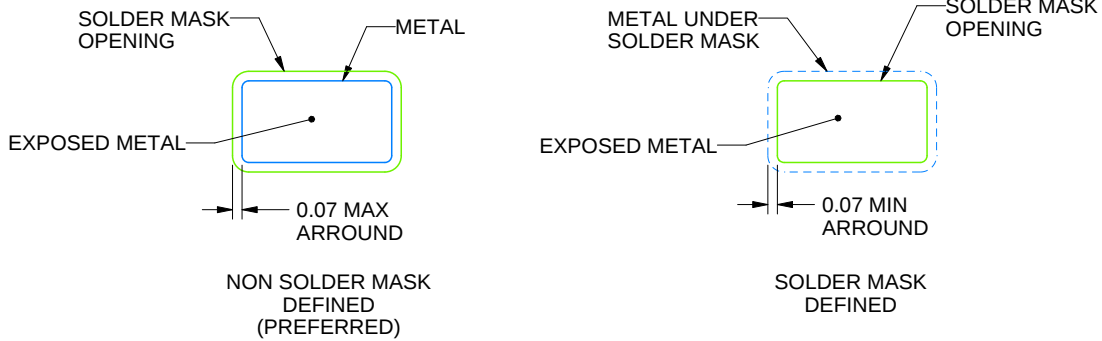
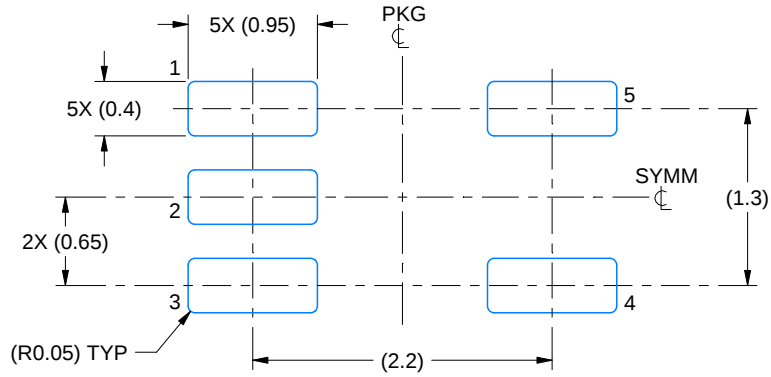
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.



4214834/G 11/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC MO-203.
4. Support pin may differ or may not be present.
5. Lead width does not comply with JEDEC.
6. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25mm per side



4214834/G 11/2024

NOTES: (continued)

7. Publication IPC-7351 may have alternate designs.
8. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:18X

4214834/G 11/2024

NOTES: (continued)

9. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
10. Board assembly site may have different recommendations for stencil design.

DGK0008A



PACKAGE OUTLINE

VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



4214862/A 04/2023

NOTES:

PowerPAD is a trademark of Texas Instruments.

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.

EXAMPLE BOARD LAYOUT

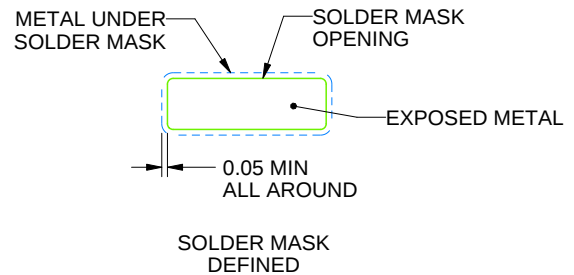
DGK0008A

TM VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X



SOLDER MASK DETAILS

4214862/A 04/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.

EXAMPLE STENCIL DESIGN

DGK0008A

TM VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
SCALE: 15X

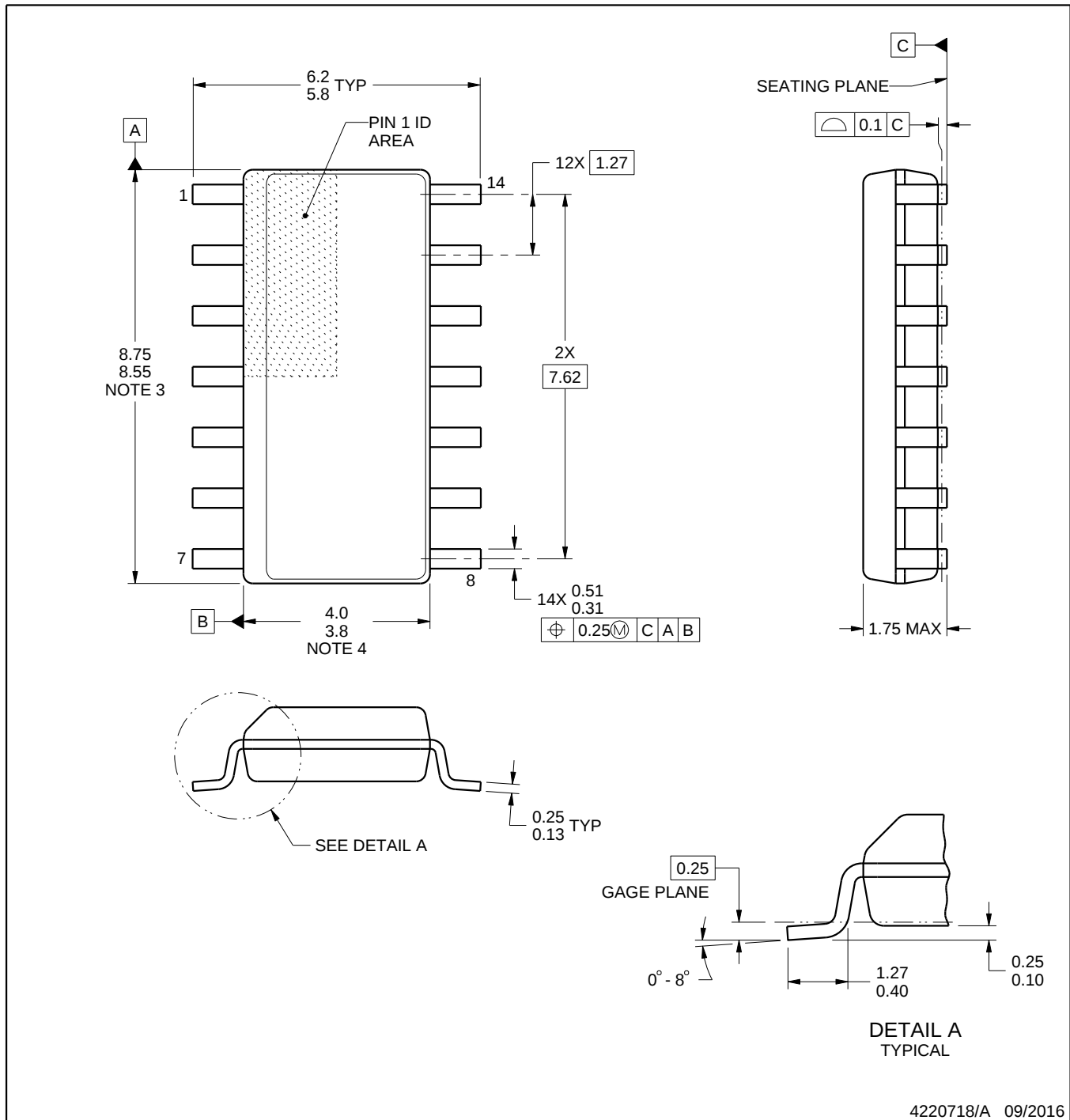
4214862/A 04/2023

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

D0014A**PACKAGE OUTLINE****SOIC - 1.75 mm max height**

SMALL OUTLINE INTEGRATED CIRCUIT



4220718/A 09/2016

NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.

EXAMPLE BOARD LAYOUT

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE
SCALE:8X



SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

4220718/A 09/2016

NOTES: (continued)

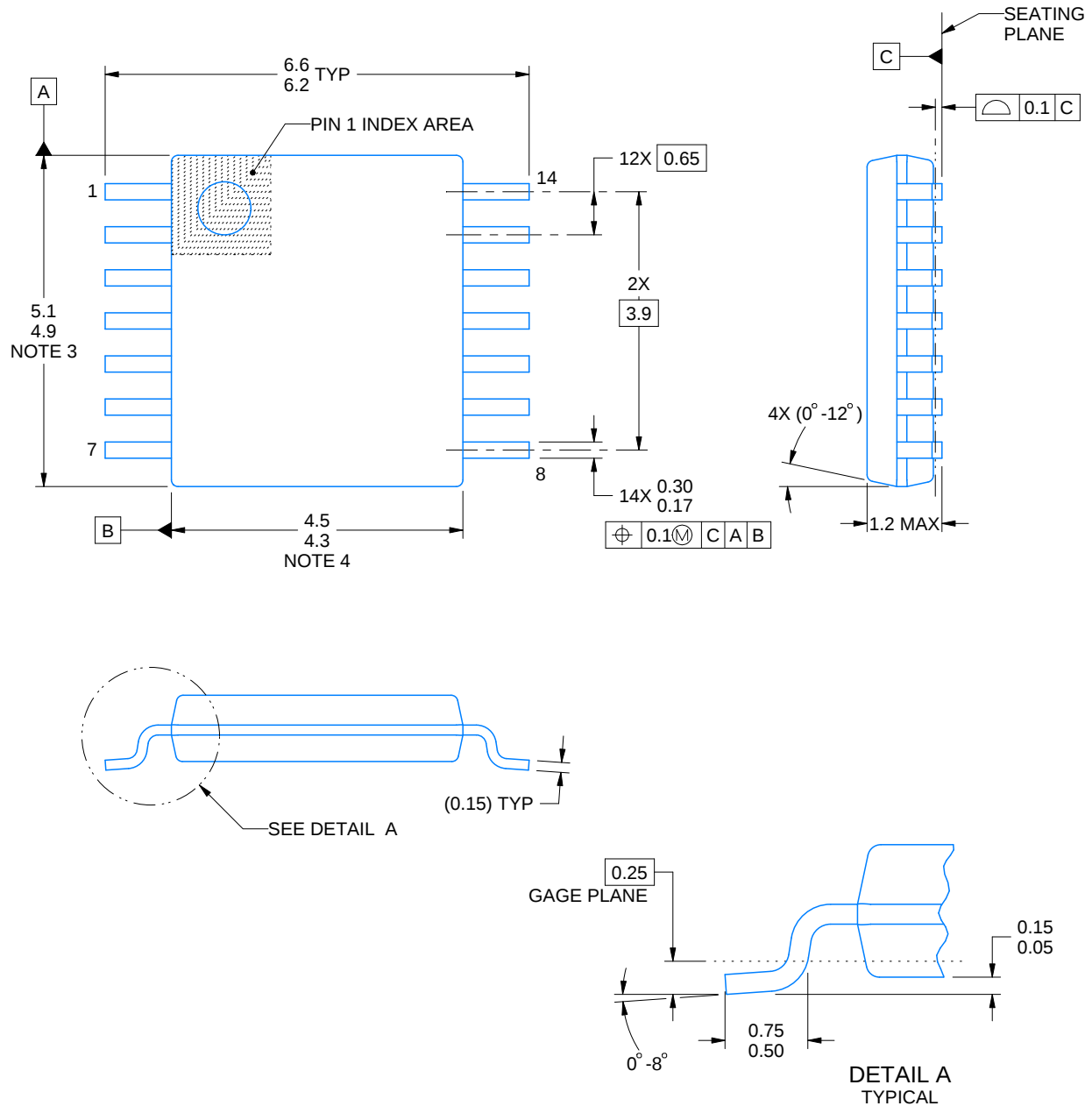
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PW0014A

PACKAGE OUTLINE

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



4220202/B 12/2023

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

EXAMPLE BOARD LAYOUT

PW0014A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



SOLDER MASK DETAILS

4220202/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0014A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220202/B 12/2023

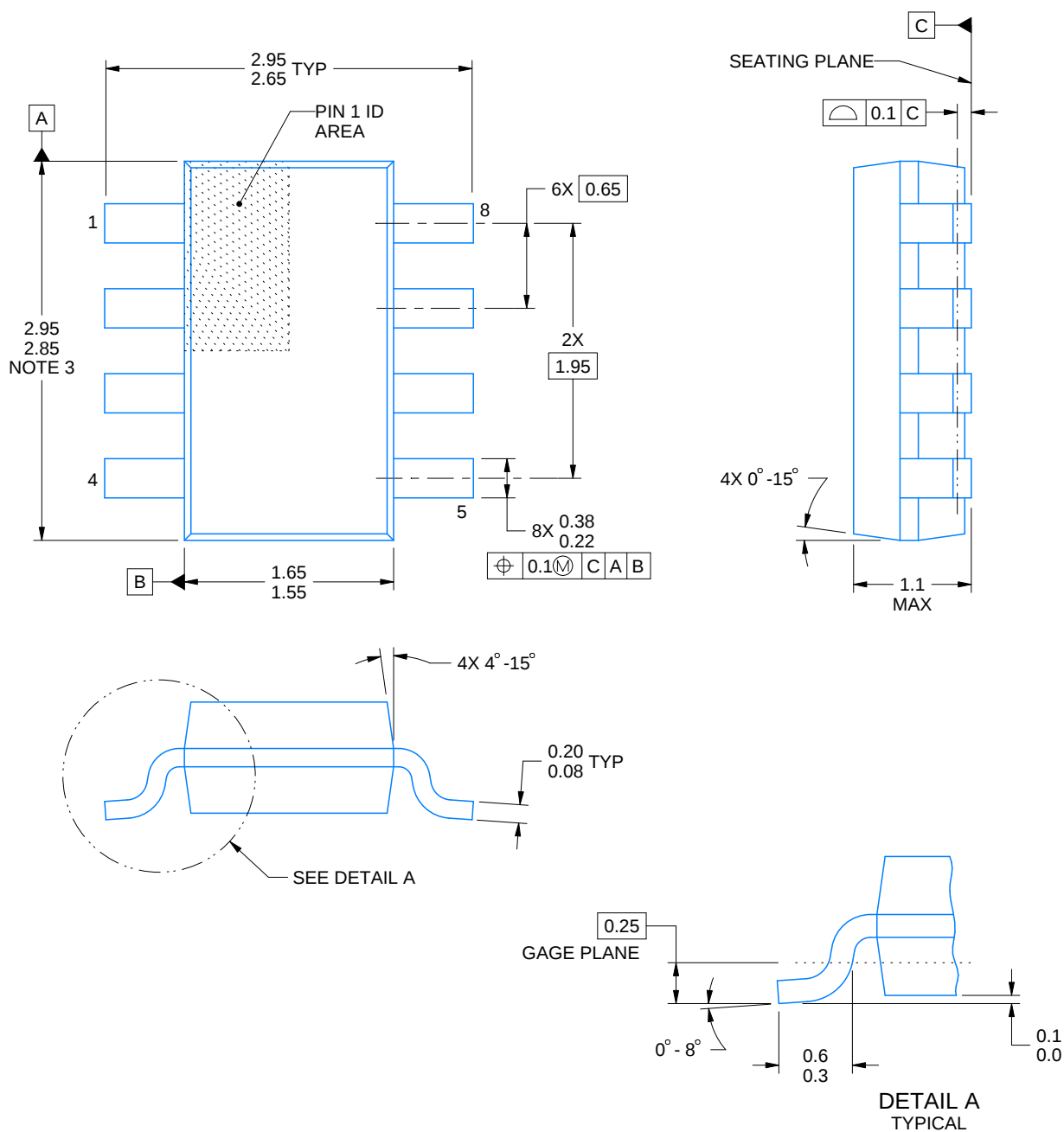
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.



SOT-23-THIN - 1.1 mm max height

PLASTIC SMALL OUTLINE



4222047/E 07/2024

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

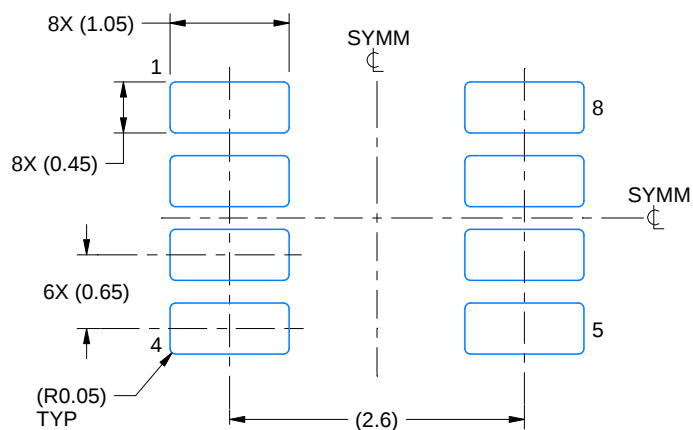
2. This drawing is subject to change without notice.

3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.

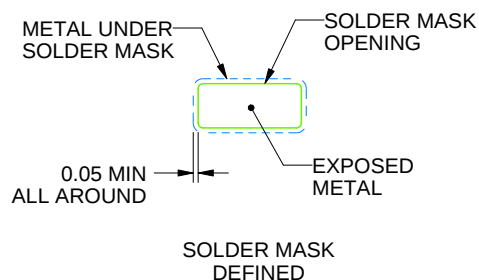
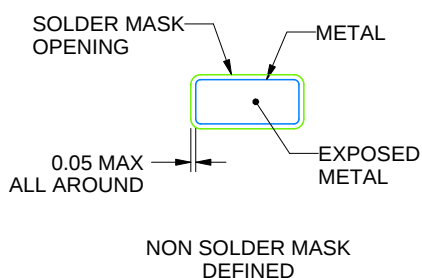
DDF0008A

SOT-23-THIN - 1.1 mm max height

PLASTIC SMALL OUTLINE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

4222047/E 07/2024

NOTES: (continued)

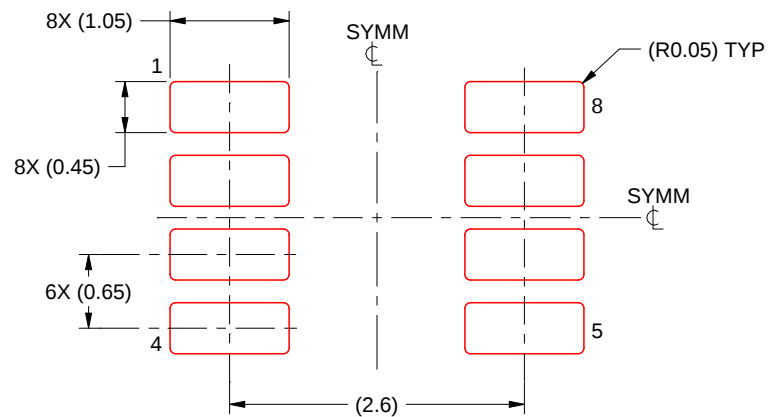
4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DDF0008A

SOT-23-THIN - 1.1 mm max height

PLASTIC SMALL OUTLINE

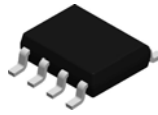


SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4222047/E 07/2024

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.

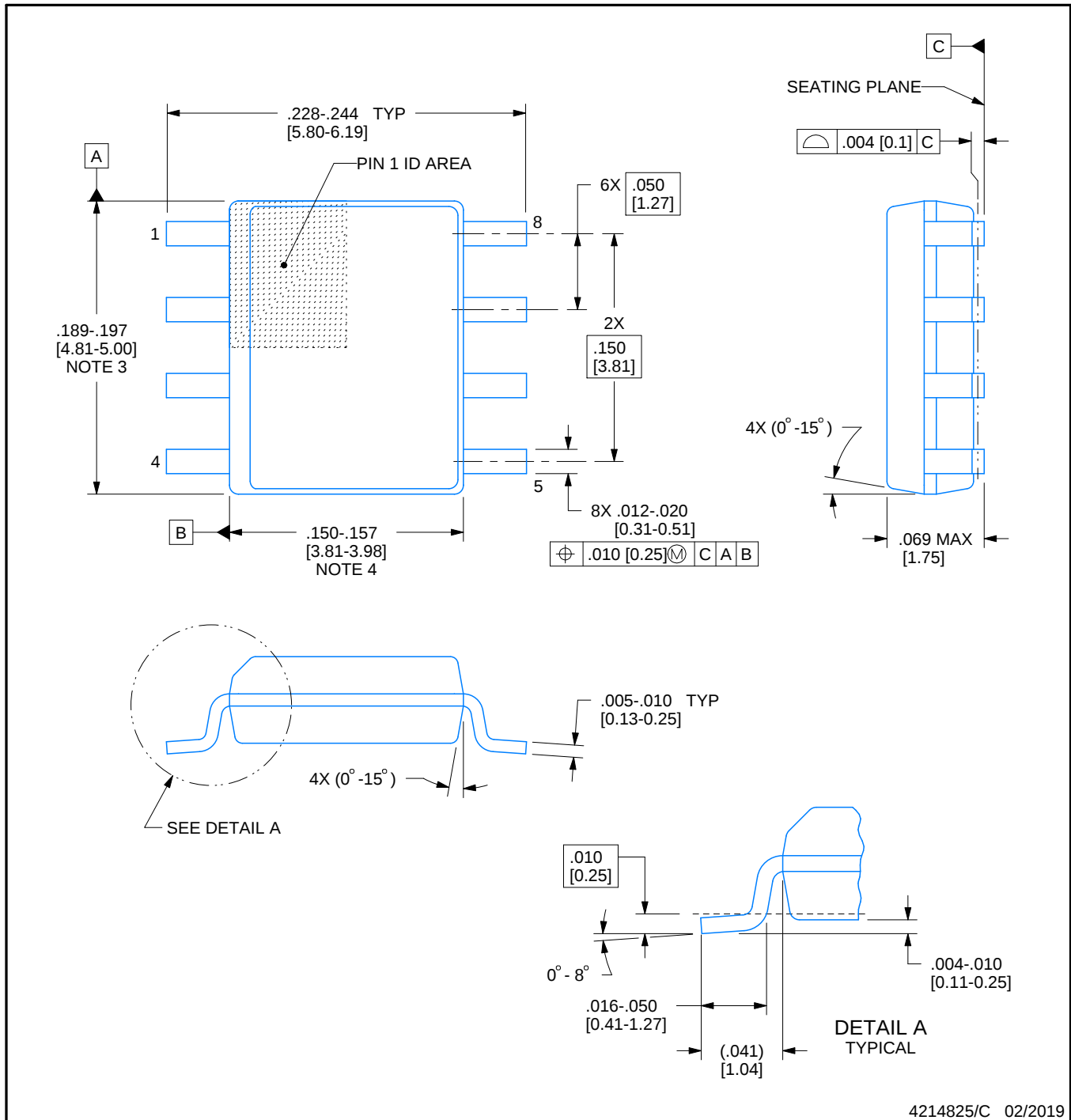


D0008A

PACKAGE OUTLINE

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



4214825/C 02/2019

NOTES:

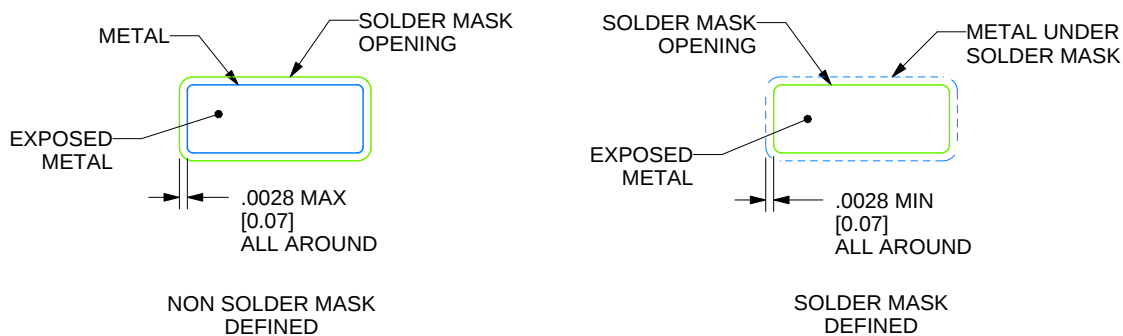
1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.

EXAMPLE BOARD LAYOUT

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



4214825/C 02/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

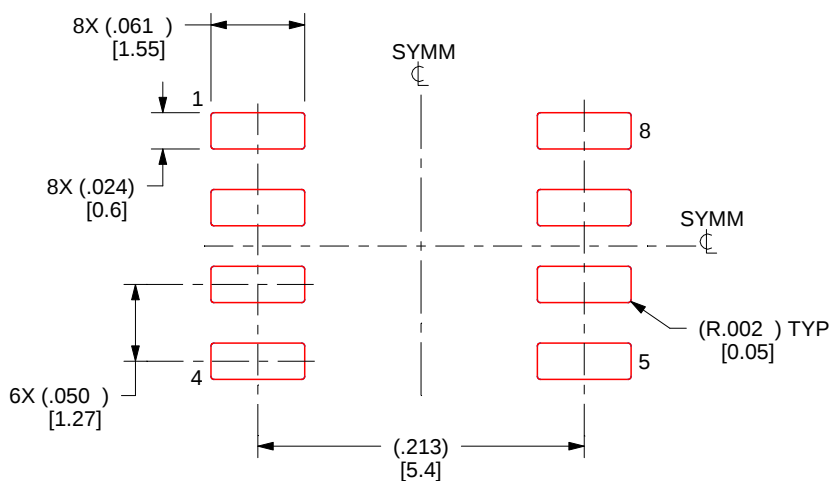
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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最終更新日：2025 年 10 月