MSP430FR231x ミクスト・シグナル・マイクロコントローラ

1 デバイスの概要

1.1 特長

- 組み込みマイクロコントローラ
  - 最高 16MHz の 16 ビット RISC アーキテクチャ
  - 3.6V～1.8V の広い電源電圧範囲 (最低電源電圧は SVS レベルにより制限されます。「SVS 仕様」を参照)
- 最適化された低消費電力モード (3V 時)
  - アクティブ・モード：126µA/MHz
  - スタンバイ：リアルタイム・クロック (RTC) カウンタ (LPM3. 5で 32768Hz の水晶発振器を使用)：0.71µA
  - シャットダウン (LPM4.5)：SVS なしで 32nA
- 高性能アナログ
  - トランスインピーダンス・アンプ (TIA) (1)
    - 電流/電圧変換
    - ハーフ・レール入力
    - 低リーク電流の負入力、最低 5pA、TSSOP16 パッケージでのみ有効
    - レール・ツー・レール出力
    - 複数の入力選択
    - 構成可能な大消費電力モードと低消費電力モード
  - 8 チャネル、10 ビットの A/D コンバータ (ADC)
    - 内蔵の 1.5V 基準電圧
    - サンプル・アンド・ホールド 200ksps
  - 拡張コンパレータ (eCOMP)
    - 基準電圧として 6 ビットのデジタル/アナログ・コンバータ (DAC) を内蔵
    - プログラマブル・ヒステリシス
    - 高消費電力モードと低消費電力モードを構成可能
  - スマート・アナログ・コンボ (SAC-L1)
    - 汎用オペアンプをサポート
    - レール・ツー・レールの入出力
    - 複数の入力選択
    - 構成可能な大消費電力モードと低消費電力モード
- 低消費電力の強誘電体 RAM (FRAM)
  - 最大 3.75KB の不揮発性メモリ
  - エラー訂正コード (ECC) 搭載
  - 書き込み保護を設定可能
  - プログラム、定数、ストレージの統合メモリ
  - 書き込みサイクルの耐久性：10^{15} 回
  - 放射線耐性、非磁性
- インテリジェントなデジタル・ペリフェラル
  - IR 変調ロジック
  - 3 つのキャプチャ / 比較レジスタを搭載した 16 ビット・タイマ (Timer_B3) × 2
  - 16 ビットのカウンタ専用 RTC × 1
  - 16 ビットの巡回冗長性検査 (CRC)
- 拡張シリアル通信
  - 拡張 USCI A (eUSCI_A) により UART、IrDA、SPI をサポート
  - 拡張 USCI B (eUSCI_B) により SPI および I^2C をサポート、リマップ機能をサポート(「信号概要」を参照)
- クロック・システム (CS)
  - オンチップの 32kHz RC 発振器 (REFO)
  - オンチップの 16MHz デジタル制御発振器 (DCO)、周波数ロック・ループ (FLL) 付き
    - オンチップの基準電圧は室温で ±1% 精度
  - オンチップの超低周波数 10kHz 発振器 (VLO)
  - オンチップの高周波数変調発振器 (MODOSC)
  - 外付けの 32kHz 水晶発振器 (LFXT)
  - 最大 16 MHz の外付けの高周波数水晶発振器 (HFXT)
  - 1～128 の MCLK プリスケーラをプログラム可能
  - 1、2、4、8 のプログラマブル・プリスケーラを使って MCLK から SMCLK を生成
- 汎用入出力およびピン機能
  - 20 ピンのパッケージに 16 の I/O を搭載
  - 12 本の割り込みピン (P1 に 8 ピン、P2 に 4 ピン) により、MCU を LPM からウェイクアップ可能
  - すべての I/O で静電容量式タッチ機能をサポート
- 開発ツールとソフトウェア
  - LaunchPad™開発キット (MSP-EXP430FR2311)
  - ターゲット開発ボード (MSP-TS430PW20)
- ファミリ・メンバー (「デバイスの比較」も参照)
  - MSP430FR2311：3.75KB のプログラム FRAM と 1KB の RAM
  - MSP430FR2310：2KB のプログラム FRAM と 1KB の RAM

(1) トランスインピーダンス・アンプについては、当初はTRIという略語を説明文、ピン名、およびレジスタ名で使用することとしました。説明文では全面的にこの略語をTIAに変更しましたが、ピン名およびレジスタ名では引き続きTRIを使用しています。

英語版のTI製品についての情報を翻訳したこの資料は、製品の概要を確認する目的で便宜的に提供しているものです。該当する正式な英語版の最新情報は、www.ti.comで閲覧でき、その内容が常に優先されます。TIでは翻訳の正確性および妥当性につきましては一切保証いたしません。実際の設計などの前には、必ず最新版の英語版をご参照くださいますようお願いいたします。

- パッケージ・オプション
  - 20 ピン TSSOP (PW20)
  - 16 ピン TSSOP (PW16)
  - 16 ピン VQFN (RGY16)

1.2 アプリケーション

- 煙感知器
- 外付けバッテリ
- ポータブル健康管理およびフィットネス
- 電力監視
- パーソナル・エレクトロニクス

1.3 概要

MSP430FR231x FRAMマイクロコントローラ(MCU)は、MSP430™MCUバリュー・ライン・センシング・ファミリの製品であり、リーク電流の小さいトランスインピーダンス・アンプ(TIA)と汎用オペアンプを内蔵しています。このMCUには強力な16ビットRISC CPU、16ビット・レジスタ、および定数ジェネレータが搭載されているため、最高水準のコード効率を実現できます。また、デジタル制御発振器(DCO)により、低消費電力モードからアクティブ・モードへ通常10µs未満でウェイクアップできます。このMCUの各種機能は、煙感知器からポータブル健康管理/フィットネス・アクセサリまで、幅広い用途に最適です。

超低消費電力のMSP430FR231x MCUファミリは複数のデバイスからなり、組み込み型の不揮発性FRAMや、さまざまなセンシングおよび測定機器に対応する多様なペリフェラル・セットを特長としています。アーキテクチャ、FRAM、ペリフェラルに多様な低消費電力モードを組み合わせ、携帯型/ワイヤレス・センシング機器で長いバッテリ駆動時間を実現するように最適化しています。FRAMは、SRAMの速度、柔軟性、耐久性とフラッシュの安定性および信頼性を両立しながら総消費電力を抑制できる不揮発性メモリ・テクノロジです。

MSP430FR231x MCUは、ハードウェアおよびソフトウェアの大規模なエコシステムによってサポートされており、リファレンス・デザインやサンプル・コードを利用して設計をすぐに開始できます。開発キットにはMSP-EXP430FR2311 LaunchPad™開発キットと、MSP-TS430PW20 20ピン・ターゲット開発ボードが含まれます。また、TIは無償の MSP430Ware™ソフトウェアも提供しており、Code Composer Studio™ IDEデスクトップのコンポーネントとして利用できます。TI Resource Explorerではクラウド・バージョンも利用可能です。MSP430 MCUには、幅広い範囲のオンライン資料、トレーニング、および E2E™コミュニティ・フォーラムによるオンライン・サポートも用意されています。

モジュールの詳細な説明については、*『MSP430FR4xx and MSP430FR2xx Family User's Guide』* (英語) を参照してください。

製品情報(1)

型番	パッケージ	本体サイズ(2)
MSP430FR2311IPW20	TSSOP (20)	6.5mm×4.4mm
MSP430FR2310IPW20		
MSP430FR2311IPW16	TSSOP (16)	5mm×4.4mm
MSP430FR2310IPW16		
MSP430FR2311IRGY	VQFN (16)	4mm×3.5mm
MSP430FR2310IRGY		

(1) 最新の製品、パッケージ、および注文情報については、9の「*付録:パッケージ・オプション*」、またはwww.ti.comのTI Webサイトを参照してください。
(2) ここに記載されているサイズは概略です。許容公差を含めたパッケージの寸法については、9の「*メカニカル・データ*」を参照してください。

注意

電気的な過剰ストレスや、データやコード・メモリの不安定化を防止するため、デバイス・レベルのESD仕様に従って、システム・レベルのESD保護を適用する必要があります。詳細については、*『MSP430™のシステム・レベルのESD考慮事項』*を参照してください。

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1.4 機能ブロック図

図 1-1に機能ブロック図を表します。

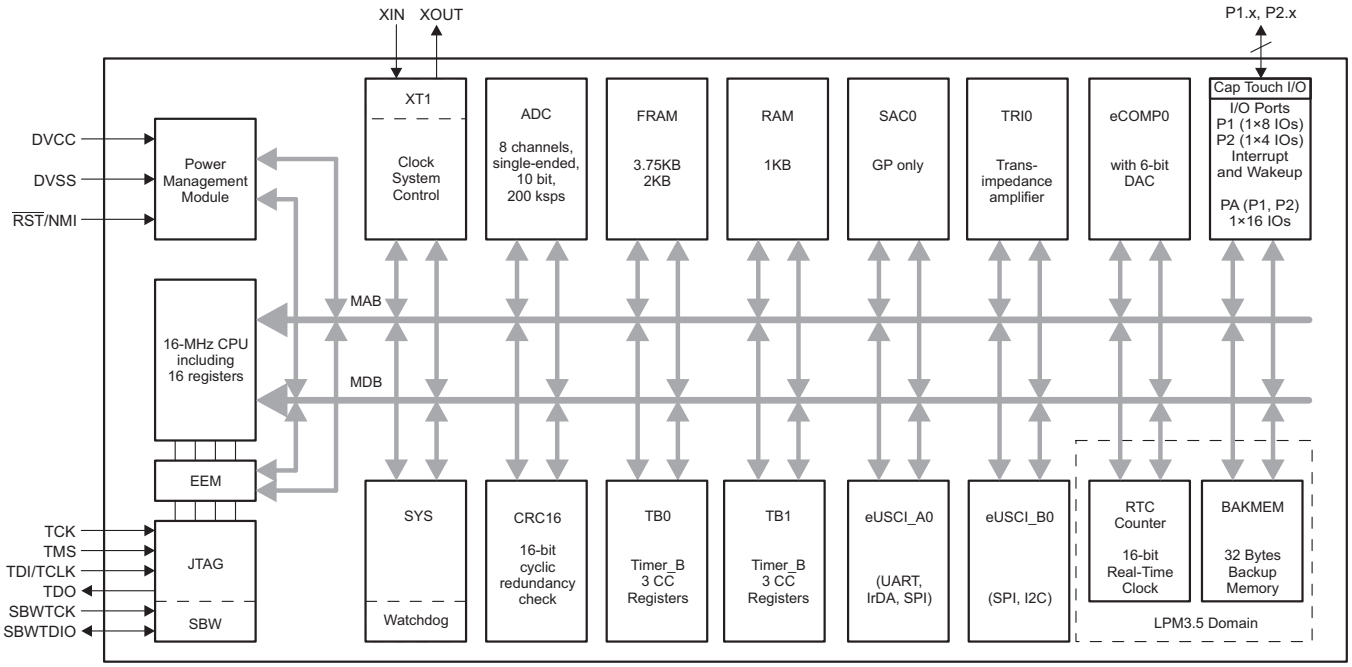


図 1-1. MSP430FR231x の機能ブロック図

- このMCUには、DVCCおよびDVSSの1つのメイン電源ペアがあり、デジタルとアナログの両方のモジュールへ電力を供給します。バイパスおよびデカップリング・コンデンサとしては、それぞれ4.7µF～10µFおよび0.1µFで、精度±5%が推奨されます。
- P1の8本すべてのピンと、P2の4本のピンにはピン割り込み機能があり、LPM4、LPM3.5、LPM4.5を含むすべてのLPMからMCUをウェイクアップできます。
- 各Timer_B3には3つのキャプチャ/比較レジスタがあります。外部的に接続されているのはCCR1およびCCR2のみです。CCR0レジスタは、内部的な期間のタイミングと割り込みの生成にのみ使用できます。
- LPM3.5では、RTCカウンタとバックアップ・メモリが動作し、他のペリフェラルはオフです。
- すべての汎用I/Oは、静電容量式タッチI/Oとして構成可能です。

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2 改訂履歴

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

リビジョン D からリビジョン E への変更点

2018年8月29日発行分から2019年12月9日発行分への変更 **Page**

- Updated Section 3.1, *Related Products* 7
- Changed the note that begins "Supply voltage changes faster than 0.2 V/µs can trigger a BOR reset..." in Section 5.3, *Recommended Operating Conditions* 15
- Added the note that begins "TI recommends that power to the DVCC pin must not exceed the limits..." in Section 5.3, *Recommended Operating Conditions* 15
- Changed the note that begins "A capacitor tolerance of ±20% or better is required..." in Section 5.3, *Recommended Operating Conditions* 15
- Combined former sections 5.8 and 5.10 to Section 5.9, *Production Distribution of LPM Supply Currents* 19
- Corrected "SVS Enabled" test condition on Figure 5-2, *LPM3.5 Supply Current vs Temperature* 19
- Added the note "See *MSP430 32-kHz Crystal Oscillators* for details on crystal section, layout, and testing" to Table 5-3, *XT1 Crystal Oscillator (Low Frequency)* 23
- Changed the note that begins "Requires external capacitors at both terminals..." in Table 5-3, *XT1 Crystal Oscillator (Low Frequency)* 23
- Added the $t_{TB,cap}$ parameter in Table 5-13, *Timer_B* 30
- Changed the parameter symbol from R_I to $R_{I,MUX}$ in Table 5-20, *ADC, Power Supply and Input Range Conditions* 36
- Corrected the test conditions for the $R_{I,MUX}$ parameter in Table 5-20, *ADC, Power Supply and Input Range Conditions* 36
- Added $R_{I,Misc}$ TYP value of 34 kΩ in Table 5-20, *ADC, Power Supply and Input Range Conditions* 36
- Added formula for R_I in Table 5-21, *ADC, 10-Bit Timing Parameters* 36
- Added the note that begins "$t_{Sample} = \ln(2^{n+1}) \times \tau$ ..." in Table 5-21, *ADC, 10-Bit Timing Parameters* 36
- Corrected bitfield from RTCCLK to RTCCKSEL in Table 6-8, *Clock Distribution* 51
- Corrected bitfield from IRDSEL to IRDSSEL in Section 6.11.8, *Timers (Timer0_B3, Timer1_B3)* , in the description that starts "The interconnection of Timer0_B3 and ..." 54
- Added P1SELC information in Table 6-31, *Port P1, P2 Registers (Base Address: 0200h)* 65
- Added P2SELC information in Table 6-31, *Port P1, P2 Registers (Base Address: 0200h)* 65
- Added note to "ADC calibration" in Table 6-46, *Device Descriptors* 72

リビジョン C からリビジョン D への変更点

2017年9月12日発行分から2018年08月28日発行分への変更 **Page**

- Updated Section 3.1, *Related Products* 7
- Combined former sections 5.8 and 5.10 to Section 5.9, *Production Distribution of LPM Supply Currents* 19
- Added note to V_{SVSH-} and V_{SVSH+} parameters in Table 5-1, *PMM, SVS and BOR* 21
- Added the $t_{TB,cap}$ parameter in Table 5-13, *Timer_B* 30
- Corrected ADCINCHx column heading in Table 6-16, *ADC Channel Connections* 58
- 8.2「*デバイスの項目表記*」のテキストおよび図を更新 79

リビジョン B からリビジョン C への変更点

2016年6月1日発行分から2017年09月11日発行分への変更 **Page**

- 特長の項目「シャットダウン (LPM4.5)」の電流を訂正 1
- テスト・データに基づき低リーク電流入力を 50pA から 5pA に改善 1
- Added Section 3.1, *Related Products* 7
- Combined former sections 5.8 and 5.10 to Section 5.9, *Production Distribution of LPM Supply Currents* 19
- Added the $t_{TB,cap}$ parameter in Table 5-13, *Timer_B* 30
- Removed ADCDIV from the formula for the TYP value in the second row of the $t_{CONVERT}$ parameter in Table 5-21, *ADC, 10-Bit Timing Parameters* (removed because ADCCLK is after division) 36
- Changed the entries for eUSCI_A0 and eUSCI_B0 in the LPM3 column from Off to Optional in Table 6-1,

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Operating Modes 45
- Added the sentence that begins "This device supports blank device detection..." in Section 6.6, *Bootloader (BSL)* 47
- Added the note "Controlled by the RTCCLK bit in the SYSCFG2 register" on Table 6-8, *Clock Distribution* 51
- Added Figure 6-1, *Clock Distribution Block Diagram* 51
- Added Figure 6-2, *Timer_B Connections* 55
- Removed SYSBERRIV register (not supported) in Table 6-26, *SYS Registers* 64
- Changed from "If the $\overline{\text{RST}}$/NMI pin is unused...with a 2.2-nF pulldown capacitor" to "If the $\overline{\text{RST}}$/NMI pin is unused...with a 10-nF pulldown capacitor" 76

リビジョン A からリビジョン B への変更点

2016年3月30日発行分から2016年05月31日発行分への変更 **Page**

- デバイスのステータスを「製品プレビュー」から「量産データ」に変更 1
- Changed the value of f_{XT1} in the table note that starts "Low-power mode 4, VLO,..." 17
- Combined former sections 5.8 and 5.10 to Section 5.9, *Production Distribution of LPM Supply Currents* 19
- Added Test Conditions to module Timer_B in Section 5.10, *Typical Characteristics – Current Consumption Per Module* 20
- Added "16 MHz" to the parameter description of $t_{FLL,\ lock}$ in Table 5-5, *DCO FLL* 25
- Added the $t_{TB,cap}$ parameter in Table 5-13, *Timer_B* 30
- Removed ±3°C from calibration temperatures in the table note that starts "The device descriptor structure contains calibration values..." 37
- Changed the unit on the E_{NI} parameter in Table 5-24, *SAC0 (SAC-L1, OA)* 39
- Changed the unit on the E_{NI} parameter in Table 5-25, *TIA0* 40

初版からリビジョン A への変更点

2016年2月23日発行分から2016年03月29日発行分への変更 **Page**

- ドキュメント全体で、TIAモジュールの名称をTRI0からTIA0に変更 3
- Changed TYP values for the $I_{AM,\ FRAM}$(0%) parameter in Section 5.4, *Active Mode Supply Current Into V_{CC} Excluding External Current* 16
- Combined former sections 5.8 and 5.10 to Section 5.9, *Production Distribution of LPM Supply Currents* 19
- Added the $t_{TB,cap}$ parameter in Table 5-13, *Timer_B* 30
- Changed MAX values of the $t_{VALID,SO}$ parameter in Table 5-18, *eUSCI (SPI Slave Mode) Switching Characteristics* 33
- Changed the TYP value of the CMRR parameter with Test Conditions of "TRIPM = 0" from 70 dB to 80 dB in Table 5-25, *TIA0* 40
- Changed the TYP value of the PSRR parameter with Test Conditions of "TRIPM = 0" from 70 dB to 80 dB in Table 5-25, *TIA0* 40
- 以前の「*開発ツールのサポート*」セクションを、8.3「ツールとソフトウェア」に置き換え 80

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3 Device Comparison

Table 3-1 summarizes the features of the available family members.

Table 3-1. Device Comparison(1) (2)

DEVICE	PROGRAM FRAM (KB)	SRAM (Bytes)	TB0, TB1	eUSCI_A	eUSCI_B	10-BIT ADC CHANNELS	SAC0 (OA)	TIA0	eCOMP0	I/O	PACKAGE
MSP430FR2311IPW20	3.75	1024	3 CCR(3)	1	1	8	1	1	1	16	20 PW (TSSOP)
MSP430FR2310IPW20	2	1024	3 CCR(3)	1	1	8	1	1	1	16	20 PW (TSSOP)
MSP430FR2311IPW16	3.75	1024	3 CCR(3)(4)	1	1	8	1	1	1	11	16 PW (TSSOP)
MSP430FR2310IPW16	2	1024	3 CCR(3)(4)	1	1	8	1	1	1	11	16 PW (TSSOP)
MSP430FR2311IRGY	3.75	1024	3 CCR(3)	1	1	8	1	1	1	12	16 RGY (VQFN)
MSP430FR2310IRGY	2	1024	3 CCR(3)	1	1	8	1	1	1	12	16 RGY (VQFN)

(1) For the most current device, package, and ordering information, see the *Package Option Addendum* in 9, or see the TI website at www.ti.com.
(2) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/packaging.
(3) A CCR register is a configurable register that provides internal and external capture or compare inputs, or internal and external PWM outputs.
(4) TB1 provides only one external connection (TB1.1) on this package.

3.1 Related Products

For information about other devices in this family of products or related products, see the following links.

TI 16-bit and 32-bit microcontrollers

High-performance, low-power solutions to enable the autonomous future

Products for MSP430 ultra-low-power sensing & measurement MCUs

One platform. One ecosystem. Endless possibilities.

Companion products for MSP430FR2311

Review products that are frequently purchased or used with this product.

Reference designs for MSP430FR2311

Find reference designs leveraging the best in TI technology – from analog and power management to embedded processors

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4 Terminal Configuration and Functions

4.1 Pin Diagrams

Figure 4-1 shows the pinout of the 20-pin PW package.

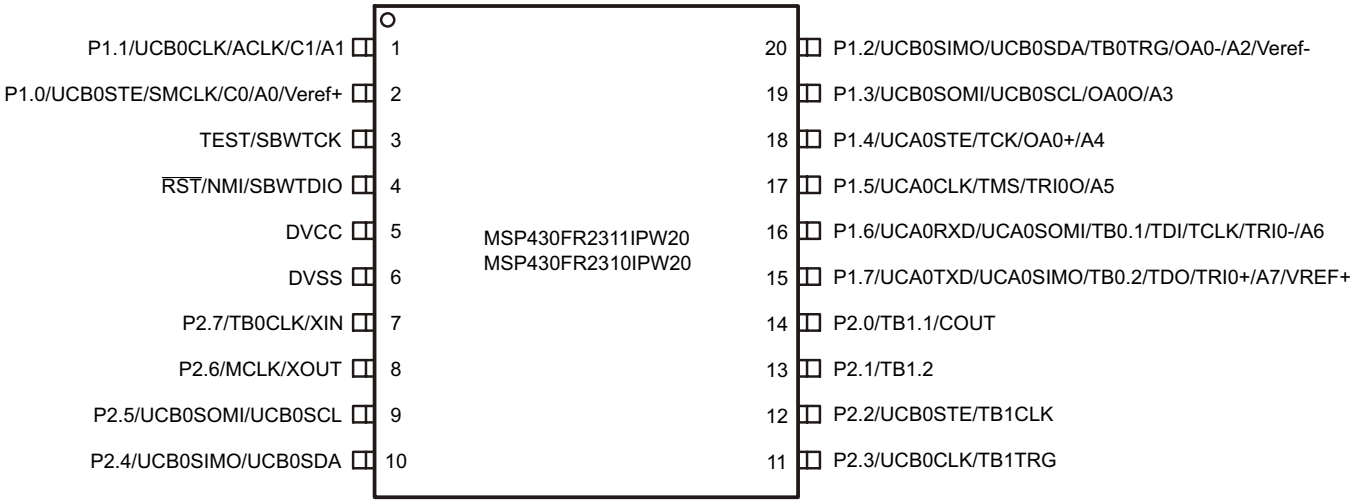


Figure 4-1. 20-Pin PW (TSSOP) (Top View)

Figure 4-2 shows the pinout of the 16-pin PW package.

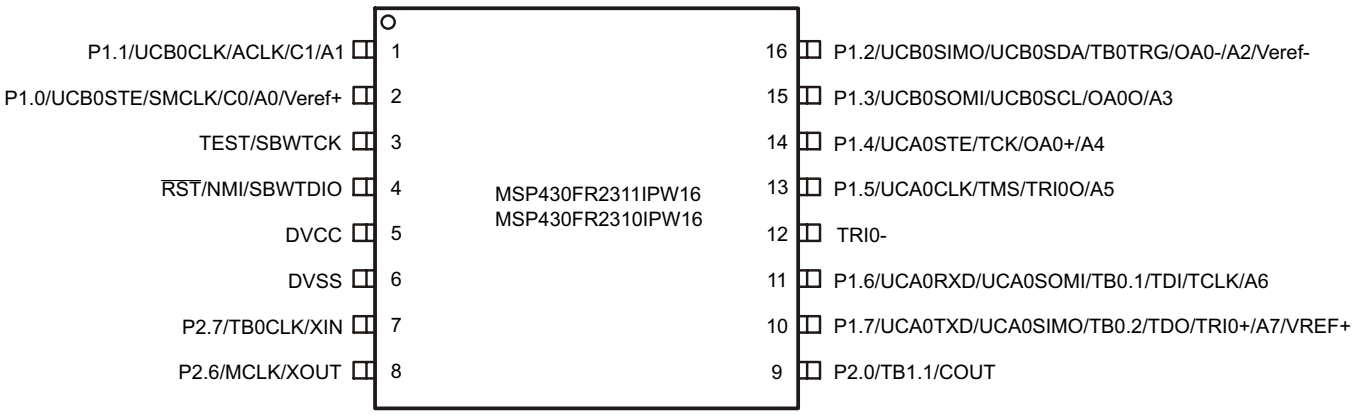


Figure 4-2. 16-Pin PW (TSSOP) (Top View)

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Figure 4-3 shows the pinout of the 16-pin RGY package.

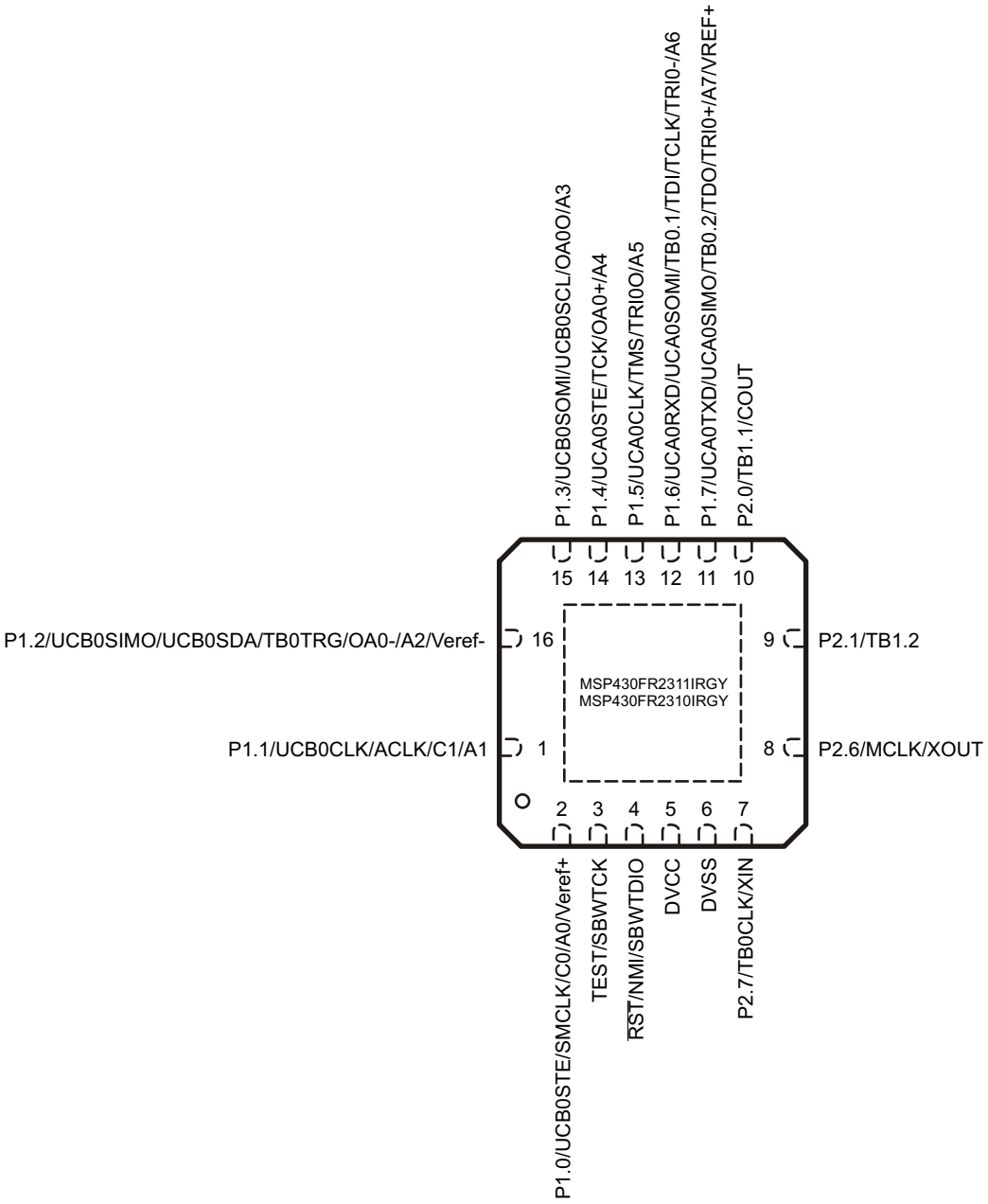


Figure 4-3. 16-Pin RGY (VQFN) (Top View)

4.2 Pin Attributes

Table 4-1 lists the attributes of all pins.

Table 4-1. Pin Attributes

PIN NUMBER			SIGNAL NAME(1) (2)	SIGNAL TYPE(3)	BUFFER TYPE(4)	POWER SOURCE	RESET STATE AFTER BOR(5)
PW20	RGY	PW16					
1	1	1	P1.1 (RD)	I/O	LVCMOS	DVCC	OFF
			UCB0CLK	I/O	LVCMOS	DVCC	N/A
			ACLK	O	LVCMOS	DVCC	N/A
			C1	I	Analog	DVCC	N/A
			A1	I	Analog	DVCC	N/A
2	2	2	P1.0 (RD)	I/O	LVCMOS	DVCC	OFF
			UCB0STE	I/O	LVCMOS	DVCC	N/A
			SMCLK	O	LVCMOS	DVCC	N/A
			C0	I	Analog	DVCC	N/A
			A0	I	Analog	DVCC	N/A
			Veref+	I	Power	DVCC	N/A
3	3	3	TEST (RD)	I	LVCMOS	DVCC	OFF
			SBWTCK	I	LVCMOS	DVCC	N/A
4	4	4	$\overline{\text{RST}}$ (RD)	I/O	LVCMOS	DVCC	OFF
			NMI	I	LVCMOS	DVCC	N/A
			SBWTDIO	I/O	LVCMOS	DVCC	N/A
5	5	5	DVCC	P	Power	DVCC	N/A
6	6	6	DVSS	P	Power	DVCC	N/A
7	7	7	P2.7 (RD)	I/O	LVCMOS	DVCC	OFF
			TB0CLK	I	LVCMOS	DVCC	N/A
			XIN	I	LVCMOS	DVCC	N/A
8	8	8	P2.6 (RD)	I/O	LVCMOS	DVCC	OFF
			MCLK	O	LVCMOS	DVCC	N/A
			XOUT	O	LVCMOS	DVCC	N/A
9	–	–	P2.5 (RD)	I/O	LVCMOS	DVCC	OFF
			UCB0SOMI	I/O	LVCMOS	DVCC	N/A
			UCB0SCL	I/O	LVCMOS	DVCC	N/A
10	–	–	P2.4 (RD)	I/O	LVCMOS	DVCC	OFF
			UCB0SIMO	I/O	LVCMOS	DVCC	N/A
			UCB0SDA	I/O	LVCMOS	DVCC	N/A
11	–	–	P2.3 (RD)	I/O	LVCMOS	DVCC	OFF
			UCB0CLK	I/O	LVCMOS	DVCC	N/A
			TB1TRG	I	LVCMOS	DVCC	N/A
12	–	–	P2.2 (RD)	I/O	LVCMOS	DVCC	OFF
			UCB0STE	I/O	LVCMOS	DVCC	N/A
			TB1CLK	I	LVCMOS	DVCC	N/A
13	9	–	P2.1(RD)	I/O	LVCMOS	DVCC	OFF
			TB1.2	I/O	LVCMOS	DVCC	N/A

(1) Signals names with (RD) denote the reset default pin name.
(2) To determine the pin mux encodings for each pin, see Section 6.12, *Input/Output Diagrams*.
(3) Signal Types: I = Input, O = Output, I/O = Input or Output.
(4) Buffer Types: LVCMOS, Analog, or Power
(5) Reset States:
OFF = High-impedance input with pullup or pulldown disabled (if available)
N/A = Not applicable

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Table 4-1. Pin Attributes (continued)

PIN NUMBER			SIGNAL NAME[1] [2]	SIGNAL TYPE[3]	BUFFER TYPE[4]	POWER SOURCE	RESET STATE AFTER BOR[5]
PW20	RGY	PW16					
14	10	9	P2.0 (RD)	I/O	LVCMOS	DVCC	OFF
			TB1.1	I/O	LVCMOS	DVCC	N/A
			COUT	O	LVCMOS	DVCC	N/A
15	11	10	P1.7 (RD)	I/O	LVCMOS	DVCC	OFF
			UCA0TXD	O	LVCMOS	DVCC	N/A
			UCA0SIMO	I/O	LVCMOS	DVCC	N/A
			TB0.2	I/O	LVCMOS	DVCC	N/A
			TDO	O	LVCMOS	DVCC	N/A
			TRI0+	I	Analog	DVCC	N/A
			A7	I	Analog	DVCC	N/A
			VREF+	O	Power	DVCC	N/A
16	12	11	P1.6 (RD)	I/O	LVCMOS	DVCC	OFF
			UCA0RXD	I	LVCMOS	DVCC	N/A
			UCA0SOMI	I/O	LVCMOS	DVCC	N/A
			TB0.1	I/O	LVCMOS	DVCC	N/A
			TDI	I	LVCMOS	DVCC	N/A
			TCLK	I	LVCMOS	DVCC	N/A
			TRI0-[6]	I	Analog	DVCC	N/A
			A6	I	Analog	DVCC	N/A
–	–	12	TRI0-	I	Analog	DVCC	N/A
17	13	13	P1.5 (RD)	I/O	LVCMOS	DVCC	OFF
			UCA0CLK	I/O	LVCMOS	DVCC	N/A
			TMS	I	LVCMOS	DVCC	N/A
			TRI0O	O	Analog	DVCC	N/A
			A5	I	Analog	DVCC	N/A
18	14	14	P1.4 (RD)	I/O	LVCMOS	DVCC	OFF
			UCA0STE	I/O	LVCMOS	DVCC	N/A
			TCK	I	LVCMOS	DVCC	N/A
			OA0+	I	Analog	DVCC	N/A
			A4	I	Analog	DVCC	N/A
19	15	15	P1.3 (RD)	I/O	LVCMOS	DVCC	OFF
			UCB0SOMI	I/O	LVCMOS	DVCC	N/A
			UCB0SCL	I/O	LVCMOS	DVCC	N/A
			OA0O	O	Analog	DVCC	N/A
			A3	I	Analog	DVCC	N/A
20	16	16	P1.2 (RD)	I/O	LVCMOS	DVCC	OFF
			UCB0SIMO	I/O	LVCMOS	DVCC	N/A
			UCB0SDA	I/O	LVCMOS	DVCC	N/A
			TB0TRG	I	LVCMOS	DVCC	N/A
			OA0-	I	Analog	DVCC	N/A
			A2	I	Analog	DVCC	N/A
			Veref-	I	Power	DVCC	N/A

(6) Not available on TSSOP-16 package

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4.3 Signal Descriptions

Table 4-2 describes the signals for all device variants and package options.

Table 4-2. Signal Descriptions

FUNCTION	SIGNAL NAME	PIN NUMBER			PIN TYPE	DESCRIPTION
		PW20	RGY	PW16		
ADC	A0	2	2	2	I	Analog input A0
	A1	1	1	1	I	Analog input A1
	A2	20	16	16	I	Analog input A2
	A3	19	15	15	I	Analog input A3
	A4	18	14	14	I	Analog input A4
	A5	17	13	13	I	Analog input A5
	A6	16	12	11	I	Analog input A6
	A7	15	11	10	I	Analog input A7
	Veref+	2	2	2	I	ADC positive reference
	Veref-	20	16	16	I	ADC negative reference
eCOMP0	C0	2	2	2	I	Comparator input channel C0
	C1	1	1	1	I	Comparator input channel C1
	COUT	14	10	9	O	Comparator output channel COUT
TIA0	TRI0+	15	11	10	I	TIA0 positive input
	TRI0-	16	12	12	I	TIA0 negative input
	TRI0O	17	13	13	O	TIA0 output
SAC0	OA0+	18	14	14	I	SAC0, OA positive input
	OA0-	20	16	16	I	SAC0, OA negative input
	OA0O	19	15	15	O	SAC0, OA output
Clock	ACLK	1	1	1	O	ACLK output
	MCLK	8	8	8	O	MCLK output
	SMCLK	2	2	2	O	SMCLK output
	XIN	7	7	7	I	Input terminal for crystal oscillator
	XOUT	8	8	8	O	Output terminal for crystal oscillator
Debug	SBWTCK	3	3	3	I	Spy-Bi-Wire input clock
	SBWTDIO	4	4	4	I/O	Spy-Bi-Wire data input/output
	TCK	18	14	14	I	Test clock
	TCLK	16	12	11	I	Test clock input
	TDI	16	12	11	I	Test data input
	TDO	15	11	10	O	Test data output
	TMS	17	13	13	I	Test mode select
	TEST	3	3	3	I	Test Mode pin – selected digital I/O on JTAG pins
System	NMI	4	4	4	I	Nonmaskable interrupt input
	$\overline{\text{RST}}$	4	4	4	I/O	Reset input, active-low
Power	DVCC	5	5	5	P	Power supply
	DVSS	6	6	6	P	Power ground
	VREF+	15	11	10	P	Output of positive reference voltage with ground as reference

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Table 4-2. Signal Descriptions (continued)

FUNCTION	SIGNAL NAME	PIN NUMBER			PIN TYPE	DESCRIPTION
		PW20	RGY	PW16		
GPIO	P1.1	1	1	1	I/O	General-purpose I/O
	P1.2	20	16	16	I/O	General-purpose I/O
	P1.3	19	12	15	I/O	General-purpose I/O
	P1.4	18	14	14	I/O	General-purpose I/O (1)
	P1.5	17	13	13	I/O	General-purpose I/O (1)
	P1.6	16	12	11	I/O	General-purpose I/O(1)
	P1.7	15	11	10	I/O	General-purpose I/O(1)
	P2.0	14	10	9	I/O	General-purpose I/O
	P2.1	13	9	–	I/O	General-purpose I/O
	P2.2	12	–	–	I/O	General-purpose I/O
	P2.3	11	–	–	I/O	General-purpose I/O
	P2.4	10	–	–	I/O	General-purpose I/O
	P2.5	9	–	–	I/O	General-purpose I/O
	P2.6	8	8	8	I/O	General-purpose I/O
	P2.7	7	7	7	I/O	General-purpose I/O
I2C	UCB0SCL	19	15	15	I/O	eUSCI_B0 I^2C clock
	UCB0SDA	20	16	16	I/O	eUSCI_B0 I^2C data
	UCB0SCL (2)	9	–	–	I/O	eUSCI_B0 I^2C clock
	UCB0SDA (2)	10	–	–	I/O	eUSCI_B0 I^2C data
SPI	UCA0STE	18	14	14	I/O	eUSCI_A0 SPI slave transmit enable
	UCA0CLK	17	13	13	I/O	eUSCI_A0 SPI clock input/output
	UCA0SOMI	16	12	11	I/O	eUSCI_A0 SPI slave out/master in
	UCA0SIMO	15	11	10	I/O	eUSCI_A0 SPI slave in/master out
	UCB0STE	2	2	2	I/O	eUSCI_B0 slave transmit enable
	UCB0CLK	1	1	1	I/O	eUSCI_B0 clock input/output
	UCB0SIMO	20	16	16	I/O	eUSCI_B0 SPI slave in/master out
	UCB0SOMI	19	15	15	I/O	eUSCI_B0 SPI slave out/master in
	UCB0STE (2)	12	–	–	I/O	eUSCI_B0 slave transmit enable
	UCB0CLK (2)	11	–	–	I/O	eUSCI_B0 clock input/output
	UCB0SIMO (2)	10	–	–	I/O	eUSCI_B0 SPI slave in/master out
	UCB0SOMI (2)	9	–	–	I/O	eUSCI_B0 SPI slave out/master in
UART	UCA0RXD	16	12	11	I	eUSCI_A0 UART receive data
	UCA0TXD	15	11	10	O	eUSCI_A0 UART transmit data
Timer_B	TB0.1	16	12	11	I/O	Timer TB0 CCR1 capture: CCI1A input, compare: Out1 outputs
	TB0.2	15	11	10	I/O	Timer TB0 CCR2 capture: CCI2A input, compare: Out2 outputs
	TB0CLK	7	7	7	I	Timer clock input TBCLK for TB0
	TB0TRG	20	16	16	I	TB0 external trigger input for TB0OUTH
	TB1.1	14	10	9	I/O	Timer TB1 CCR1 capture: CCI1A input, compare: Out1 outputs
	TB1.2	13	9	–	I/O	Timer TB1 CCR2 capture: CCI2A input, compare: Out2 outputs
	TB1CLK	12	–	–	I	Timer clock input TBCLK for TB1
	TB1TRG	11	–	–	I	TB1 external trigger input for TB1OUTH

(1) Because this pin is multiplexed with the JTAG function, TI recommends disabling the pin interrupt function while in JTAG debug to prevent collisions.
(2) This is the remapped functionality controlled by the USCIBRMP bit of the SYSCFG2 register. Only one selected port is valid at any time.

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Table 4-2. Signal Descriptions (continued)

FUNCTION	SIGNAL NAME	PIN NUMBER			PIN TYPE	DESCRIPTION
		PW20	RGY	PW16		
VQFN Pad	VQFN Thermal pad	–	Pad	–		VQFN package exposed thermal pad. TI recommends connection to V_{SS}.

NOTE

Functions shared with the four JTAG pins cannot be debugged if 4-wire JTAG is used for debug.

4.4 Pin Multiplexing

Pin multiplexing for these devices is controlled by both register settings and operating modes (for example, if the device is in test mode). For details of the settings for each pin and schematics of the multiplexed ports, see Section 6.12.

4.5 Buffer Type

Table 4-3 defines the pin buffer types that are listed in Table 4-1.

Table 4-3. Buffer Type

BUFFER TYPE (STANDARD)	NOMINAL VOLTAGE	HYSTERESIS	PU OR PD	NOMINAL PU OR PD STRENGTH (µA)	OUTPUT DRIVE STRENGTH (mA)	OTHER CHARACTERISTICS
LVCMOS	3.0 V	Y (1)	Programmable	See Section 5.12.4	See Section 5.12.4.1	
Analog	3.0 V	N	N	N/A	N/A	See analog modules in Section 5 for details.
Power (DVCC)	3.0 V	N	N	N/A	N/A	SVS enables hysteresis on DVCC.
Power (AVCC)	3.0 V	N	N	N/A	N/A	

(1) Only for input pins.

4.6 Connection of Unused Pins

Table 4-4 shows the correct termination of unused pins.

Table 4-4. Connection of Unused Pins (1)

PIN	POTENTIAL	COMMENT
Px.0 to Px.7	Open	Set to port function, output direction (PxDIR.n = 1)
$\overline{\text{RST}}$/NMI	DVCC	47-kΩ pullup or internal pullup selected with 10-nF (or 1.1-nF (2)) pulldown
TEST	Open	This pin always has an internal pulldown enabled.
TRI0-	Open	This pin is a high-impedance output.

(1) Any unused pin with a secondary function that is shared with general-purpose I/O should follow the Px.0 to Px.7 unused pin connection guidelines.
(2) The pulldown capacitor should not exceed 1.1 nF when using devices with Spy-Bi-Wire interface in Spy-Bi-Wire mode with TI tools like FET interfaces or GANG programmers. TI recommends a 1-nF capacitor to enable high-speed SBW communication.

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5 Specifications

5.1 Absolute Maximum Ratings(1)

over operating free-air temperature range (unless otherwise noted)

	MIN	MAX	UNIT
Voltage applied at DVCC pin to V_{SS}	–0.3	4.1	V
Voltage applied to any pin(2)	–0.3	V_{CC} + 0.3 (4.1 V Max)	V
Diode current at any device pin		±2	mA
Maximum junction temperature, T_J		85	°C
Storage temperature, T_{stg}(3)	–40	125	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages referenced to V_{SS}.
(3) Higher temperature may be applied during board soldering according to the current JEDEC J-STD-020 specification with peak reflow temperatures not higher than classified on the device label on the shipping boxes or reels.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±1000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±250	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 500-V HBM is possible with the necessary precautions. Pins listed as ±1000 V may actually have higher performance.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 250-V CDM is possible with the necessary precautions. Pins listed as ±250 V may actually have higher performance.

5.3 Recommended Operating Conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage applied at DVCC pin(1)(2)(3)(4)		1.8		3.6	V
V_{SS}	Supply voltage applied at DVSS pin			0		V
T_A	Operating free-air temperature		–40		85	°C
T_J	Operating junction temperature		–40		85	°C
C_{DVCC}	Recommended capacitor at DVCC(5)		4.7	10		µF
f_{SYSTEM}	Processor frequency (maximum MCLK frequency)(4)(6)	No FRAM wait states (NWAITSx = 0)	0		8	MHz
		With FRAM wait states (NWAITSx = 1)(7)	0		16(8)	
f_{ACLK}	Maximum ACLK frequency				40	kHz
f_{SMCLK}	Maximum SMCLK frequency				16(8)	MHz

(1) Supply voltage changes faster than 0.2 V/µs can trigger a BOR reset even within the recommended supply voltage range. Following the data sheet recommendation for capacitor C_{DVCC} limits the slopes accordingly.
(2) Modules may have a different supply voltage range specification. See the specification of the respective module in this data sheet.
(3) TI recommends that power to the DVCC pin must not exceed the limits specified in *Recommended Operating Conditions*. Exceeding the specified limits can cause malfunction of the device including erroneous writes to RAM and FRAM.
(4) The minimum supply voltage is defined by the SVS levels. See the SVS threshold parameters in Table 5-1.
(5) A capacitor tolerance of ±20% or better is required. A low-ESR ceramic capacitor of 100 nF (minimum) should be placed as close as possible (within a few millimeters) to the respective pin pair.
(6) Modules may have a different maximum input clock specification. See the specification of the respective module in this data sheet.
(7) Wait states only occur on actual FRAM accesses (that is, on FRAM cache misses). RAM and peripheral accesses are always executed without wait states.
(8) If clock sources such as HF crystals or the DCO with frequencies >16 MHz are used, the clock must be divided in the clock system to comply with this operating condition.

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5.4 Active Mode Supply Current Into V_{CC} Excluding External Current(1)

PARAMETER	EXECUTION MEMORY	TEST CONDITIONS	FREQUENCY (f_{MCLK} = f_{SMCLK})						UNIT
			1 MHz 0 WAIT STATES (NWAITSx = 0)		8 MHz 0 WAIT STATES (NWAITSx = 0)		16 MHz 1 WAIT STATE (NWAITSx = 1)		
			TYP	MAX	TYP	MAX	TYP	MAX	
$I_{AM, FRAM}$(0%)	FRAM 0% cache hit ratio	3.0 V, 25°C	474		2639		3156		µA
		3.0 V, 85°C	516		2919		3205		
$I_{AM, FRAM}$(100%)	FRAM 100% cache hit ratio	3.0 V, 25°C	196		585		958		µA
		3.0 V, 85°C	205		598		974		
$I_{AM, RAM}$ (2)	RAM	3.0 V, 25°C	219		750		1250		µA

(1) All inputs are tied to 0 V or to V_{CC}. Outputs do not source or sink any current. Characterized with program executing typical data processing.
f_{ACLK} = 32768 Hz, f_{MCLK} = f_{SMCLK} = f_{DCO} at specified frequency
Program and data entirely reside in FRAM. All execution is from FRAM.
(2) Program and data reside entirely in RAM. All execution is from RAM. No access to FRAM.

5.5 Active Mode Supply Current Per MHz

V_{CC} = 3.0 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	TYP	UNIT
$dI_{AM,FRAM}/df$	Active mode current consumption per MHz, execution from FRAM, no wait states(1)	[(I_{AM} 75% cache hit rate at 8 MHz) – (I_{AM} 75% cache hit rate at 1 MHz)] / 7 MHz	126	µA/MHz

(1) All peripherals are turned on in default settings.

5.6 Low-Power Mode LPM0 Supply Currents Into V_{CC} Excluding External Current

V_{CC} = 3.0 V, T_A = 25°C (unless otherwise noted)(1) (2)

PARAMETER	V_{CC}	FREQUENCY (f_{SMCLK})						UNIT
		1 MHz		8 MHz		16 MHz		
		TYP	MAX	TYP	MAX	TYP	MAX	
I_{LPM0}	2.0 V	158		307		415		µA
	3.0 V	169		318		427		

(1) All inputs are tied to 0 V or to V_{CC}. Outputs do not source or sink any current.
(2) Current for watchdog timer clocked by SMCLK included.
f_{ACLK} = 32768 Hz, f_{MCLK} = 0 MHz, f_{SMCLK} at specified frequency.

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5.7 Low-Power Mode LPM3 and LPM4 Supply Currents (Into V_{CC}) Excluding External Current

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)(1) (see Figure 5-1)

PARAMETER		V_{CC}	–40°C		25°C		85°C		UNIT
			TYP	MAX	TYP	MAX	TYP	MAX	
$I_{LPM3,XT1}$	Low-power mode 3, includes SVS(2) (3) (4)	3.0 V	1.01		1.16		2.53	5.25	µA
		2.0 V	0.99		1.13		2.49		
$I_{LPM3,VLO}$	Low-power mode 3, VLO, excludes SVS(5)	3.0 V	0.88		1.02		2.39	5.06	µA
		2.0 V	0.86		1.00		2.35		
$I_{LPM3, RTC}$	Low-power mode 3, RTC, excludes SVS(6)	3.0 V	0.96		1.11		2.49		µA
		2.0 V	0.94		1.09		2.45		
$I_{LPM4, SVS}$	Low-power mode 4, includes SVS(7)	3.0 V	0.50		0.60		1.93		µA
		2.0 V	0.48		0.59		1.91		
I_{LPM4}	Low-power mode 4, excludes SVS(7)	3.0 V	0.34		0.45		1.77		µA
		2.0 V	0.34		0.44		1.75		
$I_{LPM4, RTC, VLO}$	Low-power mode 4, RTC is sourced from VLO, excludes SVS(8)	3.0 V	0.48		0.59		1.91		µA
		2.0 V	0.48		0.58		1.89		
$I_{LPM4, RTC, XT1}$	Low-power mode 4, RTC is sourced from XT1, excludes SVS(6)(9)	3.0 V	0.89		1.04		2.41		µA
		2.0 V	0.88		1.02		2.38		

(1) All inputs are tied to 0 V or to V_{CC}. Outputs do not source or sink any current.
(2) Not applicable for devices with HF crystal oscillator only.
(3) Characterized with a Seiko Crystal SC-32S crystal with a load capacitance chosen to closely match the required load.
(4) Low-power mode 3, includes SVS test conditions:
Current for watchdog timer clocked by ACLK and RTC clocked by XT1 included. Current for brownout and SVS included (SVSHE = 1).
CPUOFF = 1, SCG0 = 1 SCG1 = 1, OSCOFF = 0 (LPM3),
f_{XT1} = 32768 Hz, $f_{ACLK} = f_{XT1}$, $f_{MCLK} = f_{SMCLK}$ = 0 MHz
(5) Low-power mode 3, VLO, excludes SVS test conditions:
Current for watchdog timer clocked by VLO included. RTC disabled. Current for brownout included. SVS disabled (SVSHE = 0).
CPUOFF = 1, SCG0 = 1 SCG1 = 1, OSCOFF = 0 (LPM3),
f_{XT1} = 32768 Hz, $f_{MCLK} = f_{SMCLK}$ = 0 MHz
(6) RTC is sourced from external 32768-Hz crystal.
(7) CPUOFF = 1, SCG0 = 1 SCG1 = 1, OSCOFF = 1 (LPM4), CPU and all clocks are disabled, WDT and RTC disabled
(8) Low-power mode 4, VLO, excludes SVS test conditions:
Current for RTC clocked by VLO included. Current for brownout included. SVS disabled (SVSHE = 0).
CPUOFF = 1, SCG0 = 1 SCG1 = 1, OSCOFF = 1 (LPM4),
f_{XT1} = 0 Hz, $f_{MCLK} = f_{SMCLK}$ = 0 MHz
(9) Low-power mode 4, XT1, excludes SVS test conditions:
Current for RTC clocked by XT1 included. Current for brownout included. SVS disabled (SVSHE = 0).
CPUOFF = 1, SCG0 = 1 SCG1 = 1, OSCOFF = 1 (LPM4),
f_{XT1} = 32768 Hz, $f_{MCLK} = f_{SMCLK}$ = 0 MHz

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5.8 Low-Power Mode LPMx.5 Supply Currents (Into V_{CC}) Excluding External Current

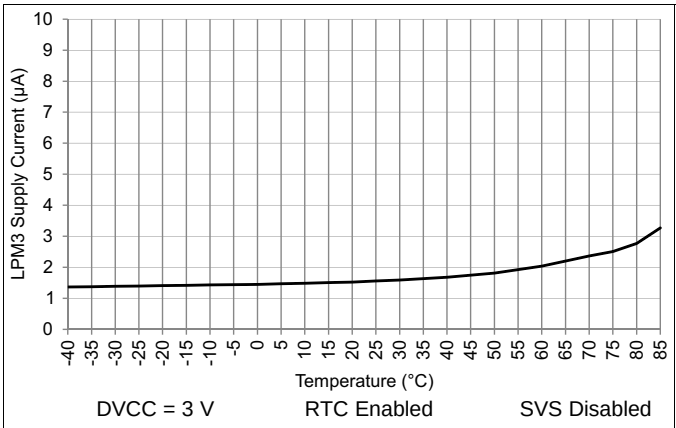
over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		V_{CC}	–40°C		25°C		85°C		UNIT
			TYP	MAX	TYP	MAX	TYP	MAX	
$I_{LPM3.5,\ XT1}$	Low-power mode 3.5, includes SVS(1) (2) (3) (also see Figure 5-2)	3.0 V	0.64		0.71		0.86	1.23	µA
		2.0 V	0.61		0.69		0.83		
$I_{LPM4.5,\ SVS}$	Low-power mode 4.5, includes SVS(4) (also see Figure 5-3)	3.0 V	0.23		0.25		0.30	0.45	µA
		2.0 V	0.21		0.24		0.29		
$I_{LPM4.5}$	Low-power mode 4.5, excludes SVS(5)	3.0 V	0.020		0.032		0.071	0.120	µA
		2.0 V	0.022		0.034		0.068		

(1) Not applicable for devices with HF crystal oscillator only.
(2) Characterized with a Seiko Crystal SC-32S crystal with a load capacitance chosen to closely match the required load.
(3) Low-power mode 3.5, includes SVS test conditions:
Current for RTC clocked by XT1 included. Current for brownout and SVS included (SVSHE = 1). Core regulator disabled.
PMMREGOFF = 1, CPUOFF = 1, SCG0 = 1 SCG1 = 1, OSCOFF = 1 (LPMx.5),
f_{XT1} = 32768 Hz, $f_{ACLK} = f_{XT1}$, $f_{MCLK} = f_{SMCLK}$ = 0 MHz
(4) Low-power mode 4.5, includes SVS test conditions:
Current for brownout and SVS included (SVSHE = 1). Core regulator disabled.
PMMREGOFF = 1, CPUOFF = 1, SCG0 = 1 SCG1 = 1, OSCOFF = 1 (LPMx.5),
f_{XT1} = 0 Hz, $f_{ACLK} = f_{MCLK} = f_{SMCLK}$ = 0 MHz
(5) Low-power mode 4.5, excludes SVS test conditions:
Current for brownout included. SVS disabled (SVSHE = 0). Core regulator disabled.
PMMREGOFF = 1, CPUOFF = 1, SCG0 = 1 SCG1 = 1, OSCOFF = 1 (LPMx.5),
f_{XT1} = 0 Hz, $f_{ACLK} = f_{MCLK} = f_{SMCLK}$ = 0 MHz

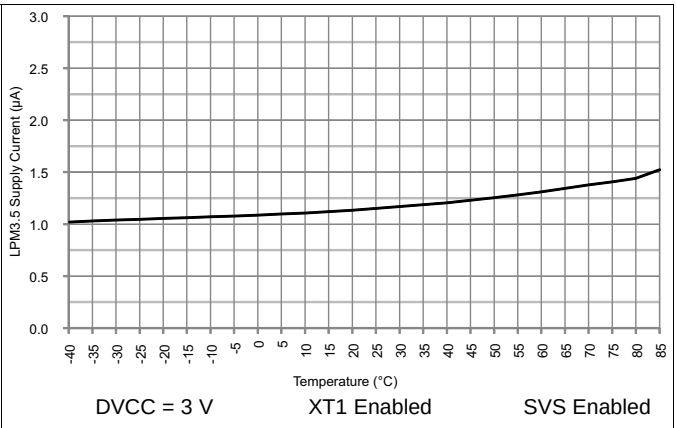
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5.9 Production Distribution of LPM Supply Currents



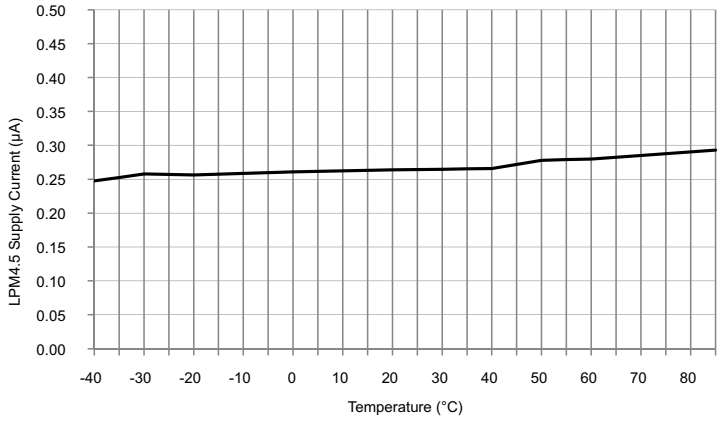
DVCC = 3 V RTC Enabled SVS Disabled

Figure 5-1. LPM3 Supply Current vs Temperature



DVCC = 3 V XT1 Enabled SVS Enabled

Figure 5-2. LPM3.5 Supply Current vs Temperature



DVCC = 3 V SVS Enabled

Figure 5-3. LPM4.5 Supply Current vs Temperature

5.10 Typical Characteristics – Current Consumption Per Module

MODULE	TEST CONDITIONS	REFERENCE CLOCK	TYP	UNIT
Timer_B	SMCLK = 8 MHz, MC = 10b	Module input clock	5	µA/MHz
eUSCI_A	UART mode	Module input clock	7	µA/MHz
eUSCI_A	SPI mode	Module input clock	5	µA/MHz
eUSCI_B	SPI mode	Module input clock	5	µA/MHz
eUSCI_B	I^2C mode, 100 kbaud	Module input clock	5	µA/MHz
RTC		32 kHz	85	nA
CRC	From start to end of operation	MCLK	8.5	µA/MHz

5.11 Thermal Resistance Characteristics

			VALUE	UNIT
θ_{JA}	Junction-to-ambient thermal resistance, still air(1)	VQFN 16 pin (RGY)	41.8	ºC/W
		TSSOP 20 pin (PW20)	92.6	
		TSSOP 16 pin (PW16)	104.1	
θ_{JC}	Junction-to-case (top) thermal resistance(2)	VQFN 16 pin (RGY)	49.1	ºC/W
		TSSOP 20 pin (PW20)	26.1	
		TSSOP 16 pin (PW16)	38.5	
θ_{JB}	Junction-to-board thermal resistance(3)	VQFN 16 pin (RGY)	18.5	ºC/W
		TSSOP 20 pin (PW20)	45.0	
		TSSOP 16 pin (PW16)	49.1	

(1) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, High-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
(2) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specific JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
(3) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.

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5.12 Timing and Switching Characteristics

5.12.1 Power Supply Sequencing

Table 5-1 lists the characteristics of the SVS and BOR.

Table 5-1. PMM, SVS and BOR

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 5-4)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{BOR, safe}$	Safe BOR power-down level(1)		0.1			V
$t_{BOR, safe}$	Safe BOR reset delay(2)		10			ms
$I_{SVSH,AM}$	SVS_H current consumption, active mode	V_{CC} = 3.6 V			1.5	µA
$I_{SVSH,LPM}$	SVS_H current consumption, low-power modes	V_{CC} = 3.6 V		240		nA
V_{SVSH-}	SVS_H power-down level(3)		1.71	1.80	1.87	V
V_{SVSH+}	SVS_H power-up level(3)		1.76	1.88	1.99	V
V_{SVSH_hys}	SVS_H hysteresis			80		mV
$t_{PD,SVSH, AM}$	SVS_H propagation delay, active mode				10	µs
$t_{PD,SVSH, LPM}$	SVS_H propagation delay, low-power modes				100	µs

(1) A safe BOR is correctly generated only if DVCC drops below this voltage before it rises.
(2) When an BOR occurs, a safe BOR is correctly generated only if DVCC is kept low longer than this period before it reaches V_{SVSH+}.
(3) For additional information, see the Dynamic Voltage Scaling Power Solution for MSP430 Devices With Single-Channel LDO Reference Design.

Figure 5-4 shows the reset conditions.

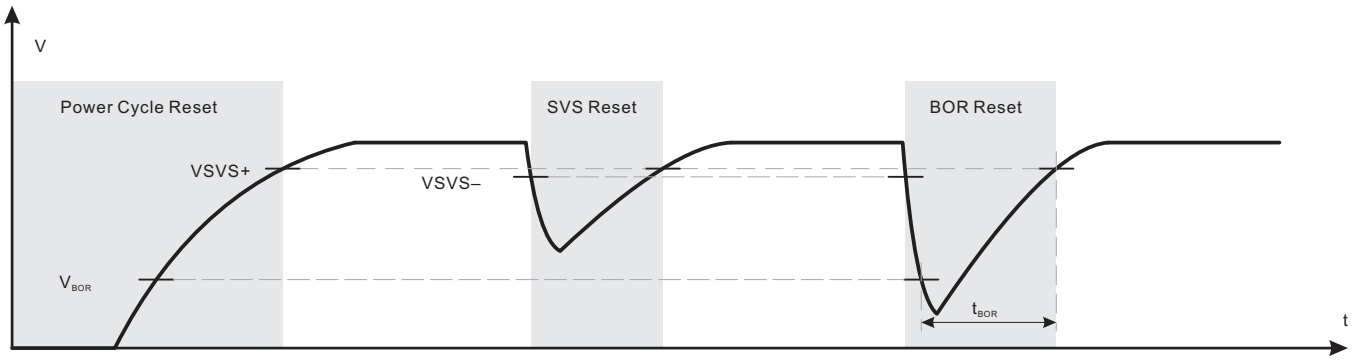


Figure 5-4. Power Cycle, SVS, and BOR Reset Conditions

5.12.2 Reset Timing

Table 5-2 lists the wake-up times from low-power modes and reset.

Table 5-2. Wake-up Times From Low-Power Modes and Reset

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$t_{WAKE-UP\ FRAM}$	(Additional) wake-up time to activate the FRAM in AM if previously disabled through the FRAM controller or from a LPM if immediate activation is selected for wakeup (1)		3 V		10		µs
$t_{WAKE-UP\ LPM0}$	Wake-up time from LPM0 to active mode (1)		3 V			200 + 2.5 / f_{DCO}	ns
$t_{WAKE-UP\ LPM3}$	Wake-up time from LPM3 to active mode (1)		3 V		10		µs
$t_{WAKE-UP\ LPM4}$	Wake-up time from LPM4 to active mode (2)		3 V		10		µs
$t_{WAKE-UP\ LPM3.5}$	Wake-up time from LPM3.5 to active mode (2)		3 V		350		µs
$t_{WAKE-UP\ LPM4.5}$	Wake-up time from LPM4.5 to active mode (2)	SVSHE = 1	3 V		350		µs
		SVSHE = 0	3 V		1		ms
$t_{WAKE-UP-RESET}$	Wake-up time from $\overline{RST}$ or BOR event to active mode (2)		3 V		1		ms
t_{RESET}	Pulse duration required at $\overline{RST}$/NMI pin to accept a reset			2			µs

(1) The wake-up time is measured from the edge of an external wake-up signal (for example, port interrupt or wake-up event) to the first externally observable MCLK clock edge.
(2) The wake-up time is measured from the edge of an external wake-up signal (for example, port interrupt or wake-up event) until the first instruction of the user program is executed.

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5.12.3 Clock Specifications

Table 5-3 lists the characteristics of the XT1 crystal oscillator (low frequency).

Table 5-3. XT1 Crystal Oscillator (Low Frequency)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)(1)(2)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$f_{XT1,\ LF}$	XT1 oscillator crystal, low frequency	LFXTBYPASS = 0			32768		Hz
$DC_{XT1,\ LF}$	XT1 oscillator LF duty cycle	Measured at MCLK, f_{LFXT} = 32768 Hz		30%		70%	
$f_{XT1,SW}$	XT1 oscillator logic-level square-wave input frequency	LFXTBYPASS = 1 (3) (4)			32768		Hz
$DC_{XT1,\ SW}$	LFXT oscillator logic-level square-wave input duty cycle	LFXTBYPASS = 1		40%		60%	
OA_{LFXT}	Oscillation allowance for LF crystals (5)	LFXTBYPASS = 0, LFXTDRIVE = {3}, f_{LFXT} = 32768 Hz, $C_{L,eff}$ = 12.5 pF			200		kΩ
$C_{L,eff}$	Integrated effective load capacitance (6)				(7)1		pF
$t_{START,LFXT}$	Start-up time (8)	f_{OSC} = 32768 Hz LFXTBYPASS = 0, LFXTDRIVE = {3}, T_A = 25°C, $C_{L,eff}$ = 12.5 pF			1000		ms
$f_{Fault,LFXT}$	Oscillator fault frequency (9)	XTS = 0(10)		0		3500	Hz

(1) To improve EMI on the LFXT oscillator, observe the following guidelines.
- Keep the trace between the device and the crystal as short as possible.
- Design a good ground plane around the oscillator pins.
- Prevent crosstalk from other clock or data lines into oscillator pins XIN and XOUT.
- Avoid running PCB traces under or adjacent to the XIN and XOUT pins.
- Use assembly materials and processes that avoid any parasitic load on the oscillator XIN and XOUT pins.
- If conformal coating is used, make sure that it does not induce capacitive or resistive leakage between the oscillator pins.

(2) See MSP430 32-kHz Crystal Oscillators for details on crystal section, layout, and testing.
(3) When LFXTBYPASS is set, LFXT circuits are automatically powered down. Input signal is a digital square wave with parametrics defined in the Schmitt-trigger inputs section of this data sheet. Duty cycle requirements are defined by $DC_{LFXT,\ SW}$.
(4) Maximum frequency of operation of the entire device cannot be exceeded.
(5) Oscillation allowance is based on a safety factor of 5 for recommended crystals. The oscillation allowance is a function of the LFXTDRIVE settings and the effective load. In general, comparable oscillator allowance can be achieved based on the following guidelines, but should be evaluated based on the actual crystal selected for the application:
- For LFXTDRIVE = {0}, $C_{L,eff}$ = 3.7 pF.
- For LFXTDRIVE = {1}, 6 pF ≤ $C_{L,eff}$ ≤ 9 pF.
- For LFXTDRIVE = {2}, 6 pF ≤ $C_{L,eff}$ ≤ 10 pF.
- For LFXTDRIVE = {3}, 6 pF ≤ $C_{L,eff}$ ≤ 12 pF.

(6) Includes parasitic bond and package capacitance (approximately 2 pF per pin).
(7) Requires external capacitors at both terminals to meet the effective load capacitance specified by crystal manufacturers. Recommended effective load capacitance values supported are 3.7 pF, 6 pF, 9 pF, and 12.5 pF. Maximum shunt capacitance of 1.6 pF. The PCB adds additional capacitance, so it must also be considered in the overall capacitance. Verify that the recommended effective load capacitance of the selected crystal is met.
(8) Includes start-up counter of 1024 clock cycles.
(9) Frequencies above the MAX specification do not set the fault flag. Frequencies in between the MIN and MAX specification may set the flag. A static condition or stuck at fault condition sets the flag.
(10) Measured with logic-level input frequency but also applies to operation with crystals.

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Table 5-4 lists the characteristics of the XT1 crystal oscillator (high frequency).

Table 5-4. XT1 Crystal Oscillator (High Frequency)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
f_{HFXT}	HFXT oscillator crystal frequency, crystal mode	XT1BYPASS = 0, XTS = 1, XT1HFFREQ = 00		1		4	MHz
		XT1BYPASS = 0, XTS = 1, XT1HFFREQ = 01		4.01		6	
		XT1BYPASS = 0, XTS = 1, XT1HFFREQ = 10		6.01		16	
$f_{HFXT,SW}$	HFXT oscillator logic-level square-wave input frequency, bypass mode	XT1BYPASS = 1, XTS = 1 (2) (3)		1		16	MHz
DC_{HFXT}	HFXT oscillator duty cycle	Measured at ACLK, $f_{HFXT,HF}$ = 4 MHz(4)		40%		60%	
$DC_{HFXT,SW}$	HFXT oscillator logic-level square-wave input duty cycle	XT1BYPASS = 1		40%		60%	
OA_{HFXT}	Oscillation allowance for HFXT crystals(5)	XT1BYPASS = 0, XT1HFSEL = 1, $f_{HFXT,HF}$ = 16 MHz, $C_{L,eff}$ = 18 pF			2.4		kΩ
$t_{START,HFXT}$	Start-up time(6)	f_{OSC} = 4 MHz, XTS = 1(4), XT1BYPASS = 0, XT1HFFREQ = 00, XT1DRIVE = 3, T_A = 25°C, $C_{L,eff}$ = 18 pF			1.6		ms
		f_{OSC} = 16 MHz, XTS = 1(4), XT1BYPASS = 0, XT1HFFREQ = 00, XT1DRIVE = 3, T_A = 25°C, $C_{L,eff}$ = 18 pF			1.1		
$C_{L,eff}$	Integrated effective load capacitance(7) (8)				1		pF
$f_{Fault,HFXT}$	Oscillator fault frequency(9) (10)			0		800	kHz

(1) To improve EMI on the HFXT oscillator, the following guidelines should be observed.
- Keep the trace between the device and the crystal as short as possible.
- Design a good ground plane around the oscillator pins.
- Prevent crosstalk from other clock or data lines into oscillator pins XIN and XOUT.
- Avoid running PCB traces under or adjacent to the XIN and XOUT pins.
- Use assembly materials and processes that avoid any parasitic load on the oscillator XIN and XOUT pins.
- If conformal coating is used, make sure that it does not induce capacitive or resistive leakage between the oscillator pins.

(2) When XT1BYPASS is set, HFXT circuits are automatically powered down. Input signal is a digital square wave with parametrics defined in the Schmitt-trigger Inputs section of this datasheet. Duty cycle requirements are defined by $DC_{HFXT, SW}$.
(3) Maximum frequency of operation of the entire device cannot be exceeded.
(4) 4-MHz crystal used for lab characterization: Abracon HC49/U AB-4.000MHZ-B2
16-MHz crystal used for lab characterization: Abracon HC49/U AB-16.000MHZ-B2
(5) Oscillation allowance is based on a safety factor of 5 for recommended crystals.
(6) Includes start-up counter of 4096 clock cycles.
(7) Includes parasitic bond and package capacitance (approximately 2 pF per pin).
Because the PCB adds additional capacitance, TI recommends verifying the correct load by measuring the oscillator frequency through MCLK or SMCLK. For a correct setup, the effective load capacitance should always match the specification of the used crystal.
(8) Requires external capacitors at both terminals. Values are specified by crystal manufacturers. Recommended values supported are 14 pF, 16 pF, and 18 pF. Maximum shunt capacitance of 7 pF.
(9) Frequencies above the MAX specification do not set the fault flag. Frequencies between the MIN and MAX might set the flag. A static condition or stuck at fault condition sets the flag.
(10) Measured with logic-level input frequency but also applies to operation with crystals.

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Table 5-5 lists the characteristics of the DCO FLL.

Table 5-5. DCO FLL

over recommended operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$f_{DCO, FLL}$	FLL lock frequency, 16 MHz, 25°C	Measured at MCLK, internal trimmed REFO as reference	3.0 V	–1.0%		1.0%	
	FLL lock frequency, 16 MHz, –40°C to 85°C			–2.0%		2.0%	
	FLL lock frequency, 16 MHz, –40°C to 85°C	Measured at MCLK, XT1 crystal as reference		–0.5%		0.5%	
f_{DUTY}	Duty cycle	Measured at MCLK, XT1 crystal as reference	3.0 V	40%	50%	60%	
$Jitter_{cc}$	Cycle-to-cycle jitter, 16 MHz	Measured at MCLK, XT1 crystal as reference	3.0 V		0.25%		
$Jitter_{long}$	Long-term jitter, 16 MHz	Measured at MCLK, XT1 crystal as reference	3.0 V		0.022%		
$t_{FLL, lock}$	FLL lock time, 16 MHz	Measured at MCLK, XT1 crystal as reference	3.0 V		200		ms

Table 5-6 lists the characteristics of the DCO frequency.

Table 5-6. DCO Frequency

over recommended operating free-air temperature (unless otherwise noted) (see Figure 5-5)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$f_{DCO, 16 MHz}$	DCO frequency, 16 MHz	DCORSEL = 101b, DISMOD = 1b, DCOFTRIM = 000b, DCO = 0		7.8		MHz
		DCORSEL = 101b, DISMOD = 1b, DCOFTRIM = 000b, DCO = 511		12.5		
		DCORSEL = 101b, DISMOD = 1b, DCOFTRIM = 111b, DCO = 0		18		
		DCORSEL = 101b, DISMOD = 1b, DCOFTRIM = 111b, DCO = 511		30		
$f_{DCO, 12 MHz}$	DCO frequency, 12 MHz	DCORSEL = 100b, DISMOD = 1b, DCOFTRIM = 000b, DCO = 0		6		MHz
		DCORSEL = 100b, DISMOD = 1b, DCOFTRIM = 000b, DCO = 511		9.5		
		DCORSEL = 100b, DISMOD = 1b, DCOFTRIM = 111b, DCO = 0		13.5		
		DCORSEL = 100b, DISMOD = 1b, DCOFTRIM = 111b, DCO = 511		22		
$f_{DCO, 8 MHz}$	DCO frequency, 8 MHz	DCORSEL = 011b, DISMOD = 1b, DCOFTRIM = 000b, DCO = 0		3.8		MHz
		DCORSEL = 011b, DISMOD = 1b, DCOFTRIM = 000b, DCO = 511		6.5		
		DCORSEL = 011b, DISMOD = 1b, DCOFTRIM = 111b, DCO = 0		9.5		
		DCORSEL = 011b, DISMOD = 1b, DCOFTRIM = 111b, DCO = 511		16		
$f_{DCO, 4 MHz}$	DCO frequency, 4 MHz	DCORSEL = 010b,, DISMOD = 1b, DCOFTRIM = 000b, DCO = 0		2		MHz
		DCORSEL = 010b, DISMOD = 1b, DCOFTRIM = 000b, DCO = 511		3.2		
		DCORSEL = 010b, DISMOD = 1b, DCOFTRIM = 111b, DCO = 0		4.8		
		DCORSEL = 010b, DISMOD = 1b, DCOFTRIM = 111b, DCO = 511		8		

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Table 5-6. DCO Frequency (continued)

over recommended operating free-air temperature (unless otherwise noted) (see Figure 5-5)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$f_{DCO, 2 MHz}$	DCO frequency, 2 MHz	DCORSEL = 001b, DISMOD = 1b, DCOFTRIM = 000b, DCO = 0		1		MHz
		DCORSEL = 001b, DISMOD = 1b, DCOFTRIM = 000b, DCO = 511		1.7		
		DCORSEL = 001b, DISMOD = 1b, DCOFTRIM = 111b, DCO = 0		2.5		
		DCORSEL = 001b, DISMOD = 1b, DCOFTRIM = 111b, DCO = 511		4.2		
$f_{DCO, 1 MHz}$	DCO frequency, 1 MHz	DCORSEL = 000b, DISMOD = 1b, DCOFTRIM = 000b, DCO = 0		0.5		MHz
		DCORSEL = 000b, DISMOD = 1b, DCOFTRIM = 000b, DCO = 511		0.85		
		DCORSEL = 000b, DISMOD = 1b, DCOFTRIM = 111b, DCO = 0		1.2		
		DCORSEL = 000b, DISMOD = 1b, DCOFTRIM = 111b, DCO = 511		2.1		

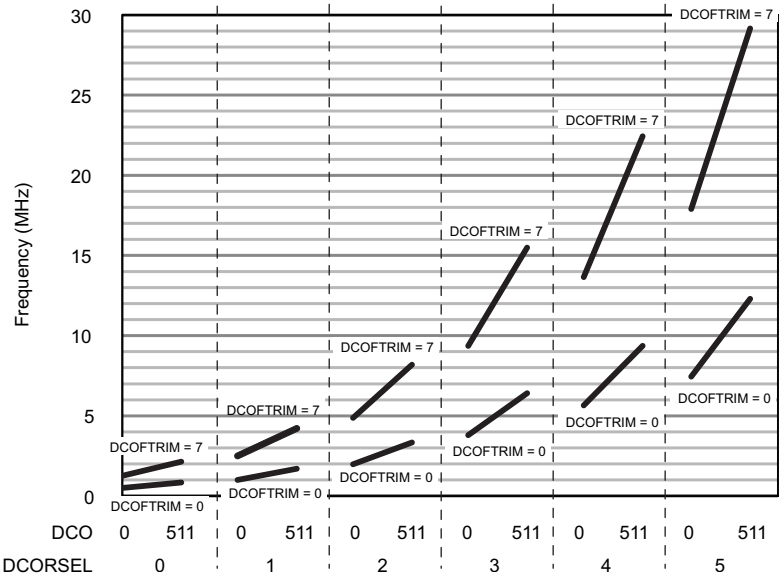


Figure 5-5. Typical DCO Frequency

Table 5-7 lists the characteristics of the REFO.

Table 5-7. REFO

over recommended operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
I_{REFO}	REFO oscillator current consumption	T_A = 25°C	3.0 V		15		µA
f_{REFO}	REFO calibrated frequency	Measured at MCLK	3.0 V		32768		Hz
	REFO absolute calibrated tolerance	T_A = –40°C to 85°C	1.8 V to 3.6 V	–3.5%		+3.5%	
df_{REFO}/d_T	REFO frequency temperature drift	Measured at MCLK(1)	3.0 V		0.01		%/°C
df_{REFO}/d_{VCC}	REFO frequency supply voltage drift	Measured at MCLK at 25°C(2)	1.8 V to 3.6 V		1		%/V
f_{DC}	REFO duty cycle	Measured at MCLK	1.8V to 3.6 V	40%	50%	60%	
t_{START}	REFO start-up time	40% to 60% duty cycle			50		µs

(1) Calculated using the box method: (MAX(–40°C to 85°C) – MIN(–40°C to 85°C)) / MIN(–40°C to 85°C) / (85°C – (–40°C))
(2) Calculated using the box method: (MAX(1.8 V to 3.6 V) – MIN(1.8 V to 3.6 V)) / MIN(1.8 V to 3.6 V) / (3.6 V – 1.8 V)

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Table 5-8 lists the characteristics of the internal very-low-power low-frequency oscillator (VLO).

Table 5-8. Internal Very-Low-Power Low-Frequency Oscillator (VLO)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
f_{VLO}	VLO frequency	Measured at MCLK	3.0 V		10		kHz
df_{VLO}/d_T	VLO frequency temperature drift	Measured at MCLK(1)	3.0 V		0.5		%/°C
df_{VLO}/dV_{CC}	VLO frequency supply voltage drift	Measured at MCLK(2)	1.8 V to 3.6 V		4		%/V
$f_{VLO,DC}$	Duty cycle	Measured at MCLK	3.0 V		50%		

(1) Calculated using the box method: (MAX(–40°C to 85°C) – MIN(–40°C to 85°C)) / MIN(–40°C to 85°C) / (85°C – (–40°C))
(2) Calculated using the box method: (MAX(1.8 V to 3.6 V) – MIN(1.8 V to 3.6 V)) / MIN(1.8 V to 3.6 V) / (3.6 V – 1.8 V)

NOTE

The VLO clock frequency is reduced by 15% (typical) when the device switches from active mode or LPM0 to LPM3 or LPM4, because the reference changes. This lower frequency is not a violation of the VLO specifications (see Table 5-8).

Table 5-9 lists the characteristics of the module oscillator (MODOSC).

Table 5-9. Module Oscillator (MODOSC)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		V_{CC}	MIN	TYP	MAX	UNIT
f_{MODOSC}	MODOSC frequency	3.0 V	3.8	4.8	5.8	MHz
f_{MODOSC}/dT	MODOSC frequency temperature drift	3.0 V		0.102		%/°C
f_{MODOSC}/dV_{CC}	MODOSC frequency supply voltage drift	1.8 V to 3.6 V		1.02		%/V
$f_{MODOSC,DC}$	Duty cycle	3.0 V	40%	50%	60%	

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5.12.4 Digital I/Os

Table 5-10 lists the characteristics of the digital inputs.

Table 5-10. Digital Inputs

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
V_{IT+}	Positive-going input threshold voltage		2 V	0.90		1.50	V
			3 V	1.35		2.25	
V_{IT-}	Negative-going input threshold voltage		2 V	0.50		1.10	V
			3 V	0.75		1.65	
V_{hys}	Input voltage hysteresis ($V_{IT+} - V_{IT-}$)		2 V	0.3		0.8	V
			3 V	0.4		1.2	
R_{Pull}	Pullup or pulldown resistor	For pullup: $V_{IN} = V_{SS}$ For pulldown: $V_{IN} = V_{CC}$		20	35	50	kΩ
$C_{I,dig}$	Input capacitance, digital only port pins	$V_{IN} = V_{SS}$ or V_{CC}			3		pF
$C_{I,ana}$	Input capacitance, port pins with shared analog functions	$V_{IN} = V_{SS}$ or V_{CC}			5		pF
$I_{lkg(Px.y)}$	High-impedance leakage current (1) (2)		2 V, 3 V	–20		+20	nA
$t_{(int)}$	External interrupt timing (external trigger pulse duration to set interrupt flag) (3)	Ports with interrupt capability (see block diagram and terminal function descriptions)	2 V, 3 V	50			ns

(1) The leakage current is measured with V_{SS} or V_{CC} applied to the corresponding pins, unless otherwise noted.
(2) The leakage of the digital port pins is measured individually. The port pin is selected for input and the pullup or pulldown resistor is disabled.
(3) An external signal sets the interrupt flag every time the minimum interrupt pulse duration $t_{(int)}$ is met. The interrupt flag may be set by trigger signals shorter than $t_{(int)}$.

Table 5-11 lists the characteristics of the digital outputs. Also see Figure 5-6 through Figure 5-9.

Table 5-11. Digital Outputs

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	$I_{(OHmax)}$ = –3 mA (1)	2.0 V	1.4		2.0	V
		$I_{(OHmax)}$ = –5 mA (1)	3.0 V	2.4		3.0	
V_{OL}	Low-level output voltage	$I_{(OLmax)}$ = 3 mA (1)	2.0 V	0.0		0.60	V
		$I_{(OLmax)}$ = 5 mA (1)	3.0 V	0.0		0.60	
f_{Port_CLK}	Clock output frequency	C_L = 20 pF (2)	2.0 V	16			MHz
			3.0 V	16			
$t_{rise,dig}$	Port output rise time, digital only port pins	C_L = 20 pF	2.0 V		10		ns
			3.0 V		7		
$t_{fall,dig}$	Port output fall time, digital only port pins	C_L = 20 pF	2.0 V		10		ns
			3.0 V		5		

(1) The maximum total current, $I_{(OHmax)}$ and $I_{(OLmax)}$, for all outputs combined should not exceed ±48 mA to hold the maximum voltage drop specified.
(2) The port can output frequencies at least up to the specified limit and might support higher frequencies.

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5.12.4.1 Digital I/O Typical Characteristics

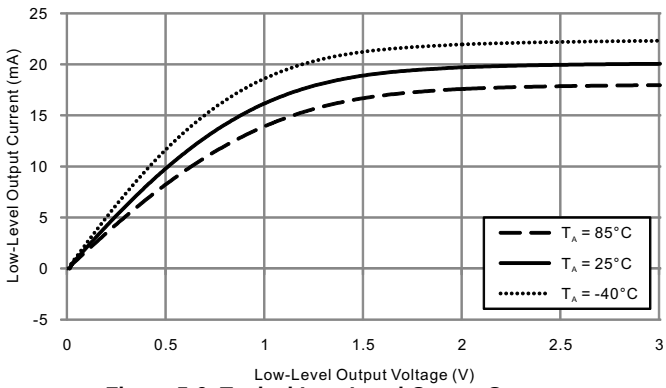


Figure 5-6. Typical Low-Level Output Current vs Low-Level Output Voltage (DVCC = 3 V)

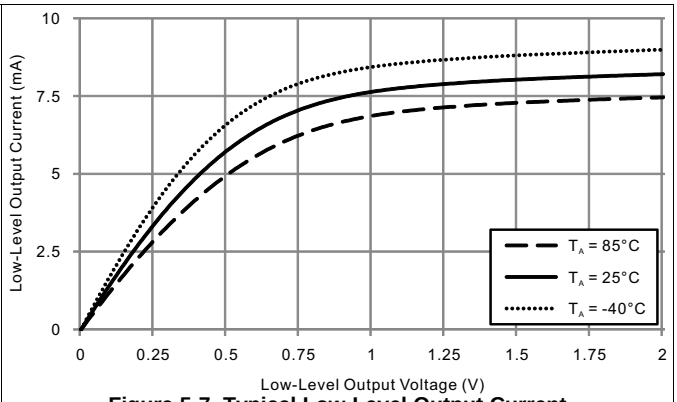


Figure 5-7. Typical Low-Level Output Current vs Low-Level Output Voltage (DVCC = 2 V)

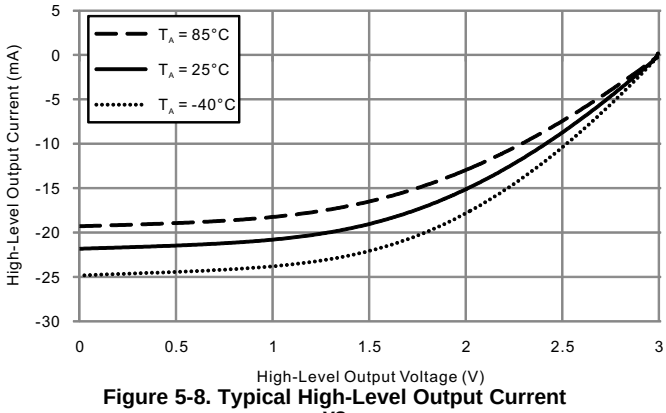


Figure 5-8. Typical High-Level Output Current vs High-Level Output Voltage (DVCC = 3 V)

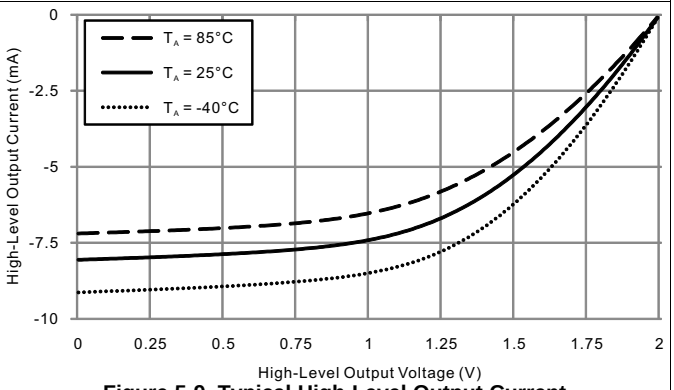


Figure 5-9. Typical High-Level Output Current vs High-Level Output Voltage (DVCC = 2 V)

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5.12.5 VREF+ Built-in Reference

Table 5-12 lists the characteristics of the VREF+.

Table 5-12. VREF+

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
V_{REF+}	Positive built-in reference voltage	EXTREFEN = 1 with 1-mA load current to ground	2.0 V, 3.0 V	1.15	1.19	1.23	V
TC_{REF+}	Temperature coefficient of built-in reference voltage	EXTREFEN = 1 with 1-mA load current			30		µV/°C

5.12.6 Timer_B

Table 5-13 lists the characteristics of the Timer_B clock frequency.

Table 5-13. Timer_B

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	MAX	UNIT
f_{TB}	Timer_B input clock frequency	Internal: SMCLK or ACLK, External: TBCLK, Duty cycle = 50% ±10%	2.0 V, 3.0 V		16	MHz
$t_{TB,cap}$	Timer_B capture timing	All capture inputs, minimum pulse duration required for capture	2.0 V, 3.0 V	20		ns

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5.12.7 eUSCI

Table 5-14 lists the clock frequency of the eUSCI in UART mode.

Table 5-14. eUSCI (UART Mode) Clock Frequency

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	MAX	UNIT
f_{eUSCI}	eUSCI input clock frequency	Internal: SMCLK or MODCLK, External: UCLK, Duty cycle = 50% ±10%	2.0 V, 3.0 V		16	MHz
f_{BITCLK}	BITCLK clock frequency (equals baud rate in Mbaud)		2.0 V, 3.0 V		5	MHz

Table 5-15 lists the switching characteristics of the eUSCI in UART mode.

Table 5-15. eUSCI (UART Mode) Switching Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
t_t	UART receive deglitch time (1)	UCGLITx = 0	2.0 V, 3.0 V		12		ns
		UCGLITx = 1			40		
		UCGLITx = 2			68		
		UCGLITx = 3			110		

(1) Pulses on the UART receive input (UCxRX) shorter than the UART receive deglitch time are suppressed. To make sure that pulses are correctly recognized, their duration must exceed the maximum specification of the deglitch time.

Table 5-16 lists the clock frequency of the eUSCI in SPI master mode.

Table 5-16. eUSCI (SPI Master Mode) Clock Frequency

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		CONDITIONS	MIN	MAX	UNIT
f_{eUSCI}	eUSCI input clock frequency	Internal: SMCLK or MODCLK, Duty cycle = 50% ±10%		8	MHz

Table 5-17 lists the switching characteristics of the eUSCI in SPI master mode.

Table 5-17. eUSCI (SPI Master Mode) Switching Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	MAX	UNIT
$t_{STE,LEAD}$	STE lead time, STE active to clock	UCSTEM = 1, UCMODEx = 01 or 10		1		UCxCLK cycles
$t_{STE,LAG}$	STE lag time, last clock to STE inactive	UCSTEM = 1, UCMODEx = 01 or 10		1		UCxCLK cycles
$t_{SU,MI}$	SOMI input data setup time		2.0 V	47		ns
			3.0 V	35		
$t_{HD,MI}$	SOMI input data hold time		2.0 V	0		ns
			3.0 V	0		
$t_{VALID,MO}$	SIMO output data valid time(2)	UCLK edge to SIMO valid, C_L = 20 pF	2.0 V		20	ns
			3.0 V		20	
$t_{HD,MO}$	SIMO output data hold time(3)	C_L = 20 pF	2.0 V	0		ns
			3.0 V	0		

(1) $f_{UCxCLK} = 1/2t_{LO/HI}$ with $t_{LO/HI} = \max(t_{VALID,MO(eUSCI)} + t_{SU,SI(Slave)}, t_{SU,MI(eUSCI)} + t_{VALID,SO(Slave)})$
For the slave parameters $t_{SU,SI(Slave)}$ and $t_{VALID,SO(Slave)}$, see the SPI parameters of the attached slave.
(2) Specifies the time to drive the next valid data to the SIMO output after the output changing UCLK clock edge. See the timing diagrams in Figure 5-10 and Figure 5-11.
(3) Specifies how long data on the SIMO output is valid after the output changing UCLK clock edge. Negative values indicate that the data on the SIMO output can become invalid before the output changing clock edge observed on UCLK. See the timing diagrams in Figure 5-10 and Figure 5-11.

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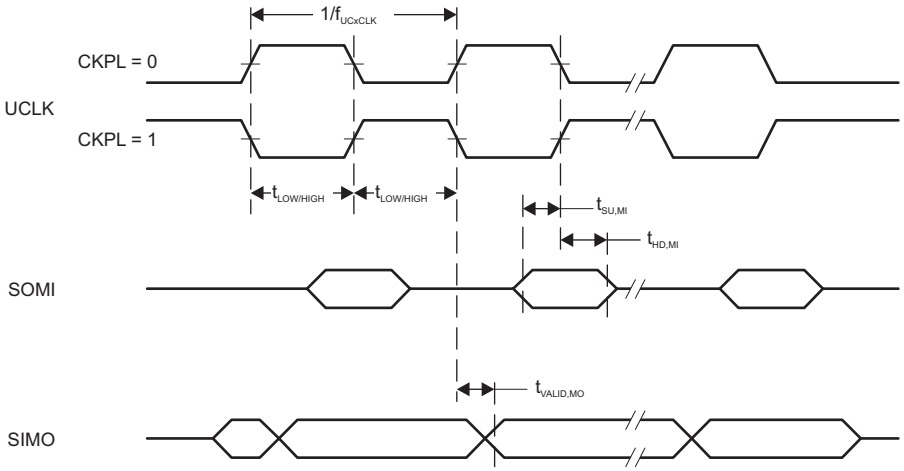


Figure 5-10. SPI Master Mode, CKPH = 0

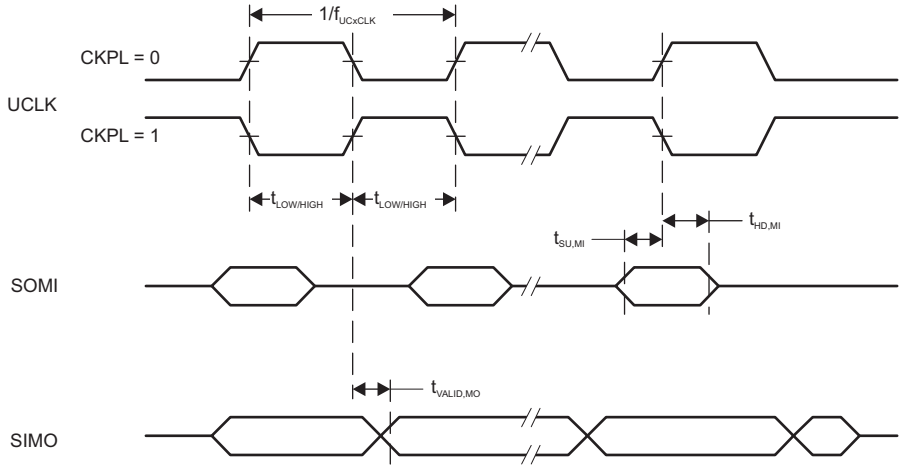


Figure 5-11. SPI Master Mode, CKPH = 1

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Table 5-18 lists the switching characteristics of the eUSCI in SPI slave mode.

Table 5-18. eUSCI (SPI Slave Mode) Switching Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	MAX	UNIT
$t_{STE,LEAD}$	STE lead time, STE active to clock		2.0 V	55		ns
			3.0 V	45		
$t_{STE,LAG}$	STE lag time, last clock to STE inactive		2.0 V	20		ns
			3.0 V	20		
$t_{STE,ACC}$	STE access time, STE active to SOMI data out		2.0 V		65	ns
			3.0 V		40	
$t_{STE,DIS}$	STE disable time, STE inactive to SOMI high impedance		2.0 V		40	ns
			3.0 V		35	
$t_{SU,SI}$	SIMO input data setup time		2.0 V	8		ns
			3.0 V	6		
$t_{HD,SI}$	SIMO input data hold time		2.0 V	12		ns
			3.0 V	12		
$t_{VALID,SO}$	SOMI output data valid time(2)	UCLK edge to SOMI valid, C_L = 20 pF	2.0 V		68	ns
			3.0 V		42	
$t_{HD,SO}$	SOMI output data hold time (3)	C_L = 20 pF	2.0 V	5		ns
			3.0 V	5		

(1) $f_{UCxCLK} = 1/2t_{LO/HI}$ with $t_{LO/HI} \geq \max(t_{VALID,MO(Master)} + t_{SU,SI(eUSCI)}, t_{SU,MI(Master)} + t_{VALID,SO(eUSCI)})$
For the master parameters $t_{SU,MI(Master)}$ and $t_{VALID,MO(Master)}$, see the SPI parameters of the attached master.
(2) Specifies the time to drive the next valid data to the SOMI output after the output changing UCLK clock edge. See the timing diagrams in Figure 5-12 and Figure 5-13.
(3) Specifies how long data on the SOMI output is valid after the output changing UCLK clock edge. See the timing diagrams in Figure 5-12 and Figure 5-13.

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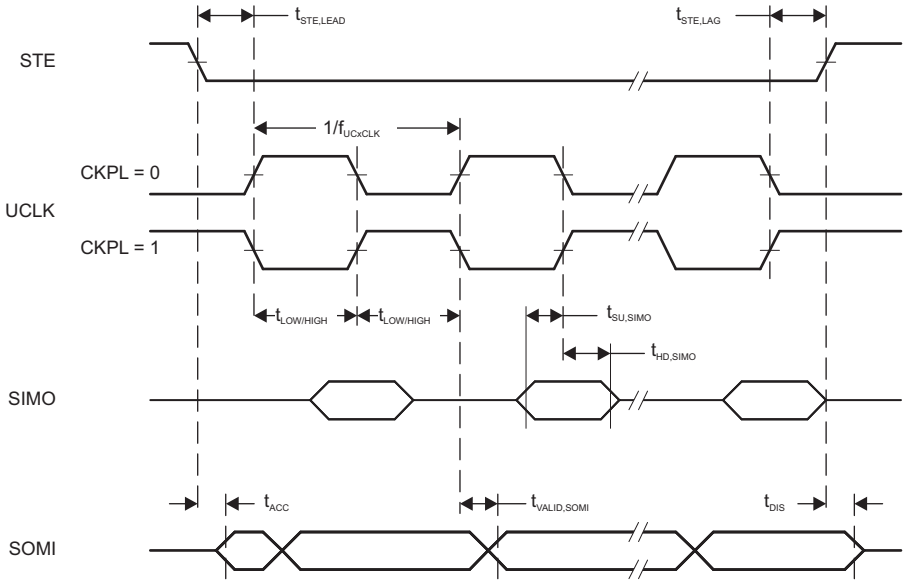


Figure 5-12. SPI Slave Mode, CKPH = 0

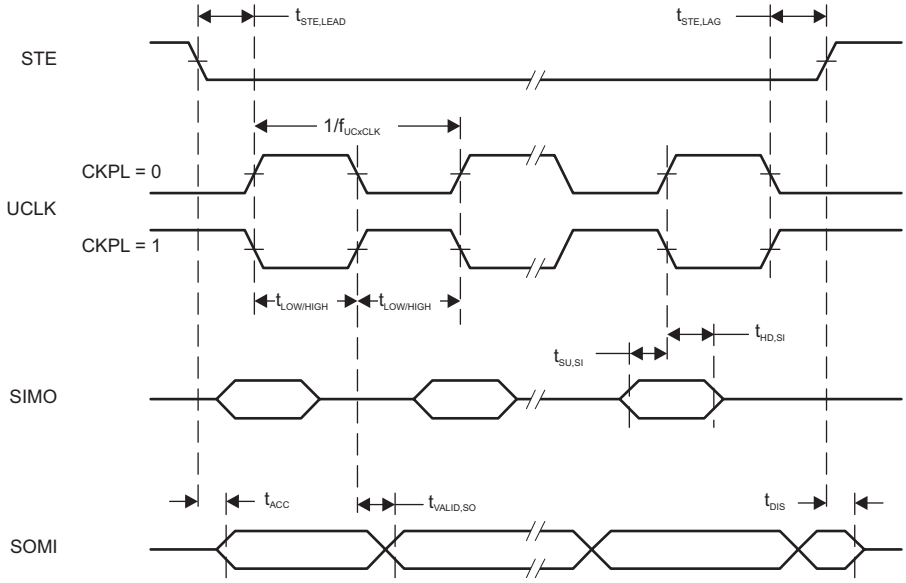


Figure 5-13. SPI Slave Mode, CKPH = 1

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Table 5-19 lists the switching characteristics of the eUSCI (I^2C mode).

Table 5-19. eUSCI (I^2C Mode) Switching Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 5-14)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
f_{eUSCI}	eUSCI input clock frequency	Internal: SMCLK or MODCLK, External: UCLK, Duty cycle = 50% ±10%				16	MHz
f_{SCL}	SCL clock frequency		2.0 V, 3.0 V	0		400	kHz
$t_{HD,STA}$	Hold time (repeated) START	f_{SCL} = 100 kHz	2.0 V, 3.0 V	4.0			µs
		f_{SCL} > 100 kHz		0.6			
$t_{SU,STA}$	Setup time for a repeated START	f_{SCL} = 100 kHz	2.0 V, 3.0 V	4.7			µs
		f_{SCL} > 100 kHz		0.6			
$t_{HD,DAT}$	Data hold time		2.0 V, 3.0 V	0			ns
$t_{SU,DAT}$	Data setup time		2.0 V, 3.0 V	250			ns
$t_{SU,STO}$	Setup time for STOP	f_{SCL} = 100 kHz	2.0 V, 3.0 V	4.0			µs
		f_{SCL} > 100 kHz		0.6			
t_{SP}	Pulse duration of spikes suppressed by input filter	UCGLITx = 0	2.0 V, 3.0 V	50		600	ns
		UCGLITx = 1		25		300	
		UCGLITx = 2		12.5		150	
		UCGLITx = 3		6.3		75	
$t_{TIMEOUT}$	Clock low time-out	UCCLTOx = 1	2.0 V, 3.0 V		27		ms
		UCCLTOx = 2			30		
		UCCLTOx = 3			33		

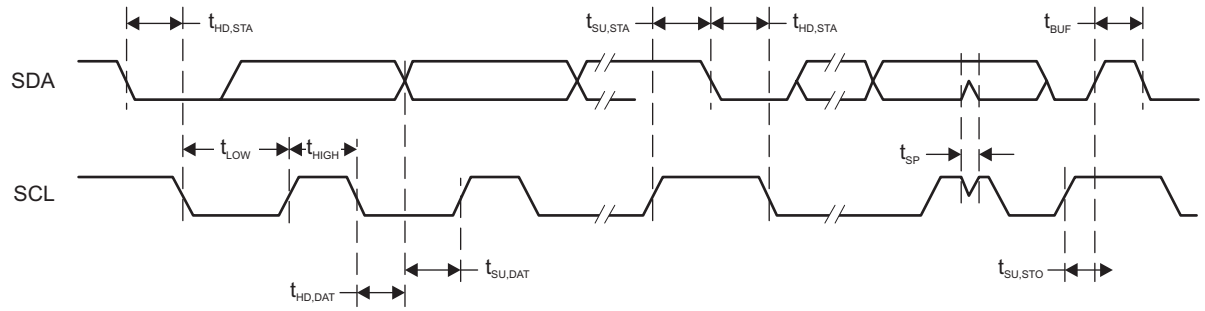


Figure 5-14. I^2C Mode Timing

5.12.8 ADC

Table 5-20 lists the characteristics of the ADC power supply and input range conditions.

Table 5-20. ADC, Power Supply and Input Range Conditions

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
DV_{CC}	ADC supply voltage			2.0		3.6	V
$V_{(Ax)}$	Analog input voltage range	All ADC pins		0		DV_{CC}	V
I_{ADC}	Operating supply current into DVCC terminal, reference current not included, repeat-single-channel mode	f_{ADCCLK} = 5 MHz, ADCON = 1, REFON = 0, SHT0 = 0, SHT1 = 0, ADCDIV = 0, ADCCONSEQx = 10b	2 V		185		µA
			3 V		207		
C_I	Input capacitance	Only one terminal Ax can be selected at one time from the pad to the ADC capacitor array, including wiring and pad	2.2 V		2.5	3.5	pF
$R_{I,MUX}$	Input MUX ON resistance	DV_{CC} = 2 V, 0 V ≤ V_{Ax} ≤ DV_{CC}				2	kΩ
$R_{I,Misc}$	Input miscellaneous resistance				34		kΩ

Table 5-21 lists the ADC 10-bit timing parameters.

Table 5-21. ADC, 10-Bit Timing Parameters

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
f_{ADCCLK}		For specified performance of ADC linearity parameters	2 V to 3.6 V	0.45	5	5.5	MHz
f_{ADCOSC}	Internal ADC oscillator (MODOSC)	ADCDIV = 0, f_{ADCCLK} = f_{ADCOSC}	2 V to 3.6 V	3.8	4.8	5.8	MHz
$t_{CONVERT}$	Conversion time	REFON = 0, Internal oscillator, 10 ADCCLK cycles, 10-bit mode, f_{ADCOSC} = 4.5 MHz to 5.5 MHz	2 V to 3.6 V	2.18		2.67	µs
		External f_{ADCCLK} from ACLK, MCLK, or SMCLK, ADCSSEL ≠ 0	2 V to 3.6 V		12 × 1 / f_{ADCCLK}		
t_{ADCON}	Turn-on settling time of the ADC	The error in a conversion started after t_{ADCON} is less than ±0.5 LSB. Reference and input signal are already settled.				100	ns
t_{Sample}	Sampling time	R_S = 1000 Ω, R_I (1) = 36000 Ω, C_I = 3.5 pF, Approximately 8 Tau (t) are required for an error of less than ±0.5 LSB (2)	2 V	1.5			µs
			3 V	2.0			

(1) $R_I = R_{I,MUX} + R_{I,Misc}$
(2) $t_{Sample} = \ln(2^{n+1}) \times \tau$, where n = ADC resolution, $\tau = (R_I + R_S) \times C_I$

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Table 5-22 lists the ADC 10-bit linearity parameters.

Table 5-22. ADC, 10-Bit Linearity Parameters

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
E_I	Integral linearity error (10-bit mode)	Veref+ reference	2.4 V to 3.6 V	–2		2	LSB
	Integral linearity error (8-bit mode)		2.0 V to 3.6 V	–2		2	
E_D	Differential linearity error (10-bit mode)	Veref+ reference	2.4 V to 3.6 V	–1		1	LSB
	Differential linearity error (8-bit mode)		2.0 V to 3.6 V	–1		1	
E_O	Offset error (10-bit mode)	Veref+ reference	2.4 V to 3.6 V	–6.5		6.5	mV
	Offset error (8-bit mode)		2.0 V to 3.6 V	–6.5		6.5	
E_G	Gain error (10-bit mode)	Veref+ as reference	2.4 V to 3.6 V	–2.0		2.0	LSB
		Internal 1.5-V reference		–3.0%		3.0%	
	Gain error (8-bit mode)	Veref+ as reference	2.0 V to 3.6 V	–2.0		2.0	LSB
		Internal 1.5-V reference		–3.0%		3.0%	
E_T	Total unadjusted error (10-bit mode)	Veref+ as reference	2.4 V to 3.6 V	–2.0		2.0	LSB
		Internal 1.5-V reference		–3.0%		3.0%	
	Total unadjusted error (8-bit mode)	Veref+ as reference	2.0 V to 3.6 V	–2.0		2.0	LSB
		Internal 1.5-V reference		–3.0%		3.0%	
V_{SENSOR}	See (1)	ADCON = 1, INCH = 0Ch, T_A = 0°C	3 V		913		mV
TC_{SENSOR}	See (2)	ADCON = 1, INCH = 0Ch	3 V		3.35		mV/°C
t_{SENSOR} (sample)	Sample time required if channel 12 is selected (3)	ADCON = 1, INCH = 0Ch, Error of conversion result ≤1 LSB, AM and all LPMs above LPM3	3 V	30			µs
		ADCON = 1, INCH = 0Ch, Error of conversion result ≤1 LSB, LPM3	3 V	100			

(1) The temperature sensor offset can vary significantly. TI recommends a single-point calibration to minimize the offset error of the built-in temperature sensor.
(2) The device descriptor structure contains calibration values for 30°C and 85°C for each available reference voltage level. The sensor voltage can be computed as $V_{SENSE} = TC_{SENSOR} \times (\text{Temperature, °C}) + V_{SENSOR}$, where TC_{SENSOR} and V_{SENSOR} can be computed from the calibration values for higher accuracy.
(3) The typical equivalent impedance of the sensor is 700 kΩ. The sample time required includes the sensor on time, $t_{SENSOR(on)}$.

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5.12.9 Enhanced Comparator (eCOMP)

Table 5-23 lists the characteristics of eCOMP0.

Table 5-23. eCOMP0

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{CC}	Supply voltage		2.0		3.6	V
V_{IC}	Common-mode input range		0		V_{CC}	V
V_{HYS}	DC input hysteresis	CPEN = 1, CPHSEL = 00		0		mV
		CPEN = 1, CPHSEL = 01		10		
		CPEN = 1, CPHSEL = 10		20		
		CPEN = 1, CPHSEL = 11		30		
V_{OFFSET}	Input offset voltage	CPEN = 1, CPMSEL = 0	–30		+30	mV
		CPEN = 1, CPMSEL = 1	–40		+40	
I_{COMP}	Quiescent current draw from V_{CC}, only comparator	$V_{IC} = V_{CC} / 2$, CPEN = 1, CPMSEL = 0		24	35	µA
		$V_{IC} = V_{CC} / 2$, CPEN = 1, CPMSEL = 1		1.6	5	
C_{IN}	Input channel capacitance (1)			1		pF
R_{IN}	Input channel series resistance	On (switch closed)		10	20	kΩ
		Off (switch open)	50			MΩ
t_{PD}	Propagation delay, response time	CPMSEL = 0, CPFLT = 0, $V_{IC} = V_{CC} / 2$, Overdrive = 20 mV			1	µs
		CPMSEL = 1, CPFLT = 0, $V_{IC} = V_{CC} / 2$, Overdrive = 20 mV		3.2		
t_{EN_CP}	Comparator enable time	CPEN = 0→1, CPMSEL = 0, V+ and V- from pads, Overdrive = 20 mV		8.5		µs
		CPEN = 0→1, CPMSEL = 1, V+ and V- from pads, Overdrive = 20 mV		1.4		
$t_{EN_CP_DAC}$	Comparator with reference DAC enable time	CPEN = 0→1, CPDACEN = 0→1, CPMSEL = 0, CPDACREFS = 1, CPDACBUF1 = 0F, Overdrive = 20 mV		8.5		µs
		CPEN = 0→1, CPDACEN = 0→1, CPMSEL = 1, CPDACREFS = 1, CPDACBUF1 = 0F, Overdrive = 20 mV		101		
t_{FDLY}	Propagation delay with analog filter active	CPMSEL = 0, CPFLTDY = 00, Overdrive = 20 mV, CPFLT = 1		0.7		µs
		CPMSEL = 0, CPFLTDY = 01, Overdrive = 20 mV, CPFLT = 1		1.1		
		CPMSEL = 0, CPFLTDY = 10, Overdrive = 20 mV, CPFLT = 1		1.9		
		CPMSEL = 0, CPFLTDY = 11, Overdrive = 20 mV, CPFLT = 1		3.4		
INL	Integral nonlinearity		–0.5		0.5	LSB
DNL	Differential nonlinearity		–0.5		0.5	LSB

(1) eCOMP C_{IN}, model, see Figure 5-15 for details.

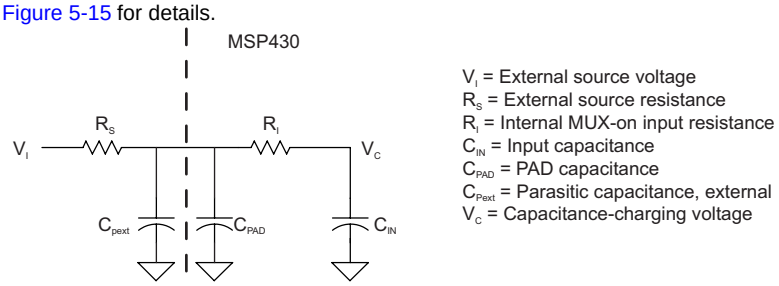


Figure 5-15. eCOMP Input Circuit

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5.12.10 Smart Analog Combo (SAC)

Table 5-24 lists the characteristics of SAC0 (SAC-L1, OA).

Table 5-24. SAC0 (SAC-L1, OA)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{CC}	Supply voltage		2.0		3.6	V
V_{OS}	Input offset voltage		–5		5	mV
dV_{OS}/dT	Offset drift	OAPM = 0		3		µV/°C
		OAPM = 1		5		
I_B	Input bias current			50		pA
V_{CM}	Input voltage range		–0.1		V_{CC} + 0.1	V
I_{IDD}	Quiescent current	OAPM = 0		350		µA
		OAPM = 1		120		
E_{NI}	Input noise voltage, f = 0.1 Hz to 10 Hz	Vin = V_{CC} / 2, OAPM = 0		40		µV
	Input noise voltage density, f = 1 kHz	Vin = V_{CC} / 2, OAPM = 0		40		nV/√Hz
	Input noise voltage, f = 10 kHz	Vin = V_{CC} / 2, OAPM = 0		20		
CMRR	Common-mode rejection ratio	OAPM = 0		70		dB
		OAPM = 1		80		
PSRR	Power supply rejection ratio	OAPM = 0		70		dB
		OAPM = 1		80		
GBW	Gain bandwidth	OAPM = 0		4		MHz
		OAPM = 1		1.4		
A_{OL}	Open-loop voltage gain	OAPM = 0		100		dB
		OAPM = 1		100		
φ_M	Phase margin	C_L = 50 pF , R_L = 2 kΩ		65		deg
	Positive slew rate	C_L = 50 pF, OAPM = 0		3		V/us
		C_L = 50 pF, OAPM = 1		1		
C_{in}	Input capacitance	Common mode		2		pF
V_O	Voltage output swing from supply rails	R_L = 10 kΩ		40	100	mV
t_{ST}	OA settling time	To 0.1% final value, G = +1, 1-V setup, C_L = 50 pF, OAPM = 0		1		µs
		To 0.1% final value, G = +1, 1-V setup, C_L = 50 pF, OAPM = 1		4.5		

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5.12.11 Transimpedance Amplifier (TIA)

Table 5-25 lists the characteristics of TIA0.

Table 5-25. TIA0

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{CC}	Supply voltage		2.0		3.6	V
V_{OS}	Input offset voltage		–5		5	mV
dV_{OS}/dT	Offset drift	TRIPM = 0		3		µV/°C
		TRIPM = 1		5		
I_B	Input bias current	V_B = 0 V, TSSOP-16 package with OA-dedicated pin input (see Figure 4-2)		5		pA
		TSSOP-20 and VQFN-16 packages		50		pA
V_{CM}	Input voltage range		–0.1		V_{CC} / 2	V
I_{IDD}	Quiescent current	TRIPM = 0		350		µA
		TRIPM = 1		120		
E_{NI}	Input noise voltage, f = 0.1 Hz to 10 Hz	Vin = V_{CC} / 2, TRIPM = 0		40		µV
	Input noise voltage density, f = 1 kHz	Vin = V_{CC} / 2, TRIPM = 0		40		nV/√Hz
	Input noise voltage, f = 10 kHz	Vin = V_{CC} / 2, TRIPM = 0		16		
CMRR	Common-mode rejection ratio	TRIPM = 0		80		dB
		TRIPM = 1		70		
PSRR	Power supply rejection ratio	TRIPM = 0		80		dB
		TRIPM = 1		70		
GBW	Gain bandwidth	TRIPM = 0		5		MHz
		TRIPM = 1		1.8		
A_{OL}	Open-loop voltage gain	TRIPM = 0		100		dB
		TRIPM = 1		100		
φ_M	Phase margin	C_L = 50 pF , R_L = 2 kΩ, TRIPM = 0		40		deg
		C_L = 50 pF , R_L = 2 kΩ, TRIPM = 1		70		
	Positive slew rate	C_L = 50 pF, TRIPM = 0		4		V/µs
		C_L = 50 pF, TRIPM = 1		1		
C_{in}	Input capacitance	Common mode		7		pF
V_O	Voltage output swing from supply rails	R_L = 10 kΩ		40	100	mV
t_{ST}	TIA settling time	To 0.1% final value, G = +1, 1-V setup, C_L = 50 pF, TRIPM = 0		3		µs
		To 0.1% final value, G = +1, 1-V setup, C_L = 50 pF, TRIPM = 1		5		

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5.12.12 FRAM

Table 5-26 lists the characteristics of the FRAM.

Table 5-26. FRAM

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Read and write endurance		10^{15}			cycles
$t_{Retention}$	Data retention duration	T_J = 25°C	100			years
		T_J= 70°C	40			
		T_J= 85°C	10			
I_{WRITE}	Current to write into FRAM			I_{READ} (1)		nA
I_{ERASE}	Erase current			N/A (2)		nA
t_{WRITE}	Write time			t_{READ} (3)		ns
t_{READ}	Read time	NWAITSx = 0		$1/f_{SYSTEM}$ (4)		ns
		NWAITSx = 1		$2/f_{SYSTEM}$ (4)		

(1) Writing to FRAM does not require a setup sequence or additional power when compared to reading from FRAM. The FRAM read current I_{READ} is included in the active mode current consumption numbers $I_{AM, FRAM}$.
(2) FRAM does not require a special erase sequence.
(3) Writing into FRAM is as fast as reading.
(4) The maximum read (and write) speed is specified by f_{SYSTEM} using the appropriate wait state settings (NWAITSx).

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5.12.13 Emulation and Debug

Table 5-27 lists the characteristics of the 2-wire Spy-Bi-Wire interface.

Table 5-27. JTAG, Spy-Bi-Wire Interface

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 5-16)

PARAMETER		V_{CC}	MIN	TYP	MAX	UNIT
f_{SBW}	Spy-Bi-Wire input frequency	2.0 V, 3.0 V	0		8	MHz
$t_{SBW,Low}$	Spy-Bi-Wire low clock pulse duration	2.0 V, 3.0 V	0.028		15	µs
$t_{SU,SBWTDIO}$	SBWTDIO setup time (before falling edge of SBWTCK in TMS and TDI slot Spy-Bi-Wire)	2.0 V, 3.0 V	4			ns
$t_{HD,SBWTDIO}$	SBWTDIO hold time (after rising edge of SBWTCK in TMS and TDI slot Spy-Bi-Wire)	2.0 V, 3.0 V	19			ns
$t_{Valid,SBWTDIO}$	SBWTDIO data valid time (after falling edge of SBWTCK in TDO slot Spy-Bi-Wire)	2.0 V, 3.0 V			31	ns
$t_{SBW,\ En}$	Spy-Bi-Wire enable time (TEST high to acceptance of first clock edge) (1)	2.0 V, 3.0 V			110	µs
$t_{SBW,Ret}$	Spy-Bi-Wire return to normal operation time(2)		15		100	µs
$R_{internal}$	Internal pulldown resistance on TEST	2.0 V, 3.0 V	20	35	50	kΩ

(1) Tools that access the Spy-Bi-Wire interface must wait for the $t_{SBW,En}$ time after pulling the TEST/SBWTCK pin high before applying the first SBWTCK clock edge.
(2) Maximum $t_{SBW,Rst}$ time after pulling or releasing the TEST/SBWTCK pin low, the Spy-Bi-Wire pins revert from their Spy-Bi-Wire function to their application function. This time applies only if the Spy-Bi-Wire mode was selected.

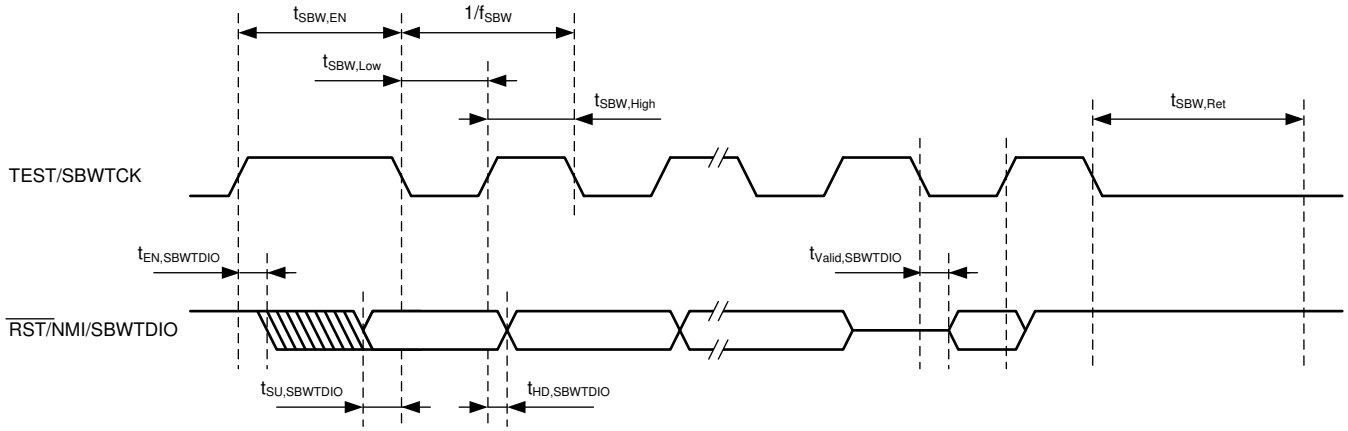


Figure 5-16. JTAG Spy-Bi-Wire Timing

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Table 5-28 lists the characteristics of the JTAG 4-wire interface.

Table 5-28. JTAG, 4-Wire Interface

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 5-17)

PARAMETER		V_{CC}	MIN	TYP	MAX	UNIT
f_{TCK}	TCK input frequency (1)	2.0 V, 3.0 V	0		10	MHz
$t_{TCK,Low}$	Spy-Bi-Wire low clock pulse duration	2.0 V, 3.0 V	15			ns
$t_{TCK,high}$	Spy-Bi-Wire high clock pulse duration	2.0 V, 3.0 V	15			ns
$t_{SU,TMS}$	TMS setup time (before rising edge of TCK)	2.0 V, 3.0 V	11			ns
$t_{HD,TMS}$	TMS hold time (after rising edge of TCK)	2.0 V, 3.0 V	3			ns
$t_{SU,TDI}$	TDI setup time (before rising edge of TCK)	2.0 V, 3.0 V	13			ns
$t_{HD,TDI}$	TDI hold time (after rising edge of TCK)	2.0 V, 3.0 V	5			ns
$t_{z\text{-}Valid,TDO}$	TDO high impedance to valid output time (after falling edge of TCK)	2.0 V, 3.0 V			26	ns
$t_{Valid,TDO}$	TDO to new valid output time (after falling edge of TCK)	2.0 V, 3.0 V			26	ns
$t_{Valid\text{-}Z,TDO}$	TDO valid to high-impedance output time (after falling edge of TCK)	2.0 V, 3.0 V			26	ns
$t_{JTAG,Ret}$	Spy-Bi-Wire return to normal operation time		15		100	µs
$R_{internal}$	Internal pulldown resistance on TEST	2.0 V, 3.0 V	20	35	50	kΩ

(1) Tools that access the Spy-Bi-Wire interface must wait for the $t_{SBW,En}$ time after pulling the TEST/SBWTCK pin high before applying the first SBWTCK clock edge.

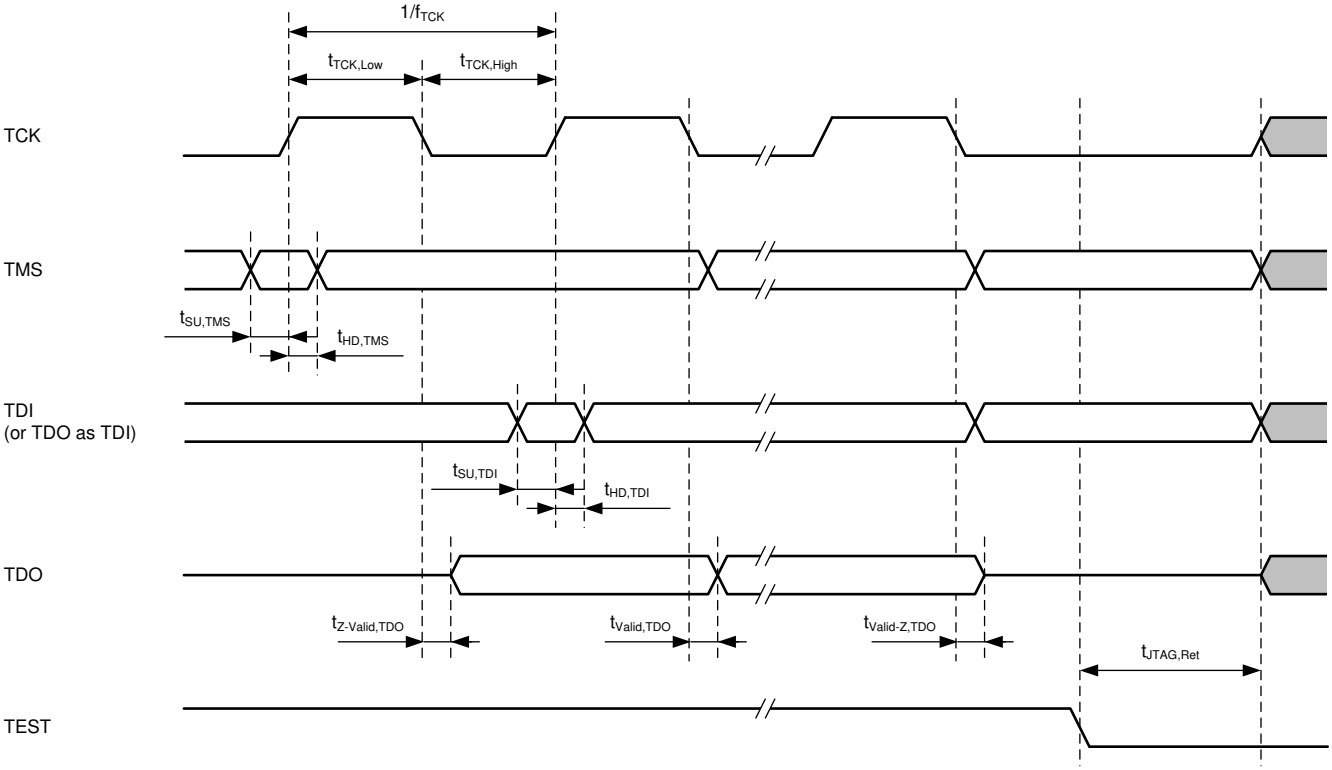


Figure 5-17. JTAG 4-Wire Timing

6 Detailed Description

6.1 Overview

The MSP430FR231x FRAM MCU features a powerful 16-bit RISC CPU, 16-bit registers, and constant generators that contribute to maximum code efficiency. The DCO also allows the device to wake up from low-power modes to active mode typically in less than 10 µs. The feature set of this microcontroller is ideal for applications ranging from smoke detectors to portable health and fitness accessories.

6.2 CPU

The MSP430 CPU has a 16-bit RISC architecture that is highly transparent to the application. All operations, other than program-flow instructions, are performed as register operations in conjunction with seven addressing modes for source operand and four addressing modes for destination operand.

The CPU is integrated with 16 registers that provide reduced instruction execution time. The register-to-register operation execution time is one cycle of the CPU clock.

Four of the registers, R0 to R3, are dedicated as program counter (PC), stack pointer (SP), status register (SR), and constant generator (CG), respectively. The remaining registers are general-purpose registers.

Peripherals are connected to the CPU using data, address, and control buses, and can be handled with all instructions.

6.3 Operating Modes

The MSP430 has one active mode and several software-selectable low-power modes of operation (see Table 6-1). An interrupt event can wake up the device from low-power mode (LPM0, LPM3, or LPM4), service the request, and restore back to the low-power mode on return from the interrupt program. Low-power modes LPM3.5 and LPM4.5 disable the core supply to minimize power consumption.

Table 6-1. Operating Modes

MODE		AM	LPM0	LPM3	LPM4	LPM3.5	LPM4.5
		ACTIVE MODE	CPU OFF	STANDBY	OFF	ONLY RTC COUNTER	SHUTDOWN
Maximum system clock		16 MHz	16 MHz	40 kHz	0	40 kHz	0
Power consumption at 25°C, 3 V		126 µA/MHz	40 µA/MHz	1.11 µA with RTC counter only in LFXT	0.45 µA without SVS	0.71 µA with RTC counter only in LFXT	32 nA without SVS
Wake-up time		N/A	instant	10 µs	10 µs	350 µs	350 µs
Wake-up events		N/A	All	All	I/O	RTC Counter I/O	I/O
Power	Regulator	Full Regulation	Full Regulation	Partial Power Down	Partial Power Down	Partial Power Down	Power Down
	SVS	On	On	Optional	Optional	Optional	Optional
	Brownout	On	On	On	On	On	On

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Table 6-1. Operating Modes (continued)

MODE		AM	LPM0	LPM3	LPM4	LPM3.5	LPM4.5
		ACTIVE MODE	CPU OFF	STANDBY	OFF	ONLY RTC COUNTER	SHUTDOWN
Clock[1]	MCLK	Active	Off	Off	Off	Off	Off
	SMCLK	Optional	Optional	Off	Off	Off	Off
	FLL	Optional	Optional	Off	Off	Off	Off
	DCO	Optional	Optional	Off	Off	Off	Off
	MODCLK	Optional	Optional	Off	Off	Off	Off
	REFO	Optional	Optional	Optional	Off	Off	Off
	ACLK	Optional	Optional	Optional	Off	Off	Off
	XT1HFCLK[2]	Optional	Optional	Off	Off	Off	Off
	XT1LFCLK	Optional	Optional	Optional	Off[3]	Optional	Off
	VLOCLK	Optional	Optional	Optional	Off[3]	Optional	Off
Core	CPU	On	Off	Off	Off	Off	Off
	FRAM	On	On	Off	Off	Off	Off
	RAM	On	On	On	On	Off	Off
	Backup Memory[4]	On	On	On	On	On	Off
Peripherals	Timer0_B3	Optional	Optional	Optional	Off	Off	Off
	Timer1_B3	Optional	Optional	Optional	Off	Off	Off
	WDT	Optional	Optional	Optional	Off	Off	Off
	eUSCI_A0	Optional	Optional	Optional	Off	Off	Off
	eUSCI_B0	Optional	Optional	Optional	Off	Off	Off
	CRC	Optional	Optional	Off	Off	Off	Off
	ADC	Optional	Optional	Optional	Off	Off	Off
	eCOMP	Optional	Optional	Optional	Optional	Off	Off
	TIA	Optional	Optional	Optional	Optional	Off	Off
	SAC0	Optional	Optional	Optional	Optional	Off	Off
	RTC Counter	Optional	Optional	Optional	Off	Optional	Off
I/O	General Digital Input/Output	On	Optional	State Held	State Held	State Held	State Held
	Capacitive Touch I/O	Optional	Optional	Optional	Off	Off	Off

(1) The status shown for LPM4 applies to internal clocks only.
(2) HFXT must be disabled before entering into LPM3, LPM4, or LPMx.5 mode.
(3) Refer to following NOTE for details info as below.
(4) Backup memory contains one 32-byte register in the peripheral memory space. See Table 6-23 and Table 6-38 for the memory allocation of backup memory.

NOTE

XT1CLK and VLOCLK can be active during LPM4 if requested by low-frequency peripherals.

6.4 Interrupt Vector Addresses

The interrupt vectors and the power-up start address are in the address range 0FFFFh to 0FF80h (see Table 6-2). The vector contains the 16-bit address of the interrupt-handler instruction sequence.

Table 6-2. Interrupt Sources, Flags, and Vectors

INTERRUPT SOURCE	INTERRUPT FLAG	SYSTEM INTERRUPT	WORD ADDRESS	PRIORITY
System Reset Power-up, Brownout, Supply Supervisor External Reset RST Watchdog Time-out, Key Violation FRAM uncorrectable bit error detection Software POR, BOR FLL unlock error	SVSHIFG PMMRSTIFG WDTIFG PMMPORIFG, PMMBORIFG SYSRSTIV FLLULPUC	Reset	FFFEh	63, Highest
System NMI Vacant Memory Access JTAG Mailbox FRAM access time error FRAM bit error detection	VMAIFG JMBINIFG, JMBOUTIFG CBDIFG, UBDIFG	(Non)maskable	FFFCh	62
User NMI External NMI Oscillator Fault	NMIIFG OFIFG	(Non)maskable	FFFAh	61
Timer0_B3	TB0CCR0 CCIFG0	Maskable	FFF8h	60
Timer0_B3	TB0CCR1 CCIFG1, TB0CCR2 CCIFG2, TB0IFG (TB0IV)	Maskable	FFF6h	59
Timer1_B3	TB1CCR0 CCIFG0	Maskable	FFF4h	58
Timer1_B3	TB1CCR1 CCIFG1, TB1CCR2 CCIFG2, TB1IFG (TB1IV)	Maskable	FFF2h	57
RTC Counter	RTCIFG	Maskable	FFF0h	56
Watchdog Timer Interval mode	WDTIFG	Maskable	FFEEh	55
eUSCI_A0 Receive or Transmit	UCTXCPTIFG, UCSTTIFG, UCRXIFG, UCTXIFG (UART mode) UCRXIFG, UCTXIFG (SPI mode) (UCA0IV))	Maskable	FFECh	54
eUSCI_B0 Receive or Transmit	UCB0RXIFG, UCB0TXIFG (SPI mode) UCALIFG, UCNACKIFG, UCSTTIFG, UCSTPIFG, UCRXIFG0, UCTXIFG0, UCRXIFG1, UCTXIFG1, UCRXIFG2, UCTXIFG2, UCRXIFG3, UCTXIFG3, UCCNTIFG, UCBIT9IFG,UCCLTOIFG(I^2C mode) (UCB0IV)	Maskable	FFEAh	53
ADC	ADCIFG0, ADCINIFG, ADCLOIFG, ADCHIIFG, ADCTOVIFG, ADCOVIFG (ADCIV)	Maskable	FFE8h	52
P1	P1IFG.0 to P1IFG.7 (P1IV)	Maskable	FFE6h	51
P2	P2IFG.0 to P2IFG.7 (P2IV)(1)	Maskable	FFE4h	50
eCOMP	CPIIFG, CPIFG (CPIV)	Maskable	FFE2h	49
Reserved	Reserved	Maskable	FFE0h to FF88h	

(1) P2.0, P2.1, P2.6, and P2.7 support both pin and software interrupts. Others ports support software interrupts only.

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Table 6-2. Interrupt Sources, Flags, and Vectors (continued)

INTERRUPT SOURCE	INTERRUPT FLAG	SYSTEM INTERRUPT	WORD ADDRESS	PRIORITY
Signatures	BSL Signature 2		0FF86h	
	BSL Signature 1		0FF84h	
	JTAG Signature 2		0FF82h	
	JTAG Signature 1		0FF80h	

6.5 Memory Organization

Table 6-3 summarizes the memory map of the MSP430FR231x MCUs.

Table 6-3. Memory Organization

	ACCESS	MSP430FR2311	MSP430FR2310
Memory (FRAM) Main: interrupt vectors and signatures Main: code memory	Read/Write (Optional Write Protect)(1)	3.75KB FFFFh to FF80h FFFFh to F100h	2KB FFFFh to FF80h FFFFh to F800h
RAM	Read/Write	1KB 23FFh to 2000h	1KB 23FFh to 2000h
Bootloader (BSL1) Memory (ROM) (TI Internal Use)	Read only	2KB 17FFh to 1000h	2KB 17FFh to 1000h
Bootloader (BSL2) Memory (ROM) (TI Internal Use)	Read only	1KB FFFFFh to FFC00h	1KB FFFFFh to FFC00h
Peripherals	Read/Write	4KB 0FFFh to 0000h	4KB 0FFFh to 0000h

(1) The Program FRAM can be write protected by setting the PFWP bit in the SYSCFG0 register. See the *System Resets, Interrupts, and Operating Modes, System Control Module (SYS)* chapter in the *MSP430FR4xx and MSP430FR2xx Family User's Guide* for more details

6.6 Bootloader (BSL)

The BSL lets users program the FRAM or RAM using a UART or I^2C serial interface. Access to the device memory through the BSL is protected by a user-defined password. Use of the BSL requires four pins (see Table 6-4 and Table 6-5). BSL entry requires a specific entry sequence on the $\overline{\text{RST}}$/NMI/SBWTDIO and TEST/SBWTCK pins.

This device supports blank device detection to automatically invoke the BSL and skip the special entry sequence, which saves time and simplifies onboard programming. For complete description of the features of the BSL and its implementation, see *MSP430 FRAM Device Bootloader (BSL) User's Guide*.

Table 6-4. UART BSL Pin Requirements and Functions

DEVICE SIGNAL	BSL FUNCTION
$\overline{\text{RST}}$/NMI/SBWTDIO	Entry sequence signal
TEST/SBWTCK	Entry sequence signal
P1.7	Data transmit
P1.6	Data receive
V_{CC}	Power supply
VSS	Ground supply

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Table 6-5. I²C BSL Pin Requirements and Functions

DEVICE SIGNAL	BSL FUNCTION
$\overline{\text{RST}}$/NMI/SBWTDIO	Entry sequence signal
TEST/SBWTCK	Entry sequence signal
P1.2	Data receive and transmit
P1.3	Clock
V_{CC}	Power supply
VSS	Ground supply

6.7 JTAG Standard Interface

The MSP430 family supports the standard JTAG interface which requires four signals for sending and receiving data. The JTAG signals are shared with general-purpose I/O. The TEST/SBWTCK pin enables the JTAG signals. In addition to these signals, the $\overline{\text{RST}}$/NMI/SBWTDIO pin interfaces with MSP430 development tools and device programmers. Table 6-6 lists the JTAG pin requirements. For further details on interfacing to development tools and device programmers, see the *MSP430 Hardware Tools User's Guide*.

Table 6-6. JTAG Pin Requirements and Function

DEVICE SIGNAL	DIRECTION	JTAG FUNCTION
P1.4/UCA0STE/TCK/OA0+/A4	IN	JTAG clock input
P1.5/UCA0CLK/TMS/TRI0O/A5	IN	JTAG state control
P1.6/UCA0RXD/UCA0SOMI/TB0.1/TDI/TCLK/TRI0-/A6	IN	JTAG data input and TCLK input
P1.7/UCA0TXD/UCA0SIMO/TB0.2/TDO/TRI0+/A7/VREF+	OUT	JTAG data output
TEST/SBWTCK	IN	Enable JTAG pins
RST/NMI/SBWTDIO	IN	External reset
V_{CC}		Power supply
VSS		Ground supply

6.8 Spy-Bi-Wire Interface (SBW)

The MSP430 family supports the 2-wire Spy-Bi-Wire interface. Spy-Bi-Wire can be used to interface with MSP430 development tools and device programmers. Table 6-7 lists the Spy-Bi-Wire interface pin requirements. For further details on interfacing to development tools and device programmers, see the *MSP430 Hardware Tools User's Guide*.

Table 6-7. Spy-Bi-Wire Pin Requirements and Functions

DEVICE SIGNAL	DIRECTION	SBW FUNCTION
TEST/SBWTCK	IN	Spy-Bi-Wire clock input
RST/NMI/SBWTDIO	IN, OUT	Spy-Bi-Wire data input and output
V_{CC}	–	Power supply
VSS	–	Ground supply

6.9 FRAM

The FRAM can be programmed using the JTAG port, Spy-Bi-Wire (SBW), the BSL, or in system by the CPU. Features of the FRAM include:

- Byte and word access capability
- Programmable wait state generation
- Error correction coding (ECC)

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6.10 Memory Protection

The device features memory protection of user access authority and write protection include:

- Securing the whole memory map to prevent unauthorized access from JTAG port or BSL, by writing JTAG and BSL signatures using the JTAG port, SBW, the BSL, or in system by the CPU.
- Write protection enabled to prevent unwanted write operation to FRAM contents by setting the control bits with accordingly password in System Configuration register 0. For more detailed information, see the *System Resets, Interrupts, and Operating Modes, System Control Module (SYS)* chapter in the *MSP430FR4xx and MSP430FR2xx Family User's Guide*.

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6.11 Peripherals

Peripherals are connected to the CPU through data, address, and control buses. All peripherals can be handled by using all instructions in the memory map. For complete module description, see the *MSP430FR4xx and MSP430FR2xx Family User's Guide*.

6.11.1 Power-Management Module (PMM) and On-chip Reference Voltages

The PMM includes an integrated voltage regulator that supplies the core voltage to the device. The PMM also includes supply voltage supervisor (SVS) and brownout protection. The brownout reset circuit (BOR) is implemented to provide the proper internal reset signal to the device during power on and power off. The SVS circuitry detects if the supply voltage drops below a user-selectable safe level. SVS circuitry is available on the primary supply.

The device contains two on-chip reference: 1.5 V for internal reference and 1.2 V for external reference.

The 1.5-V reference is internally connected to ADC channel 13. DVCC is internally connected to ADC channel 15. When DVCC is set as the reference voltage for ADC conversion, the DVCC can be easily represent as Equation 1 by using ADC sampling 1.5-V reference without any external components support.

$$DVCC = (1023 \times 1.5\ V) \div 1.5\text{-V reference ADC result} \quad (1)$$

The 1.5-V reference is also internally connected to the Comparator built-in DAC as reference voltage. DVCC is internally connected to another source of DAC reference, and both are controlled by the CPDACREFS bit. For more detailed information, see the *Enhanced Comparator (eCOMP)* chapter of the *MSP430FR4xx and MSP430FR2xx Family User's Guide*.

A 1.2-V reference voltage can be buffered, when EXTREFEN = 1 on PMMCTL2 register, and it can be output to P1.7/UCA0TXD/UCA0SIMO/TB0.2/TDO/TRI0+/A7/VREF+ , meanwhile the ADC channel 7 can also be selected to monitor this voltage. For more detailed information, see the *MSP430FR4xx and MSP430FR2xx Family User's Guide*.

6.11.2 Clock System (CS) and Clock Distribution

The clock system includes a 32-kHz low-frequency oscillator (XT1 low frequency) or up to a 16-MHz high-frequency crystal oscillator (XT1 high frequency), an internal very low-power low-frequency oscillator (VLO), an integrated 32-kHz RC oscillator (REFO), an integrated internal digitally controlled oscillator (DCO) that can use frequency-locked loop (FLL) locking with internal or external 32-kHz reference clock, and on-chip asynchronous high-speed clock (MODOSC). The clock system is designed to target cost-effective designs with minimal external components. A fail-safe mechanism is designed for XT1. The clock system module offers the following clock signals.

- Main Clock (MCLK): system clock used by the CPU and all relevant peripherals accessed by the bus. All clock sources except MODOSC can be selected as the source with a predivider of 1, 2, 4, 8, 16, 32, 64, or 128.
- Sub-Main Clock (SMCLK): subsystem clock used by the peripheral modules. SMCLK derives from the MCLK with a predivider of 1, 2, 4, or 8. This means SMCLK is always equal to or less than MCLK.
- Auxiliary Clock (ACLK): derived from the external XT1 clock or internal REFO clock up to 40 kHz.

All peripherals may have one or several clock sources depending on specific functionality. Table 6-8 and Table 6-9 show the clock distribution used in this device.

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Table 6-8. Clock Distribution

	CLOCK SOURCE SELECT BITS(1)	MCLK	SMCLK	ACLK	MODCLK	VLOCLK	EXTERNAL PIN
Frequency Range		DC to 16 MHz	DC to 16 MHz	DC to 40 kHz	5 MHz ±10%	10 kHz ±50%	–
CPU	N/A	Default	–	–	–	–	–
FRAM	N/A	Default	–	–	–	–	–
RAM	N/A	Default	–	–	–	–	–
CRC	N/A	Default	–	–	–	–	–
I/O	N/A	Default	–	–	–	–	
TB0	TBSSEL	–	10b	01b	–	–	00b (TB0CLK pin)
TB1	TBSSEL	–	10b	01b	–	–	00b (TB1CLK pin)
eUSCI_A0	UCSSEL	–	10b or 11b	01b	–	–	00b (UCA0CLK pin)
eUSCI_B0	UCSSEL	–	10b or 11b	01b	–	–	00b (UCB0CLK pin)
WDT	WDTSSEL	–	00b	01b	–	10b	–
ADC	ADCSSEL	–	10b or 11b	01b	00b	–	–
RTC	RTCSS	–	01b(2)	01b(2)	–	11b	–

(1) N/A = not applicable
(2) Controlled by the RTCCKSEL bit in the SYSCFG2 register.

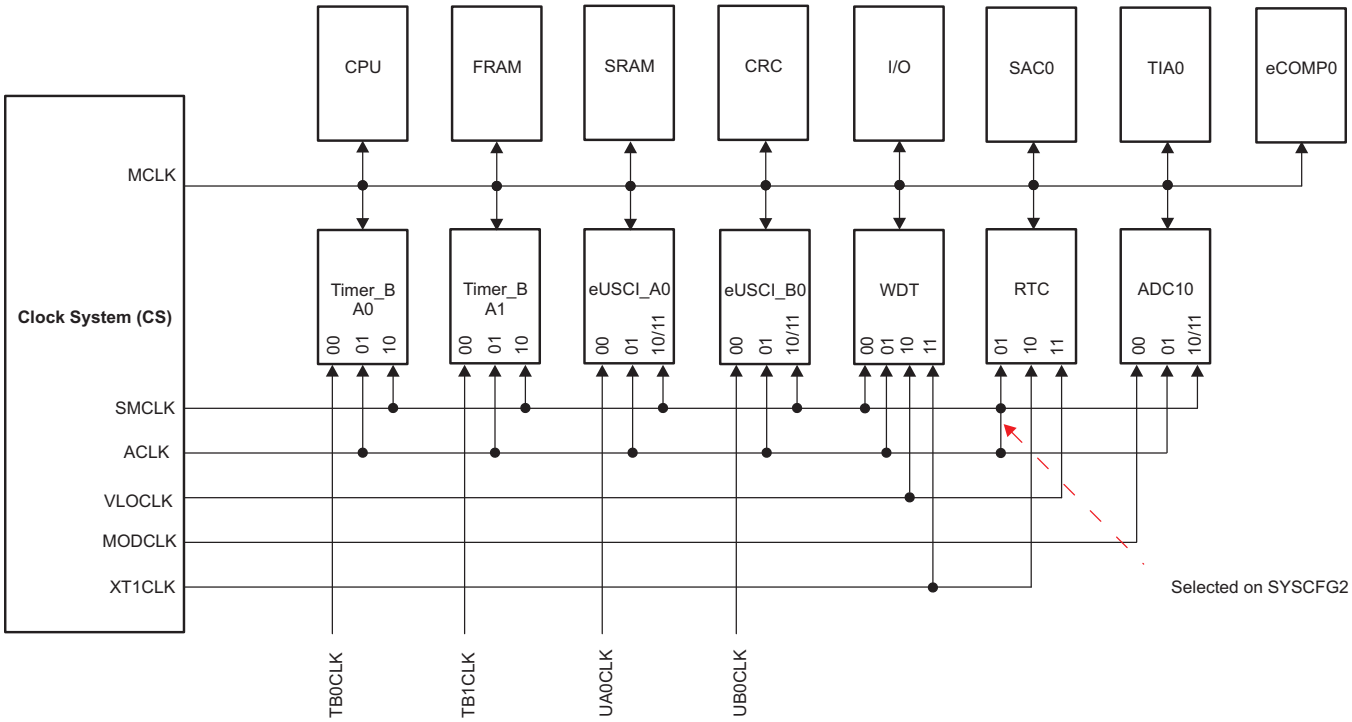


Figure 6-1. Clock Distribution Block Diagram

Table 6-9. XTCLK Distribution

OPERATION MODE	CLOCK SOURCE SELECT BITS	XTHFCLK	XTLFCLK	XTLFCLK (LPMx.5)
		AM TO LPM0	AM TO LPM3	AM TO LPM3.5
MCLK	SELMS	10b	10b	10b
SMCLK	SELMS	10b	10b	10b
REFO	SELREF	0b	0b	0b
ACLK	SELA	0b	0b	0b
RTC	RTCSS	–	10b	10b

6.11.3 General-Purpose Input/Output Port (I/O)

There are up to 16 I/O ports implemented.

- P1 and P2 are full 8-bit ports.
- All individual I/O bits are independently programmable.
- Any combination of input and output is possible for P1 and P2. All inputs of P1 and four inputs of P2 (P2.0, P2.1, P2.6, P2.7) can be configured for interrupt input.
- Programmable pullup or pulldown on all ports.
- All inputs of P1 and four inputs of P2 (P2.0, P2.1, P2.6, P2.7) can be configured for edge-selectable interrupt and for LPM3.5, LPM4, and LPM4.5 wake-up input capability.
- Read and write access to port-control registers is supported by all instructions.
- Ports can be accessed byte-wise or word-wise in pairs.
- Capacitive Touch I/O functionality is supported on all pins.

NOTE

Configuration of digital I/Os after BOR reset

To prevent any cross currents during start-up of the device, all port pins are high-impedance with Schmitt triggers and module functions disabled. To enable the I/O functions after a BOR reset, the ports must be configured first and then the LOCKLPM5 bit must be cleared. For details, see the *Configuration After Reset* section in the *Digital I/O* chapter of the *MSP430FR4xx and MSP430FR2xx Family User's Guide*.

6.11.4 Watchdog Timer (WDT)

The primary function of the WDT module is to perform a controlled system restart after a software problem occurs. If the selected time interval expires, a system reset is generated. If the watchdog function is not needed in an application, the module can be configured as interval timer and can generate interrupts at selected time intervals.

Table 6-10. WDT Clocks

WDTSSEL	NORMAL OPERATION (WATCHDOG AND INTERVAL TIMER MODE)
00	SMCLK
01	ACLK
10	VLOCLK
11	Reserved

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6.11.5 System Module (SYS)

The SYS module handles many of the system functions within the device. These system functions include power-on reset (POR) and power-up clear (PUC) handling, NMI source selection and management, reset interrupt vector generators, bootloader entry mechanisms, and configuration management (device descriptors) (see Table 6-11). SYS also includes a data exchange mechanism through SBW called a JTAG mailbox that can be used in the application.

Table 6-11. System Module Interrupt Vector Registers

INTERRUPT VECTOR REGISTER	ADDRESS	INTERRUPT EVENT	VALUE	PRIORITY
SYSRSTIV, System Reset	015Eh	No interrupt pending	00h	
		Brownout (BOR)	02h	Highest
		RSTIFG $\overline{\text{RST}}$/NMI (BOR)	04h	
		PMMSWBOR software BOR (BOR)	06h	
		LPMx.5 wakeup (BOR)	08h	
		Security violation (BOR)	0Ah	
		Reserved	0Ch	
		SVSHIFG SVSH event (BOR)	0Eh	
		Reserved	10h	
		Reserved	12h	
		PMMSWPOR software POR (POR)	14h	
		WDTIFG watchdog time-out (PUC)	16h	
		WDTPW password violation (PUC)	18h	
		FRCTLPW password violation (PUC)	1Ah	
		Uncorrectable FRAM bit error detection	1Ch	
		Peripheral area fetch (PUC)	1Eh	
		PMMPW PMM password violation (PUC)	20h	
		Reserved	22h	
		FLL unlock (PUC)	24h	
		Reserved	26h to 3Eh	Lowest
SYSSNIV, System NMI	015Ch	No interrupt pending	00h	
		SVS low-power reset entry	02h	Highest
		Uncorrectable FRAM bit error detection	04h	
		Reserved	06h	
		Reserved	08h	
		Reserved	0Ah	
		Reserved	0Ch	
		Reserved	0Eh	
		Reserved	10h	
		VMAIFG Vacant memory access	12h	
		JMBINIFG JTAG mailbox input	14h	
		JMBOUTIFG JTAG mailbox output	16h	
		Correctable FRAM bit error detection	18h	
		Reserved	1Ah to 1Eh	Lowest
SYSUNIV, User NMI	015Ah	No interrupt pending	00h	
		NMIIFG NMI pin or SVS_H event	02h	Highest
		OFIFG oscillator fault	04h	
		Reserved	06h to 1Eh	Lowest

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6.11.6 Cyclic Redundancy Check (CRC)

The 16-bit cyclic redundancy check (CRC) module produces a signature based on a sequence of data values and can be used for data checking purposes. The CRC generation polynomial is compliant with CRC-16-CCITT standard of $x^{16} + x^{12} + x^5 + 1$.

6.11.7 Enhanced Universal Serial Communication Interface (eUSCI_A0, eUSCI_B0)

The eUSCI modules are used for serial data communications. The eUSCI_A module supports either UART or SPI communications. The eUSCI_B module supports either SPI or I^2C communications. In addition, the eUSCI_A module supports automatic baud-rate detection and IrDA.. The eUSCI_B module is connected either from P1 port or P2 port, it can be selected from the USCIBRMAP bit of the SYSCFG2 register (see Table 6-12).

Table 6-12. eUSCI Pin Configurations

	PIN	**UART**	**SPI**
eUSCI_A0	P1.7	TXD	SIMO
	P1.6	RXD	SOMI
	P1.5	–	SCLK
	P1.4	–	STE
eUSCI_B0	**PIN** (USCIBRMP = 0)	**I^2C**	**SPI**
	P1.0	–	STE
	P1.1	–	SCLK
	P1.2	SDA	SIMO
	P1.3	SCL	SOMI
	PIN (USCIBRMP = 1)	**I^2C**	**SPI**
	P2.2	–	STE
	P2.3	–	SCLK
	P2.4	SDA	SIMO
	P2.5	SCL	SOMI

6.11.8 Timers (Timer0_B3, Timer1_B3)

The Timer0_B3 and Timer1_B3 modules are 16-bit timers and counters with three capture/compare registers each. Each can support multiple captures or compares, PWM outputs, and interval timing (see Table 6-13 and Table 6-14). Each has extensive interrupt capabilities. Interrupts may be generated from the counter on overflow conditions and from each of the capture/compare registers. The CCR0 registers on TB0 and TB1 are not externally connected and can be used only for hardware period timing and interrupt generation. In Up mode, they can set the overflow value of the counter.

The interconnection of Timer0_B3 and Timer1_B3 can modulate the eUSCI_A pin of UCA0TXD/UCA0SIMO in either ASK or FSK mode, with which a user can easily acquire a modulated infrared command for directly driving an external IR diode (see Figure 6-2). The IR functions are fully controlled by the SYS configuration registers including IREN (enable), IRPSEL (polarity select), IRMSEL (mode select), IRDSSEL (data select), and IRDATA (data) bits. For more information, see the *System Resets, Interrupts, and Operating Modes, System Control Module (SYS)* chapter in the *MSP430FR4xx and MSP430FR2xx Family User's Guide*.

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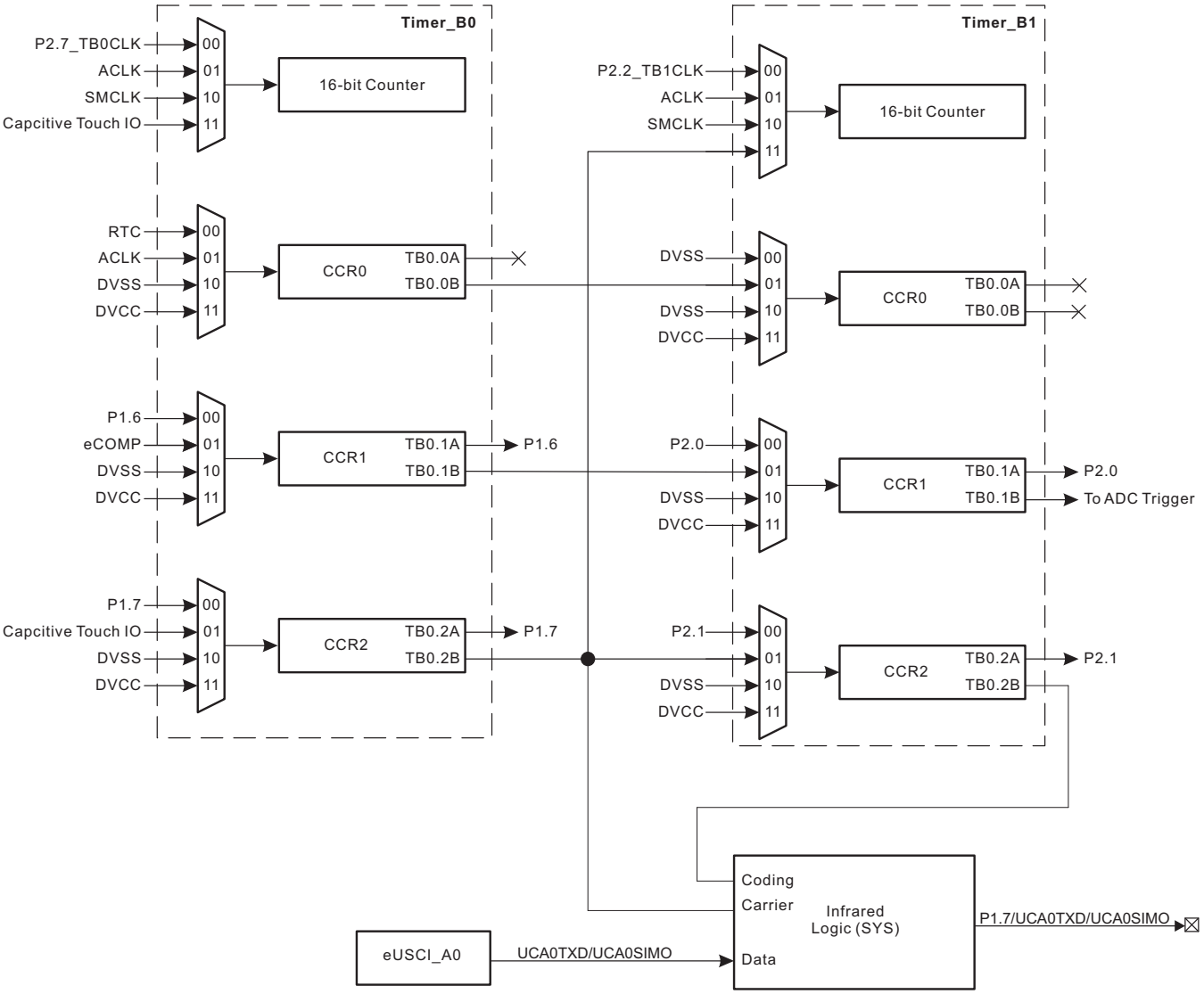


Figure 6-2. Timer_B Connections

Table 6-13. Timer0_B3 Signal Connections

PORT PIN	DEVICE INPUT SIGNAL	MODULE INPUT NAME	MODULE BLOCK	MODULE OUTPUT SIGNAL	DEVICE OUTPUT SIGNAL
P2.7	TB0CLK	TBCLK	Timer	N/A	
	ACLK (internal)	ACLK			
	SMCLK (internal)	SMCLK			
	From Capacitive Touch I/O (internal)	INCLK			
	From RTC (internal)	CCI0A	CCR0	TB0	
	ACLK (internal)	CCI0B			Timer1_B3 CCI0B input
	DVSS	GND			
	DVCC	V_{CC}			
P1.6	TB0.1	CCI1A	CCR1	TB1	TB0.1
	From eCOMP (internal)	CCI1B			Timer1_B3 CCI1B input
	DVSS	GND			
	DVCC	V_{CC}			
P1.7	TB0.2	CCI2A	CCR2	TB2	TB0.2
	From Capacitive Touch I/O (internal)	CCI2B			Timer1_B3 INCLK Timer1_B3 CCI2B input, IR input
	DVSS	GND			
	DVCC	V_{CC}			

Table 6-14. Timer1_B3 Signal Connections

PORT PIN	DEVICE INPUT SIGNAL	MODULE INPUT NAME	MODULE BLOCK	MODULE OUTPUT SIGNAL	DEVICE OUTPUT SIGNAL
P2.2	TB1CLK	TBCLK	Timer	N/A	
	ACLK (internal)	ACLK			
	SMCLK (internal)	SMCLK			
	Timer0_B3 CCR2B output (internal)	INCLK			
	DVSS	CCI0A	CCR0	TB0	
	Timer0_B3 CCR0B output (internal)	CCI0B			
	DVSS	GND			
	DVCC	V_{CC}			
P2.0	TB1.1	CCI1A	CCR1	TB1	TB1.1
	Timer0_B3 CCR1B output (internal)	CCI1B			To ADC trigger
	DVSS	GND			
	DVCC	V_{CC}			
P2.1	TB1.2	CCI2A	CCR2	TB2	TB1.2
	Timer0_B3 CCR2B output (internal)	CCI2B			IR input
	DVSS	GND			
	DVCC	V_{CC}			

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The Timer_B module includes a feature that puts all Timer_B outputs into a high-impedance state when the selected source is triggered. The source can be selected from an external pin or an internal signal, and it is controlled by TBxTRG in SYS. For more information, see the *System Resets, Interrupts, and Operating Modes, System Control Module (SYS)* chapter in the *MSP430FR4xx and MSP430FR2xx Family User's Guide*.

Table 6-15 lists the Timer_B high-impedance trigger source selections.

Table 6-15. TBxOUTH

TBxTRGSEL	TBxOUTH TRIGGER SOURCE SELECTION	Timer_B PAD OUTPUT HIGH IMPEDANCE
TB0TRGSEL = 0	eCOMP0 output (internal)	P1.6, P1.7
TB0TRGSEL= 1	P1.2	
TB1TRGSEL = 0	eCOMP0 output (internal)	P2.0, P2.1
TB1TRGSEL = 1	P2.3	

6.11.9 Backup Memory (BAKMEM)

The BAKMEM supports data retention during LPM3.5 mode. This device provides up to 32 bytes that are retained during LPM3.5.

6.11.10 Real-Time Clock (RTC) Counter

The RTC counter is a 16-bit modulo counter that is functional in AM, LPM0, LPM3, LPM4, and LPM3.5. This module may periodically wake up the CPU from LPM0, LPM3, LPM4, and LPM3.5 based on timing from a low-power clock source such as the XT1, ACLK, or VLO clocks. In AM, RTC can be driven by SMCLK to generate high-frequency timing events and interrupts. ACLK and SMCLK both can source to the RTC, however only one of them can be selected simultaneously. The RTC overflow events trigger:

- Timer0_B3 CCI0A
- ADC conversion trigger when ADCSHSx bits are set as 01b

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6.11.11 10-Bit Analog-to-Digital Converter (ADC)

The 10-bit ADC module supports fast 10-bit analog-to-digital conversions with single-ended input. The module implements a 10-bit SAR core, sample select control, a reference generator, and a conversion result buffer. A window comparator with lower and upper limits allows CPU-independent result monitoring with three window comparator interrupt flags.

The ADC supports 10 external inputs and 4 internal inputs (see Table 6-16).

Table 6-16. ADC Channel Connections

ADCINCHx	ADC CHANNELS	EXTERNAL PIN
0	A0/Veref+	P1.0
1	A1	P1.1
2	A2/Veref-	P1.2
3	A3	P1.3
4	A4	P1.4
5	A5	P1.5
6	A6	P1.6
7	A7(1)	P1.7
8	Not used	N/A
9	Not used	N/A
10	Not used	N/A
11	Not used	N/A
12	On-chip temperature sensor	N/A
13	Reference voltage (1.5 V)	N/A
14	DVSS	N/A
15	DVCC	N/A

(1) When A7 is used, the PMM 1.2-V reference voltage can be output to this pin by setting the PMM control register. The 1.2-V voltage can be measured by the A7 channel.

The analog-to-digital conversion can be started by software or a hardware trigger. Table 6-17 lists the trigger sources that are available.

Table 6-17. ADC Trigger Signal Connections

ADCSHSx		TRIGGER SOURCE
BINARY	DECIMAL	
00	0	ADCSC bit (software trigger)
01	1	RTC event
10	2	TB1.1B
11	3	eCOMP0 COUT

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6.11.12 eCOMP0

The enhanced comparator is an analog voltage comparator with built-in 6-bit DAC as an internal voltage reference. The integrated 6-bit DAC can be set up to 64 steps for comparator reference voltage. This module has 4-level programmable hysteresis and configurable power modes, high power or low power.

eCOMP0 supports external inputs and internal inputs (see Table 6-18) and outputs (see Table 6-19).

Table 6-18. eCOMP0 Input Channel Connections

CPPSEL, CPNSEL BINARY	eCOMP0 CHANNELS	EXTERNAL OR INTERNAL CONNECTION
000	C0	P1.0
001	C1	P1.1
010	Not used	N/A
011	Not used	N/A
100	C4	SAC0 , OA0O on positive port TIA0, TRI0O on negative port
101	Not used	N/A
110	C6	Built-in 6-bit DAC

Table 6-19. eCOMP0 Output Channel Connections

eCOMP0 OUT	EXTERNAL PIN OUT, MODULE
1	P2.0
2	TB0.1B, TB0 (TB0OUTH), TB1 (TB1OUTH), ADC

6.11.13 SAC0

The Smart Analog Combo (SAC) integrates a high-performance low-power operational amplifier. SAC-L1 is integrated in FR231x. SAC-L1 supports only a general-purpose amplifier. For more information, see the *Smart Analog Combo (SAC)* chapter in the *MSP430FR4xx and MSP430FR2xx Family User's Guide*.

SAC0 supports external inputs and internal inputs (see Table 6-20 and Table 6-21).

Table 6-20. SAC0 Positive Input Channel Connections

PSEL	SAC0 CHANNELS	EXTERNAL PIN OUT, MODULE
00	SAC0, OA0 positive channel 1	P1.4
10	SAC0, OA0 positive channel 2	TRI0O

Table 6-21. SAC0 Negative Input Channel Connections

NSEL	SAC0 CHANNELS	EXTERNAL PIN OUT, MODULE
00	SAC0, OA0 negative channel 1	P1.2
10	Not used	N/A

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6.11.14 TIA0

The Transimpedance Amplifier (TIA) is a high-performance low-power amplifier with rail-to-rail output. This module is an amplifier that converts current to voltage. It has programmable power modes: high power or low power. For more information, see the *Transimpedance Amplifier (TIA)* chapter in the *MSP430FR4xx and MSP430FR2xx Family User's Guide*.

The FR231x device in the TSSOP-16 package supports a dedicated low-leakage pad for TIA negative input to support low-leakage performance. In other packages (TSSOP-20 and VQFN-16), the TIA negative port is shared with a GPIO to support the transimpedance amplifier function. For more information, see Section 4 and Table 5-25.

The TIA supports external input (see Table 6-22 and Section 4).

Table 6-22. TIA Input Channel Connections

TRIPSEL	TIA0 CHANNELS	EXTERNAL PIN OUT, MODULE
00	Positive input	P1.7
01	Not used	N/A
10	Not used	N/A
11	Not used	N/A

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6.11.15 eCOMP0, SAC0, TIA0, and ADC in SOC Interconnection

Figure 6-3 shows how the high-performance analog modules are internally connected.

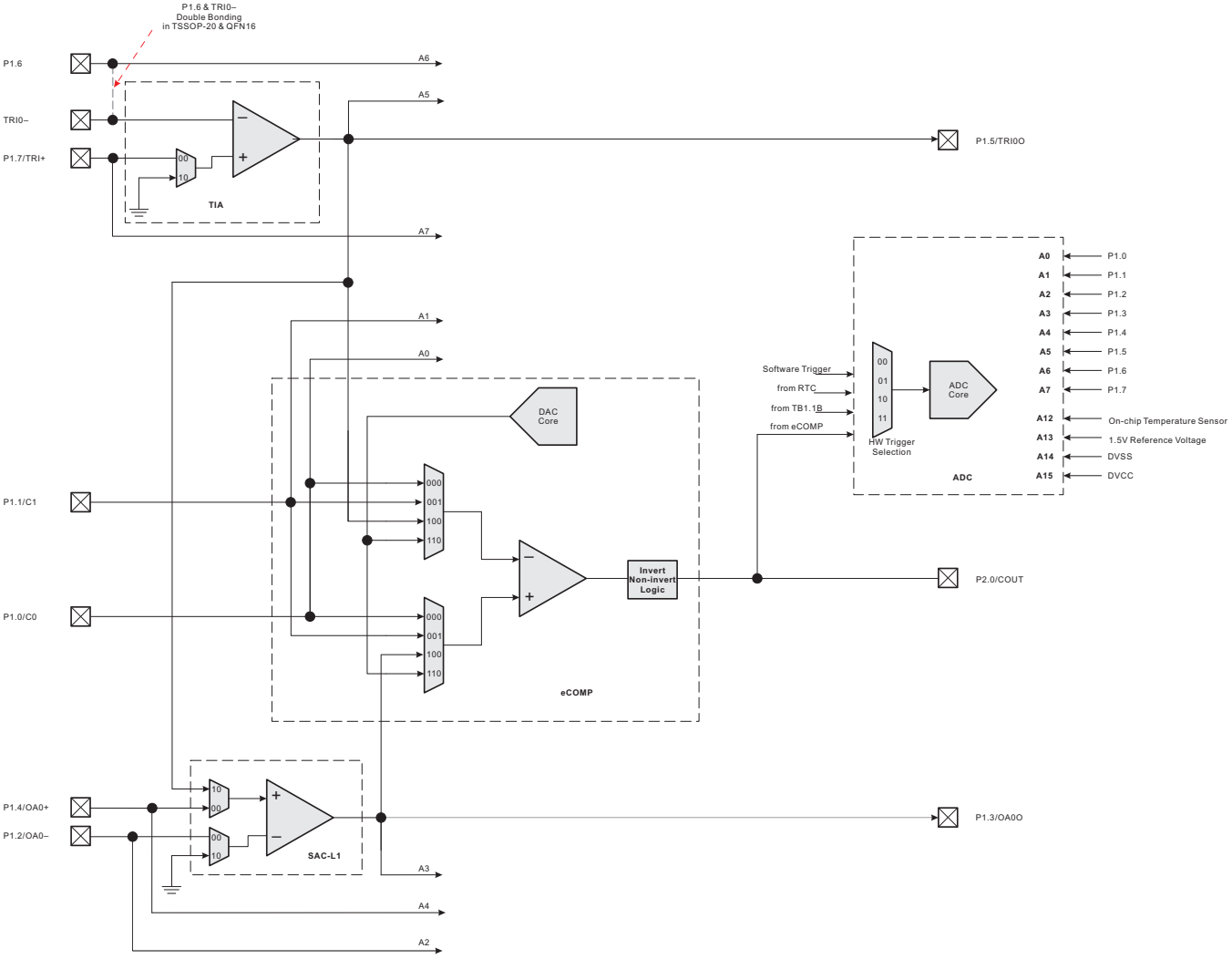


Figure 6-3. High-Performance Analog SOC Interconnection

Figure 6-4 shows how the analog modules can be connected internally.

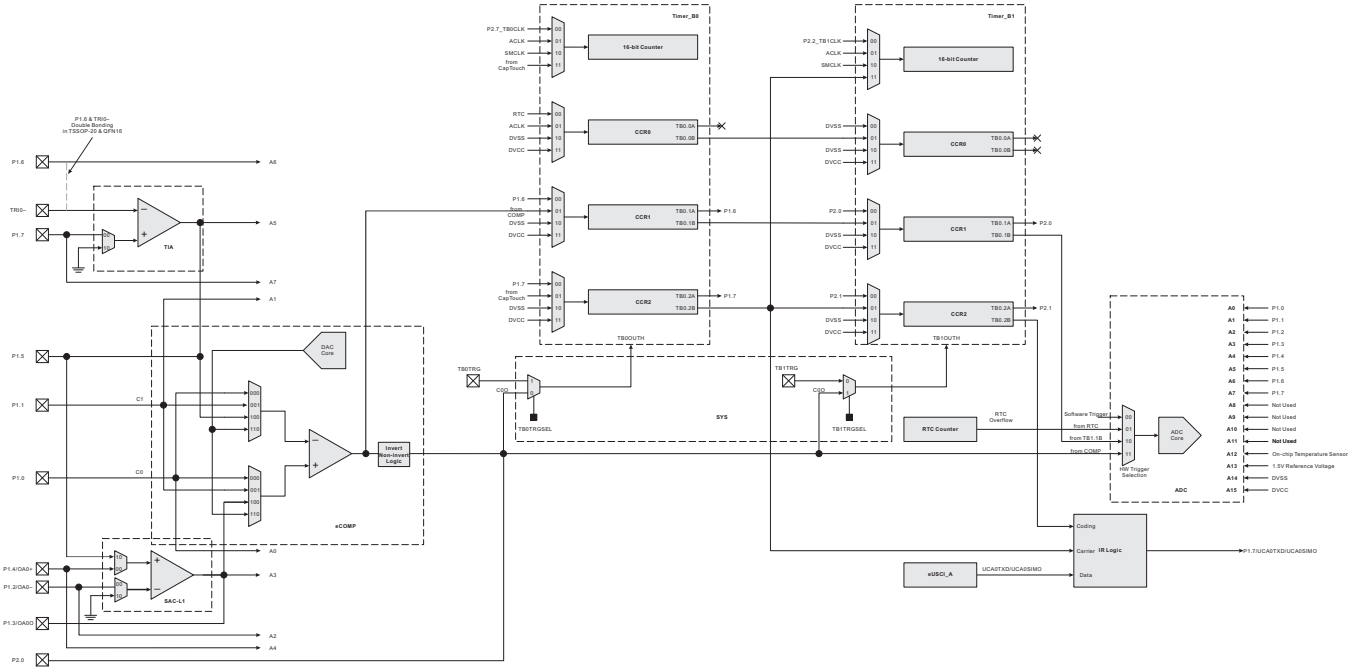


Figure 6-4. SOC Interconnection

6.11.16 Embedded Emulation Module (EEM)

The EEM supports real-time in-system debugging. The EEM on these devices has the following features:

- Three hardware triggers or breakpoints on memory access
- One hardware trigger or breakpoint on CPU register write access
- Up to four hardware triggers that can be combined to form complex triggers or breakpoints
- One cycle counter
- Clock control on module level

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6.11.17 Peripheral File Map

Table 6-23 lists the base address of the registers for each peripheral. Table 6-24 through Table 6-42 list all of the available registers for each peripheral and their address offsets.

Table 6-23. Peripherals Summary

MODULE NAME	BASE ADDRESS	SIZE
Special Functions (see Table 6-24)	0100h	0010h
PMM (see Table 6-25)	0120h	0020h
SYS (see Table 6-26)	0140h	0040h
CS (see Table 6-27)	0180h	0020h
FRAM (see Table 6-28)	01A0h	0010h
CRC (see Table 6-29)	01C0h	0008h
WDT (see Table 6-30)	01CCh	0002h
Port P1, P2 (see Table 6-31)	0200h	0020h
Capacitive Touch I/O (see Table 6-32)	02E0h	0010h
RTC (see Table 6-33)	0300h	0010h
Timer0_B3 (see Table 6-34)	0380h	0030h
Timer1_B3 (see Table 6-35)	03C0h	0030h
eUSCI_A0 (see Table 6-36)	0500h	0020h
eUSCI_B0 (see Table 6-37)	0540h	0030h
Backup Memory (see Table 6-38)	0660h	0020h
ADC (see Table 6-39)	0700h	0040h
eCOMP0 (see Table 6-40)	08E0h	0020h
SAC0 (see Table 6-41)	0C80h	0010h
TIA0 (see Table 6-42)	0F00h	0010h

Table 6-24. Special Function Registers (Base Address: 0100h)

REGISTER DESCRIPTION	REGISTER	OFFSET
SFR interrupt enable	SFRIE1	00h
SFR interrupt flag	SFRIFG1	02h
SFR reset pin control	SFRRPCR	04h

Table 6-25. PMM Registers (Base Address: 0120h)

REGISTER DESCRIPTION	REGISTER	OFFSET
PMM control 0	PMMCTL0	00h
PMM control 1	PMMCTL1	02h
PMM control 2	PMMCTL2	04h
PMM interrupt flags	PMMIFG	0Ah
PM5 control 0	PM5CTL0	10h

Table 6-26. SYS Registers (Base Address: 0140h)

REGISTER DESCRIPTION	REGISTER	OFFSET
System control	SYSCTL	00h
Bootloader configuration area	SYSBSLC	02h
JTAG mailbox control	SYSJMBC	06h
JTAG mailbox input 0	SYSJMBI0	08h
JTAG mailbox input 1	SYSJMBI1	0Ah
JTAG mailbox output 0	SYSJMBO0	0Ch

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Table 6-26. SYS Registers (Base Address: 0140h) (continued)

REGISTER DESCRIPTION	REGISTER	OFFSET
JTAG mailbox output 1	SYSJMBO1	0Eh
User NMI vector generator	SYSUNIV	1Ah
System NMI vector generator	SYSSNIV	1Ch
Reset vector generator	SYSRSTIV	1Eh
System configuration 0	SYSCFG0	20h
System configuration 1	SYSCFG1	22h
System configuration 2	SYSCFG2	24h

Table 6-27. CS Registers (Base Address: 0180h)

REGISTER DESCRIPTION	REGISTER	OFFSET
CS control 0	CSCTL0	00h
CS control 1	CSCTL1	02h
CS control 2	CSCTL2	04h
CS control 3	CSCTL3	06h
CS control 4	CSCTL4	08h
CS control 5	CSCTL5	0Ah
CS control 6	CSCTL6	0Ch
CS control 7	CSCTL7	0Eh
CS control 8	CSCTL8	10h

Table 6-28. FRAM Registers (Base Address: 01A0h)

REGISTER DESCRIPTION	REGISTER	OFFSET
FRAM control 0	FRCTL0	00h
General control 0	GCCTL0	04h
General control 1	GCCTL1	06h

Table 6-29. CRC Registers (Base Address: 01C0h)

REGISTER DESCRIPTION	REGISTER	OFFSET
CRC data input	CRC16DI	00h
CRC data input reverse byte	CRCDIRB	02h
CRC initialization and result	CRCINIRES	04h
CRC result reverse byte	CRCRESR	06h

Table 6-30. WDT Registers (Base Address: 01CCh)

REGISTER DESCRIPTION	REGISTER	OFFSET
Watchdog timer control	WDTCTL	00h

Table 6-31. Port P1, P2 Registers (Base Address: 0200h)

REGISTER DESCRIPTION	REGISTER	OFFSET
Port P1 input	P1IN	00h
Port P1 output	P1OUT	02h
Port P1 direction	P1DIR	04h
Port P1 pulling enable	P1REN	06h
Port P1 selection 0	P1SEL0	0Ah
Port P1 selection 1	P1SEL1	0Ch
Port P1 interrupt vector word	P1IV	0Eh

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Table 6-31. Port P1, P2 Registers (Base Address: 0200h) (continued)

REGISTER DESCRIPTION	REGISTER	OFFSET
Port P1 complement selection	P1SELC	16h
Port P1 interrupt edge select	P1IES	18h
Port P1 interrupt enable	P1IE	1Ah
Port P1 interrupt flag	P1IFG	1Ch
Port P2 input	P2IN	01h
Port P2 output	P2OUT	03h
Port P2 direction	P2DIR	05h
Port P2 pulling enable	P2REN	07h
Port P2 selection 0	P2SEL0	0Bh
Port P2 selection 1	P2SEL1	0Dh
Port P2 complement selection	P2SELC	17h
Port P2 interrupt vector word	P2IV	1Eh
Port P2 interrupt edge select	P2IES	19h
Port P2 interrupt enable	P2IE	1Bh
Port P2 interrupt flag	P2IFG	1Dh

Table 6-32. Capacitive Touch I/O Registers (Base Address: 02E0h)

REGISTER DESCRIPTION	REGISTER	OFFSET
Capacitive touch I/O 0 control	CAPIO0CTL	0Eh

Table 6-33. RTC Registers (Base Address: 0300h)

REGISTER DESCRIPTION	REGISTER	OFFSET
RTC control	RTCCTL	00h
RTC interrupt vector	RTCIV	04h
RTC modulo	RTCMOD	08h
RTC counter	RTCCNT	0Ch

Table 6-34. Timer0_B3 Registers (Base Address: 0380h)

REGISTER DESCRIPTION	REGISTER	OFFSET
TB0 control	TB0CTL	00h
Capture/compare control 0	TB0CCTL0	02h
Capture/compare control 1	TB0CCTL1	04h
Capture/compare control 2	TB0CCTL2	06h
TB0 counter	TB0R	10h
Capture/compare 0	TB0CCR0	12h
Capture/compare 1	TB0CCR1	14h
Capture/compare 2	TB0CCR2	16h
TB0 expansion 0	TB0EX0	20h
TB0 interrupt vector	TB0IV	2Eh

Table 6-35. Timer1_B3 Registers (Base Address: 03C0h)

REGISTER DESCRIPTION	REGISTER	OFFSET
TB1 control	TB1CTL	00h
Capture/compare control 0	TB1CCTL0	02h
Capture/compare control 1	TB1CCTL1	04h
Capture/compare control 2	TB1CCTL2	06h

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Table 6-35. Timer1_B3 Registers (Base Address: 03C0h) (continued)

REGISTER DESCRIPTION	REGISTER	OFFSET
TB1 counter	TB1R	10h
Capture/compare 0	TB1CCR0	12h
Capture/compare 1	TB1CCR1	14h
Capture/compare 2	TB1CCR2	16h
TB1 expansion 0	TB1EX0	20h
TB1 interrupt vector	TB1IV	2Eh

Table 6-36. eUSCI_A0 Registers (Base Address: 0500h)

REGISTER DESCRIPTION	REGISTER	OFFSET
eUSCI_A control word 0	UCA0CTLW0	00h
eUSCI_A control word 1	UCA0CTLW1	02h
eUSCI_A control rate 0	UCA0BR0	06h
eUSCI_A control rate 1	UCA0BR1	07h
eUSCI_A modulation control	UCA0MCTLW	08h
eUSCI_A status	UCA0STAT	0Ah
eUSCI_A receive buffer	UCA0RXBUF	0Ch
eUSCI_A transmit buffer	UCA0TXBUF	0Eh
eUSCI_A LIN control	UCA0ABCTL	10h
eUSCI_A IrDA transmit control	lUCA0IRTCTL	12h
eUSCI_A IrDA receive control	lUCA0IRRCTL	13h
eUSCI_A interrupt enable	UCA0IE	1Ah
eUSCI_A interrupt flags	UCA0IFG	1Ch
eUSCI_A interrupt vector word	UCA0IV	1Eh

Table 6-37. eUSCI_B0 Registers (Base Address: 0540h)

REGISTER DESCRIPTION	REGISTER	OFFSET
eUSCI_B control word 0	UCB0CTLW0	00h
eUSCI_B control word 1	UCB0CTLW1	02h
eUSCI_B bit rate 0	UCB0BR0	06h
eUSCI_B bit rate 1	UCB0BR1	07h
eUSCI_B status word	UCB0STATW	08h
eUSCI_B byte counter threshold	UCB0TBCNT	0Ah
eUSCI_B receive buffer	UCB0RXBUF	0Ch
eUSCI_B transmit buffer	UCB0TXBUF	0Eh
eUSCI_B I2C own address 0	UCB0I2COA0	14h
eUSCI_B I2C own address 1	UCB0I2COA1	16h
eUSCI_B I2C own address 2	UCB0I2COA2	18h
eUSCI_B I2C own address 3	UCB0I2COA3	1Ah
eUSCI_B receive address	UCB0ADDRX	1Ch
eUSCI_B address mask	UCB0ADDMASK	1Eh
eUSCI_B I2C slave address	UCB0I2CSA	20h
eUSCI_B interrupt enable	UCB0IE	2Ah
eUSCI_B interrupt flags	UCB0IFG	2Ch
eUSCI_B interrupt vector word	UCB0IV	2Eh

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Table 6-38. Backup Memory Registers (Base Address: 0660h)

REGISTER DESCRIPTION	REGISTER	OFFSET
Backup memory 0	BAKMEM0	00h
Backup memory 1	BAKMEM1	02h
Backup memory 2	BAKMEM2	04h
Backup memory 3	BAKMEM3	06h
Backup memory 4	BAKMEM4	08h
Backup memory 5	BAKMEM5	0Ah
Backup memory 6	BAKMEM6	0Ch
Backup memory 7	BAKMEM7	0Eh
Backup memory 8	BAKMEM8	10h
Backup memory 9	BAKMEM9	12h
Backup memory 10	BAKMEM10	14h
Backup memory 11	BAKMEM11	16h
Backup memory 12	BAKMEM12	18h
Backup memory 13	BAKMEM13	1Ah
Backup memory 14	BAKMEM14	1Ch
Backup memory 15	BAKMEM15	1Eh

Table 6-39. ADC Registers (Base Address: 0700h)

REGISTER DESCRIPTION	REGISTER	OFFSET
ADC control 0	ADCCTL0	00h
ADC control 1	ADCCTL1	02h
ADC control 2	ADCCTL2	04h
ADC window comparator low threshold	ADCLO	06h
ADC window comparator high threshold	ADCHI	08h
ADC memory control 0	ADCMCTL0	0Ah
ADC conversion memory	ADCMEM0	12h
ADC interrupt enable	ADCIE	1Ah
ADC interrupt flags	ADCIFG	1Ch
ADC interrupt vector word	ADCIV	1Eh

Table 6-40. eCOMP0 Registers (Base Address: 08E0h)

REGISTER DESCRIPTION	REGISTER	OFFSET
Comparator control 0	CPCTL0	00h
Comparator control 1	CPCTL1	02h
Comparator interrupt	CPINT	06h
Comparator interrupt vector	CPIV	08h
Comparator built-in DAC control	CPDACCTL	10h
Comparator built-in DAC data	CPDACDATA	12h

Table 6-41. SAC0 Registers (Base Address: 0C80h)

REGISTER DESCRIPTION	REGISTER	OFFSET
SAC0 OA control	SAC0OA	00h

Table 6-42. TIA0 Registers (Base Address: 0F00h)

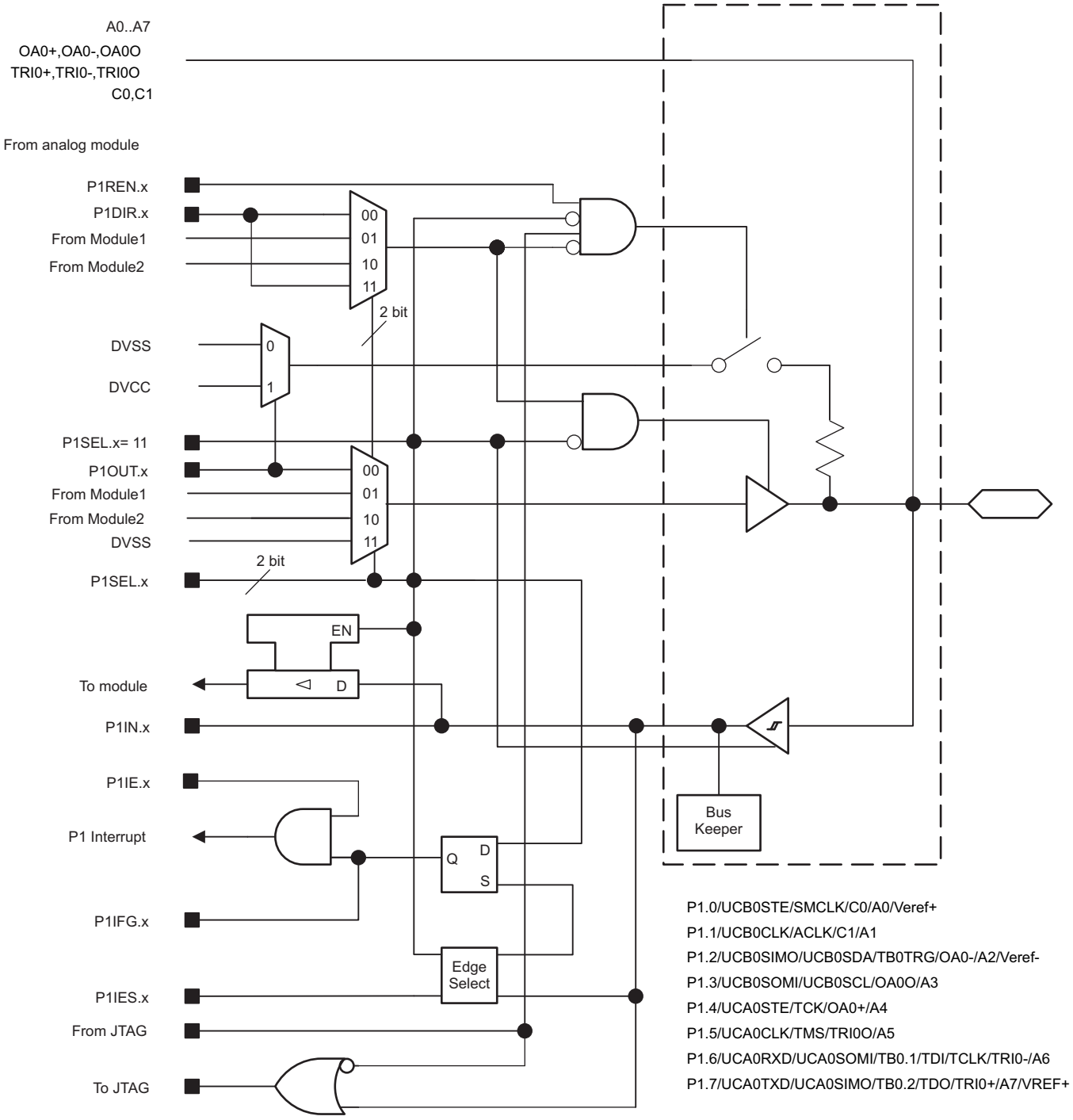
REGISTER DESCRIPTION	REGISTER	OFFSET
TIA control	TRICTL	00h

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6.12 Input/Output Diagrams

6.12.1 Port P1 Input/Output With Schmitt Trigger

Figure 6-5 shows the port diagram. Table 6-43 summarizes the selection of the port functions.



NOTE: Functional representation only.

Figure 6-5. Port P1 Input/Output With Schmitt Trigger

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Table 6-43. Port P1 Pin Functions

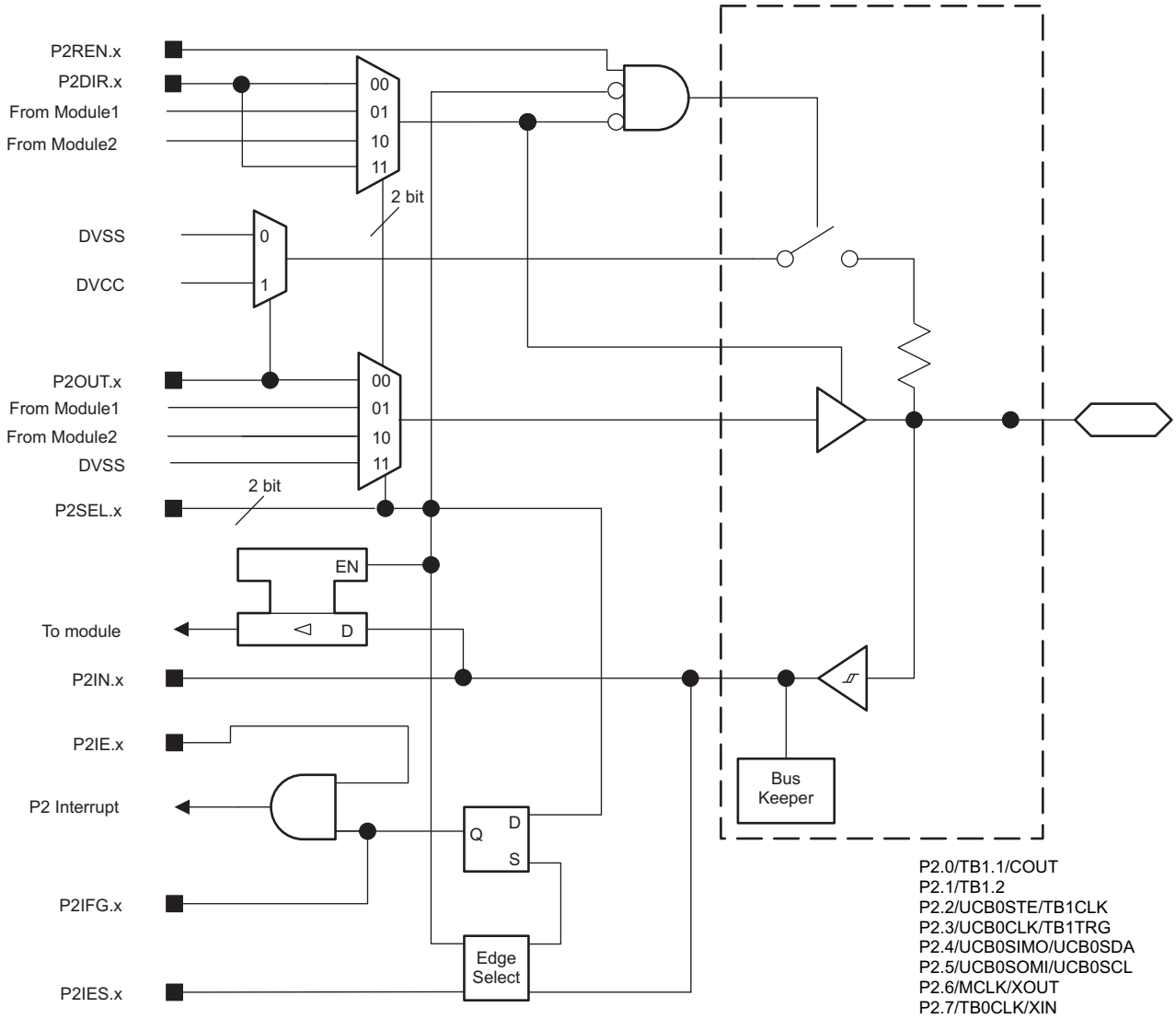
PIN NAME (P1.x)	x	FUNCTION	CONTROL BITS AND SIGNALS[1]		
			P1DIR.x	P1SELx	JTAG
P1.0/UCB0STE/SMCLK/ C0/A0/Veref+	0	P1.0 (I/O)	I: 0; O: 1	00	N/A
		UCB0STE	X	01	N/A
		SMCLK	1	10	N/A
		VSS	0		
		C0, A0/Veref+	X	11	N/A
P1.1/UCB0CLK/ACLK/ C1A1	1	P1.1 (I/O)	I: 0; O: 1	0	N/A
		UCB0CLK	X	01	N/A
		ACLK	1	10	N/A
		VSS	0		
		C1, A1	X	11	N/A
P1.2/UCB0SIMO/ UCB0SDA/TB0TRG/ OA0-/A2/Veref-	2	P1.2 (I/O)	I: 0; O: 1	00	N/A
		UCB0SIMO/UCB0SDA	X	01	N/A
		TB0TRG	0	10	N/A
		OA0-, A2/Veref-	X	11	N/A
P1.3/UCB0SOMI/ UCB0SCL/OA0O/A3	3	P1.3 (I/O)	I: 0; O: 1	00	N/A
		UCB0SOMI/UCB0SCL	X	01	N/A
		OA0O, A3	X	11	N/A
P1.4/UCA0STE/TCK/ OA0+/A4	4	P1.4 (I/O)	I: 0; O: 1	00	Disabled
		UCA0STE	X	01	Disabled
		OA0+, A4	X	11	Disabled
		JTAG TCK	X	X	TCK
P1.5/UCA0CLK/TMS/ TRI0O/A5	5	P1.5 (I/O)	I: 0; O: 1	00	Disabled
		UCA0CLK	X	01	Disabled
		TRI0O, A5	X	11	Disabled
		JTAG TMS	X	X	TMS
P1.6/UCA0RXD/ UCA0SOMI/TB0.1/TDI/ TCLK/TRI0-/A6	6	P1.6 (I/O)	I: 0; O: 1	00	Disabled
		UCA0RXD/UCA0SOMI	X	01	Disabled
		TB0.CCI1A	0	10	Disabled
		TB0.1	1		
		TRI0-, A6	X	11	Disabled
		JTAG TDI/TCLK	X	X	TDI/TCLK
P1.7/UCA0TXD/ UCA0SIMO/TB0.2/TDO/ TRI0+/A7/VREF+	7	P1.7 (I/O)	I: 0; O: 1	00	Disabled
		UCA0TXD/UCA0SIMO	X	01	Disabled
		TB0.CCI2A	0	10	Disabled
		TB0.2	1		
		TRI0+, A7, VREF+	X	11	Disabled
		JTAG TDO	X	X	TDO

(1) X = don't care

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6.12.2 Port P2 Input/Output With Schmitt Trigger

Figure 6-6 shows the port diagram. Table 6-44 summarizes the selection of the port functions.



NOTE: Functional representation only.

Figure 6-6. Port P2 Input/Output With Schmitt Trigger

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Table 6-44. Port P2 Pin Functions

PIN NAME (P2.x)	x	FUNCTION	CONTROL BITS AND SIGNALS(1)	
			P2DIR.x	P2SELx
P2.0/TB1.1/COUT	0	P2.0 (I/O)	I: 0; O: 1	00
		TB1.CCI1A	0	01
		TB1.1	1	
		COUT	1	10
P2.1/TB1.2	1	P2.1 (I/O)0	I: 0; O: 1	00
		TB1.CCI2A	0	01
		TB1.2	1	
P2.2/UCB0STE/TB1CLK	2	P2.2 (I/O)	I: 0; O: 1	00
		UCB0STE	X	01
		TB1CLK	0	10
		VSS	1	
P2.3/UCB0CLK/TB1TRG	3	P2.3 (I/O)	I: 0; O: 1	00
		UCB0CLK	X	01
		TB1TRG	0	10
P2.4/UCB0SIMO/UCB0SDA	4	P2.4 (I/O)	I: 0; O: 1	00
		UCB0SIMO/UCB0SDA	X	01
P2.5/UCB0SOMI/UCB0SCL	5	P2.5 (I/O)	I: 0; O: 1	00
		UCB0SOMI/UCB0SCL	X	01
P2.6/MCLK/XOUT	6	P2.6 (I/O)	I: 0; O: 1	00
		MCLK	1	01
		VSS	0	
		XOUT	X	10
P2.7/TB0CLK/XIN	7	P2.7 (I/O)	I: 0; O: 1	00
		TB0CLK	0	01
		VSS	1	
		XIN	X	10

(1) X = don't care

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6.13 Device Descriptors (TLV)

Table 6-45 lists the Device IDs of the MSP430FR231x MCU variants. Table 6-46 lists the contents of the device descriptor tag-length-value (TLV) structure for the devices.

Table 6-45. Device IDs

DEVICE	DEVICE ID	
	1A04h	1A05h
MSP430FR2311	F0	82
MSP430FR2310	F1	82

Table 6-46. Device Descriptors

DESCRIPTION		MSP430FR231x	
		ADDRESS	VALUE
Info block	Info length	1A00h	06h
	CRC length	1A01h	06h
	CRC value(1)	1A02h	Per unit
		1A03h	Per unit
	Device ID	1A04h	See Table 6-45.
		1A05h	
	Hardware revision	1A06h	Per unit
	Firmware revision	1A07h	Per unit
Die record	Die record tag	1A08h	08h
	Die record length	1A09h	0Ah
	Lot wafer ID	1A0Ah	Per unit
		1A0Bh	Per unit
		1A0Ch	Per unit
		1A0Dh	Per unit
	Die X position	1A0Eh	Per unit
		1A0Fh	Per unit
	Die Y position	1A10h	Per unit
		1A11h	Per unit
	Test result	1A12h	Per unit
		1A13h	Per unit
ADC calibration	ADC calibration tag	1A14h	Per unit
	ADC calibration length	1A15h	Per unit
	ADC gain factor	1A16h	Per unit
		1A17h	Per unit
	ADC offset	1A18h	Per unit
		1A19h	Per unit
	ADC 1.5-V reference, temperature 30°C(2)	1A1Ah	Per unit
		1A1Bh	Per unit
	ADC 1.5-V reference, temperature 85°C(2)	1A1Ch	Per unit
		1A1Dh	Per unit

(1) The CRC value covers the checksum from 0x1A04h to 0x1A77h by applying CRC-CCITT-16 polynomial of $X^{16} + X^{12} + X^5 + 1$
(2) TI recommends to do a two-point calibration for the on-chip temperature sensor in precision application.

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Table 6-46. Device Descriptors (continued)

DESCRIPTION		MSP430FR231x	
		ADDRESS	VALUE
Reference and DCO calibration	Calibration tag	1A1Eh	12h
	Calibration length	1A1Fh	04h
	1.5-V reference factor	1A20h	Per unit
		1A21h	Per unit
	DCO tap settings for 16 MHz, temperature 30°C (3)	1A22h	Per unit
		1A23h	Per unit

(3) This value can be directly loaded into the DCO bits in the CSCTL0 register to get an accurate 16-MHz frequency at room temperature, especially when MCU exits from LPM3 and below. TI also suggests using a predivider to decrease the frequency if the temperature drift might result an overshoot above 16 MHz.

6.14 Identification

6.14.1 Revision Identification

The device revision information is shown as part of the top-side marking on the device package. The device-specific errata sheet describes these markings. For links to all of the errata sheets for the devices in this data sheet, see 8.4.

The hardware revision is also stored in the Device Descriptor structure in the Info Block section. For details on this value, see the "Hardware Revision" entries in Section 6.13.

6.14.2 Device Identification

The device type can be identified from the top-side marking on the device package. The device-specific errata sheet describes these markings. For links to all of the errata sheets for the devices in this data sheet, see 8.4.

A device identification value is also stored in the Device Descriptor structure in the Info Block section. For details on this value, see the "Device ID" entries in Section 6.13.

6.14.3 JTAG Identification

Programming through the JTAG interface, including reading and identifying the JTAG ID, is described in detail in the *MSP430 Programming With the JTAG Interface*.

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7 Applications, Implementation, and Layout

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their implementation to confirm system functionality.

7.1 Device Connection and Layout Fundamentals

This section describes the recommended guidelines when designing with the MSP430. These guidelines are to make sure that the device has proper connections for powering, programming, debugging, and optimum analog performance.

7.1.1 Power Supply Decoupling and Bulk Capacitors

TI recommends connecting a combination of a 10-µF capacitor and a 100-nF low-ESR ceramic decoupling capacitor to the DVCC pin. Higher-value capacitors may be used but can affect supply rail ramp-up time. Decoupling capacitors must be placed as close as possible to the pins that they decouple (within a few millimeters).

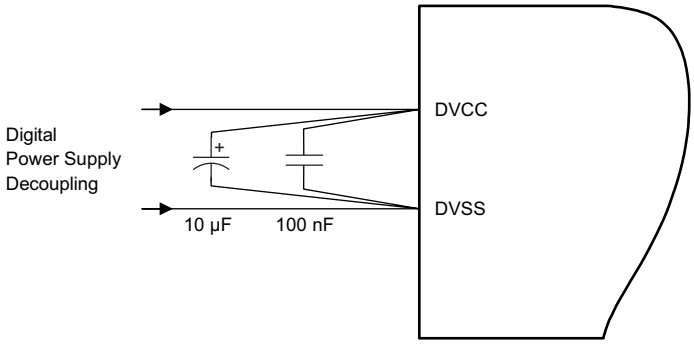


Figure 7-1. Power Supply Decoupling

7.1.2 External Oscillator

Depending on the device variant (see Table 3-1), the device can support a low-frequency crystal (32 kHz) on the LFXT pins, a high-frequency crystal on the HFXT pins, or both. External bypass capacitors for the crystal oscillator pins are required.

It is also possible to apply digital clock signals to the LFXIN and HFXIN input pins that meet the specifications of the respective oscillator if the appropriate LFXTBYPASS or HFXTBYPASS mode is selected. In this case, the associated LFXOUT and HFXOUT pins can be used for other purposes. If the LFXOUT and HFXOUT pins are left unused, they must be terminated according to Section 4.6.

Figure 7-2 shows a typical connection diagram.

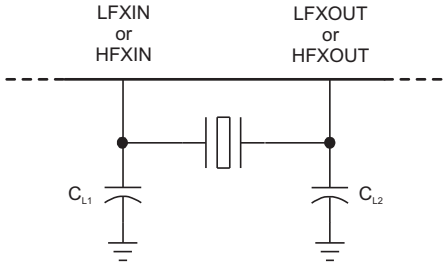


Figure 7-2. Typical Crystal Connection

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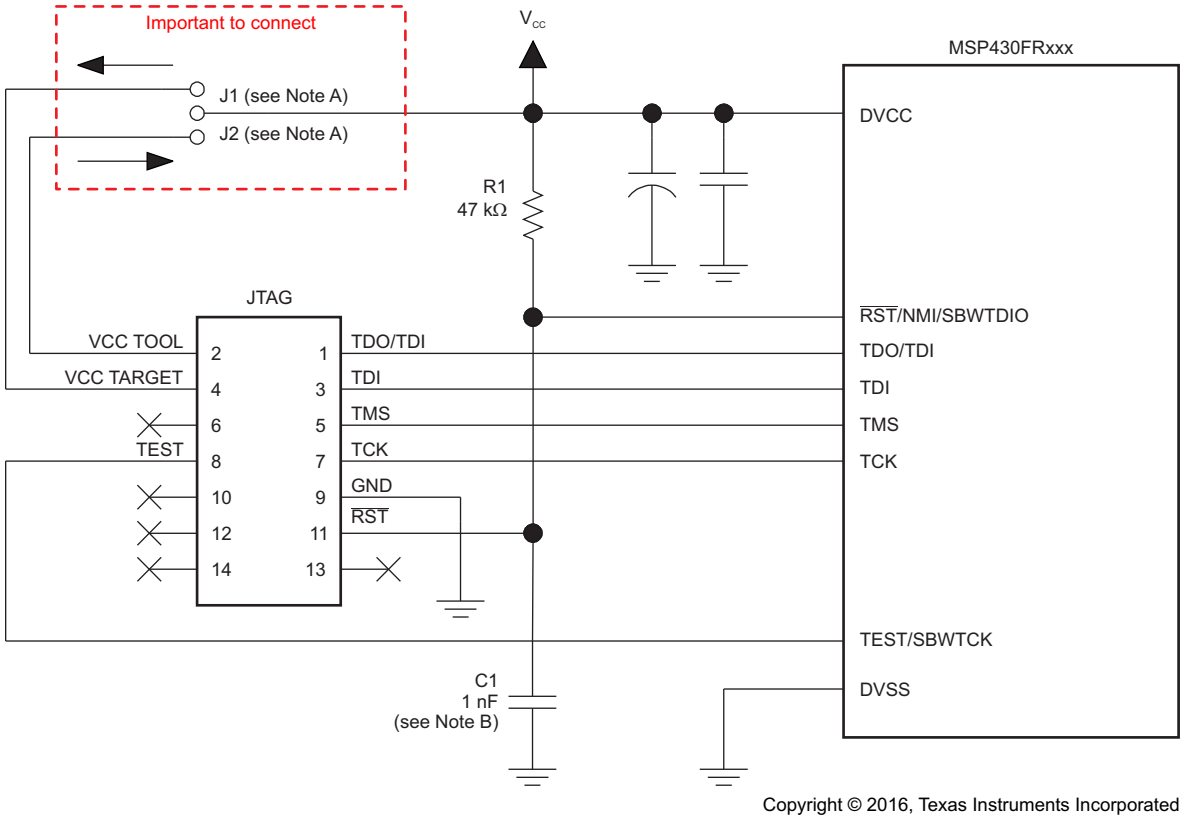
See *MSP430 32-kHz Crystal Oscillators* for more information on selecting, testing, and designing a crystal oscillator with the MSP430 devices.

7.1.3 JTAG

With the proper connections, the debugger and a hardware JTAG interface (such as the MSP-FET or MSP-FET430UIF) can be used to program and debug code on the target board. In addition, the connections also support the MSP-GANG production programmers, thus providing an easy way to program prototype boards, if desired. Figure 7-3 shows the connections between the 14-pin JTAG connector and the target device required to support in-system programming and debugging for 4-wire JTAG communication. Figure 7-4 shows the connections for 2-wire JTAG mode (Spy-Bi-Wire).

The connections for the MSP-FET and MSP-FET430UIF interface modules and the MSP-GANG are identical. Both can supply V_{CC} to the target board (through pin 2). In addition, the MSP-FET and MSP-FET430UIF interface modules and MSP-GANG have a V_{CC} sense feature that, if used, requires an alternate connection (pin 4 instead of pin 2). The VCC-sense feature detects the local V_{CC} present on the target board (that is, a battery or other local power supply) and adjusts the output signals accordingly. Figure 7-3 and Figure 7-4 show a jumper block that supports both scenarios of supplying V_{CC} to the target board. If this flexibility is not required, the desired V_{CC} connections may be hardwired to eliminate the jumper block. Pins 2 and 4 must not be connected at the same time.

For additional design information regarding the JTAG interface, see the *MSP430 Hardware Tools User's Guide*.

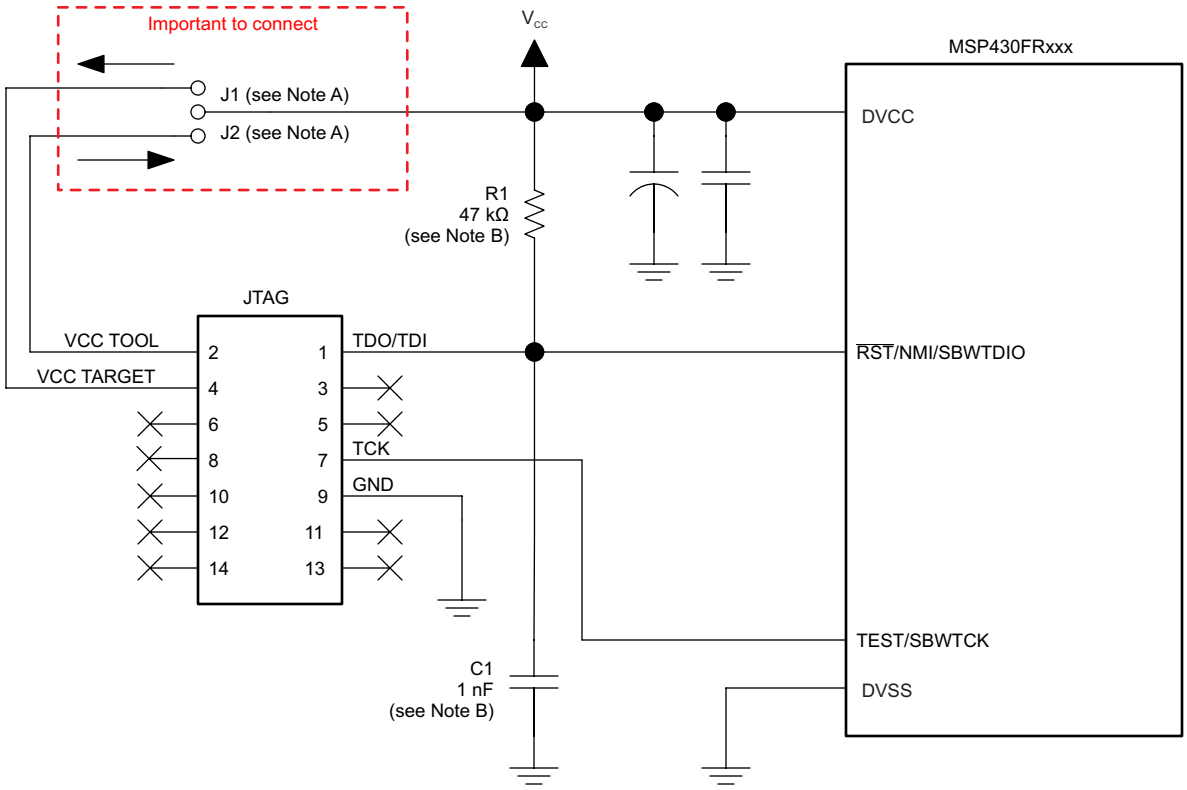


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A. If a local target power supply is used, make connection J1. If power from the debug or programming adapter is used, make connection J2.

B. The upper limit for C1 is 1.1 nF when using TI tools. TI recommends a 1-nF capacitor to enable high-speed SBW communication.

Figure 7-3. Signal Connections for 4-Wire JTAG Communication



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A. Make connection J1 if a local target power supply is used, or make connection J2 if the target is powered from the debug or programming adapter.

B. The device RST/NMI/SBWTDIO pin is used in 2-wire mode for bidirectional communication with the device during JTAG access, and any capacitance that is attached to this signal may affect the ability to establish a connection with the device. The upper limit for C1 is 1.1 nF when using TI tools. TI recommends a 1-nF capacitor to enable high-speed SBW communication.

Figure 7-4. Signal Connections for 2-Wire JTAG Communication (Spy-Bi-Wire)

7.1.4 Reset

The reset pin can be configured as a reset function (default) or as an NMI function in the Special Function Register (SFR), SFRRPCR.

In reset mode, the RST/NMI pin is active low, and a pulse applied to this pin that meets the reset timing specifications generates a BOR-type device reset.

Setting SYSNMI causes the RST/NMI pin to be configured as an external NMI source. The external NMI is edge sensitive, and its edge is selectable by SYSNMIIES. Setting the NMIIE enables the interrupt of the external NMI. When an external NMI event occurs, the NMIIFG is set.

The RST/NMI pin can have either a pullup or pulldown that is enabled or not. SYSRSTUP selects either pullup or pulldown, and SYSRSTRE causes the pullup (default) or pulldown to be enabled (default) or not. If the RST/NMI pin is unused, it is required either to select and enable the internal pullup or to connect an external 47-kΩ pullup resistor to the RST/NMI pin with a 10-nF pulldown capacitor. The pulldown capacitor should not exceed 1.1 nF when using devices with Spy-Bi-Wire interface in Spy-Bi-Wire mode or in 4-wire JTAG mode with TI tools like FET interfaces or GANG programmers.

See the *MSP430FR4xx and MSP430FR2xx Family User's Guide* for more information on the referenced control registers and bits.

7.1.5 Unused Pins

For details on the connection of unused pins, see Section 4.6.

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7.1.6 General Layout Recommendations

- Proper grounding and short traces for external crystal to reduce parasitic capacitance. See *MSP430 32-kHz Crystal Oscillators* for recommended layout guidelines.
- Proper bypass capacitors on DVCC, AVCC, and reference pins if used.
- Avoid routing any high-frequency signal close to an analog signal line. For example, keep digital switching signals such as PWM or JTAG signals away from the oscillator circuit and ADC signals.
- Proper ESD level protection should be considered to protect the device from unintended high-voltage electrostatic discharge. See *MSP430 System-Level ESD Considerations* for guidelines.

7.1.7 Do's and Don'ts

During power up, power down, and device operation, the voltage difference between AVCC and DVCC must not exceed the limits specified in the Absolute Maximum Ratings section. Exceeding the specified limits may cause malfunction of the device including erroneous writes to RAM and FRAM.

7.2 Peripheral- and Interface-Specific Design Information

7.2.1 ADC Peripheral

7.2.1.1 Partial Schematic

Figure 7-5 shows the recommended decoupling circuit when an external voltage reference is used.

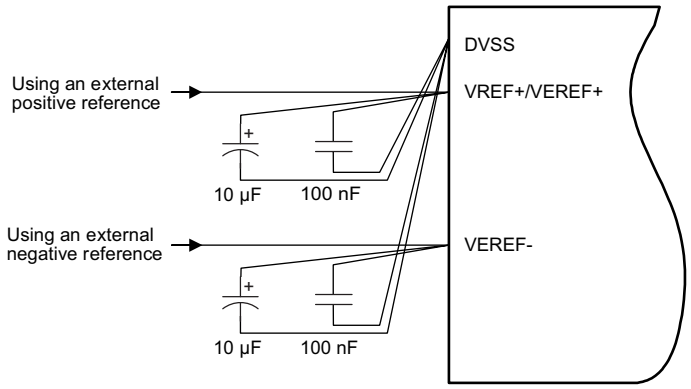


Figure 7-5. ADC Grounding and Noise Considerations

7.2.1.2 Design Requirements

As with any high-resolution ADC, appropriate printed-circuit-board layout and grounding techniques should be followed to eliminate ground loops, unwanted parasitic effects, and noise.

Ground loops are formed when return current from the ADC flows through paths that are common with other analog or digital circuitry. If care is not taken, this current can generate small unwanted offset voltages that can add to or subtract from the reference or input voltages of the ADC. The general guidelines in Section 7.1.1 combined with the connections shown in Figure 7-5 prevent this.

In addition to grounding, ripple and noise spikes on the power-supply lines that are caused by digital switching or switching power supplies can corrupt the conversion result. TI recommends a noise-free design using separate analog and digital ground planes with a single-point connection to achieve high accuracy.

Figure 7-5 shows the recommended decoupling circuit when an external voltage reference is used. The internal reference module has a maximum drive current as described in the sections *ADC Pin Enable* and *1.2-V Reference Settings* of the *MSP430FR4xx and MSP430FR2xx Family User's Guide*.

The reference voltage must be a stable voltage for accurate measurements. The capacitor values that are selected in the general guidelines filter out the high- and low-frequency ripple before the reference voltage enters the device. In this case, the 10-µF capacitor buffers the reference pin and filters any low-frequency ripple. A bypass capacitor of 100 nF filters out any high-frequency noise.

7.2.1.3 Layout Guidelines

Components that are shown in the partial schematic (see Figure 7-5) should be placed as close as possible to the respective device pins to avoid long traces, because they add additional parasitic capacitance, inductance, and resistance on the signal.

Avoid routing analog input signals close to a high-frequency pin (for example, a high-frequency PWM), because the high-frequency switching can be coupled into the analog signal.

7.3 Typical Applications

Table 7-1 provides a link to a LaunchPad™ development kit. For the most up-to-date list of available tools and TI Designs, see the device-specific product folders listed in 8.5.

Table 7-1. Tools

NAME	LINK
MSP430FR2311 LaunchPad Development Kit	http://www.ti.com/tool/MSP-EXP430FR2311

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8 デバイスおよびドキュメントのサポート

8.1 はじめに

MSP430™ファミリのデバイス、および開発に役立つツールやライブラリの詳細については、「MSP430™ 超低消費電力センシング / 測定マイコン」の概要ページを参照してください。

8.2 デバイスの項目表記

製品開発サイクルの段階を示すために、TIではMSP　MCUデバイスのすべての型番に接頭辞が割り当てられています。MSP MCU商用ファミリの各番号には、MSP、XMSのいずれかの接頭辞があります。これらの接頭辞は、製品開発の進展段階を表します。段階には、エンジニアリング・プロトタイプ(XMS)から、完全認定済みの量産デバイス(MSP)までがあります。

XMS - 実験段階のデバイスで、最終的なデバイスの電気的仕様を表しているとは限りません。

MSP - 完全に認定済みの量産版デバイスです。

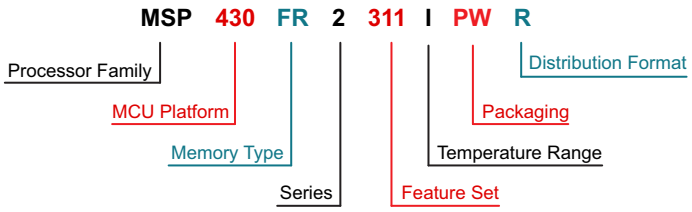
XMSデバイスは、次の免責事項付きで出荷されます。

「開発中の製品は、社内での評価用です。」

MSPデバイスの特性は完全に明確化されており、デバイスの品質と信頼性が十分に示されています。TIの標準保証が適用されます。

プロトタイプ・デバイス(XMS)は標準の量産デバイスよりも故障率が高いことが予想されます。これらのデバイスは、予測される最終使用時の故障率が未定義であるため、TIはそれらのデバイスを量産システムで使用しないよう推奨しています。認定された量産デバイスのみを使用する必要があります。

TIデバイスの項目表記には、デバイス・ファミリ名の接尾辞も含まれます。この接尾辞は、温度範囲、パッケージ・タイプ、配布形式を示しています。デバイス名の各部の読み方を図 8-1に示します。



Processor Family	MSP = Mixed-Signal Processor XMS = Experimental Silicon	
MCU Platform	MSP430 = TI's MSP430 16-Bit Low-Power Microcontroller Platform	
Memory Type	FR = FRAM	
Series	2 = FRAM 2 Series up to 16 MHz without LCD	
Feature Set	**First and Second Digits: Smart Analog Combo (SAC) Level / ADC Channels / COMP / 16-bit Timers / I/O** 31 = SAC-L1 / Up to 8 / 1 / 2 / Up to 16	**Third Digit: FRAM (KB) / SRAM (KB)** 1 = 4 / 1 0 = 2 / 1
Temperature Range	I = –40°C to 85°C	
Packaging	www.ti.com/packaging	
Distribution Format	T = Small reel R = Large reel No marking = Tube or tray	

図 8-1. デバイスの項目表記

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8.3 ツールとソフトウェア

表 8-1 は、これらのマイクロコントローラでサポートされるデバッグ機能の一覧です。利用可能な機能の詳細については、『*Code Composer Studio™ v5.2 ユーザーズ・ガイド MSP430™ 版ユーザーズ・ガイド*』を参照してください。

表 8-1. ハードウェアの特長

MSP430のアーキテクチャ	4線式JTAG	2線式JTAG	ブレーク・ポイント (N)	範囲ブレーク・ポイント	クロック制御	状態シーケンサ	トレース・バッファ	LPMx.5デバッグ・サポート	EEMのバージョン
MSP430Xv2	○	○	3	○	○	×	×	×	S

設計キットと評価基板

MSP430FR2311 LaunchPad開発キット

MSP-EXP430FR2311 LaunchPad開発キットは、MSP430FR2311 MCU用の使いやすいマイクロコントローラ開発ボードです。プログラミング、デバッグ、電力測定を行うためのオンボード・エミュレーションなど、MSP430FR2x FRAMプラットフォームの迅速な開発に必要なすべての機能を備えています。

MSP-FET＋MSP-TS430PW20 FRAMマイクロコントローラ開発キット・バンドル

MSP-FET430U20バンドルは、2つのデバッグ・ツールを組み合わせたもので、MSP430FR23xマイクロコントローラ用の20ピンPWパッケージ(MSP430FR2311PW20など)をサポートしています。これら2つのツールには、MSP-TS430PW20とMSP-FETが含まれています。

MSP430FR2x MCU用MSP-TS430PW20 20ピン・ターゲット開発ボード

MSP-TS430PW20 はスタンドアロンの ZIF ソケット・ターゲット・ボードで、JTAG インターフェイスまたは Spy-Bi-Wire (2線式の JTAG) プロトコルによるシステム内の MSP430 MCU のプログラムとデバッグに使用されます。この開発ボードは、20 ピンまたは 16 ピンの TSSOP パッケージ (TI パッケージ・コード:PW) に封止された MSP430FR23x および MSP430FR21x のフラッシュ部品をすべてサポートしています。

ソフトウェア

MSP430Ware™ソフトウェア

MSP430Wareソフトウェアは、すべてのMSP430デバイス向けのサンプル・コード、データシート、その他の設計リソースを、1つの便利なパッケージとしてまとめたものです。既存のMSP430用設計リソースの完全なコレクションに加えて、MSP430WareソフトウェアにはMSP430ドライバ・ライブラリという高レベルのAPIも含まれています。このライブラリにより、MSP430ハードウェアを簡単にプログラムできます。MSP430Wareソフトウェアは CCSのコンポーネントとして、またはスタンドアロンのパッケージとして入手できます。

MSP430FR231xのサンプル・コード

すべてのMSPデバイス用に、内蔵の各ペリフェラルをさまざまなアプリケーションの要求に応じて構成するためのCコード・サンプルが用意されています。

MSP ドライバ・ライブラリ

MSPドライバ・ライブラリの抽象化されたAPIには、使いやすい関数呼び出しが含まれているため、MSP430ハードウェアのビットやバイトを直接操作する煩雑さから解放されます。使いやすいAPIガイドにより包括的な技術資料が参照でき、それぞれの関数呼び出しと、認識されるパラメータの詳細が記載されています。開発者は、ドライバ・ライブラリの関数を使用して、最小限のオーバーヘッドで完全なプロジェクトを作成できます。

MSP EnergyTrace™ テクノロジ

MSP430 マイコン向け EnergyTrace テクノロジはエネルギー・ベースのコード分析ツールで、アプリケーションのエネルギー・プロファイルの測定と表示を行うとともに、消費電力の大幅な低減のための最適化も可能です。

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ULP (超低消費電力) Advisor

ULP Advisor™ソフトウェアは、MSPおよびMSP432マイクロコントローラの超低消費電力機能を十分に活用できる、最も効率的なコードを開発者が作成できるよう手引きするツールです。ULP Advisorはマイクロコントローラに熟練した開発者と、新しい開発者の両方を対象としており、包括的なULPチェックリストを使用してコードをチェックし、アプリケーションのエネルギー消費を最小化するため役立ちます。ビルド時に、消費電力低減のためさらに最適化が可能なコードの部分を明らかにするため通知と注釈を出力します。

MSP超低消費電力マイクロコントローラ用FRAM組み込みソフトウェア・ユーティリティ

FRAMユーティリティは、組み込みソフトウェア・ユーティリティのコレクションとして成長するように設計されており、超低消費電力とほぼ無限の書き込み耐性というFRAMの特長を活用できます。このユーティリティはMSP430FRxx FRAMマイクロコントローラで利用でき、アプリケーション開発に役立つサンプル・コードを提供します。搭載されているユーティリティには、Compute Through Power Loss (CTPL)があります。CTPLはユーティリティAPIセットで、LPMx.5低消費電力モードにより使いやすさを実現する一方、強力なシャットダウン・モードにより、停電検出時にアプリケーションが重要なシステム・コンポーネントを保存・復元できます。

IEC60730 ソフトウェア・パッケージ

IEC60730 MSP430ソフトウェア・パッケージは、クラスBまでの製品について、お客様がIEC 60730-1:2010 (家庭および同様な用途に使用される自動電気制御 – 第1部: 一般的な要件)に準拠するため役立つよう開発されています。この分類には家電機器、アーク検出器、電力コンバータ、電動工具、電動アシスト自転車、その他多くの製品が含まれます。IEC60730 MSP430 ソフトウェア・パッケージはMSP430 MCUで実行するお客様のアプリケーションに組み込むことができるため、消費者向けデバイスがIEC 60730-1:2010クラスBの機能安全性に準拠していることの認定作業を簡素化できます。

MSP 用の固定小数点算術ライブラリ

MSP IQmathおよびQmathライブラリは、Cプログラマ向けの高度に最適化された高精度の算術関数のコレクションで、浮動小数点アルゴリズムをMSP430およびMSP432デバイスの固定小数点コードへシームレスに移行できます。これらのルーチンは通常、最適な実行速度、高精度、超低消費電力が重視される、演算集中型のリアルタイム・アプリケーションで使用されます。IQmathライブラリとQmathライブラリを使用すると、浮動小数点演算を使用して記述した同等のコードに比べて、実行速度を大幅に高速化するとともに、消費電力の大幅な削減が可能です。

MSP430用の浮動小数点算術ライブラリ

低消費電力で低コストのマイクロコントローラ分野にさらなる革新を引き起こすため、TIはMSPMATHLIBを提供します。この浮動小数点算術ライブラリは、弊社デバイスのインテリジェントなペリフェラルを活用し、標準のMSP430算術関数よりも最高で26倍も高速なスカラー関数です。Mathlibは、設計へ簡単に組み入れることができます。このライブラリは無償で、Code Composer Studio IDEとIAR Embedded Workbench IDEの両方に組み込まれています。

開発ツール

Code Composer Studio™: MSPマイクロコントローラ用の統合開発環境

Code Composer Studio (CCS)は、すべてのMSPマイクロコントローラ・デバイスをサポートする統合開発環境(IDE)です。CCSは、組み込みアプリケーションの開発とデバッグに使用される、組み込み用ソフトウェア・ユーティリティのスイートです。最適化C/C++コンパイラ、ソース・コード・エディタ、プロジェクト・ビルド環境、デバッガ、プロファイラなど、多数の機能が含まれています。

コマンドライン・プログラマ

MSP Flasher は、FET プログラマまたは eZ430 を経由し、JTAG または Spy-Bi-Wire (SBW) 通信を使用して MSP マイクロコントローラをプログラムするための、オープン・ソースでシェル・ベースのインターフェイスです。MSP Flasher は、IDE を使用せずにバイナリ・ファイル (.txt または .hex) を MSP マイクロコントローラへ直接ダウンロードできます。

MSP MCU プログラマおよびデバッガ

MSP-FETは強力なエミュレーション開発ツールで、多くの場合にデバッグ・プローブと呼ばれます。ユーザーはこのツールを使用して、MSP低消費電力MCUのアプリケーション開発をすぐに始めることができます。MCUのソフトウェアを作成する場合は通常、結果として得られたバイナリ・プログラムをMSPデバイスにダウンロードし、検証とデバッグを行う必要があります。

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MSP-GANG量産プログラマ

MSP Gang プログラマは MSP430 または MSP432 用のデバイス・プログラマで、8つまでの同一の MSP430 または MSP432 のフラッシュまたは FRAM デバイスを同時にプログラムできます。MSP Gang プログラマは、標準の RS-232 または USB 接続を使用してホスト PC と接続し、柔軟なプログラミング・オプションが用意されているため、ユーザーはプロセスを完全にカスタマイズ可能です。

8.4 ドキュメントのサポート

以下のドキュメントには、MSP430FR231xマイクロコントローラについての解説が記載されています。これらのドキュメントのコピーは、www.ti.comで入手できます。

ドキュメントの更新通知を受け取る方法

ドキュメント更新の通知を、シリコンの正誤表も含めて受け取るには、ti.com でお使いのデバイスの製品フォルダへ移動します (製品フォルダへのリンクについては、 8.5 を参照してください)。右上の「アラートを受け取る」ボタンをクリックします。これによって登録が行われ、変更された製品情報の概要を毎週受け取ることができます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

正誤表

『MSP430FR2311デバイス正誤表』

機能仕様に対する既知の例外が記載されています。

『MSP430FR2310デバイス正誤表』

機能仕様に対する既知の例外が記載されています。

ユーザー・ガイド

『MSP430FR4xxおよびMSP430FR2xxファミリ ユーザー・ガイド』

このデバイス・ファミリで利用可能なすべてのモジュールとペリフェラルについての詳細情報です。

『MSP430 FRAMデバイス・ブートローダ(BSL) ユーザー・ガイド』

MSP430 MCUに搭載されたブートローダ(BSL)を使用すると、プロトタイプ作成フェーズ、最終的な量産、およびサービス中に、MSP430 MCUの組み込みメモリと通信できます。必要に応じて、プログラム可能メモリ(フラッシュ・メモリ)とデータ・メモリ(RAM)の両方を変更できます。

『JTAGインターフェイスによるMSP430のプログラミング』

このドキュメントでは、JTAG通信ポートを使用してMSP430のフラッシュ・ベースおよびFRAMベースのマイクロコントローラ・ファミリのメモリ・モジュールを消去、プログラム、検証するために必要な機能について解説しています。さらに、すべてのMSP430デバイスで利用可能なJTAGアクセス・セキュリティ・ヒューズのプログラム方法についても解説しています。このドキュメントには、標準の4線式JTAGインターフェイスと2線式JTAGインターフェイスの両方を使用してデバイスにアクセスする方法が解説されています。2線式JTAGインターフェイスはSpy-Bi-Wire (SBW)とも呼ばれます。

『MSP430ハードウェア・ツール ユーザー・ガイド』

このマニュアルには、TI MSP-FET430フラッシュ・エミュレーション・ツール(FET)のハードウェアについて解説されています。このFETは、MSP430超低消費電力マイクロコントローラ用のプログラム開発ツールです。利用可能なインターフェイスとして、パラレル・ポート・インターフェイスとUSBインターフェイスの両方について解説されています。

アプリケーション・レポート

『MSP430 32kHz水晶発振器』

適切な水晶、正しい負荷回路、および適切な基板レイアウトの選択は、安定した水晶発振器のために重要です。このアプリケーション・レポートでは、水晶発振器の機能について要約し、MSP430 MCU の超低消費電力動作用の適切な水晶を選択するためのパラメータについて説明します。また、正しい基板レイアウトについてのヒントや例も紹介しています。このドキュメントには、量産時の安定した発振器の動作を保証するために行うことができる、発振器のテストについての詳細情報も記載されています。

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『MSP430 システム・レベルESDの考慮事項』

シリコン・テクノロジのスケーリングによる低電圧化の進行と、コスト効率の優れた超低消費電力コンポーネントを設計する必要性の高まりにより、システム・レベルの ESD の要求はますます高まっています。このアプリケーション・レポートでは、基板設計者と OEM が堅牢なシステム・レベルのデザインを理解し設計できるよう、各種の ESD トピックについて扱います。現実世界でのシステム・レベルのESD保護設計の例のいくつかと、その結果についても解説します。

8.5 関連リンク

表 8-2 に、クイック・アクセス・リンクの一覧を示します。カテゴリには、技術資料、サポートおよびコミュニティ・リソース、ツールとソフトウェア、およびサンプル注文またはご購入へのクイック・アクセスが含まれます。

表 8-2. 関連リンク

製品	プロダクト・フォルダ	ご注文はこちら	技術資料	ツールとソフトウェア	サポートとコミュニティ
MSP430FR2311	ここをクリック	ここをクリック	ここをクリック	ここをクリック	ここをクリック
MSP430FR2310	ここをクリック	ここをクリック	ここをクリック	ここをクリック	ここをクリック

8.6 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Community
TI's Engineer-to-Engineer (E2E) Community. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas, and help solve problems with fellow engineers.

TI Embedded Processors Wiki
Texas Instruments Embedded Processors Wiki. Established to help developers get started with embedded processors from Texas Instruments and to foster innovation and growth of general knowledge about the hardware and software surrounding these devices.

8.7 商標

LaunchPad, MSP430, MSP430Ware, Code Composer Studio, E2E, EnergyTrace, ULP Advisor are trademarks of Texas Instruments.
All other trademarks are the property of their respective owners.

8.8 静電気放電に関する注意事項

すべての集積回路は、適切なESD保護方法を用いて、取扱いと保存を行うようにして下さい。

静電気放電はわずかな性能の低下から完全なデバイスの故障に至るまで、様々な損傷を与えます。高精度の集積回路は、損傷に対して敏感であり、極めてわずかなパラメータの変化により、デバイスに規定された仕様に適合しなくなる場合があります。

8.9 Glossary

TI Glossary This glossary lists and explains terms, acronyms, and definitions.

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9 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。この情報は、そのデバイスについて利用可能な最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
MSP430FR2310IPW16	Active	Production	TSSOP (PW) | 16	90 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	FR2310
MSP430FR2310IPW16.A	Active	Production	TSSOP (PW) | 16	90 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	FR2310
MSP430FR2310IPW16R	Active	Production	TSSOP (PW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	FR2310
MSP430FR2310IPW16R.A	Active	Production	TSSOP (PW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	FR2310
MSP430FR2310IPW20	Active	Production	TSSOP (PW) | 20	70 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	FR2310
MSP430FR2310IPW20.A	Active	Production	TSSOP (PW) | 20	70 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	FR2310
MSP430FR2310IPW20R	Active	Production	TSSOP (PW) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	FR2310
MSP430FR2310IPW20R.A	Active	Production	TSSOP (PW) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	FR2310
MSP430FR2310IRGYR	Active	Production	VQFN (RGY) | 16	3000 | LARGE T&R	Yes	NIPDAU | SN	Level-2-260C-1 YEAR	-40 to 85	FR2310
MSP430FR2310IRGYR.A	Active	Production	VQFN (RGY) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	FR2310
MSP430FR2310IRGYT	Active	Production	VQFN (RGY) | 16	250 | SMALL T&R	Yes	NIPDAU | SN	Level-2-260C-1 YEAR	-40 to 85	FR2310
MSP430FR2310IRGYT.A	Active	Production	VQFN (RGY) | 16	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	FR2310
MSP430FR2311IPW16	Active	Production	TSSOP (PW) | 16	90 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	FR2311
MSP430FR2311IPW16.A	Active	Production	TSSOP (PW) | 16	90 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	FR2311
MSP430FR2311IPW16R	Active	Production	TSSOP (PW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	FR2311
MSP430FR2311IPW16R.A	Active	Production	TSSOP (PW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	FR2311
MSP430FR2311IPW20	Active	Production	TSSOP (PW) | 20	70 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	FR2311
MSP430FR2311IPW20.A	Active	Production	TSSOP (PW) | 20	70 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	FR2311
MSP430FR2311IPW20R	Active	Production	TSSOP (PW) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	FR2311
MSP430FR2311IPW20R.A	Active	Production	TSSOP (PW) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	FR2311
MSP430FR2311IRGYR	Active	Production	VQFN (RGY) | 16	3000 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 85	FR2311
MSP430FR2311IRGYR.A	Active	Production	VQFN (RGY) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	FR2311
MSP430FR2311IRGYT	Active	Production	VQFN (RGY) | 16	250 | SMALL T&R	Yes	NIPDAU | SN	Level-2-260C-1 YEAR	-40 to 85	FR2311
MSP430FR2311IRGYT.A	Active	Production	VQFN (RGY) | 16	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	FR2311

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

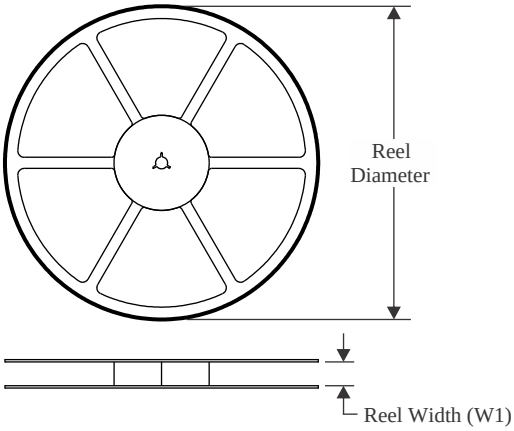
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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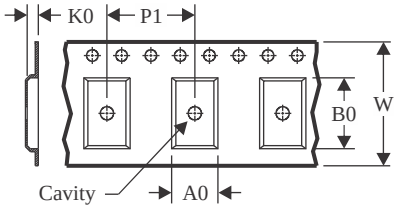
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

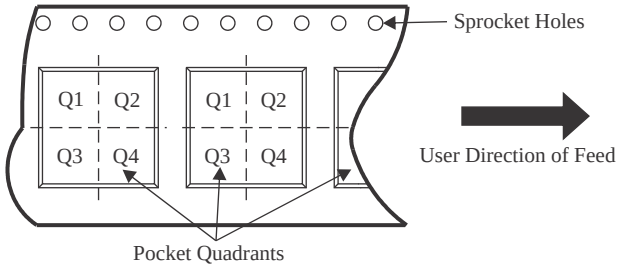


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

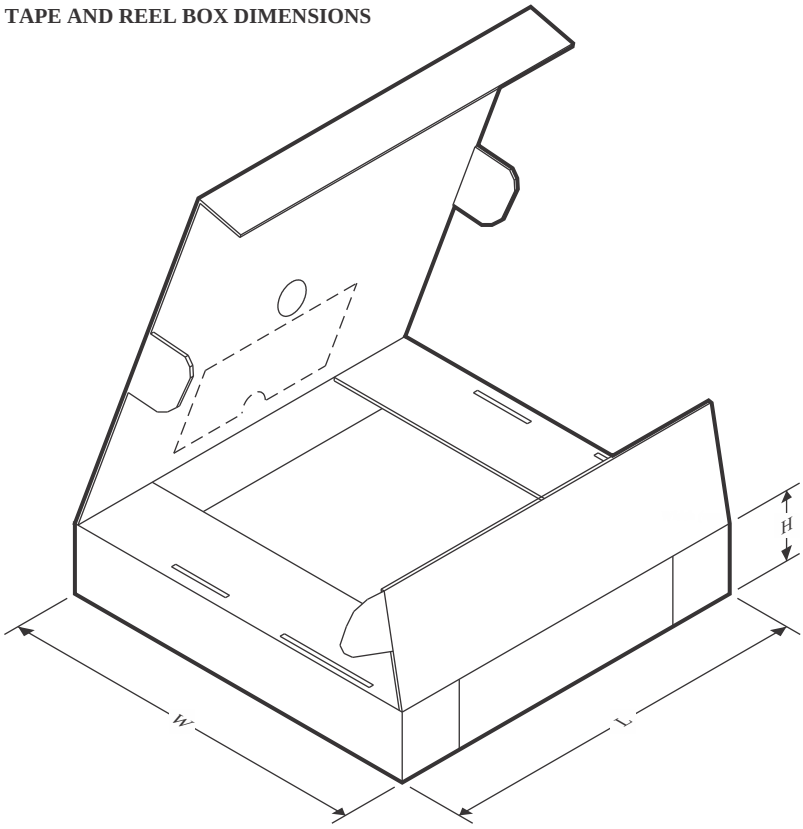
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
MSP430FR2310IPW16R	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
MSP430FR2310IPW20R	TSSOP	PW	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1
MSP430FR2310IRGYR	VQFN	RGY	16	3000	330.0	12.4	3.8	4.3	1.5	8.0	12.0	Q1
MSP430FR2310IRGYR	VQFN	RGY	16	3000	330.0	12.4	3.8	4.3	1.5	8.0	12.0	Q1
MSP430FR2310IRGYT	VQFN	RGY	16	250	180.0	12.4	3.8	4.3	1.5	8.0	12.0	Q1
MSP430FR2310IRGYT	VQFN	RGY	16	250	180.0	12.4	3.8	4.3	1.5	8.0	12.0	Q1
MSP430FR2311IPW16R	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
MSP430FR2311IPW20R	TSSOP	PW	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1
MSP430FR2311IRGYR	VQFN	RGY	16	3000	330.0	12.4	3.8	4.3	1.5	8.0	12.0	Q1
MSP430FR2311IRGYR	VQFN	RGY	16	3000	330.0	12.4	3.8	4.3	1.5	8.0	12.0	Q1
MSP430FR2311IRGYT	VQFN	RGY	16	250	180.0	12.4	3.8	4.3	1.5	8.0	12.0	Q1
MSP430FR2311IRGYT	VQFN	RGY	16	250	180.0	12.4	3.8	4.3	1.5	8.0	12.0	Q1

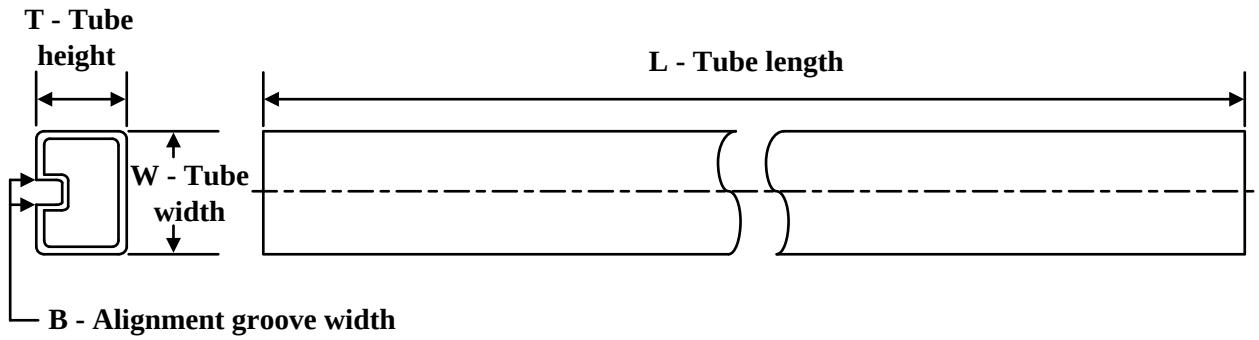
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
MSP430FR2310IPW16R	TSSOP	PW	16	2000	350.0	350.0	43.0
MSP430FR2310IPW20R	TSSOP	PW	20	2000	350.0	350.0	43.0
MSP430FR2310IRGYR	VQFN	RGY	16	3000	346.0	346.0	33.0
MSP430FR2310IRGYR	VQFN	RGY	16	3000	367.0	367.0	35.0
MSP430FR2310IRGYT	VQFN	RGY	16	250	210.0	185.0	35.0
MSP430FR2310IRGYT	VQFN	RGY	16	250	210.0	185.0	35.0
MSP430FR2311IPW16R	TSSOP	PW	16	2000	350.0	350.0	43.0
MSP430FR2311IPW20R	TSSOP	PW	20	2000	350.0	350.0	43.0
MSP430FR2311IRGYR	VQFN	RGY	16	3000	346.0	346.0	33.0
MSP430FR2311IRGYR	VQFN	RGY	16	3000	367.0	367.0	35.0
MSP430FR2311IRGYT	VQFN	RGY	16	250	210.0	185.0	35.0
MSP430FR2311IRGYT	VQFN	RGY	16	250	210.0	185.0	35.0

TUBE



*All dimensions are nominal

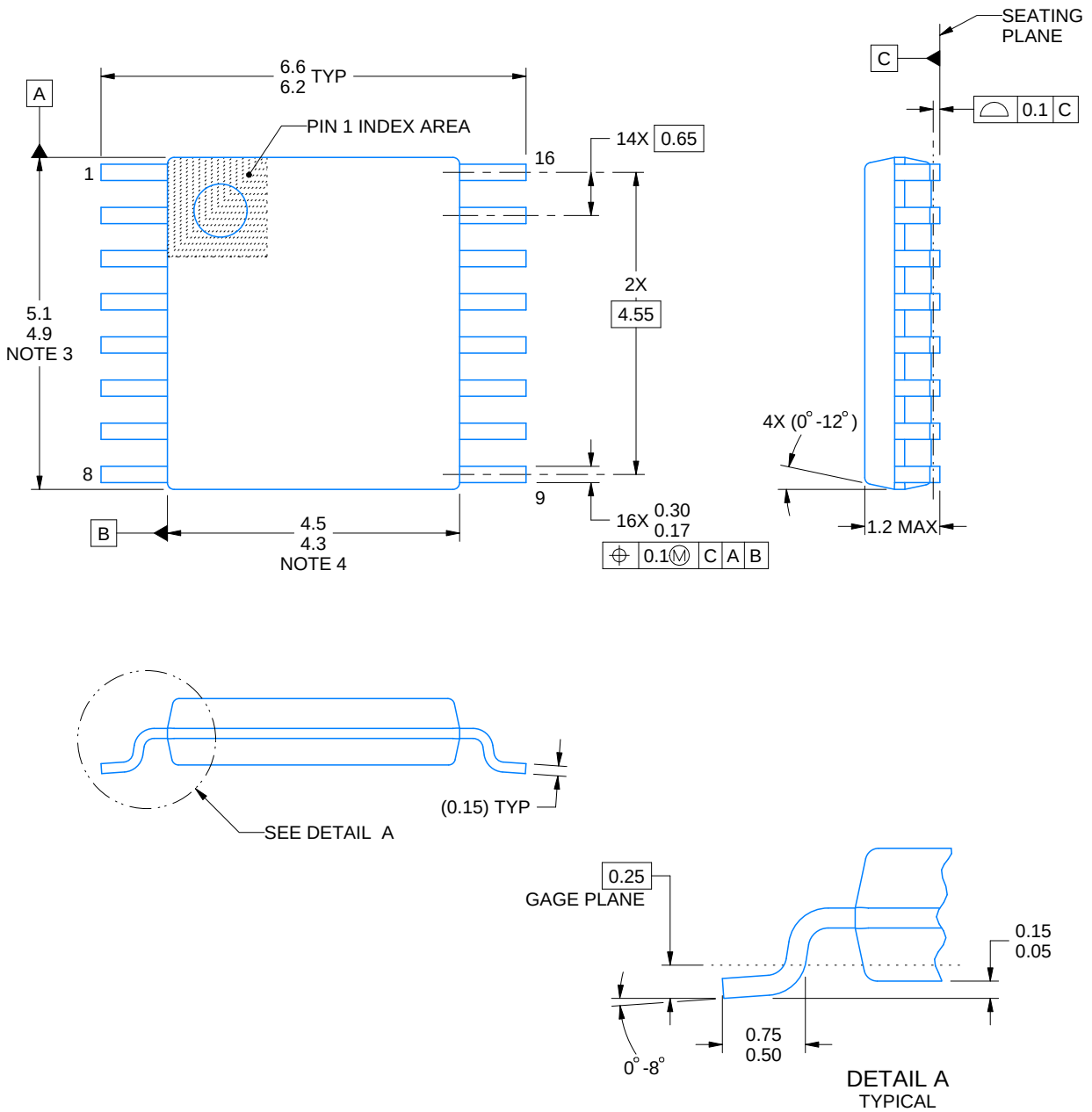
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
MSP430FR2310IPW16	PW	TSSOP	16	90	530	10.2	3600	3.5
MSP430FR2310IPW16.A	PW	TSSOP	16	90	530	10.2	3600	3.5
MSP430FR2310IPW20	PW	TSSOP	20	70	530	10.2	3600	3.5
MSP430FR2310IPW20.A	PW	TSSOP	20	70	530	10.2	3600	3.5
MSP430FR2311IPW16	PW	TSSOP	16	90	530	10.2	3600	3.5
MSP430FR2311IPW16.A	PW	TSSOP	16	90	530	10.2	3600	3.5
MSP430FR2311IPW20	PW	TSSOP	20	70	530	10.2	3600	3.5
MSP430FR2311IPW20.A	PW	TSSOP	20	70	530	10.2	3600	3.5

PACKAGE OUTLINE

PW0016A

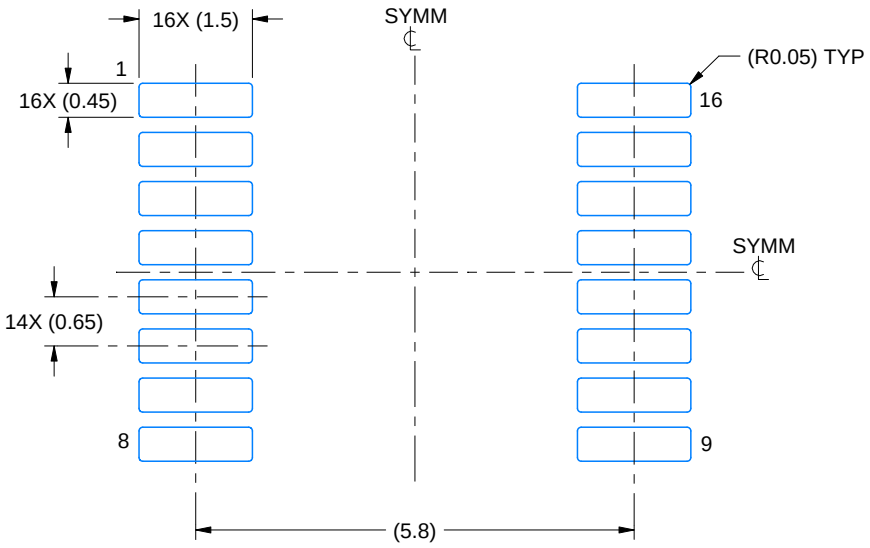
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

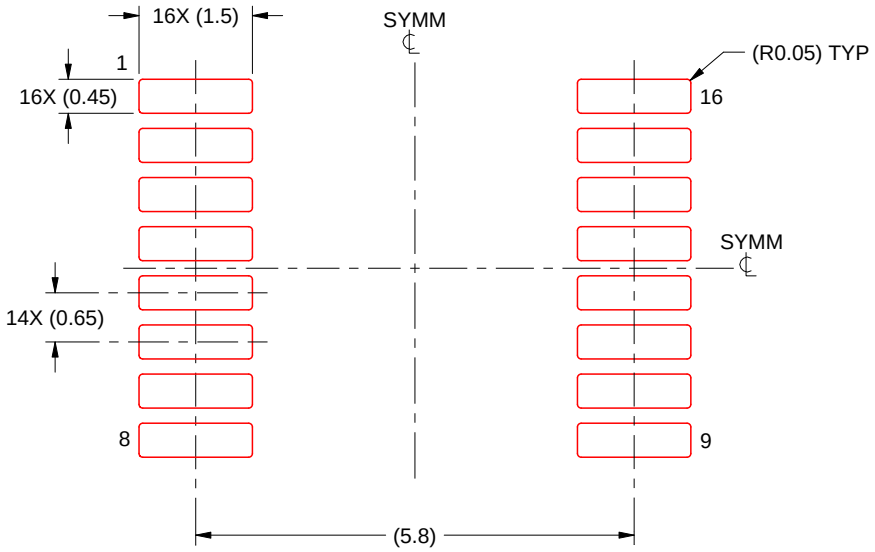


SOLDER MASK DETAILS

4220204/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220204/B 12/2023

NOTES: (continued)

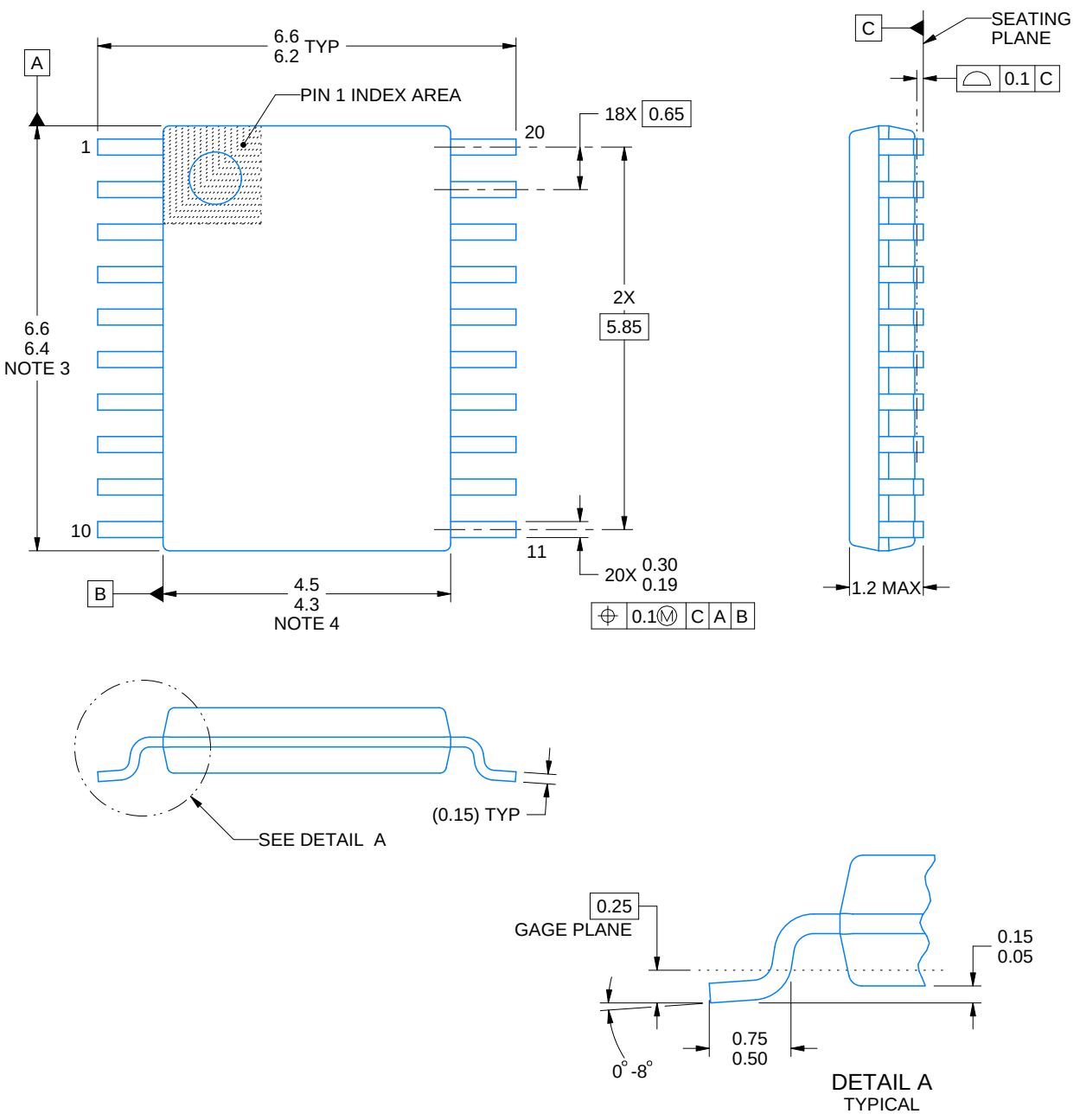
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

PW0020A

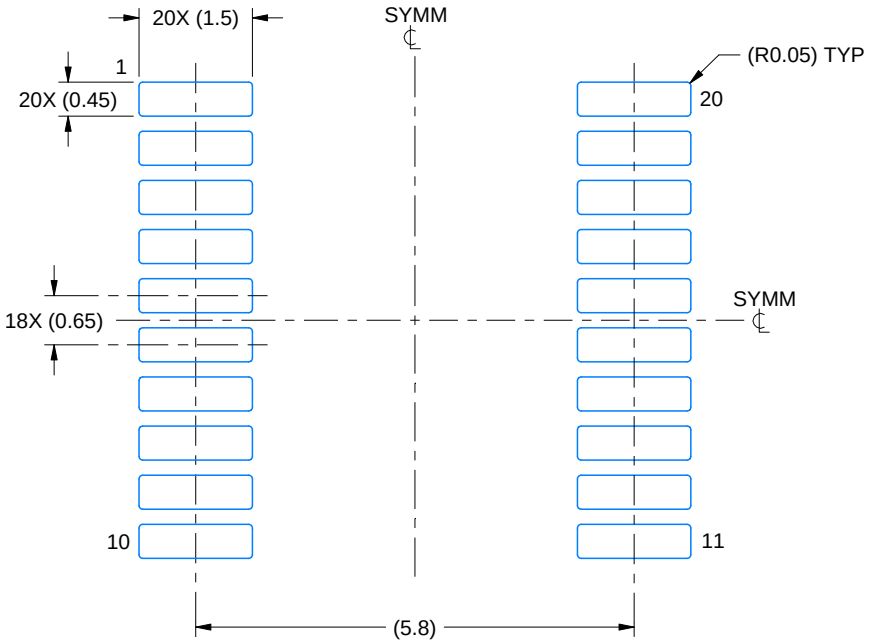
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

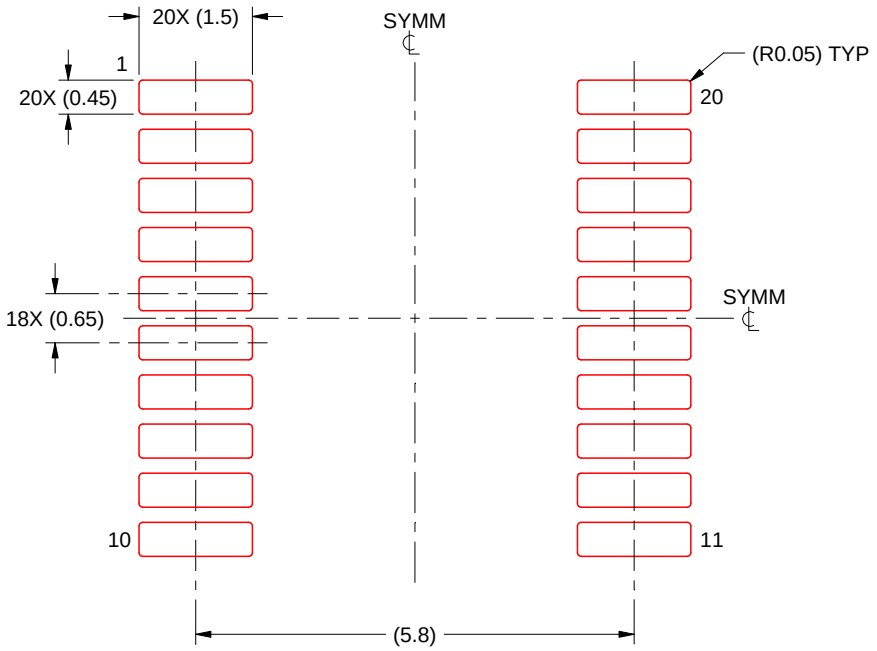


SOLDER MASK DETAILS

4220206/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220206/A 02/2017

NOTES: (continued)

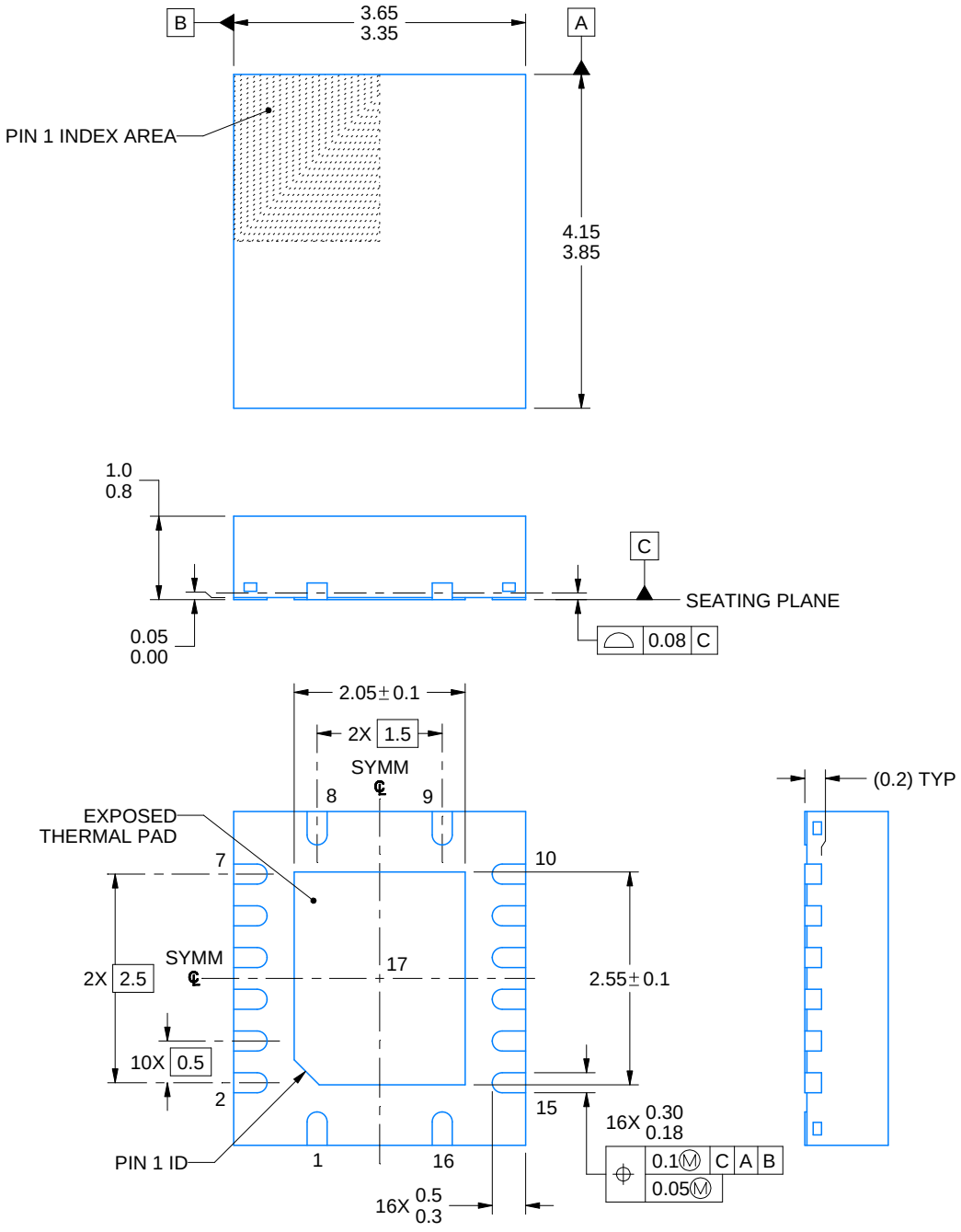
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

RGY0016A

PACKAGE OUTLINE

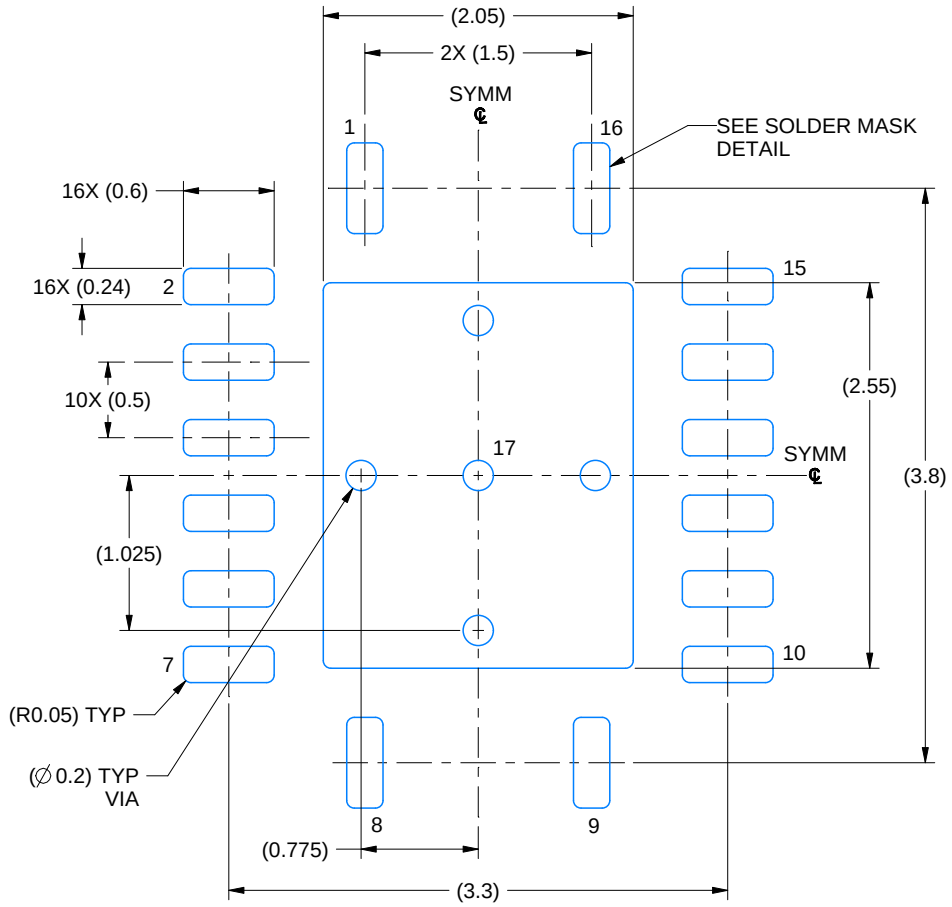
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

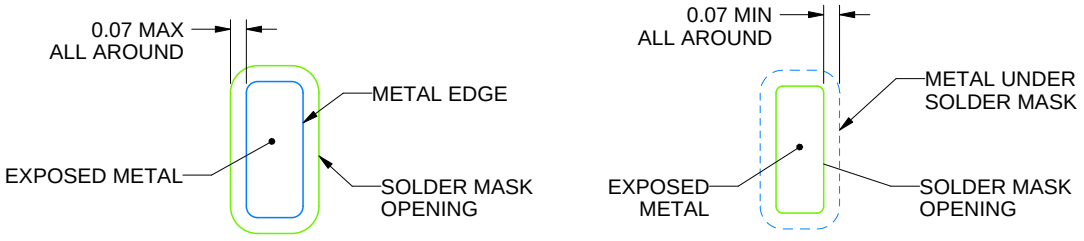


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X

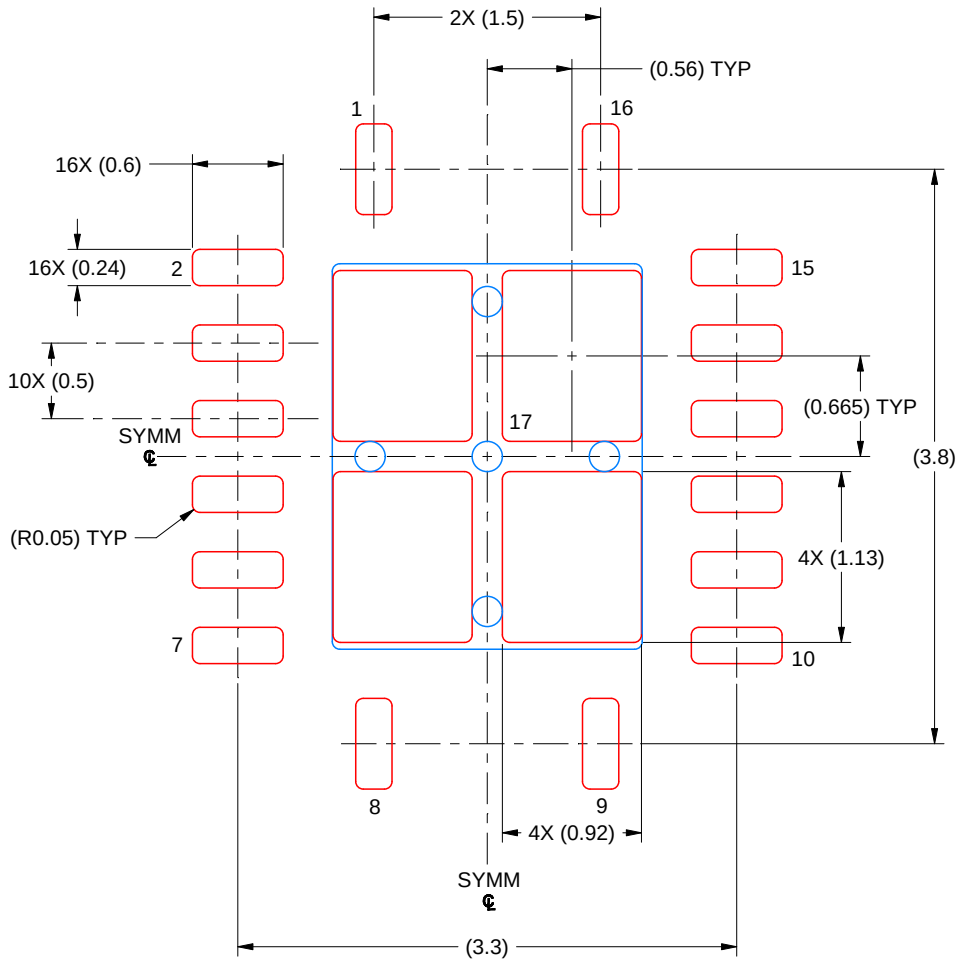


SOLDER MASK DETAILS

4225140/A 07/2019

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 20X

EXPOSED PAD 17
80% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

4225140/A 07/2019

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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最終更新日：2025 年 10 月