# MSP430FR2433 ミクスト・シグナル・マイクロコントローラ

## 1 デバイスの概要

### 1.1 特長

- 組み込みマイクロコントローラ
  - 16 ビットの RISC アーキテクチャ
  - 最高 16MHz のクロック周波数をサポート
  - 3.6V～1.8V の広い電源電圧範囲 (最小電源電圧は SVS レベルにより制限されます。「SVS 仕様」を参照)
- 最適化された超低消費電力モード
  - アクティブ・モード：126µA/MHz (標準値)
  - スタンバイ：VLO 使用で 1µA 未満
  - LPM3.5 リアルタイム・クロック (RTC) カウンタ、32,768Hz の水晶発振器を使用：730nA (標準値)
  - シャットダウン (LPM4.5)：16nA (標準値)
- 高性能アナログ
  - 8 チャネル、10 ビットの A/D コンバータ (ADC)
    - 内蔵の 1.5V 基準電圧
    - サンプル・アンド・ホールド 200ksps
- 拡張シリアル通信
  - 2 つの拡張ユニバーサル・シリアル通信インターフェイス (eUSCI_A) により UART、IrDA、SPI をサポート
  - 1 つの eUSCI (eUSCI_B) が SPI および $I^2C$ をサポート
- インテリジェントなデジタル・ペリフェラル
  - 4 つの 16 ビット・タイマ
    - 3 つのキャプチャ/比較レジスタを搭載したタイマ (Timer_A3) × 2
    - 2 つのキャプチャ/比較レジスタを搭載したタイマ (Timer_A2) × 2
  - 16 ビット・カウンタ専用 RTC × 1
  - 16 ビットの巡回冗長性検査 (CRC)
- 低消費電力の強誘電体 RAM (FRAM)
  - 最大 15.5KB の不揮発性メモリ
  - エラー訂正コード (ECC) 搭載
  - 書き込み保護を設定可能
  - プログラム、定数、ストレージの統合メモリ
  - 書き込みサイクルの耐久性：$10^{15}$ 回
  - 放射線耐性、非磁性
  - 高いFRAM:SRAM比、最大4:1
- クロック・システム (CS)
  - オンチップの 32kHz RC 発振器 (REFO)
  - オンチップの 16MHz デジタル制御発振器 (DCO)、周波数ロック・ループ (FLL) 付き
    - オンチップの基準電圧は室温で ±1% 精度
  - オンチップの超低周波数 10kHz 発振器 (VLO)
  - オンチップの高周波数変調発振器 (MODOSC)
  - 外付けの 32kHz 水晶発振器 (LFXT)
  - 1～128 の MCLK プリスケーラをプログラム可能
  - 1、2、4、8 のプログラマブル・プリスケーラを使って MCLK から SMCLK を生成
- 汎用入出力およびピン機能
  - VQFN-24 パッケージに合計 19 の I/O を搭載
  - 16 本の割り込みピン (P1 および P2) により、低消費電力モードから MCU をウェイクアップ可能
- 開発ツールとソフトウェア
  - 開発ツール
    - LaunchPad™開発キット (MSP-EXP430FR2433)
    - ターゲット開発ボード (MSP-TS430RGE24A)
- ファミリ・メンバー (「デバイスの比較」も参照)
  - MSP430FR2433：15KB のプログラム FRAM、512 バイトの情報 FRAM、4KB の RAM
- パッケージ・オプション
  - 24ピン：VQFN (RGE)
  - 24ピン：DSBGA (YQW)

### 1.2 アプリケーション

- 小型産業用センサ
- 低消費電力の医療、保健、フィットネス用機器
- 電子ドア・ロック
- エネルギー・ハーベスト

### 1.3 概要

MSP430FR2433マイクロコントローラ(MCU)は、超低コストのセンシング/測定用MCUファミリであるTIのMSP430™ バリュー・ライン・センシング製品に属しています。そのアーキテクチャ、FRAM、内蔵ペリフェラルは、多様な低消費電力モードと組み合わせることで、小型 VQFN パッケージ (4mm × 4mm) の携帯型バッテリ駆動センシング アプリケーションで長いバッテリ駆動時間を達成できるように最適化されています。

英語版のTI製品についての情報を翻訳したこの資料は、製品の概要を確認する目的で便宜的に提供しているものです。該当する正式な英語版の最新情報は、www.ti.comで閲覧でき、その内容が常に優先されます。TIでは翻訳の正確性および妥当性につきましては一切保証いたしません。実際の設計などの前には、必ず最新版の英語版をご参照くださいますようお願いいたします。

MSP430超低消費電力FRAMマイクロコントローラ・プラットフォームは、独自の組み込みFRAMと包括的な超低消費電力のシステム・アーキテクチャを組み合わせたもので、システム設計者は性能向上とエネルギー消費量削減を同時に実現できます。FRAMテクノロジは、RAMの低エネルギーでの高速書き込み、柔軟性、耐久性と、フラッシュの不揮発性を併せ持つものです。

MSP430FR2433 MCUは、ハードウェアおよびソフトウェアの大規模なエコシステムによってサポートされており、リファレンス・デザインやサンプル・コードを利用して設計をすぐに開始できます。開発キットには、MSP-EXP430FR2433 LaunchPad™開発キットとMSP-TS430RGE24A 24ピン・ターゲット開発ボードがあります。また、TI は無償の MSP430Ware™ ソフトウェアも提供しており、Code Composer Studio™ IDE デスクトップのコンポーネントとして利用できます。また、TI Resource Explorer ではクラウド・バージョンを利用できます。MSP430 MCU には、広範囲のオンライン資料、トレーニング、および E2E™ サポート・フォーラムによるオンライン・サポートも用意されています。

モジュールの詳細な説明については、*『MSP430FR4xx and MSP430FR2xx Family User's Guide』* (英語) を参照してください。

**製品情報(1)**

| 型番 | パッケージ | 本体サイズ (2) |
|---|---|---|
| MSP430FR2433IRGE | VQFN (24) | 4mm×4mm |
| MSP430FR2433IYQW | DSBGA (24) | 2.29mm×2.34mm |

(1) 最新の製品、パッケージ、および注文情報については、9の「*付録:パッケージ・オプション*」、または www.ti.comのTI Webサイトを参照してください。
(2) ここに記載されているサイズは概略です。許容公差を含めたパッケージの寸法については、9の「*メカニカル・データ*」を参照してください。

注意

電気的な過剰ストレスや、データやコード・メモリの不安定化を防止するため、デバイス・レベルのESD仕様に従って、システム・レベルのESD保護を適用する必要があります。詳細については、*『MSP430のシステム・レベルのESD考慮事項』*を参照してください。


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## 1.4 機能ブロック図

機能ブロック図を、図 1-1に示します。

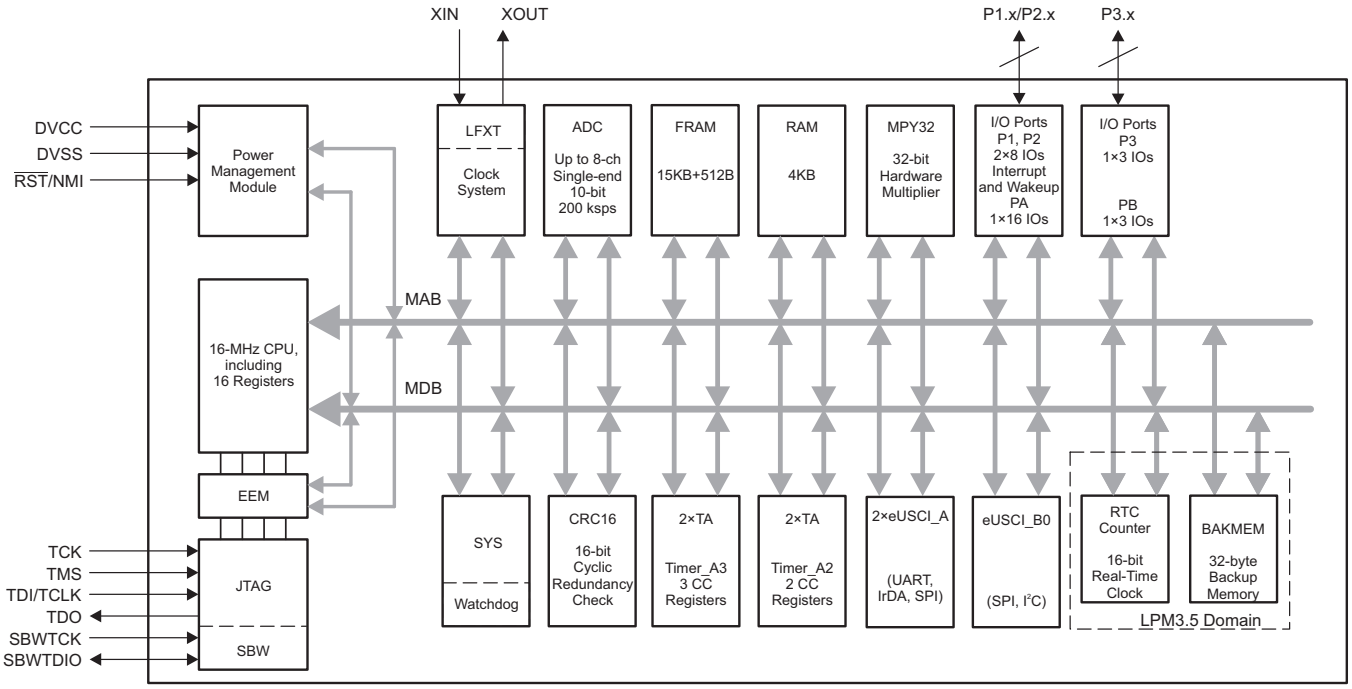


**図 1-1. 機能ブロック図**

- このMCUには、DVCCおよびDVSSの1つのメイン電源ペアがあり、デジタルとアナログの両方のモジュールへ電力を供給します。バイパスおよびデカップリング・コンデンサとしては、それぞれ4.7µF～10µFおよび0.1µFで、精度±5%が推奨されます。
- P1およびP2にはピン割り込み機能があり、LPM3.5およびLPM4を含むすべてのLPMからMCUをウェイクアップできます。
- 各Timer_A3には3つのキャプチャ/比較レジスタがありますが、外部的に接続されているのはCCR1およびCCR2のみです。CCR0レジスタは、内部的な期間のタイミングと割り込みの生成にのみ使用できます。
- 各Timer_A2には2つのキャプチャ/比較レジスタがありますが、比較/キャプチャ機能はCCR1のみです。CCR0レジスタは、内部的な期間のタイミングと割り込みの生成にのみ使用できます。
- LPM3.5モードでは、他のペリフェラルがオフの間もRTCモジュールは機能できます。

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# Table of Contents

**1 デバイスの概要 ..... 1**
1.1 特長 ..... 1
1.2 アプリケーション ..... 1
1.3 概要 ..... 1
1.4 機能ブロック図 ..... 3
**2 改訂履歴 ..... 5**
**3 Device Comparison ..... 7**
3.1 Related Products ..... 7
**4 Terminal Configuration and Functions ..... 8**
4.1 Pin Diagram ..... 8
4.2 Pin Attributes ..... 10
4.3 Signal Descriptions ..... 12
4.4 Pin Multiplexing ..... 15
4.5 Buffer Types ..... 15
4.6 Connection of Unused Pins ..... 15
**5 Specifications ..... 16**
5.1 Absolute Maximum Ratings ..... 16
5.2 ESD Ratings ..... 16
5.3 Recommended Operating Conditions ..... 16
5.4 Active Mode Supply Current Into $V_{CC}$ Excluding External Current ..... 17
5.5 Active Mode Supply Current Per MHz ..... 17
5.6 Low-Power Mode LPM0 Supply Currents Into $V_{CC}$ Excluding External Current ..... 17
5.7 Low-Power Mode (LPM3 and LPM4) Supply Currents (Into $V_{CC}$) Excluding External Current ..... 18
5.8 Low-Power Mode LPMx.5 Supply Currents (Into $V_{CC}$) Excluding External Current ..... 18
5.9 Typical Characteristics - Low-Power Mode Supply Currents ..... 19
5.10 Thermal Resistance Characteristics ..... 20
5.11 Timing and Switching Characteristics ..... 21
**6 Detailed Description ..... 40**
6.1 Overview ..... 40
6.2 CPU ..... 40
6.3 Operating Modes ..... 40
6.4 Interrupt Vector Addresses ..... 41
6.5 Bootloader (BSL) ..... 43
6.6 JTAG Standard Interface ..... 43
6.7 Spy-Bi-Wire Interface (SBW) ..... 44
6.8 FRAM ..... 44
6.9 Memory Protection ..... 44
6.10 Peripherals ..... 45
6.11 Input/Output Diagrams ..... 54
6.12 Device Descriptors ..... 60
6.13 Memory ..... 61
6.14 Identification ..... 69
**7 Applications, Implementation, and Layout ..... 70**
7.1 Device Connection and Layout Fundamentals ..... 70
7.2 Peripheral- and Interface-Specific Design Information ..... 73
**8 デバイスおよびドキュメントのサポート ..... 75**
8.1 使い始めと次の手順 ..... 75
8.2 デバイスの項目表記 ..... 75
8.3 ツールとソフトウェア ..... 76
8.4 ドキュメントのサポート ..... 78
8.5 Community Resources ..... 79
8.6 商標 ..... 79
8.7 静電気放電に関する注意事項 ..... 79
8.8 Export Control Notice ..... 79
8.9 Glossary ..... 79
**9 メカニカル、パッケージ、および注文情報 ..... 80**


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# 2 改訂履歴

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

## リビジョン E からリビジョン F への変更点

**2019年8月20日発行分から2019年12月9日発行分への変更** **Page**

- Changed the note that begins "Supply voltage changes faster than 0.2 V/µs can trigger a BOR reset..." in Section 5.3, *Recommended Operating Conditions* ..... 16
- Added the note that begins "TI recommends that power to the DVCC pin must not exceed the limits..." in Section 5.3, *Recommended Operating Conditions* ..... 16
- Changed the note that begins "A capacitor tolerance of ±20% or better is required..." in Section 5.3, *Recommended Operating Conditions* ..... 16
- Changed the note that begins "Requires external capacitors at both terminals..." in Table 5-4, *XT1 Crystal Oscillator (Low Frequency)* ..... 23
- Added the $t_{(int)}$ parameter in Table 5-10, *Digital Inputs* ..... 27
- Added the $t_{TA,cap}$ parameter in Table 5-13, *Timer_A* ..... 29
- Corrected the test conditions for the $R_{I,MUX}$ parameter in Table 5-20, *ADC, Power Supply and Input Range Conditions* ..... 35
- Added the note that begins "$t_{Sample} = \ln(2^{n+1}) \times \tau$ ..." in Table 5-21, *ADC, 10-Bit Timing Parameters* ..... 35
- Changed the CRC covered end address to 0x1AF5 in note (1) in Table 6-22, *Device Descriptors* ..... 60

## リビジョン D からリビジョン E への変更点

**2018年9月11日発行分から2019年08月19日発行分への変更** **Page**

- Added the $t_{TA,cap}$ parameter in Table 5-13, *Timer_A* ..... 29
- Changed the parameter symbol from $R_I$ to $R_{I,MUX}$ in Table 5-20 , *ADC, Power Supply and Input Range Conditions* . 35
- Added $R_{I,Misc}$ TYP value of 34 kΩ in Table 5-20 , *ADC, Power Supply and Input Range Conditions* ..... 35
- Added formula for $R_I$ calculation in Table 5-21 , *ADC, 10-Bit Timing Parameters* ..... 35
- Removed the description of "±3°C" in table note that starts "The device descriptor structure ..." of Table 5-22, *ADC, 10-Bit Linearity Parameters* ..... 36
- Corrected bitfield from IRDSEL to IRDSSEL in Section 6.10.8, *Timers (Timer0_A3, Timer1_A3, Timer2_A2 and Timer3_A2)*, in the description that starts "The interconnection of Timer0_A3 and ..." ..... 51
- Corrected the ADCINCHx column heading in Table 6-15, *ADC Channel Connections* ..... 53
- Corrected the ADCSHSx column heading in Table 6-16, *ADC Trigger Signal Connections* ..... 53
- Added P1SELC information in Table 6-32, *Port P1, P2 Registers (Base Address: 0200h)* ..... 64
- Added P2SELC information in Table 6-32, *Port P1, P2 Registers (Base Address: 0200h)* ..... 64
- Added P3SELC information in Table 6-33, *Port P3 Registers (Base Address: 0220h)* ..... 64

## リビジョン C からリビジョン D への変更点

**2018年8月29日発行分から2018年09月10日発行分への変更** **Page**

- Removed SYNC signal (not supported) from Figure 4-1, *32-Pin RHB Package (Top View)* ..... 8
- Combined two YQW pinout figures into one, and removed SYNC signal (not supported) in Figure 4-2, *24-Pin YQW Package (Top and Bottom Views)* ..... 9
- Added the $t_{TA,cap}$ parameter in Table 5-13, *Timer_A* ..... 29
- Removed SYNC signal (not supported) from figure and table in Section 6.11.2, *Port P2 (P2.0 to P2.2) Input/Output With Schmitt Trigger* ..... 56

## リビジョン B からリビジョン C への変更点

**2017年6月20日発行分から2018年08月28日発行分への変更** **Page**

- Updated Section 3.1, *Related Products* ..... 7

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- Corrected description of pin C5 on YQW package (changed from DVSS to NC) in Table 4-1, *Pin Attributes* ..... 11
- Corrected typos in the pin numbers of P2.3,5,6 in the RGE package in Table 4-2 ..... 13
- Corrected typos in the pin numbers of UCA1RXD and UCA1TXD in the RGE package in Table 4-2 ..... 14
- Changed description of NC pins from "No internal connection" to "No connection" in Table 4-2, *Signal Descriptions* 14
- Corrected package type in VQFN row (changed from QFN to VQFN) in Table 4-2, *Signal Descriptions* ..... 14
- Changed HBM limit to ±1000 V and CDM limit to ±250 V in Section 5.2, *ESD Ratings* ..... 16
- Added note to $V_{SVSH-}$ and $V_{SVSH+}$ parameters in Table 5-2, *PMM, SVS and BOR* ..... 21
- Added the $t_{TA,cap}$ parameter in Table 5-13, *Timer_A* ..... 29
- Moved "FRAM access time error" to "System Reset" row and added ACCTEIFG to interrupt flag column in Table 6-2, *Interrupt Sources, Flags, and Vectors* ..... 41
- Corrected the offset for P2SEL1 in Table 6-32, *Port P1, P2 Registers (Base Address: 0200h)* ..... 64
- 8.2「*デバイスの項目表記*」のテキストおよび図を更新 ..... 75

## リビジョン A からリビジョン B への変更点

**2017年6月9日発行分から2017年06月19日発行分への変更** **Page**

- 図 1-1「*機能ブロック図*」のFRAMおよびRAMのサイズを訂正 ..... 3
- Added the $t_{TA,cap}$ parameter in Table 5-13, *Timer_A* ..... 29

## 初版からリビジョン A への変更点

**2015年10月21日発行分から2017年06月8日発行分への変更** **Page**

- 一覧の「広い電源電圧範囲」を含む項目に注を追加 ..... 1
- 1.1「*特長*」の「パッケージ・オプション」一覧に DSBGA (YQW) パッケージを追加 ..... 1
- 1.3「*概要*」の*製品情報*の表にDSBGA (YQW)パッケージ・オプションを追加 ..... 2
- Added row for MSP430FR2433IYQW to Table 3-1, *Device Comparison* ..... 7
- Added Section 3.1, *Related Products* ..... 7
- Added DSBGA (YQW) package to Table 4-1, *Pin Attributes* ..... 10
- Added DSBGA (YQW) package to Table 4-2, *Signal Descriptions* ..... 12
- Added row for VQFN thermal pad ..... 14
- Removed FRAM reflow note ..... 16
- In the note that starts "Low-power mode 3, VLO, excludes SVS test conditions...", changed "$f_{XT1}$ = 0 Hz" to "$f_{XT1}$ = 32768 Hz" ..... 18
- Added DSBGA (YQW) package and changed notes for Section 5.10, *Thermal Resistance Characteristics* ..... 20
- Added note that starts "The VLO clock frequency is reduced by 15%..." ..... 26
- Added the $t_{TA,cap}$ parameter in Table 5-13, *Timer_A* ..... 29
- Removed ADCDIV from the formula for the TYP value in the second row of the $t_{CONVERT}$ parameter in Table 5-21, *ADC, 10-Bit Timing Parameters* (removed because ADCCLK is after division) ..... 35
- Added note to "Clock" in Table 6-1, *Operating Modes* ..... 40
- Added note that starts "XT1CLK and VLOCLK can be active during LPM4..." ..... 41
- Add description of blank device detection ..... 43
- Corrected description in Section 6.10.10, *Backup Memory (BKMEM)* ..... 52
- Changed the paragraph that starts "Quickly switching digital signals and ..." in Section 7.2.1.2, *Design Requirements* ..... 73
- 図 8-1「*デバイスの項目表記*」を更新 ..... 75
- 従来の「*開発ツールのサポート*」セクションを 8.3、「*ツールとソフトウェア*」に置き換え ..... 76
- 8.4「*ドキュメントのサポート*」の形式および内容を更新 ..... 78


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# 3 Device Comparison

Table 3-1 summarizes the features of the available family members.

**Table 3-1. Device Comparison(1)(2)**

| DEVICE | PROGRAM FRAM + INFORMATION FRAM (bytes) | SRAM (bytes) | TA0 TO TA3 | eUSCI_A | | eUSCI_B | 10-BIT ADC CHANNELS | GPIOs | PACKAGE |
|---|---|---|---|---|---|---|---|---|---|
| | | | | UART | SPI | | | | |
| MSP430FR2433IRGE | 15360 + 512 | 4096 | 2, 3 × CCR(3)<br>2, 2 × CCR | up to 2 | up to 2 | 1 | 8 | 19 | 24 RGE (VQFN) |
| MSP430FR2433IYQW | 15360 + 512 | 4096 | 2, 3 × CCR(3)<br>2, 2 × CCR | up to 2 | 1 | 1 | 8 | 17 | 24 YQW (DSBGA) |

(1) For the most current package and ordering information, see the *Package Option Addendum* in 9, or see the TI website at www.ti.com.
(2) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/packaging.
(3) A CCR register is a configurable register that provides internal and external capture or compare inputs, or internal and external PWM outputs.

## 3.1 Related Products

For information about other devices in this family of products or related products, see the following links.

TI 16-bit and 32-bit microcontrollers

High-performance, low-power solutions to enable the autonomous future

Products for MSP430 ultra-low-power sensing & measurement MCUs

One platform. One ecosystem. Endless possibilities.

Companion products for MSP430FR2433

Review products that are frequently purchased or used with this product.

Reference designs for MSP430FR2433

Find reference designs leveraging the best in TI technology – from analog and power management to embedded processors

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# 4 Terminal Configuration and Functions

## 4.1 Pin Diagram

Figure 4-1 shows the pinout of the 24-pin RGE package.

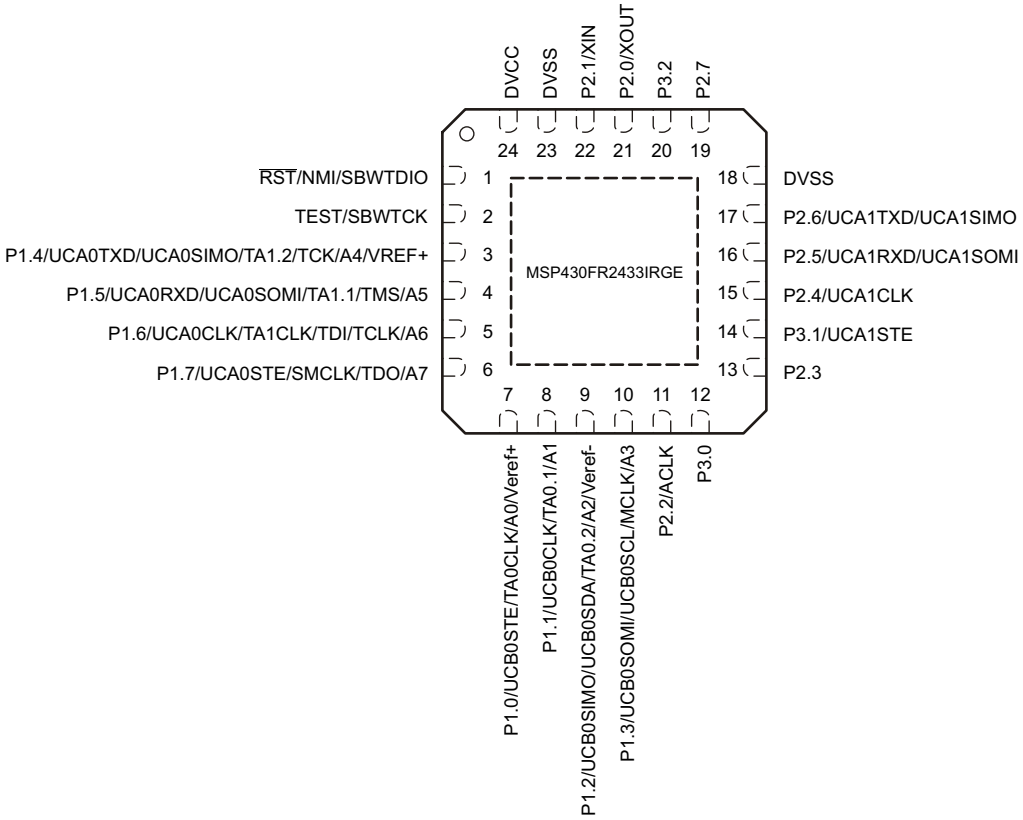


**Figure 4-1. 24-Pin RGE Package (Top View)**


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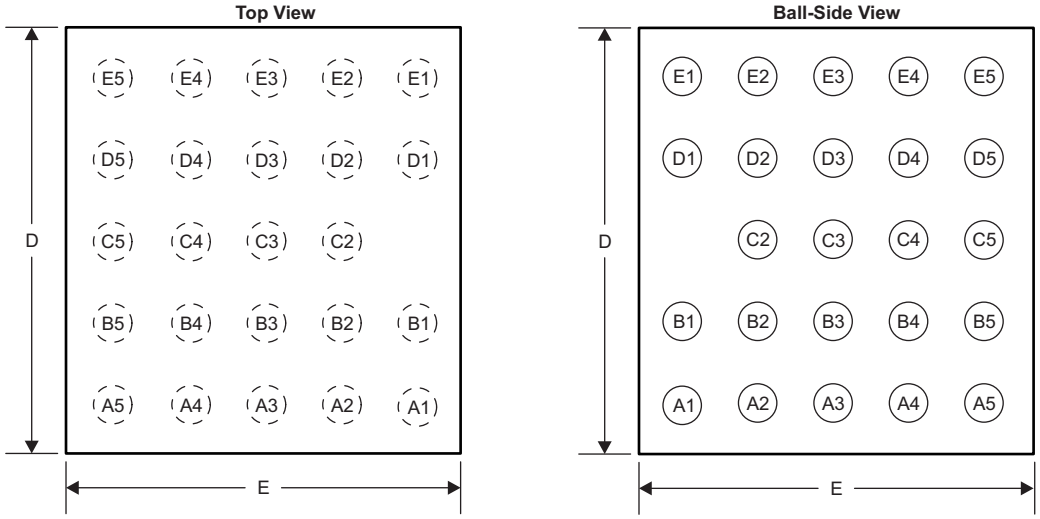
Figure 4-2 shows the pinout of the 24-pin YQW package.




| PIN NO. | SIGNAL NAME | PIN NO. | SIGNAL NAME |
|---|---|---|---|
| A1 | P1.1/UCB0CLK/TA0.1/A1 | C4 | NC |
| A2 | P1.3/UCB0SOMI/UCB0SCL/MCLK/A3 | C5 | NC |
| A3 | P2.2/ACLK | D1 | P1.4/UCA0TXD/UCA0SIMO/TA1.2/TCK/A4/VREF+ |
| A4 | P3.0 | D2 | TEST/SBWTCK |
| A5 | P2.3 | D3 | DVSS |
| B1 | P1.0/UCB0STE/TA0CLK/A0/Veref+ | D4 | P3.2 |
| B2 | P1.2/UCB0SIMO/UCB0SDA/TA0.2/A2/Veref- | D5 | NC |
| B3 | P1.7/UCA0STE/SMCLK/TDO/A7 | E1 | $\overline{\text{RST}}$/NMI/SBWTDIO |
| B4 | P2.5/UCA1RXD | E2 | DVCC |
| B5 | P2.6/UCA1TXD | E3 | P2.1/XIN |
| C2 | P1.5/UCA0RXD/UCA0SOMI/TA1.1/TMS/A5 | E4 | P2.0/XOUT |
| C3 | P1.6/UCA0CLK/TA1CLK/TDI/TCLK/A6 | E5 | P2.7 |

**Figure 4-2. 24-Pin YQW Package (Top and Bottom Views)**

## 4.2 Pin Attributes

Table 4-1 lists the attributes of all pins.

**Table 4-1. Pin Attributes**

| PIN NUMBER | | SIGNAL NAME(1) (2) | SIGNAL TYPE(3) | BUFFER TYPE(4) | POWER SOURCE(5) | RESET STATE AFTER BOR(6) |
|---|---|---|---|---|---|---|
| RGE | YQW | | | | | |
| 1 | E1 | $\overline{\text{RST}}$ (RD) | I | LVCMOS | DVCC | OFF |
| | | NMI | I | LVCMOS | DVCC | – |
| | | SBWTDIO | I/O | LVCMOS | DVCC | – |
| 2 | D2 | TEST (RD) | I | LVCMOS | DVCC | OFF |
| | | SBWTCK | I | LVCMOS | DVCC | – |
| 3 | D1 | P1.4 (RD) | I/O | LVCMOS | DVCC | OFF |
| | | UCA0TXD | O | LVCMOS | DVCC | – |
| | | UCA0SIMO | I/O | LVCMOS | DVCC | – |
| | | TA1.2 | I/O | LVCMOS | DVCC | – |
| | | TCK | I | LVCMOS | DVCC | – |
| | | A4 | I | Analog | DVCC | – |
| | | VREF+ | O | Power | DVCC | – |
| 4 | C2 | P1.5 (RD) | I/O | LVCMOS | DVCC | OFF |
| | | UCA0RXD | I | LVCMOS | DVCC | – |
| | | UCA0SOMI | I/O | LVCMOS | DVCC | – |
| | | TA1.1 | I/O | LVCMOS | DVCC | – |
| | | TMS | I | LVCMOS | DVCC | – |
| | | A5 | I | Analog | DVCC | – |
| 5 | C3 | P1.6 (RD) | I/O | LVCMOS | DVCC | OFF |
| | | UCA0CLK | I/O | LVCMOS | DVCC | – |
| | | TA1CLK | I | LVCMOS | DVCC | – |
| | | TDI | I | LVCMOS | DVCC | – |
| | | TCLK | I | LVCMOS | DVCC | – |
| | | A6 | I | Analog | DVCC | – |
| 6 | B3 | P1.7 (RD) | I/O | LVCMOS | DVCC | OFF |
| | | UCA0STE | I/O | LVCMOS | DVCC | – |
| | | SMCLK | O | LVCMOS | DVCC | – |
| | | TDO | O | LVCMOS | DVCC | – |
| | | A7 | I | Analog | DVCC | – |
| 7 | B1 | P1.0 (RD) | I/O | LVCMOS | DVCC | OFF |
| | | UCB0STE | I/O | LVCMOS | DVCC | – |
| | | TA0CLK | I | LVCMOS | DVCC | – |
| | | A0 | I | Analog | DVCC | – |
| | | Veref+ | I | Power | DVCC | – |

(1) Signals names with (RD) denote the reset default pin name.
(2) To determine the pin mux encodings for each pin, see Section 6.11, *Input/Output Diagrams*.
(3) Signal Types: I = Input, O = Output, I/O = Input or Output
(4) Buffer Types: LVCMOS, Analog, or Power (see Table 4-3)
(5) The power source shown in this table is the I/O power source, which may differ from the module power source.
(6) Reset States:
OFF = High-impedance with Schmitt trigger and pullup or pulldown (if available) disabled
N/A = Not applicable


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**Table 4-1. Pin Attributes (continued)**

| PIN NUMBER | | SIGNAL NAME(1) (2) | SIGNAL TYPE(3) | BUFFER TYPE(4) | POWER SOURCE(5) | RESET STATE AFTER BOR(6) |
|---|---|---|---|---|---|---|
| RGE | YQW | | | | | |
| 8 | A1 | P1.1 (RD) | I/O | LVCMOS | DVCC | OFF |
| | | UCB0CLK | I/O | LVCMOS | DVCC | – |
| | | TA0.1 | I/O | LVCMOS | DVCC | – |
| | | A1 | I | Analog | DVCC | – |
| 9 | B2 | P1.2 (RD) | I/O | LVCMOS | DVCC | OFF |
| | | UCB0SIMO | I/O | LVCMOS | DVCC | – |
| | | UCB0SDA | I/O | LVCMOS | DVCC | – |
| | | TA0.2 | I/O | LVCMOS | DVCC | – |
| | | A2 | I | Analog | DVCC | – |
| | | Veref- | I | Power | DVCC | – |
| 10 | A2 | P1.3 (RD) | I/O | LVCMOS | DVCC | OFF |
| | | UCB0SOMI | I/O | LVCMOS | DVCC | – |
| | | UCB0SCL | I/O | LVCMOS | DVCC | – |
| | | MCLK | O | LVCMOS | DVCC | – |
| | | A3 | I | Analog | DVCC | – |
| 11 | A3 | P2.2 (RD) | I/O | LVCMOS | DVCC | OFF |
| | | ACLK | I/O | LVCMOS | DVCC | – |
| 12 | A4 | P3.0 | I/O | LVCMOS | DVCC | OFF |
| 13 | A5 | P2.3 | I/O | LVCMOS | DVCC | OFF |
| 14 | – | P3.1 (RD) | I/O | LVCMOS | DVCC | OFF |
| | | UCA1STE | I/O | LVCMOS | DVCC | – |
| 15 | – | P2.4 (RD) | I/O | LVCMOS | DVCC | OFF |
| | | UCA1CLK | I/O | LVCMOS | DVCC | – |
| 16 | B4 | P2.5 (RD) | I/O | LVCMOS | DVCC | OFF |
| | | UCA1RXD | I | LVCMOS | DVCC | – |
| | | UCA1SOMI | I/O | LVCMOS | DVCC | – |
| 17 | B5 | P2.6 (RD) | I/O | LVCMOS | DVCC | OFF |
| | | UCA1TXD | O | LVCMOS | DVCC | – |
| | | UCA1SIMO | I/O | LVCMOS | DVCC | – |
| 18 | – | DVSS | P | Power | DVCC | N/A |
| – | C5 | NC | – | – | – | – |
| 19 | E5 | P2.7 | I/O | LVCMOS | DVCC | OFF |
| 20 | D4 | P3.2 | I/O | LVCMOS | DVCC | OFF |
| 21 | E4 | P2.0 (RD) | I/O | LVCMOS | DVCC | OFF |
| | | XOUT | O | LVCMOS | DVCC | – |
| 22 | E3 | P2.1 (RD) | I/O | LVCMOS | DVCC | OFF |
| | | XIN | I | LVCMOS | DVCC | – |
| 23 | D3 | DVSS | P | Power | DVCC | N/A |
| 24 | E2 | DVCC | P | Power | DVCC | N/A |

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## 4.3 Signal Descriptions

Table 4-2 describes the device signals.

**Table 4-2. Signal Descriptions**

| FUNCTION | SIGNAL NAME | PIN NUMBER | | PIN TYPE(1) | DESCRIPTION |
|---|---|---|---|---|---|
| | | RGE | YQW | | |
| ADC | A0 | 7 | B1 | I | Analog input A0 |
| | A1 | 8 | A1 | I | Analog input A1 |
| | A2 | 9 | B2 | I | Analog input A2 |
| | A3 | 10 | A2 | I | Analog input A3 |
| | A4 | 3 | D1 | I | Analog input A4 |
| | A5 | 4 | C2 | I | Analog input A5 |
| | A6 | 5 | C3 | I | Analog input A6 |
| | A7 | 6 | B3 | I | Analog input A7 |
| | Veref+ | 7 | B1 | I | ADC positive reference |
| | Veref- | 9 | B2 | I | ADC negative reference |
| Clock | ACLK | 11 | A3 | O | ACLK output |
| | MCLK | 10 | A2 | O | MCLK output |
| | SMCLK | 6 | B3 | O | SMCLK output |
| | XIN | 22 | E3 | I | Input terminal for crystal oscillator |
| | XOUT | 21 | E4 | O | Output terminal for crystal oscillator |
| Debug | SBWTCK | 2 | D2 | I | Spy-Bi-Wire input clock |
| | SBWTDIO | 1 | E1 | I/O | Spy-Bi-Wire data input/output |
| | TCK | 3 | D1 | I | Test clock |
| | TCLK | 5 | C3 | I | Test clock input |
| | TDI | 5 | C3 | I | Test data input |
| | TDO | 6 | B3 | O | Test data output |
| | TEST | 2 | D2 | I | Test Mode pin – selected digital I/O on JTAG pins |
| | TMS | 4 | C2 | I | Test mode select |

(1) Pin Types: I = Input, O = Output, I/O = Input or Output, P = Power


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**Table 4-2. Signal Descriptions (continued)**

| FUNCTION | SIGNAL NAME | PIN NUMBER | | PIN TYPE(1) | DESCRIPTION |
|---|---|---|---|---|---|
| | | RGE | YQW | | |
| GPIO | P1.0 | 7 | B1 | I/O | General-purpose I/O |
| | P1.1 | 8 | A1 | I/O | General-purpose I/O |
| | P1.2 | 9 | B2 | I/O | General-purpose I/O |
| | P1.3 | 10 | A2 | I/O | General-purpose I/O |
| | P1.4 | 3 | D1 | I/O | General-purpose I/O(2) |
| | P1.5 | 4 | C2 | I/O | General-purpose I/O(2) |
| | P1.6 | 5 | C3 | I/O | General-purpose I/O(2) |
| | P1.7 | 6 | B3 | I/O | General-purpose I/O(2) |
| | P2.0 | 21 | E4 | I/O | General-purpose I/O |
| | P2.1 | 22 | E3 | I/O | General-purpose I/O |
| | P2.2 | 11 | A3 | I/O | General-purpose I/O |
| | P2.3 | 13 | A5 | I/O | General-purpose I/O |
| | P2.4 | 15 | – | I/O | General-purpose I/O |
| | P2.5 | 16 | B4 | I/O | General-purpose I/O |
| | P2.6 | 17 | B5 | I/O | General-purpose I/O |
| | P2.7 | 19 | E5 | I/O | General-purpose I/O |
| | P3.0 | 12 | A4 | I/O | General-purpose I/O |
| | P3.1 | 14 | – | I/O | General-purpose I/O |
| | P3.2 | 20 | D4 | I/O | General-purpose I/O |
| $I^2C$ | UCB0SCL | 10 | A2 | I/O | eUSCI_B0 $I^2C$ clock |
| | UCB0SDA | 9 | B2 | I/O | eUSCI_B0 $I^2C$ data |
| Power | DVCC | 24 | E2 | P | Power supply |
| | DVSS | 23 | D3 | P | Power ground |
| | VREF+ | 3 | D1 | P | Output of positive reference voltage with ground as reference |
| SPI | UCA0CLK | 5 | C3 | I/O | eUSCI_A0 SPI clock input/output |
| | UCA0SIMO | 3 | D1 | I/O | eUSCI_A0 SPI slave in/master out |
| | UCA0SOMI | 4 | C2 | I/O | eUSCI_A0 SPI slave out/master in |
| | UCA0STE | 6 | B3 | I/O | eUSCI_A0 SPI slave transmit enable |
| | UCA1CLK | 15 | – | I/O | eUSCI_A1 SPI clock input/output |
| | UCA1SIMO | 17 | B5 | I/O | eUSCI_A1 SPI slave in/master out |
| | UCA1SOMI | 16 | B4 | I/O | eUSCI_A1 SPI slave out/master in |
| | UCA1STE | 14 | – | I/O | eUSCI_A1 SPI slave transmit enable |
| | UCB0CLK | 8 | A1 | I/O | eUSCI_B0 clock input/output |
| | UCB0SIMO | 9 | B2 | I/O | eUSCI_B0 SPI slave in/master out |
| | UCB0SOMI | 10 | A2 | I/O | eUSCI_B0 SPI slave out/master in |
| | UCB0STE | 7 | B1 | I/O | eUSCI_B0 slave transmit enable |
| System | NMI | 1 | E1 | I | Nonmaskable interrupt input |
| | $\overline{RST}$ | 1 | E1 | I | Active-low reset input |

(2) Because this pin is multiplexed with the JTAG function, TI recommends disabling the pin interrupt function while in JTAG debug to prevent collisions.

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**Table 4-2. Signal Descriptions (continued)**

| FUNCTION | SIGNAL NAME | PIN NUMBER | | PIN TYPE(1) | DESCRIPTION |
|---|---|---|---|---|---|
| | | RGE | YQW | | |
| Timer_A | TA0.1 | 8 | A1 | I/O | Timer TA0 CCR1 capture: CCI1A input, compare: Out1 outputs |
| | TA0.2 | 9 | B2 | I/O | Timer TA0 CCR2 capture: CCI2A input, compare: Out2 outputs |
| | TA0CLK | 7 | B1 | I | Timer clock input TACLK for TA0 |
| | TA1.1 | 4 | C2 | I/O | Timer TA1 CCR1 capture: CCI1A input, compare: Out1 outputs |
| | TA1.2 | 3 | D1 | I/O | Timer TA1 CCR2 capture: CCI2A input, compare: Out2 outputs |
| | TA1CLK | 5 | C3 | I | Timer clock input TACLK for TA1 |
| UART | UCA0RXD | 4 | C2 | I | eUSCI_A0 UART receive data |
| | UCA0TXD | 3 | D1 | O | eUSCI_A0 UART transmit data |
| | UCA1RXD | 16 | B4 | I | eUSCI_A1 UART receive data |
| | UCA1TXD | 17 | B5 | O | eUSCI_A1 UART transmit data |
| No connection | NC | | C4, C5, D5 | I/O | No connection |
| VQFN Pad | VQFN thermal pad | Pad | N/A | | VQFN package exposed thermal pad. Connection to $V_{SS}$ is recommended |


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## 4.4 Pin Multiplexing

Pin multiplexing for these MCUs is controlled by both register settings and operating modes (for example, if the MCU is in test mode). For details of the settings for each pin and schematics of the multiplexed ports, see Section 6.11.

## 4.5 Buffer Types

Table 4-3 defines the pin buffer types that are listed in Table 4-1.

**Table 4-3. Buffer Types**

| BUFFER TYPE (STANDARD) | NOMINAL VOLTAGE | HYSTERESIS | PU OR PD | NOMINAL PU OR PD STRENGTH (µA) | OUTPUT DRIVE STRENGTH (mA) | OTHER CHARACTERISTICS |
|---|---|---|---|---|---|---|
| LVCMOS | 3.0 V | Y(1) | Programmable | See Section 5.11.4 | See Section 5.11.4 | |
| Analog | 3.0 V | N | N/A | N/A | N/A | See analog modules in Section 5 for details. |
| Power (DVCC) | 3.0 V | N | N/A | N/A | N/A | SVS enables hysteresis on DVCC. |
| Power (AVCC) | 3.0 V | N | N/A | N/A | N/A | |

(1) Only for input pins.

## 4.6 Connection of Unused Pins

Table 4-4 lists the correct termination of unused pins.

**Table 4-4. Connection of Unused Pins(1)**

| PIN | POTENTIAL | COMMENT |
|---|---|---|
| Px.0 to Px.7 | Open | Switched to port function, output direction (PxDIR.n = 1) |
| $\overline{\text{RST}}$/NMI | $DV_{CC}$ | 47-kΩ pullup or internal pullup selected with 10-nF (or 1.1-nF) pulldown(2) |
| TEST | Open | This pin always has an internal pulldown enabled. |

(1) Any unused pin with a secondary function that is shared with general-purpose I/O should follow the Px.0 to Px.7 unused pin connection guidelines.
(2) The pulldown capacitor should not exceed 1.1 nF when using MCUs with Spy-Bi-Wire interface in Spy-Bi-Wire mode with TI tools like FET interfaces or GANG programmers.

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# 5 Specifications

## 5.1 Absolute Maximum Ratings(1)

over operating free-air temperature range (unless otherwise noted)

| | MIN | MAX | UNIT |
|---|---|---|---|
| Voltage applied at DVCC pin to $V_{SS}$ | –0.3 | 4.1 | V |
| Voltage applied to any other pin(2) | –0.3 | $V_{CC}$ + 0.3 (4.1 V Max) | V |
| Diode current at any device pin | | ±2 | mA |
| Maximum junction temperature, $T_J$ | | 85 | °C |
| Storage temperature, $T_{stg}$(3) | –40 | 125 | °C |

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages referenced to $V_{SS}$.
(3) Higher temperature may be applied during board soldering according to the current JEDEC J-STD-020 specification with peak reflow temperatures not higher than classified on the device label on the shipping boxes or reels.

## 5.2 ESD Ratings

| | | | VALUE | UNIT |
|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1) | ±1000 | V |
| | | Charged-device model (CDM), per JEDEC specification JESD22-C101(2) | ±250 | |

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Pins listed as ±1000 V may actually have higher performance.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Pins listed as ±250 V may actually have higher performance.

## 5.3 Recommended Operating Conditions

| | | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage applied at DVCC pin(1)(2)(3)(4) | | 1.8 | | 3.6 | V |
| $V_{SS}$ | Supply voltage applied at DVSS pin | | | 0 | | V |
| $T_A$ | Operating free-air temperature | | –40 | | 85 | °C |
| $T_J$ | Operating junction temperature | | –40 | | 85 | °C |
| $C_{DVCC}$ | Recommended capacitor at DVCC(5) | | 4.7 | 10 | | µF |
| $f_{SYSTEM}$ | Processor frequency (maximum MCLK frequency)(6) | No FRAM wait states (NWAITSx = 0) | 0 | | 8 | MHz |
| | | With FRAM wait states (NWAITSx = 1)(7) | 0 | | 16(8) | |
| $f_{ACLK}$ | Maximum ACLK frequency | | | | 40 | kHz |
| $f_{SMCLK}$ | Maximum SMCLK frequency | | | | 16(8) | MHz |

(1) Supply voltage changes faster than 0.2 V/µs can trigger a BOR reset even within the recommended supply voltage range. Following the data sheet recommendation for capacitor $C_{DVCC}$ limits the slopes accordingly.
(2) Modules may have a different supply voltage range specification. See the specification of the respective module in this data sheet.
(3) TI recommends that power to the DVCC pin must not exceed the limits specified in *Recommended Operating Conditions*. Exceeding the specified limits can cause malfunction of the device including erroneous writes to RAM and FRAM.
(4) The minimum supply voltage is defined by the SVS levels. See the SVS threshold parameters in Table 5-2.
(5) A capacitor tolerance of ±20% or better is required. A low-ESR ceramic capacitor of 100 nF (minimum) should be placed as close as possible (within a few millimeters) to the respective pin pair.
(6) Modules may have a different maximum input clock specification. See the specification of the respective module in this data sheet.
(7) Wait states only occur on actual FRAM accesses (that is, on FRAM cache misses). RAM and peripheral accesses are always executed without wait states.
(8) If clock sources such as HF crystals or the DCO with frequencies >16 MHz are used, the clock must be divided in the clock system to comply with this operating condition.


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## 5.4 Active Mode Supply Current Into $V_{CC}$ Excluding External Current(1)

$V_{CC}$ = 3 V, $T_A$ = 25°C (unless otherwise noted)

| PARAMETER | EXECUTION MEMORY | TEST CONDITION | FREQUENCY ($f_{MCLK}$ = $f_{SMCLK}$) | | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | 1 MHz 0 WAIT STATES (NWAITSx = 0) | | 8 MHz 0 WAIT STATES (NWAITSx = 0) | | 16 MHz 1 WAIT STATE (NWAITSx = 1) | | |
| | | | TYP | MAX | TYP | MAX | TYP | MAX | |
| $I_{AM,\ FRAM}$(0%) | FRAM 0% cache hit ratio | 3 V, 25°C | 504 | | 2772 | | 3047 | 3480 | µA |
| | | 3 V, 85°C | 516 | | 2491 | | 2871 | | |
| $I_{AM,\ FRAM}$(100%) | FRAM 100% cache hit ratio | 3 V, 25°C | 203 | | 625 | | 1000 | 1215 | µA |
| | | 3 V, 85°C | 212 | | 639 | | 1016 | | |
| $I_{AM,\ RAM}$(2) | RAM | 3 V, 25°C | 229 | | 818 | | 1377 | | µA |

(1) All inputs are tied to 0 V or to $V_{CC}$. Outputs do not source or sink any current. Characterized with program executing typical data processing.
$f_{ACLK}$ = 32768 Hz, $f_{MCLK}$ = $f_{SMCLK}$ = $f_{DCO}$ at specified frequency
Program and data entirely reside in FRAM. All execution is from FRAM.
(2) Program and data reside entirely in RAM. All execution is from RAM. No access to FRAM.

## 5.5 Active Mode Supply Current Per MHz

$V_{CC}$ = 3 V, $T_A$ = 25°C (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | TYP | UNIT |
|---|---|---|---|---|
| $dI_{AM,FRAM}/df$ | Active mode current consumption per MHz, execution from FRAM, no wait states | [$I_{AM}$ (75% cache hit rate) at 8 MHz – $I_{AM}$ (75% cache hit rate) at 1 MHz)] / 7 MHz | 126 | µA/MHz |

## 5.6 Low-Power Mode LPM0 Supply Currents Into $V_{CC}$ Excluding External Current

$V_{CC}$ = 3 V, $T_A$ = 25°C (unless otherwise noted)(1)(2)

| PARAMETER | $V_{CC}$ | FREQUENCY ($f_{SMCLK}$) | | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | 1 MHz | | 8 MHz | | 16 MHz | | |
| | | TYP | MAX | TYP | MAX | TYP | MAX | |
| $I_{LPM0}$ | 2 V | 156 | | 328 | | 420 | | µA |
| | 3 V | 166 | | 342 | | 433 | | |

(1) All inputs are tied to 0 V or to $V_{CC}$. Outputs do not source or sink any current.
(2) Current for watchdog timer clocked by SMCLK included.
$f_{ACLK}$ = 32768 Hz, $f_{MCLK}$ = 0 MHz, $f_{SMCLK}$ at specified frequency.

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## 5.7 Low-Power Mode (LPM3 and LPM4) Supply Currents (Into $V_{CC}$) Excluding External Current

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (1)

| PARAMETER | | $V_{CC}$ | –40°C | | 25°C | | 85°C | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | TYP | MAX | TYP | MAX | TYP | MAX | |
| $I_{LPM3,XT1}$ | Low-power mode 3, 12.5-pF crystal, includes SVS (2)(3)(4) | 3 V | 0.98 | | 1.18 | 1.65 | 3.24 | | µA |
| | | 2 V | 0.96 | | 1.16 | | 3.21 | | |
| $I_{LPM3,VLO}$ | Low-power mode 3, VLO, excludes SVS (5) | 3 V | 0.78 | | 0.98 | 1.40 | 3.04 | | µA |
| | | 2 V | 0.76 | | 0.96 | | 3.01 | | |
| $I_{LPM3,\ RTC}$ | Low-power mode 3, RTC, excludes SVS (6) (see Figure 5-1) | 3 V | 0.93 | | 1.13 | | 3.19 | | µA |
| $I_{LPM4,\ SVS}$ | Low-power mode 4, includes SVS | 3 V | 0.51 | | 0.65 | | 2.65 | | µA |
| | | 2 V | 0.49 | | 0.64 | | 2.63 | | |
| $I_{LPM4}$ | Low-power mode 4, excludes SVS | 3 V | 0.35 | | 0.49 | | 2.49 | | µA |
| | | 2 V | 0.34 | | 0.48 | | 2.46 | | |

(1) All inputs are tied to 0 V or to $V_{CC}$. Outputs do not source or sink any current.
(2) Not applicable for MCUs with HF crystal oscillator only.
(3) Characterized with a Micro Crystal MS1V-T1K crystal with a load capacitance of 12.5 pF. The internal and external load capacitance are chosen to closely match the required 12.5-pF load.
(4) Low-power mode 3, 12.5-pF crystal, includes SVS test conditions:
Current for watchdog timer clocked by ACLK and RTC clocked by XT1 included. Current for brownout and SVS included (SVSHE = 1).
CPUOFF = 1, SCG0 = 1 SCG1 = 1, OSCOFF = 0 (LPM3),
$f_{XT1}$ = 32768 Hz, $f_{ACLK} = f_{XT1}$, $f_{MCLK} = f_{SMCLK}$ = 0 MHz
(5) Low-power mode 3, VLO, excludes SVS test conditions:
Current for watchdog timer clocked by VLO included. RTC disabled. Current for brownout included. SVS disabled (SVSHE = 0).
CPUOFF = 1, SCG0 = 1 SCG1 = 1, OSCOFF = 0 (LPM3)
$f_{XT1}$ = 32768 Hz, $f_{ACLK} = f_{MCLK} = f_{SMCLK}$ = 0 MHz
(6) RTC periodically wakes up every second with external 32768-Hz input as source.

## 5.8 Low-Power Mode LPMx.5 Supply Currents (Into $V_{CC}$) Excluding External Current

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | $V_{CC}$ | –40°C | | 25°C | | 85°C | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | TYP | MAX | TYP | MAX | TYP | MAX | |
| $I_{LPM3.5,\ XT1}$ | Low-power mode 3.5, 12.5-pF crystal, includes SVS (1)(2)(3) (see Figure 5-2) | 3 V | 0.65 | | 0.73 | 0.95 | 0.99 | 1.42 | µA |
| | | 2 V | 0.63 | | 0.71 | | 0.87 | | |
| $I_{LPM4.5,\ SVS}$ | Low-power mode 4.5, includes SVS (4) (see Figure 5-3) | 3 V | 0.22 | | 0.24 | 0.31 | 0.30 | 0.38 | µA |
| | | 2 V | 0.21 | | 0.23 | | 0.28 | | |
| $I_{LPM4.5}$ | Low-power mode 4.5, excludes SVS (5) | 3 V | 0.012 | | 0.016 | 0.055 | 0.061 | 0.120 | µA |
| | | 2 V | 0.002 | | 0.007 | | 0.044 | | |

(1) Not applicable for MCUs with HF crystal oscillator only.
(2) Characterized with a Micro Crystal MS1V-T1K crystal with a load capacitance of 12.5 pF. The internal and external load capacitance are chosen to closely match the required 12.5-pF load.
(3) Low-power mode 3.5, 12.5-pF crystal, includes SVS test conditions:
Current for RTC clocked by XT1 included. Current for brownout and SVS included (SVSHE = 1). Core regulator disabled.
PMMREGOFF = 1, CPUOFF = 1, SCG0 = 1 SCG1 = 1, OSCOFF = 1 (LPMx.5),
$f_{XT1}$ = 32768 Hz, $f_{ACLK}$ = 0, $f_{MCLK} = f_{SMCLK}$ = 0 MHz
(4) Low-power mode 4.5, includes SVS test conditions:
Current for brownout and SVS included (SVSHE = 1). Core regulator disabled.
PMMREGOFF = 1, CPUOFF = 1, SCG0 = 1 SCG1 = 1, OSCOFF = 1 (LPMx.5),
$f_{XT1}$ = 0 Hz, $f_{ACLK} = f_{MCLK} = f_{SMCLK}$ = 0 MHz
(5) Low-power mode 4.5, excludes SVS test conditions:
Current for brownout included. SVS disabled (SVSHE = 0). Core regulator disabled.
PMMREGOFF = 1, CPUOFF = 1, SCG0 = 1 SCG1 = 1, OSCOFF = 1 (LPMx.5),
$f_{XT1}$ = 0 Hz, $f_{ACLK} = f_{MCLK} = f_{SMCLK}$ = 0 MHz


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## 5.9 Typical Characteristics - Low-Power Mode Supply Currents

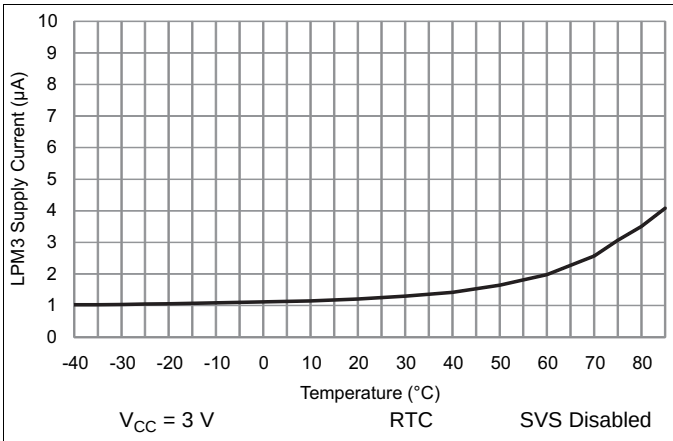


**Figure 5-1. LPM3 Supply Current vs Temperature**

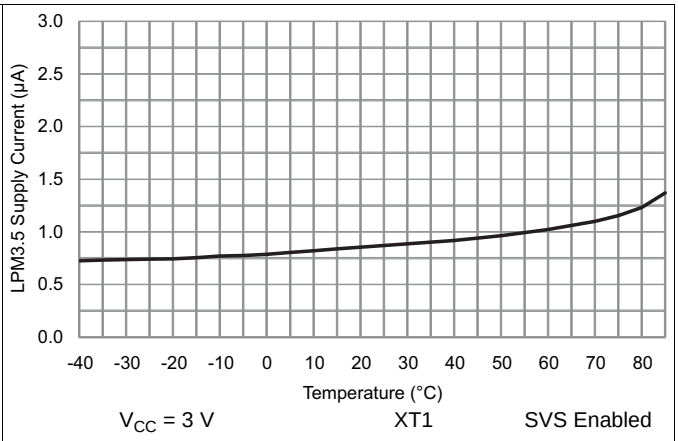


**Figure 5-2. LPM3.5 Supply Current vs Temperature**

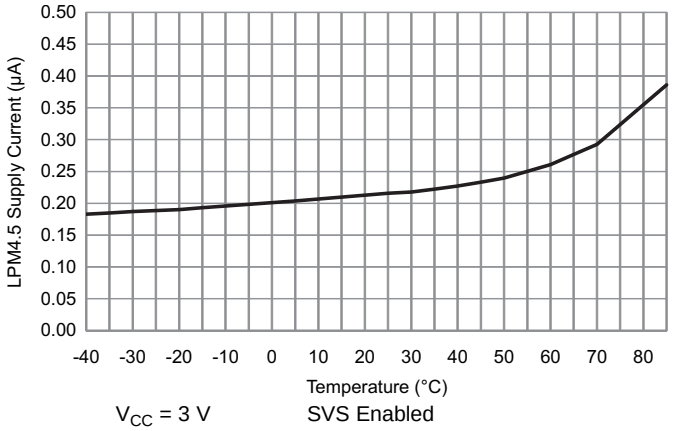


**Figure 5-3. LPM4.5 Supply Current vs Temperature**

**Table 5-1. Typical Characteristics – Current Consumption Per Module**

| MODULE | TEST CONDITIONS | REFERENCE CLOCK | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| Timer_A | | Module input clock | | 5 | | µA/MHz |
| eUSCI_A | UART mode | Module input clock | | 7 | | µA/MHz |
| eUSCI_A | SPI mode | Module input clock | | 5 | | µA/MHz |
| eUSCI_B | SPI mode | Module input clock | | 5 | | µA/MHz |
| eUSCI_B | $I^2C$ mode, 100 kbaud | Module input clock | | 5 | | µA/MHz |
| RTC | | 32 kHz | | 85 | | nA |
| CRC | From start to end of operation | MCLK | | 8.5 | | µA/MHz |

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## 5.10 Thermal Resistance Characteristics

| THERMAL METRIC(1) | | | VALUE(2) | UNIT |
|---|---|---|---|---|
| $R\theta_{JA}$ | Junction-to-ambient thermal resistance, still air | VQFN 24 pin (RGE) | 32.6 | °C/W |
| | | DSBGA 24 pin (YQW) | 63.7 | |
| $R\theta_{JC}$ | Junction-to-case (top) thermal resistance | VQFN 24 pin (RGE) | 32.4 | °C/W |
| | | DSBGA 24 pin (YQW) | 0.3 | |
| $R\theta_{JB}$ | Junction-to-board thermal resistance | VQFN 24 pin (RGE) | 10.1 | °C/W |
| | | DSBGA 24 pin (YQW) | 9.2 | |

(1) For more information about traditional and new thermal metrics, see *Semiconductor and IC Package Thermal Metrics*.
(2) These values are based on a JEDEC-defined 2S2P system (with the exception of the Theta JC ($R\theta_{JC}$) value, which is based on a JEDEC-defined 1S0P system) and will change based on environment and application. For more information, see these EIA/JEDEC standards:
- JESD51-2, *Integrated Circuits Thermal Test Method Environmental Conditions - Natural Convection (Still Air)*
- JESD51-3, *Low Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*
- JESD51-7, *High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*
- JESD51-9, *Test Boards for Area Array Surface Mount Package Thermal Measurements*


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## 5.11 Timing and Switching Characteristics

### 5.11.1 Power Supply Sequencing

Table 5-2 lists the characteristics of the SVS and BOR.

**Table 5-2. PMM, SVS and BOR**

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 5-4)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{BOR, safe}$ | Safe BOR power-down level(1) | | 0.1 | | | V |
| $t_{BOR, safe}$ | Safe BOR reset delay(2) | | 10 | | | ms |
| $I_{SVSH,AM}$ | $SVS_H$ current consumption, active mode | $V_{CC}$ = 3.6 V | | | 1.5 | µA |
| $I_{SVSH,LPM}$ | $SVS_H$ current consumption, low-power modes | $V_{CC}$ = 3.6 V | | 240 | | nA |
| $V_{SVSH-}$ | $SVS_H$ power-down level(3) | | 1.71 | 1.80 | 1.86 | V |
| $V_{SVSH+}$ | $SVS_H$ power-up level(3) | | 1.74 | 1.89 | 1.99 | V |
| $V_{SVSH_hys}$ | $SVS_H$ hysteresis | | | 80 | | mV |
| $t_{PD,SVSH, AM}$ | $SVS_H$ propagation delay, active mode | | | | 10 | µs |
| $t_{PD,SVSH, LPM}$ | $SVS_H$ propagation delay, low-power modes | | | | 100 | µs |
| $V_{REF, 1.2V}$ | 1.2-V REF voltage(4) | | 1.158 | 1.20 | 1.242 | V |

(1) A safe BOR can be correctly generated only if DVCC drops below this voltage before it rises.
(2) When an BOR occurs, a safe BOR can be correctly generated only if DVCC is kept low longer than this period before it reaches $V_{SVSH+}$.
(3) For additional information, see the Dynamic Voltage Scaling Power Solution for MSP430 Devices With Single-Channel LDO Reference Design.
(4) This is a characterized result with external 1-mA load to ground from –40°C to 85°C.

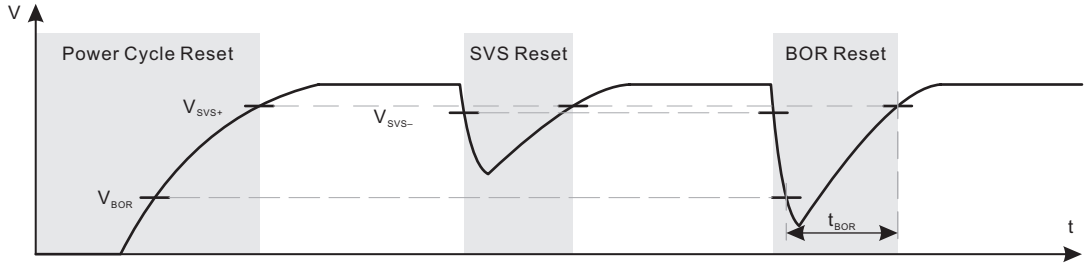


**Figure 5-4. Power Cycle, SVS, and BOR Reset Conditions**

### 5.11.2 Reset Timing

Table 5-3 lists the wake-up times.

**Table 5-3. Wake-up Times From Low-Power Modes and Reset**

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | $V_{CC}$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $t_{WAKE-UP\ FRAM}$ | Additional wake-up time to activate the FRAM in AM if previously disabled by the FRAM controller or from a LPM if immediate activation is selected for wakeup (1) | | 3 V | | 10 | | µs |
| $t_{WAKE-UP\ LPM0}$ | Wake-up time from LPM0 to active mode (1) | | 3 V | | | 200 + 2.5 / $f_{DCO}$ | ns |
| $t_{WAKE-UP\ LPM3}$ | Wake-up time from LPM3 to active mode (2) | | 3 V | | 10 | | µs |
| $t_{WAKE-UP\ LPM4}$ | Wake-up time from LPM4 to active mode | | 3 V | | 10 | | µs |
| $t_{WAKE-UP\ LPM3.5}$ | Wake-up time from LPM3.5 to active mode (2) | | 3 V | | 350 | | µs |
| $t_{WAKE-UP\ LPM4.5}$ | Wake-up time from LPM4.5 to active mode (2) | SVSHE = 1 | 3 V | | 350 | | µs |
| | | SVSHE = 0 | | | 1 | | ms |
| $t_{WAKE-UP-RESET}$ | Wake-up time from $\overline{RST}$ or BOR event to active mode (2) | | 3 V | | 1 | | ms |
| $t_{RESET}$ | Pulse duration required at $\overline{RST}$/NMI pin to accept a reset | | 3 V | 2 | | | µs |

(1) The wake-up time is measured from the edge of an external wake-up signal (for example, port interrupt or wake-up event) to the first externally observable MCLK clock edge.
(2) The wake-up time is measured from the edge of an external wake-up signal (for example, port interrupt or wake-up event) until the first instruction of the user program is executed.


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### 5.11.3 Clock Specifications

Table 5-4 lists the characteristics of XT1.

**Table 5-4. XT1 Crystal Oscillator (Low Frequency)**

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)(1)

| PARAMETER | | TEST CONDITIONS | $V_{CC}$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $f_{XT1,\ LF}$ | XT1 oscillator crystal, low frequency | LFXTBYPASS = 0 | | | 32768 | | Hz |
| $DC_{XT1,\ LF}$ | XT1 oscillator LF duty cycle | Measured at MCLK, $f_{LFXT}$ = 32768 Hz | | 30% | | 70% | |
| $f_{XT1,SW}$ | XT1 oscillator logic-level square-wave input frequency | LFXTBYPASS = 1 (2)(3) | | | 32.768 | | kHz |
| $DC_{XT1,\ SW}$ | LFXT oscillator logic-level square-wave input duty cycle | LFXTBYPASS = 1 | | 40% | | 60% | |
| $OA_{LFXT}$ | Oscillation allowance for LF crystals (4) | LFXTBYPASS = 0, LFXTDRIVE = {3}, $f_{LFXT}$ = 32768 Hz, $C_{L,eff}$ = 12.5 pF | | | 200 | | kΩ |
| $C_{L,eff}$ | Integrated effective load capacitance(5) | See (6) | | | 1 | | pF |
| $t_{START,LFXT}$ | Start-up time (7) | $f_{OSC}$ = 32768 Hz, LFXTBYPASS = 0, LFXTDRIVE = {3}, $T_A$ = 25°C, $C_{L,eff}$ = 12.5 pF | | | 1000 | | ms |
| $f_{Fault,LFXT}$ | Oscillator fault frequency (8) | XTS = 0(9) | | 0 | | 3500 | Hz |

(1) To improve EMI on the LFXT oscillator, observe the following guidelines:
- Keep the trace between the device and the crystal as short as possible.
- Design a good ground plane around the oscillator pins.
- Prevent crosstalk from other clock or data lines into oscillator pins XIN and XOUT.
- Avoid running PCB traces underneath or adjacent to the XIN and XOUT pins.
- Use assembly materials and processes that avoid any parasitic load on the oscillator XIN and XOUT pins.
- If conformal coating is used, make sure that it does not induce capacitive or resistive leakage between the oscillator pins.

(2) When LFXTBYPASS is set, LFXT circuits are automatically powered down. Input signal is a digital square wave with parametrics defined in the Schmitt-trigger inputs section of this data sheet. Duty cycle requirements are defined by $DC_{LFXT,\ SW}$.

(3) Maximum frequency of operation of the entire device cannot be exceeded.

(4) Oscillation allowance is based on a safety factor of 5 for recommended crystals. The oscillation allowance is a function of the LFXTDRIVE settings and the effective load. In general, comparable oscillator allowance can be achieved based on the following guidelines, but should be evaluated based on the actual crystal selected for the application:
- For LFXTDRIVE = {0}, $C_{L,eff}$ = 3.7 pF
- For LFXTDRIVE = {1}, 6 pF ≤ $C_{L,eff}$ ≤ 9 pF
- For LFXTDRIVE = {2}, 6 pF ≤ $C_{L,eff}$ ≤ 10 pF
- For LFXTDRIVE = {3}, 6 pF ≤ $C_{L,eff}$ ≤ 12 pF

(5) Includes parasitic bond and package capacitance (approximately 2 pF per pin).

(6) Requires external capacitors at both terminals to meet the effective load capacitance specified by crystal manufacturers. Recommended effective load capacitance values supported are 3.7 pF, 6 pF, 9 pF, and 12.5 pF. Maximum shunt capacitance of 1.6 pF. The PCB adds additional capacitance, so it must also be considered in the overall capacitance. Verify that the recommended effective load capacitance of the selected crystal is met.

(7) Includes start-up counter of 1024 clock cycles.

(8) Frequencies above the MAX specification do not set the fault flag. Frequencies between the MIN and MAX specifications might set the flag. A static condition or stuck at fault condition sets the flag.

(9) Measured with logic-level input frequency but also applies to operation with crystals.

Table 5-5 lists the characteristics of the FLL.

**Table 5-5. DCO FLL, Frequency**

over recommended operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | $V_{CC}$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $f_{DCO,\ FLL}$ | FLL lock frequency, 16 MHz, 25°C | Measured at MCLK, Internal trimmed REFO as reference | 3 V | –1.0% | | 1.0% | |
| | FLL lock frequency, 16 MHz, –40°C to 85°C | | 3 V | –2.0% | | 2.0% | |
| | FLL lock frequency, 16 MHz, –40°C to 85°C | Measured at MCLK, XT1 crystal as reference | 3 V | –0.5% | | 0.5% | |

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**Table 5-5. DCO FLL, Frequency (continued)**

over recommended operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | $V_{CC}$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $f_{DUTY}$ | Duty cycle | Measured at MCLK, XT1 crystal as reference | 3 V | 40% | 50% | 60% | |
| $Jitter_{cc}$ | Cycle-to-cycle jitter, 16 MHz | | 3 V | | 0.25% | | |
| $Jitter_{long}$ | Long term jitter, 16 MHz | | 3 V | | 0.022% | | |
| $t_{FLL, lock}$ | FLL lock time | | 3 V | | 280 | | ms |
| $t_{start-up}$ | DCO start-up time, 2 MHz | Measured at MCLK | 3 V | | 16 | | µs |

Table 5-6 lists the characteristics of the DCO.

**Table 5-6. DCO Frequency**

over recommended operating free-air temperature (unless otherwise noted) (also see Figure 5-5)

| PARAMETER | | TEST CONDITIONS | $V_{CC}$ | TYP | UNIT |
|---|---|---|---|---|---|
| $f_{DCO, 16MHz}$ | DCO frequency, 16 MHz | DCORSEL = 101b, DISMOD = 1b, DCOFTRIMEN = 1b, DCOFTRIM = 000b, DCO = 0 | 3 V | 7.46 | MHz |
| | | DCORSEL = 101b, DISMOD = 1b, DCOFTRIMEN = 1b, DCOFTRIM = 000b, DCO = 511 | | 12.26 | |
| | | DCORSEL = 101b, DISMOD = 1b, DCOFTRIMEN = 1b, DCOFTRIM = 111b, DCO = 0 | | 17.93 | |
| | | DCORSEL = 101b, DISMOD = 1b, DCOFTRIMEN = 1b, DCOFTRIM = 111b, DCO = 511 | | 29.1 | |
| $f_{DCO, 12MHz}$ | DCO frequency, 12 MHz | DCORSEL = 100b, DISMOD = 1b, DCOFTRIMEN = 1b, DCOFTRIM = 000b, DCO = 0 | 3 V | 5.75 | MHz |
| | | DCORSEL = 100b, DISMOD = 1b, DCOFTRIMEN = 1b, DCOFTRIM = 000b, DCO = 511 | | 9.5 | |
| | | DCORSEL = 100b, DISMOD = 1b, DCOFTRIMEN = 1b, DCOFTRIM = 111b, DCO = 0 | | 13.85 | |
| | | DCORSEL = 100b, DISMOD = 1b, DCOFTRIMEN = 1b, DCOFTRIM = 111b, DCO = 511 | | 22.5 | |
| $f_{DCO, 8MHz}$ | DCO frequency, 8 MHz | DCORSEL = 011b, DISMOD = 1b, DCOFTRIMEN = 1b, DCOFTRIM = 000b, DCO = 0 | 3 V | 3.91 | MHz |
| | | DCORSEL = 011b, DISMOD = 1b, DCOFTRIMEN = 1b, DCOFTRIM = 000b, DCO = 511 | | 6.49 | |
| | | DCORSEL = 011b, DISMOD = 1b, DCOFTRIMEN = 1b, DCOFTRIM = 111b, DCO = 0 | | 9.5 | |
| | | DCORSEL = 011b, DISMOD = 1b, DCOFTRIMEN = 1b, DCOFTRIM = 111b, DCO = 511 | | 15.6 | |
| $f_{DCO, 4MHz}$ | DCO frequency, 4 MHz | DCORSEL = 010b, DISMOD = 1b, DCOFTRIMEN = 1b, DCOFTRIM = 000b, DCO = 0 | 3 V | 2.026 | MHz |
| | | DCORSEL = 010b, DISMOD = 1b, DCOFTRIMEN = 1b, DCOFTRIM = 000b, DCO = 511 | | 3.407 | |
| | | DCORSEL = 010b, DISMOD = 1b, DCOFTRIMEN = 1b, DCOFTRIM = 111b, DCO = 0 | | 4.95 | |
| | | DCORSEL = 010b, DISMOD = 1b, DCOFTRIMEN = 1b, DCOFTRIM = 111b, DCO = 511 | | 8.26 | |
| $f_{DCO, 2MHz}$ | DCO frequency, 2 MHz | DCORSEL = 001b, DISMOD = 1b, DCOFTRIMEN = 1b, DCOFTRIM = 000b, DCO = 0 | 3 V | 1.0225 | MHz |
| | | DCORSEL = 001b, DISMOD = 1b, DCOFTRIMEN = 1b, DCOFTRIM = 000b, DCO = 511 | | 1.729 | |
| | | DCORSEL = 001b, DISMOD = 1b, DCOFTRIMEN = 1b, DCOFTRIM = 111b, DCO = 0 | | 2.525 | |
| | | DCORSEL = 001b, DISMOD = 1b, DCOFTRIMEN = 1b, DCOFTRIM = 111b, DCO = 511 | | 4.25 | |


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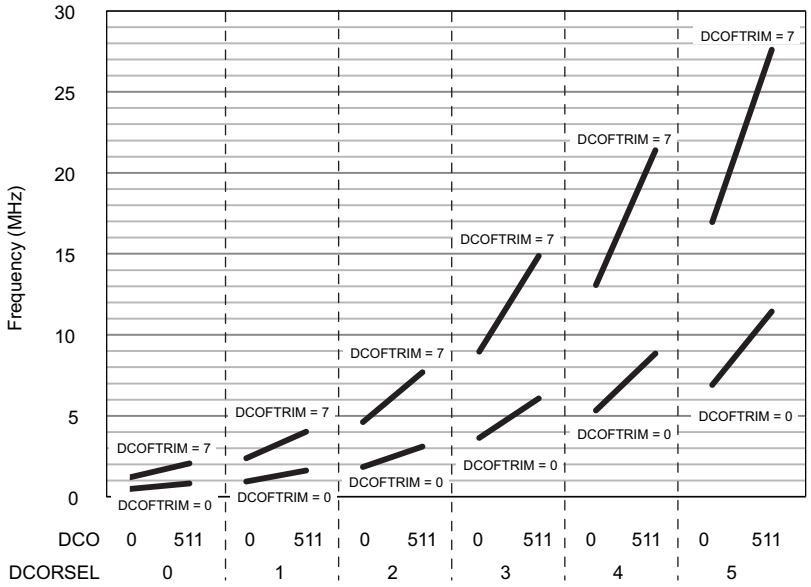
**Table 5-6. DCO Frequency (continued)**

over recommended operating free-air temperature (unless otherwise noted) (also see Figure 5-5)

| PARAMETER | | TEST CONDITIONS | $V_{CC}$ | TYP | UNIT |
|---|---|---|---|---|---|
| $f_{DCO, 1MHz}$ | DCO frequency, 1 MHz | DCORSEL = 000b, DISMOD = 1b, DCOFTRIMEN = 1b, DCOFTRIM = 000b, DCO = 0 | 3 V | 0.5319 | MHz |
| | | DCORSEL = 000b, DISMOD = 1b, DCOFTRIMEN = 1b, DCOFTRIM = 000b, DCO = 511 | | 0.9029 | |
| | | DCORSEL = 000b, DISMOD = 1b, DCOFTRIMEN = 1b, DCOFTRIM = 111b, DCO = 0 | | 1.307 | |
| | | DCORSEL = 000b, DISMOD = 1b, DCOFTRIMEN = 1b, DCOFTRIM = 111b, DCO = 511 | | 2.21 | |




$V_{CC}$ = 3 V $T_A$ = –40°C to 85°C

**Figure 5-5. Typical DCO Frequency**

Table 5-7 lists the characteristics of the REFO.

**Table 5-7. REFO**

over recommended operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | $V_{CC}$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $I_{REFO}$ | REFO oscillator current consumption | $T_A$ = 25°C | 3 V | | 15 | | µA |
| $f_{REFO}$ | REFO calibrated frequency | Measured at MCLK | 3 V | | 32768 | | Hz |
| | REFO absolute calibrated tolerance | –40°C to 85°C | 1.8 V to 3.6 V | –3.5% | | +3.5% | |
| $df_{REFO}/d_T$ | REFO frequency temperature drift | Measured at MCLK(1) | 3 V | | 0.01 | | %/°C |
| $df_{REFO}/d_{VCC}$ | REFO frequency supply voltage drift | Measured at MCLK at 25°C(2) | 1.8 V to 3.6 V | | 1 | | %/V |
| $f_{DC}$ | REFO duty cycle | Measured at MCLK | 1.8 V to 3.6 V | 40% | 50% | 60% | |
| $t_{START}$ | REFO start-up time | 40% to 60% duty cycle | | | 50 | | µs |

(1) Calculated using the box method: (MAX(–40°C to 85°C) – MIN(–40°C to 85°C)) / MIN(–40°C to 85°C) / (85°C – (–40°C))
(2) Calculated using the box method: (MAX(1.8 V to 3.6 V) – MIN(1.8 V to 3.6 V)) / MIN(1.8 V to 3.6 V) / (3.6 V – 1.8 V)

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Table 5-8 lists the characteristics of the VLO.

**NOTE**

The VLO clock frequency is reduced by 15% (typical) when the device switches from active mode to LPM3 or LPM4, because the reference changes. This lower frequency is not a violation of the VLO specifications (see Table 5-8).

**Table 5-8. Internal Very-Low-Power Low-Frequency Oscillator (VLO)**

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | $V_{CC}$ | TYP | UNIT |
|---|---|---|---|---|---|
| $f_{VLO}$ | VLO frequency | Measured at MCLK | 3 V | 10 | kHz |
| $df_{VLO}/d_T$ | VLO frequency temperature drift | Measured at MCLK(1) | 3 V | 0.5 | %/°C |
| $df_{VLO}/dV_{CC}$ | VLO frequency supply voltage drift | Measured at MCLK(2) | 2 V to 3.6 V | 4 | %/V |
| $f_{VLO,DC}$ | Duty cycle | Measured at MCLK | 3 V | 50% | |

(1) Calculated using the box method: (MAX(–40°C to 85°C) – MIN(–40°C to 85°C)) / MIN(–40°C to 85°C) / (85°C – (–40°C))
(2) Calculated using the box method: (MAX(1.8 V to 3.6 V) – MIN(1.8 V to 3.6 V)) / MIN(1.8 V to 3.6 V) / (3.6 V – 1.8 V)

Table 5-9 lists the characteristics of the MODOSC.

**Table 5-9. Module Oscillator (MODOSC)**

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | $V_{CC}$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $f_{MODOSC}$ | MODOSC frequency | 3 V | 3.8 | 4.8 | 5.8 | MHz |
| $f_{MODOSC}/dT$ | MODOSC frequency temperature drift | 3 V | | 0.102 | | %/℃ |
| $f_{MODOSC}/dV_{CC}$ | MODOSC frequency supply voltage drift | 1.8 V to 3.6 V | | 1.02 | | %/V |
| $f_{MODOSC,DC}$ | Duty cycle | 3 V | 40% | 50% | 60% | |


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### 5.11.4 Digital I/Os

Table 5-10 lists the characteristics of the digital inputs.

**Table 5-10. Digital Inputs**

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | $V_{CC}$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $V_{IT+}$ | Positive-going input threshold voltage | | 2 V | 0.90 | | 1.50 | V |
| | | | 3 V | 1.35 | | 2.25 | |
| $V_{IT-}$ | Negative-going input threshold voltage | | 2 V | 0.50 | | 1.10 | V |
| | | | 3 V | 0.75 | | 1.65 | |
| $V_{hys}$ | Input voltage hysteresis ($V_{IT+} - V_{IT-}$) | | 2 V | 0.3 | | 0.8 | V |
| | | | 3 V | 0.4 | | 1.2 | |
| $R_{Pull}$ | Pullup or pulldown resistor | For pullup: $V_{IN} = V_{SS}$<br>For pulldown: $V_{IN} = V_{CC}$ | | 20 | 35 | 50 | kΩ |
| $C_{I,dig}$ | Input capacitance, digital only port pins | $V_{IN} = V_{SS}$ or $V_{CC}$ | | | 3 | | pF |
| $C_{I,ana}$ | Input capacitance, port pins with shared analog functions | $V_{IN} = V_{SS}$ or $V_{CC}$ | | | 5 | | pF |
| $I_{lkg(Px.y)}$ | High-impedance leakage current | See (1) (2) | 2 V, 3 V | –20 | | 20 | nA |
| $t_{(int)}$ | External interrupt timing (external trigger pulse duration to set interrupt flag)(3) | Ports with interrupt capability (see block diagram and terminal function descriptions) | 2 V, 3 V | 50 | | | ns |

(1) The leakage current is measured with $V_{SS}$ or $V_{CC}$ applied to the corresponding pins, unless otherwise noted.
(2) The leakage of the digital port pins is measured individually. The port pin is selected for input and the pullup or pulldown resistor is disabled.
(3) An external signal sets the interrupt flag every time the minimum interrupt pulse duration $t_{(int)}$ is met. It may be set by trigger signals shorter than $t_{(int)}$.

Table 5-11 lists the characteristics of the digital outputs.

**Table 5-11. Digital Outputs**

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (also see Figure 5-6, Figure 5-7, Figure 5-8, and Figure 5-9)

| PARAMETER | | TEST CONDITIONS | $V_{CC}$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $V_{OH}$ | High-level output voltage | $I_{(OHmax)}$ = –3 mA(1) | 2 V | 1.4 | | 2.0 | V |
| | | $I_{(OHmax)}$ = –5 mA(1) | 3 V | 2.4 | | 3.0 | |
| $V_{OL}$ | Low-level output voltage | $I_{(OLmax)}$ = 3 mA(1) | 2 V | 0.0 | | 0.60 | V |
| | | $I_{(OHmax)}$ = 5 mA(1) | 3 V | 0.0 | | 0.60 | |
| $f_{Port_CLK}$ | Clock output frequency | $C_L$ = 20 pF(2) | 2 V | 16 | | | MHz |
| | | | 3 V | 16 | | | |
| $t_{rise,dig}$ | Port output rise time, digital only port pins | $C_L$ = 20 pF | 2 V | | 10 | | ns |
| | | | 3 V | | 7 | | |
| $t_{fall,dig}$ | Port output fall time, digital only port pins | $C_L$ = 20 pF | 2 V | | 10 | | ns |
| | | | 3 V | | 5 | | |

(1) The maximum total current, $I_{(OHmax)}$ and $I_{(OLmax)}$, for all outputs combined should not exceed ±48 mA to hold the maximum voltage drop specified.
(2) The port can output frequencies at least up to the specified limit and might support higher frequencies.

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### 5.11.4.1 Typical Characteristics – Outputs at 3 V and 2 V

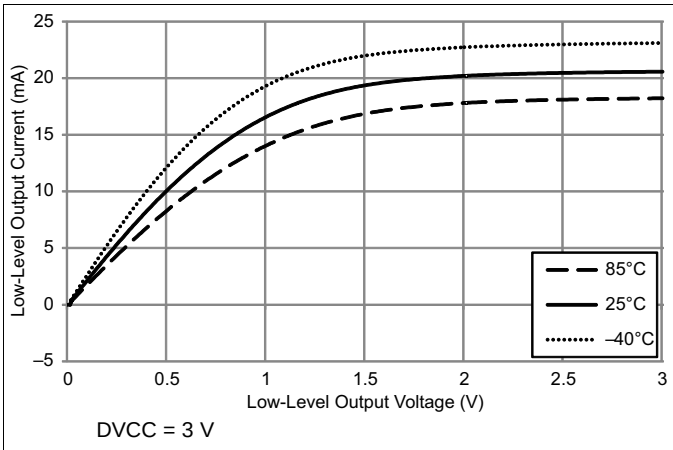


**Figure 5-6. Typical Low-Level Output Current vs Low-Level Output Voltage**

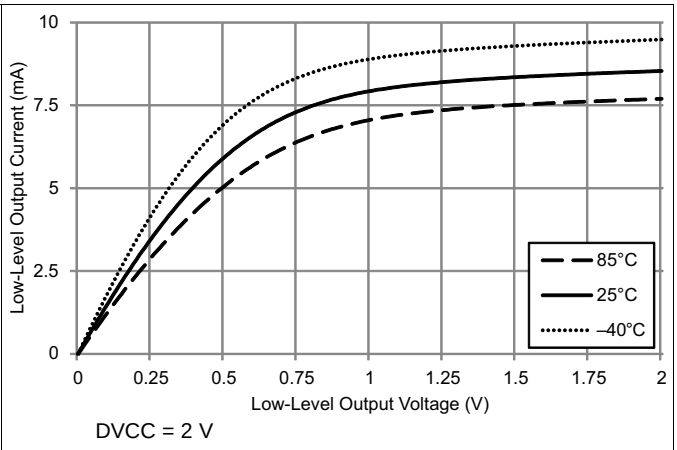


**Figure 5-7. Typical Low-Level Output Current vs Low-Level Output Voltage**

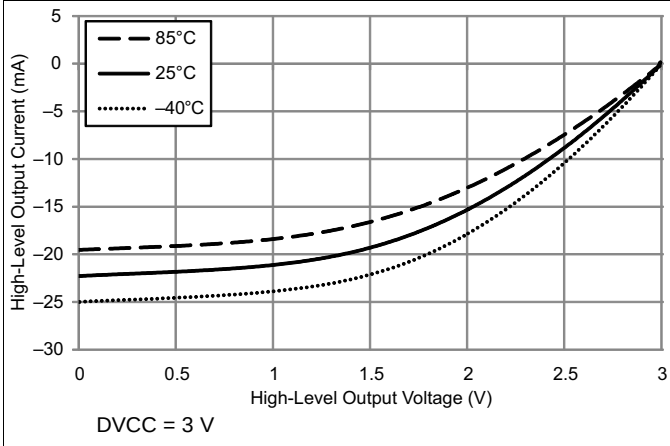


**Figure 5-8. Typical High-Level Output Current vs High-Level Output Voltage**

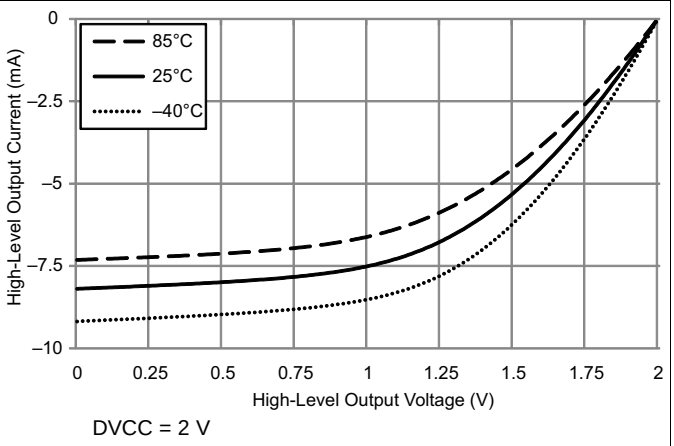


**Figure 5-9. Typical High-Level Output Current vs High-Level Output Voltage**


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### 5.11.5 VREF+ Built-in Reference

Table 5-12 lists the characteristics of VREF+.

**Table 5-12. VREF+**

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | $V_{CC}$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $V_{REF+}$ | Positive built-in reference voltage | EXTREFEN = 1 with 1-mA load current | 2 V, 3 V | 1.15 | 1.19 | 1.23 | V |
| $TC_{REF+}$ | Temperature coefficient of built-in reference voltage | | | | 30 | | µV/°C |

### 5.11.6 Timer_A

Table 5-13 lists the characteristics of Timer_A.

**Table 5-13. Timer_A**

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 5-10 and Figure 5-11)

| PARAMETER | | TEST CONDITIONS | $V_{CC}$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $f_{TA}$ | Timer_A input clock frequency | Internal: SMCLK or ACLK,<br>External: TACLK,<br>duty cycle = 50% ±10% | 2 V, 3 V | | | 16 | MHz |
| $t_{TA,cap}$ | Timer_A capture timing | All capture inputs, minimum pulse duration required for capture | 2 V, 3 V | 20 | | | ns |

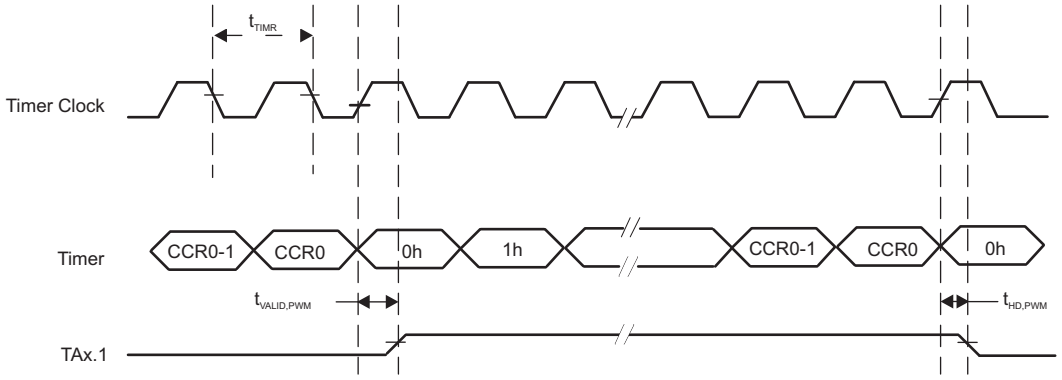


**Figure 5-10. Timer PWM Mode**

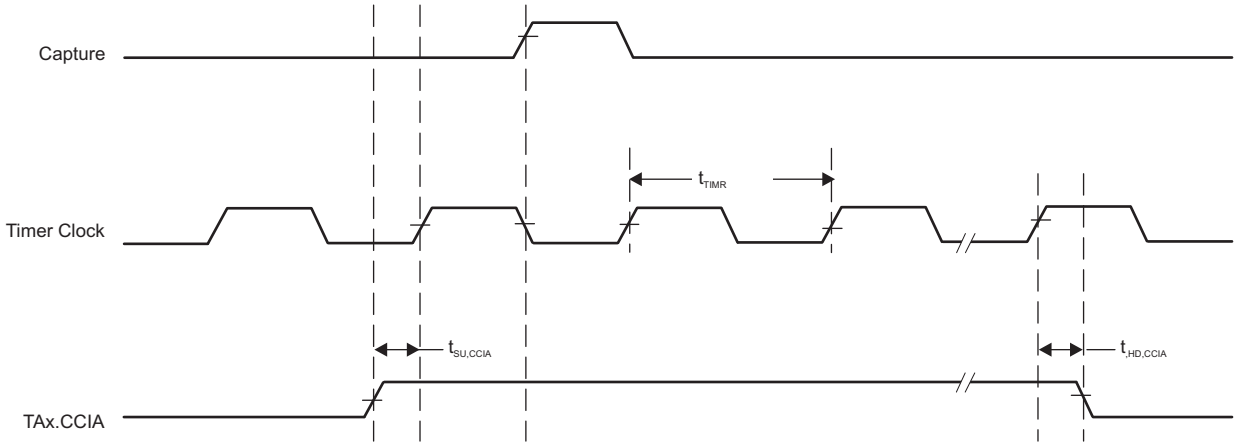


**Figure 5-11. Timer Capture Mode**

### 5.11.7 eUSCI

Table 5-14 lists the supported frequencies of the eUSCI in UART mode.

**Table 5-14. eUSCI (UART Mode) Clock Frequency**

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | $V_{CC}$ | MIN | MAX | UNIT |
|---|---|---|---|---|---|---|
| $f_{eUSCI}$ | eUSCI input clock frequency | Internal: SMCLK or MODCLK, External: UCLK, duty cycle = 50% ±10% | 2 V, 3 V | | 16 | MHz |
| $f_{BITCLK}$ | BITCLK clock frequency (equals baud rate in Mbaud) | | 2 V, 3 V | | 5 | MHz |

Table 5-15 lists the characteristics of the eUSCI in UART mode.

**Table 5-15. eUSCI (UART Mode)**

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | $V_{CC}$ | TYP | UNIT |
|---|---|---|---|---|---|
| $t_t$ | UART receive deglitch time (1) | UCGLITx = 0 | 2 V, 3 V | 12 | ns |
| | | UCGLITx = 1 | | 40 | |
| | | UCGLITx = 2 | | 68 | |
| | | UCGLITx = 3 | | 110 | |

(1) Pulses on the UART receive input (UCxRX) shorter than the UART receive deglitch time are suppressed. To ensure that pulses are correctly recognized, their duration should exceed the maximum specification of the deglitch time.

Table 5-16 lists the supported frequencies of the eUSCI in SPI master mode.

**Table 5-16. eUSCI (SPI Master Mode) Clock Frequency**

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $f_{eUSCI}$ | eUSCI input clock frequency | Internal: SMCLK or MODCLK, duty cycle = 50% ±10% | | 8 | MHz |

Table 5-17 lists the characteristics of the eUSCI in SPI master mode.

**Table 5-17. eUSCI (SPI Master Mode)**

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (1)

| PARAMETER | | TEST CONDITIONS | $V_{CC}$ | MIN | MAX | UNIT |
|---|---|---|---|---|---|---|
| $t_{STE,LEAD}$ | STE lead time, STE active to clock | UCSTEM = 0, UCMODEx = 01 or 10 | | 1 | | UCxCLK cycles |
| | | UCSTEM = 1, UCMODEx = 01 or 10 | | | | |
| $t_{STE,LAG}$ | STE lag time, last clock to STE inactive | UCSTEM = 0, UCMODEx = 01 or 10 | | 1 | | UCxCLK cycles |
| | | UCSTEM = 1, UCMODEx = 01 or 10 | | | | |
| $t_{SU,MI}$ | SOMI input data setup time | | 2 V | 45 | | ns |
| | | | 3 V | 35 | | |
| $t_{HD,MI}$ | SOMI input data hold time | | 2 V | 0 | | ns |
| | | | 3 V | 0 | | |
| $t_{VALID,MO}$ | SIMO output data valid time (2) | UCLK edge to SIMO valid, $C_L$ = 20 pF | 2 V | | 20 | ns |
| | | | 3 V | | 20 | |
| $t_{HD,MO}$ | SIMO output data hold time (3) | $C_L$ = 20 pF | 2 V | 0 | | ns |
| | | | 3 V | 0 | | |

(1) $f_{UCxCLK} = 1 / 2t_{LO/HI}$ with $t_{LO/HI} = \max(t_{VALID,MO(eUSCI)} + t_{SU,SI(Slave)}, t_{SU,MI(eUSCI)} + t_{VALID,SO(Slave)})$
For the slave parameters $t_{SU,SI(Slave)}$ and $t_{VALID,SO(Slave)}$, see the SPI parameters of the attached slave.
(2) Specifies the time to drive the next valid data to the SIMO output after the output changing UCLK clock edge. See the timing diagrams in Figure 5-12 and Figure 5-13.
(3) Specifies how long data on the SIMO output is valid after the output changing UCLK clock edge. Negative values indicate that the data on the SIMO output can become invalid before the output changing clock edge observed on UCLK. See the timing diagrams in Figure 5-12 and Figure 5-13.


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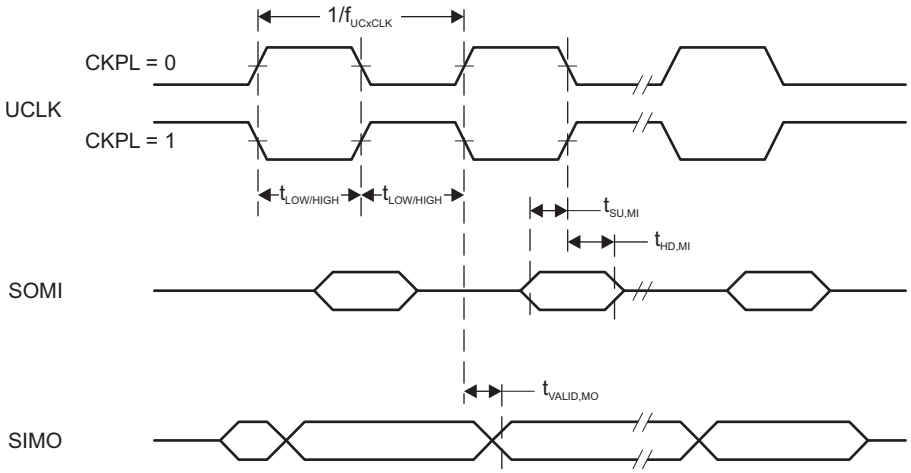


**Figure 5-12. SPI Master Mode, CKPH = 0**

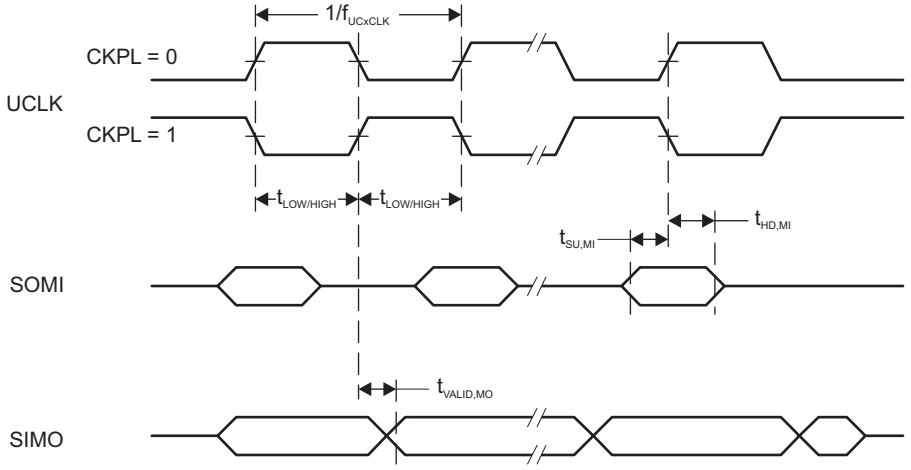


**Figure 5-13. SPI Master Mode, CKPH = 1**

Table 5-18 lists the characteristics of the eUSCI in SPI slave mode.

**Table 5-18. eUSCI (SPI Slave Mode)**

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)(1)

| PARAMETER | | TEST CONDITIONS | $V_{CC}$ | MIN | MAX | UNIT |
|---|---|---|---|---|---|---|
| $t_{STE,LEAD}$ | STE lead time, STE active to clock | | 2 V | 55 | | ns |
| | | | 3 V | 45 | | |
| $t_{STE,LAG}$ | STE lag time, Last clock to STE inactive | | 2 V | 20 | | ns |
| | | | 3 V | 20 | | |
| $t_{STE,ACC}$ | STE access time, STE active to SOMI data out | | 2 V | | 65 | ns |
| | | | 3 V | | 40 | |
| $t_{STE,DIS}$ | STE disable time, STE inactive to SOMI high impedance | | 2 V | | 40 | ns |
| | | | 3 V | | 35 | |
| $t_{SU,SI}$ | SIMO input data setup time | | 2 V | 6 | | ns |
| | | | 3 V | 4 | | |
| $t_{HD,SI}$ | SIMO input data hold time | | 2 V | 12 | | ns |
| | | | 3 V | 12 | | |
| $t_{VALID,SO}$ | SOMI output data valid time(2) | UCLK edge to SOMI valid, $C_L$ = 20 pF | 2 V | | 65 | ns |
| | | | 3 V | | 40 | |
| $t_{HD,SO}$ | SOMI output data hold time (3) | $C_L$ = 20 pF | 2 V | 5 | | ns |
| | | | 3 V | 5 | | |

(1) $f_{UCxCLK} = 1/2t_{LO/HI}$ with $t_{LO/HI} \geq \max(t_{VALID,MO(Master)} + t_{SU,SI(eUSCI)}, t_{SU,MI(Master)} + t_{VALID,SO(eUSCI)})$
For the master parameters $t_{SU,MI(Master)}$ and $t_{VALID,MO(Master)}$, see the SPI parameters of the attached master.
(2) Specifies the time to drive the next valid data to the SOMI output after the output changing UCLK clock edge. See the timing diagrams in Figure 5-14 and Figure 5-15.
(3) Specifies how long data on the SOMI output is valid after the output changing UCLK clock edge. See the timing diagrams in Figure 5-14 and Figure 5-15.


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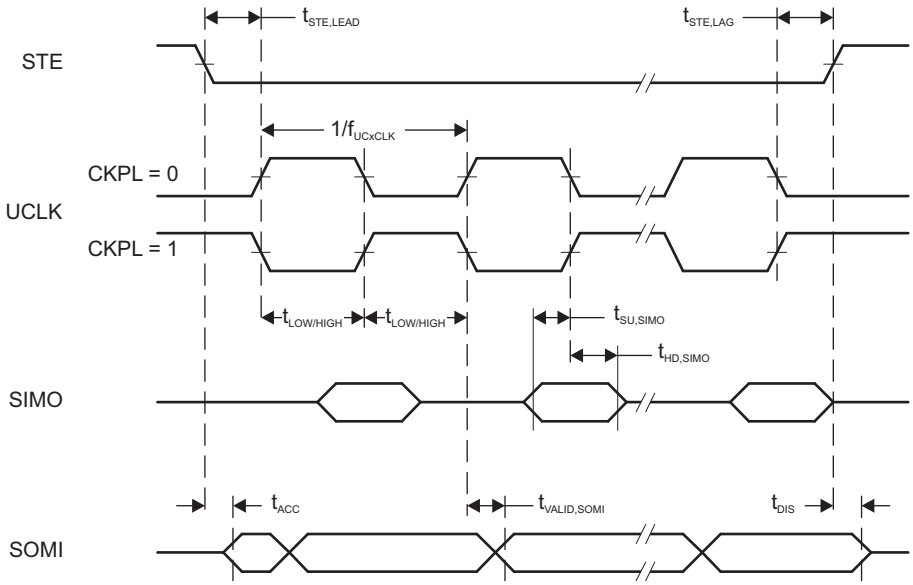


**Figure 5-14. SPI Slave Mode, CKPH = 0**

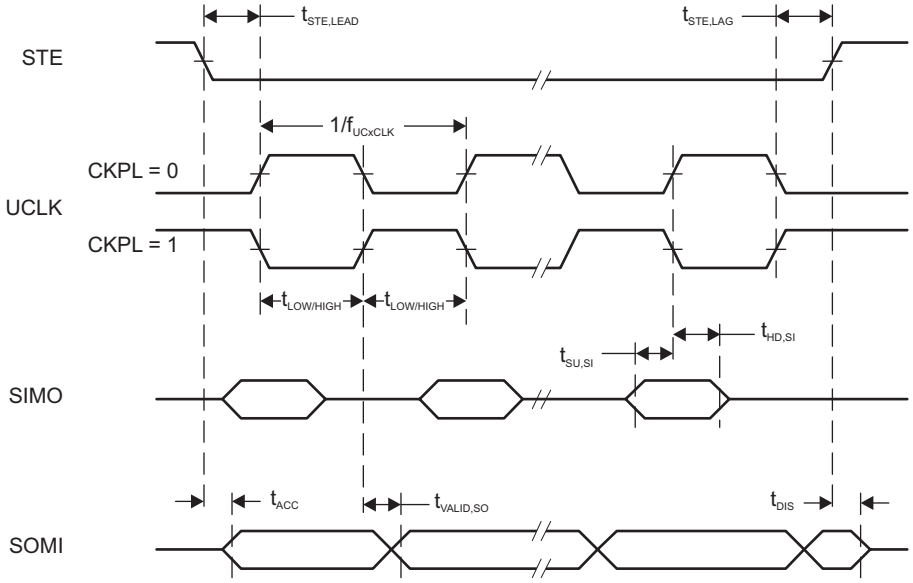


**Figure 5-15. SPI Slave Mode, CKPH = 1**

Table 5-19 lists the characteristics of the eUSCI in I²C mode.

**Table 5-19. eUSCI (I²C Mode)**

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 5-16)

| PARAMETER | | TEST CONDITIONS | $V_{CC}$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $f_{eUSCI}$ | eUSCI input clock frequency | Internal: SMCLK or MODCLK, External: UCLK Duty cycle = 50% ±10% | | | | 16 | MHz |
| $f_{SCL}$ | SCL clock frequency | | 2 V, 3 V | 0 | | 400 | kHz |
| $t_{HD,STA}$ | Hold time (repeated) START | $f_{SCL}$ = 100 kHz | 2 V, 3 V | 4.0 | | | µs |
| | | $f_{SCL}$ > 100 kHz | | 0.6 | | | |
| $t_{SU,STA}$ | Setup time for a repeated START | $f_{SCL}$ = 100 kHz | 2 V, 3 V | 4.7 | | | µs |
| | | $f_{SCL}$ > 100 kHz | | 0.6 | | | |
| $t_{HD,DAT}$ | Data hold time | | 2 V, 3 V | 0 | | | ns |
| $t_{SU,DAT}$ | Data setup time | | 2 V, 3 V | 250 | | | ns |
| $t_{SU,STO}$ | Setup time for STOP | $f_{SCL}$ = 100 kHz | 2 V, 3 V | 4.0 | | | µs |
| | | $f_{SCL}$ > 100 kHz | | 0.6 | | | |
| $t_{SP}$ | Pulse duration of spikes suppressed by input filter | UCGLITx = 0 | 2 V, 3 V | 50 | | 600 | ns |
| | | UCGLITx = 1 | | 25 | | 300 | |
| | | UCGLITx = 2 | | 12.5 | | 150 | |
| | | UCGLITx = 3 | | 6.3 | | 75 | |
| $t_{TIMEOUT}$ | Clock low time-out | UCCLTOx = 1 | 2 V, 3 V | | 27 | | ms |
| | | UCCLTOx = 2 | | | 30 | | |
| | | UCCLTOx = 3 | | | 33 | | |

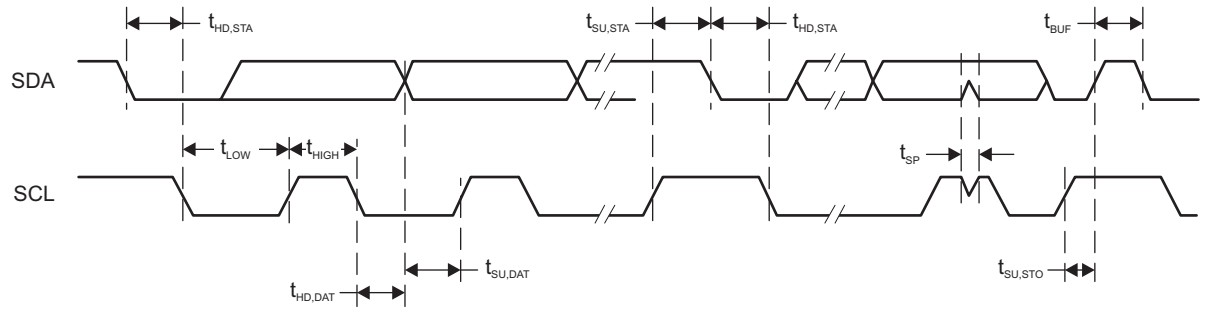


**Figure 5-16. I²C Mode Timing**


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### 5.11.8 ADC

Table 5-20 lists the input requirements of the ADC.

**Table 5-20. ADC, Power Supply and Input Range Conditions**

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | $V_{CC}$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $DV_{CC}$ | ADC supply voltage | | | 2.0 | | 3.6 | V |
| $V_{(Ax)}$ | Analog input voltage range | All ADC pins | | 0 | | $DV_{CC}$ | V |
| $I_{ADC}$ | Operating supply current into DVCC terminal, reference current not included, repeat-single-channel mode | $f_{ADCCLK}$ = 5 MHz, ADCON = 1, REFON = 0, SHT0 = 0, SHT1 = 0, ADCDIV = 0, ADCCONSEQx = 10b | 2 V | | 185 | | µA |
| | | | 3 V | | 207 | | |
| $C_I$ | Input capacitance | Only one terminal Ax can be selected at one time, from the pad to the ADC capacitor array, including wiring and pad | 2.2 V | | 1.6 | 2.0 | pF |
| $R_{I,MUX}$ | Input MUX ON resistance | $DV_{CC}$ = 2 V, 0 V ≤ $V_{Ax}$ ≤ $DV_{CC}$ | | | | 2 | kΩ |
| $R_{I,Misc}$ | Input miscellaneous resistance | | | | 34 | | kΩ |

Table 5-21 lists the timing parameters of the ADC.

**Table 5-21. ADC, 10-Bit Timing Parameters**

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | $V_{CC}$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $f_{ADCCLK}$ | | For specified performance of ADC linearity parameters | 2 V to 3.6 V | 0.45 | 5 | 5.5 | MHz |
| $f_{ADCOSC}$ | Internal ADC oscillator (MODOSC) | ADCDIV = 0, $f_{ADCCLK}$ = $f_{ADCOSC}$ | 2 V to 3.6 V | 4.5 | 5.0 | 5.5 | MHz |
| $t_{CONVERT}$ | Conversion time | REFON = 0, Internal oscillator, 10 ADCCLK cycles, 10-bit mode, $f_{ADCOSC}$ = 4.5 MHz to 5.5 MHz | 2 V to 3.6 V | 2.18 | | 2.67 | µs |
| | | External $f_{ADCCLK}$ from ACLK or SMCLK, ADCSSEL ≠ 0 | 2 V to 3.6 V | | 12 × 1 / $f_{ADCCLK}$ | | |
| $t_{ADCON}$ | Turnon settling time of the ADC | The error in a conversion started after $t_{ADCON}$ is less than ±0.5 LSB, Reference and input signal already settled | | | | 100 | ns |
| $t_{Sample}$ | Sampling time | $R_S$ = 1000 Ω, $R_I$ (1) = 36000 Ω, $C_I$ = 3.5 pF, Approximately 8 Tau (t) are required for an error of less than ±0.5 LSB (2) | 2 V | 1.5 | | | µs |
| | | | 3 V | 2.0 | | | |

(1) $R_I = R_{I,MUX} + R_{I,Misc}$
(2) $t_{Sample} = \ln(2^{n+1}) \times \tau$, where n = ADC resolution, $\tau = (R_I + R_S) \times C_I$

Table 5-22 lists the linearity parameters of the ADC.

**Table 5-22. ADC, 10-Bit Linearity Parameters**

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | $V_{CC}$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $E_I$ | Integral linearity error (10-bit mode) | $V_{eref+}$ as reference | 2.4 V to 3.6 V | –2 | | 2 | LSB |
| | Integral linearity error (8-bit mode) | | 2 V to 3.6 V | –2 | | 2 | |
| $E_D$ | Differential linearity error (10-bit mode) | $V_{eref+}$ as reference | 2.4 V to 3.6 V | –1 | | 1 | LSB |
| | Differential linearity error (8-bit mode) | | 2 V to 3.6 V | –1 | | 1 | |
| $E_O$ | Offset error (10-bit mode) | $V_{eref+}$ as reference | 2.4 V to 3.6 V | –6.5 | | 6.5 | mV |
| | Offset error (8-bit mode) | | 2 V to 3.6 V | –6.5 | | 6.5 | |
| $E_G$ | Gain error (10-bit mode) | $V_{eref+}$ as reference | 2.4 V to 3.6 V | –2.0 | | 2.0 | LSB |
| | | Internal 1.5-V reference | | –3.0% | | 3.0% | |
| | Gain error (8-bit mode) | $V_{eref+}$ as reference | 2 V to 3.6 V | –2.0 | | 2.0 | LSB |
| | | Internal 1.5-V reference | | –3.0% | | 3.0% | |
| $E_T$ | Total unadjusted error (10-bit mode) | $V_{eref+}$ as reference | 2.4 V to 3.6 V | –2.0 | | 2.0 | LSB |
| | | Internal 1.5-V reference | | –3.0% | | 3.0% | |
| | Total unadjusted error (8-bit mode) | $V_{eref+}$ as reference | 2 V to 3.6 V | –2.0 | | 2.0 | LSB |
| | | Internal 1.5-V reference | | –3.0% | | 3.0% | |
| $V_{SENSOR}$ | See (1) | ADCON = 1, INCH = 0Ch, $T_A$ = 0°C | 3 V | | 913 | | mV |
| $TC_{SENSOR}$ | See (2) | ADCON = 1, INCH = 0Ch | 3 V | | 3.35 | | mV/°C |
| $t_{SENSOR}$ (sample) | Sample time required if channel 12 is selected (3) | ADCON = 1, INCH = 0Ch, Error of conversion result ≤1 LSB, AM and all LPMs above LPM3 | 3 V | 30 | | | µs |
| | | ADCON = 1, INCH = 0Ch, Error of conversion result ≤1 LSB, LPM3 | 3 V | 100 | | | |

(1) The temperature sensor offset can vary significantly. TI recommends a single-point calibration to minimize the offset error of the built-in temperature sensor.
(2) The device descriptor structure contains calibration values for 30°C and 85°C for each available reference voltage level. The sensor voltage can be computed as $V_{SENSE} = TC_{SENSOR} \times (\text{Temperature, °C}) + V_{SENSOR}$ , where $TC_{SENSOR}$ and $V_{SENSOR}$ can be computed from the calibration values for higher accuracy.
(3) The typical equivalent impedance of the sensor is 700 kΩ. The sample time required includes the sensor on time, $t_{SENSOR(on)}$.


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### 5.11.9 FRAM

Table 5-23 lists the characteristics of the FRAM.

**Table 5-23. FRAM**

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| | Read and write endurance | | $10^{15}$ | | | cycles |
| $t_{Retention}$ | Data retention duration | $T_J$ = 25°C | 100 | | | years |
| | | $T_J$ = 70°C | 40 | | | |
| | | $T_J$ = 85°C | 10 | | | |
| $I_{WRITE}$ | Current to write into FRAM | | | $I_{READ}$ (1) | | nA |
| $I_{ERASE}$ | Erase current | | | N/A (2) | | nA |
| $t_{WRITE}$ | Write time | | | $t_{READ}$ (3) | | ns |
| $t_{READ}$ | Read time | NWAITSx = 0 | | $1/f_{SYSTEM}$ (4) | | ns |
| | | NWAITSx = 1 | | $2/f_{SYSTEM}$ (4) | | |

(1) Writing to FRAM does not require a setup sequence or additional power when compared to reading from FRAM. The FRAM read current $I_{READ}$ is included in the active mode current consumption parameter $I_{AM,FRAM}$.
(2) FRAM does not require a special erase sequence.
(3) Writing into FRAM is as fast as reading.
(4) The maximum read (and write) speed is specified by $f_{SYSTEM}$ using the appropriate wait state settings (NWAITSx).

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### 5.11.10 Debug and Emulation

Table 5-24 lists the characteristics of the Spy-Bi-Wire interface.

**Table 5-24. JTAG, Spy-Bi-Wire Interface**

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 5-17)

| PARAMETER | | $V_{CC}$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $f_{SBW}$ | Spy-Bi-Wire input frequency | 2 V, 3 V | 0 | | 10 | MHz |
| $t_{SBW,Low}$ | Spy-Bi-Wire low clock pulse duration | 2 V, 3 V | 0.028 | | 15 | µs |
| $t_{SU,\ SBWTDIO}$ | SBWTDIO setup time (before falling edge of SBWTCK in TMS and TDI slot, Spy-Bi-Wire) | 2 V, 3 V | 4 | | | ns |
| $t_{HD,\ SBWTDIO}$ | SBWTDIO hold time (after rising edge of SBWTCK in TMS and TDI slot, Spy-Bi-Wire) | 2 V, 3 V | 19 | | | ns |
| $t_{Valid,\ SBWTDIO}$ | SBWTDIO data valid time (after falling edge of SBWTCK in TDO slot, Spy-Bi-Wire) | 2 V, 3 V | | | 31 | ns |
| $t_{SBW,\ En}$ | Spy-Bi-Wire enable time (TEST high to acceptance of first clock edge) (1) | 2 V, 3 V | | | 110 | µs |
| $t_{SBW,Ret}$ | Spy-Bi-Wire return to normal operation time (2) | 2 V, 3 V | 15 | | 100 | µs |
| $R_{internal}$ | Internal pulldown resistance on TEST | 2 V, 3 V | 20 | 35 | 50 | kΩ |

(1) Tools that access the Spy-Bi-Wire interface must wait for the $t_{SBW,En}$ time after pulling the TEST/SBWTCK pin high before applying the first SBWTCK clock edge.
(2) Maximum $t_{SBW,Ret}$ time after pulling or releasing the TEST/SBWTCK pin low until the Spy-Bi-Wire pins revert from their Spy-Bi-Wire function to their application function. This time applies only if the Spy-Bi-Wire mode is selected.

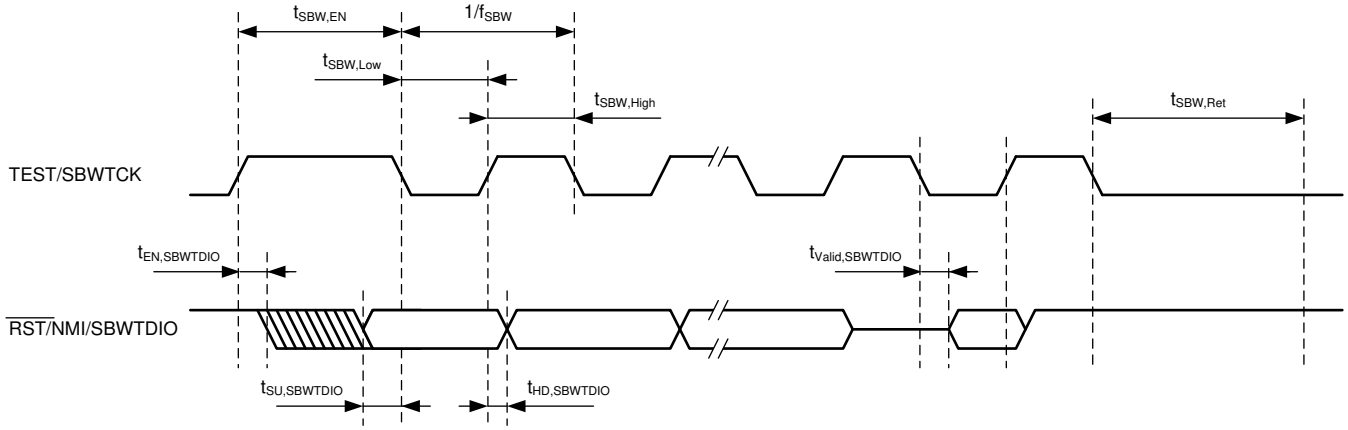


**Figure 5-17. JTAG Spy-Bi-Wire Timing**


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Table 5-25 lists the characteristics of the 4-wire JTAG interface.

**Table 5-25. JTAG, 4-Wire Interface**

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 5-18)

| PARAMETER | | $V_{CC}$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $f_{TCK}$ | TCK input frequency(1) | 2 V, 3 V | 0 | | 10 | MHz |
| $t_{TCK,Low}$ | TCK low clock pulse duration | 2 V, 3 V | 15 | | | ns |
| $t_{TCK,High}$ | TCK high clock pulse duration | 2 V, 3 V | 15 | | | ns |
| $t_{SU,TMS}$ | TMS setup time (before rising edge of TCK) | 2 V, 3 V | 11 | | | ns |
| $t_{HD,TMS}$ | TMS hold time (after rising edge of TCK) | 2 V, 3 V | 3 | | | ns |
| $t_{SU,TDI}$ | TDI setup time (before rising edge of TCK) | 2 V, 3 V | 13 | | | ns |
| $t_{HD,TDI}$ | TDI hold time (after rising edge of TCK) | 2 V, 3 V | 5 | | | ns |
| $t_{Z-Valid,TDO}$ | TDO high impedance to valid output time (after falling edge of TCK) | 2 V, 3 V | | | 26 | ns |
| $t_{Valid,TDO}$ | TDO to new valid output time (after falling edge of TCK) | 2 V, 3 V | | | 26 | ns |
| $t_{Valid-Z,TDO}$ | TDO valid to high-impedance output time (after falling edge of TCK) | 2 V, 3 V | | | 26 | ns |
| $t_{JTAG,Ret}$ | Spy-Bi-Wire return to normal operation time | | 15 | | 100 | µs |
| $R_{internal}$ | Internal pulldown resistance on TEST | 2 V, 3 V | 20 | 35 | 50 | kΩ |

(1) $f_{TCK}$ may be restricted to meet the timing requirements of the module selected.

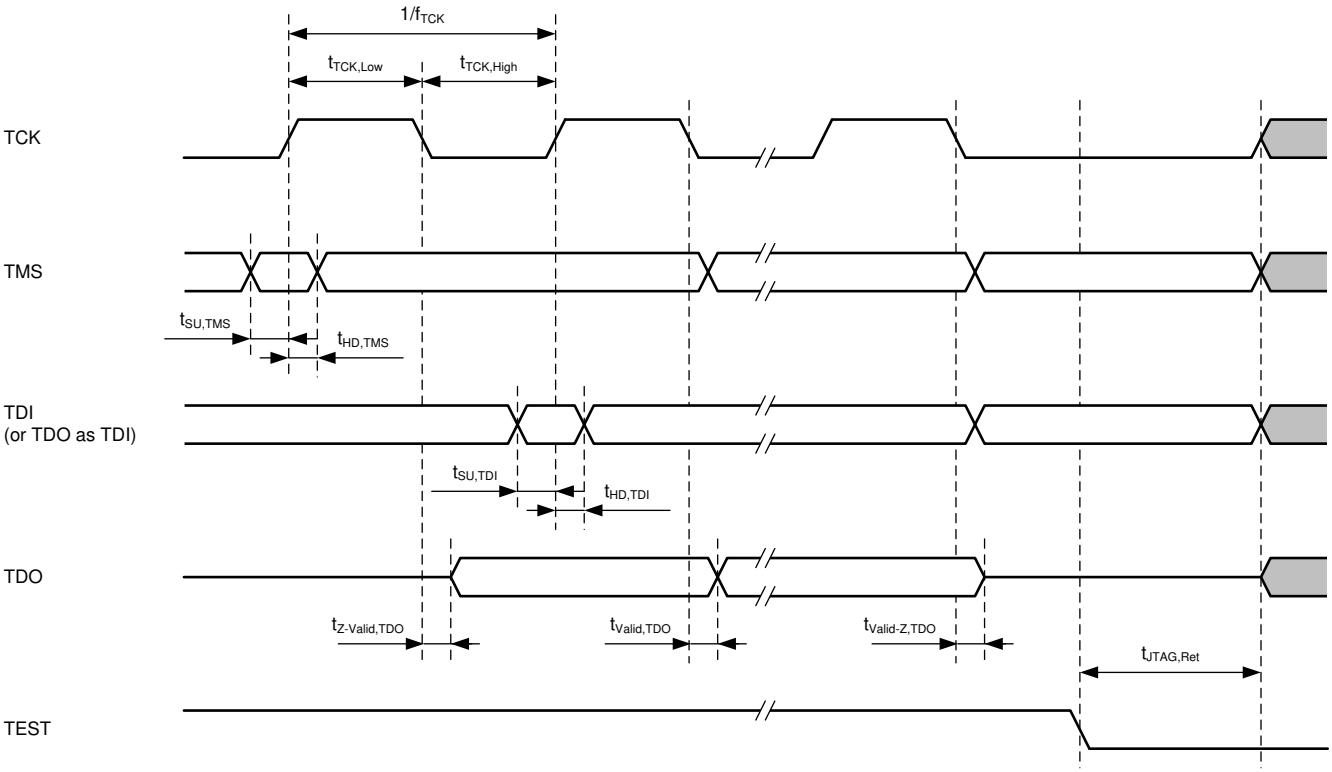


**Figure 5-18. JTAG 4-Wire Timing**

# 6 Detailed Description

## 6.1 Overview

The MSP430FR2433 is an ultra-low-power MCU. The architecture, combined with extensive low-power modes, is optimized to achieve extended battery life in, for example, portable measurement applications. The MCU features four 16-bit timers, three eUSCIs that support UART, SPI, and $I^2C$, a hardware multiplier, an RTC module with alarm capabilities, and a high-performance 10-bit ADC.

## 6.2 CPU

The MSP430 CPU has a 16-bit RISC architecture that is highly transparent to the application. All operations, other than program-flow instructions, are performed as register operations in conjunction with seven addressing modes for source operand and four addressing modes for destination operand.

The CPU is integrated with 16 registers that provide reduced instruction execution time. The register-to-register operation execution time is one cycle of the CPU clock.

Four of the registers, R0 to R3, are dedicated as program counter (PC), stack pointer (SP), status register (SR), and constant generator (CG), respectively. The remaining registers are general-purpose registers.

Peripherals are connected to the CPU using data, address, and control buses. Peripherals can be managed with all instructions.

## 6.3 Operating Modes

The MSP430FR2433 MCU has one active mode and several software-selectable low-power modes of operation (see Table 6-1). An interrupt event can wake the MCU from low-power mode (LPM0 or LPM3), service the request, and restore the MCU back to the low-power mode on return from the interrupt program. Low-power modes LPM3.5 and LPM4.5 disable the core supply to minimize power consumption.

**Table 6-1. Operating Modes**

| MODE | | AM | LPM0 | LPM3 | LPM4 | LPM3.5 | LPM4.5 |
|---|---|---|---|---|---|---|---|
| | | ACTIVE MODE (FRAM ON) | CPU OFF | STANDBY | OFF | ONLY RTC | SHUTDOWN |
| Maximum system clock | | 16 MHz | 16 MHz | 40 kHz | 0 | 40 kHz | 0 |
| Power consumption at 25°C, 3 V | | 126 µA/MHz | 40 µA/MHz | 1.2 µA with RTC counter only in LFXT | 0.49 µA without SVS | 0.73 µA with RTC counter only in LFXT | 16 nA without SVS |
| Wake-up time | | N/A | Instant | 10 µs | 10 µs | 350 µs | 350 µs |
| Wake-up events | | N/A | All | All | I/O | RTC I/O | I/O |
| Power | Regulator | Full Regulation | Full Regulation | Partial Power Down | Partial Power Down | Partial Power Down | Power Down |
| | SVS | On | On | Optional | Optional | Optional | Optional |
| | Brownout | On | On | On | On | On | On |
| Clock(1) | MCLK | Active | Off | Off | Off | Off | Off |
| | SMCLK | Optional | Optional | Off | Off | Off | Off |
| | FLL | Optional | Optional | Off | Off | Off | Off |
| | DCO | Optional | Optional | Off | Off | Off | Off |
| | MODCLK | Optional | Optional | Off | Off | Off | Off |
| | REFO | Optional | Optional | Optional | Off | Off | Off |
| | ACLK | Optional | Optional | Optional | Off | Off | Off |
| | XT1CLK | Optional | Optional | Optional | Off | Optional | Off |
| | VLOCLK | Optional | Optional | Optional | Off | Optional | Off |

(1) The status shown for LPM4 applies to internal clocks only.


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**Table 6-1. Operating Modes (continued)**

| MODE | | AM | LPM0 | LPM3 | LPM4 | LPM3.5 | LPM4.5 |
|---|---|---|---|---|---|---|---|
| | | ACTIVE MODE (FRAM ON) | CPU OFF | STANDBY | OFF | ONLY RTC | SHUTDOWN |
| Core | CPU | On | Off | Off | Off | Off | Off |
| | FRAM | On | On | Off | Off | Off | Off |
| | RAM | On | On | On | On | Off | Off |
| | Backup memory(2) | On | On | On | On | On | Off |
| Peripherals | Timer0_A3 | Optional | Optional | Optional | Off | Off | Off |
| | Timer1_A3 | Optional | Optional | Optional | Off | Off | Off |
| | Timer2_A2 | Optional | Optional | Optional | Off | Off | Off |
| | Timer3_A2 | Optional | Optional | Optional | Off | Off | Off |
| | WDT | Optional | Optional | Optional | Off | Off | Off |
| | eUSCI_A0 | Optional | Optional | Off | Off | Off | Off |
| | eUSCI_A1 | Optional | Optional | Off | Off | Off | Off |
| | eUSCI_B0 | Optional | Optional | Off | Off | Off | Off |
| | CRC | Optional | Optional | Off | Off | Off | Off |
| | ADC | Optional | Optional | Optional | Off | Off | Off |
| | RTC | Optional | Optional | Optional | Off | Optional | Off |
| I/O | General-purpose digital input/output | On | Optional | State Held | State Held | State Held | State Held |

(2) Backup memory contains 32 bytes of register space in peripheral memory. See Table 6-24 and Table 6-43 for its memory allocation.

**NOTE**

XT1CLK and VLOCLK can be active during LPM4 if requested by low-frequency peripherals, such as RTC or WDT.

## 6.4 Interrupt Vector Addresses

The interrupt vectors and the power-up start address are in the address range 0FFFFh to 0FF80h (see Table 6-2). The vector contains the 16-bit address of the appropriate interrupt-handler instruction sequence.

**Table 6-2. Interrupt Sources, Flags, and Vectors**

| INTERRUPT SOURCE | INTERRUPT FLAG | SYSTEM INTERRUPT | WORD ADDRESS | PRIORITY |
|---|---|---|---|---|
| **System Reset**<br>Power up, Brownout, Supply supervisor<br>External reset RST<br>Watchdog time-out, Key violation<br>FRAM access time error<br>FRAM uncorrectable bit error detection<br>Software POR, BOR<br>FLL unlock error | PMMPORIFG, PMMBORIFG, SVSHIFG<br>PMMRSTIFG<br>WDTIFG<br>ACCTEIFG<br>UBDIFG<br>SYSRSTIV<br>FLLUNLOCKIFG | Reset | FFFEh | 63, Highest |
| **System NMI**<br>Vacant memory access<br>JTAG mailbox<br>FRAM bit error detection | VMAIFG<br>JMBINIFG, JMBOUTIFG<br>CBDIFG, UBDIFG | Nonmaskable | FFFCh | 62 |
| **User NMI**<br>External NMI<br>Oscillator fault | NMIIFG<br>OFIFG | Nonmaskable | FFFAh | 61 |
| Timer0_A3 | TA0CCR0 CCIFG0 | Maskable | FFF8h | 60 |
| Timer0_A3 | TA0CCR1 CCIFG1, TA0CCR2 CCIFG2, TA0IFG (TA0IV) | Maskable | FFF6h | 59 |

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**Table 6-2. Interrupt Sources, Flags, and Vectors (continued)**

| INTERRUPT SOURCE | INTERRUPT FLAG | SYSTEM INTERRUPT | WORD ADDRESS | PRIORITY |
|---|---|---|---|---|
| Timer1_A3 | TA1CCR0 CCIFG0 | Maskable | FFF4h | 58 |
| Timer1_A3 | TA1CCR1 CCIFG1, TA1CCR2 CCIFG2, TA1IFG (TA1IV) | Maskable | FFF2h | 57 |
| Timer2_A2 | TA2CCR0 CCIFG0 | Maskable | FFF0h | 56 |
| Timer2_A2 | TA2CCR1 CCIFG1, TA2IFG (TA2IV) | | FFEEh | 55 |
| Timer3_A2 | TA3CCR0 CCIFG0 | Maskable | FFECh | 54 |
| Timer3_A2 | TA3CCR1 CCIFG1, TA3IFG (TA3IV) | | FFEAh | 53 |
| RTC | RTCIFG | Maskable | FFE8h | 52 |
| Watchdog timer interval mode | WDTIFG | Maskable | FFE6h | 51 |
| eUSCI_A0 receive or transmit | UCTXCPTIFG, UCSTTIFG, UCRXIFG, UCTXIFG (UART mode) UCRXIFG, UCTXIFG (SPI mode) (UCA0IV) | Maskable | FFE4h | 50 |
| eUSCI_A1 receive or transmit | UCTXCPTIFG, UCSTTIFG, UCRXIFG, UCTXIFG (UART mode) UCRXIFG, UCTXIFG (SPI mode) (UCA1IV) | Maskable | FFE2h | 49 |
| eUSCI_B0 receive or transmit | UCB0RXIFG, UCB0TXIFG (SPI mode) UCALIFG, UCNACKIFG, UCSTTIFG, UCSTPIFG, UCRXIFG0, UCTXIFG0, UCRXIFG1, UCTXIFG1, UCRXIFG2, UCTXIFG2, UCRXIFG3, UCTXIFG3, UCCNTIFG, UCBIT9IFG ($I^2C$ mode) (UCB0IV) | Maskable | FFE0h | 48 |
| ADC | ADCIFG0, ADCINIFG, ADCLOIFG, ADCHIIFG, ADCTOVIFG, ADCOVIFG (ADCIV) | Maskable | FFDEh | 47 |
| P1 | P1IFG.0 to P1IFG.7 (P1IV) | Maskable | FFDCh | 46 |
| P2 | P2IFG.0 to P2IFG.7 (P2IV) | Maskable | FFDAh | 45, Lowest |
| Reserved | Reserved | Maskable | FFD6h to FF88h | |
| Signatures | BSL Signature 2 | | 0FF86h | |
| | BSL Signature 1 | | 0FF84h | |
| | JTAG Signature 2 | | 0FF82h | |
| | JTAG Signature 1 | | 0FF80h | |


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## 6.5 Bootloader (BSL)

The BSL lets users program the FRAM or RAM using either the UART serial interface or the $I^2C$ interface. Access to the MCU memory through the BSL is protected by an user-defined password. Use of the BSL requires four pins (see Table 6-3 and Table 6-4). BSL entry requires a specific entry sequence on the $\overline{\text{RST}}$/NMI/SBWTDIO and TEST/SBWTCK pins. This device supports the blank device detection to automatically invoke the BSL, skipping this special entry sequence, to save time and simplify onboard programming. For a complete description of the features of the BSL, see the MSP430 FRAM Device Bootloader (BSL) User's Guide.

**Table 6-3. UART BSL Pin Requirements and Functions**

| DEVICE SIGNAL | BSL FUNCTION |
|---|---|
| $\overline{\text{RST}}$/NMI/SBWTDIO | Entry sequence signal |
| TEST/SBWTCK | Entry sequence signal |
| P1.4 | Data transmit |
| P1.5 | Data receive |
| VCC | Power supply |
| VSS | Ground supply |

**Table 6-4. $I^2C$ BSL Pin Requirements and Functions**

| DEVICE SIGNAL | BSL FUNCTION |
|---|---|
| $\overline{\text{RST}}$/NMI/SBWTDIO | Entry sequence signal |
| TEST/SBWTCK | Entry sequence signal |
| P1.2 | Data transmit and receive |
| P1.3 | Clock |
| VCC | Power supply |
| VSS | Ground supply |

## 6.6 JTAG Standard Interface

The MSP low-power microcontrollers support the standard JTAG interface, which requires four signals for sending and receiving data. The JTAG signals are shared with general-purpose I/O. The TEST/SBWTCK pin enables the JTAG signals. In addition to these signals, the $\overline{\text{RST}}$/NMI/SBWTDIO is required to interface with MSP430 development tools and device programmers. Table 6-5 lists the JTAG pin requirements. For further details on interfacing to development tools and device programmers, see the *MSP430 Hardware Tools User's Guide*. For details on using the JTAG interface, see *MSP430 Programming With the JTAG Interface*.

**Table 6-5. JTAG Pin Requirements and Function**

| DEVICE SIGNAL | DIRECTION | JTAG FUNCTION |
|---|---|---|
| P1.4/UCA0TXD/UCA0SIMO/TA1.2/TCK/A4/VREF+ | IN | JTAG clock input |
| P1.5/UCA0RXD/UCA0SOMI/TA1.1/TMS/A5 | IN | JTAG state control |
| P1.6/UCA0CLK/TA1CLK/TDI/TCLK/A6 | IN | JTAG data input, TCLK input |
| P1.7/UCA0STE/SMCLK/TDO/A7 | OUT | JTAG data output |
| TEST/SBWTCK | IN | Enable JTAG pins |
| $\overline{\text{RST}}$/NMI/SBWTDIO | IN | External reset |
| DVCC | – | Power supply |
| DVSS | – | Ground supply |

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## 6.7 Spy-Bi-Wire Interface (SBW)

The MSP low-power microcontrollers support the 2-wire SBW interface. SBW can be used to interface with MSP development tools and device programmers. Table 6-6 lists the SBW interface pin requirements. For further details on interfacing to development tools and device programmers, see the *MSP430 Hardware Tools User's Guide*. For details on using the SBW interface, see the *MSP430 Programming With the JTAG Interface*.

**Table 6-6. Spy-Bi-Wire Pin Requirements and Functions**

| DEVICE SIGNAL | DIRECTION | SBW FUNCTION |
|---|---|---|
| TEST/SBWTCK | IN | Spy-Bi-Wire clock input |
| $\overline{\text{RST}}$/NMI/SBWTDIO | IN, OUT | Spy-Bi-Wire data input and output |
| DVCC | – | Power supply |
| DVSS | – | Ground supply |

## 6.8 FRAM

The FRAM can be programmed using the JTAG port, SBW, the BSL, or in-system by the CPU. Features of the FRAM include:

- Byte and word access capability
- Programmable wait state generation
- Error correction coding (ECC)

## 6.9 Memory Protection

The device features memory protection for user access authority and write protection, including options to:

- Secure the whole memory map to prevent unauthorized access from JTAG port or BSL, by writing JTAG and BSL signatures using the JTAG port, SBW, the BSL, or in-system by the CPU.
- Enable write protection to prevent unwanted write operation to FRAM contents by setting the control bits in the System Configuration 0 register. For detailed information, see the *System Resets, Interrupts, and Operating Modes, System Control Module (SYS)* chapter in the *MP430FR4xx and MP430FR2xx Family User's Guide*.


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## 6.10 Peripherals

Peripherals are connected to the CPU through data, address, and control buses. All peripherals can be handled by using all instructions in the memory map. For complete module description, see the *MP430FR4xx and MP430FR2xx Family User's Guide*.

### *6.10.1 Power-Management Module (PMM)*

The PMM includes an integrated voltage regulator that supplies the core voltage to the device. The PMM also includes supply voltage supervisor (SVS) and brownout protection. The brownout reset circuit (BOR) is implemented to provide the proper internal reset signal to the device during power on and power off. The SVS circuitry detects if the supply voltage drops below a user-selectable safe level. SVS circuitry is available on the primary supply.

The device contains two on-chip reference: 1.5 V for internal reference and 1.2 V for external reference.

The 1.5-V reference is internally connected to ADC channel 13. DVCC is internally connected to ADC channel 15. When DVCC is set as the reference voltage for ADC conversion, the DVCC can be easily represent as Equation 1 by using ADC sampling 1.5-V reference without any external components support.

$$DVCC = (1023 \times 1.5\ V) \div 1.5\text{-}V\ reference\ ADC\ result \quad (1)$$

A 1.2-V reference voltage can be buffered and output to P1.4/MCLK/TCK/A4/VREF+, when EXTREFEN = 1 in the PMMCTL1 register. ADC channel 4 can also be selected to monitor this voltage. For more detailed information, see the *MP430FR4xx and MP430FR2xx Family User's Guide*.

### *6.10.2 Clock System (CS) and Clock Distribution*

The clock system includes a 32-kHz crystal oscillator (XT1), an internal very-low-power low-frequency oscillator (VLO), an integrated 32-kHz RC oscillator (REFO), an integrated internal digitally controlled oscillator (DCO) that may use frequency-locked loop (FLL) locking with internal or external 32-kHz reference clock, and an on-chip asynchronous high-speed clock (MODOSC). The clock system is designed for cost-effective designs with minimal external components. A fail-safe mechanism is included for XT1. The clock system module offers the following clock signals.

- Main Clock (MCLK): The system clock used by the CPU and all relevant peripherals accessed by the bus. All clock sources except MODOSC can be selected as the source with a predivider of 1, 2, 4, 8, 16, 32, 64, or 128.
- Sub-Main Clock (SMCLK): The subsystem clock used by the peripheral modules. SMCLK derives from the MCLK with a predivider of 1, 2, 4, or 8. This means SMCLK is always equal to or less than MCLK.
- Auxiliary Clock (ACLK): This clock is derived from the external XT1 clock or internal REFO clock up to 40 kHz.

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All peripherals may have one or several clock sources depending on specific functionality. Table 6-7 lists the clock distribution used in this device.

**Table 6-7. Clock Distribution**

| | CLOCK SOURCE SELECT BITS | MCLK | SMCLK | ACLK | MODCLK | XT1CLK | VLOCLK | EXTERNAL PIN |
|---|---|---|---|---|---|---|---|---|
| Frequency Range | | DC to 16 MHz | DC to 16 MHz | DC to 40 kHz | 5 MHz ±10% | DC to 40 kHz | 10 kHz ±50% | – |
| CPU | N/A | Default | – | – | – | – | – | – |
| FRAM | N/A | Default | – | – | – | – | – | – |
| RAM | N/A | Default | – | – | – | – | – | – |
| CRC | N/A | Default | – | – | – | – | – | – |
| I/O | N/A | Default | – | – | – | – | – | – |
| TA0 | TASSEL | – | 10b | 01b | – | – | – | 00b (TA0CLK pin) |
| TA1 | TASSEL | – | 10b | 01b | – | – | – | 00b (TA1CLK pin) |
| TA2 | TASSEL | – | 10b | 01b | – | – | – | – |
| TA3 | TASSEL | – | 10b | 01b | – | – | – | – |
| eUSCI_A0 | UCSSEL | – | 10b or 11b | – | 01b | – | – | 00b (UCA0CLK pin) |
| eUSCI_A1 | UCSSEL | – | 10b or 11b | – | 01b | – | – | 00b (UCA1CLK pin) |
| eUSCI_B0 | UCSSEL | – | 10b or 11b | – | 01b | – | – | 00b (UCB0CLK pin) |
| WDT | WDTSSEL | – | 00b | 01b | – | – | 10b or 11b | – |
| ADC | ADCSSEL | – | 11b | 01b | 00b | – | – | – |
| RTC | RTCSS | – | 01b | – | – | 10b | 11b | – |

### 6.10.3 General-Purpose Input/Output Port (I/O)

Up to 19 I/O ports are implemented.

- P1 and P2 are full 8-bit ports; P3 has 3 bits implemented.
- All individual I/O bits are independently programmable.
- Any combination of input, output, and interrupt conditions is possible.
- All ports support programmable pullup or pulldown.
- Edge-selectable interrupt and LPM3.5 and LPM4.5 wake-up input capability is available for P1 and P2.
- Read and write access to port-control registers is supported by all instructions.
- Ports can be accessed byte-wise or word-wise in pairs.

**NOTE**

**Configuration of digital I/Os after BOR reset**

To prevent any cross currents during start-up of the device, all port pins are high-impedance with Schmitt triggers and module functions disabled. To enable the I/O functions after a BOR reset, the ports must be configured first and then the LOCKLPM5 bit must be cleared. For details, see the *Configuration After Reset* section in the *Digital I/O* chapter of the *MP430FR4xx and MP430FR2xx Family User's Guide*.


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### 6.10.4 Watchdog Timer (WDT)

The primary function of the WDT module is to perform a controlled system restart after a software problem occurs. If the selected time interval expires, a system reset is generated. If the watchdog function is not needed in an application, the module can be configured as interval timer and can generate interrupts at selected time intervals. Table 6-8 lists the system clocks that can be used to source the WDT.

**Table 6-8. WDT Clocks**

| WDTSSEL | NORMAL OPERATION (WATCHDOG AND INTERVAL TIMER MODE) |
|---|---|
| 00 | SMCLK |
| 01 | ACLK |
| 10 | VLOCLK |
| 11 | Reserved |

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### 6.10.5 System (SYS) Module

The SYS module handles many of the system functions within the device. These features include power-on reset (POR) and power-up clear (PUC) handling, NMI source selection and management, reset interrupt vector generators, bootloader entry mechanisms, and configuration management (device descriptors). The SYS module also includes a data exchange mechanism through SBW called a JTAG mailbox mail box that can be used in the application. Table 6-9 summarizes the interrupts that are managed by the SYS module.

**Table 6-9. System Module Interrupt Vector Registers**

| INTERRUPT VECTOR REGISTER | ADDRESS | INTERRUPT EVENT | VALUE | PRIORITY |
|---|---|---|---|---|
| SYSRSTIV, System Reset | 015Eh | No interrupt pending | 00h | |
| | | Brownout (BOR) | 02h | Highest |
| | | RSTIFG $\overline{\text{RST}}$/NMI (BOR) | 04h | |
| | | PMMSWBOR software BOR (BOR) | 06h | |
| | | LPMx.5 wake up (BOR) | 08h | |
| | | Security violation (BOR) | 0Ah | |
| | | Reserved | 0Ch | |
| | | SVSHIFG SVSH event (BOR) | 0Eh | |
| | | Reserved | 10h | |
| | | Reserved | 12h | |
| | | PMMSWPOR software POR (POR) | 14h | |
| | | WDTIFG watchdog time-out (PUC) | 16h | |
| | | WDTPW password violation (PUC) | 18h | |
| | | FRCTLPW password violation (PUC) | 1Ah | |
| | | Uncorrectable FRAM bit error detection | 1Ch | |
| | | Peripheral area fetch (PUC) | 1Eh | |
| | | PMMPW PMM password violation (PUC) | 20h | |
| | | FLL unlock (PUC) | 24h | |
| | | Reserved | 22h, 26h to 3Eh | Lowest |
| SYSSNIV, System NMI | 015Ch | No interrupt pending | 00h | |
| | | SVS low-power reset entry | 02h | Highest |
| | | Uncorrectable FRAM bit error detection | 04h | |
| | | Reserved | 06h | |
| | | Reserved | 08h | |
| | | Reserved | 0Ah | |
| | | Reserved | 0Ch | |
| | | Reserved | 0Eh | |
| | | Reserved | 10h | |
| | | VMAIFG Vacant memory access | 12h | |
| | | JMBINIFG JTAG mailbox input | 14h | |
| | | JMBOUTIFG JTAG mailbox output | 16h | |
| | | Correctable FRAM bit error detection | 18h | |
| | | Reserved | 1Ah to 1Eh | Lowest |
| SYSUNIV, User NMI | 015Ah | No interrupt pending | 00h | |
| | | NMIIFG NMI pin or $SVS_H$ event | 02h | Highest |
| | | OFIFG oscillator fault | 04h | |
| | | Reserved | 06h to 1Eh | Lowest |


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### 6.10.6 Cyclic Redundancy Check (CRC)

The 16-bit cyclic redundancy check (CRC) module produces a signature based on a sequence of data values and can be used for data checking purposes. The CRC generation polynomial is compliant with CRC-16-CCITT standard of $x^{16} + x^{12} + x^5 + 1$.

### 6.10.7 Enhanced Universal Serial Communication Interface (eUSCI_A0, eUSCI_B0)

The eUSCI modules are used for serial data communications. The eUSCI_A module supports either UART or SPI communications. The eUSCI_B module supports either SPI or $I^2C$ communications. Additionally, eUSCI_A supports automatic baud-rate detection and IrDA. Table 6-10 lists the pin configurations that are required for each eUSCI mode.

**Table 6-10. eUSCI Pin Configurations**

| | PIN | UART | SPI |
|---|---|---|---|
| eUSCI_A0 | P1.4 | TXD | SIMO |
| | P1.5 | RXD | SOMI |
| | P1.6 | – | SCLK |
| | P1.7 | – | STE |
| eUSCI_A1 | P2.6 | TXD | SIMO |
| | P2.5 | RXD | SOMI |
| | P2.4 | – | SCLK |
| | P3.1 | – | STE |
| | **PIN** | **$I^2C$** | **SPI** |
| eUSCI_B0 | P1.0 | – | STE |
| | P1.1 | – | SCLK |
| | P1.2 | SDA | SIMO |
| | P1.3 | SCL | SOMI |

### 6.10.8 Timers (Timer0_A3, Timer1_A3, Timer2_A2 and Timer3_A2)

The Timer0_A3 and Timer1_A3 modules are 16-bit timers and counters with three capture/compare registers each. Both timers support multiple captures or compares, PWM outputs, and interval timing (see Table 6-11 and Table 6-12). Both timers have extensive interrupt capabilities. Interrupts may be generated from the counter on overflow conditions and from each capture/compare register.

The CCR0 registers on Timer0_A3 and Timer1_A3 are not externally connected and can be used only for hardware period timing and interrupt generation. In Up mode, these CCR0 registers can be used to set the overflow value of the counter.

**Table 6-11. Timer0_A3 Signal Connections**

| PORT PIN | DEVICE INPUT SIGNAL | MODULE INPUT NAME | MODULE BLOCK | MODULE OUTPUT SIGNAL | DEVICE OUTPUT SIGNAL |
|---|---|---|---|---|---|
| P1.0 | TA0CLK | TACLK | Timer | N/A | |
| | ACLK (internal) | ACLK | | | |
| | SMCLK (internal) | SMCLK | | | |
| | | CCI0A | CCR0 | TA0 | |
| | | CCI0B | | | Timer1_A3 CCI0B input |
| | DVSS | GND | | | |
| | DVCC | VCC | | | |
| P1.1 | TA0.1 | CCI1A | CCR1 | TA1 | TA0.1 |
| | from RTC (internal) | CCI1B | | | Timer1_A3 CCI1B input |
| | DVSS | GND | | | |
| | DVCC | VCC | | | |
| P1.2 | TA0.2 | CCI2A | CCR2 | TA2 | TA0.2 |
| | | CCI2B | | | Timer1_A3 CCI2B input, IR Input |
| | DVSS | GND | | | |
| | DVCC | VCC | | | |


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**Table 6-12. Timer1_A3 Signal Connections**

| PORT PIN | DEVICE INPUT SIGNAL | MODULE INPUT NAME | MODULE BLOCK | MODULE OUTPUT SIGNAL | DEVICE OUTPUT SIGNAL |
|---|---|---|---|---|---|
| P1.6 | TA1CLK | TACLK | Timer | N/A | |
| | ACLK (internal) | ACLK | | | |
| | SMCLK (internal) | SMCLK | | | |
| | | CCI0A | CCR0 | TA0 | |
| | Timer0_A3 CCR0B output (internal) | CCI0B | | | |
| | DVSS | GND | | | |
| | DVCC | VCC | | | |
| P1.5 | TA1.1 | CCI1A | CCR1 | TA1 | TA1.1 |
| | Timer0_A3 CCR1B output (internal) | CCI1B | | | to ADC trigger |
| | DVSS | GND | | | |
| | DVCC | VCC | | | |
| P1.4 | TA1.2 | CCI2A | CCR2 | TA2 | TA1.2 |
| | Timer0_A3 CCR2B output (internal) | CCI2B | | | IR Input |
| | DVSS | GND | | | |
| | DVCC | VCC | | | |

The interconnection of Timer0_A3 and Timer1_A3 can be used to modulate the eUSCI_A pin of UCA0TXD/UCA0SIMO in either ASK or FSK mode, with which a user can easily acquire a modulated infrared command for directly driving an external IR diode. The IR functions are fully controlled by SYS configuration registers 1 including IREN (enable), IRPSEL (polarity select), IRMSEL (mode select), IRDSSEL (data select), and IRDATA (data) bits. For more information, see the *System Resets, Interrupts, and Operating Modes, System Control Module (SYS)* chapter in the *MP430FR4xx and MP430FR2xx Family User's Guide*.

The Timer2_A2 and Timer3_A2 modules are 16-bit timers and counters with two capture/compare registers each. Both timers support multiple captures or compares and interval timing (see Table 6-13 and Table 6-14). Both timers have extensive interrupt capabilities. Interrupts may be generated from the counter on overflow conditions and from each capture register.

The CCR0 registers on Timer2_TA2 and Timer3_TA2 are not externally connected and can be used only for hardware period timing and interrupt generation. In Up mode, these CCR0 registers can be used to set the overflow value of the counter. Timer2_A2 and Timer3_A2 are only internally connected and do not support PWM output.

**Table 6-13. Timer2_A2 Signal Connections**

| DEVICE INPUT SIGNAL | MODULE INPUT NAME | MODULE BLOCK | MODULE OUTPUT SIGNAL | DEVICE OUTPUT SIGNAL |
|---|---|---|---|---|
| ACLK (internal) | ACLK | Timer | N/A | |
| SMCLK (internal) | SMCLK | | | |
| | CCI0A | CCR0 | TA0 | |
| | CCI0B | | | Timer3_A3 CCI0B input |
| DVSS | GND | | | |
| DVCC | VCC | | | |
| | CCI1A | CCR1 | CCR1 | |
| | CCI1B | | | Timer3_A3 CCI1B input |
| DVSS | GND | | | |
| DVCC | VCC | | | |

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**Table 6-14. Timer3_A2 Signal Connections**

| DEVICE INPUT SIGNAL | MODULE INPUT NAME | MODULE BLOCK | MODULE OUTPUT SIGNAL | DEVICE OUTPUT SIGNAL |
|---|---|---|---|---|
| ACLK (internal) | ACLK | Timer | N/A | |
| SMCLK (internal) | SMCLK | | | |
| | CCI0A | CCR0 | TA0 | |
| Timer3_A3 CCI0B input | CCI0B | | | |
| DVSS | GND | | | |
| DVCC | VCC | | | |
| | CCI1A | CCR1 | CCR1 | |
| Timer3_A3 CCI1B input | CCI1B | | | |
| DVSS | GND | | | |
| DVCC | VCC | | | |

### 6.10.9 Hardware Multiplier (MPY)

The multiplication operation is supported by a dedicated peripheral module. The module performs operations with 32-, 24-, 16-, and 8-bit operands. The MPY module supports signed multiplication, unsigned multiplication, signed multiply-and-accumulate, and unsigned multiply-and-accumulate operations.

### 6.10.10 Backup Memory (BAKMEM)

The BAKMEM supports data retention during LPM3.5. This device provides up to 32 bytes that are retained during LPM3.5.

### 6.10.11 Real-Time Clock (RTC)

The RTC is a 16-bit modulo counter that is functional in AM, LPM0, LPM3, and LPM3.5. This module may periodically wake up the CPU from LPM0, LPM3, and LPM3.5 based on timing from a low-power clock source such as the XT1 and VLO clocks. In AM, SMCLK can drive the RTC to generate high-frequency timing events and interrupts. The RTC overflow events trigger:

- Timer0_A3 CCR1B
- ADC conversion trigger when ADCSHSx bits are set as 01b


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### 6.10.12 10-Bit Analog-to-Digital Converter (ADC)

The 10-bit ADC module supports fast 10-bit analog-to-digital conversions with single-ended input. The module implements a 10-bit SAR core, sample select control, reference generator and a conversion result buffer. A window comparator with lower and upper limits allows CPU-independent result monitoring with three window comparator interrupt flags.

The ADC supports 10 external inputs and 4 internal inputs (see Table 6-15).

**Table 6-15. ADC Channel Connections**

| ADCINCHx | ADC CHANNELS | EXTERNAL PINOUT |
|---|---|---|
| 0 | A0/Veref+ | P1.0 |
| 1 | A1 | P1.1 |
| 2 | A2/Veref- | P1.2 |
| 3 | A3 | P1.3 |
| 4 | A4 (1) | P1.4 |
| 5 | A5 | P1.5 |
| 6 | A6 | P1.6 |
| 7 | A7 | P1.7 |
| 8 | A8 | NA |
| 9 | A9 | NA |
| 10 | Not used | N/A |
| 11 | Not used | N/A |
| 12 | On-chip temperature sensor | N/A |
| 13 | Reference voltage (1.5 V) | N/A |
| 14 | DVSS | N/A |
| 15 | DVCC | N/A |

(1) When A4 is used, the PMM 1.2-V reference voltage can be output to this pin by setting the PMM control register. The 1.2-V voltage can be directly measured by A4 channel.

Software or a hardware trigger can start the analog-to-digital conversion. Table 6-16 lists the trigger sources that are available.

**Table 6-16. ADC Trigger Signal Connections**

| ADCSHSx | | TRIGGER SOURCE |
|---|---|---|
| BINARY | DECIMAL | |
| 00 | 0 | ADCSC bit (software trigger) |
| 01 | 1 | RTC event |
| 10 | 2 | TA1.1B |
| 11 | 3 | -- |

### 6.10.13 Embedded Emulation Module (EEM)

The EEM supports real-time in-system debugging. The EEM on these devices has the following features:

- Three hardware triggers or breakpoints on memory access
- One hardware trigger or breakpoint on CPU register write access
- Up to four hardware triggers that can be combined to form complex triggers or breakpoints
- One cycle counter
- Clock control on module level
- EEM version: S

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## 6.11 Input/Output Diagrams

### 6.11.1 Port P1 Input/Output With Schmitt Trigger

Figure 6-1 shows the port diagram. Table 6-17 summarizes the selection of pin function.

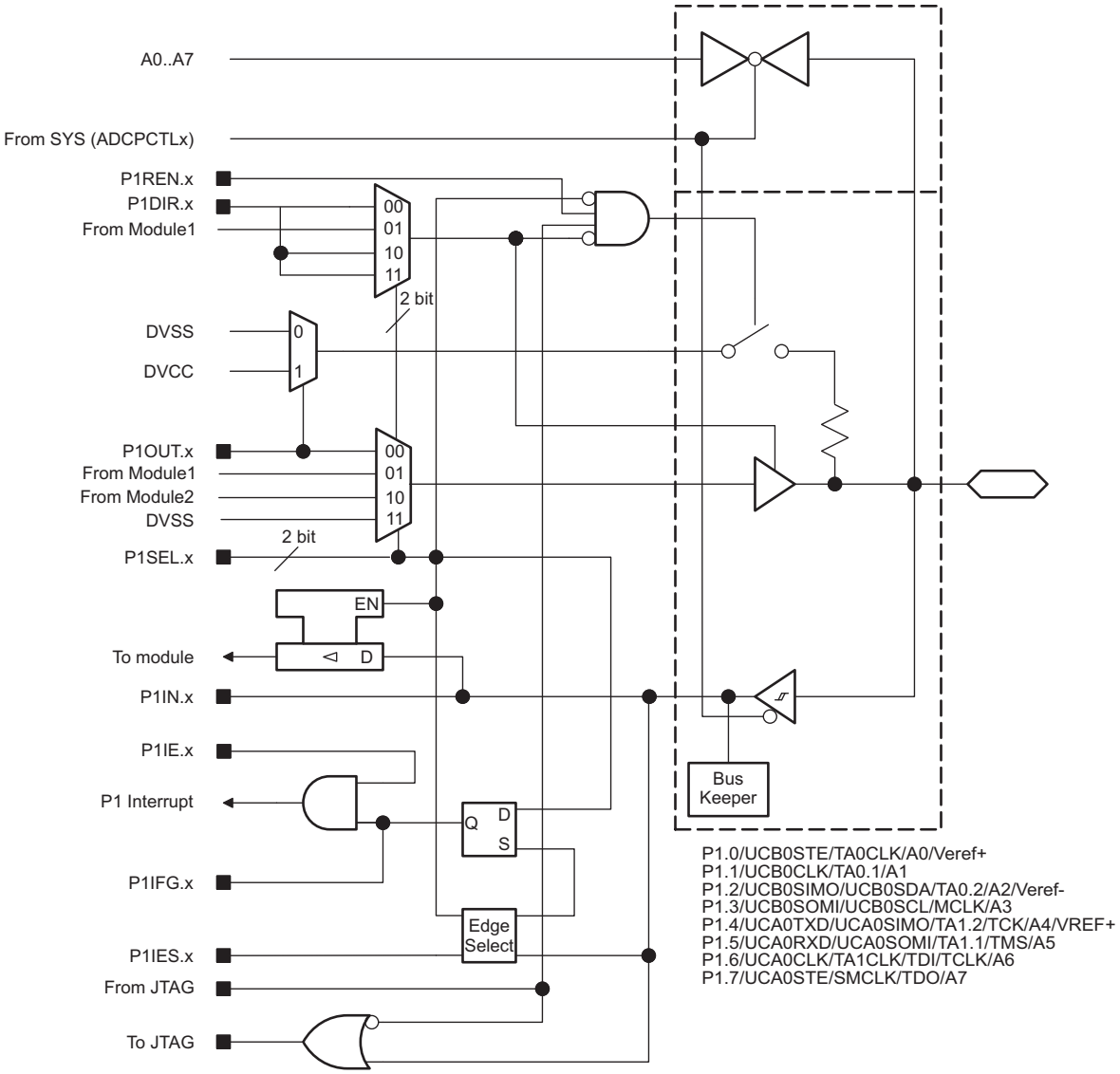


**Figure 6-1. Port P1 (P1.0 to P1.7) Input/Output With Schmitt Trigger**


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**Table 6-17. Port P1 (P1.0 to P1.7) Pin Functions**

| PIN NAME (P1.x) | x | FUNCTION | CONTROL BITS AND SIGNALS[1] | | | |
|---|---|---|---|---|---|---|
| | | | P1DIR.x | P1SELx | ADCPCTLx[2] | JTAG |
| P1.0/UCB0STE/ TA0CLK/A0 | 0 | P1.0 (I/O) | I: 0; O: 1 | 00 | 0 | N/A |
| | | UCB0STE | X | 01 | 0 | N/A |
| | | TA0CLK | 0 | 10 | 0 | N/A |
| | | A0/Veref+ | X | X | 1 (x = 0) | N/A |
| P1.1/UCB0CLK/TA0.1/ A1 | 1 | P1.1 (I/O) | I: 0; O: 1 | 00 | 0 | N/A |
| | | UCB0CLK | X | 01 | 0 | N/A |
| | | TA0.CCI1A | 0 | 10 | 0 | N/A |
| | | TA0.1 | 1 | | | |
| | | A1 | X | X | 1 (x = 1) | N/A |
| P1.2/UCB0SIMO/ UCB0SDA/TA0.2/A2 | 2 | P1.2 (I/O) | I: 0; O: 1 | 00 | 0 | N/A |
| | | UCB0SIMO/UCB0SDA | X | 01 | 0 | N/A |
| | | TA0.CCI2A | 0 | 10 | 0 | N/A |
| | | TA0.2 | 1 | | | |
| | | A2/Veref- | X | X | 1 (x = 2) | N/A |
| P1.3/UCB0SOMI/ UCB0SCL/MCLK/A3 | 3 | P1.3 (I/O) | I: 0; O: 1 | 00 | 0 | N/A |
| | | UCB0SOMI/UCB0SCL | X | 01 | 0 | N/A |
| | | MCLK | 1 | 10 | 0 | N/A |
| | | A3 | X | X | 1 (x = 3) | N/A |
| P1.4/UCA0TXD/ UCA0SIMO/TA1.2/TCK/ A4 /VREF+ | 4 | P1.4 (I/O) | I: 0; O: 1 | 00 | 0 | Disabled |
| | | UCA0TXD/UCA0SIMO | X | 01 | 0 | Disabled |
| | | TA1.CCI2A | 0 | 10 | 0 | Disabled |
| | | TA1.2 | 1 | | | |
| | | A4, VREF+ | X | X | 1 (x = 4) | Disabled |
| | | JTAG TCK | X | X | X | TCK |
| P1.5/UCA0RXD/ UCA0SOMI/TA1.1/TMS/ A5 | 5 | P1.5 (I/O) | I: 0; O: 1 | 00 | 0 | Disabled |
| | | UCA0RXD/UCA0SOMI | X | 01 | 0 | Disabled |
| | | TA1.CCI1A | 0 | 10 | 0 | Disabled |
| | | TA1.1 | 1 | | | |
| | | A5 | X | X | 1 (x = 5) | Disabled |
| | | JTAG TMS | X | X | X | TMS |
| P1.6/UCA0CLK/ TA1CLK/TDI/TCLK/A6 | 6 | P1.6 (I/O) | I: 0; O: 1 | 00 | 0 | Disabled |
| | | UCA0CLK | X | 01 | | Disabled |
| | | TA1CLK | 0 | 10 | 0 | Disabled |
| | | A6 | X | X | 1 (x = 6) | Disabled |
| | | JTAG TDI/TCLK | X | X | X | TDI/TCLK |
| P1.7/UCA0STE/SMCLK/ TDO/A7 | 7 | P1.7 (I/O) | I: 0; O: 1 | 00 | 0 | Disabled |
| | | UCA0STE | X | 01 | 0 | Disabled |
| | | SMCLK | 1 | 10 | 0 | Disabled |
| | | A7 | X | X | 1 (x = 7) | Disabled |
| | | JTAG TDO | X | X | X | TDO |

(1) X = don't care
(2) Setting the ADCPCTLx bit in SYSCFG2 register disables both the output driver and input Schmitt trigger to prevent leakage when analog signals are applied.

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### 6.11.2 Port P2 (P2.0 to P2.2) Input/Output With Schmitt Trigger

Figure 6-2 shows the port diagram. Table 6-18 summarizes the selection of pin function.

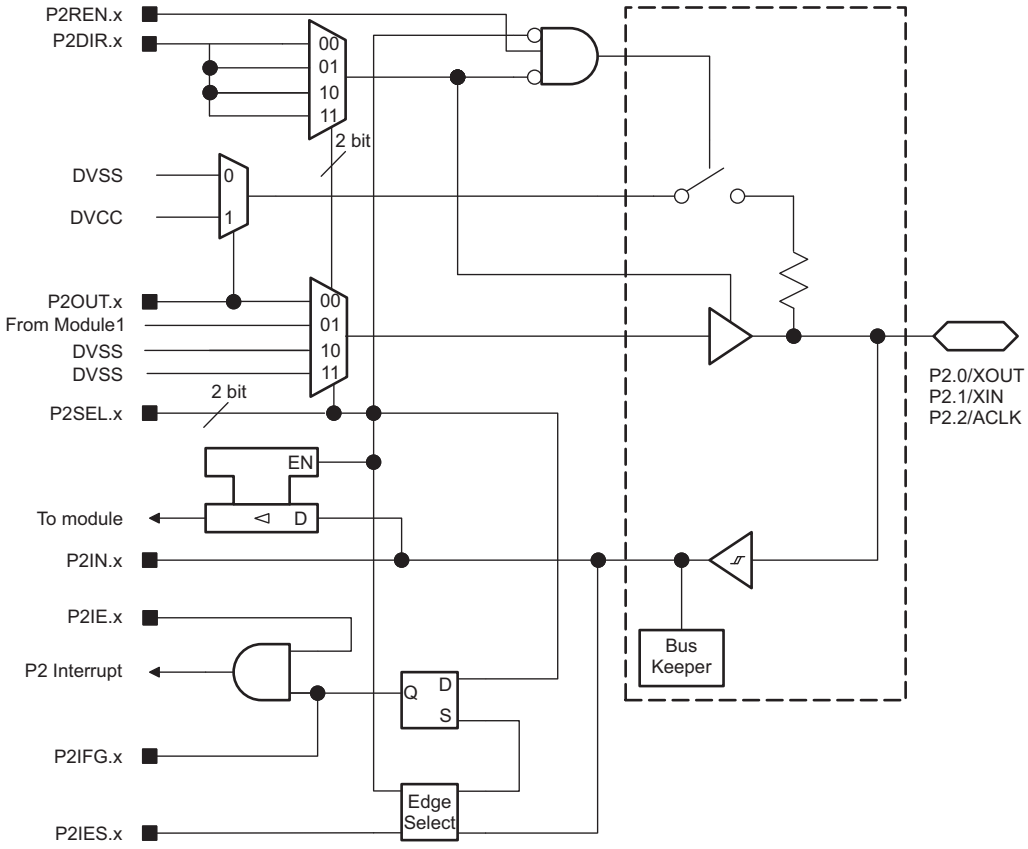


**Figure 6-2. Port P2 (P2.0 to P2.2) Input/Output With Schmitt Trigger**

**Table 6-18. Port P2 (P2.0 to P2.2) Pin Functions**

| PIN NAME (P2.x) | x | FUNCTION | CONTROL BITS AND SIGNALS(1) | |
|---|---|---|---|---|
| | | | P2DIR.x | P2SELx |
| P2.0/XOUT | 0 | P2.0 (I/O) | I: 0; O: 1 | 00 |
| | | XOUT | X | 01 |
| P2.1/XIN | 1 | P2.1 (I/O) | I: 0; O: 1 | 00 |
| | | XIN | X | 01 |
| P2.2/ACLK | 2 | P2.2 (I/O) | I: 0; O: 1 | 00 |
| | | ACLK | 1 | 10 |

(1) X = don't care


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### 6.11.3 Port P2 (P2.3 to P2.7) Input/Output With Schmitt Trigger

Figure 6-3 shows the port diagram. Table 6-19 summarizes the selection of pin function.

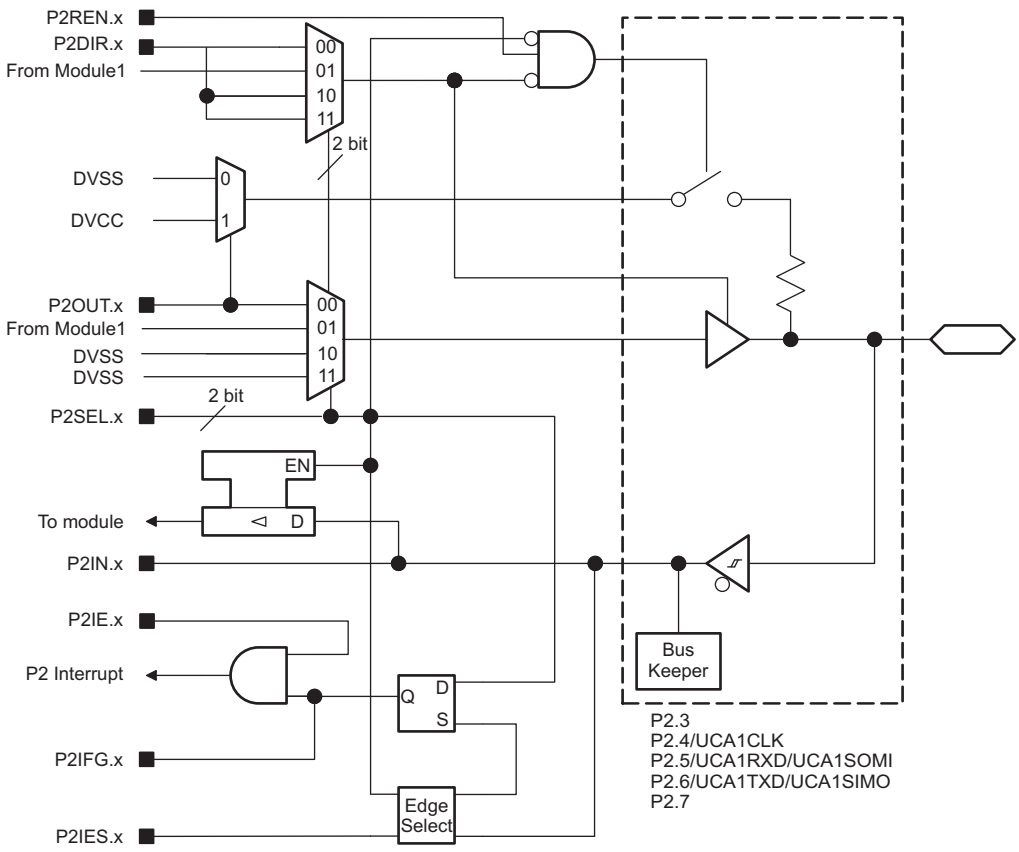


**Figure 6-3. Port P2 (P2.3 to P2.7) Input/Output With Schmitt Trigger**

**Table 6-19. Port P2 (P2.3 to P2.7) Pin Functions**

| PIN NAME (P2.x) | x | FUNCTION | CONTROL BITS AND SIGNALS(1) | | |
|---|---|---|---|---|---|
| | | | P2DIR.x | P2SELx | ANALOG FUNCTION |
| P2.3 | 3 | P2.3 (I/O) | I: 0; O: 1 | 00 | 0 |
| P2.4/UCA1CLK | 4 | P2.4 (I/O) | I: 0; O: 1 | 00 | 0 |
| | | UCA1CLK | X | 01 | 0 |
| P2.5/UCA1RXD/ UCA1SOMI | 5 | P2.5 (I/O) | I: 0; O: 1 | 00 | 0 |
| | | UCA1RXD/UCA1SOMI | X | 01 | 0 |
| P2.6/UCA1TXD/ UCA1SIMO | 6 | P2.6 (I/O) | I: 0; O: 1 | 00 | 0 |
| | | UCA1TXD/'UCA1SIMO | X | 01 | 0 |
| P2.7 | 7 | P2.7 (I/O) | I: 0; O: 1 | 0 | 0 |

(1) X = don't care


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### 6.11.4 Port P3 (P3.0 to P3.2) Input/Output With Schmitt Trigger

Figure 6-4 shows the port diagram. Table 6-20 summarizes the selection of pin function.

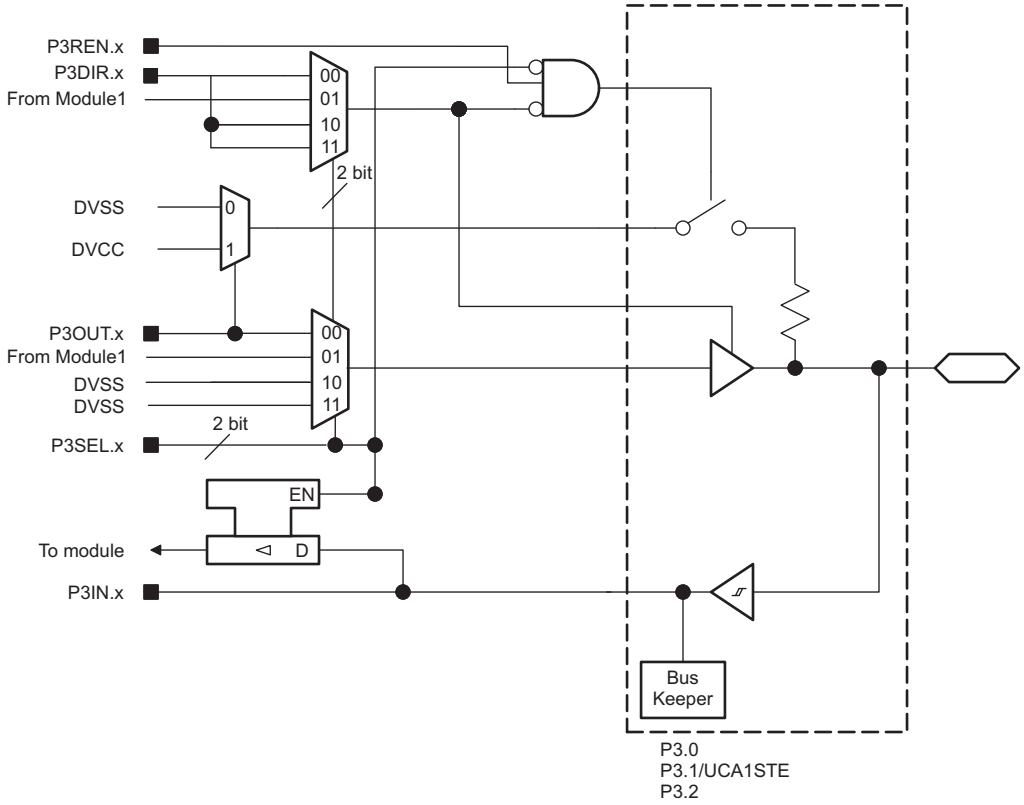


**Figure 6-4. Port P3 (P3.0 to P3.2) Input/Output With Schmitt Trigger**

**Table 6-20. Port P3 (P3.0 to P3.2) Pin Functions**

| PIN NAME (P3.x) | x | FUNCTION | CONTROL BITS AND SIGNALS(1) | |
|---|---|---|---|---|
| | | | P3DIR.x | P3SEL.x |
| P3.0 | 0 | P3.0 (I/O) | I: 0; O: 1 | 00 |
| P3.1/UCA1STE | 1 | P3.1 (I/O) | I: 0; O: 1 | 00 |
| | | UCA1STE | X | 01 |
| P3.2 | 2 | P3.2 (I/O) | I: 0; O: 1 | 00 |

(1) X = don't care

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## 6.12 Device Descriptors

Table 6-21 lists the Device IDs of the devices. Table 6-22 lists the contents of the device descriptor tag-length-value (TLV) structure for the devices.

**Table 6-21. Device IDs**

| DEVICE | DEVICE ID | |
|---|---|---|
| | 1A05h | 1A04h |
| MSP430FR2433 | 82h | 40h |

**Table 6-22. Device Descriptors**

| DESCRIPTION | | MSP430FR2433 | |
|---|---|---|---|
| | | ADDRESS | VALUE |
| Information Block | Info length | 1A00h | 06h |
| | CRC length | 1A01h | 06h |
| | CRC value(1) | 1A02h | Per unit |
| | | 1A03h | Per unit |
| | Device ID | 1A04h | See Table 6-21. |
| | | 1A05h | |
| | Hardware revision | 1A06h | Per unit |
| | Firmware revision | 1A07h | Per unit |
| Die Record | Die record tag | 1A08h | 08h |
| | Die record length | 1A09h | 0Ah |
| | Lot wafer ID | 1A0Ah | Per unit |
| | | 1A0Bh | Per unit |
| | | 1A0Ch | Per unit |
| | | 1A0Dh | Per unit |
| | Die X position | 1A0Eh | Per unit |
| | | 1A0Fh | Per unit |
| | Die Y position | 1A10h | Per unit |
| | | 1A11h | Per unit |
| | Test result | 1A12h | Per unit |
| | | 1A13h | Per unit |
| ADC Calibration | ADC calibration tag | 1A14h | Per unit |
| | ADC calibration length | 1A15h | Per unit |
| | ADC gain factor | 1A16h | Per unit |
| | | 1A17h | Per unit |
| | ADC offset | 1A18h | Per unit |
| | | 1A19h | Per unit |
| | ADC 1.5-V reference temperature 30°C | 1A1Ah | Per unit |
| | | 1A1Bh | Per unit |
| | ADC 1.5-V reference temperature 85°C | 1A1Ch | Per unit |
| | | 1A1Dh | Per unit |

(1) The CRC value covers the checksum from 0x1A04h to 0x1AF5h by applying the CRC-CCITT-16 polynomial of $x^{16} + x^{12} + x^5 + 1$.


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**Table 6-22. Device Descriptors (continued)**

| DESCRIPTION | | MSP430FR2433 | |
|---|---|---|---|
| | | ADDRESS | VALUE |
| Reference and DCO Calibration | Calibration tag | 1A1Eh | 12h |
| | Calibration length | 1A1Fh | 04h |
| | 1.5-V reference factor | 1A20h | Per unit |
| | | 1A21h | Per unit |
| | DCO tap setting for 16 MHz, temperature 30°C(2) | 1A22h | Per unit |
| | | 1A23h | Per unit |

(2) This value can be directly loaded into DCO bits in CSCTL0 registers to get accurate 16-MHz frequency at room temperature, especially when the MCU exits from LPM3 and below. TI suggests using the predivider to decrease the frequency if the temperature drift might result an overshoot beyond 16 MHz.

## 6.13 Memory

### *6.13.1 Memory Organization*

Table 6-23 summarizes the memory map of the device.

**Table 6-23. Memory Organization**

| | ACCESS | MSP430FR2433 |
|---|---|---|
| Memory (FRAM)<br>Main: interrupt vectors and signatures<br>Main: code memory | Read/Write<br>(Optional Write Protect)(1) | 15KB<br>FFFFh to FF80h<br>FFFFh to C400h |
| RAM | Read/Write | 4KB<br>2FFFh to 2000h |
| Information Memory (FRAM) | Read/Write<br>(Optional Write Protect)(2) | 512 bytes<br>19FFh to 1800h |
| Bootstrap loader (BSL1) Memory (ROM) | Read only | 2KB<br>17FFh to 1000h |
| Bootstrap loader (BSL2) Memory (ROM) | Read only | 1KB<br>FFFFFh to FFC00h |
| Peripherals | Read/Write | 4KB<br>0FFFh to 0000h |

(1) The Program FRAM can be write protected by setting the PFWP bit in the SYSCFG0 register. See the SYS chapter in the *MSP430FR4xx and MSP430FR2xx Family User's Guide* for more details.
(2) The Information FRAM can be write protected by setting the DFWP bit in the SYSCFG0 register. See the SYS chapter in the *MSP430FR4xx and MSP430FR2xx Family User's Guide* for more details.

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### 6.13.2 Peripheral File Map

Table 6-24 lists the available peripherals and the register base address for each. Table 6-25 to Table 6-44 list the registers and address offsets for each peripheral.

**Table 6-24. Peripherals Summary**

| MODULE NAME | BASE ADDRESS | SIZE |
|---|---|---|
| Special Functions (See Table 6-25) | 0100h | 0010h |
| PMM (See Table 6-26) | 0120h | 0020h |
| SYS (See Table 6-27) | 0140h | 0040h |
| CS (See Table 6-28) | 0180h | 0020h |
| FRAM (See Table 6-29) | 01A0h | 0010h |
| CRC (See Table 6-30) | 01C0h | 0008h |
| WDT (See Table 6-31) | 01CCh | 0002h |
| Port P1, P2 (See Table 6-32) | 0200h | 0020h |
| Port P3 (See Table 6-33) | 0220h | 0020h |
| RTC (See Table 6-34) | 0300h | 0010h |
| Timer0_A3 (See Table 6-35) | 0380h | 0030h |
| Timer1_A3 (See Table 6-36) | 03C0h | 0030h |
| Timer2_A2 (See Table 6-37) | 0400h | 0030h |
| Timer3_A2 (See Table 6-38) | 0440h | 0030h |
| MPY32 (See Table 6-39) | 04C0h | 0030h |
| eUSCI_A0 (See Table 6-40) | 0500h | 0020h |
| eUSCI_A1 (See Table 6-41) | 0520h | 0020h |
| eUSCI_B0 (See Table 6-42) | 0540h | 0030h |
| Backup Memory (See Table 6-43) | 0660h | 0020h |
| ADC (See Table 6-44) | 0700h | 0040h |

**Table 6-25. Special Function Registers (Base Address: 0100h)**

| REGISTER DESCRIPTION | ACRONYM | OFFSET |
|---|---|---|
| SFR interrupt enable | SFRIE1 | 00h |
| SFR interrupt flag | SFRIFG1 | 02h |
| SFR reset pin control | SFRRPCR | 04h |

**Table 6-26. PMM Registers (Base Address: 0120h)**

| REGISTER DESCRIPTION | ACRONYM | OFFSET |
|---|---|---|
| PMM control 0 | PMMCTL0 | 00h |
| PMM control 1 | PMMCTL1 | 02h |
| PMM control 2 | PMMCTL2 | 04h |
| PMM interrupt flags | PMMIFG | 0Ah |
| PM5 control 0 | PM5CTL0 | 10h |


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**Table 6-27. SYS Registers (Base Address: 0140h)**

| REGISTER DESCRIPTION | ACRONYM | OFFSET |
|---|---|---|
| System control | SYSCTL | 00h |
| Bootloader configuration area | SYSBSLC | 02h |
| JTAG mailbox control | SYSJMBC | 06h |
| JTAG mailbox input 0 | SYSJMBI0 | 08h |
| JTAG mailbox input 1 | SYSJMBI1 | 0Ah |
| JTAG mailbox output 0 | SYSJMBO0 | 0Ch |
| JTAG mailbox output 1 | SYSJMBO1 | 0Eh |
| Bus error vector generator | SYSBERRIV | 18h |
| User NMI vector generator | SYSUNIV | 1Ah |
| System NMI vector generator | SYSSNIV | 1Ch |
| Reset vector generator | SYSRSTIV | 1Eh |
| System configuration 0 | SYSCFG0 | 20h |
| System configuration 1 | SYSCFG1 | 22h |
| System configuration 2 | SYSCFG2 | 24h |

**Table 6-28. CS Registers (Base Address: 0180h)**

| REGISTER DESCRIPTION | ACRONYM | OFFSET |
|---|---|---|
| CS control 0 | CSCTL0 | 00h |
| CS control 1 | CSCTL1 | 02h |
| CS control 2 | CSCTL2 | 04h |
| CS control 3 | CSCTL3 | 06h |
| CS control 4 | CSCTL4 | 08h |
| CS control 5 | CSCTL5 | 0Ah |
| CS control 6 | CSCTL6 | 0Ch |
| CS control 7 | CSCTL7 | 0Eh |
| CS control 8 | CSCTL8 | 10h |

**Table 6-29. FRAM Registers (Base Address: 01A0h)**

| REGISTER DESCRIPTION | ACRONYM | OFFSET |
|---|---|---|
| FRAM control 0 | FRCTL0 | 00h |
| General control 0 | GCCTL0 | 04h |
| General control 1 | GCCTL1 | 06h |

**Table 6-30. CRC Registers (Base Address: 01C0h)**

| REGISTER DESCRIPTION | ACRONYM | OFFSET |
|---|---|---|
| CRC data input | CRC16DI | 00h |
| CRC data input reverse byte | CRCDIRB | 02h |
| CRC initialization and result | CRCINIRES | 04h |
| CRC result reverse byte | CRCRESR | 06h |

**Table 6-31. WDT Registers (Base Address: 01CCh)**

| REGISTER DESCRIPTION | ACRONYM | OFFSET |
|---|---|---|
| Watchdog timer control | WDTCTL | 00h |

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**Table 6-32. Port P1, P2 Registers (Base Address: 0200h)**

| REGISTER DESCRIPTION | ACRONYM | OFFSET |
|---|---|---|
| Port P1 input | P1IN | 00h |
| Port P1 output | P1OUT | 02h |
| Port P1 direction | P1DIR | 04h |
| Port P1 pulling enable | P1REN | 06h |
| Port P1 selection 0 | P1SEL0 | 0Ah |
| Port P1 selection 1 | P1SEL1 | 0Ch |
| Port P1 interrupt vector word | P1IV | 0Eh |
| Port P1 complement selection | P1SELC | 16h |
| Port P1 interrupt edge select | P1IES | 18h |
| Port P1 interrupt enable | P1IE | 1Ah |
| Port P1 interrupt flag | P1IFG | 1Ch |
| Port P2 input | P2IN | 01h |
| Port P2 output | P2OUT | 03h |
| Port P2 direction | P2DIR | 05h |
| Port P2 pulling enable | P2REN | 07h |
| Port P2 selection 0 | P2SEL0 | 0Bh |
| Port P2 selection 1 | P2SEL1 | 0Dh |
| Port P2 interrupt vector word | P2IV | 1Eh |
| Port P2 complement selection | P2SELC | 17h |
| Port P2 interrupt edge select | P2IES | 19h |
| Port P2 interrupt enable | P2IE | 1Bh |
| Port P2 interrupt flag | P2IFG | 1Dh |

**Table 6-33. Port P3 Registers (Base Address: 0220h)**

| REGISTER DESCRIPTION | ACRONYM | OFFSET |
|---|---|---|
| Port P3 input | P3IN | 00h |
| Port P3 output | P3OUT | 02h |
| Port P3 direction | P3DIR | 04h |
| Port P3 pulling enable | P3REN | 06h |
| Port P3 selection 0 | P3SEL0 | 0Ah |
| Port P3 selection 1 | P3SEL1 | 0 |
| Port P3 complement selection | P3SELC | 16h |

**Table 6-34. RTC Registers (Base Address: 0300h)**

| REGISTER DESCRIPTION | ACRONYM | OFFSET |
|---|---|---|
| RTC control | RTCCTL | 00h |
| RTC interrupt vector | RTCIV | 04h |
| RTC modulo | RTCMOD | 08h |
| RTC counter | RTCCNT | 0Ch |


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**Table 6-35. Timer0_A3 Registers (Base Address: 0380h)**

| REGISTER DESCRIPTION | ACRONYM | OFFSET |
|---|---|---|
| TA0 control | TA0CTL | 00h |
| Capture/compare control 0 | TA0CCTL0 | 02h |
| Capture/compare control 1 | TA0CCTL1 | 04h |
| Capture/compare control 2 | TA0CCTL2 | 06h |
| TA0 counter | TA0R | 10h |
| Capture/compare 0 | TA0CCR0 | 12h |
| Capture/compare 1 | TA0CCR1 | 14h |
| Capture/compare 2 | TA0CCR2 | 16h |
| TA0 expansion 0 | TA0EX0 | 20h |
| TA0 interrupt vector | TA0IV | 2Eh |

**Table 6-36. Timer1_A3 Registers (Base Address: 03C0h)**

| REGISTER DESCRIPTION | ACRONYM | OFFSET |
|---|---|---|
| TA1 control | TA1CTL | 00h |
| Capture/compare control 0 | TA1CCTL0 | 02h |
| Capture/compare control 1 | TA1CCTL1 | 04h |
| Capture/compare control 2 | TA1CCTL2 | 06h |
| TA1 counter | TA1R | 10h |
| Capture/compare 0 | TA1CCR0 | 12h |
| Capture/compare 1 | TA1CCR1 | 14h |
| Capture/compare 2 | TA1CCR2 | 16h |
| TA1 expansion 0 | TA1EX0 | 20h |
| TA1 interrupt vector | TA1IV | 2Eh |

**Table 6-37. Timer2_A2 Registers (Base Address: 0400h)**

| REGISTER DESCRIPTION | ACRONYM | OFFSET |
|---|---|---|
| TA2 control | TA2CTL | 00h |
| Capture/compare control 0 | TA2CCTL0 | 02h |
| Capture/compare control 1 | TA2CCTL1 | 04h |
| TA2 counter | TA2R | 10h |
| Capture/compare 0 | TA2CCR0 | 12h |
| Capture/compare 1 | TA2CCR1 | 14h |
| TA2 expansion 0 | TA2EX0 | 20h |
| TA2 interrupt vector | TA2IV | 2Eh |

**Table 6-38. Timer3_A2 Registers (Base Address: 0440h)**

| REGISTER DESCRIPTION | ACRONYM | OFFSET |
|---|---|---|
| TA3 control | TA3CTL | 00h |
| Capture/compare control 0 | TA3CCTL0 | 02h |
| Capture/compare control 1 | TA3CCTL1 | 04h |
| TA3 counter | TA3R | 10h |
| Capture/compare 0 | TA3CCR0 | 12h |
| Capture/compare 1 | TA3CCR1 | 14h |
| TA3 expansion 0 | TA3EX0 | 20h |
| TA3 interrupt vector | TA3IV | 2Eh |

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**Table 6-39. MPY32 Registers (Base Address: 04C0h)**

| REGISTER DESCRIPTION | ACRONYM | OFFSET |
|---|---|---|
| 16-bit operand 1 – multiply | MPY | 00h |
| 16-bit operand 1 – signed multiply | MPYS | 02h |
| 16-bit operand 1 – multiply accumulate | MAC | 04h |
| 16-bit operand 1 – signed multiply accumulate | MACS | 06h |
| 16-bit operand 2 | OP2 | 08h |
| 16 × 16 result low word | RESLO | 0Ah |
| 16 × 16 result high word | RESHI | 0Ch |
| 16 × 16 sum extension | SUMEXT | 0Eh |
| 32-bit operand 1 – multiply low word | MPY32L | 10h |
| 32-bit operand 1 – multiply high word | MPY32H | 12h |
| 32-bit operand 1 – signed multiply low word | MPYS32L | 14h |
| 32-bit operand 1 – signed multiply high word | MPYS32H | 16h |
| 32-bit operand 1 – multiply accumulate low word | MAC32L | 18h |
| 32-bit operand 1 – multiply accumulate high word | MAC32H | 1Ah |
| 32-bit operand 1 – signed multiply accumulate low word | MACS32L | 1Ch |
| 32-bit operand 1 – signed multiply accumulate high word | MACS32H | 1Eh |
| 32-bit operand 2 – low word | OP2L | 20h |
| 32-bit operand 2 – high word | OP2H | 22h |
| 32 × 32 result 0 – least significant word | RES0 | 24h |
| 32 × 32 result 1 | RES1 | 26h |
| 32 × 32 result 2 | RES2 | 28h |
| 32 × 32 result 3 – most significant word | RES3 | 2Ah |
| MPY32 control 0 | MPY32CTL0 | 2Ch |

**Table 6-40. eUSCI_A0 Registers (Base Address: 0500h)**

| REGISTER DESCRIPTION | ACRONYM | OFFSET |
|---|---|---|
| eUSCI_A control word 0 | UCA0CTLW0 | 00h |
| eUSCI_A control word 1 | UCA0CTLW1 | 02h |
| eUSCI_A control rate 0 | UCA0BR0 | 06h |
| eUSCI_A control rate 1 | UCA0BR1 | 07h |
| eUSCI_A modulation control | UCA0MCTLW | 08h |
| eUSCI_A status | UCA0STAT | 0Ah |
| eUSCI_A receive buffer | UCA0RXBUF | 0Ch |
| eUSCI_A transmit buffer | UCA0TXBUF | 0Eh |
| eUSCI_A LIN control | UCA0ABCTL | 10h |
| eUSCI_A IrDA transmit control | lUCA0IRTCTL | 12h |
| eUSCI_A IrDA receive control | lUCA0IRRCTL | 13h |
| eUSCI_A interrupt enable | UCA0IE | 1Ah |
| eUSCI_A interrupt flags | UCA0IFG | 1Ch |
| eUSCI_A interrupt vector word | UCA0IV | 1Eh |


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**Table 6-41. eUSCI_A1 Registers (Base Address: 0520h)**

| REGISTER DESCRIPTION | ACRONYM | OFFSET |
|---|---|---|
| eUSCI_A control word 0 | UCA1CTLW0 | 00h |
| eUSCI_A control word 1 | UCA1CTLW1 | 02h |
| eUSCI_A control rate 0 | UCA1BR0 | 06h |
| eUSCI_A control rate 1 | UCA1BR1 | 07h |
| eUSCI_A modulation control | UCA1MCTLW | 08h |
| eUSCI_A status | UCA1STAT | 0Ah |
| eUSCI_A receive buffer | UCA1RXBUF | 0Ch |
| eUSCI_A transmit buffer | UCA1TXBUF | 0Eh |
| eUSCI_A LIN control | UCA1ABCTL | 10h |
| eUSCI_A IrDA transmit control | lUCA1IRTCTL | 12h |
| eUSCI_A IrDA receive control | lUCA1IRRCTL | 13h |
| eUSCI_A interrupt enable | UCA1IE | 1Ah |
| eUSCI_A interrupt flags | UCA1IFG | 1Ch |
| eUSCI_A interrupt vector word | UCA1IV | 1Eh |

**Table 6-42. eUSCI_B0 Registers (Base Address: 0540h)**

| REGISTER DESCRIPTION | ACRONYM | OFFSET |
|---|---|---|
| eUSCI_B control word 0 | UCB0CTLW0 | 00h |
| eUSCI_B control word 1 | UCB0CTLW1 | 02h |
| eUSCI_B bit rate 0 | UCB0BR0 | 06h |
| eUSCI_B bit rate 1 | UCB0BR1 | 07h |
| eUSCI_B status word | UCB0STATW | 08h |
| eUSCI_B byte counter threshold | UCB0TBCNT | 0Ah |
| eUSCI_B receive buffer | UCB0RXBUF | 0Ch |
| eUSCI_B transmit buffer | UCB0TXBUF | 0Eh |
| eUSCI_B I2C own address 0 | UCB0I2COA0 | 14h |
| eUSCI_B I2C own address 1 | UCB0I2COA1 | 16h |
| eUSCI_B I2C own address 2 | UCB0I2COA2 | 18h |
| eUSCI_B I2C own address 3 | UCB0I2COA3 | 1Ah |
| eUSCI_B receive address | UCB0ADDRX | 1Ch |
| eUSCI_B address mask | UCB0ADDMASK | 1Eh |
| eUSCI_B I2C slave address | UCB0I2CSA | 20h |
| eUSCI_B interrupt enable | UCB0IE | 2Ah |
| eUSCI_B interrupt flags | UCB0IFG | 2Ch |
| eUSCI_B interrupt vector word | UCB0IV | 2Eh |

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**Table 6-43. Backup Memory Registers (Base Address: 0660h)**

| REGISTER DESCRIPTION | ACRONYM | OFFSET |
|---|---|---|
| Backup memory 0 | BAKMEM0 | 00h |
| Backup memory 1 | BAKMEM1 | 02h |
| Backup memory 2 | BAKMEM2 | 04h |
| Backup memory 3 | BAKMEM3 | 06h |
| Backup memory 4 | BAKMEM4 | 08h |
| Backup memory 5 | BAKMEM5 | 0Ah |
| Backup memory 6 | BAKMEM6 | 0Ch |
| Backup memory 7 | BAKMEM7 | 0Eh |
| Backup memory 8 | BAKMEM8 | 10h |
| Backup memory 9 | BAKMEM9 | 12h |
| Backup memory 10 | BAKMEM10 | 14h |
| Backup memory 11 | BAKMEM11 | 16h |
| Backup memory 12 | BAKMEM12 | 18h |
| Backup memory 13 | BAKMEM13 | 1Ah |
| Backup memory 14 | BAKMEM14 | 1Ch |
| Backup memory 15 | BAKMEM15 | 1Eh |

**Table 6-44. ADC Registers (Base Address: 0700h)**

| REGISTER DESCRIPTION | ACRONYM | OFFSET |
|---|---|---|
| ADC control 0 | ADCCTL0 | 00h |
| ADC control 1 | ADCCTL1 | 02h |
| ADC control 2 | ADCCTL2 | 04h |
| ADC window comparator low threshold | ADCLO | 06h |
| ADC window comparator high threshold | ADCHI | 08h |
| ADC memory control 0 | ADCMCTL0 | 0Ah |
| ADC conversion memory | ADCMEM0 | 12h |
| ADC interrupt enable | ADCIE | 1Ah |
| ADC interrupt flags | ADCIFG | 1Ch |
| ADC interrupt vector word | ADCIV | 1Eh |


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## 6.14 Identification

### 6.14.1 Revision Identification

The device revision information is included as part of the top-side marking on the device package. The device-specific errata sheet describes these markings (see 8.4).

The hardware revision is also stored in the Device Descriptor structure in the Information Block section. For details on this value, see the Hardware Revision entries in Table 6-22.

### 6.14.2 Device Identification

The device type can be identified from the top-side marking on the device package. The device-specific errata sheet describes these markings (see 8.4).

A device identification value is also stored in the Device Descriptor structure in the Information Block section. For details on this value, see the Device ID entries in Table 6-22.

### 6.14.3 JTAG Identification

Programming through the JTAG interface, including reading and identifying the JTAG ID, is described in *MSP430 Programming With the JTAG Interface*.

# 7 Applications, Implementation, and Layout

**NOTE**

Information in the following Applications section is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

## 7.1 Device Connection and Layout Fundamentals

This section discusses the recommended guidelines when designing with the MSP430 devices. These guidelines are to make sure that the device has proper connections for powering, programming, debugging, and optimum analog performance.

### *7.1.1 Power Supply Decoupling and Bulk Capacitors*

TI recommends connecting a combination of a 10-µF and a 100-nF low-ESR ceramic decoupling capacitor to the DVCC and DVSS pins (see Figure 7-1). Higher-value capacitors may be used but can impact supply rail ramp-up time. Decoupling capacitors must be placed as close as possible to the pins that they decouple (within a few millimeters). Additionally, TI recommends separated grounds with a single-point connection for better noise isolation from digital-to-analog circuits on the board and to achieve high analog accuracy.

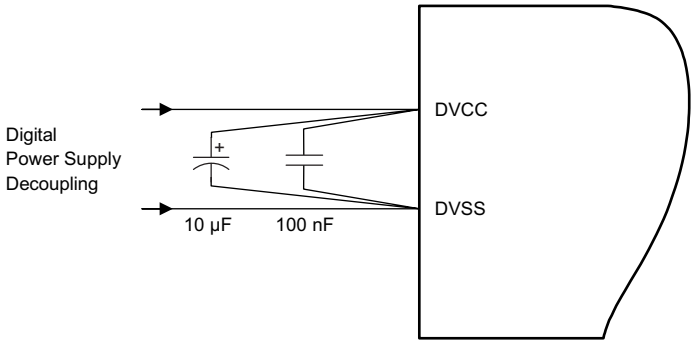


**Figure 7-1. Power Supply Decoupling**

### *7.1.2 External Oscillator*

This device supports only a low-frequency crystal (32 kHz) on the XIN and XOUT pins. External bypass capacitors for the crystal oscillator pins are required.

It is also possible to apply digital clock signals to the XIN input pin that meet the specifications of the respective oscillator if the appropriate XT1BYPASS mode is selected. In this case, the associated XOUT pin can be used for other purposes. If the XIN and XOUT pins are not used, they must be terminated according to Section 4.6.

Figure 7-2 shows a typical connection diagram.

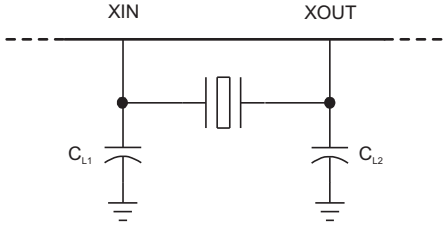


**Figure 7-2. Typical Crystal Connection**


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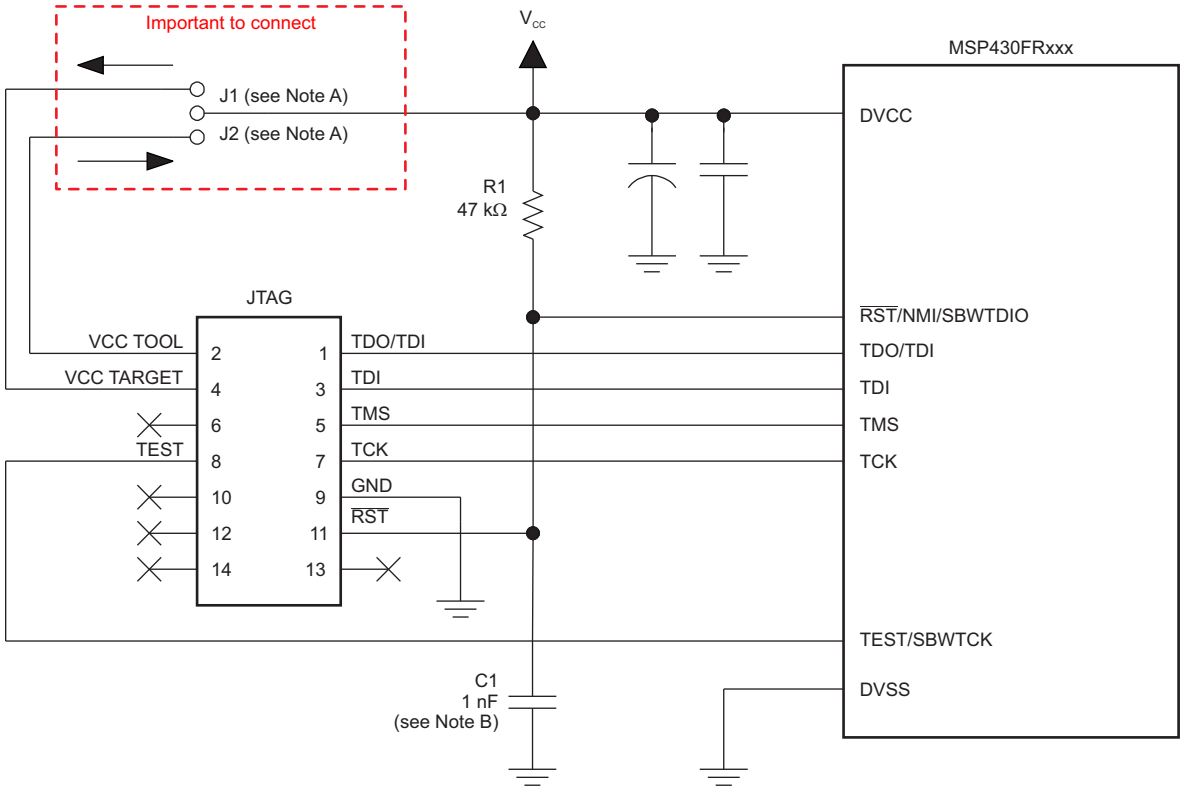
See *MSP430 32-kHz Crystal Oscillators* for more information on selecting, testing, and designing a crystal oscillator with the MSP430 devices.

### 7.1.3 JTAG

With the proper connections, the debugger and a hardware JTAG interface (such as the MSP-FET or MSP-FET430UIF) can be used to program and debug code on the target board. In addition, the connections also support the MSP-GANG production programmers, thus providing an easy way to program prototype boards, if desired. Figure 7-3 shows the connections between the 14-pin JTAG connector and the target device required to support in-system programming and debugging for 4-wire JTAG communication. Figure 7-4 shows the connections for 2-wire JTAG mode (Spy-Bi-Wire).

The connections for the MSP-FET and MSP-FET430UIF interface modules and the MSP-GANG are identical. Both can supply $V_{CC}$ to the target board (through pin 2). In addition, the MSP-FET and MSP-FET430UIF interface modules and MSP-GANG have a $V_{CC}$ sense feature that, if used, requires an alternate connection (pin 4 instead of pin 2). The $V_{CC}$ sense feature detects the local $V_{CC}$ present on the target board (that is, a battery or other local power supply) and adjusts the output signals accordingly. Figure 7-3 and Figure 7-4 show a jumper block that supports both scenarios of supplying $V_{CC}$ to the target board. If this flexibility is not required, the desired $V_{CC}$ connections may be hard-wired to eliminate the jumper block. Pins 2 and 4 must not be connected at the same time.

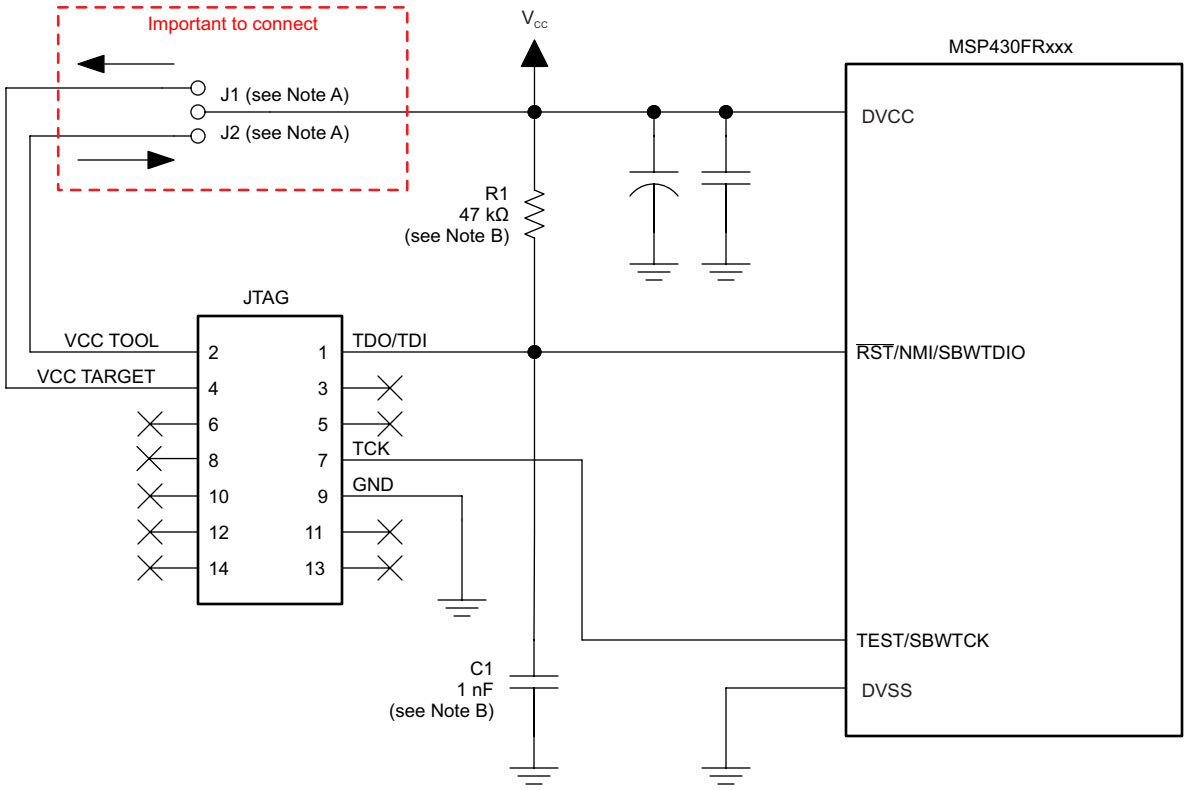
For additional design information regarding the JTAG interface, see the *MSP430 Hardware Tools User's Guide*.




A. If a local target power supply is used, make connection J1. If power from the debug or programming adapter is used, make connection J2.

B. The upper limit for C1 is 1.1 nF when using current TI tools.

**Figure 7-3. Signal Connections for 4-Wire JTAG Communication**




A. Make connection J1 if a local target power supply is used, or make connection J2 if the target is powered from the debug or programming adapter.

B. The device $\overline{\text{RST}}$/NMI/SBWTDIO pin is used in 2-wire mode for bidirectional communication with the device during JTAG access, and any capacitance that is attached to this signal may affect the ability to establish a connection with the device. The upper limit for C1 is 1.1 nF when using current TI tools.

**Figure 7-4. Signal Connections for 2-Wire JTAG Communication (Spy-Bi-Wire)**

### 7.1.4 Reset

The reset pin can be configured as a reset function (default) or as an NMI function in the Special Function Register (SFR), SFRRPCR.

In reset mode, the $\overline{\text{RST}}$/NMI pin is active low, and a pulse applied to this pin that meets the reset timing specifications generates a BOR-type device reset.

Setting SYSNMI causes the $\overline{\text{RST}}$/NMI pin to be configured as an external NMI source. The external NMI is edge sensitive, and its edge is selectable by SYSNMIIES. Setting the NMIIE enables the interrupt of the external NMI. When an external NMI event occurs, the NMIIFG is set.

The $\overline{\text{RST}}$/NMI pin can have either a pullup or pulldown that is enabled or not. SYSRSTUP selects either pullup or pulldown, and SYSRSTRE causes the pullup (default) or pulldown to be enabled (default) or not. If the $\overline{\text{RST}}$/NMI pin is unused, it is required either to select and enable the internal pullup or to connect an external 47-kΩ pullup resistor to the $\overline{\text{RST}}$/NMI pin with a 1.1-nF pulldown capacitor. The pulldown capacitor should not exceed 1.1 nF when using devices with Spy-Bi-Wire interface in Spy-Bi-Wire mode or in 4-wire JTAG mode with TI tools like FET interfaces or GANG programmers.

See the *MSP430FR4xx and MSP430FR2xx Family User's Guide* for more information on the referenced control registers and bits.

### 7.1.5 Unused Pins

For details on the connection of unused pins, see Section 4.6.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### 7.1.6 General Layout Recommendations

- Proper grounding and short traces for external crystal to reduce parasitic capacitance. For recommended layout guidelines, see *MSP430 32-kHz Crystal Oscillators*.
- Proper bypass capacitors on DVCC and reference pins, if used.
- Avoid routing any high-frequency signal close to an analog signal line. For example, keep digital switching signals such as PWM or JTAG signals away from the oscillator circuit and ADC signals.
- Proper ESD level protection should be considered to protect the device from unintended high-voltage electrostatic discharge. For guidelines see *MSP430 System-Level ESD Considerations*.

### 7.1.7 Do's and Don'ts

During power up, power down, and device operation, DVCC must not exceed the limits specified in Section 5.1. Exceeding the specified limits may cause malfunction of the device including erroneous writes to RAM and FRAM.

## 7.2 Peripheral- and Interface-Specific Design Information

### 7.2.1 ADC Peripheral

#### 7.2.1.1 Partial Schematic

Figure 7-5 shows the recommended decoupling circuit when an external voltage reference is used.

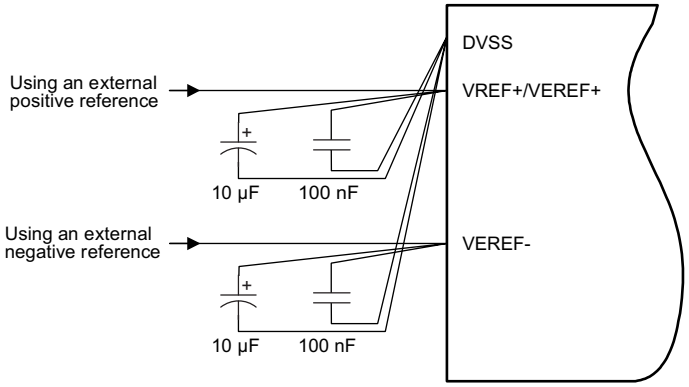


**Figure 7-5. ADC Grounding and Noise Considerations**

#### 7.2.1.2 Design Requirements

As with any high-resolution ADC, appropriate PCB layout and grounding techniques must be followed to eliminate ground loops, unwanted parasitic effects, and noise.

Ground loops are formed when return current from the ADC flows through paths that are common with other analog or digital circuitry. If care is not taken, this current can generate small unwanted offset voltages that can add to or subtract from the reference or input voltages of the ADC. The general guidelines in Section 7.1.1 combined with the connections shown in Figure 7-5 prevent this.

Quickly switching digital signals and noisy power supply lines can corrupt the conversion results, so keep the ADC input trace shielded from those digital and power supply lines. Putting the MCU in low-power mode during the ADC conversion improves the ADC performance in a noisy environment. If the device includes the analog power pair inputs (AVCC and AVSS), TI recommends a noise-free design using separate analog and digital ground planes with a single-point connection to achieve high accuracy.

Figure 7-5 shows the recommended decoupling circuit when an external voltage reference is used. The internal reference module has a maximum drive current as described in the sections *ADC Pin Enable* and *1.2-V Reference Settings* of the *MSP430FR4xx and MSP430FR2xx Family User's Guide*.

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The reference voltage must be a stable voltage for accurate measurements. The capacitor values that are selected in the general guidelines filter out the high- and low-frequency ripple before the reference voltage enters the device. In this case, the 10-µF capacitor buffers the reference pin and filters any low-frequency ripple. A bypass capacitor of 100 nF filters out any high-frequency noise.

#### 7.2.1.3 Layout Guidelines

Components that are shown in the partial schematic (see Figure 7-5) should be placed as close as possible to the respective device pins to avoid long traces, because they add additional parasitic capacitance, inductance, and resistance on the signal.

Avoid routing analog input signals close to a high-frequency pin (for example, a high-frequency PWM), because the high-frequency switching can be coupled into the analog signal.


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# 8 デバイスおよびドキュメントのサポート

## 8.1 使い始めと次の手順

MSP　低消費電力マイクロコントローラ、および開発に役立つツールやライブラリの詳細については、「MSP430™ 超低消費電力センシング/測定マイコン」ページを参照してください。

## 8.2 デバイスの項目表記

製品開発サイクルの段階を示すために、TIではMSP　MCUデバイスのすべての型番に接頭辞が割り当てられています。MSP MCU商用ファミリの各番号には、MSP、XMSのいずれかの接頭辞があります。これらの接頭辞は、製品開発の進展段階を表します。段階には、エンジニアリング・プロトタイプ(XMS)から、完全認定済みの量産デバイス(MSP)までがあります。

**XMS** - 実験段階のデバイスで、最終的なデバイスの電気的仕様を表しているとは限りません。

**MSP** - 完全に認定済みの量産版デバイスです。

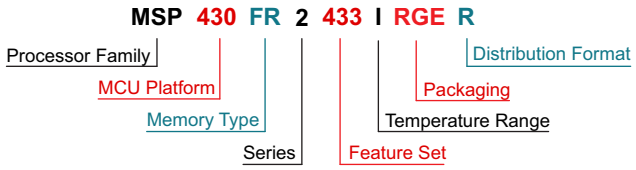
XMSデバイスは、次の免責事項付きで出荷されます。

「開発中の製品は、社内での評価用です。」

MSPデバイスの特性は完全に明確化されており、デバイスの品質と信頼性が十分に示されています。TIの標準保証が適用されます。

プロトタイプ・デバイス(XMS)は標準の量産デバイスよりも故障率が高いことが予想されます。これらのデバイスは、予測される最終使用時の故障率が未定義であるため、TIはそれらのデバイスを量産システムで使用しないよう推奨しています。認定された量産デバイスのみを使用する必要があります。

TIデバイスの項目表記には、デバイス・ファミリ名の接尾辞も含まれます。この接尾辞は、温度範囲、パッケージ・タイプ、配布形式を示しています。デバイス名の各部の読み方を図 8-1に示します。




| | | |
|---|---|---|
| **Processor Family** | MSP = Mixed-Signal Processor<br>XMS = Experimental Silicon | |
| **MCU Platform** | 430 = MSP430 16-bit low-power platform | |
| **Memory Type** | FR = FRAM | |
| **Series** | 2 = Up to 16 MHz without LCD | |
| **Feature Set** | **First and Second Digits:**<br>**ADC Channels / eUSCIs / 16-bit Timers / I/Os**<br>43 = Up to 8 / 3 / 4 / Up to 19 | **Third Digit:**<br>**FRAM (KB) / SRAM (KB)**<br>3 = 16 / 4 |
| **Temperature Range** | I = –40°C to 85°C | |
| **Packaging** | www.ti.com/packaging | |
| **Distribution Format** | T = Small reel<br>R = Large reel<br>No Marking = Tube or tray | |

**図 8-1. デバイスの項目表記**

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## 8.3 ツールとソフトウェア

すべてのMSPマイクロコントローラは、広範なソフトウェアおよびハードウェア開発ツールによりサポートされています。ツールは、TIおよびさまざまなサードパーティーから入手できます。すべてのツールの一覧は、『低消費電力MCU用の開発キットとソフトウェア』で参照できます。

MSP430FR211xマイクロコントローラのデバッグ機能の一覧を、表 8-1に示します。利用可能な機能の詳細については、*『Code Composer Studio™ v5.2 ユーザーズ・ガイド MSP430™ 版ユーザーズ・ガイド』*を参照してください。

**表 8-1. ハードウェアのデバッグ機能**

| MSP430のアーキテクチャ | 4線式 JTAG | 2線式 JTAG | ブレーク・ポイント (N) | 範囲ブレーク・ポイント | クロック制御 | 状態シーケンサ | トレース・バッファ | LPMx.5デバッグ・サポート | EEM のバージョン |
|---|---|---|---|---|---|---|---|---|---|
| MSP430Xv2 | ○ | ○ | 3 | ○ | ○ | × | × | × | S |

設計キットと評価基板

MSP-FET + MSP-TS430RGE24A 評価基板のバンドル

MSP-FETは強力なフラッシュ・エミュレーション・ツールで、MSP430マイクロコントローラによるアプリケーション開発をすぐに開始できます。MSP-FETはUSBインターフェイスを備えており、これによりJTAGインターフェイスまたはピン数を低減したSpy Bi-Wire (2線式JTAG)プロトコルを使用して、MSP430をインシステムでプログラミングおよびデバッグできます。同梱のMSP-FET開発ツールは、すべてのMSP430デバイスによる開発をサポートしています。

ソフトウェア

MSP430Wareソフトウェア

MSP430Wareは、MSP430コードの効果的な作成・構築に役立つ設計リソース集です。MSP430Wareは、MSP430ドライバ・ライブラリやUSBといったデバイス/ペリフェラル別ライブラリからグラフィックス・ライブラリや静電容量式タッチ・ライブラリといった用途別ライブラリまで、高度に抽象化されたソフトウェア・ライブラリを幅広く取り揃えています。特にMSP430ドライバ・ライブラリは重要なライブラリであり、これによりソフトウェア開発者は便利なAPIを活用して下位の複雑なハードウェア・ペリフェラルを制御でき、最終的なコードは読みやすく、保守しやすいものになります。

MSP430FR243x/MSP430FR253x/MSP430FR263xのサンプル・コード

すべての MSP デバイス用に、内蔵の各ペリフェラルをさまざまな用途のニーズに合わせて構成するための C コード・サンプルが用意されています。

MSP ドライバ・ライブラリ

MSPドライバ・ライブラリの抽象化されたAPIには、使いやすい関数呼び出しが含まれているため、MSP430ハードウェアのビットやバイトを直接操作する煩雑さから解放されます。使いやすいAPIガイドにより包括的な技術資料が参照でき、それぞれの関数呼び出しと、認識されるパラメータの詳細が記載されています。開発者は、ドライバ・ライブラリの関数を使用して、最小限のオーバーヘッドで完全なプロジェクトを作成できます。

MSP EnergyTrace™ テクノロジ

MSP430 マイコン向け EnergyTrace テクノロジはエネルギー・ベースのコード分析ツールで、アプリケーションのエネルギー・プロファイルの測定と表示を行うとともに、消費電力の大幅な低減のための最適化も可能です。

ULP (超低消費電力) Advisor

ULP Advisor™ソフトウェアは、MSPおよびMSP432マイクロコントローラの超低消費電力機能を十分に活用できる、最も効率的なコードを開発者が作成できるよう手引きするツールです。ULP Advisorはマイクロコントローラに熟練した開発者と、新しい開発者の両方を対象としており、包括的なULPチェックリストを使用してコードをチェックし、アプリケーションのエネルギー消費を最小化するため役立ちます。ビルド時に、消費電力低減のためさらに最適化が可能なコードの部分を明らかにするため通知と注釈を出力します。


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### IEC60730 ソフトウェア・パッケージ

IEC60730 MSP430ソフトウェア・パッケージは、クラスBまでの製品について、お客様がIEC 60730-1:2010 (家庭および同様な用途に使用される自動電気制御 – 第1部: 一般的な要件)に準拠するため役立つよう開発されています。この分類には家電機器、アーク検出器、電力コンバータ、電動工具、電気自転車、その他多くの製品が含まれます。IEC60730 MSP430ソフトウェア・パッケージは、MSP430で実行するお客様のアプリケーションに組み込むことができるため、消費者向けデバイスがIEC 60730-1:2010クラスBの機能安全性に準拠していることの認定作業を簡素化できます。

### MSP 用の固定小数点算術ライブラリ

MSP IQmath および Qmath ライブラリは、C プログラマが浮動小数点アルゴリズムを MSP430 および MSP432 デバイスの固定小数点コードにシームレスに移植するための高度に最適化された高精度算術関数のコレクションです。これらのルーチンは通常、最適な実行速度、高精度、超低消費電力が重視される、演算集中型のリアルタイム・アプリケーションで使用されます。IQmathライブラリとQmathライブラリを使用すると、浮動小数点演算を使用して記述した同等のコードに比べて、実行速度を大幅に高速化するとともに、消費電力の大幅な削減が可能です。

### MSP430用の浮動小数点算術ライブラリ

低消費電力で低コストのマイクロコントローラ分野にさらなる革新を引き起こすため、TIはMSPMATHLIBを提供します。この浮動小数点算術ライブラリは、弊社デバイスのインテリジェントなペリフェラルを活用し、標準のMSP430算術関数よりも最高で26倍も高速なスカラー関数です。Mathlibは、設計へ簡単に組み入れることができます。このライブラリは無償で、Code Composer Studio IDEとIAR Embedded Workbench IDEの両方に組み込まれています。

開発ツール

### Code Composer Studio™: MSPマイクロコントローラ用の統合開発環境

Code Composer Studio (CCS)は、すべてのMSPマイクロコントローラ・デバイスをサポートする統合開発環境(IDE)です。CCSは、組み込みアプリケーションの開発とデバッグに使用される、組み込み用ソフトウェア・ユーティリティのスイートです。最適化C/C++コンパイラ、ソース・コード・エディタ、プロジェクト・ビルド環境、デバッガ、プロファイラなど、多数の機能が含まれています。

### コマンドライン・プログラマ

MSP Flasher は、FET プログラマまたは eZ430 を経由し、JTAG または Spy-Bi-Wire (SBW) 通信を使用して MSP マイクロコントローラをプログラムするための、オープン・ソースでシェル・ベースのインターフェイスです。MSP Flasher は、IDE を使用せずにバイナリ・ファイル (.txt または .hex) を MSP マイクロコントローラへ直接ダウンロードできます。

### MSP MCU プログラマおよびデバッガ

MSP-FET は、MSP 低消費電力マイクロコントローラ (MCU) でのアプリケーション開発をすばやく開始できる強力なエミュレーション開発ツールです (デバッグ・プローブとも呼ばれます)。MCUのソフトウェアを作成する場合は通常、結果として得られたバイナリ・プログラムをMSPデバイスにダウンロードし、検証とデバッグを行う必要があります。MSP-FETは、ホスト・コンピュータとターゲットMSPの間で、デバッグ通信経路を提供します。さらに MSP-FET は、コンピュータの USB インターフェイスと MSP UART の間のバックチャネル UART 接続にも対応します。これにより MSP のプログラマは、コンピュータ上で動作している端末ソフトウェアと MSP との間でシリアル通信を簡単に行うことができます。

### MSP-GANG量産プログラマ

MSP Gang Programmer は、8 つまでの同一の MSP430 または MSP432 のフラッシュまたは FRAM デバイスを同時にプログラムできます。MSP Gang Programmerは、標準のRS-232またはUSB接続を使用してホストPCに接続でき、柔軟なプログラミング・オプションにより、プロセスを完全にカスタマイズ可能です。MSP Gang Programmer には、Gang Splitter と呼ばれる拡張ボードが付属しており、MSP Gang Programmer と複数のターゲット・デバイスとの間で相互接続機能を実装します。

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## 8.4 ドキュメントのサポート

以下のドキュメントは MSP430FR2433 MCU について記載したものです。これらのドキュメントのコピーは、www.ti.comで入手できます。

ドキュメントの更新通知を受け取る方法

ドキュメント更新の通知を、シリコンの正誤表も含めて受け取るには、ti.comでお使いのデバイスの製品フォルダへ移動します (例: MSP430FR2433)。右上の隅にある「通知を受け取る」ボタンをクリックします。これによって登録が行われ、変更された製品情報の概要を毎週受け取ることができます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

正誤表

『MSP430FR2433正誤表』

機能仕様に対する既知の例外が記載されています。

ユーザー・ガイド

『MSP430FR4xxおよびMSP430FR2xxファミリ ユーザー・ガイド』

このデバイス・ファミリで利用可能なモジュールとペリフェラルについての詳細情報です。

『MSP430 FRAMデバイス・ブートローダ(BSL) ユーザー・ガイド』

ブートローダ(BSL)はMSP430 MCUプロジェクトの開発および更新時にメモリをプログラムするための手段を提供します。シリアル・プロトコルを使用してコマンドを送信するユーティリティにより、この機能をアクティブにできます。BSLにより、ユーザーはMSP430 MCUの動作を制御し、パーソナル・コンピュータや他のデバイスを使用してデータを交換できます。

『MSP430ハードウェア・ツール ユーザー・ガイド』

このマニュアルには、TI MSP-FET430フラッシュ・エミュレーション・ツール(FET)のハードウェアについて解説されています。FETは、MSP430超低消費電力マイクロコントローラ用のプログラム開発ツールです。

アプリケーション・レポート

『MSP430 FRAMテクノロジ - ハウツーとベスト・プラクティス』

FRAMは不揮発性メモリ・テクノロジで、SRAMと同様に動作し、多くの新しいアプリケーションを可能にすると同時に、ファームウェアの設計方法に変革をもたらすものです。このアプリケーション・レポートでは、組み込みソフトウェア開発の観点から、MSP430のFRAMテクノロジを使用する方法と、そのベスト・プラクティスについて概説しています。特定用途向けのコード、定数、データ容量の制限、FRAMの使用に従って、アプリケーションのエネルギー消費を最適化するようメモリ・レイアウトを実装する方法について解説します。

『MSP430FR4xxおよびMSP430FR2xxファミリでのVLO較正』

MSP430FR4xxおよびMSP430FR2xx (FR4xx/FR2xx)ファミリのマイクロコントローラ(MCU)には、いくつかの高速高精度クロックや、いくつかの低消費電力でシステム・コストの低いクロックを含めて、各種のクロック・ソースが用意されています。ユーザーは、性能、消費電力、システム・コストを比較して、最良のものを選択できます。オンチップの超低周波数発振器(VLO)は、FR4xx/FR2xxファミリのMCUに内蔵されている、標準周波数10kHzのクロック・ソースです。VLOは消費電力が非常に低いため、広範なアプリケーションに使用されます。


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『MSP430 32kHz水晶発振器』

適切な水晶、正しい負荷回路、および適切な基板レイアウトの選択は、安定した水晶発振器のために重要です。このアプリケーション・レポートでは、水晶発振器の機能について要約し、MSP430の超低消費電力動作用の適切な水晶を選択するためのパラメータについて説明します。また、正しい基板レイアウトについてのヒントや例も紹介しています。このドキュメントには、量産時の安定した発振器の動作を保証するために行うことができる、発振器のテストについての詳細情報も記載されています。

『MSP430 システム・レベルESDの考慮事項』

シリコン・テクノロジのスケーリングによる低電圧化の進行と、コスト効率の優れた超低消費電力コンポーネントを設計する必要性の高まりにより、システム・レベルの ESD の要求はますます高まっています。このアプリケーション・レポートでは、基板設計者と OEM が堅牢なシステム・レベルのデザインを理解し設計できるよう、各種の ESD トピックについて扱います。

## 8.5 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Community
*TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas, and help solve problems with fellow engineers.

TI Embedded Processors Wiki
*Texas Instruments Embedded Processors Wiki*. Established to help developers get started with embedded processors from Texas Instruments and to foster innovation and growth of general knowledge about the hardware and software surrounding these devices.

## 8.6 商標

LaunchPad, MSP430, MSP430Ware, Code Composer Studio, E2E, EnergyTrace, ULP Advisor are trademarks of Texas Instruments.
All other trademarks are the property of their respective owners.

## 8.7 静電気放電に関する注意事項

すべての集積回路は、適切なESD保護方法を用いて、取扱いと保存を行うようにして下さい。

静電気放電はわずかな性能の低下から完全なデバイスの故障に至るまで、様々な損傷を与えます。高精度の集積回路は、損傷に対して敏感であり、極めてわずかなパラメータの変化により、デバイスに規定された仕様に適合しなくなる場合があります。

## 8.8 Export Control Notice

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## 8.9 Glossary

**TI Glossary** This glossary lists and explains terms, acronyms, and definitions.

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# 9 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。この情報は、そのデバイスについて利用可能な最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。


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## PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package \| Pins | Package qty \| Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|---|---|---|---|---|---|---|---|---|---|
| M430FR2433IRGERG4.A | Active | Production | VQFN (RGE) \| 24 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | FR2433 |
| MSP430FR2433IRGER | Active | Production | VQFN (RGE) \| 24 | 3000 \| LARGE T&R | Yes | NIPDAU \| SN | Level-1-260C-UNLIM | -40 to 85 | FR2433 |
| MSP430FR2433IRGER.A | Active | Production | VQFN (RGE) \| 24 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | FR2433 |
| MSP430FR2433IRGET | Active | Production | VQFN (RGE) \| 24 | 250 \| SMALL T&R | Yes | NIPDAU \| SN | Level-1-260C-UNLIM | -40 to 85 | FR2433 |
| MSP430FR2433IRGET.A | Active | Production | VQFN (RGE) \| 24 | 250 \| SMALL T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | FR2433 |
| MSP430FR2433IYQWR | Active | Production | DSBGA (YQW) \| 24 | 3000 \| LARGE T&R | Yes | SNAGCU | Level-1-260C-UNLIM | -40 to 85 | 430FR2433 |
| MSP430FR2433IYQWR.A | Active | Production | DSBGA (YQW) \| 24 | 3000 \| LARGE T&R | Yes | SNAGCU | Level-1-260C-UNLIM | -40 to 85 | 430FR2433 |
| MSP430FR2433IYQWT | Active | Production | DSBGA (YQW) \| 24 | 250 \| SMALL T&R | Yes | SNAGCU | Level-1-260C-UNLIM | -40 to 85 | 430FR2433 |
| MSP430FR2433IYQWT.A | Active | Production | DSBGA (YQW) \| 24 | 250 \| SMALL T&R | Yes | SNAGCU | Level-1-260C-UNLIM | -40 to 85 | 430FR2433 |

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

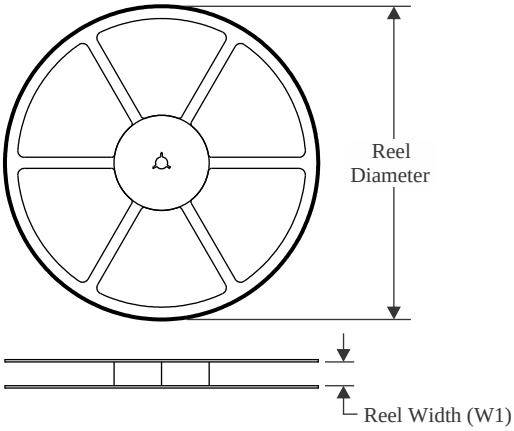
**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative

and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

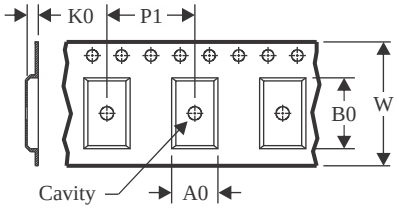
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

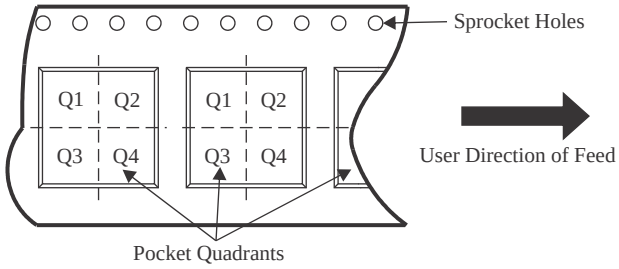



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

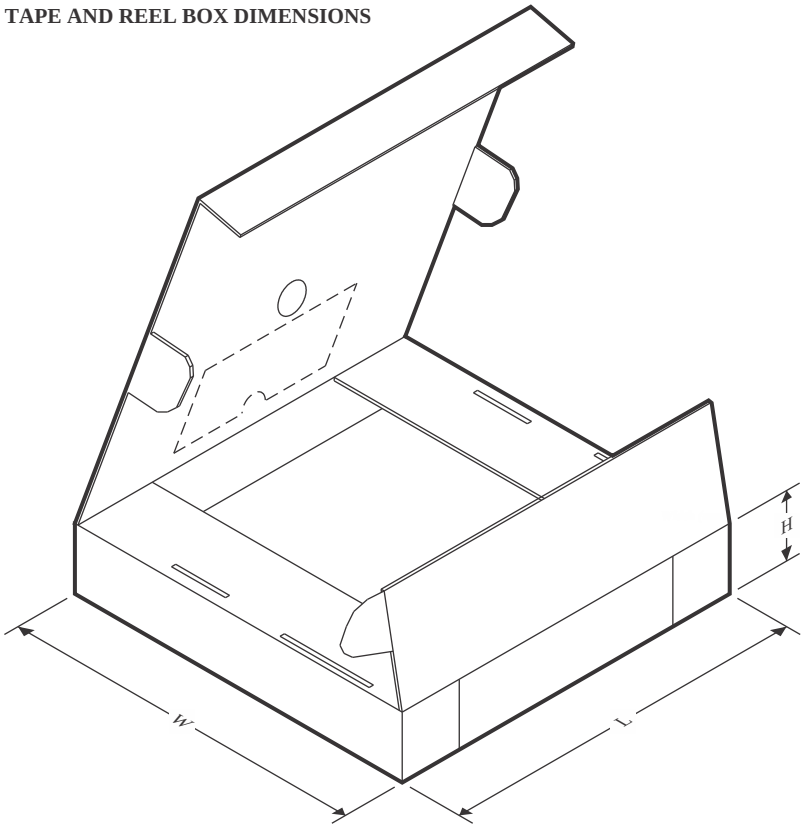
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| MSP430FR2433IRGER | VQFN | RGE | 24 | 3000 | 330.0 | 12.4 | 4.25 | 4.25 | 1.15 | 8.0 | 12.0 | Q2 |
| MSP430FR2433IRGER | VQFN | RGE | 24 | 3000 | 330.0 | 12.4 | 4.25 | 4.25 | 1.15 | 8.0 | 12.0 | Q2 |
| MSP430FR2433IRGET | VQFN | RGE | 24 | 250 | 180.0 | 12.4 | 4.25 | 4.25 | 1.15 | 8.0 | 12.0 | Q2 |
| MSP430FR2433IRGET | VQFN | RGE | 24 | 250 | 180.0 | 12.4 | 4.25 | 4.25 | 1.15 | 8.0 | 12.0 | Q2 |
| MSP430FR2433IYQWR | DSBGA | YQW | 24 | 3000 | 180.0 | 8.4 | 2.38 | 2.4 | 0.8 | 4.0 | 8.0 | Q1 |
| MSP430FR2433IYQWT | DSBGA | YQW | 24 | 250 | 180.0 | 8.4 | 2.38 | 2.4 | 0.8 | 4.0 | 8.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

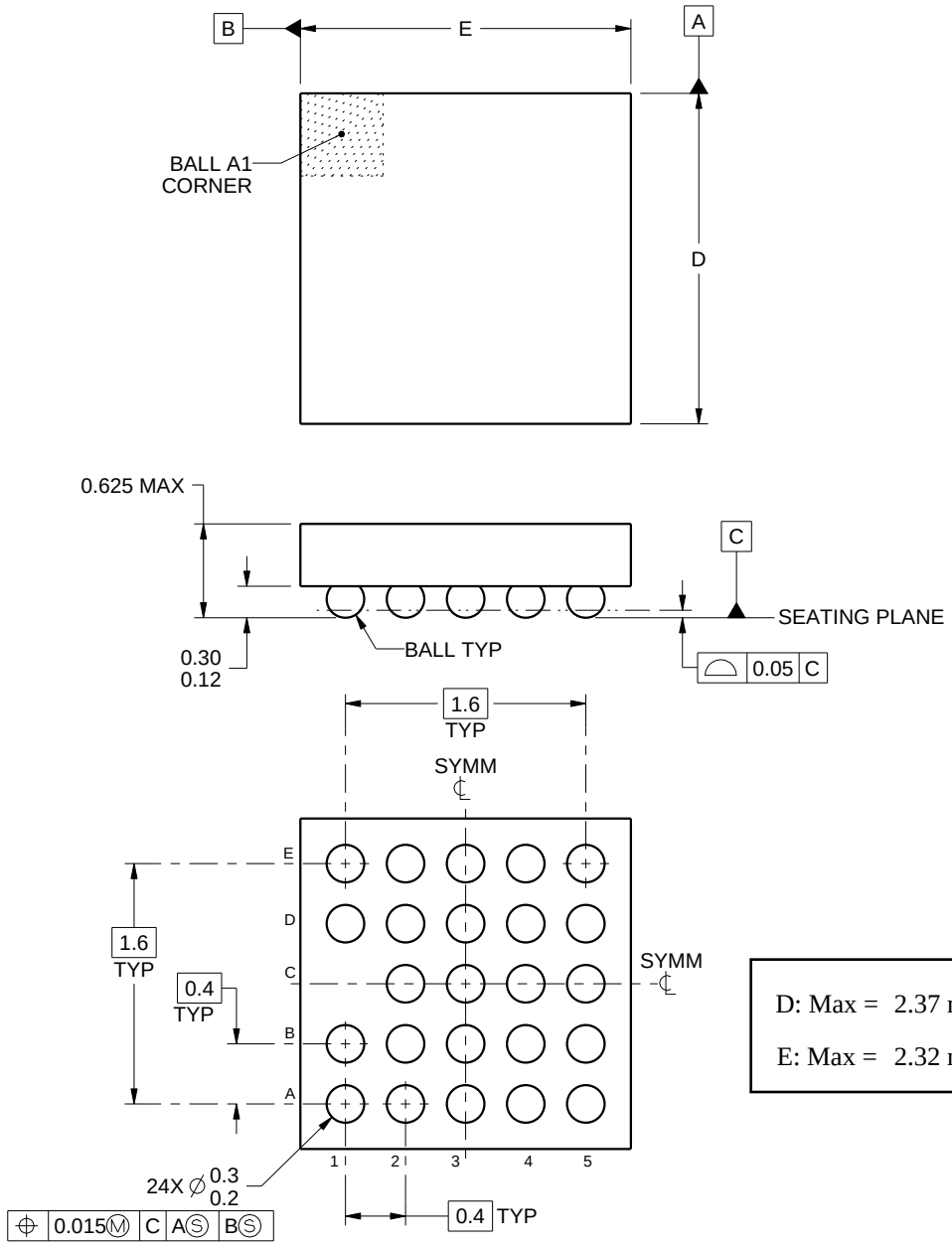
| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| MSP430FR2433IRGER | VQFN | RGE | 24 | 3000 | 346.0 | 346.0 | 33.0 |
| MSP430FR2433IRGER | VQFN | RGE | 24 | 3000 | 360.0 | 360.0 | 36.0 |
| MSP430FR2433IRGET | VQFN | RGE | 24 | 250 | 182.0 | 182.0 | 20.0 |
| MSP430FR2433IRGET | VQFN | RGE | 24 | 250 | 210.0 | 185.0 | 35.0 |
| MSP430FR2433IYQWR | DSBGA | YQW | 24 | 3000 | 182.0 | 182.0 | 20.0 |
| MSP430FR2433IYQWT | DSBGA | YQW | 24 | 250 | 182.0 | 182.0 | 20.0 |

# PACKAGE OUTLINE

## YQW0024

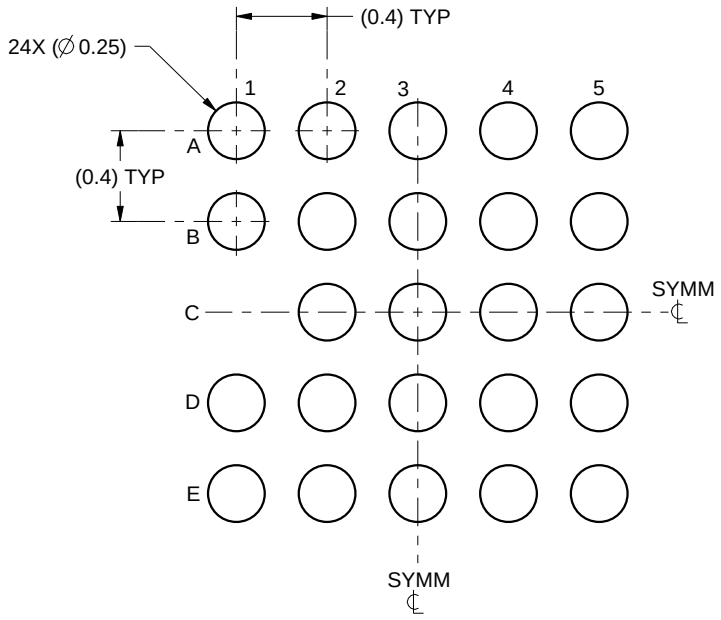
## DSBGA - 0.625 mm max height

DIE SIZE BALL GRID ARRAY

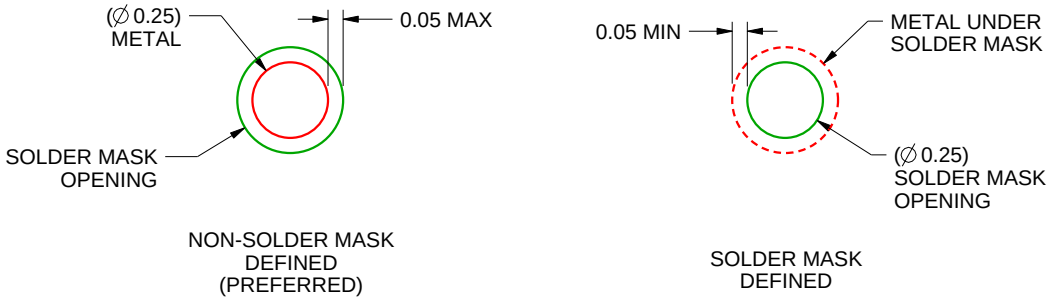



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.




LAND PATTERN EXAMPLE
SCALE:30X




SOLDER MASK DETAILS
NOT TO SCALE

4221561/A 02/2016

NOTES: (continued)

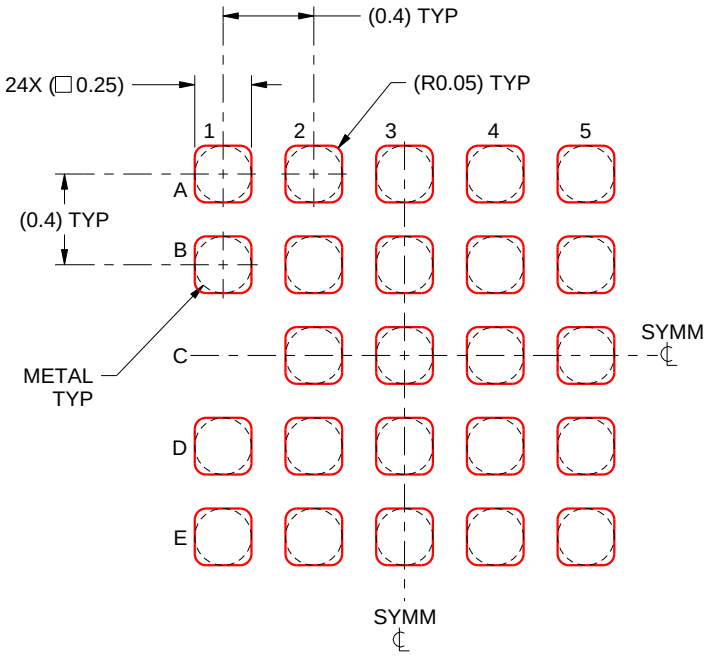
3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints.
   See Texas Instruments Literature No. SNVA009 (www.ti.com/lit/snva009).

# EXAMPLE STENCIL DESIGN

## YQW0024

## DSBGA - 0.625 mm max height

DIE SIZE BALL GRID ARRAY




SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:30X

4221561/A 02/2016

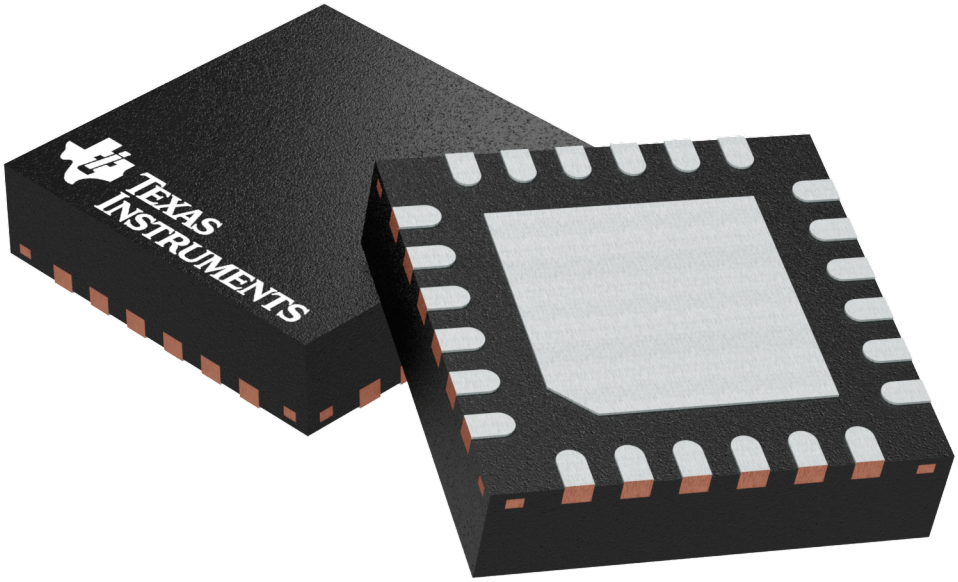
NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

# RGE 24

# VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



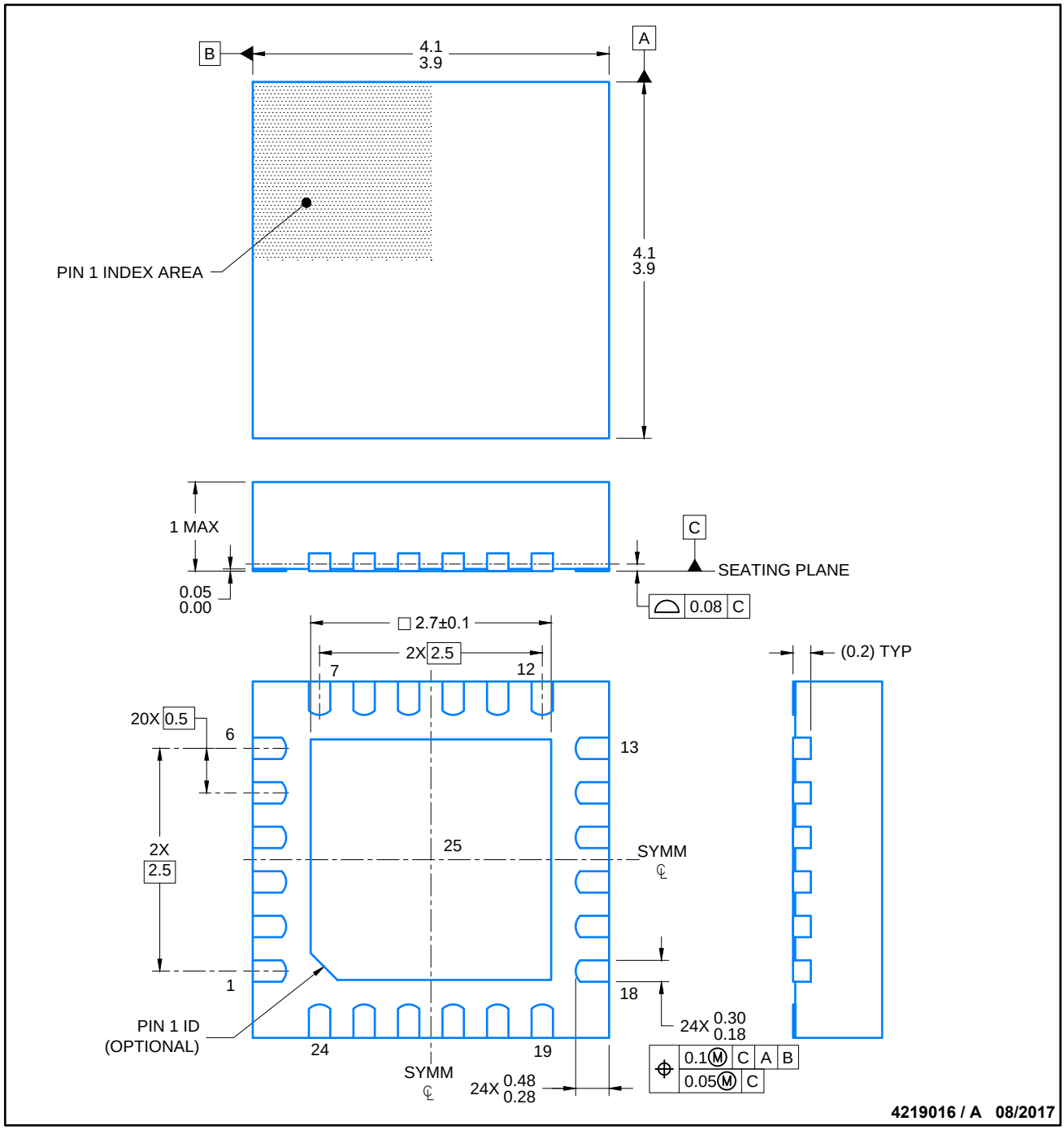

Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

# PACKAGE OUTLINE

## RGE0024H

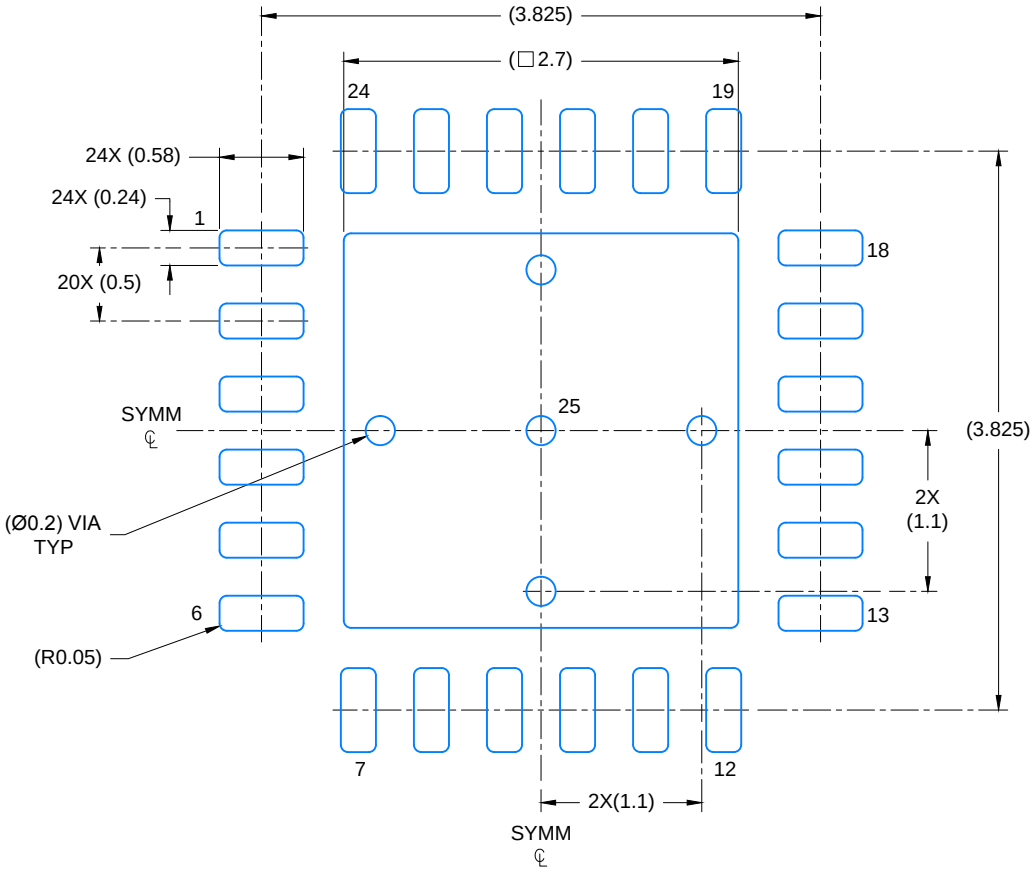
### VQFN - 1 mm max height

PLASTIC QUAD FLATPACK- NO LEAD



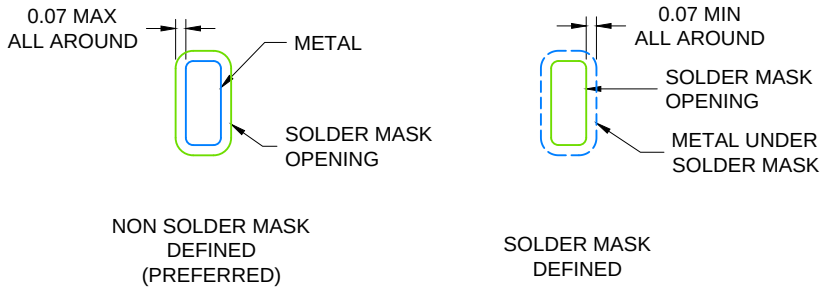

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.




LAND PATTERN EXAMPLE

SCALE: 20X

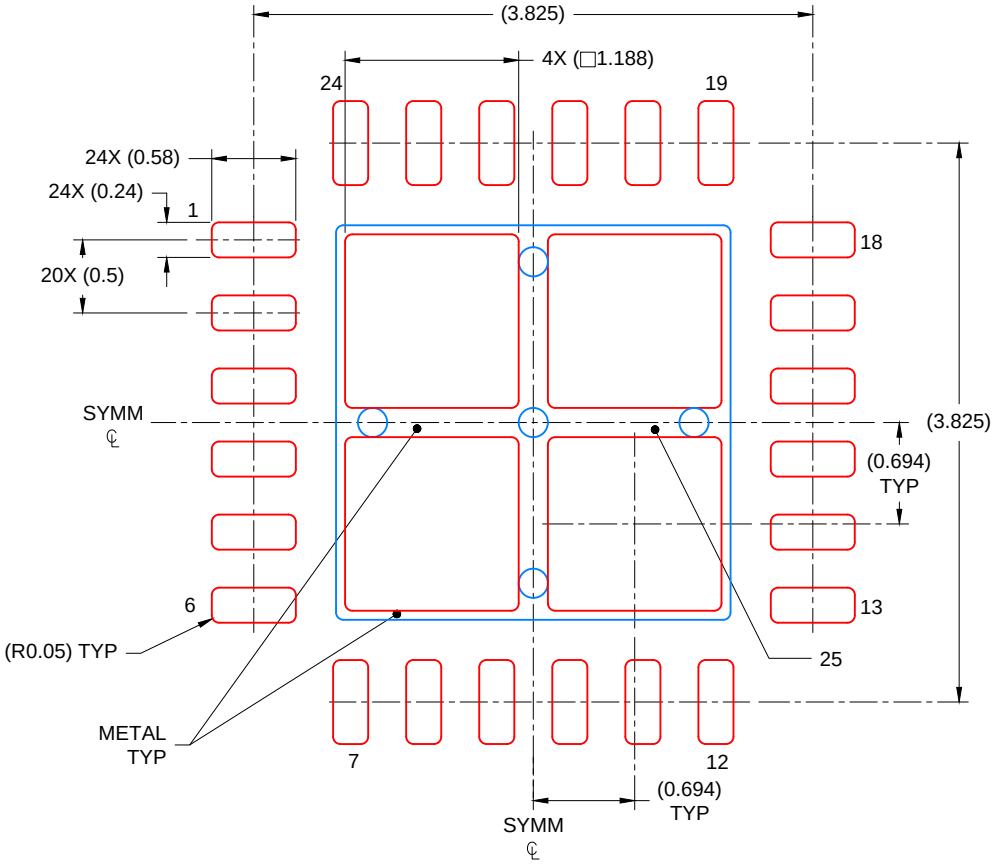



SOLDER MASK DETAILS

4219016 / A 08/2017

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
78% PRINTED COVERAGE BY AREA
SCALE: 20X

4219016 / A 08/2017

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations..

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