MUX36xxx 36V、低容量、低リーク電流、高精度のアナログ・マルチプレクサ

1 特長

- 低いオン容量
  - MUX36S08: 9.4pF
  - MUX36D04: 6.7pF
- 低入力リーク電流: 1pA
- 低電荷注入: 0.3pC
- レール・ツー・レール動作
- 幅広い電源電圧範囲: ±5V～±18V、10V～36V
- 低オン抵抗: 125Ω
- 遷移時間: 92ns
- Break-Before-Makeの切り替え動作
- V_{DD}に接続可能なENピン
- ロジック・レベル: 2V～V_{DD}
- 低い消費電流: 45µA
- ESD保護(HBM): 2000V
- 業界標準のTSSOPパッケージと小型のWQFNパッケージ
- 他の構成については、次の資料を参照
  - TMUX6111/12/13 (4 チャネル SPST)
  - TMUX6121/22/23 (2 チャネル SPST)
  - TMUX6119 (1 チャネル SPDT)
  - TMUX6136 (2 チャネル SPDT)
  - TMUX6104 (1 チャネル 4:1)

2 アプリケーション

- ファクトリ・オートメーションと産業プロセス制御
- プログラマブル・ロジック・コントローラ（PLC）
- アナログ入力モジュール
- ATE試験装置
- バッテリ・モニタリング・システム

3 概要

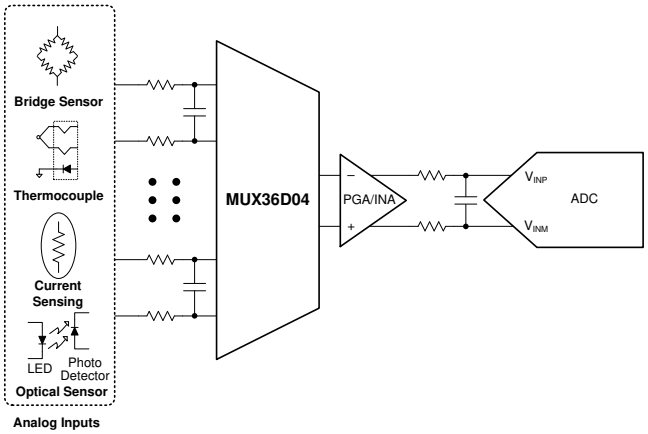
MUX36S08およびMUX36D04 (MUX36xxx)は、最新のCMOS (相補型金属酸化膜半導体)アナログ・マルチプレクサ(MUX)です。MUX36S08は8:1シングルエンド・チャネル、MUX36D04は差動4:1またはデュアル4:1シングルエンド・チャネルを提供します。MUX36S08およびMUX36D04は、デュアル電源(±5V～±18V)でも単電源(10V～36V)でも正常に動作します。また、対称電源(V_{DD} = 12V、V_{SS} = –12Vなど)でも、非対称電源(V_{DD} = 12V、V_{SS} = –5Vなど)でも正常に動作します。すべてのデジタル入力にはTTLロジック互換のスレッショルドがあり、有効な電源電圧範囲で動作していれば、TTLとCMOSの両方のロジックと互換性が確保されます。

製品情報(1)

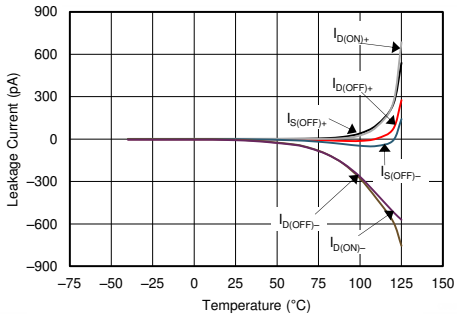
型番	パッケージ	本体サイズ(公称)
MUX36S08	TSSOP (16)	5.00mm×4.40mm
MUX36D04	WQFN (16)	4.00mm×4.00mm

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にあるパッケージ・オプションについての付録を参照してください。

概略回路図



リーク電流と温度



英語版のTI製品についての情報を翻訳したこの資料は、製品の概要を確認する目的で便宜的に提供しているものです。該当する正式な英語版の最新情報は、www.ti.comで閲覧でき、その内容が常に優先されます。TIでは翻訳の正確性および妥当性につきましては一切保証いたしません。実際の設計などの前には、必ず最新版の英語版をご参照くださいますようお願いいたします。

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4 改訂履歴

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Revision C (April 2018) から **Revision D** に変更 **Page**

- 「*特長*」:「他の構成については、次の資料を参照」を 追加 ... 1
- Added RRJ (WQFN) package option to the MUX36D08 ... 5
- Changed the WQFN S6 pin number From: 19 To: 9 ... 5
- Added the RRJ package option to the MUX36D04 ... 6
- Added WQFN (RRJ) data to *Thermal Information* ... 8
- Changed On-resistance drift unit value From: Ω To: %/°C ... 8
- Changed $I_{DL(ON)}$ unit value From: nA To: pA ... 8

Revision B (July 2016) から **Revision C** に変更 **Page**

- 「特長」にWQFNパッケージ・オプションを 追加 ... 1
- 「製品情報」にWQFNパッケージ・オプションを 追加 ... 1
- Changed Description column of MUX36D04 row in *Device Comparison Table* ... 5
- Added WQFN (RUM) data to *Thermal Information* ... 8
- Changed On-resistance drift TYP value From: 0.52 To: 0.64 in *Electrical Characteristics: Dual Supply* ... 8
- Changed Analog Switch, I_D parameter in *Electrical Characteristics: Dual Supply* table: split parameter into $I_{D(OFF)}$ and $I_{D(ON)}$ parameters, changed symbols, parameter names, and test conditions ... 8
- Changed Analog Switch, $I_{DL(ON)}$ parameter test conditions in *Electrical Characteristics: Dual Supply* table ... 8
- Changed On-resistance drift TYP value From: 0.47 To: 1.13 in *Electrical Characteristics: Single Supply* ... 10
- Changed Analog Switch, I_D parameter in *Electrical Characteristics: Single Supply* table: split parameter into $I_{D(OFF)}$

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and $I_{D(ON)}$ parameters, changed symbols, parameter names, and $I_{D(ON)}$ test conditions 10
- Changed and swapped data between 25°C and 85°C to fix the typo 11
- Changed 図 30: changed low-voltage level to 0 V 19
- Changed 図 33: added 0 V line, flipped V_S supply symbol 21
- Changed 図 37: changed 5 V_{RMS} marking in *Audio Precision* box 23
- Changed description of MUX36D04 in *Overview* section 24
- Changed 図 43: changed OPA140 amplifier and charge kickback filter box 28

Revision A (January 2016) から Revision B に変更 **Page**

- Added differential on-leakage current parameter to *Electrical Characteristics* table 8
- Added *Differential On-Leakage Current* section 18

2016年1月発行のものから更新 **Page**

- 製品プレビューから量産データに変更 1

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5 概要（続き）

MUX36S08およびMUX36D04のオン/オフ・リーク電流は非常に低いため、これらのマルチプレクサは入力インピーダンスの高い信号源からの信号を、最小限の誤差でスイッチング可能です。消費電流が45µAと低いため、携帯用アプリケーションで使用できます。

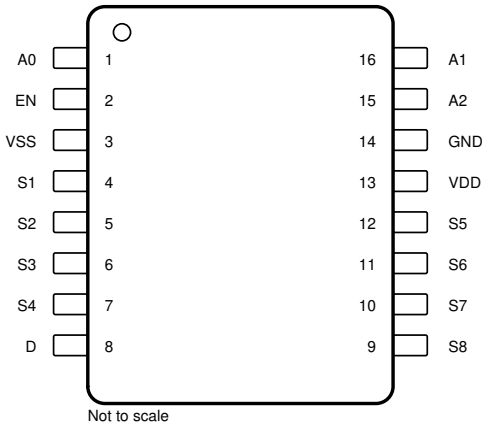
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6 Device Comparison Table

PRODUCT	DESCRIPTION
MUX36S08	8-channel, single-ended analog multiplexer (8:1 mux)
MUX36D04	4-channel differential or dual 4:1 single-ended analog multiplexer (8:2 mux)

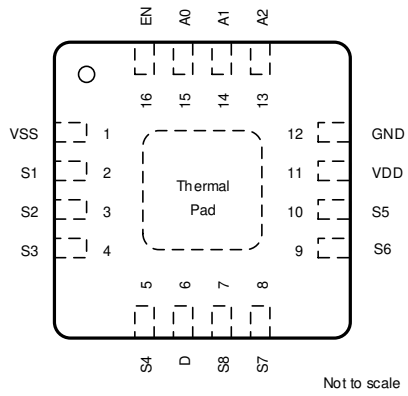
7 Pin Configuration and Functions

MUX36S08: PW Package
16-Pin TSSOP
Top View



Not to scale

MUX36S08: RUM and RRJ Package
16-Pin WQFN
Top View



Not to scale

RUM and RRJ have the same package dimension, but different thermal pad dimension and lead finger length.

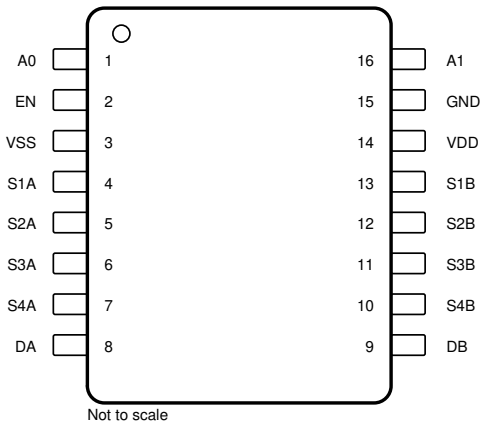
Pin Functions: MUX36S08

PIN			FUNCTION	DESCRIPTION
NAME	TSSOP	WQFN		
A0	1	15	Digital input	Address line 0
A1	16	14	Digital input	Address line 1
A2	15	13	Digital input	Address line 2
D	8	6	Analog input or output	Drain pin. Can be an input or output.
EN	2	16	Digital input	Active high digital input. When this pin is low, all switches are turned off. When this pin is high, the A[2:0] logic inputs determine which switch is turned on.
GND	14	12	Power supply	Ground (0 V) reference
S1	4	2	Analog input or output	Source pin 1. Can be an input or output.
S2	5	3	Analog input or output	Source pin 2. Can be an input or output.
S3	6	4	Analog input or output	Source pin 3. Can be an input or output.
S4	7	5	Analog input or output	Source pin 4. Can be an input or output.
S5	12	10	Analog input or output	Source pin 5. Can be an input or output.
S6	11	9	Analog input or output	Source pin 6. Can be an input or output.
S7	10	8	Analog input or output	Source pin 7. Can be an input or output.
S8	9	7	Analog input or output	Source pin 8. Can be an input or output.
VDD	13	11	Power supply	Positive power supply. This pin is the most positive power-supply potential. For reliable operation, connect a decoupling capacitor ranging from 0.1 µF to 10 µF between V_{DD} and GND.
VSS	3	1	Power supply	Negative power supply. This pin is the most negative power-supply potential. In single-supply applications, this pin can be connected to ground. For reliable operation, connect a decoupling capacitor ranging from 0.1 µF to 10 µF between V_{SS} and GND.
Thermal Pad(1)	-	-	Power supply	Exposed Pad. The exposed pad is electrically connected to V_{SS} internally. Connect EP to V_{SS} to achieve rated thermal and ESD performance.

(1) RUM and RRJ have the same package dimension, but different thermal pad dimension and lead finger length.

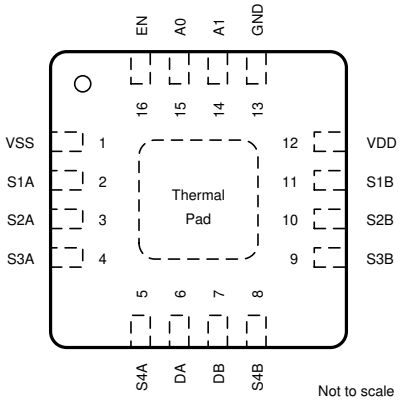
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MUX36D04: PW Package
16-Pin TSSOP
Top View



Not to scale

MUX36D04: RUM and RRJ Package
16-Pin WQFN
Top View



Not to scale

RUM and RRJ have the same package dimension, but different thermal pad dimension and lead finger length.

Pin Functions: MUX36D04

PIN			FUNCTION	DESCRIPTION
NAME	TSSOP	WQFN		
A0	1	15	Digital input	Address line 0
A1	16	14	Digital input	Address line 1
DA	8	6	Analog input or output	Drain pin A. Can be an input or output.
DB	9	7	Analog input or output	Drain pin B. Can be an input or output.
EN	2	16	Digital input	Active high digital input. When this pin is low, all switches are turned off. When this pin is high, the A[1:0] logic inputs determine which pair of switches is turned on.
GND	15	13	Power supply	Ground (0 V) reference
S1A	4	2	Analog input or output	Source pin 1A. Can be an input or output.
S2A	5	3	Analog input or output	Source pin 2A. Can be an input or output.
S3A	6	4	Analog input or output	Source pin 3A. Can be an input or output.
S4A	7	5	Analog input or output	Source pin 4A. Can be an input or output.
S1B	13	11	Analog input or output	Source pin 1B. Can be an input or output.
S2B	12	10	Analog input or output	Source pin 2B. Can be an input or output.
S3B	11	9	Analog input or output	Source pin 3B. Can be an input or output.
S4B	10	8	Analog input or output	Source pin 4B. Can be an input or output.
V_{DD}	14	12	Power supply	Positive power supply. This pin is the most positive power supply potential. For reliable operation, connect a decoupling capacitor ranging from 0.1 µF to 10 µF between V_{DD} and GND.
V_{SS}	3	1	Power supply	Negative power supply. This pin is the most negative power supply potential. In single-supply applications, this pin can be connected to ground. For reliable operation, connect a decoupling capacitor ranging from 0.1 µF to 10 µF between V_{SS} and GND.
Thermal Pad(1)	-	-	Power supply	Exposed Pad. The exposed pad is electrically connected to VSS internally. Connect EP to V_{SS} to achieve rated thermal and ESD performance.

(1) RUM and RRJ have the same package dimension, but different thermal pad dimension and lead finger length.

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8 Specifications

8.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
Voltage	Supply	V_{DD}	–0.3	40	V
		V_{SS}	–40	0.3	
		$V_{DD} – V_{SS}$		40	
	Digital input pins: (2)EN, A0, A1, A2		$V_{SS} – 0.3$	$V_{DD} + 0.3$	V
	Analog input pins: (2)Sx, SxA, SxB, D, DA, DB		$V_{SS} – 2$	$V_{DD} + 2$	V
Current(3)			–30	30	mA
Temperature	Operating, T_A		–55	150	°C
	Junction, T_J			150	
	Storage, T_{stg}		–65	150	

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Only one pin at a time
(3) Voltage limits are valid if current is limited to ±30 mA.

8.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

8.3 Recommended Operating Conditions

			MIN	NOM	MAX	UNIT
V_{DD}(1)	Positive power-supply voltage	Dual supply	5		18	V
		Single supply	10		36	
V_{SS}(2)	Negative power-supply voltage (dual supply)		–5		–18	V
$V_{DD} – V_{SS}$	Supply voltage		10		36	V
V_S	Source pins voltage(3)		V_{SS}		V_{DD}	V
V_D	Drain pins voltage		V_{SS}		V_{DD}	V
V_{EN}	Enable pin voltage		V_{SS}		V_{DD}	V
V_A	Address pins voltage		V_{SS}		V_{DD}	V
I_{CH}	Channel current (T_A = 25°C)		–25		25	mA
T_A	Operating temperature		–40		125	°C

(1) When V_{SS} = 0 V, V_{DD} can range from 10 V to 36 V.
(2) V_{DD} and V_{SS} can be any value as long as 10 V ≤ ($V_{DD} – V_{SS}$) ≤ 36 V.
(3) V_S is the voltage on all S pins.

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8.4 Thermal Information

THERMAL METRIC[1]		MUX36S08 and MUX36D04			UNIT
		PW (TSSOP)	RUM (WQFN)	RRJ (WQFN)	
		16 PINS	16 PINS	16 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	103.8	37.3	46.2	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	36.8	31.6	37.7	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	49.8	16.2	21.7	°C/W
ψ_{JT}	Junction-to-top characterization parameter	2.7	0.5	0.7	°C/W
ψ_{JB}	Junction-to-board characterization parameter	49.1	16.2	21.7	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	6.1	6.2	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

8.5 Electrical Characteristics: Dual Supply

at T_A = 25°C, V_{DD} = 15 V, and V_{SS} = –15 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
ANALOG SWITCH							
	Analog signal range	T_A = –40°C to +125°C		V_{SS}		V_{DD}	V
R_{ON}	On-resistance	V_S = 0 V, I_{CH} = 1 mA			125	170	Ω
		V_S = ±10 V, I_{CH} = 1 mA			145	200	Ω
			T_A = –40°C to +85°C			230	Ω
			T_A = –40°C to +125°C			250	Ω
ΔR_{ON}	On-resistance mismatch between channels	V_S = ±10 V, I_{CH} = 1 mA			2.4	6	Ω
			T_A = –40°C to +85°C			9	Ω
			T_A = –40°C to +125°C			11	Ω
R_{FLAT}	On-resistance flatness	V_S = 10 V, 0 V, –10 V			2.4	6	Ω
			T_A = –40°C to +85°C			53	Ω
			T_A = –40°C to +125°C			58	Ω
	On-resistance drift	V_S = 0 V			0.64		%/°C
$I_{S(OFF)}$	Input leakage current	Switch state is off, V_S = ±10 V, V_D = ±10 V[1]		–0.04	0.001	0.04	nA
			T_A = –40°C to +85°C	–0.15		0.15	nA
			T_A = –40°C to +125°C	–1.9		1.9	nA
$I_{D(OFF)}$	Output off leakage current	Switch state is off, V_S = ±10 V, V_D = ±10 V[1]		–0.1	0.005	0.1	nA
			T_A = -40°C to +85°C	–0.5		0.5	nA
			T_A = –40°C to +125°C	–2		2	nA
$I_{D(ON)}$	Output on leakage current	Switch state is on, V_D = ±10 V, V_S = floating		–0.1	0.008	0.1	nA
			T_A = –40°C to +85°C	–0.5		0.5	nA
			T_A = –40°C to +125°C	–3.3		3.3	nA
$I_{DL(ON)}$	Differential on-leakage current	Switch state is on, V_{DA} = V_{DB} = ±10 V, V_S = floating		–15	3	15	pA
			T_A = –40°C to +85°C	–100		100	pA
			T_A = –40°C to +125°C	–500		500	pA
LOGIC INPUT							
V_{IH}	Logic voltage high			2			V
V_{IL}	Logic voltage low					0.8	V

(1) When V_S is positive, V_D is negative, and vice versa.

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Electrical Characteristics: Dual Supply (continued)

at T_A = 25°C, V_{DD} = 15 V, and V_{SS} = –15 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
I_D	Input current					0.15	µA
SWITCH DYNAMICS(2)							
t_{ON}	Enable turn-on time	V_S = ±10 V, R_L = 300 Ω, C_L= 35 pF			88	136	ns
			T_A = –40°C to +85°C			144	
			T_A = –40°C to +125°C			151	
t_{OFF}	Enable turn-off time	V_S = ±10 V, R_L = 300 Ω, C_L= 35 pF			63	75	ns
			T_A = –40°C to +85°C			83	
			T_A = –40°C to +125°C			90	
t_t	Transition time	V_S = 10 V, R_L = 300 Ω, C_L= 35 pF			92	143	ns
			T_A = –40°C to +85°C			151	
			T_A = –40°C to +125°C			157	
t_{BBM}	Break-before-make time delay	V_S = 10 V, R_L = 300 Ω, C_L= 35 pF, T_A = –40°C to +125°C		30	54		ns
Q_J	Charge injection	C_L = 1 nF, R_S = 0 Ω	V_S = 0 V		0.3		pC
			V_S = –15 V to +15 V		±0.6		
	Off-isolation	R_L = 50 Ω, V_S = 1 V_{RMS}, f = 1 MHz	Nonadjacent channel to D, DA, DB		–96		dB
			Adjacent channel to D, DA, DB		–85		
	Channel-to-channel crosstalk	R_L = 50 Ω, V_S = 1 V_{RMS}, f = 1 MHz	Nonadjacent channels		–96		dB
			Adjacent channels		–88		
$C_{S(OFF)}$	Input off-capacitance	f = 1 MHz, V_S = 0 V			2.4	2.9	pF
$C_{D(OFF)}$	Output off-capacitance	f = 1 MHz, V_S = 0 V	MUX36S08		7.5	8.4	pF
			MUX36D04		4.3	5	
$C_{S(ON)}$, $C_{D(ON)}$	Output on-capacitance	f = 1 MHz, V_S = 0 V	MUX36S08		9.4	10.6	pF
			MUX36D04		6.7	7.7	
POWER SUPPLY							
	V_{DD} supply current	All V_A = 0 V or 3.3 V, V_S = 0 V, V_{EN} = 3.3 V			45	59	µA
			T_A = –40°C to +85°C			62	
			T_A = –40°C to +125°C			83	
	V_{SS} supply current	All V_A = 0 V or 3.3 V, V_S = 0 V, V_{EN} = 3.3 V			25	34	µA
			T_A = –40°C to +85°C			37	
			T_A = –40°C to +125·C			57	

(2) Specified by design, not subject to production testing.

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8.6 Electrical Characteristics: Single Supply

at T_A = 25°C, V_{DD} = 12 V, and V_{SS} = 0 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
ANALOG SWITCH							
	Analog signal range	T_A = –40°C to +125°C		V_{SS}		V_{DD}	V
R_{ON}	On-resistance	V_S = 10 V, I_{CH} = 1 mA			235	340	Ω
			T_A = –40°C to +85°C			390	
			T_A = –40°C to +125°C			430	
ΔR_{ON}	On-resistance match	V_S = 10 V, I_{CH} = 1 mA			3.1	12	Ω
			T_A = –40°C to +85°C			19	
			T_A = –40°C to +125°C			23	
	On-resistance drift	V_S = 10 V			1.13		%/°C
$I_{S(OFF)}$	Input leakage current	Switch state is off, V_S = 1 V and V_D = 10 V, or V_S = 10 V and V_D = 1 V(1)		–0.04	0.001	0.04	nA
			T_A = –40°C to +85°C	–0.15		0.15	
			T_A = –40°C to +125°C	–1.9		1.9	
$I_{D(OFF)}$	Output off leakage current	Switch state is off, V_S = 1 V and V_D = 10 V, or V_S = 10 V and V_D = 1 V(1)		–0.1	0.005	0.1	nA
			T_A = –40°C to +85°C	–0.5		0.5	
			T_A = –40°C to +125°C	–2		2	
$I_{D(ON)}$	Output on leakage current	Switch state is on, V_D = 1 V and 10 V, V_S = floating		–0.1	0.008	0.1	nA
			T_A = –40°C to +85°C	–0.5		0.5	
			T_A = –40°C to +125°C	–3.3		3.3	
LOGIC INPUT							
V_{IH}	Logic voltage high			2.0			V
V_{IL}	Logic voltage low					0.8	V
I_D	Input current					0.15	µA
SWITCH DYNAMIC CHARACTERISTICS(2)							
t_{ON}	Enable turn-on time	V_S = 8 V, R_L = 300 Ω, C_L= 35 pF			85	140	ns
			T_A = –40°C to +85°C			145	
			T_A = –40°C to +125°C			149	
t_{OFF}	Enable turn-off time	V_S = 8 V, R_L = 300 Ω, C_L= 35 pF			48	83	ns
			T_A = –40°C to +85°C			94	
			T_A = –40°C to +125°C			102	
t_t	Transition time	V_S = 8 V, C_L= 35 pF			87	147	ns
		V_S = 8 V, R_L = 300 Ω, C_L= 35 pF	T_A = –40°C to +85°C			153	
		V_S = 8 V, R_L = 300 Ω, C_L= 35 pF	T_A = –40°C to +125°C			155	
t_{BBM}	Break-before-make time delay	V_S = 8 V, R_L = 300 Ω, C_L= 35 pF, T_A = –40°C to +125°C		30	54		ns
Q_J	Charge injection	C_L = 1 nF, R_S = 0 Ω	V_S = 6 V		0.15		pC
			V_S = 0 V to 12 V,		±0.4		
	Off-isolation	R_L = 50 Ω, V_S = 1 V_{RMS}, f = 1 MHz	Nonadjacent channel to D, DA, DB		-96		dB
			Adjacent channel to D, DA, DB		-85		
	Channel-to-channel crosstalk	R_L = 50 Ω, V_S = 1 V_{RMS}, f = 1 MHz	Nonadjacent channels		–96		dB
			Adjacent channels		-88		
$C_{S(OFF)}$	Input off-capacitance	f = 1 MHz, V_S = 6 V			2.7	3.2	pF
$C_{D(OFF)}$	Output off-capacitance	f = 1 MHz, V_S = 6 V	MUX36S08		9.1	10	pF
			MUX36D04		5	5.7	
$C_{S(ON)}$, $C_{D(ON)}$	Output on-capacitance	f = 1 MHz, V_S = 6 V	MUX36S08		10.8	12	pF
			MUX36D04		6.9	8	

(1) When V_S is 1 V, V_D is 10 V, and vice versa.
(2) Specified by design; not subject to production testing.

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Electrical Characteristics: Single Supply (continued)

at T_A = 25°C, V_{DD} = 12 V, and V_{SS} = 0 V (unless otherwise noted)

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
POWER SUPPLY						
V_{DD} supply current	All V_A = 0 V or 3.3 V, V_S = 0 V, V_{EN} = 3.3 V			42	53	µA
		T_A = –40°C to +85°C			56	
		T_A = –40°C to +125°C			77	
V_{SS} supply current	All V_A = 0 V or 3.3 V, V_S = 0 V, V_{EN} = 3.3 V			23	31	µA
		T_A = –40°C to +85°C			38	
		T_A = –40°C to +125°C			51	

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8.7 Typical Characteristics

at T_A = 25°C, V_{DD} = 15 V, and V_{SS} = –15 V (unless otherwise noted)

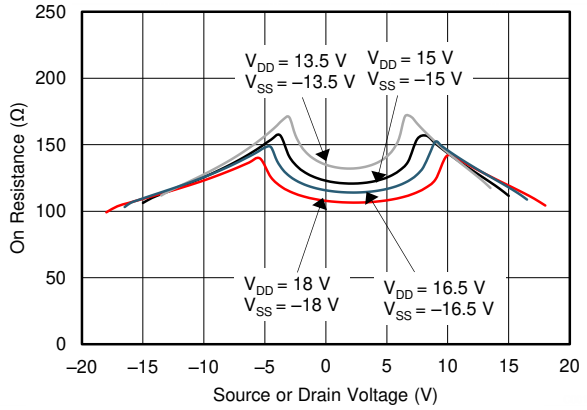
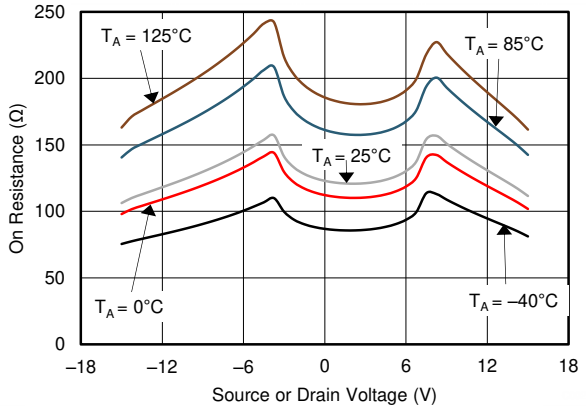


図 1. On-Resistance vs Source or Drain Voltage



V_{DD} = 15 V, V_{SS} = –15 V

図 2. On-Resistance vs Source or Drain Voltage

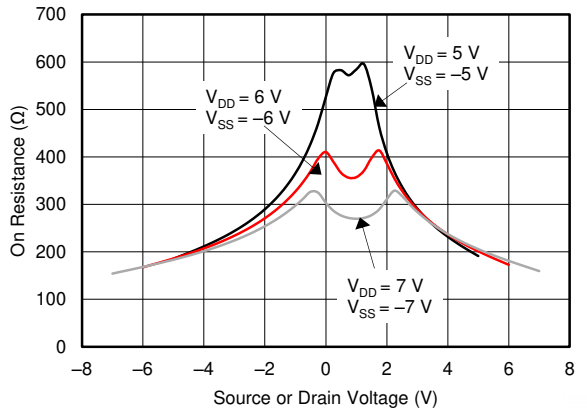
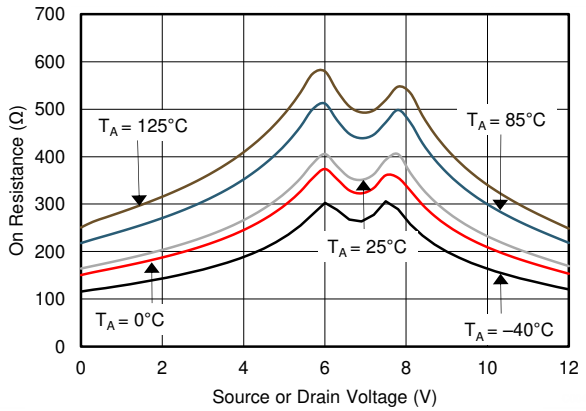


図 3. On-Resistance vs Source or Drain Voltage



V_{DD} = 12 V, V_{SS} = 0 V

図 4. On-Resistance vs Source or Drain Voltage

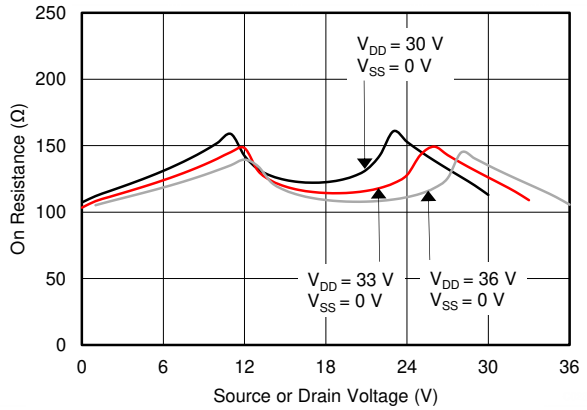


図 5. On-Resistance vs Source or Drain Voltage

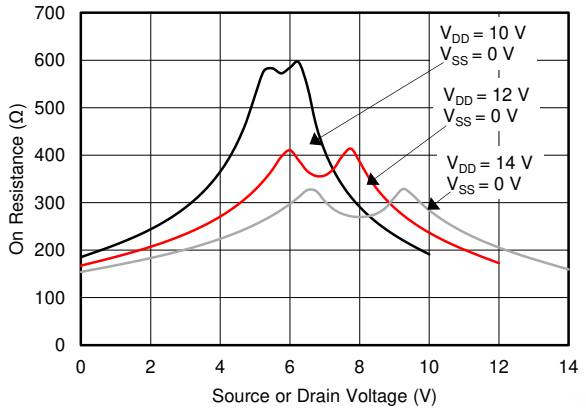
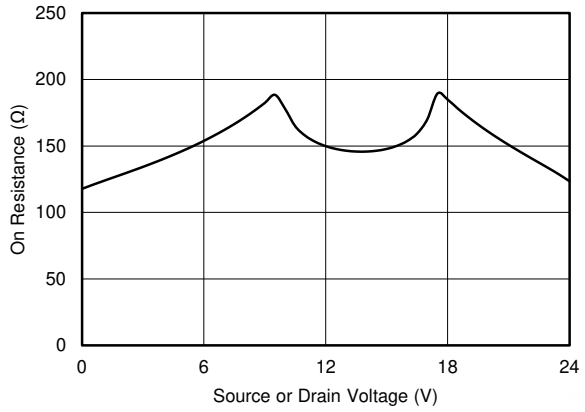


図 6. On-Resistance vs Source or Drain Voltage

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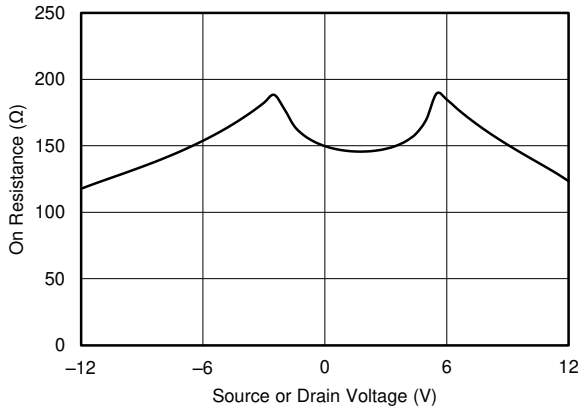
Typical Characteristics (continued)

at T_A = 25°C, V_{DD} = 15 V, and V_{SS} = –15 V (unless otherwise noted)



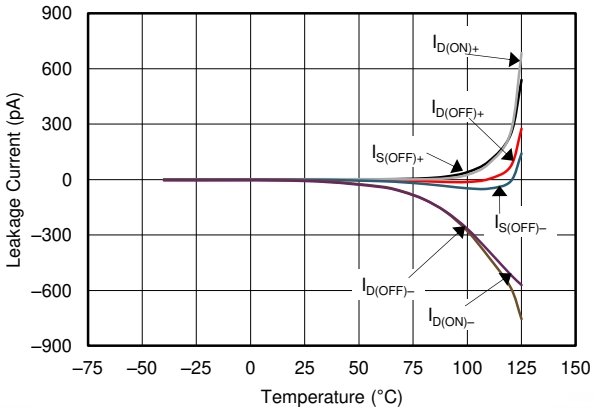
V_{DD} = 24 V, V_{SS} = 0 V

図 7. On-Resistance vs Source or Drain Voltage



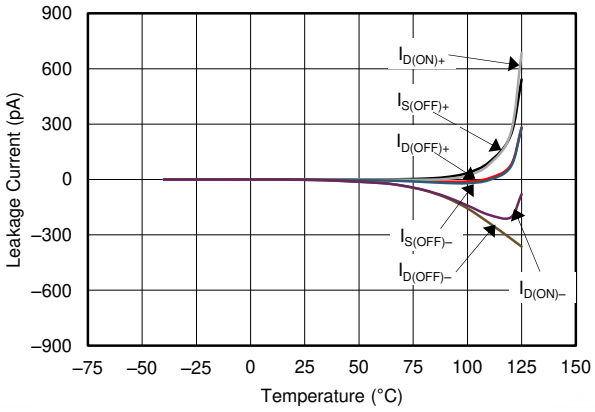
V_{DD} = 12 V, V_{SS} = –12 V

図 8. On-Resistance vs Source or Drain Voltage



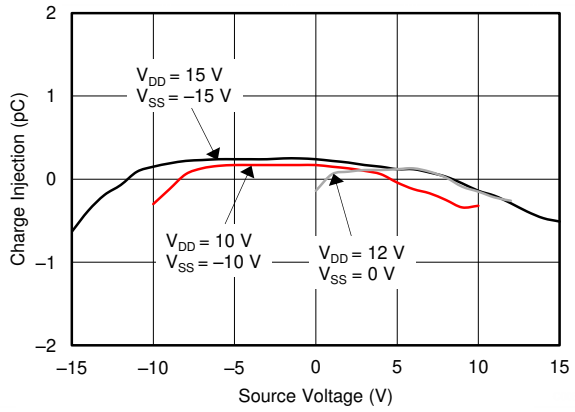
V_{DD} = 15 V, V_{SS} = –15 V

図 9. Leakage Current vs Temperature



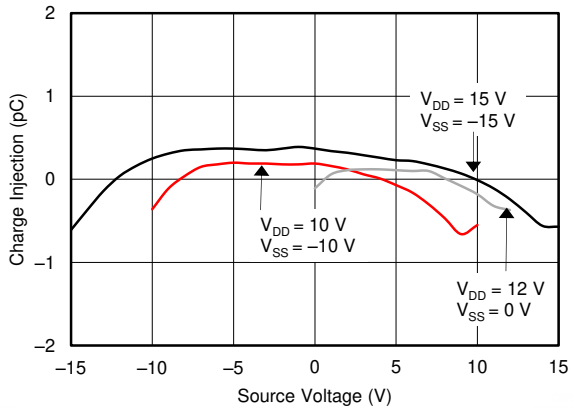
V_{DD} = 12 V, V_{SS} = 0 V

図 10. Leakage Current vs Temperature



MUX36S08, source-to-drain

図 11. Charge Injection vs Source Voltage



MUX36D04, source-to-drain

図 12. Charge Injection vs Source Voltage

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Typical Characteristics (continued)

at T_A = 25°C, V_{DD} = 15 V, and V_{SS} = –15 V (unless otherwise noted)

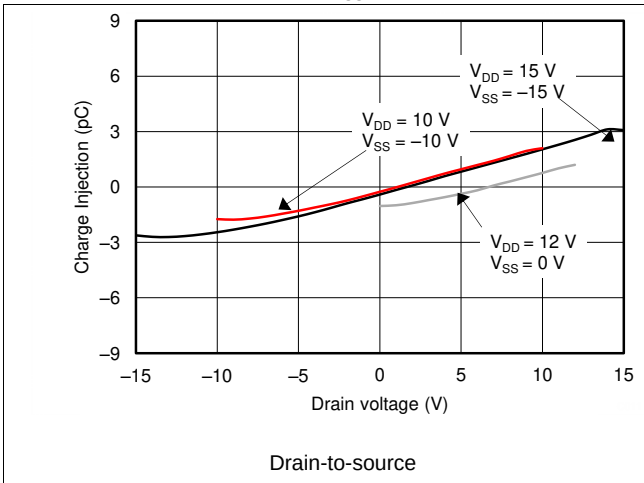


図 13. Charge Injection vs Source or Drain Voltage

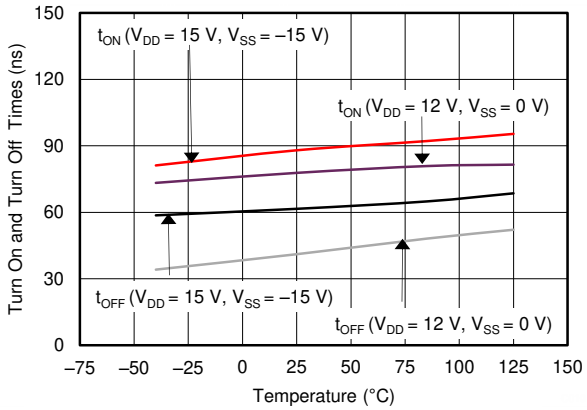


図 14. Turn-On and Turn-Off Times vs Temperature

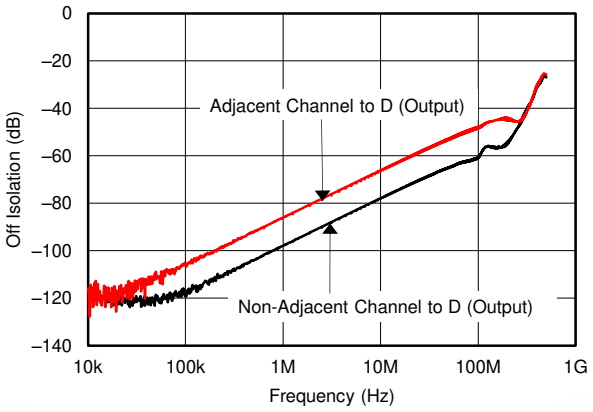


図 15. Off Isolation vs Frequency

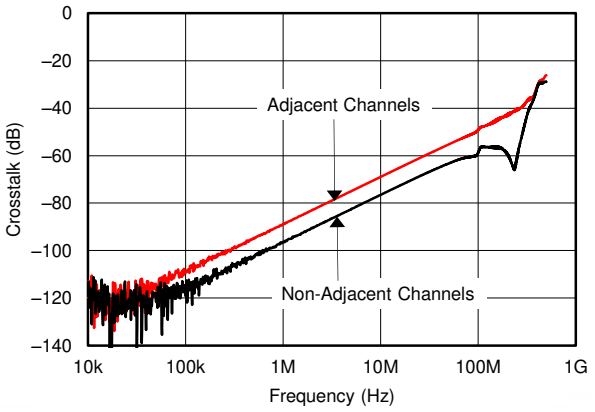


図 16. Crosstalk vs Frequency

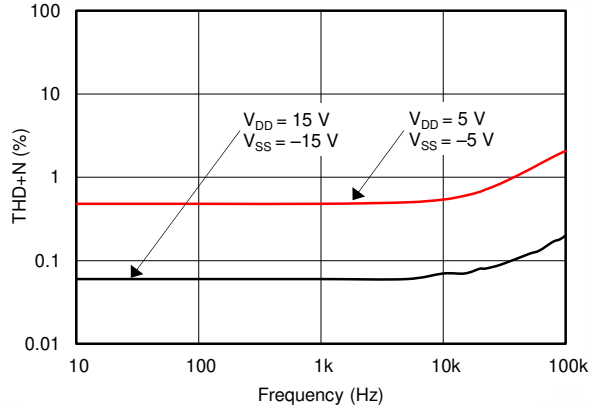


図 17. THD+N vs Frequency

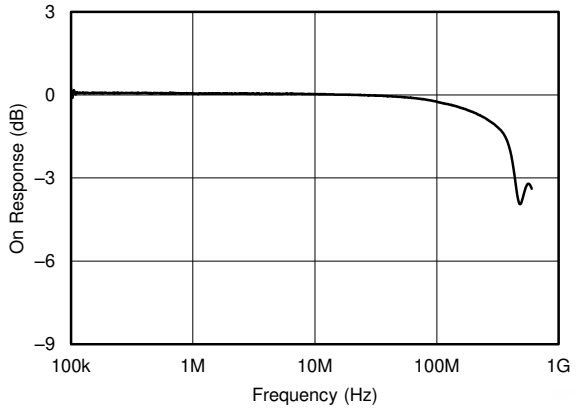
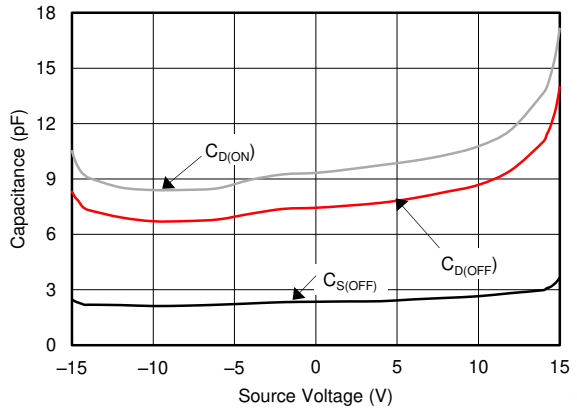


図 18. On Response vs Frequency

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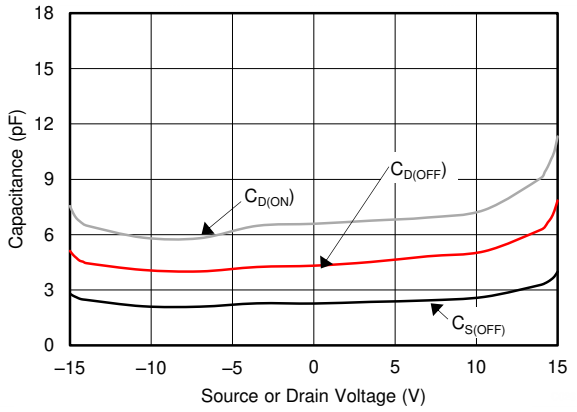
Typical Characteristics (continued)

at T_A = 25°C, V_{DD} = 15 V, and V_{SS} = –15 V (unless otherwise noted)



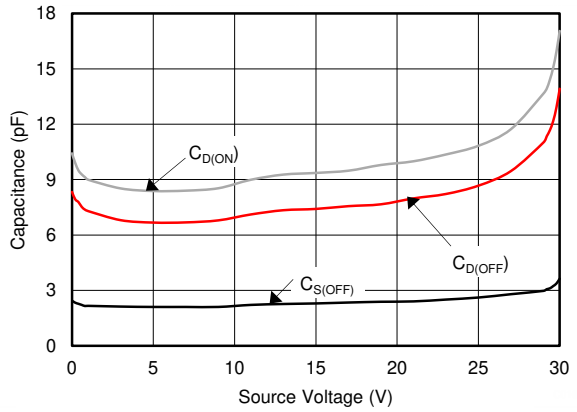
MUX36S08, V_{DD} = 15 V, V_{SS} = –15 V

図 19. Capacitance vs Source Voltage



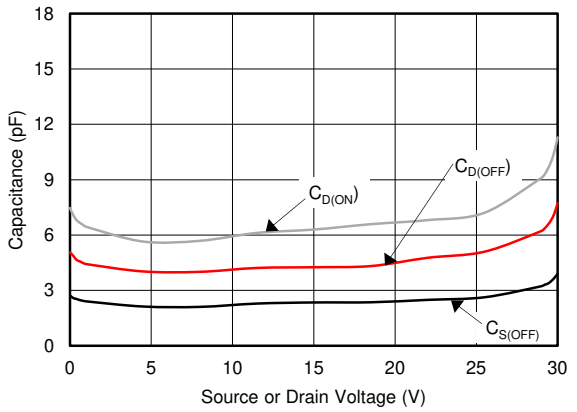
MUX36D04, V_{DD} = 15 V, V_{SS} = –15 V

図 20. Capacitance vs Source Voltage



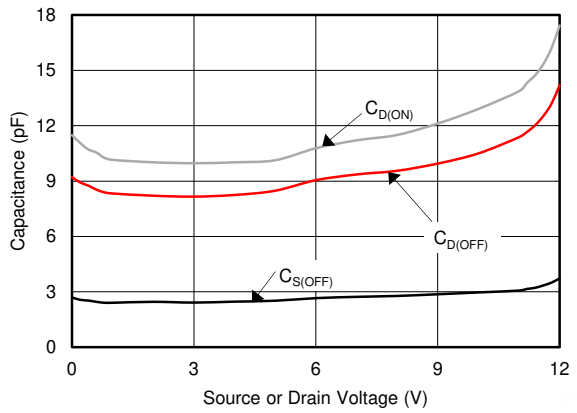
MUX36S08, V_{DD} = 30 V, V_{SS} = 0 V

図 21. Capacitance vs Source Voltage



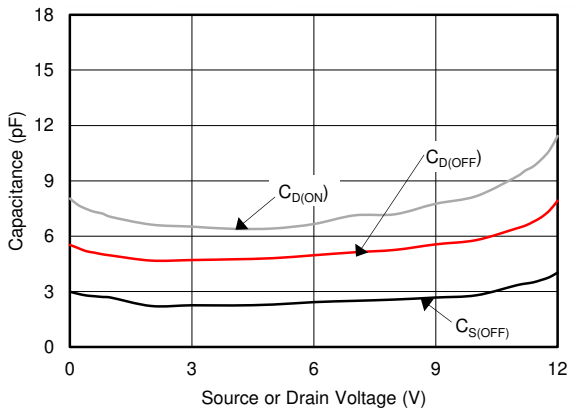
MUX36D04, V_{DD} = 30 V, V_{SS} = 0 V

図 22. Capacitance vs Source Voltage



MUX36S08, V_{DD} = 12 V, V_{SS} = 0 V

図 23. Capacitance vs Source Voltage



MUX36D04, V_{DD} = 12 V, V_{SS} = 0 V

図 24. Capacitance vs Source Voltage

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Typical Characteristics (continued)

at T_A = 25°C, V_{DD} = 15 V, and V_{SS} = –15 V (unless otherwise noted)

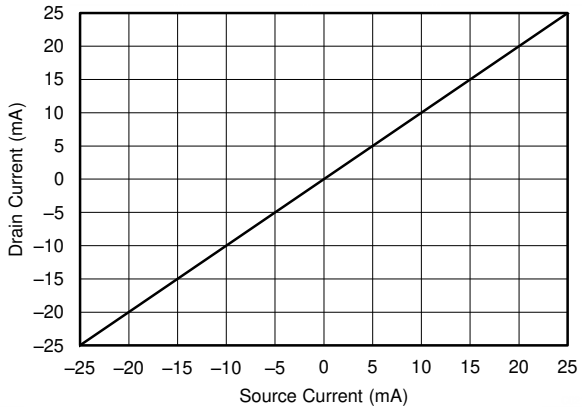


図 25. Source Current vs Drain Current

9 Parameter Measurement Information

9.1 Truth Tables

表 1 and 表 2 show the truth tables for the MUX36S08 and MUX36D04, respectively.

表 1. MUX36S08 Truth Table

EN	A2	A1	A0	STATE
0	X(1)	X(1)	X(1)	All channels are off
1	0	0	0	Channel 1
1	0	0	1	Channel 2
1	0	1	0	Channel 3
1	0	1	1	Channel 4
1	1	0	0	Channel 5
1	1	0	1	Channel 6
1	1	1	0	Channel 7
1	1	1	1	Channel 8

(1) X denotes *don't care*..

表 2. MUX36D04 Truth Table

EN	A1	A0	STATE
0	X(1)	X(1)	All channels are off
1	0	0	Channels 1A and 1B
1	0	1	Channels 2A and 2B
1	1	0	Channels 3A and 3B
1	1	1	Channels 4A and 4B

(1) X denotes *don't care*.

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9.2 On-Resistance

The on-resistance of the MUX36xxx is the ohmic resistance across the source (Sx, SxA, or SxB) and drain (D, DA, or DB) pins of the device. The on-resistance varies with input voltage and supply voltage. The symbol R_{ON} is used to denote on-resistance. The measurement setup used to measure R_{ON} is shown in 図 26. Voltage (V) and current (I_{CH}) are measured using this setup, and R_{ON} is computed as shown in 式 1:

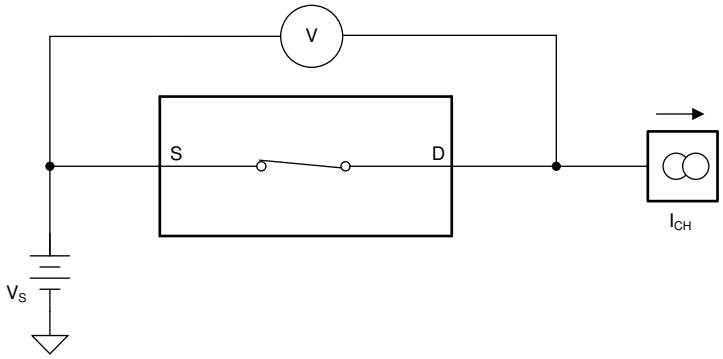


図 26. On-Resistance Measurement Setup

$$R_{ON} = V / I_{CH} \quad (1)$$

9.3 Off-Leakage Current

There are two types of leakage currents associated with a switch during the off state:

1. Source off-leakage current
2. Drain off-leakage current

Source leakage current is defined as the leakage current flowing into or out of the source pin when the switch is off. This current is denoted by the symbol $I_{S(OFF)}$.

Drain leakage current is defined as the leakage current flowing into or out of the drain pin when the switch is off. This current is denoted by the symbol $I_{D(OFF)}$.

The setup used to measure both off-leakage currents is shown in 図 27

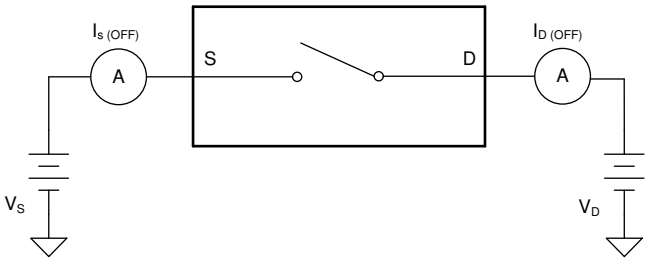


図 27. Off-Leakage Measurement Setup

9.4 On-Leakage Current

On-leakage current is defined as the leakage current that flows into or out of the drain pin when the switch is in the on state. The source pin is left floating during the measurement. 図 28 shows the circuit used for measuring the on-leakage current, denoted by $I_{D(ON)}$.

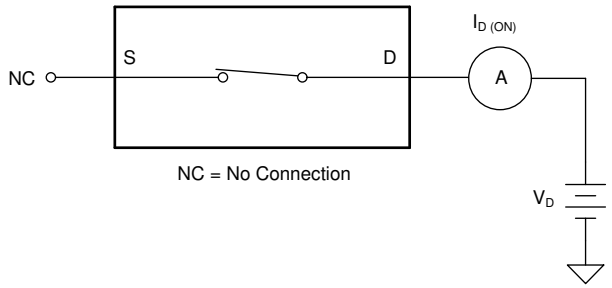


図 28. On-Leakage Measurement Setup

9.5 Differential On-Leakage Current

In case of a differential signal, the on-leakage current is defined as the differential leakage current that flows into or out of the drain pins when the switches is in the on state. The source pins are left floating during the measurement. 図 29 shows the circuit used for measuring the on-leakage current on each signal path, denoted by $I_{DA(ON)}$ and $I_{DB(ON)}$. The absolute difference between these two current is defined as the differential on-leakage current $I_{DL(ON)}$.

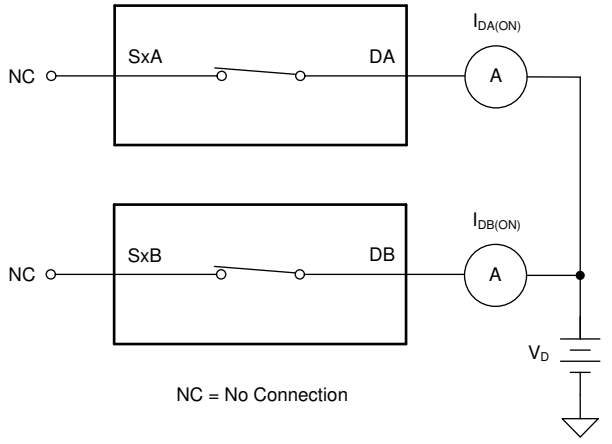


図 29. Differential On-Leakage Measurement Setup

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9.6 Transition Time

Transition time is defined as the time taken by the output of the MUX36xxx to rise or fall to 90% of the transition after the digital address signal has fallen or risen to 50% of the transition. 図 30 shows the setup used to measure transition time, denoted by the symbol t_t.

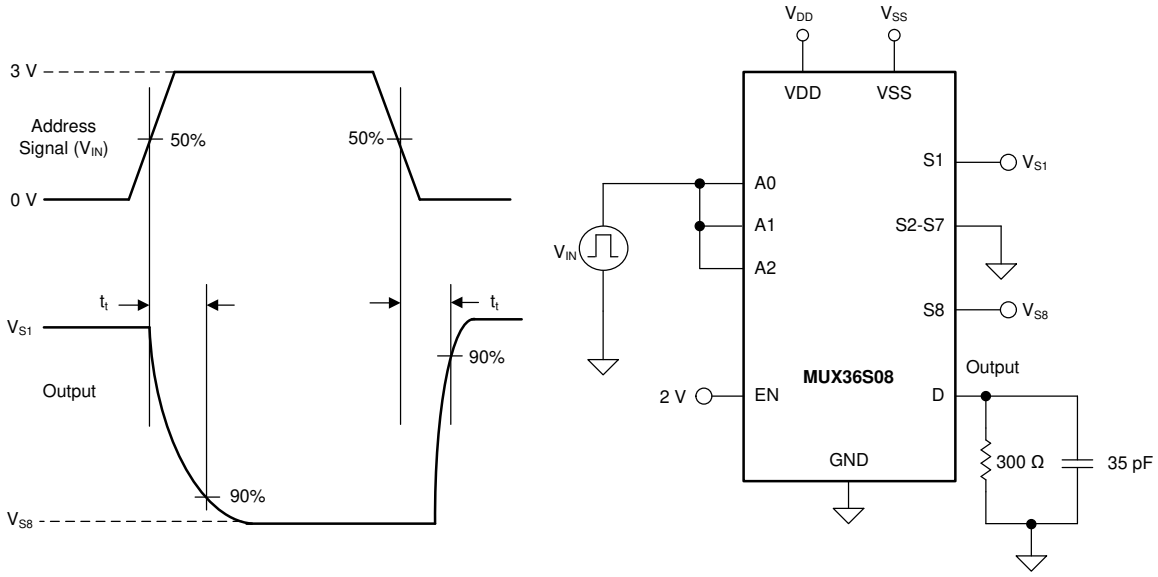


図 30. Transition-Time Measurement Setup

9.7 Break-Before-Make Delay

Break-before-make delay is a safety feature that prevents two inputs from connecting when the MUX36xxx is switching. The MUX36xxx output first breaks from the on-state switch before making the connection with the next on-state switch. The time delay between the *break* and the *make* is known as break-before-make delay. 図 31 shows the setup used to measure break-before-make delay, denoted by the symbol t_{BBM}.

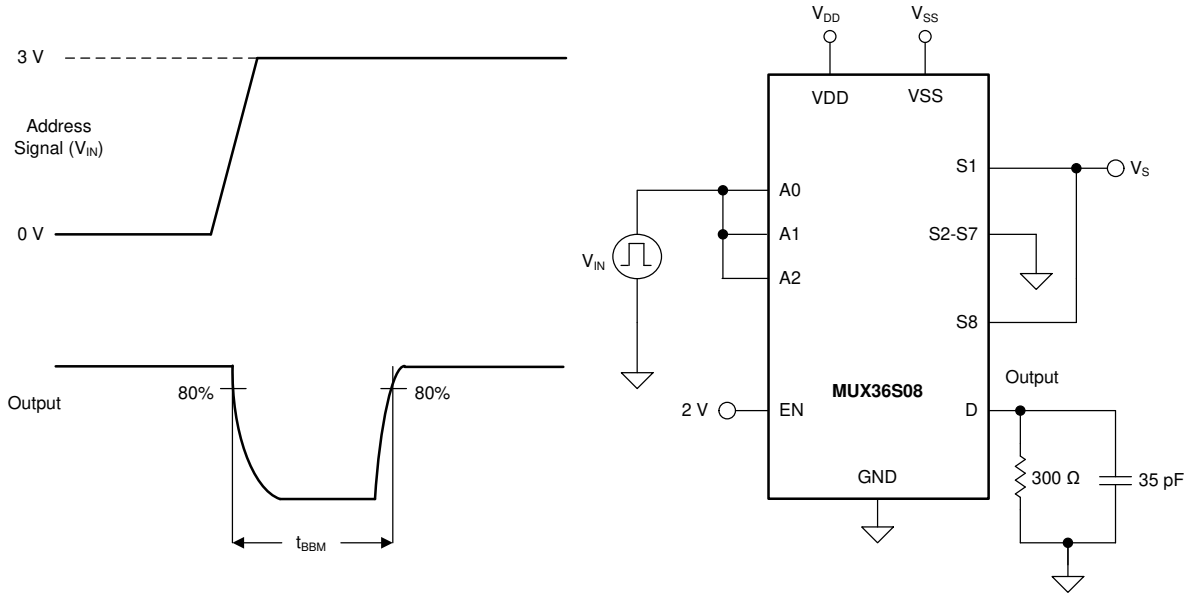


図 31. Break-Before-Make Delay Measurement Setup

9.8 Turn-On and Turn-Off Time

Turn-on time is defined as the time taken by the output of the MUX36xxx to rise to a 90% final value after the enable signal has risen to a 50% final value. 図 32 shows the setup used to measure turn-on time. Turn-on time is denoted by the symbol t_{ON}.

Turn off time is defined as the time taken by the output of the MUX36xxx to fall to a 10% initial value after the enable signal has fallen to a 50% initial value. 図 32 shows the setup used to measure turn-off time. Turn-off time is denoted by the symbol t_{OFF}.

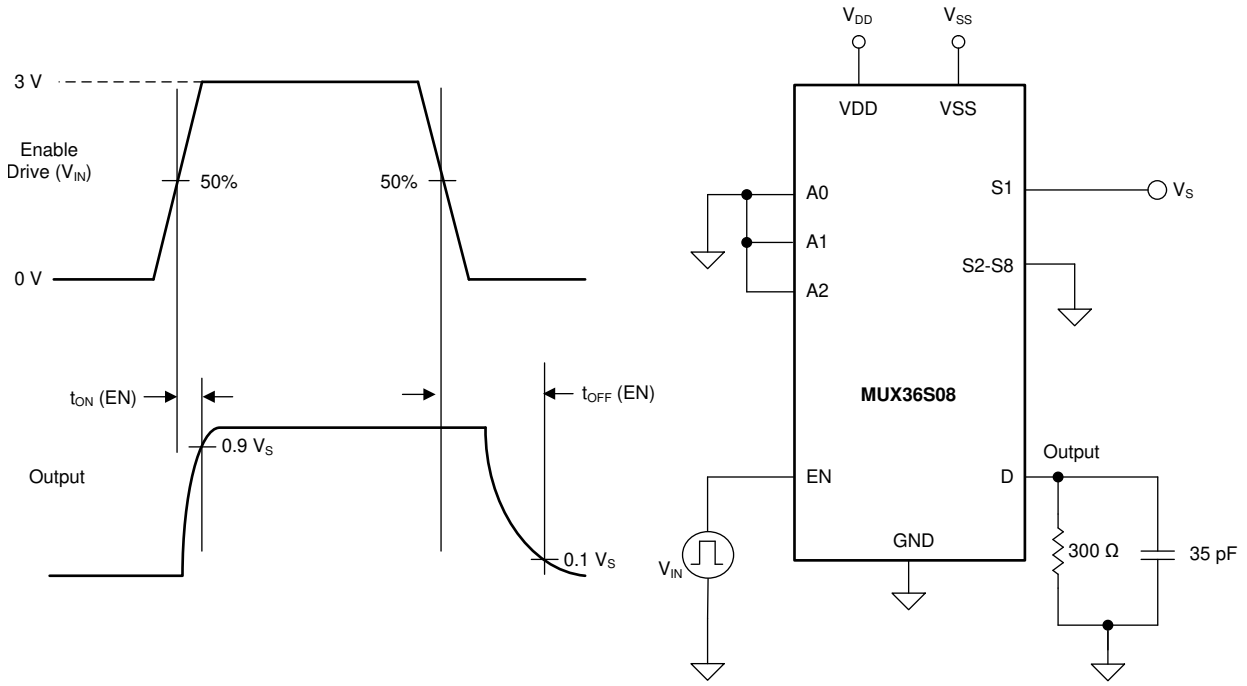


図 32. Turn-On and Turn-Off Time Measurement Setup

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9.9 Charge Injection

The MUX36xxx have a simple transmission-gate topology. Any mismatch in capacitance between the NMOS and PMOS transistors results in a charge injected into the drain or source during the falling or rising edge of the gate signal. The amount of charge injected into the source or drain of the device is known as charge injection, and is denoted by the symbol Q_{INJ}. 図 33 shows the setup used to measure charge injection.

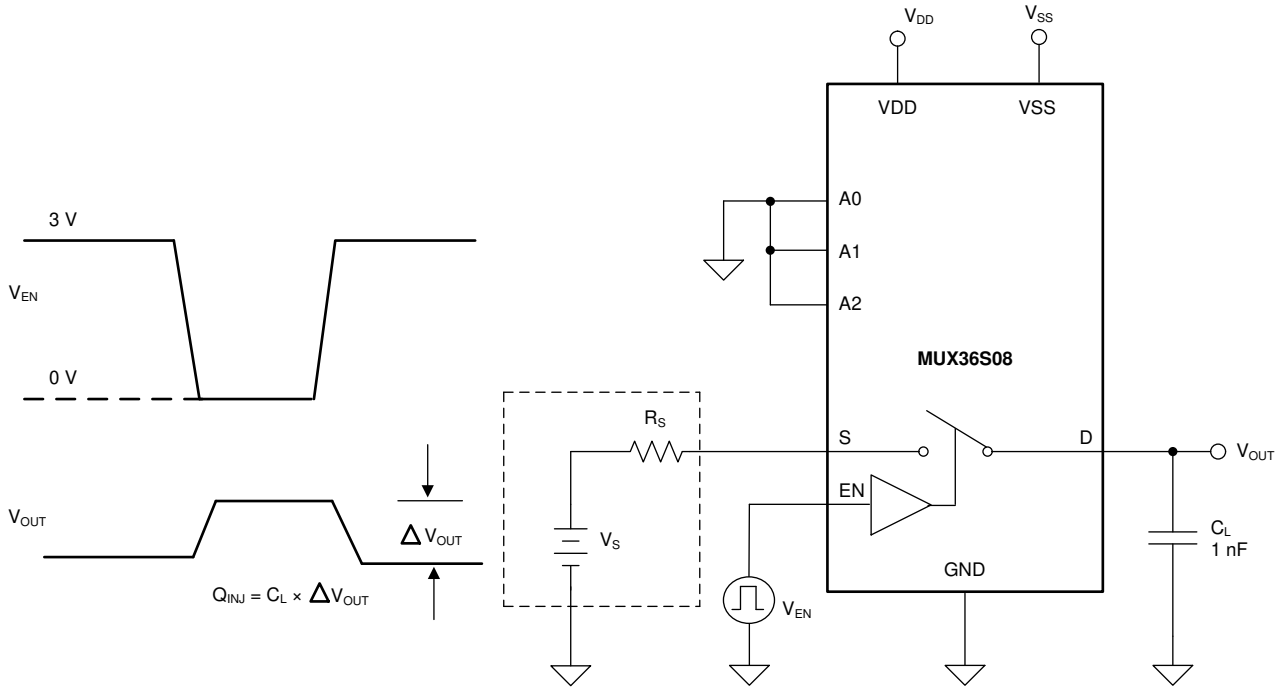


図 33. Charge-Injection Measurement Setup

9.10 Off Isolation

Off isolation is defined as the voltage at the drain pin (D, DA, or DB) of the MUX36xxx when a 1-V_{RMS} signal is applied to the source pin (Sx, SxA, or SxB) of an off-channel. 図 34 shows the setup used to measure off isolation. Use 式 2 to compute off isolation.

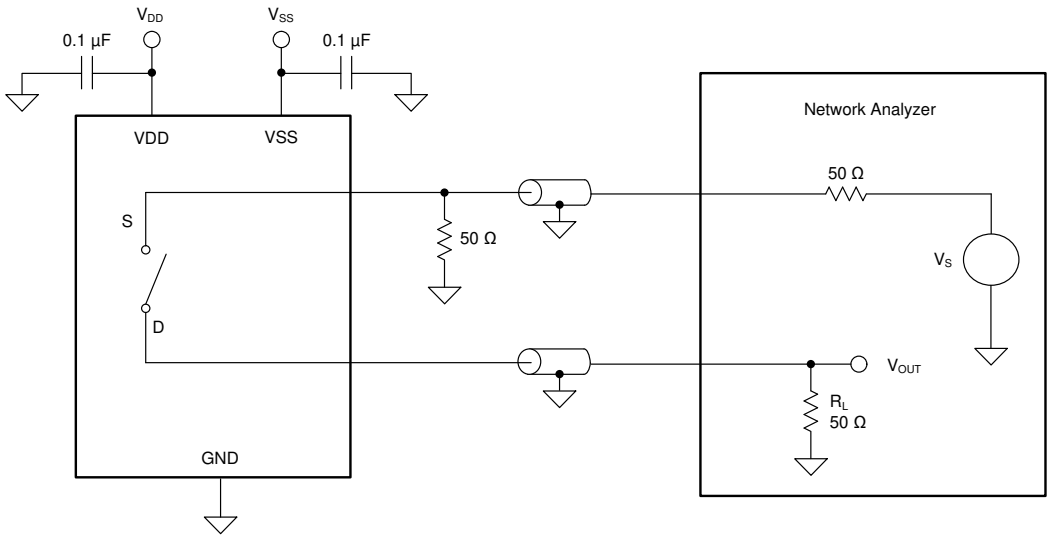


図 34. Off Isolation Measurement Setup

$$\text{Off Isolation} = 20 \cdot \text{Log}\left(\frac{V_{OUT}}{V_S}\right) \quad (2)$$

9.11 Channel-to-Channel Crosstalk

Channel-to-channel crosstalk is defined as the voltage at the source pin (Sx, SxA, or SxB) of an off-channel, when a 1-V_{RMS} signal is applied at the source pin of an on-channel. 図 35 shows the setup used to measure, and 式 3 is the equation used to compute, channel-to-channel crosstalk.

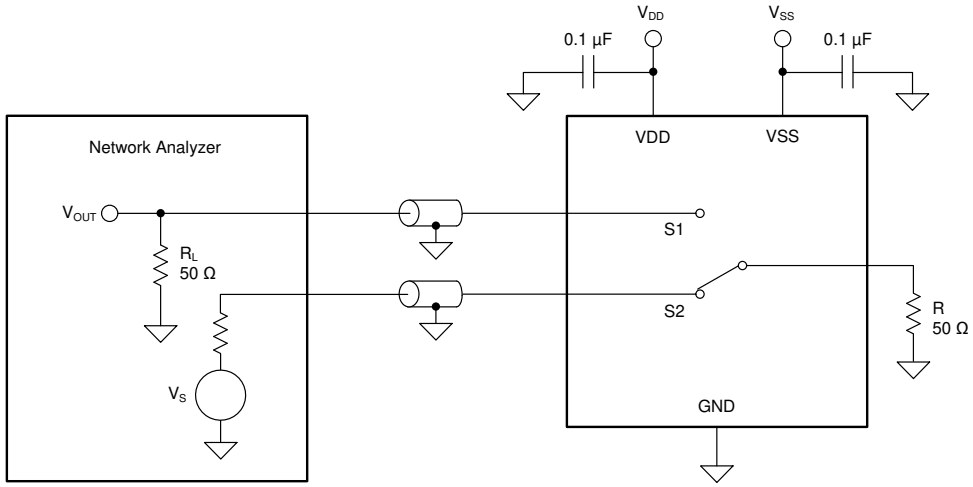


図 35. Channel-to-Channel Crosstalk Measurement Setup

$$\text{Channel-to-Channel Crosstalk} = 20 \cdot \text{Log}\left(\frac{V_{OUT}}{V_S}\right) \quad (3)$$

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9.12 Bandwidth

Bandwidth is defined as the range of frequencies that are attenuated by < 3 dB when the input is applied to the source pin of an on-channel, and the output is measured at the drain pin of the MUX36xxx. 図 36 shows the setup used to measure bandwidth of the mux. Use 式 4 to compute the attenuation.

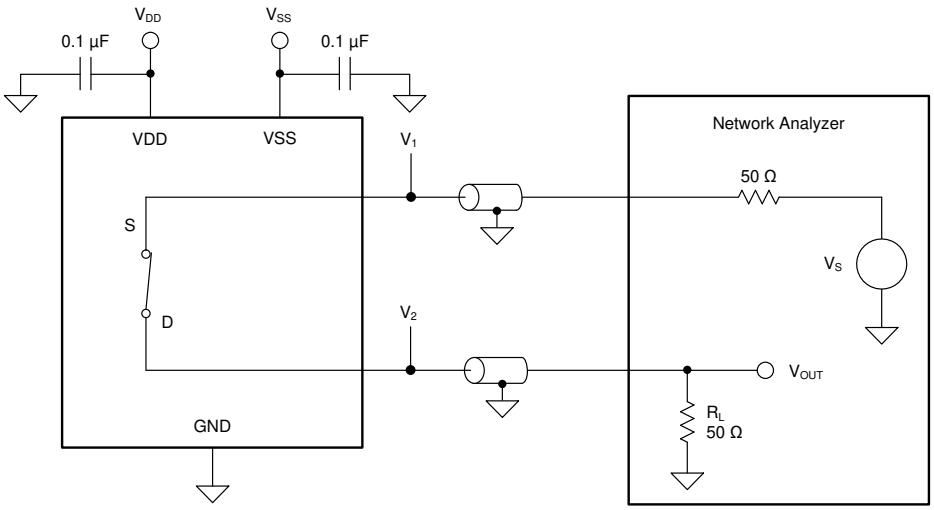


図 36. Bandwidth Measurement Setup

$$\text{Attenuation} = 20 \cdot \text{Log}\left(\frac{V_2}{V_1}\right) \quad (4)$$

9.13 THD + Noise

The total harmonic distortion (THD) of a signal is a measurement of the harmonic distortion, and is defined as the ratio of the sum of the powers of all harmonic components to the power of the fundamental frequency at the mux output. The on-resistance of the MUX36xxx varies with the amplitude of the input signal and results in distortion when the drain pin is connected to a low-impedance load. Total harmonic distortion plus noise is denoted as THD+N. 図 37 shows the setup used to measure THD+N of the MUX36xxx.

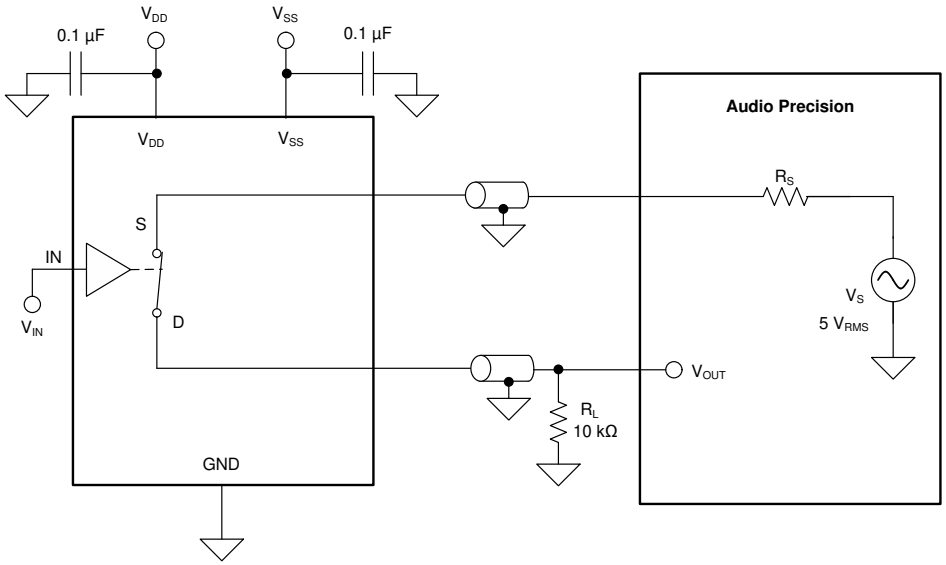


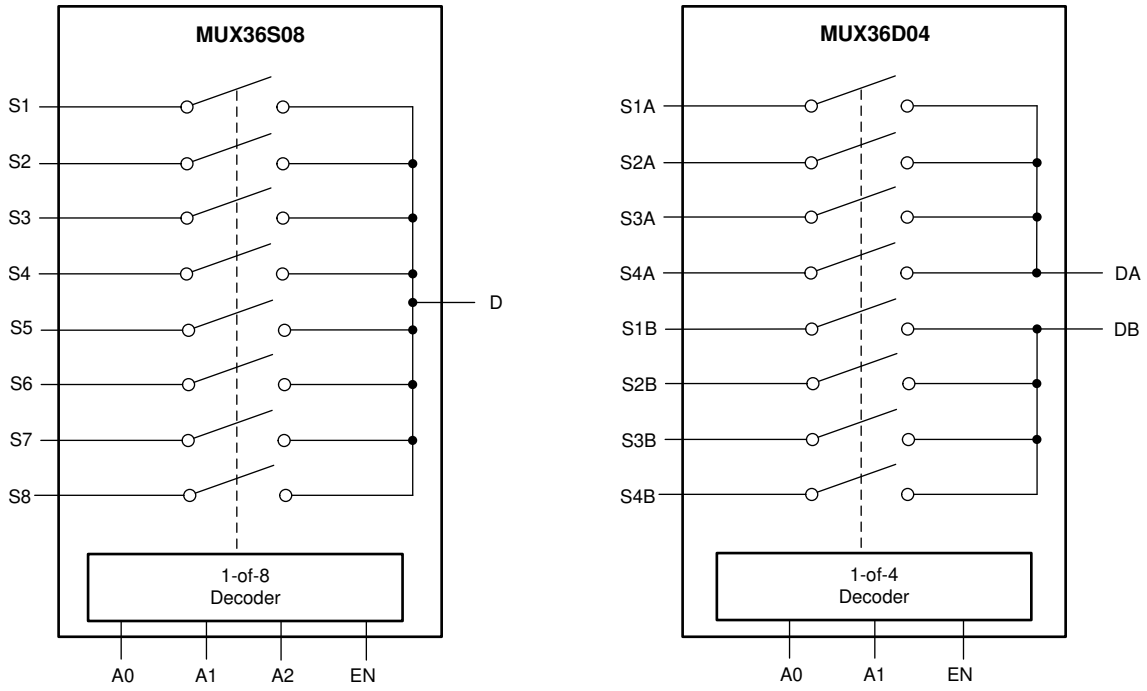
図 37. THD+N Measurement Setup

10 Detailed Description

10.1 Overview

The MUX36xxx are a family of analog multiplexers. The *Functional Block Diagram* section provides a top-level block diagram of both the MUX36S08 and MUX36D04. The MUX36S08 is an 8-channel, single-ended, analog mux. The MUX36D04 is a 4-channel, differential or dual 4:1, single-ended, analog mux. Each channel is turned on or turned off based on the state of the address lines and enable pin.

10.2 Functional Block Diagram



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10.3 Feature Description

10.3.1 Ultralow Leakage Current

The MUX36xxx provide extremely low on- and off-leakage currents. The MUX36xxx are capable of switching signals from high source-impedance inputs into a high input-impedance op amp with minimal offset error because of the ultralow leakage currents. 図 38 shows typical leakage currents of the MUX36xxx versus temperature.

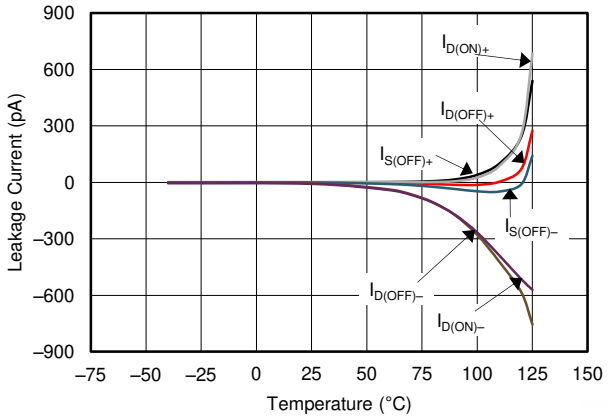


図 38. Leakage Current vs Temperature

10.3.2 Ultralow Charge Injection

The MUX36xxx have a simple transmission gate topology, as shown in 図 39. Any mismatch in the stray capacitance associated with the NMOS and PMOS causes an output level change whenever the switch is opened or closed.

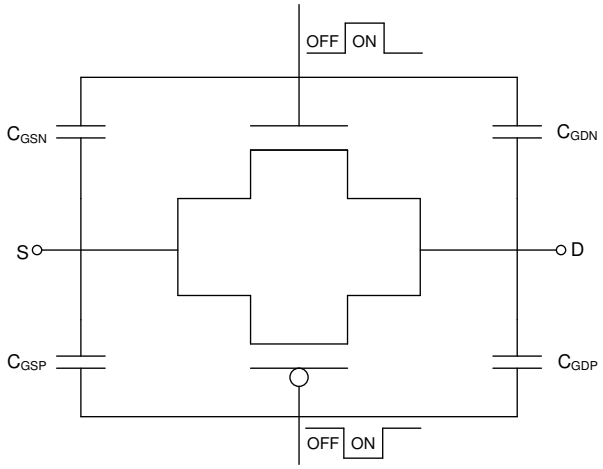


図 39. Transmission Gate Topology

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Feature Description (continued)

The MUX36xxx have special charge-injection cancellation circuitry that reduces the source-to-drain charge injection to as low as 0.3 pC at V_S = 0 V, and ±0.6 pC in the full signal range, as shown in 図 40.

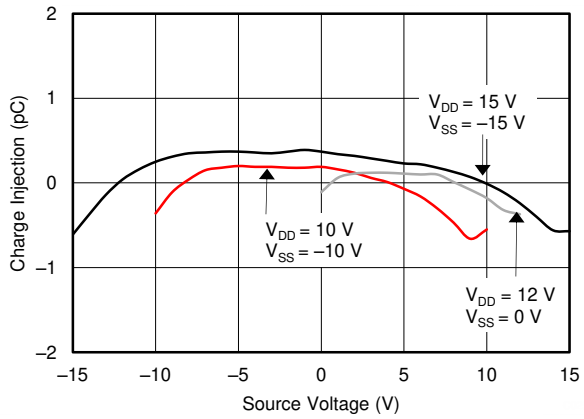


図 40. Source-to-Drain Charge Injection vs Source or Drain Voltage

The drain-to-source charge injection becomes important when the device is used as a demultiplexer (demux), where D becomes the input and Sx becomes the output. 図 41 shows the drain-to-source charge injection across the full signal range.

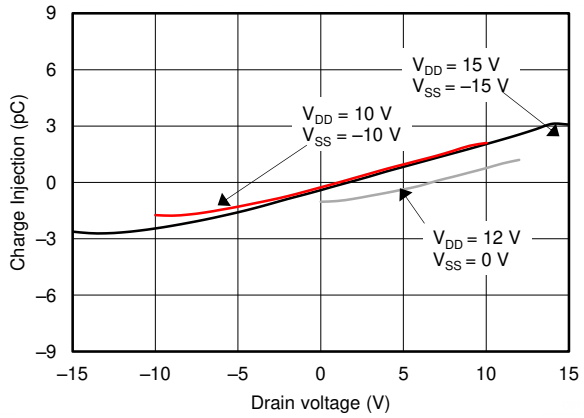


図 41. Drain-to-Source Charge Injection vs Source or Drain Voltage

10.3.3 Bidirectional Operation

The MUX36xxx are operable as both a mux and demux. The source (Sx, SxA, SxB) and drain (D, DA, DB) pins of the MUX36xxx are used either as input or output. Each MUX36xxx channel has very similar characteristics in both directions.

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Feature Description (continued)

10.3.4 Rail-to-Rail Operation

The valid analog signal for the MUX36xxx ranges from V_{SS} to V_{DD}. The input signal to the MUX36xxx swings from V_{SS} to V_{DD} without any significant degradation in performance. The on-resistance of the MUX36xxx varies with input signal, as shown in 図 42

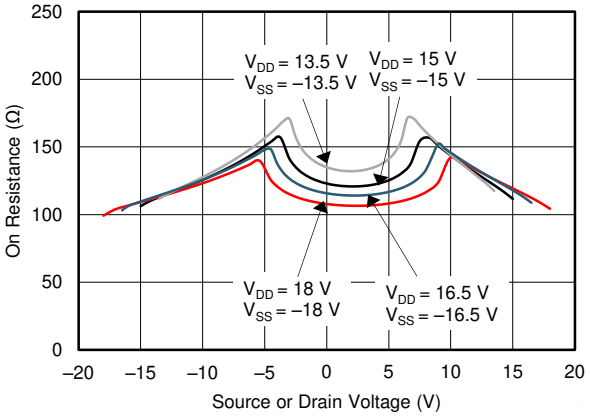


図 42. On-Resistance vs Source or Drain Voltage

10.4 Device Functional Modes

When the EN pin of the MUX36xxx is pulled high, one of the switches is closed based on the state of the address lines. When the EN pin is pulled low, all the switches are in an open state irrespective of the state of the address lines. The EN pin can be connected to V_{DD} (as high as 36 V).

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11 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

11.1 Application Information

The MUX36xxx family offers outstanding input/output leakage currents and ultralow charge injection. These devices operate up to 36 V, and offer true rail-to-rail input and output. The on-capacitance of the MUX36xxx is very low. These features makes the MUX36xxx a family of precision, robust, high-performance analog multiplexer for high-voltage, industrial applications.

11.2 Typical Application

図 43 shows a 16-bit, differential, 4-channel, multiplexed, data-acquisition system. This example is typical in industrial applications that require low distortion and a high-voltage differential input. The circuit uses the ADS8864, a 16-bit, 400-kSPS successive-approximation-resistor (SAR) analog-to-digital converter (ADC), along with a precision, high-voltage, signal-conditioning front end, and a 4-channel differential mux. This TI Precision Design details the process for optimizing the precision, high-voltage, front-end drive circuit using the MUX36D04, OPA192 and OPA140 to achieve excellent dynamic performance and linearity with the ADS8864.

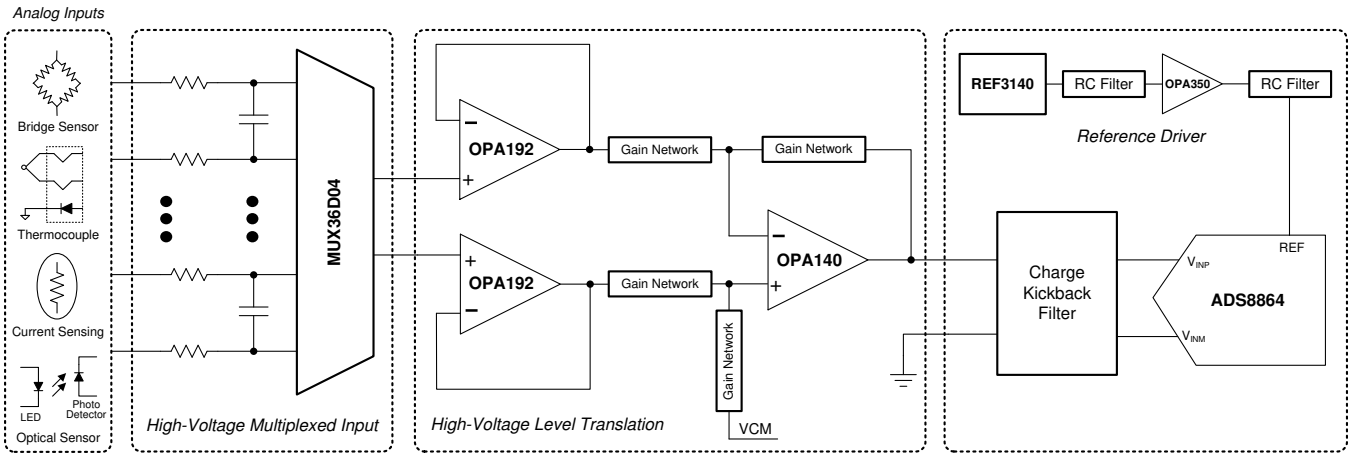


図 43. 16-Bit Precision Multiplexed Data-Acquisition System for High-Voltage Inputs With Lowest Distortion

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Typical Application (continued)

11.2.1 Design Requirements

The primary objective is to design a ±20 V, differential, 4-channel, multiplexed, data-acquisition system with lowest distortion using the 16-bit ADS8864 at a throughput of 400 kSPS for a 10-kHz, full-scale, pure, sine-wave input. The design requirements for this block design are:

- System supply voltage: ±15 V
- ADC supply voltage: 3.3 V
- ADC sampling rate: 400 kSPS
- ADC reference voltage (REFP): 4.096 V
- System input signal: A high-voltage differential input signal with a peak amplitude of 20 V and frequency (f_{IN}) of 10 kHz are applied to each differential input of the mux.

11.2.2 Detailed Design Procedure

The purpose of this precision design is to design an optimal, high-voltage, multiplexed, data-acquisition system for highest system linearity and fast settling. The overall system block diagram is illustrated in 図 43. The circuit is a multichannel, data-acquisition signal chain consisting of an input low-pass filter, mux, mux output buffer, attenuating SAR ADC driver, and the reference driver. The architecture allows fast sampling of multiple channels using a single ADC, providing a low-cost solution. This design systematically approaches each analog circuit block to achieve a 16-bit settling for a full-scale input stage voltage and linearity for a 10-kHz sinusoidal input signal at each input channel.

TI Precision Designs

For step-by-step design procedure, circuit schematics, bill of materials, PCB files, simulation results, and test results, refer to TI Precision Design TIPD151, *16-Bit, 400-kSPS, 4-Channel Multiplexed Data-Acquisition System for High-Voltage Inputs with Lowest Distortion*.

11.2.3 Application Curve

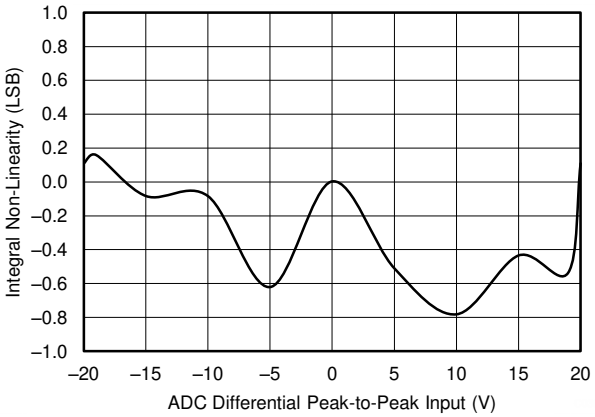


図 44. ADC 16-Bit Linearity Error for the Multiplexed Data-Acquisition Block

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12 Power Supply Recommendations

The MUX36xxx operates across a wide supply range of ±5 V to ±18 V (10 V to 36 V in single-supply mode). They also perform well with unsymmetric supplies such as V_{DD} = 12 V and V_{SS}= –5 V. For reliable operation, use a supply decoupling capacitor ranging between 0.1 µF to 10 µF at both the VDD and VSS pins to ground.

The on-resistance of the MUX36xxx varies with supply voltage, as illustrated in 図 45

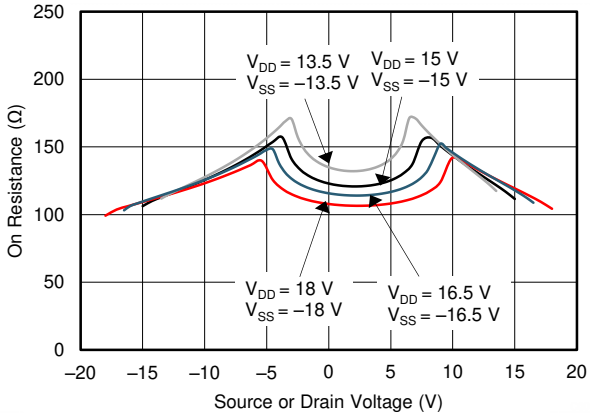


図 45. On-Resistance Variation With Supply and Input Voltage

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13 Layout

13.1 Layout Guidelines

図 46 illustrates an example of a PCB layout with the MUX36S08IPW, and 図 47 illustrates an example of a PCB layout with MUX36D04IPW.

Some key considerations are:

1. Decouple the VDD and VSS pins with a 0.1-µF capacitor, placed as close to the pin as possible. Make sure that the capacitor voltage rating is sufficient for the V_{DD} and V_{SS} supplies.
2. Keep the input lines as short as possible. In case of the differential signal, make sure the A inputs and B inputs are as symmetric as possible.
3. Use a solid ground plane to help distribute heat and reduce electromagnetic interference (EMI) noise pickup.
4. Do not run sensitive analog traces in parallel with digital traces. Avoid crossing digital and analog traces if possible, and only make perpendicular crossings when necessary.

13.2 Layout Example

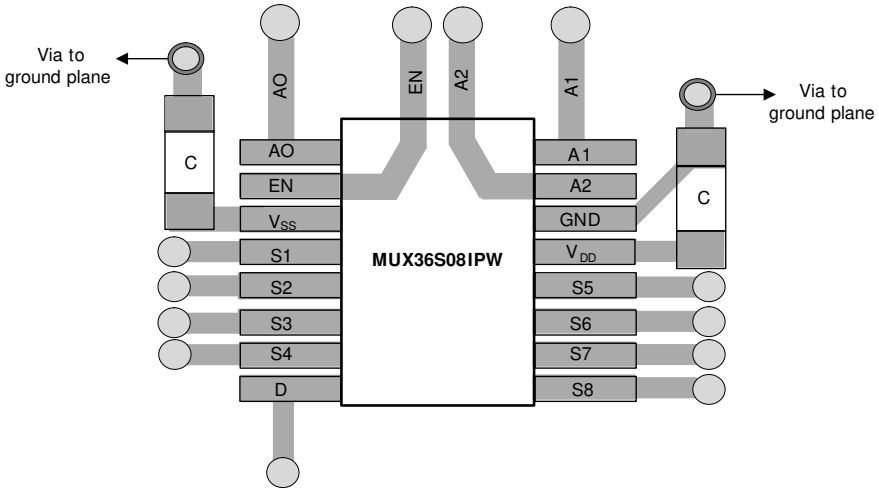


図 46. MUX36S08IPW Layout Example

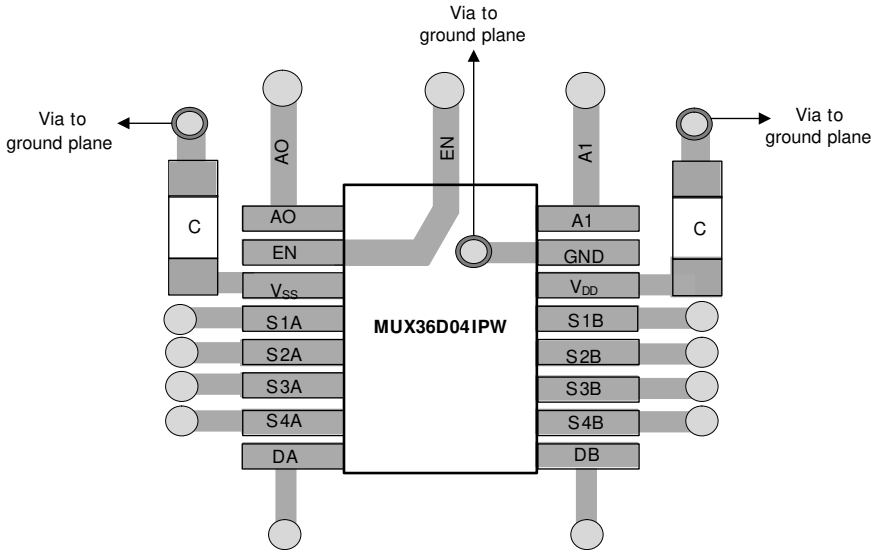


図 47. MUX36D04IPW Layout Example

14 デバイスおよびドキュメントのサポート

14.1 ドキュメントのサポート

14.1.1 関連資料

- 『ADS8664 12ビット、500kSPS、4および8チャネル、シングル電源、バイポーラ入力範囲のSAR ADC』(SBAS492)
- 『OPA140 高精度、低ノイズ、レール・ツー・レール出力、11MHz JFETオペアンプ』(SBOS498)
- 『OPA192　36V、高精度、レール・ツー・レール入力/出力、低オフセット電圧、低入力バイアス電流、e-trim™搭載のオペアンプ』(SBOS620)

14.2 関連リンク

表 3 に、クイック・アクセス・リンクの一覧を示します。カテゴリには、技術資料、サポートおよびコミュニティ・リソース、ツールとソフトウェア、およびサンプル注文またはご購入へのクイック・アクセスが含まれます。

表 3. 関連リンク

製品	プロダクト・フォルダ	ご注文はこちら	技術資料	ツールとソフトウェア	サポートとコミュニティ
MUX36S08	ここをクリック	ここをクリック	ここをクリック	ここをクリック	ここをクリック
MUX36D04	ここをクリック	ここをクリック	ここをクリック	ここをクリック	ここをクリック

14.3 ドキュメントの更新通知を受け取る方法

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14.4 コミュニティ・リソース

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

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静電気放電はわずかな性能の低下から完全なデバイスの故障に至るまで、様々な損傷を与えます。高精度の集積回路は、損傷に対して敏感であり、極めてわずかなパラメータの変化により、デバイスに規定された仕様に適合しなくなる場合があります。

14.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

15 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。これらの情報は、指定のデバイスに対して提供されている最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
MUX36D04IPW	Active	Production	TSSOP (PW) | 16	90 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	MUXD04C
MUX36D04IPW.B	Active	Production	TSSOP (PW) | 16	90 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	MUXD04C
MUX36D04IPWR	Active	Production	TSSOP (PW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	MUXD04C
MUX36D04IPWR.B	Active	Production	TSSOP (PW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	MUXD04C
MUX36D04IPWRG4	Active	Production	TSSOP (PW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	MUXD04C
MUX36D04IPWRG4.B	Active	Production	TSSOP (PW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	MUXD04C
MUX36D04IRRJR	Active	Production	WQFN (RRJ) | 16	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	MUX 36D04
MUX36D04IRRJR.B	Active	Production	WQFN (RRJ) | 16	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	MUX 36D04
MUX36D04IRUMR	Active	Production	WQFN (RUM) | 16	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	MUX 36D04
MUX36D04IRUMR.B	Active	Production	WQFN (RUM) | 16	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	MUX 36D04
MUX36D04IRUMRG4	Active	Production	WQFN (RUM) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	MUX 36D04
MUX36D04IRUMRG4.B	Active	Production	WQFN (RUM) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	MUX 36D04
MUX36S08IPW	Active	Production	TSSOP (PW) | 16	90 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	MUXS08B
MUX36S08IPW.B	Active	Production	TSSOP (PW) | 16	90 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	MUXS08B
MUX36S08IPWR	Active	Production	TSSOP (PW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	MUXS08B
MUX36S08IPWR.B	Active	Production	TSSOP (PW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	MUXS08B
MUX36S08IPWRG4	Active	Production	TSSOP (PW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	MUXS08B
MUX36S08IPWRG4.B	Active	Production	TSSOP (PW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	MUXS08B
MUX36S08IRRJR	Active	Production	WQFN (RRJ) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	MUX 36S08
MUX36S08IRRJR.B	Active	Production	WQFN (RRJ) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	MUX 36S08
MUX36S08IRUMR	Active	Production	WQFN (RUM) | 16	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	MUX 36S08
MUX36S08IRUMR.B	Active	Production	WQFN (RUM) | 16	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	MUX 36S08

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

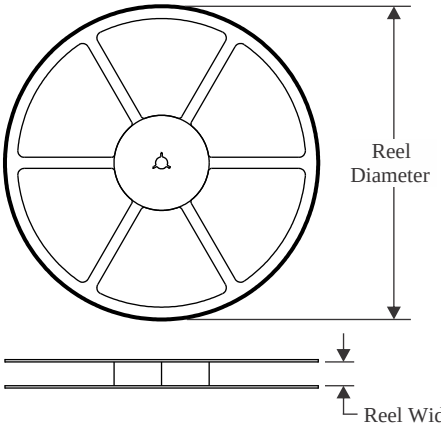
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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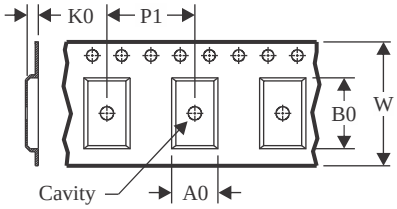
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

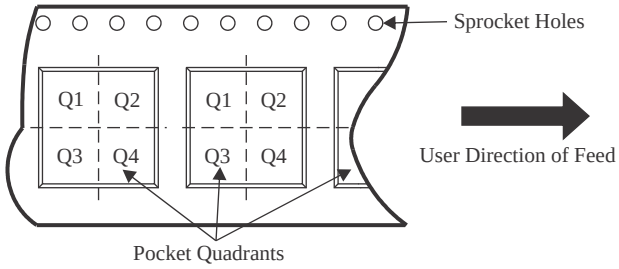


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

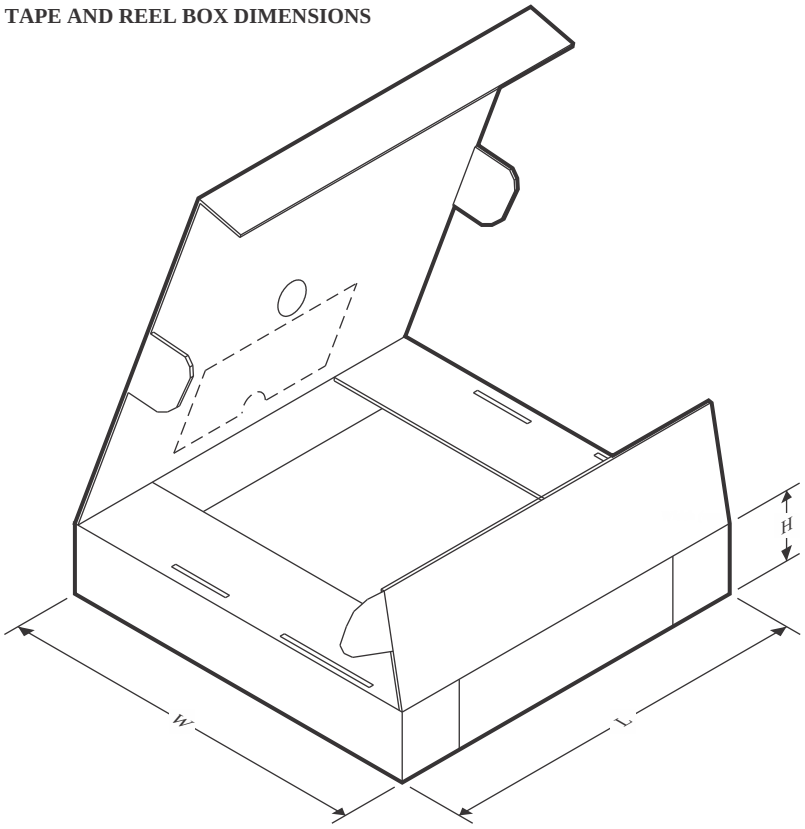
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
MUX36D04IPWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
MUX36D04IPWRG4	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
MUX36D04IRRJR	WQFN	RRJ	16	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
MUX36D04IRUMR	WQFN	RUM	16	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
MUX36D04IRUMRG4	WQFN	RUM	16	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
MUX36S08IPWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
MUX36S08IPWRG4	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
MUX36S08IRRJR	WQFN	RRJ	16	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
MUX36S08IRUMR	WQFN	RUM	16	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2

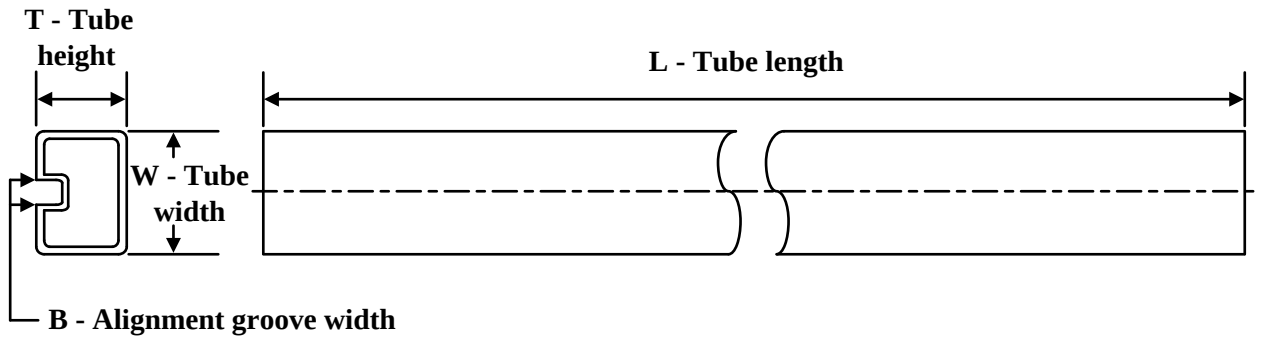
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
MUX36D04IPWR	TSSOP	PW	16	2000	353.0	353.0	32.0
MUX36D04IPWRG4	TSSOP	PW	16	2000	353.0	353.0	32.0
MUX36D04IRRJR	WQFN	RRJ	16	3000	360.0	360.0	36.0
MUX36D04IRUMR	WQFN	RUM	16	3000	360.0	360.0	36.0
MUX36D04IRUMRG4	WQFN	RUM	16	3000	367.0	367.0	35.0
MUX36S08IPWR	TSSOP	PW	16	2000	353.0	353.0	32.0
MUX36S08IPWRG4	TSSOP	PW	16	2000	353.0	353.0	32.0
MUX36S08IRRJR	WQFN	RRJ	16	3000	360.0	360.0	36.0
MUX36S08IRUMR	WQFN	RUM	16	3000	360.0	360.0	36.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
MUX36D04IPW	PW	TSSOP	16	90	530	10.2	3600	3.5
MUX36D04IPW.B	PW	TSSOP	16	90	530	10.2	3600	3.5
MUX36S08IPW	PW	TSSOP	16	90	530	10.2	3600	3.5
MUX36S08IPW.B	PW	TSSOP	16	90	530	10.2	3600	3.5

GENERIC PACKAGE VIEW

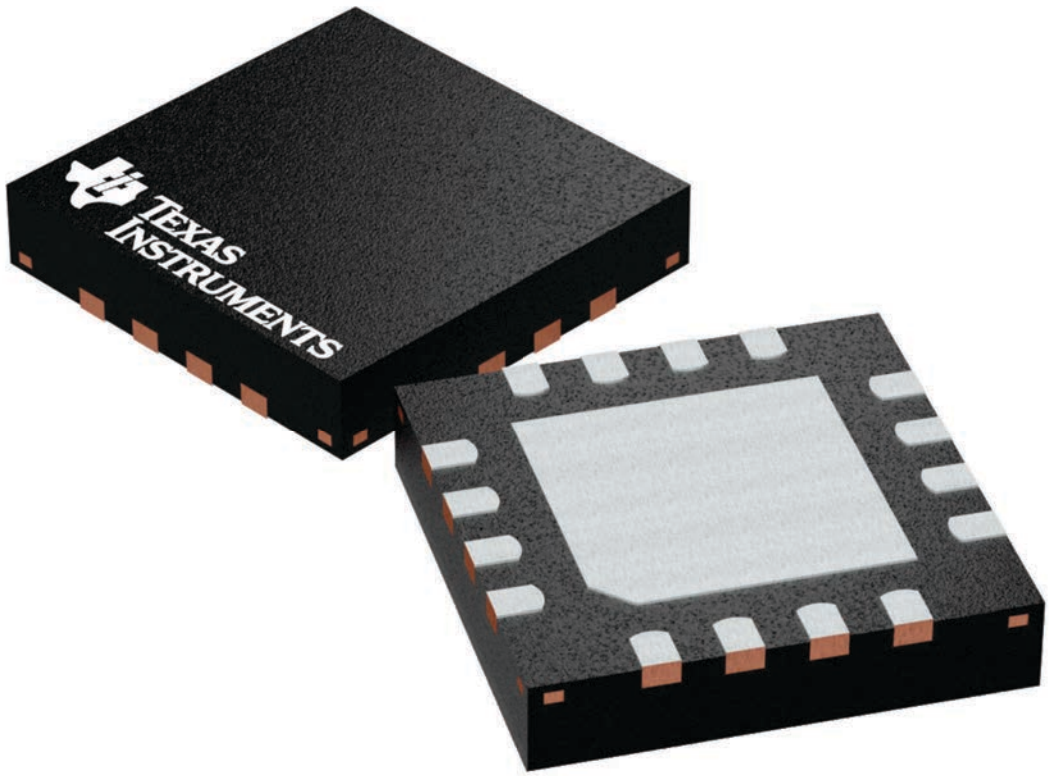
RUM 16

WQFN - 0.8 mm max height

4 x 4, 0.65 mm pitch

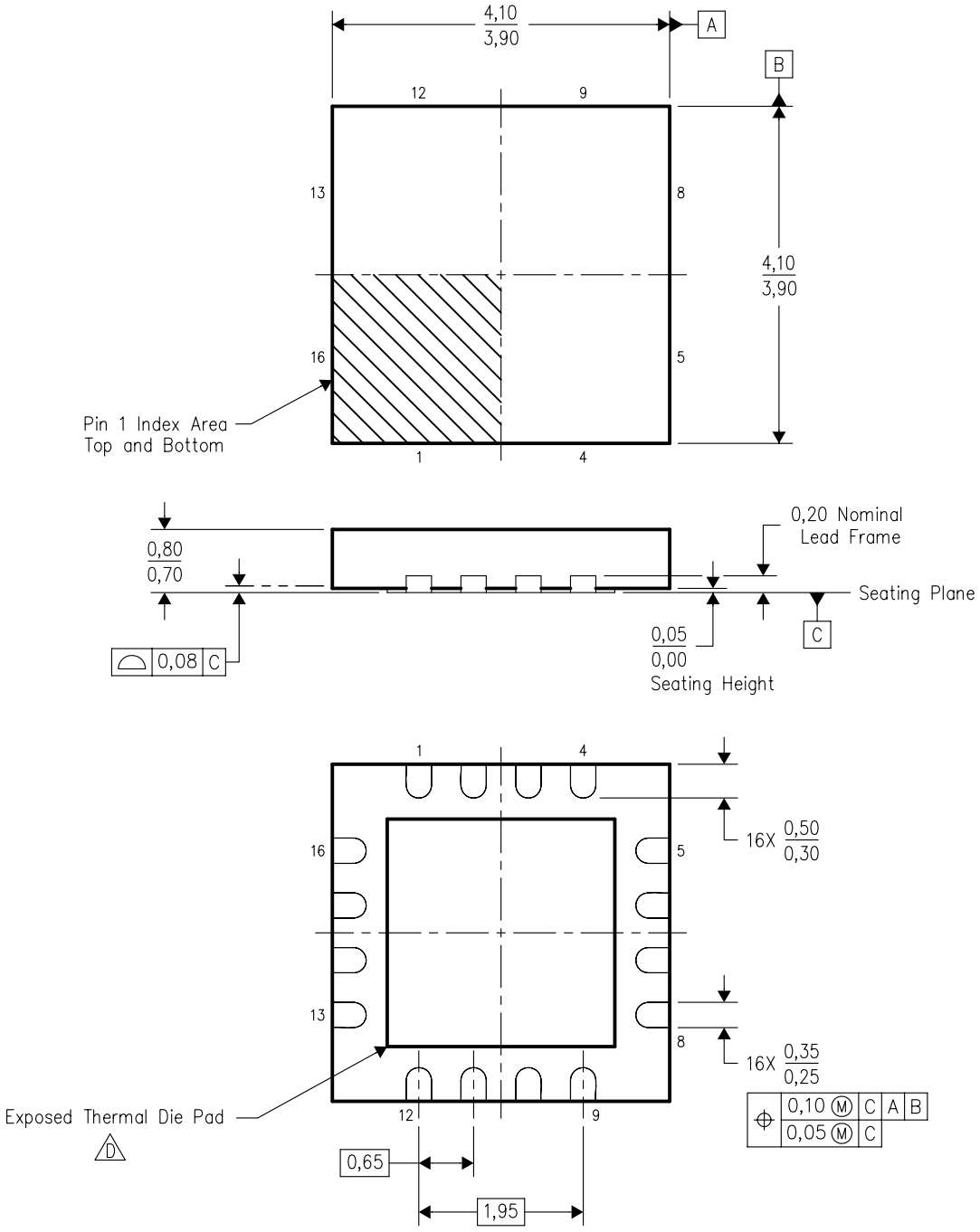
PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4224843/A

RUM (S–PQFP–N16) PLASTIC QUAD FLATPACK



4209092/A 10/2007

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
E. Package complies to JEDEC MO–220 variation WGGC–3.

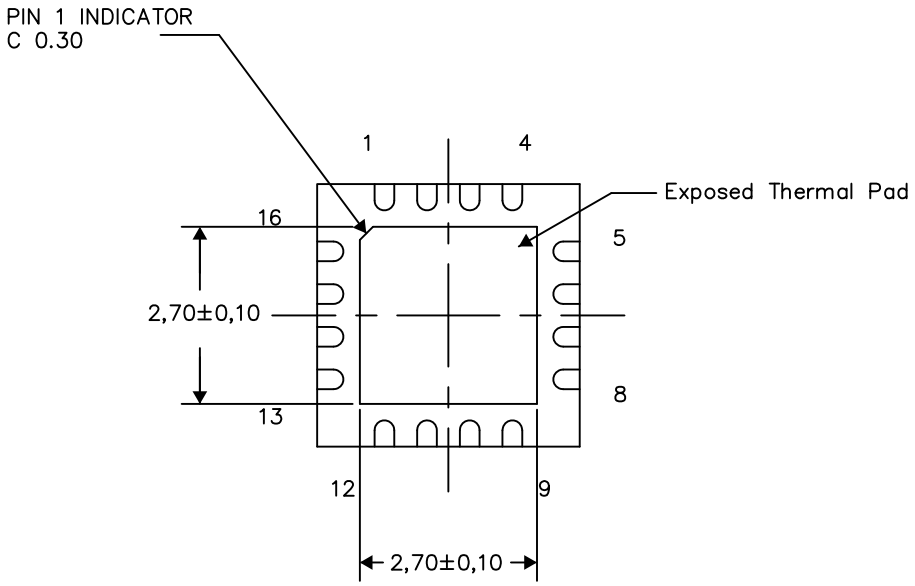
RUM (S–PWQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

Exposed Thermal Pad Dimensions

4209093–2/F 09/15

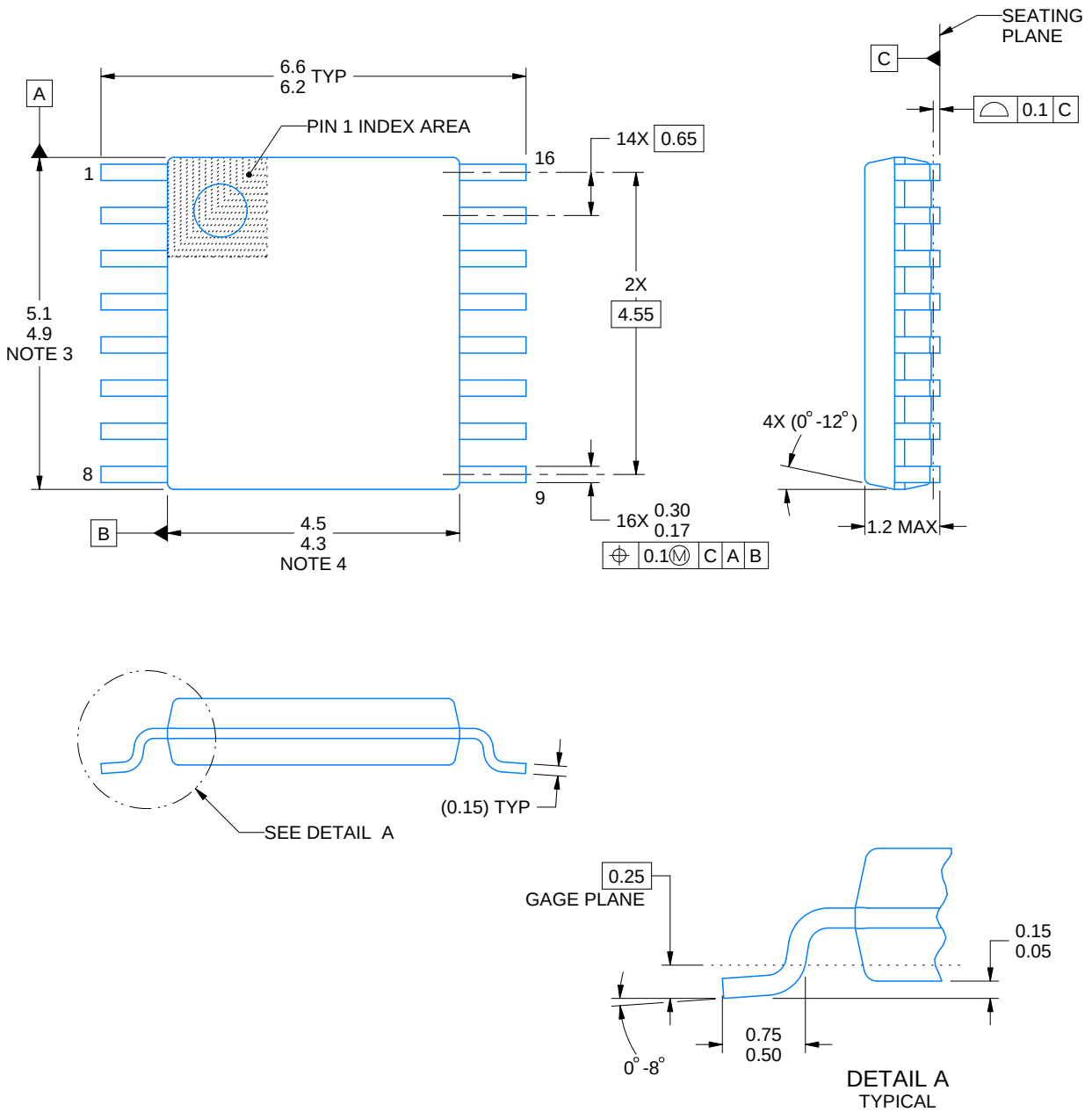
NOTES: All linear dimensions are in millimeters

PACKAGE OUTLINE

PW0016A

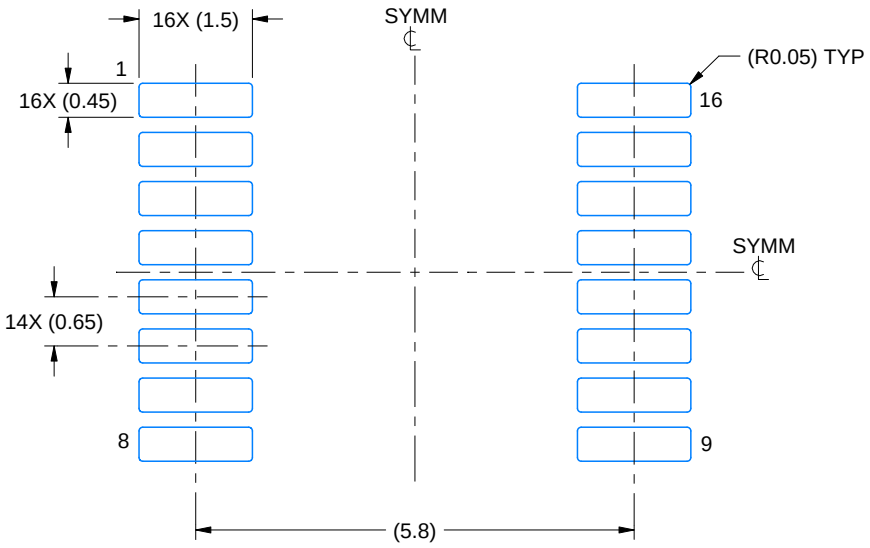
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

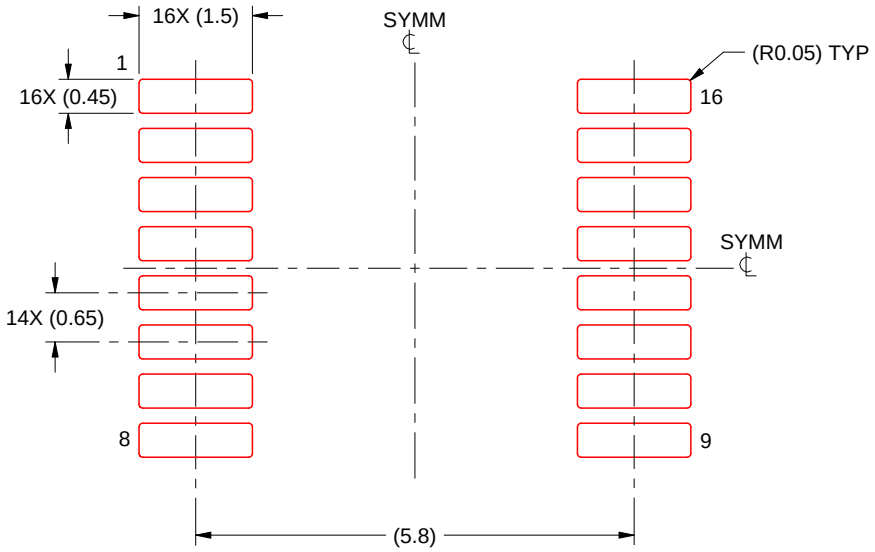


SOLDER MASK DETAILS

4220204/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220204/B 12/2023

NOTES: (continued)

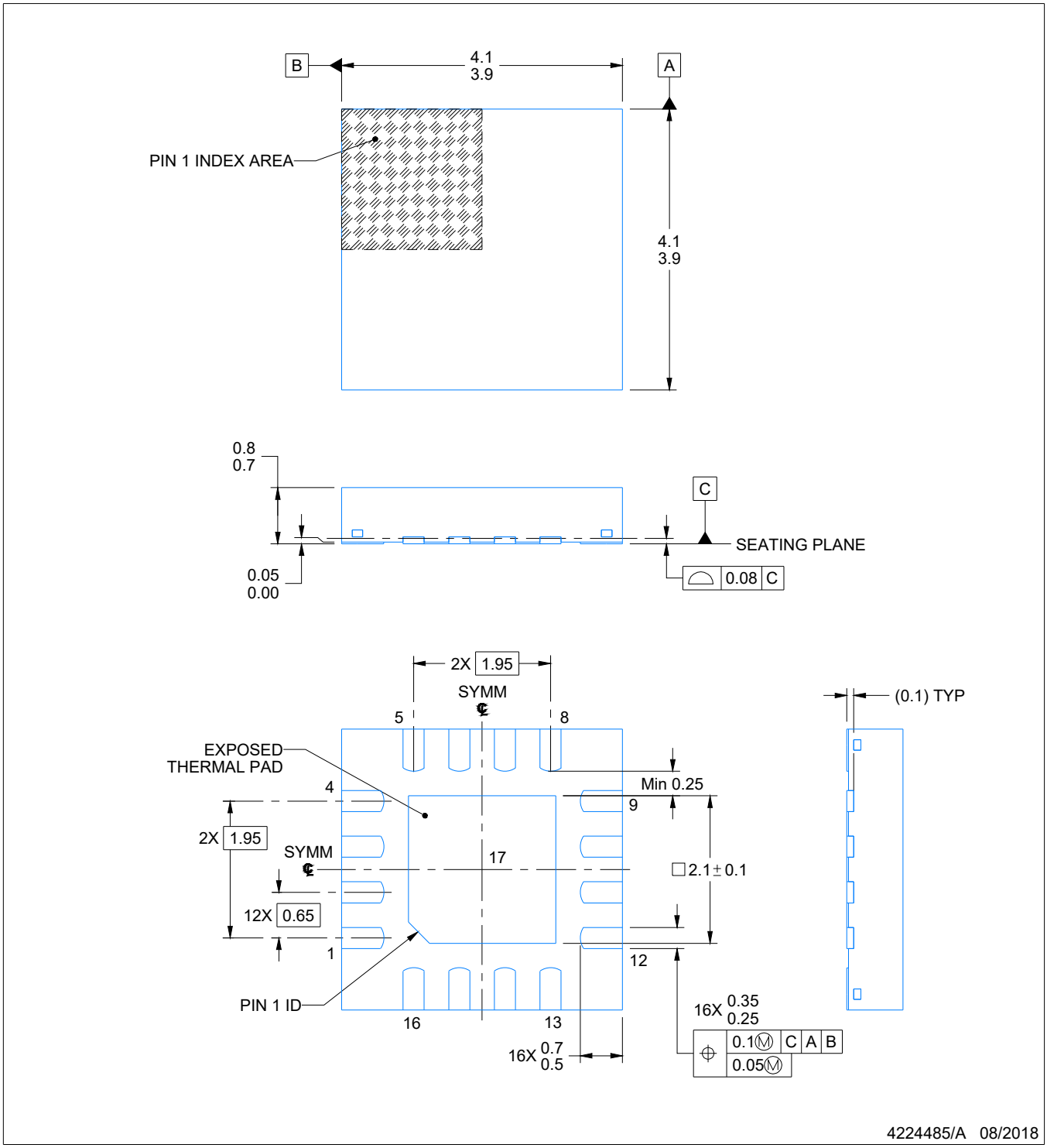
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

RRJ0016A

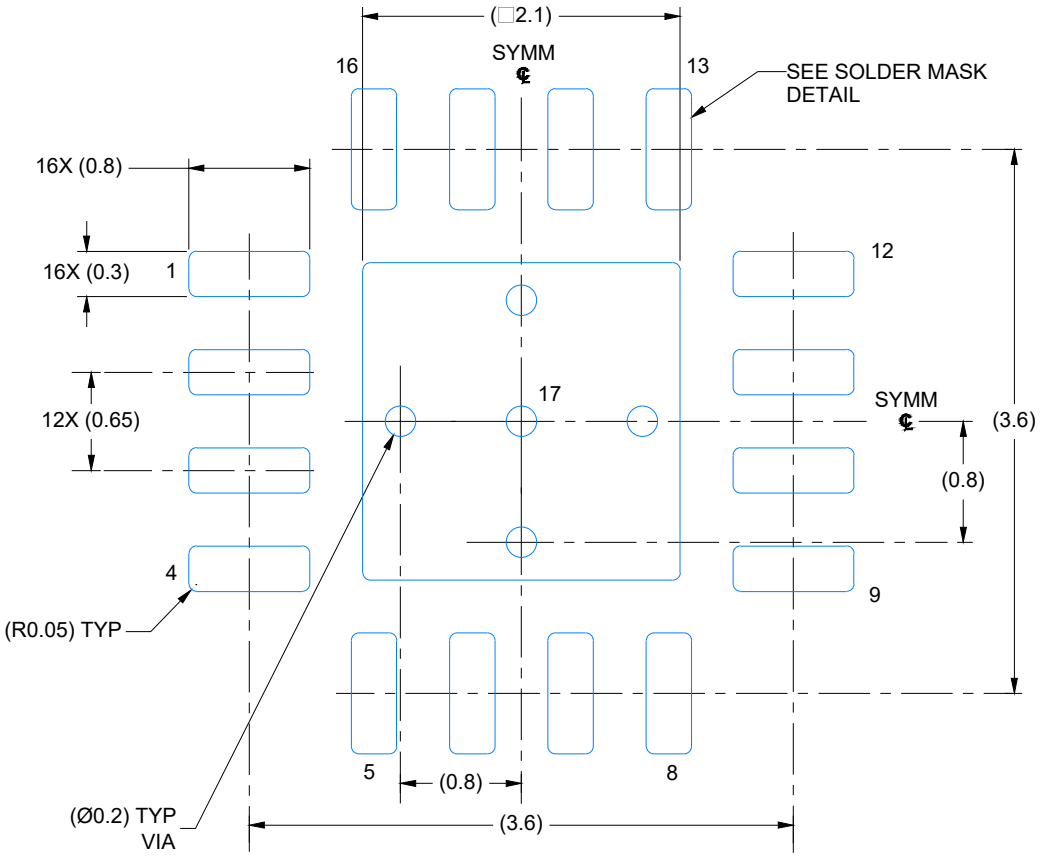
WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

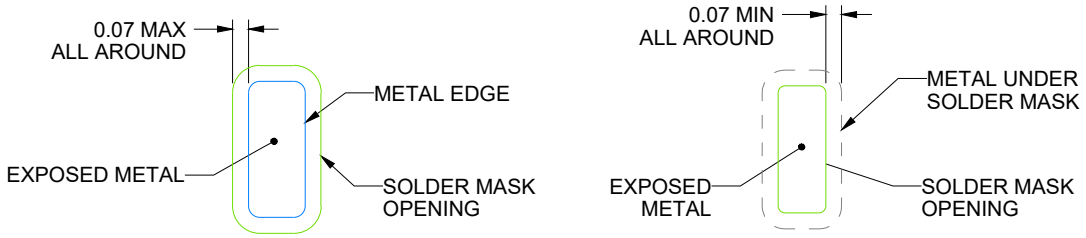


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X



NON SOLDER MASK DEFINED (PREFERRED)

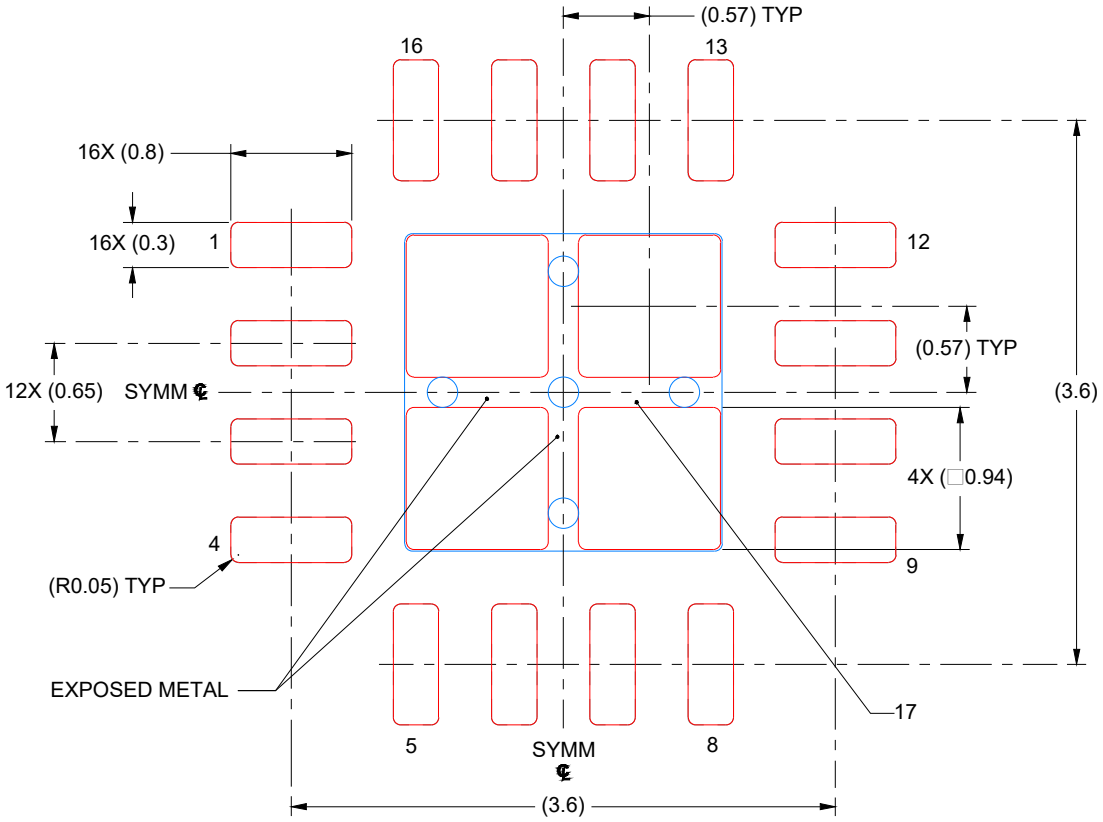
SOLDER MASK DEFINED

SOLDER MASK DETAILS

4224485/A 08/2018

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 20X

EXPOSED PAD 17
80% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

4224485/A 08/2018

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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最終更新日：2025 年 10 月