

# OPAx196 36V、低消費電力、低オフセット電圧、レール・ツー・レール・オペアンプ

## 1 特長

- 低いオフセット電圧:  $\pm 100\mu\text{V}$  (最大値)
- 低いオフセット電圧ドリフト係数:  $\pm 0.5\mu\text{V}/^\circ\text{C}$  (標準値)
- 低いバイアス電流:  $\pm 5\text{pA}$  (標準値)
- 高い同相除去: 140dB
- 低ノイズ: 1kHz時に  $15\text{nV}/\sqrt{\text{Hz}}$
- レール・ツー・レール入出力
- 差動入力電圧範囲は電源レールまで
- 広い帯域幅: 2.5MHz GBW
- 低い静止電流: アンプごとに  $140\mu\text{A}$  (標準値)
- 広い電源電圧範囲:  $\pm 2.25\text{V} \sim \pm 18\text{V}$ ,  $4.5\text{V} \sim 36\text{V}$
- EMIおよびRFIフィルタ入力
- 高い容量性負荷駆動能力: 1nF
- 業界標準パッケージ
  - シングル: SOIC-8, SOT-5, VSSOP-8
  - デュアル: SOIC-8, VSSOP-8
  - クワッド: SOIC-14, TSSOP-14, QFN-16

## 2 アプリケーション

- 多重化データ収集システム
- テストおよび計測機器
- 高分解能のADCドライバ・アンプ
- SAR ADCリファレンス・バッファ
- アナログ入出力モジュール
- ハイサイドおよびローサイドの電流センシング
- 高精度コンパレータ
- 医療用計測機器

## 3 概要

OPAx196ファミリ(OPA196、OPA2196、OPA4196)は新世代の36V、レール・ツー・レール e-trim™ オペアンプです。

これらのデバイスは、非常に低いオフセット電圧(標準値 $\pm 25\mu\text{V}$ )とドリフト係数(標準値 $\pm 0.5\mu\text{V}/^\circ\text{C}$ )、低いバイアス電流(標準値 $\pm 5\text{pA}$ )を特長とし、静止電流も出力範囲の全体にわたって非常に低い値(チャンネルごとに標準値 $140\mu\text{A}$ )です。

電源レールまでの差動入力電圧範囲、高い出力電流( $\pm 65\text{mA}$ )、1nFまでの高い容量性負荷の駆動といった独自の特長により、OPAx196は高電圧の産業用アプリケーションに適した堅牢で高性能なオペアンプです。

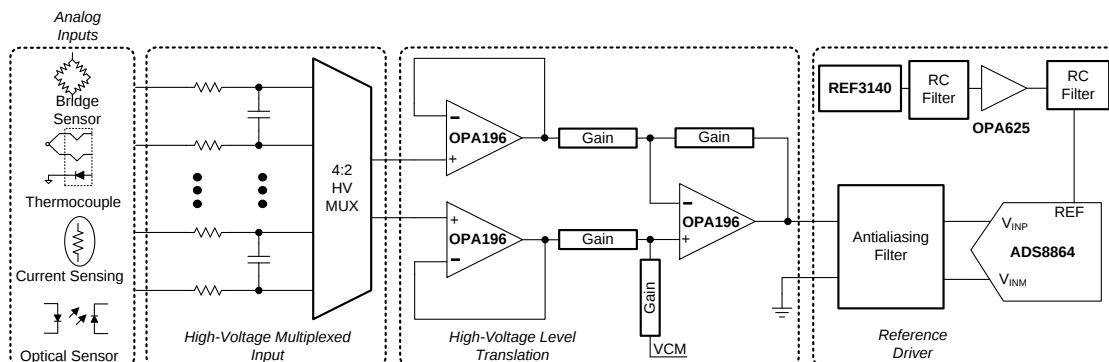
OPAx196ファミリのオペアンプは、標準のパッケージで供給され、 $-40^\circ\text{C} \sim +125^\circ\text{C}$ で動作が規定されています。

### 製品情報<sup>(1)</sup>

| 型番      | パッケージ      | 本体サイズ(公称)     |
|---------|------------|---------------|
| OPA196  | SOIC (8)   | 4.90mm×3.90mm |
|         | SOT (5)    | 2.90mm×1.60mm |
|         | VSSOP (8)  | 3.00mm×3.00mm |
| OPA2196 | SOIC (8)   | 4.90mm×3.90mm |
|         | VSSOP (8)  | 3.00mm×3.00mm |
| OPA4196 | SOIC (14)  | 8.65mm×3.90mm |
|         | TSSOP (14) | 5.00mm×4.40mm |

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にあるパッケージ・オプションについての付録を参照してください。

### 高電圧の多重化データ収集システムにおけるOPA196



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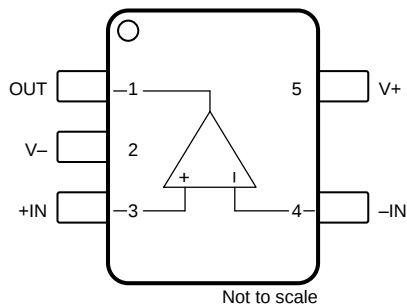
## 4 改訂履歴

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

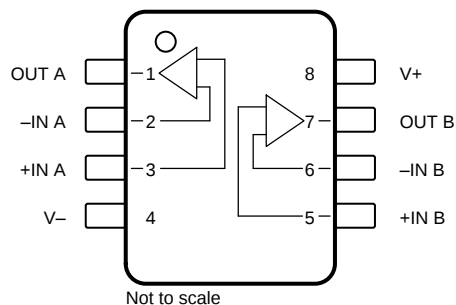
| 日付      | 改訂内容 | 注  |
|---------|------|----|
| 2017年7月 | *    | 初版 |

## 5 Pin Configuration and Functions

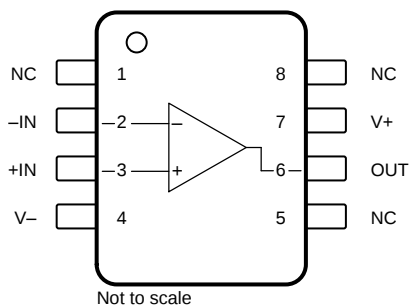
**DBV Package: OPA196**  
**5-Pin SOT**  
**Top View**



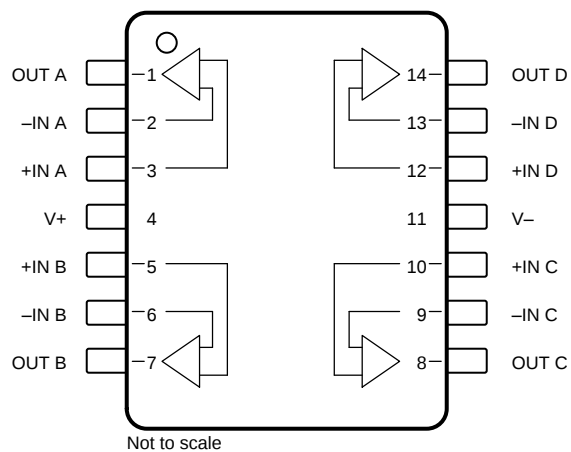
**D and DGK Packages: OPA2196**  
**8-Pin SOIC and VSSOP**  
**Top View**



**D and DGK Packages: OPA196**  
**8-Pin SOIC and VSSOP**  
**Top View**



**D and PW Packages: OPA4196**  
**14-Pin SOIC and TSSOP**  
**Top View**



(1) NC = No internal connection.

**Pin Functions: OPA196**

| PIN  |                          |           | I/O | DESCRIPTION                                   |
|------|--------------------------|-----------|-----|-----------------------------------------------|
| NAME | OPA196                   |           |     |                                               |
|      | D (SOIC),<br>DGK (VSSOP) | DBV (SOT) |     |                                               |
| +IN  | 3                        | 3         | I   | Noninverting input                            |
| −IN  | 2                        | 4         | I   | Inverting input                               |
| NC   | 1, 5, 8                  | —         | —   | No internal connection (can be left floating) |
| OUT  | 6                        | 1         | O   | Output                                        |
| V+   | 7                        | 5         | —   | Positive (highest) power supply               |
| V−   | 4                        | 2         | —   | Negative (lowest) power supply                |

**Pin Functions: OPA2196 and OPA4196**

| NAME  | PIN                      |                         | I/O | DESCRIPTION                     |
|-------|--------------------------|-------------------------|-----|---------------------------------|
|       | OPA2196                  | OPA4196                 |     |                                 |
|       | D (SOIC),<br>DGK (VSSOP) | D (SOIC),<br>PW (TSSOP) |     |                                 |
| +IN A | 3                        | 3                       | I   | Noninverting input, channel A   |
| +IN B | 5                        | 5                       | I   | Noninverting input, channel B   |
| +IN C | —                        | 10                      | I   | Noninverting input, channel C   |
| +IN D | —                        | 12                      | I   | Noninverting input, channel D   |
| –IN A | 2                        | 2                       | I   | Inverting input, channel A      |
| –IN B | 6                        | 6                       | I   | Inverting input, channel B      |
| –IN C | —                        | 9                       | I   | Inverting input, channel C      |
| –IN D | —                        | 13                      | I   | Inverting input, channel D      |
| OUT A | 1                        | 1                       | O   | Output, channel A               |
| OUT B | 7                        | 7                       | O   | Output, channel B               |
| OUT C | —                        | 8                       | O   | Output, channel C               |
| OUT D | —                        | 14                      | O   | Output, channel D               |
| V+    | 8                        | 4                       | —   | Positive (highest) power supply |
| V–    | 4                        | 11                      | —   | Negative (lowest) power supply  |

## 6 Specifications

### 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

|                                     |                    |              | MIN                         | MAX        | UNIT       |
|-------------------------------------|--------------------|--------------|-----------------------------|------------|------------|
| Supply voltage, $V_S = (V+) - (V-)$ |                    |              | ±20<br>(+40, single supply) |            | V          |
| Signal input pins                   | Voltage            | Common-mode  | (V-) – 0.5                  | (V+) + 0.5 | V          |
|                                     |                    | Differential | (V+) – (V-) + 0.2           |            |            |
|                                     | Current            |              | ±10                         |            | mA         |
| Output short circuit <sup>(2)</sup> |                    |              | Continuous                  | Continuous | Continuous |
| Temperature                         | Operating          |              | –40                         | 150        | °C         |
|                                     | Junction           |              | 150                         |            |            |
|                                     | Storage, $T_{stg}$ |              | –65                         | 150        |            |

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) Short-circuit to ground, one amplifier per package.

### 6.2 ESD Ratings

|             |                         |         |                                                                                | VALUE | UNIT |
|-------------|-------------------------|---------|--------------------------------------------------------------------------------|-------|------|
| $V_{(ESD)}$ | Electrostatic discharge | OPAx196 | Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>              | ±3000 | V    |
| $V_{(ESD)}$ | Electrostatic discharge | OPA196  | Charged-device model (CDM), per JEDEC specification JESD22-C101 <sup>(2)</sup> | ±1000 | V    |
|             |                         | OPA2196 |                                                                                | ±500  | V    |
|             |                         | OPA4196 |                                                                                | ±500  | V    |

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

|                                     | MIN         | NOM | MAX      | UNIT |
|-------------------------------------|-------------|-----|----------|------|
| Supply voltage, $V_S = (V+) - (V-)$ | 4.5 (±2.25) |     | 36 (±18) | V    |
| Specified temperature               | –40         |     | 125      | °C   |

### 6.4 Thermal Information: OPA196

| THERMAL METRIC <sup>(1)</sup> |                                              | OPA196   |             |           | UNIT |
|-------------------------------|----------------------------------------------|----------|-------------|-----------|------|
|                               |                                              | 8 PINS   |             | 5 PINS    |      |
|                               |                                              | D (SOIC) | DGK (VSSOP) | DBV (SOT) |      |
| $R_{\theta JA}$               | Junction-to-ambient thermal resistance       | 115.8    | 180.4       | 158.8     | °C/W |
| $R_{\theta JC(top)}$          | Junction-to-case(top) thermal resistance     | 60.1     | 67.9        | 60.7      | °C/W |
| $R_{\theta JB}$               | Junction-to-board thermal resistance         | 56.4     | 102.1       | 44.8      | °C/W |
| $\Psi_{JT}$                   | Junction-to-top characterization parameter   | 12.8     | 10.4        | 1.6       | °C/W |
| $\Psi_{JB}$                   | Junction-to-board characterization parameter | 55.9     | 100.3       | 4.2       | °C/W |
| $R_{\theta JC(bot)}$          | Junction-to-case(bottom) thermal resistance  | N/A      | N/A         | N/A       | °C/W |

- (1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

## 6.5 Thermal Information: OPA2196

| THERMAL METRIC <sup>(1)</sup> |                                              | OPA2196  |             | UNIT |
|-------------------------------|----------------------------------------------|----------|-------------|------|
|                               |                                              | 8 PINS   |             |      |
|                               |                                              | D (SOIC) | DGK (VSSOP) |      |
| R <sub>θJA</sub>              | Junction-to-ambient thermal resistance       | 107.9    | 158         | °C/W |
| R <sub>θJC(top)</sub>         | Junction-to-case(top) thermal resistance     | 53.9     | 48.6        | °C/W |
| R <sub>θJB</sub>              | Junction-to-board thermal resistance         | 48.9     | 78.7        | °C/W |
| Ψ <sub>JT</sub>               | Junction-to-top characterization parameter   | 6.6      | 3.9         | °C/W |
| Ψ <sub>JB</sub>               | Junction-to-board characterization parameter | 48.3     | 77.3        | °C/W |
| R <sub>θJC(bot)</sub>         | Junction-to-case(bottom) thermal resistance  | N/A      | N/A         | °C/W |

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

## 6.6 Thermal Information: OPA4196

| THERMAL METRIC <sup>(1)</sup> |                                              | OPA4196  |            | UNIT |
|-------------------------------|----------------------------------------------|----------|------------|------|
|                               |                                              | 14 PINS  |            |      |
|                               |                                              | D (SOIC) | PW (TSSOP) |      |
| R <sub>θJA</sub>              | Junction-to-ambient thermal resistance       | 86.4     | 92.6       | °C/W |
| R <sub>θJC(top)</sub>         | Junction-to-case(top) thermal resistance     | 46.3     | 27.5       | °C/W |
| R <sub>θJB</sub>              | Junction-to-board thermal resistance         | 41.0     | 33.6       | °C/W |
| Ψ <sub>JT</sub>               | Junction-to-top characterization parameter   | 11.3     | 1.9        | °C/W |
| Ψ <sub>JB</sub>               | Junction-to-board characterization parameter | 40.7     | 33.1       | °C/W |
| R <sub>θJC(bot)</sub>         | Junction-to-case(bottom) thermal resistance  | N/A      | N/A        | °C/W |

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

## 6.7 Electrical Characteristics: $V_S = \pm 4\text{ V}$ to $\pm 18\text{ V}$ ( $V_S = 8\text{ V}$ to $36\text{ V}$ )

at  $T_A = 25^\circ\text{C}$ ,  $V_{CM} = V_{OUT} = V_S / 2$ , and  $R_L = 10\text{ k}\Omega$  connected to  $V_S / 2$  (unless otherwise noted)

| PARAMETER            |                              | TEST CONDITIONS                                                                                    |                                  | MIN                                           | TYP        | MAX        | UNIT                     |
|----------------------|------------------------------|----------------------------------------------------------------------------------------------------|----------------------------------|-----------------------------------------------|------------|------------|--------------------------|
| OFFSET VOLTAGE       |                              |                                                                                                    |                                  |                                               |            |            |                          |
| V <sub>OS</sub>      | Input offset voltage         | V <sub>S</sub> = ±18 V                                                                             |                                  |                                               | ±25        | ±100       | μV                       |
|                      |                              | (V+) – 3.0 V < V <sub>CM</sub> < (V+) – 1.5 V                                                      |                                  | See <a href="#">Common-Mode Voltage Range</a> |            |            |                          |
|                      |                              | V <sub>S</sub> = ±18 V,<br>V <sub>CM</sub> = (V+) – 1.5 V                                          |                                  |                                               | ±25        | ±100       |                          |
| dV <sub>OS</sub> /dT | Input offset voltage drift   | V <sub>S</sub> = ±18 V, V <sub>CM</sub> = (V+) – 3 V                                               | T <sub>A</sub> = –40°C to +125°C |                                               | ±0.5       |            | μV/°C                    |
|                      |                              | V <sub>S</sub> = ±18 V, V <sub>CM</sub> = (V+) – 1.5 V                                             |                                  |                                               | ±0.8       |            |                          |
| PSRR                 | Power-supply rejection ratio | T <sub>A</sub> = –40°C to +125°C                                                                   |                                  |                                               | ±0.3       | ±1         | μV/V                     |
| INPUT BIAS CURRENT   |                              |                                                                                                    |                                  |                                               |            |            |                          |
| I <sub>B</sub>       | Input bias current           |                                                                                                    |                                  |                                               | ±5         | ±20        | pA                       |
| I <sub>OS</sub>      | Input offset current         |                                                                                                    |                                  |                                               | ±2         | ±20        | pA                       |
| NOISE                |                              |                                                                                                    |                                  |                                               |            |            |                          |
| E <sub>n</sub>       | Input voltage noise          | (V–) – 0.1 V < V <sub>CM</sub> < (V+) – 3 V                                                        | f = 0.1 Hz to 10 Hz              |                                               | 1.4        |            | μV <sub>PP</sub>         |
|                      |                              | (V+) – 1.5 V < V <sub>CM</sub> < (V+) + 0.1 V                                                      | f = 0.1 Hz to 10 Hz              |                                               | 7          |            |                          |
| e <sub>n</sub>       | Input voltage noise density  | (V–) – 0.1 V < V <sub>CM</sub> < (V+) – 3 V                                                        | f = 100 Hz                       |                                               | 18         |            | nV/√Hz                   |
|                      |                              |                                                                                                    | f = 1 kHz                        |                                               | 15         |            |                          |
|                      |                              | (V+) – 1.5 V < V <sub>CM</sub> < (V+) + 0.1 V                                                      | f = 100 Hz                       |                                               | 53         |            |                          |
|                      |                              |                                                                                                    | f = 1 kHz                        |                                               | 24         |            |                          |
| i <sub>n</sub>       | Input current noise density  | f = 1 kHz                                                                                          |                                  |                                               | 1.5        |            | fA/√Hz                   |
| INPUT VOLTAGE        |                              |                                                                                                    |                                  |                                               |            |            |                          |
| V <sub>CM</sub>      | Common-mode voltage range    |                                                                                                    |                                  | (V–) – 0.1                                    |            | (V+) + 0.1 | V                        |
| CMRR                 | Common-mode rejection ratio  | V <sub>S</sub> = ±18 V,<br>(V–) – 0.1 V < V <sub>CM</sub> < (V+) – 3 V                             |                                  | 120                                           | 140        |            | dB                       |
|                      |                              | V <sub>S</sub> = ±18 V,<br>(V–) < V <sub>CM</sub> < (V+) – 3 V                                     | T <sub>A</sub> = –40°C to +125°C | 114                                           | 126        |            |                          |
|                      |                              | V <sub>S</sub> = ±18 V,<br>(V+) – 1.5 V < V <sub>CM</sub> < (V+)                                   |                                  | 96                                            | 120        |            |                          |
|                      |                              |                                                                                                    | T <sub>A</sub> = –40°C to +125°C | 86                                            | 100        |            |                          |
|                      |                              | (V+) – 3 V < V <sub>CM</sub> < (V+) – 1.5 V                                                        |                                  | See <a href="#">Typical Characteristics</a>   |            |            |                          |
| INPUT IMPEDANCE      |                              |                                                                                                    |                                  |                                               |            |            |                          |
| Z <sub>ID</sub>      | Differential                 |                                                                                                    |                                  |                                               | 100    1.6 |            | MΩ    pF                 |
| Z <sub>IC</sub>      | Common-mode                  |                                                                                                    |                                  |                                               | 1    6.4   |            | 10 <sup>13</sup> Ω    pF |
| OPEN-LOOP GAIN       |                              |                                                                                                    |                                  |                                               |            |            |                          |
| A <sub>OL</sub>      | Open-loop voltage gain       | V <sub>S</sub> = ±18 V,<br>(V–) + 0.6 V < V <sub>O</sub> < (V+) – 0.6 V,<br>R <sub>L</sub> = 2 kΩ  |                                  | 124                                           | 134        |            | dB                       |
|                      |                              |                                                                                                    | T <sub>A</sub> = –40°C to +125°C | 114                                           | 126        |            |                          |
|                      |                              | V <sub>S</sub> = ±18 V,<br>(V–) + 0.3 V < V <sub>O</sub> < (V+) – 0.3 V,<br>R <sub>L</sub> = 10 kΩ |                                  | 126                                           | 140        |            |                          |
|                      |                              |                                                                                                    | T <sub>A</sub> = –40°C to +125°C | 120                                           | 134        |            |                          |

**Electrical Characteristics:  $V_S = \pm 4\text{ V}$  to  $\pm 18\text{ V}$  ( $V_S = 8\text{ V}$  to  $36\text{ V}$ ) (continued)**

 at  $T_A = 25^\circ\text{C}$ ,  $V_{CM} = V_{OUT} = V_S / 2$ , and  $R_L = 10\text{ k}\Omega$  connected to  $V_S / 2$  (unless otherwise noted)

| PARAMETER          |                                   | TEST CONDITIONS                                                         |                                                   | MIN                                         | TYP | MAX | UNIT             |
|--------------------|-----------------------------------|-------------------------------------------------------------------------|---------------------------------------------------|---------------------------------------------|-----|-----|------------------|
| FREQUENCY RESPONSE |                                   |                                                                         |                                                   |                                             |     |     |                  |
| GBW                | Unity gain bandwidth              |                                                                         |                                                   | 2.5                                         |     |     | MHz              |
| SR                 | Slew rate                         | $V_S = \pm 18\text{ V}$ , $G = 1$ , 10-V step                           | Rising                                            | 7.5                                         |     |     | V/ $\mu\text{s}$ |
|                    |                                   |                                                                         | Falling                                           | 5.5                                         |     |     |                  |
| $t_s$              | Settling time                     | $T_O 0.01\%$ , $C_L = 20\text{ pF}$                                     | $V_S = \pm 18\text{ V}$ , $G = 1$ , 2-V step      | 0.7                                         |     |     | $\mu\text{s}$    |
|                    |                                   |                                                                         | $V_S = \pm 18\text{ V}$ , $G = 1$ , 5-V step      | 1                                           |     |     |                  |
|                    |                                   | $T_O 0.001\%$ , $C_L = 20\text{ pF}$                                    | $V_S = \pm 18\text{ V}$ , $G = 1$ , 2-V step      | 1.8                                         |     |     |                  |
|                    |                                   |                                                                         | $V_S = \pm 18\text{ V}$ , $G = 1$ , 5-V step      | 3.7                                         |     |     |                  |
| $t_{OR}$           | Overload recovery time            | $V_{IN} \times G = V_S$                                                 | From overload to negative rail                    | 0.4                                         |     |     | $\mu\text{s}$    |
|                    |                                   |                                                                         | From overload to positive rail                    | 1                                           |     |     |                  |
| THD+N              | Total harmonic distortion + noise | $G = 1$ , $f = 1\text{ kHz}$ , $V_O = 3.5\text{ V}_{RMS}$               |                                                   | 0.0012%                                     |     |     |                  |
|                    | Crosstalk                         | OPA2196 and OPA4196, at dc                                              |                                                   | 150                                         |     |     | dB               |
|                    |                                   | OPA2196 and OPA4196, $f = 100\text{ kHz}$                               |                                                   | 130                                         |     |     | dB               |
| OUTPUT             |                                   |                                                                         |                                                   |                                             |     |     |                  |
| $V_O$              | Voltage output swing from rail    | Positive rail                                                           | No load                                           | 5                                           |     | 15  | mV               |
|                    |                                   |                                                                         | $R_L = 10\text{ k}\Omega$                         | 50                                          |     | 110 |                  |
|                    |                                   |                                                                         | $R_L = 2\text{ k}\Omega$                          | 200                                         |     | 500 |                  |
|                    |                                   | Negative rail                                                           | No load                                           | 5                                           |     | 15  |                  |
|                    |                                   |                                                                         | $R_L = 10\text{ k}\Omega$                         | 50                                          |     | 110 |                  |
|                    |                                   |                                                                         | $R_L = 2\text{ k}\Omega$                          | 200                                         |     | 500 |                  |
| $I_{SC}$           | Short-circuit current             | $V_S = \pm 18\text{ V}$                                                 |                                                   | $\pm 65$                                    |     |     | mA               |
| $C_L$              | Capacitive load drive             |                                                                         |                                                   | See <a href="#">Typical Characteristics</a> |     |     |                  |
| $Z_O$              | Open-loop output impedance        | $f = 1\text{ MHz}$ , $I_O = 0\text{ A}$ , See <a href="#">Figure 19</a> |                                                   | 700                                         |     |     | $\Omega$         |
| POWER SUPPLY       |                                   |                                                                         |                                                   |                                             |     |     |                  |
| $I_Q$              | Quiescent current per amplifier   | $I_O = 0\text{ A}$                                                      |                                                   | 140                                         |     | 200 | $\mu\text{A}$    |
|                    |                                   |                                                                         | $T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$ |                                             |     | 250 |                  |
| TEMPERATURE        |                                   |                                                                         |                                                   |                                             |     |     |                  |
| Thermal protection |                                   |                                                                         |                                                   | 180                                         |     |     | $^\circ\text{C}$ |
| Thermal hysteresis |                                   |                                                                         |                                                   | 30                                          |     |     | $^\circ\text{C}$ |

## 6.8 Electrical Characteristics: $V_S = \pm 2.25\text{ V to } \pm 4\text{ V}$ ( $V_S = 4.5\text{ V to } 8\text{ V}$ )

at  $T_A = +25^\circ\text{C}$ ,  $V_{CM} = V_{OUT} = V_S / 2$ , and  $R_L = 10\text{ k}\Omega$  connected to  $V_S / 2$  (unless otherwise noted)

| PARAMETER            |                              | TEST CONDITIONS                                                                                     |                                  | MIN                                           | TYP        | MAX  | UNIT                     |
|----------------------|------------------------------|-----------------------------------------------------------------------------------------------------|----------------------------------|-----------------------------------------------|------------|------|--------------------------|
| OFFSET VOLTAGE       |                              |                                                                                                     |                                  |                                               |            |      |                          |
| V <sub>OS</sub>      | Input offset voltage         | V <sub>S</sub> = ±2.25V,<br>V <sub>CM</sub> = (V+) – 3 V                                            |                                  | ±25                                           |            | ±100 | μV                       |
|                      |                              | (V+) – 3.0 V < V <sub>CM</sub> < (V+) – 1.5 V                                                       |                                  | See <a href="#">Common-Mode Voltage Range</a> |            |      |                          |
|                      |                              | V <sub>S</sub> = ±3V,<br>V <sub>CM</sub> = (V+) – 1.5 V                                             |                                  | ±25                                           |            | ±100 |                          |
| dV <sub>OS</sub> /dT | Input offset voltage drift   | V <sub>S</sub> = ±2.25V, V <sub>CM</sub> = (V+) – 3 V                                               | T <sub>A</sub> = –40°C to +125°C | ±0.5                                          |            |      | μV/°C                    |
|                      |                              | V <sub>S</sub> = ±2.25V, V <sub>CM</sub> = (V+) – 1.5 V                                             |                                  | ±0.5                                          |            |      |                          |
| PSRR                 | Power-supply rejection ratio | T <sub>A</sub> = –40°C to +125°C, V <sub>CM</sub> = V <sub>S</sub> / 2 – 0.75 V                     |                                  | ±1                                            |            |      | μV/V                     |
| INPUT BIAS CURRENT   |                              |                                                                                                     |                                  |                                               |            |      |                          |
| I <sub>B</sub>       | Input bias current           |                                                                                                     |                                  | ±5                                            |            | ±20  | pA                       |
| I <sub>OS</sub>      | Input offset current         |                                                                                                     |                                  | ±2                                            |            | ±20  | pA                       |
| NOISE                |                              |                                                                                                     |                                  |                                               |            |      |                          |
| E <sub>n</sub>       | Input voltage noise          | (V–) – 0.1 V < V <sub>CM</sub> < (V+) – 3 V                                                         | f = 0.1 Hz to 10 Hz              | 1.4                                           |            |      | μV <sub>PP</sub>         |
|                      |                              | (V+) – 1.5 V < V <sub>CM</sub> < (V+) + 0.1 V                                                       | f = 0.1 Hz to 10 Hz              | 7                                             |            |      |                          |
| e <sub>n</sub>       | Input voltage noise density  | (V–) – 0.1 V < V <sub>CM</sub> < (V+) – 3 V                                                         | f = 100 Hz                       | 18                                            |            |      | nV/√Hz                   |
|                      |                              |                                                                                                     | f = 1 kHz                        | 15                                            |            |      |                          |
|                      |                              | (V+) – 1.5 V < V <sub>CM</sub> < (V+) + 0.1 V                                                       | f = 100 Hz                       | 53                                            |            |      |                          |
|                      |                              |                                                                                                     | f = 1 kHz                        | 24                                            |            |      |                          |
| i <sub>n</sub>       | Input current noise density  | f = 1 kHz                                                                                           |                                  | 1.5                                           |            |      | fA/√Hz                   |
| INPUT VOLTAGE        |                              |                                                                                                     |                                  |                                               |            |      |                          |
| V <sub>CM</sub>      | Common-mode voltage range    |                                                                                                     |                                  | (V–) – 0.1                                    | (V+) + 0.1 |      | V                        |
| CMRR                 | Common-mode rejection ratio  | V <sub>S</sub> = ±2.25 V,<br>(V–) – 0.1 V < V <sub>CM</sub> < (V+) – 3 V                            |                                  | 96                                            | 110        |      | dB                       |
|                      |                              | V <sub>S</sub> = ±2.25 V,<br>(V–) < V <sub>CM</sub> < (V+) – 3 V                                    | T <sub>A</sub> = –40°C to +125°C | 90                                            | 104        |      |                          |
|                      |                              | V <sub>S</sub> = ±2.25 V,<br>(V+) – 1.5 V < V <sub>CM</sub> < (V+)                                  | T <sub>A</sub> = –40°C to +125°C | 96                                            | 120        |      |                          |
|                      |                              |                                                                                                     |                                  | 84                                            | 100        |      |                          |
|                      |                              | (V+) – 3 V < V <sub>CM</sub> < (V+) – 1.5 V                                                         |                                  | See <a href="#">Typical Characteristics</a>   |            |      |                          |
| INPUT IMPEDANCE      |                              |                                                                                                     |                                  |                                               |            |      |                          |
| Z <sub>ID</sub>      | Differential                 |                                                                                                     |                                  | 100    1.6                                    |            |      | MΩ    pF                 |
| Z <sub>IC</sub>      | Common-mode                  |                                                                                                     |                                  | 1    6.4                                      |            |      | 10 <sup>13</sup> Ω    pF |
| OPEN-LOOP GAIN       |                              |                                                                                                     |                                  |                                               |            |      |                          |
| A <sub>OL</sub>      | Open-loop voltage gain       | V <sub>S</sub> = ±2.25V,<br>(V–) + 0.6 V < V <sub>O</sub> < (V+) – 0.6 V,<br>R <sub>L</sub> = 2 kΩ  |                                  | 110                                           | 120        |      | dB                       |
|                      |                              |                                                                                                     | T <sub>A</sub> = –40°C to +125°C | 100                                           | 114        |      |                          |
|                      |                              | V <sub>S</sub> = ±2.25V,<br>(V–) + 0.3 V < V <sub>O</sub> < (V+) – 0.3 V,<br>R <sub>L</sub> = 10 kΩ |                                  | 110                                           | 126        |      |                          |
|                      |                              |                                                                                                     | T <sub>A</sub> = –40°C to +125°C | 106                                           | 120        |      |                          |

**Electrical Characteristics:  $V_S = \pm 2.25\text{ V}$  to  $\pm 4\text{ V}$  ( $V_S = 4.5\text{ V}$  to  $8\text{ V}$ ) (continued)**

 at  $T_A = +25^\circ\text{C}$ ,  $V_{CM} = V_{OUT} = V_S / 2$ , and  $R_L = 10\text{ k}\Omega$  connected to  $V_S / 2$  (unless otherwise noted)

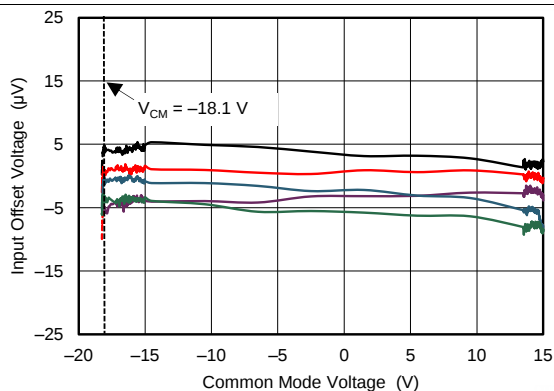
| PARAMETER          |                                 | TEST CONDITIONS                                                         |                                                   | MIN                                         | TYP | MAX | UNIT             |
|--------------------|---------------------------------|-------------------------------------------------------------------------|---------------------------------------------------|---------------------------------------------|-----|-----|------------------|
| FREQUENCY RESPONSE |                                 |                                                                         |                                                   |                                             |     |     |                  |
| GBW                | Unity gain bandwidth            |                                                                         |                                                   | 2.2                                         |     |     | MHz              |
| SR                 | Slew rate                       | $V_S = \pm 2.25\text{V}$ , $G = 1$ , 1-V step                           | Rising                                            | 6.5                                         |     |     | V/ $\mu\text{s}$ |
|                    |                                 |                                                                         | Falling                                           | 5.5                                         |     |     |                  |
| $t_{\text{OR}}$    | Overload recovery time          | $V_{\text{IN}} \times G = V_S$                                          | From overload to negative rail                    | 0.4                                         |     |     | $\mu\text{s}$    |
|                    |                                 |                                                                         | From overload to positive rail                    | 1                                           |     |     |                  |
|                    | Crosstalk                       | OPA2196 and OPA4196, at dc                                              |                                                   | 150                                         |     |     | dB               |
|                    |                                 | OPA2196 and OPA4196, $f = 100\text{ kHz}$                               |                                                   | 130                                         |     |     | dB               |
| OUTPUT             |                                 |                                                                         |                                                   |                                             |     |     |                  |
| $V_O$              | Voltage output swing from rail  | Positive rail                                                           | No load                                           | 5                                           | 15  |     | mV               |
|                    |                                 |                                                                         | $R_L = 10\text{ k}\Omega$                         | 15                                          | 110 |     |                  |
|                    |                                 |                                                                         | $R_L = 2\text{ k}\Omega$                          | 60                                          | 500 |     |                  |
|                    |                                 | Negative rail                                                           | No load                                           | 5                                           | 15  |     |                  |
|                    |                                 |                                                                         | $R_L = 10\text{ k}\Omega$                         | 15                                          | 110 |     |                  |
|                    |                                 |                                                                         | $R_L = 2\text{ k}\Omega$                          | 60                                          | 500 |     |                  |
| $I_{\text{SC}}$    | Short-circuit current           | $V_S = \pm 2.25\text{V}$                                                |                                                   | $\pm 30$                                    |     |     | mA               |
| $C_L$              | Capacitive load drive           |                                                                         |                                                   | See <a href="#">Typical Characteristics</a> |     |     |                  |
| $Z_O$              | Open-loop output impedance      | $f = 1\text{ MHz}$ , $I_O = 0\text{ A}$ , see <a href="#">Figure 19</a> |                                                   | 700                                         |     |     | $\Omega$         |
| POWER SUPPLY       |                                 |                                                                         |                                                   |                                             |     |     |                  |
| $I_Q$              | Quiescent current per amplifier | $I_O = 0\text{ A}$                                                      |                                                   | 140                                         | 200 |     | $\mu\text{A}$    |
|                    |                                 |                                                                         | $T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$ | 250                                         |     |     |                  |
| TEMPERATURE        |                                 |                                                                         |                                                   |                                             |     |     |                  |
|                    | Thermal protection              |                                                                         |                                                   | 180                                         |     |     | $^\circ\text{C}$ |
|                    | Thermal hysteresis              |                                                                         |                                                   | 30                                          |     |     | $^\circ\text{C}$ |

## 6.9 Typical Characteristics

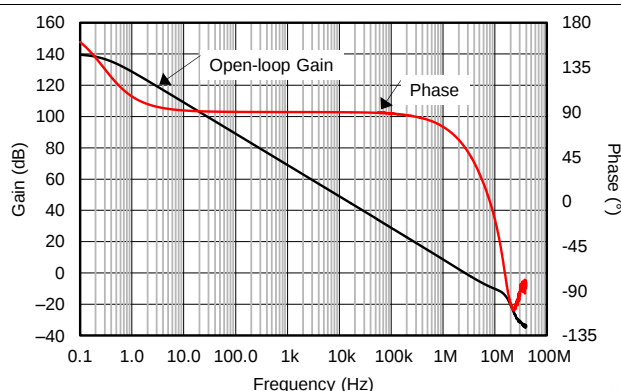
**Table 1. Table of Graphs**

| DESCRIPTION                                                    | FIGURE                                     |
|----------------------------------------------------------------|--------------------------------------------|
| Offset Voltage vs Common-Mode Voltage                          | Figure 1                                   |
| Open-Loop Gain and Phase vs Frequency                          | Figure 2                                   |
| Closed-Loop Gain and Phase vs Frequency                        | Figure 3                                   |
| Input Bias Current vs Common-Mode Voltage                      | Figure 4                                   |
| Input Bias Current vs Temperature                              | Figure 5                                   |
| Output Voltage Swing vs Output Current (maximum supply)        | Figure 6, Figure 7                         |
| CMRR and PSRR vs Frequency                                     | Figure 8                                   |
| CMRR vs Temperature                                            | Figure 9                                   |
| PSRR vs Temperature                                            | Figure 10                                  |
| 0.1-Hz to 10-Hz Noise                                          | Figure 11                                  |
| Input Voltage Noise Spectral Density vs Frequency              | Figure 12                                  |
| THD+N Ratio vs Frequency                                       | Figure 13                                  |
| THD+N vs Output Amplitude                                      | Figure 14                                  |
| Quiescent Current vs Supply Voltage                            | Figure 15                                  |
| Quiescent Current vs Temperature                               | Figure 16                                  |
| Open Loop Gain vs Temperature                                  | Figure 17, Figure 18                       |
| Open Loop Output Impedance vs Frequency                        | Figure 19                                  |
| Small Signal Overshoot vs Capacitive Load (100-mV output step) | Figure 20, Figure 21                       |
| No Phase Reversal                                              | Figure 22                                  |
| Overload Recovery                                              | Figure 23                                  |
| Small-Signal Step Response (100 mV)                            | Figure 24, Figure 25                       |
| Large-Signal Step Response                                     | Figure 26, Figure 27                       |
| Settling Time                                                  | Figure 28, Figure 29, Figure 30, Figure 31 |
| Short-Circuit Current vs Temperature                           | Figure 32                                  |
| Maximum Output Voltage vs Frequency                            | Figure 33                                  |
| Propagation Delay Rising Edge                                  | Figure 34                                  |
| Propagation Delay Falling Edge                                 | Figure 35                                  |

At  $T_A = 25^\circ\text{C}$ ,  $V_S = \pm 18\text{ V}$ ,  $V_{CM} = V_S / 2$ ,  $R_L = 10\text{ k}\Omega$  connected to  $V_S / 2$ , and  $C_L = 100\text{ pF}$ , unless otherwise noted.



**Figure 1. Offset Voltage vs Common-Mode Voltage**



**Figure 2. Open-Loop Gain and Phase vs Frequency**

At  $T_A = 25^\circ\text{C}$ ,  $V_S = \pm 18\text{ V}$ ,  $V_{CM} = V_S / 2$ ,  $R_L = 10\text{ k}\Omega$  connected to  $V_S / 2$ , and  $C_L = 100\text{ pF}$ , unless otherwise noted.

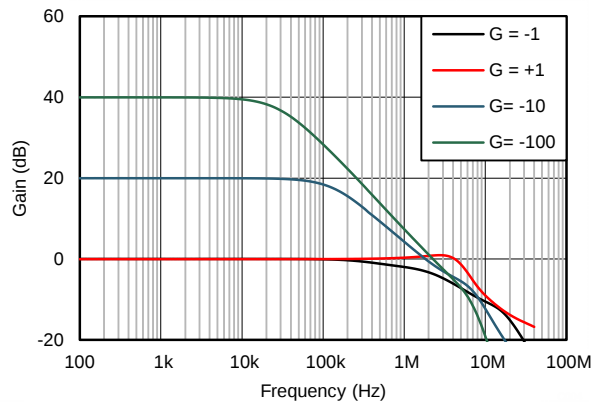


Figure 3. Closed-Loop Gain vs Frequency

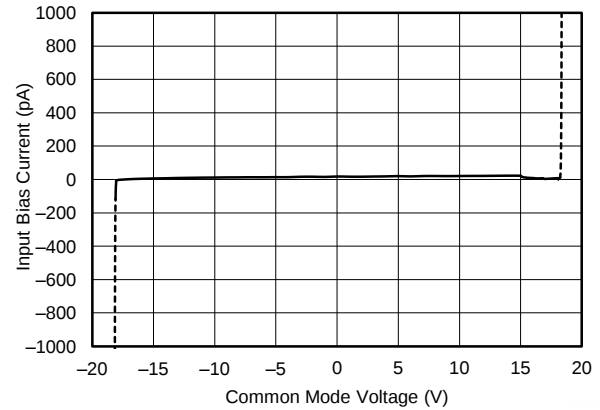


Figure 4. Input Bias Current vs Common-Mode Voltage

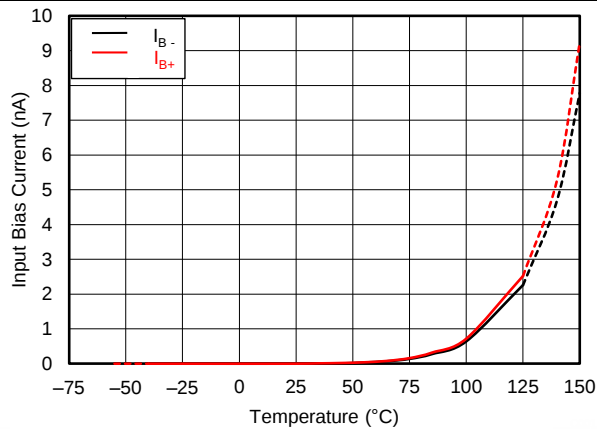


Figure 5. Input Bias Current vs Temperature

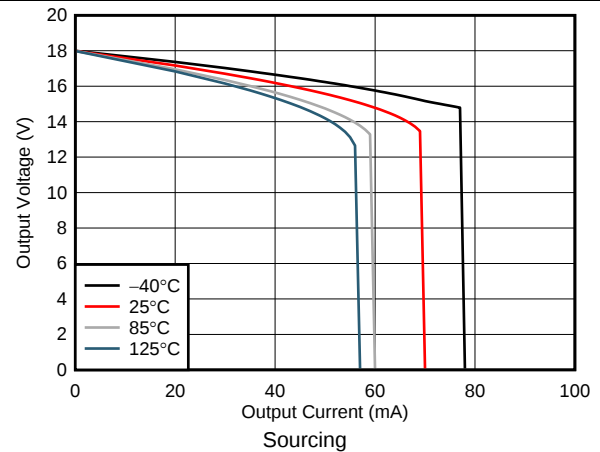


Figure 6. Output Voltage Swing vs Output Current

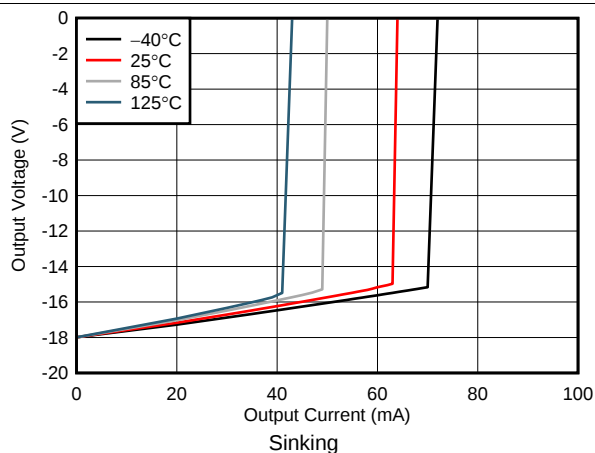


Figure 7. Output Voltage Swing vs Output Current

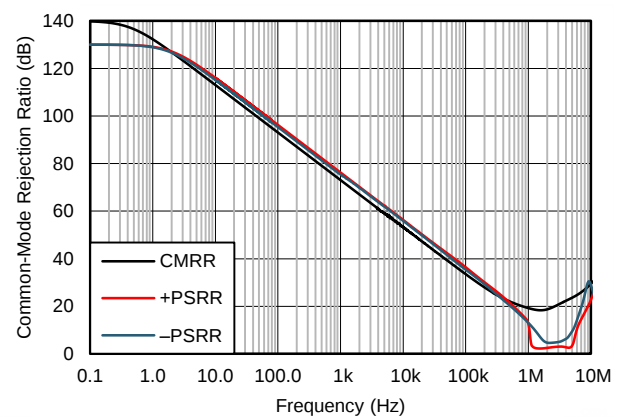
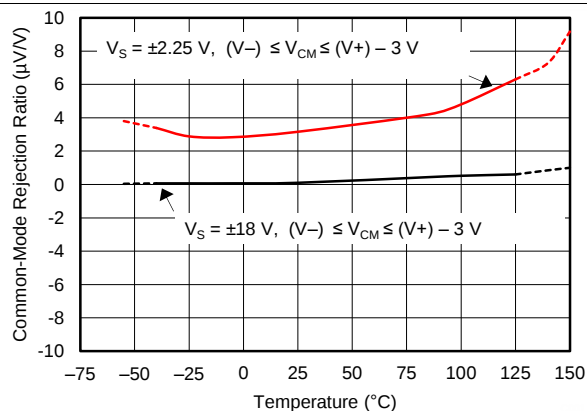
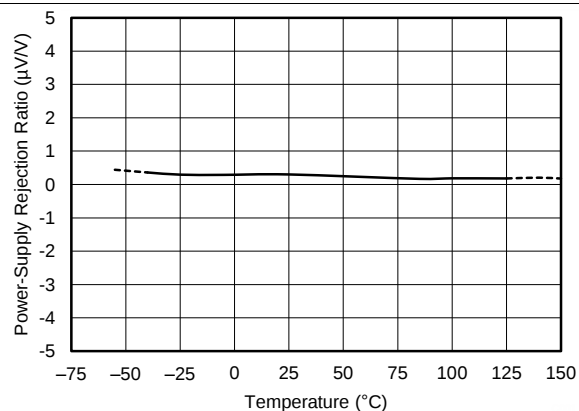


Figure 8. CMRR and PSRR vs Frequency

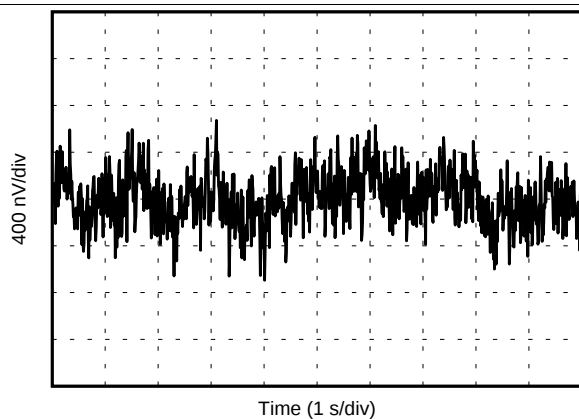
At  $T_A = 25^\circ\text{C}$ ,  $V_S = \pm 18\text{ V}$ ,  $V_{CM} = V_S / 2$ ,  $R_L = 10\text{ k}\Omega$  connected to  $V_S / 2$ , and  $C_L = 100\text{ pF}$ , unless otherwise noted.



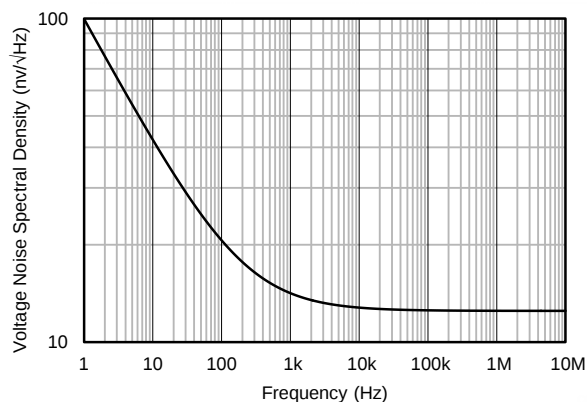
**Figure 9. CMRR vs Temperature**



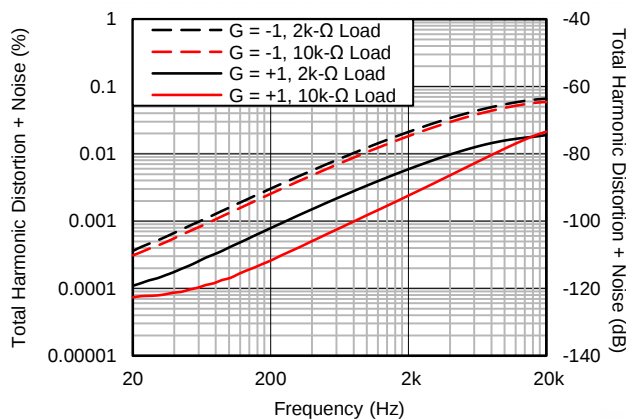
**Figure 10. PSRR vs Temperature**



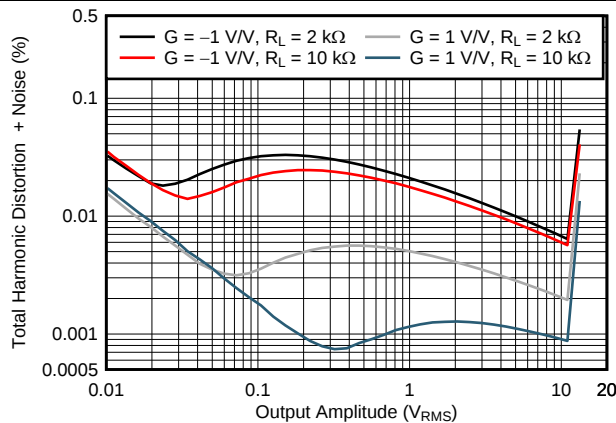
**Figure 11. 0.1-Hz to 10-Hz Noise**



**Figure 12. Input Voltage Noise Spectral Density vs Frequency**



**Figure 13. THD+N vs Frequency**



**Figure 14. THD+N vs Output Amplitude**

At  $T_A = 25^\circ\text{C}$ ,  $V_S = \pm 18\text{ V}$ ,  $V_{CM} = V_S / 2$ ,  $R_L = 10\text{ k}\Omega$  connected to  $V_S / 2$ , and  $C_L = 100\text{ pF}$ , unless otherwise noted.

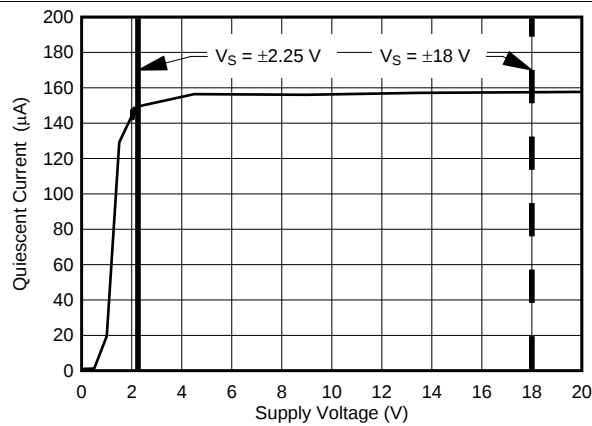


Figure 15. Quiescent Current vs Supply Voltage

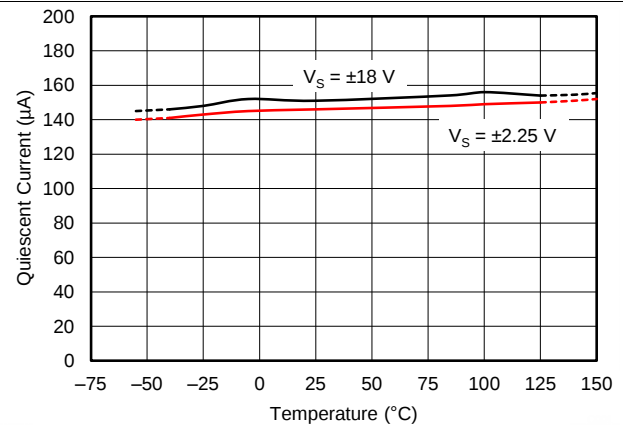


Figure 16. Quiescent Current vs Temperature

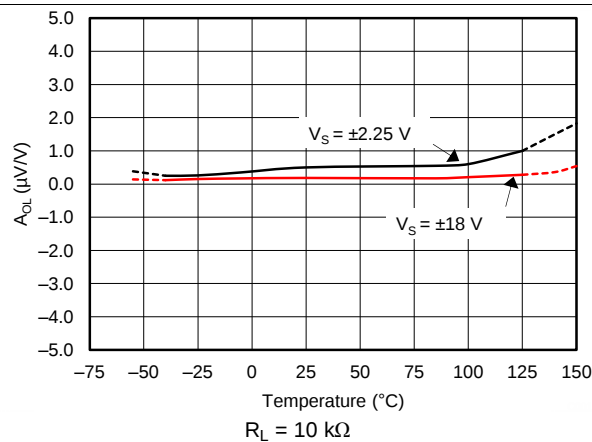


Figure 17. Open-Loop Gain vs Temperature

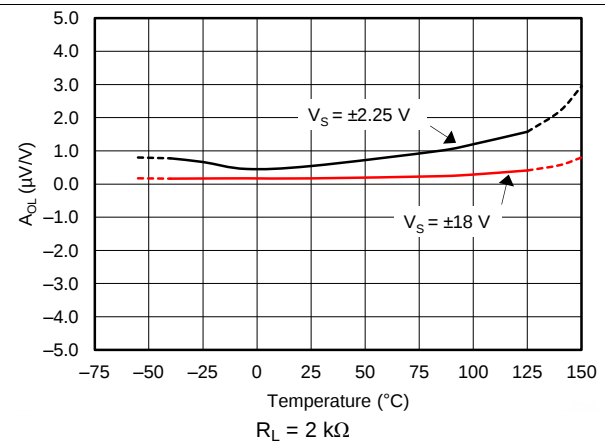


Figure 18. Open-Loop Gain vs Temperature

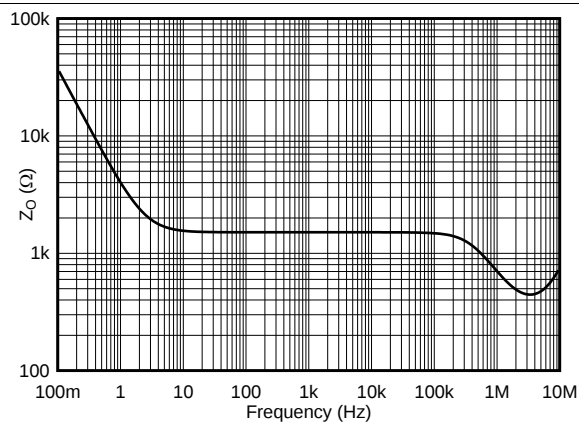


Figure 19. Open-Loop Output Impedance vs Frequency

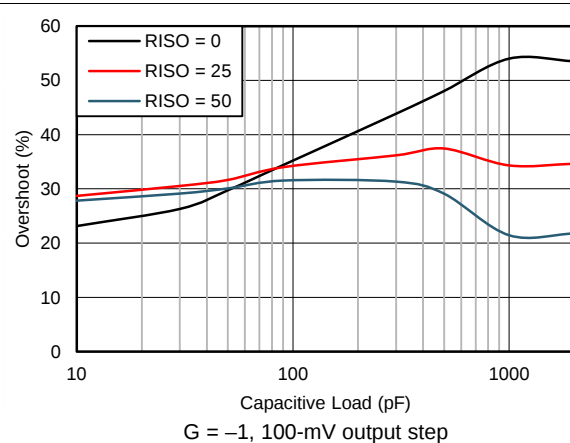
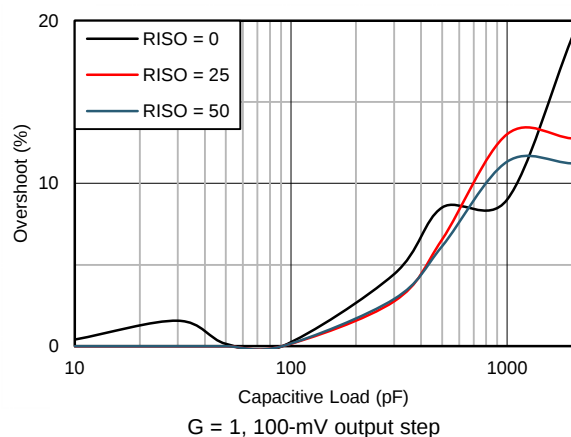
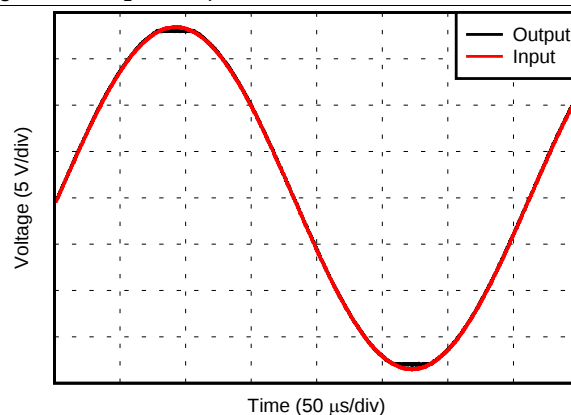


Figure 20. Small-Signal Overshoot vs Capacitive Load (100-mV Output Step)

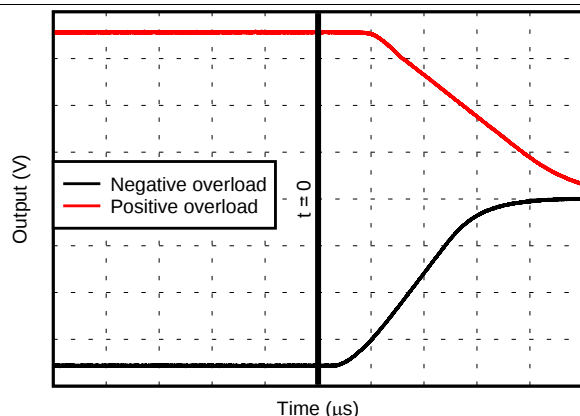
At  $T_A = 25^\circ\text{C}$ ,  $V_S = \pm 18\text{ V}$ ,  $V_{CM} = V_S / 2$ ,  $R_L = 10\text{ k}\Omega$  connected to  $V_S / 2$ , and  $C_L = 100\text{ pF}$ , unless otherwise noted.



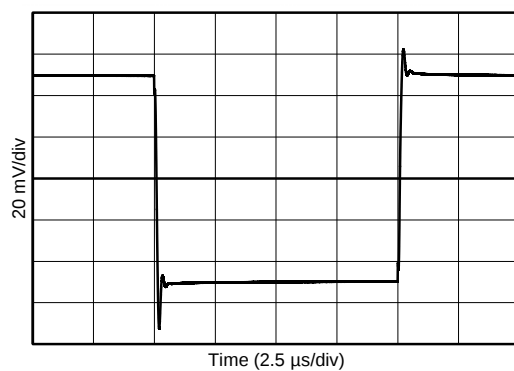
**Figure 21. Small-Signal Overshoot vs Capacitive Load**



**Figure 22. No Phase Reversal**

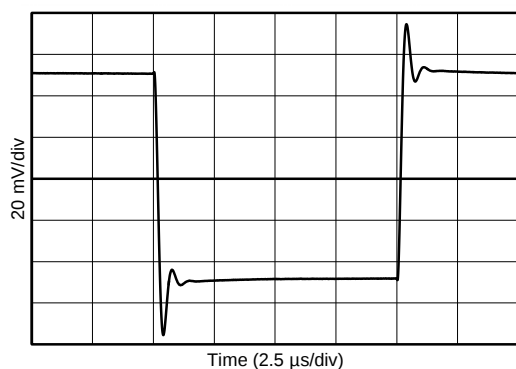


**Figure 23. Overload Recovery**



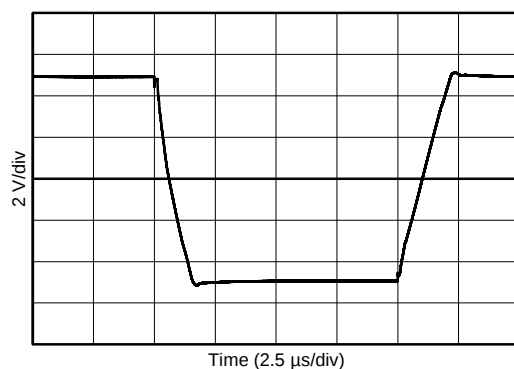
$G = 1$ ,  $C_L = 10\text{ pF}$

**Figure 24. Small-Signal Step Response**



$G = -1$ ,  $R_L = 1\text{ k}\Omega$ ,  $C_L = 10\text{ pF}$

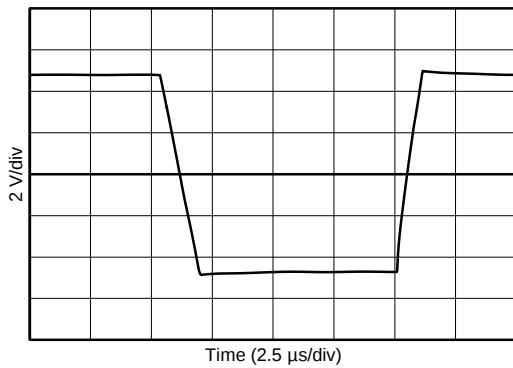
**Figure 25. Small-Signal Step Response**



$G = 1$ ,  $C_L = 10\text{ pF}$

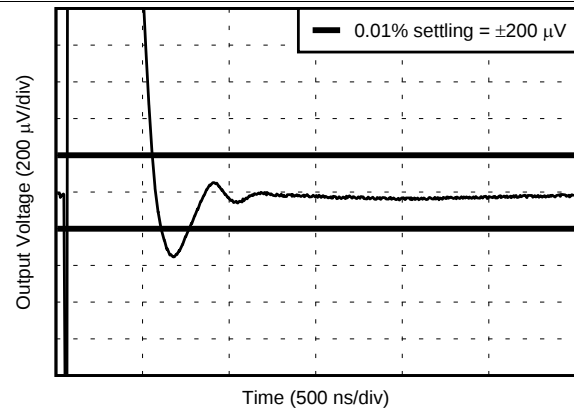
**Figure 26. Large-Signal Step Response**

At  $T_A = 25^\circ\text{C}$ ,  $V_S = \pm 18\text{ V}$ ,  $V_{CM} = V_S / 2$ ,  $R_L = 10\text{ k}\Omega$  connected to  $V_S / 2$ , and  $C_L = 100\text{ pF}$ , unless otherwise noted.



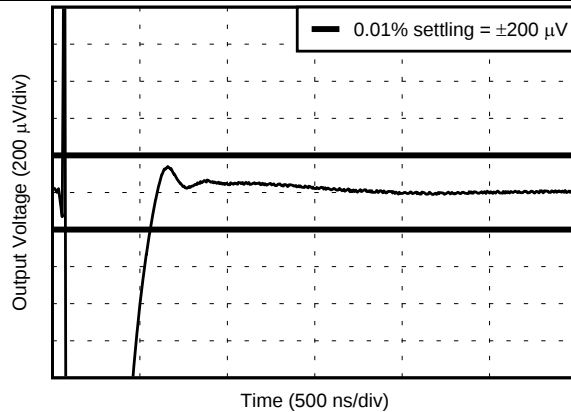
$G = -1$ ,  $R_L = 1\text{ k}\Omega$ ,  $C_L = 10\text{ pF}$

Figure 27. Large-Signal Step Response



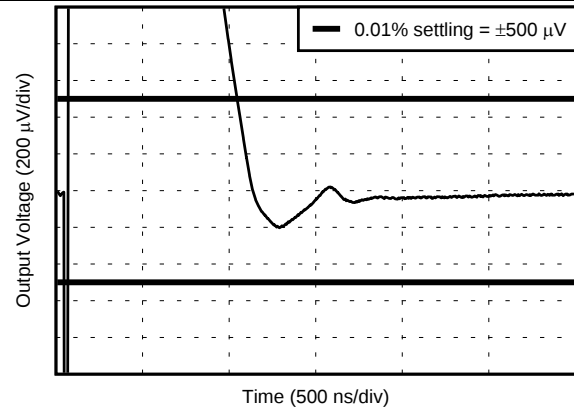
Gain = 1, 2-V step, rising, step applied at  $t = 0\text{ μs}$  on all four plots

Figure 28. 0.01% Settling Time



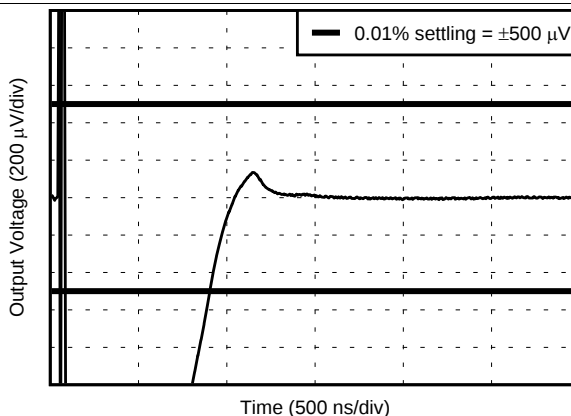
Gain = 1, 2-V step, falling, step applied at  $t = 0\text{ μs}$

Figure 29. 0.01% Settling Time



Gain = 1, 5-V step, rising, step applied at  $t = 0\text{ μs}$

Figure 30. 0.01% Settling Time



Gain = 1, 5-V step, falling, step applied at  $t = 0\text{ μs}$

Figure 31. 0.01% Settling Time

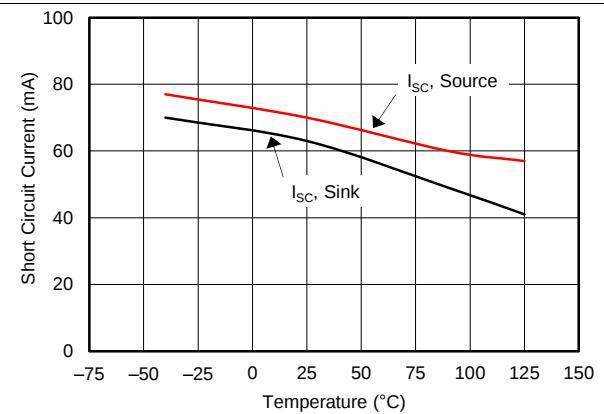
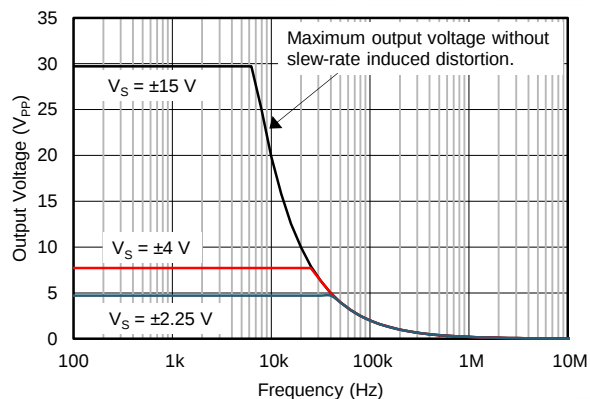
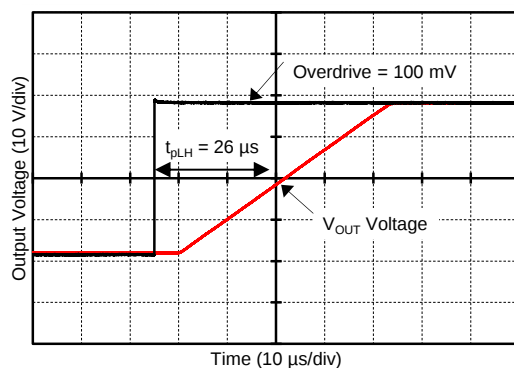


Figure 32. Short-Circuit Current vs Temperature

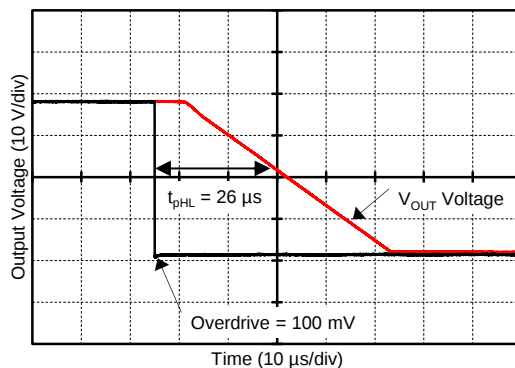
At  $T_A = 25^\circ\text{C}$ ,  $V_S = \pm 18\text{ V}$ ,  $V_{CM} = V_S / 2$ ,  $R_L = 10\text{ k}\Omega$  connected to  $V_S / 2$ , and  $C_L = 100\text{ pF}$ , unless otherwise noted.



**Figure 33. Maximum Output Voltage vs Frequency**



**Figure 34. Propagation Delay Rising Edge**



**Figure 35. Propagation Delay Falling Edge**

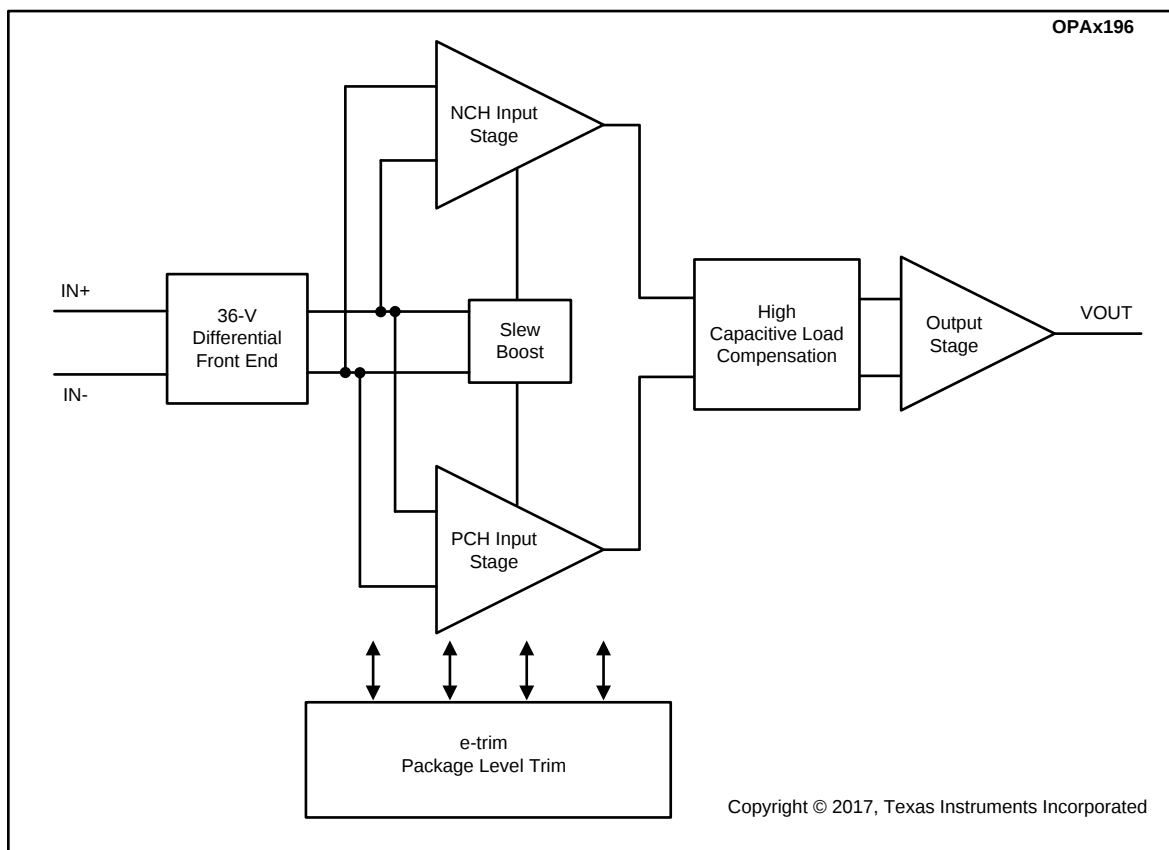
## 7 Detailed Description

### 7.1 Overview

The OPAx196 family of operational amplifiers use *e-trim*, a method of package-level trim for offset and offset temperature drift implemented during the final steps of manufacturing after the plastic molding process. This method minimizes the influence of inherent input transistor mismatch, as well as errors induced during package molding. The trim communication occurs on the output pin of the standard pinout, and after the trim points are set, further communication to the trim structure is permanently disabled. The [Functional Block Diagram](#) shows the simplified diagram of the OPA196 with e-trim.

Unlike previous e-trim op amps, the OPAx196 uses a patented two-temperature trim architecture to achieve a very low offset voltage and low voltage offset drift over the full specified temperature range. This level of precision performance at wide supply voltages makes these amplifiers useful for high-impedance industrial sensors, filters, and high-voltage data acquisition.

### 7.2 Functional Block Diagram



## 7.3 Feature Description

### 7.3.1 Input Protection Circuitry

The OPAx196 uses a unique input architecture to eliminate the need for input protection diodes but still provides robust input protection under transient conditions. Conventional input diode protection schemes shown in [Figure 36](#) can be activated by fast transient step responses and can introduce signal distortion and settling time delays because of alternate current paths, as shown in [Figure 37](#). For low-gain circuits, these fast-ramping input signals forward-bias back-to-back diodes that cause an increase in input current, resulting in extended settling time.

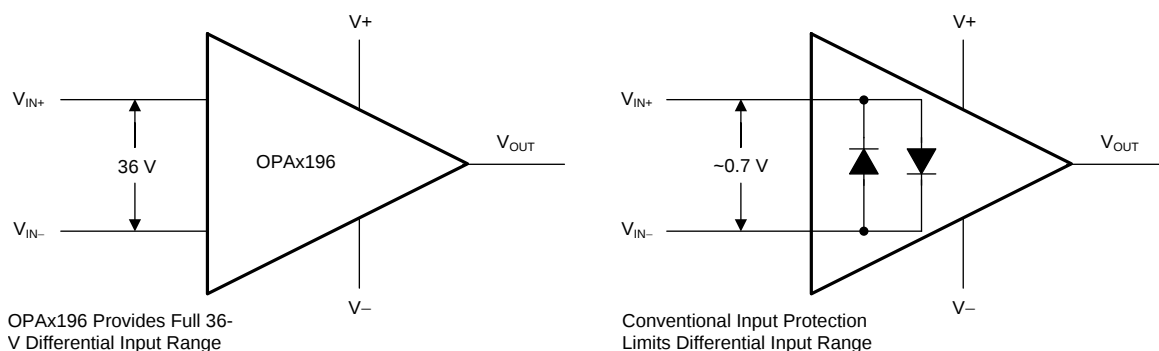


Figure 36. OPA196 Input Protection Does Not Limit Differential Input Capability

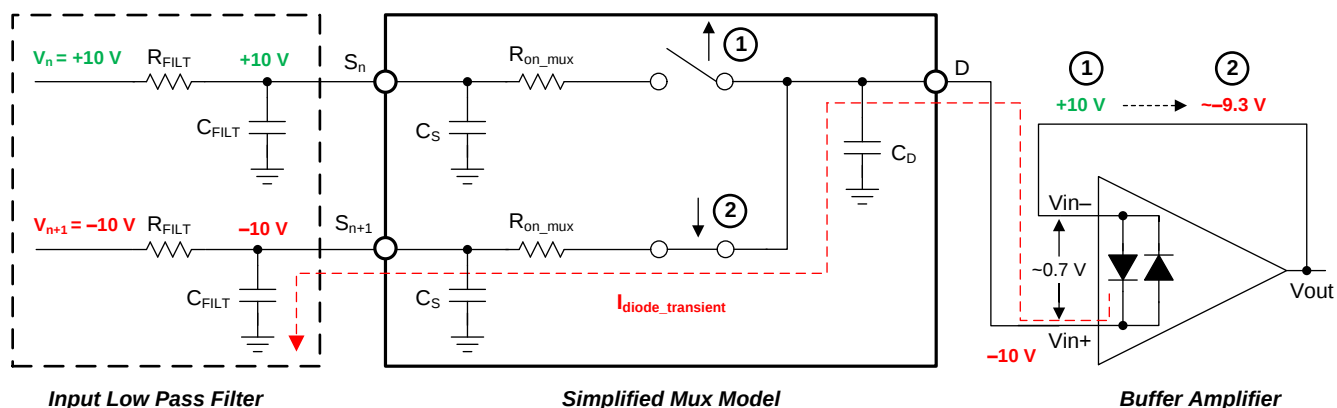


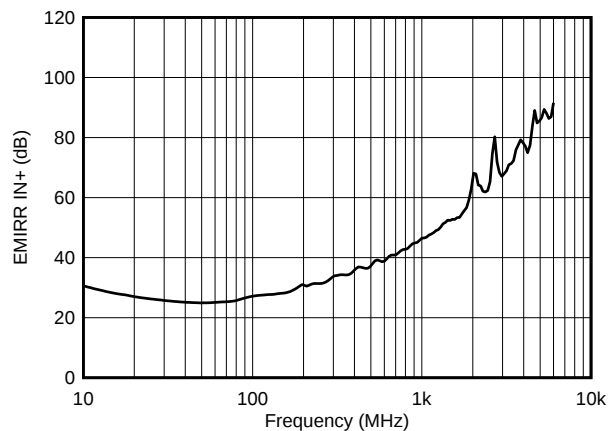
Figure 37. Back-to-Back Diodes Create Settling Issues

The OPAx196 family of operational amplifiers provides a true high-impedance differential input capability for high-voltage applications. This patented input protection architecture does not introduce additional signal distortion or delayed settling time, making the device an optimal op amp for multichannel, high-switched, input applications. The OPA196 can tolerate a maximum differential swing (voltage between inverting and noninverting pins of the op amp) of up to 36 V, making the device suitable for use as a comparator or in applications with fast-ramping input signals such as multiplexed data-acquisition systems (see [Figure 49](#)).

## Feature Description (continued)

### 7.3.2 EMI Rejection

The OPAx196 uses integrated electromagnetic interference (EMI) filtering to reduce the effects of EMI from sources such as wireless communications and densely-populated boards with a mix of analog signal chain and digital components. EMI immunity can be improved with circuit design techniques; the OPAx196 benefits from these design improvements. Texas Instruments has developed the ability to accurately measure and quantify the immunity of an operational amplifier over a broad frequency spectrum extending from 10 MHz to 6 GHz. [Figure 38](#) shows the results of this testing on the OPAx196. [Table 2](#) shows the EMIRR IN+ values for the OPAx196 at particular frequencies commonly encountered in real-world applications. Applications listed in [Table 2](#) may be centered on or operated near the particular frequency shown. Detailed information can also be found in the application report [EMI Rejection Ratio of Operational Amplifiers](#), available for download from [www.ti.com](#).



$$P_{RF} = -10 \text{ dBm}, V_S = \pm 15 \text{ V}, V_{CM} = 0 \text{ V}$$

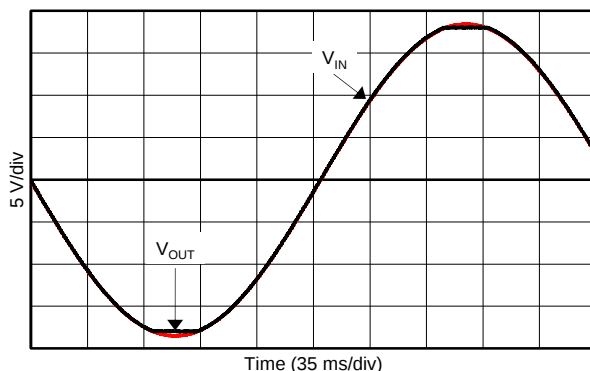
**Figure 38. EMIRR Testing**

**Table 2. OPA196 EMIRR IN+ For Frequencies of Interest**

| FREQUENCY | APPLICATION OR ALLOCATION                                                                                                                                                        | EMIRR IN+ |
|-----------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------|
| 400 MHz   | Mobile radio, mobile satellite, space operation, weather, radar, ultra-high frequency (UHF) applications                                                                         | 36 dB     |
| 900 MHz   | Global system for mobile communications (GSM) applications, radio communication, navigation, GPS (to 1.6 GHz), GSM, aeronautical mobile, UHF applications                        | 45 dB     |
| 1.8 GHz   | GSM applications, mobile personal communications, broadband, satellite, L-band (1 GHz to 2 GHz)                                                                                  | 57 dB     |
| 2.4 GHz   | 802.11b, 802.11g, 802.11n, Bluetooth®, mobile personal communications, industrial, scientific and medical (ISM) radio band, amateur radio and satellite, S-band (2 GHz to 4 GHz) | 62 dB     |
| 3.6 GHz   | Radiolocation, aero communication and navigation, satellite, mobile, S-band                                                                                                      | 76 dB     |
| 5.0 GHz   | 802.11a, 802.11n, aero communication and navigation, mobile communication, space and satellite operation, C-band (4 GHz to 8 GHz)                                                | 86 dB     |

### 7.3.3 Phase Reversal Protection

The OPAx196 family has internal phase-reversal protection. Many op amps exhibit phase reversal when the input is driven beyond the linear common-mode range. This condition is most often encountered in noninverting circuits when the input is driven beyond the specified common-mode voltage range, causing the output to reverse into the opposite rail. The OPAx196 is a rail-to-rail input op amp, and therefore the common-mode range can extend up to the rails. Input signals beyond the rails do not cause phase reversal; instead, the output limits into the appropriate rail. This performance is shown in [Figure 39](#).



**Figure 39. No Phase Reversal**

### 7.3.4 Thermal Protection

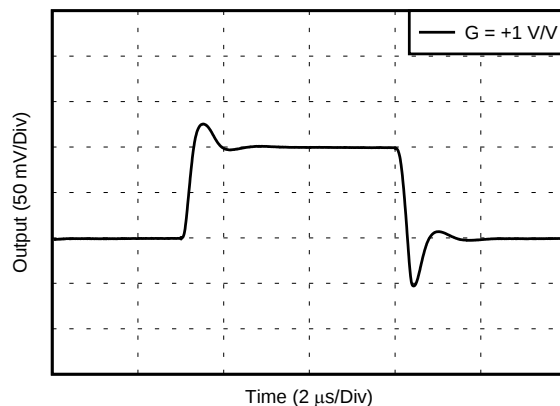
The internal power dissipation of any amplifier causes the internal (junction) temperature to rise. This phenomenon is called *self heating*. The OPAx196 has a thermal protection feature that prevents damage from self heating.

This thermal protection works by monitoring the temperature of the output stage and turning off the op amp output drive for temperatures above approximately 180°C. Thermal protection forces the output to a high-impedance state. The OPAx196 is also designed with approximately 30°C of thermal hysteresis. Thermal hysteresis prevents the output stage from cycling in and out of the high-impedance state. The OPAx196 returns to normal operation when the output stage temperature falls below approximately 150°C.

The absolute maximum junction temperature of the OPAx196 is 150°C. Exceeding the limits shown in the [Absolute Maximum Ratings](#) table may cause damage to the device. Thermal protection triggers at 180°C because of unit-to-unit variance, but does not interfere with device operation up to the absolute maximum ratings. This thermal protection is not designed to prevent this device from exceeding absolute maximum ratings, but rather from excessive thermal overload.

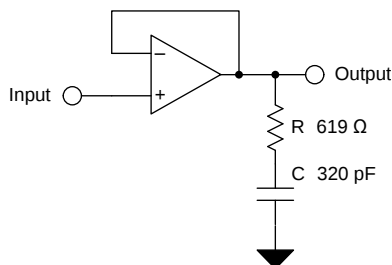
### 7.3.5 Capacitive Load and Stability

The OPAx196 features a patented output stage capable of driving large capacitive loads, and in a unity-gain configuration, directly drives up to 1 nF of pure capacitive load. Increasing the gain enhances the ability of the amplifier to drive greater capacitive loads; see [Figure 40](#). The particular op amp circuit configuration, layout, gain, and output loading are some of the factors to consider when establishing whether an amplifier will be stable in operation.



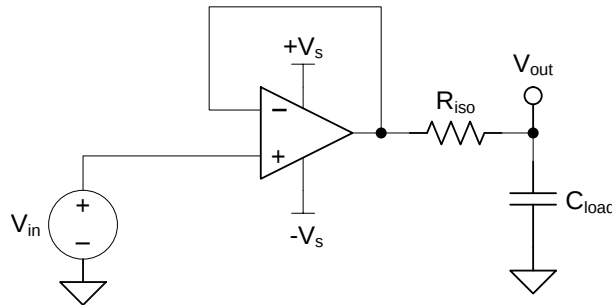
**Figure 40. Transient Response with a Purely Capacitive Load of 1 nF**

Like many low-power amplifiers, some ringing can occur even with capacitive loads less than 100 pF. In unity-gain configurations with no or very light dc loads, place an RC snubber circuit at the OPAx196 output to reduce any possibility of ringing in lightly-loaded applications. [Figure 41](#) illustrates the recommended RC snubber circuit.



**Figure 41. RC Snubber Circuit for Lightly-Loaded Applications in Unity Gain**

For additional drive capability in unity-gain configurations, improve capacitive load drive by inserting a small, 10-Ω to 20-Ω resistor ( $R_{ISO}$ ) in series with the output, as shown in [Figure 42](#). This resistor significantly reduces ringing while maintaining dc performance for purely capacitive loads. However, if there is a resistive load in parallel with the capacitive load, a voltage divider is created, introducing a gain error at the output and slightly reducing the output swing. The error introduced is proportional to the ratio  $R_{ISO} / R_L$  and is generally negligible at low output levels. A high capacitive load drive makes the OPA196 well suited for applications such as reference buffers, MOSFET gate drives, and cable-shield drives. The circuit shown in [Figure 42](#) uses  $R_{ISO}$  to stabilize the output of an op amp.  $R_{ISO}$  modifies the open-loop gain of the system for increased phase margin. Results using the OPA196 are summarized in [Table 3](#). For additional information on techniques to optimize and design using this circuit, TI Precision Design [TIDU032](#) details complete design goals, simulation, and test results.



**Figure 42. Extending Capacitive Load Drive With the OPA196**

**Table 3. OPA196 Capacitive Load Drive Solution Using Isolation Resistor Comparison of Calculated and Measured Results**

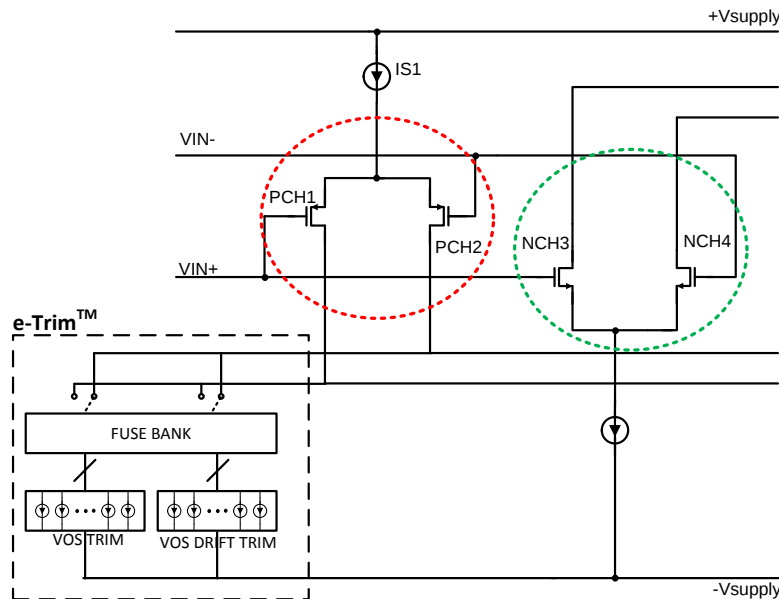
| PARAMETER              | VALUE  |         |     |         |     |        |      |      |     |
|------------------------|--------|---------|-----|---------|-----|--------|------|------|-----|
| Capacitive Load        | 100 pF | 1000 pF |     | 0.01 μF |     | 0.1 μF |      | 1 μF |     |
| Phase Margin           | 45°    | 45°     | 60° | 45°     | 60° | 45°    | 60°  | 45°  | 60° |
| R <sub>ISO</sub> (Ω)   | 280    | 113     | 432 | 68      | 210 | 17.8   | 53.6 | 3.6  | 10  |
| Measured Overshoot (%) | 23     | 23      | 8   | 23      | 8   | 23     | 8    | 23   | 8   |



For step-by-step design procedure, circuit schematics, bill of materials, printed circuit board (PCB) files, simulation results, and test results, refer to [TI Precision Design TIDU032, Capacitive Load Drive Solution using an Isolation Resistor](#).

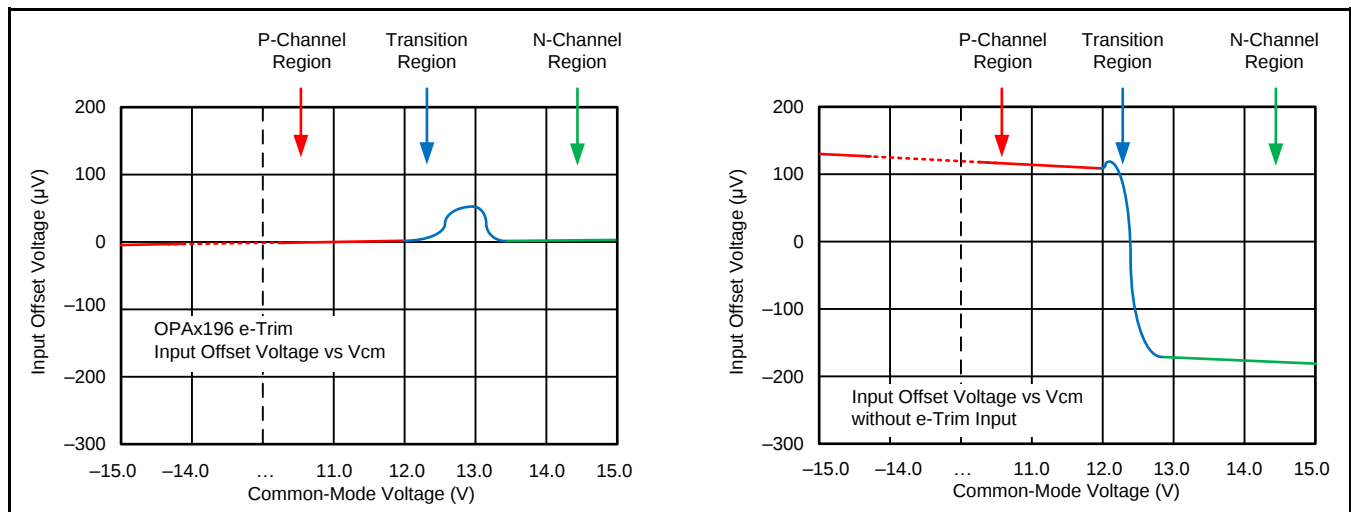
### 7.3.6 Common-Mode Voltage Range

The OPAx196 is a 36-V, true rail-to-rail input operational amplifier with an input common-mode range that extends 100 mV beyond either supply rail. This wide range is achieved with paralleled complementary N-channel and P-channel differential input pairs, as shown in Figure 43. The N-channel pair is active for input voltages close to the positive rail, typically  $(V+) - 3\text{ V}$  to 100 mV above the positive supply. The P-channel pair is active for inputs from 100 mV below the negative supply to approximately  $(V+) - 1.5\text{ V}$ . There is a small transition region, typically  $(V+) - 3\text{ V}$  to  $(V+) - 1.5\text{ V}$  in which both input pairs are active. This transition region varies modestly with process variation. Within this region PSRR, CMRR, offset voltage, offset drift, noise, and THD performance are degraded compared to operation outside this region.



**Figure 43. Rail-to-Rail Input Stage**

To achieve the best performance for two-stage rail-to-rail input amplifiers, avoid the transition region when possible. The OPAx196 uses a precision trim for both the N-channel and P-channel regions. This technique enables significantly lower levels of offset than previous-generation devices, causing variance in the transition region of the input stages to appear exaggerated relative to offset over the full common-mode range, as shown in Figure 44.



**Figure 44. Common-Mode Transition vs Standard Rail-to-Rail Amplifiers**

### 7.3.7 Electrical Overstress

Designers often ask questions about the capability of an operational amplifier to withstand electrical overstress (EOS). These questions tend to focus on the device inputs, but may involve the supply voltage pins or even the output pin. Each of these different pin functions have electrical stress limits determined by the voltage breakdown characteristics of the particular semiconductor fabrication process and specific circuits connected to the pin. Additionally, internal electrostatic discharge (ESD) protection is built into these circuits to protect them from accidental ESD events both before and during product assembly.

Having a good understanding of this basic ESD circuitry and its relevance to an electrical overstress event is helpful. See [Figure 45](#) for an illustration of the ESD circuits contained in the OPAx196 (indicated by the dashed line area). The ESD protection circuitry involves several current-steering diodes connected from the input and output pins and routed back to the internal power-supply lines, where the diodes meet at an absorption device or the power-supply ESD cell, internal to the operational amplifier. This protection circuitry is intended to remain inactive during normal circuit operation.

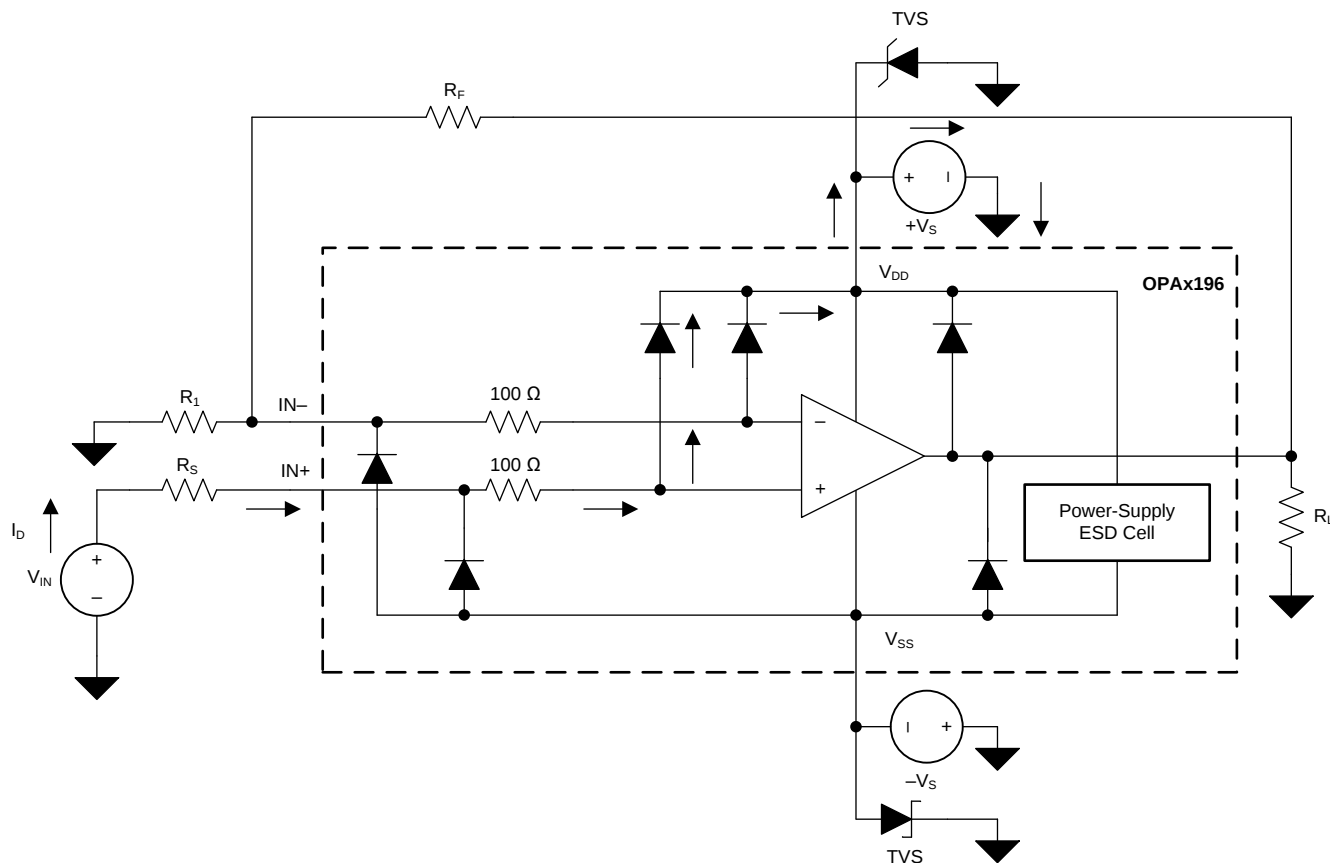


Figure 45. Equivalent Internal ESD Circuitry Relative to a Typical Circuit Application

An ESD event is very high voltage for a very short duration (for example, 1 kV for 100 ns); whereas, an EOS event is lower voltage for a longer duration (for example, 50 V for 100 ms). The ESD diodes are designed for out-of-circuit ESD protection (that is, during assembly, test, and storage of the device before being soldered to the PCB). During an ESD event, the ESD signal is passed through the ESD steering diodes to an absorption circuit labeled ESD power-supply circuit. The ESD absorption circuit clamps the supplies to a safe level.

Although this behavior is necessary for out-of-circuit protection, excessive current and damage is caused if activated in-circuit. A transient voltage suppressor (TVS) can be used to prevent against damage caused by turning on the ESD absorption circuit during an in-circuit ESD event. Using the appropriate current limiting resistors and TVS diodes allows for the use of device ESD diodes to protect against EOS events.

### **7.3.8 Overload Recovery**

Overload recovery is defined as the time required for the op amp output to recover from a saturated state to a linear state. The output devices of the op amp enter a saturation region when the output voltage exceeds the rated operating voltage, either due to the high input voltage or the high gain. After the device enters the saturation region, the charge carriers in the output devices require time to return back to the linear state. After the charge carriers return back to the linear state, the device begins to slew at the specified slew rate. Thus, the propagation delay in case of an overload condition is the sum of the overload recovery time and the slew time.

## **7.4 Device Functional Modes**

The OPAx196 has a single functional mode and is operational when the power-supply voltage is greater than 4.5 V ( $\pm 2.25$  V). The maximum power supply voltage for the OPAx196 is 36 V ( $\pm 18$  V).

## 8 Application and Implementation

### NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### 8.1 Application Information

The OPAx196 family offers outstanding dc precision and ac performance. These devices operate up to 36-V supply rails and offer true rail-to-rail input/output, ultralow offset voltage and offset voltage drift, as well as 2-MHz bandwidth and high capacitive load drive. These features make the OPAx196 a robust, high-performance operational amplifier for high-voltage industrial applications.

### 8.2 Typical Applications

#### 8.2.1 Low-side Current Measurement

Figure 46 shows the OPA196 configured in a low-side current sensing application. For a full analysis of the circuit shown in Figure 46 including theory, calculations, simulations, and measured data see the 0-1A, single-supply, low-side, current sensing solution, see [TIPD129](#).

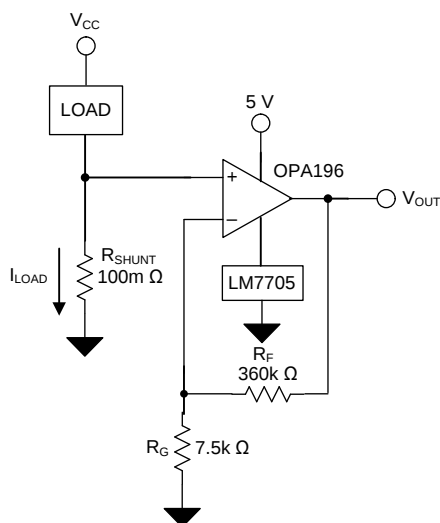


Figure 46. OPA196 in a Low-Side, Current-Sensing Application

##### 8.2.1.1 Design Requirements

The design requirements for this design are:

- Load current: 0 A to 1 A
- Output voltage: 4.9 V
- Maximum shunt voltage: 100 mV

## Typical Applications (continued)

### 8.2.1.2 Detailed Design Procedure

The transfer function of the circuit in [Figure 46](#) is given in [Equation 1](#):

$$V_{OUT} = I_{LOAD} \times R_{SHUNT} \times \text{Gain} \quad (1)$$

The load current ( $I_{LOAD}$ ) produces a voltage drop across the shunt resistor ( $R_{SHUNT}$ ). The load current is set from 0 A to 1 A. To keep the shunt voltage below 100 mV at maximum load current, the largest shunt resistor is defined using [Equation 2](#).

$$R_{SHUNT} = \frac{V_{SHUNT\_MAX}}{I_{LOAD\_MAX}} = \frac{100\text{mV}}{1\text{A}} = 100\text{m}\Omega \quad (2)$$

Using [Equation 2](#),  $R_{SHUNT}$  is calculated to be 100 mΩ. The voltage drop produced by  $I_{LOAD}$  and  $R_{SHUNT}$  is amplified by the OPA196 to produce an output voltage of 0 V to 4.9 V. The gain needed by the OPA196 to produce the necessary output voltage is calculated using [Equation 3](#):

$$\text{Gain} = \frac{(V_{OUT\_MAX} - V_{OUT\_MIN})}{(V_{IN\_MAX} - V_{IN\_MIN})} \quad (3)$$

Using [Equation 3](#), the required gain is calculated to be 49 V/V, which is set with resistors  $R_F$  and  $R_G$ . [Equation 4](#) is used to size the resistors,  $R_F$  and  $R_G$ , to set the gain of the OPA196 to 49 V/V.

$$\text{Gain} = 1 + \frac{(R_F)}{(R_G)} \quad (4)$$

Choosing  $R_F$  as 360 kΩ,  $R_G$  is calculated to be 7.5 kΩ.  $R_F$  and  $R_G$  were chosen as 360 kΩ and 7.5 kΩ because they are standard value resistors that create a 49:1 ratio. Other resistors that create a 49:1 ratio can also be used. [Figure 2](#) shows the measured transfer function of the circuit shown in [Figure 46](#).

### 8.2.1.3 Application Curves

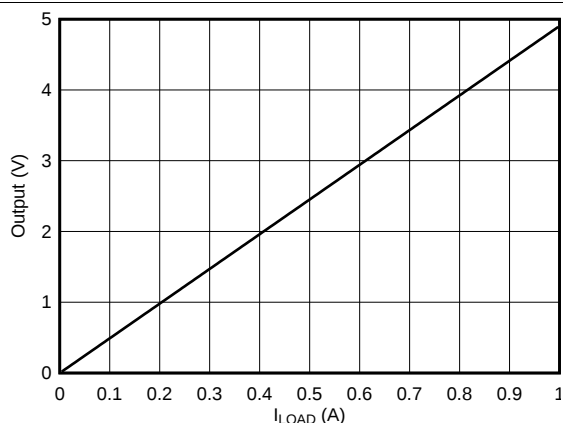


Figure 47. Low-Side, Current-Sense, Transfer Function

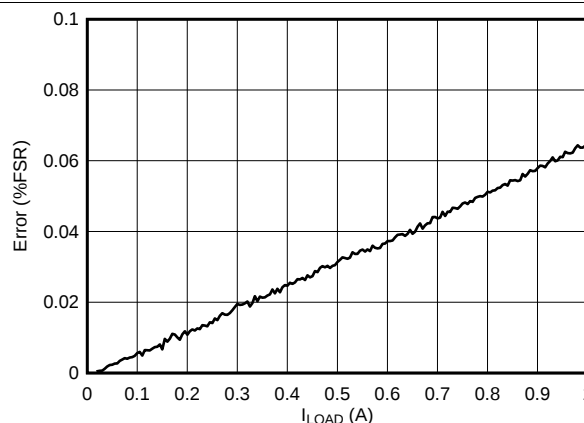


Figure 48. Low-Side, Current-Sense, Full-Scale Error

## Typical Applications (continued)

### 8.2.2 16-Bit Precision Multiplexed Data-Acquisition System

Figure 49 shows a 16-bit, differential, 4-channel, multiplexed, data-acquisition system. This example is typical in industrial applications that require low distortion and a high-voltage differential input. The circuit uses the ADS8864, a 16-bit, 400-kSPS successive-approximation-resistor (SAR), analog-to-digital converter (ADC), along with a precision, high-voltage, signal-conditioning front-end, and a 4-channel differential multiplexer (mux). This application example shows the process for optimizing the precision, high-voltage, front-end drive circuit using the OPA196 and OPA140 to achieve excellent dynamic performance and linearity with the ADS8864. The full TI Precision Design can be found in TIDU181.

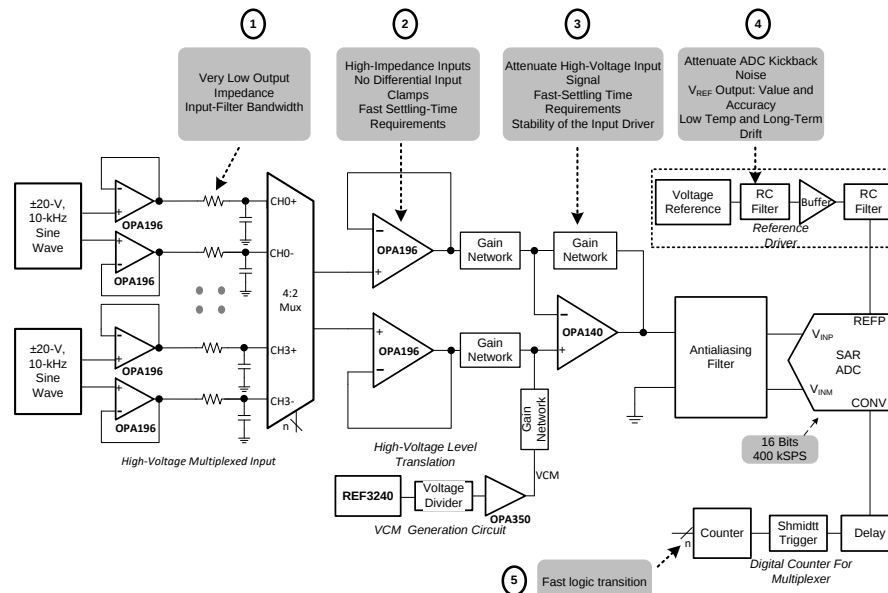


Figure 49. OPA196 in 16-Bit, 400-kSPS, 4-Channel, Multiplexed Data Acquisition System for High-Voltage Inputs With Lowest Distortion

#### 8.2.2.1 Design Requirements

The primary objective is to design a  $\pm 20$ -V, differential, 4-channel, multiplexed, data acquisition system with lowest distortion using the 16-bit ADS8864 at a throughput of 400 kSPS for a 10-kHz, full-scale, pure sine-wave input. The design requirements for this block design are:

- System supply voltage:  $\pm 15$  V
- ADC supply voltage: 3.3 V
- ADC sampling rate: 400 kSPS
- ADC reference voltage (REFP): 4.096 V
- System input signal: A high-voltage differential input signal with a peak amplitude of 10 V and frequency ( $f_{IN}$ ) of 10 kHz are applied to each differential input of the mux.

#### 8.2.2.2 Detailed Design Procedure

The purpose of this application example is to design an optimal, high-voltage, multiplexed, data-acquisition system for highest system linearity and fast settling. The overall system block diagram is shown in Figure 49. The circuit is a multichannel, data-acquisition, signal chain consisting of an input low-pass filter, multiplexer (mux), mux output buffer, attenuating SAR ADC driver, digital counter for the mux, and the reference driver. The architecture allows fast sampling of multiple channels using a single ADC, providing a low-cost solution. The two primary design considerations to maximize the performance of a precision, multiplexed, data-acquisition system are the mux input analog front-end and the high-voltage, level translation, SAR ADC driver design. However, carefully design each analog circuit block based on the ADC performance specifications in order to achieve the fastest settling at 16-bit resolution and lowest distortion system. Figure 49 includes the most important specifications for each individual analog block.

## Typical Applications (continued)

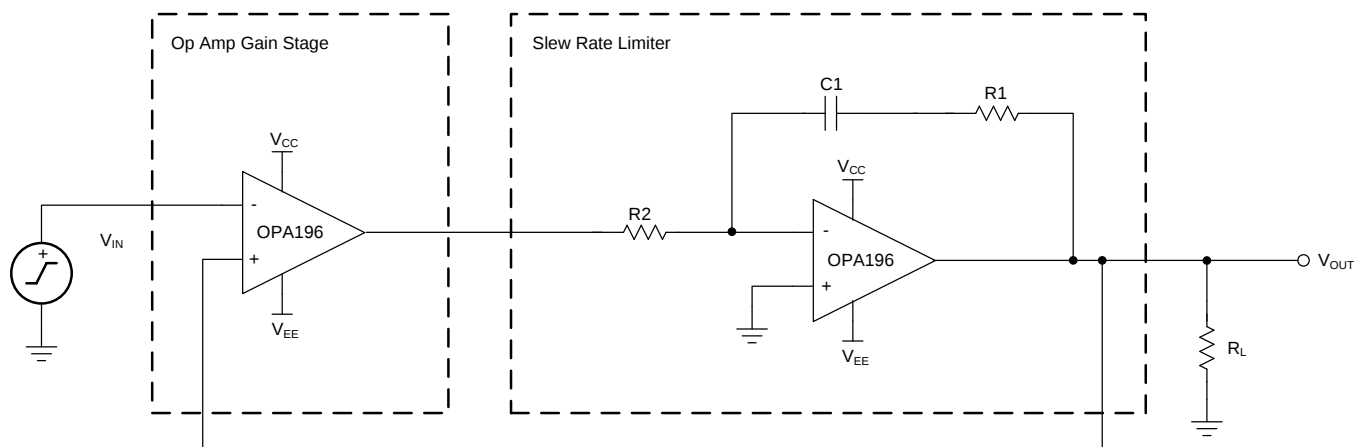
This design systematically approaches each analog circuit block to achieve a 16-bit settling for a full-scale input stage voltage and linearity for a 10-kHz sinusoidal input signal at each input channel. The first step in the design is to understand the requirement for an extremely-low-impedance input-filter design for the mux. This understanding helps in the decision of an appropriate input filter and selection of a mux to meet the system settling requirements. The next important step is the design of the attenuating analog front-end (AFE) used to level translate the high-voltage input signal to a low-voltage ADC input while maintaining the amplifier stability. Then, the next step is to design a digital interface to switch the mux input channels with minimum delay. The final design challenge is to design a high-precision, reference-driver circuit that provides the required REFP reference voltage with low offset, drift, and noise contributions.



For step-by-step design procedure, circuit schematics, bill of materials, PCB files, simulation results, and test results, refer to [TI Precision Design TIDU181, 16-bit, 400-kSPS, 4-Channel, Multiplexed Data Acquisition System for High Voltage Inputs with Lowest Distortion](#).

### 8.2.3 Slew Rate Limit for Input Protection

In control systems for valves or motors, abrupt changes in voltages or currents can cause mechanical damages. By controlling the slew rate of the command voltages into the drive circuits, the load voltages ramps up and down at a safe rate. For symmetrical slew-rate applications (positive slew rate equals negative slew rate), one additional op amp provides slew-rate control for a given analog gain stage. The unique input protection and high output current and slew rate of the OPAx196 make the device an optimal amplifier to achieve slew rate control for both dual- and single-supply systems. [Figure 50](#) shows the OPA196 in a slew-rate limit design.



**Figure 50. Slew Rate Limiter Uses One Op Amp**



For step-by-step design procedure, circuit schematics, bill of materials, PCB files, simulation results, and test results, refer to [TI Precision Design TIDU026, Slew Rate Limiter Uses One Op Amp](#).

## 9 Power-Supply Recommendations

The OPAx196 is specified for operation from 4.5 V to 36 V ( $\pm 2.25$  V to  $\pm 18$  V); many specifications apply from  $-40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$ . Parameters that can exhibit significant variance with regard to operating voltage or temperature are presented in the [Typical Characteristics](#).

### CAUTION

Supply voltages larger than 40 V can permanently damage the device; see the [Absolute Maximum Ratings](#).

Place 0.1- $\mu\text{F}$  bypass capacitors close to the power-supply pins to reduce errors coupling in from noisy or high-impedance power supplies. For more detailed information on bypass capacitor placement, refer to the [Layout](#) section.

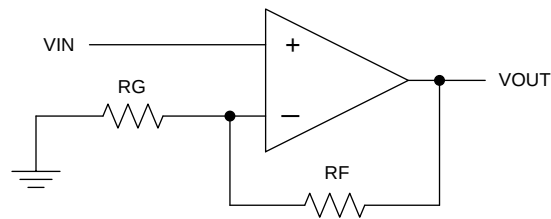
## 10 Layout

### 10.1 Layout Guidelines

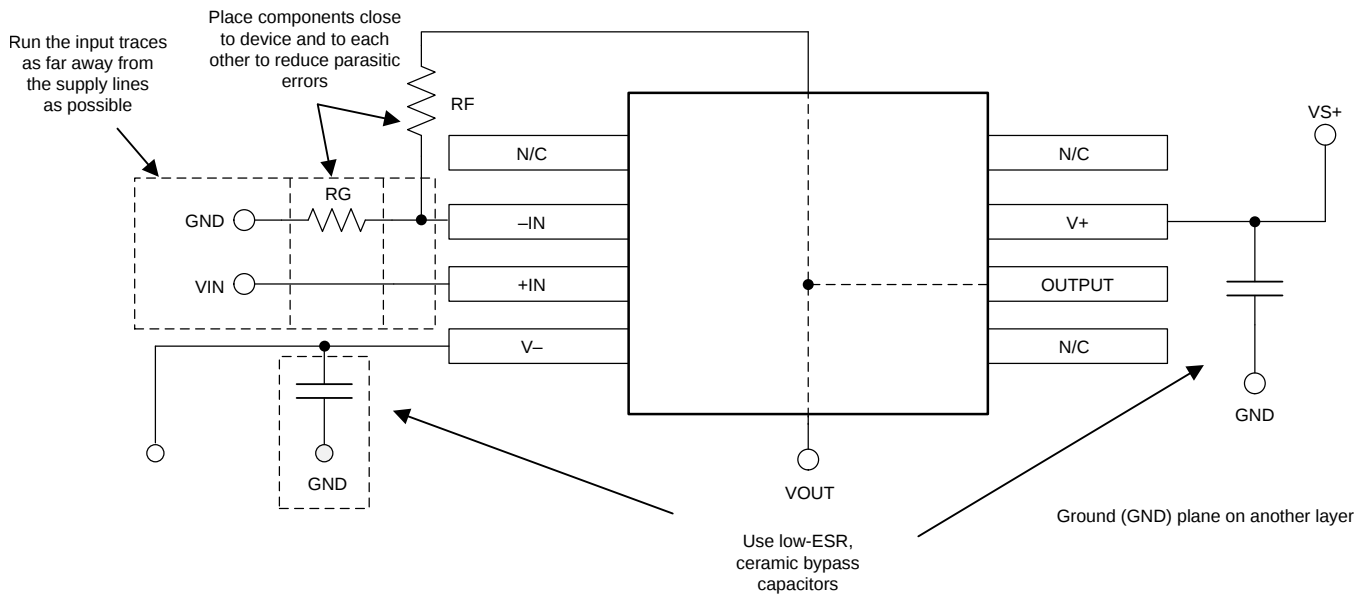
For best operational performance of the device, use good PCB layout practices, including:

- Connect low-ESR, 0.1- $\mu\text{F}$  ceramic bypass capacitors between each supply pin and ground, placed as close as possible to the device. A single bypass capacitor from  $V+$  to ground is applicable for single-supply applications.
  - Noise can propagate into analog circuitry through the power pins of the circuit as a whole and op amp itself. Bypass capacitors are used to reduce the coupled noise by providing low-impedance power sources local to the analog circuitry.
- Make sure to physically separate digital and analog grounds paying attention to the flow of the ground current. Separate grounding for analog and digital portions of circuitry is one of the simplest and most-effective methods of noise suppression. One or more layers on multilayer PCBs are usually devoted to ground planes. A ground plane helps distribute heat and reduces EMI noise pickup.
- In order to reduce parasitic coupling, run the input traces as far away as possible from the supply or output traces. If these traces cannot be kept separate, crossing the sensitive trace perpendicular is much better as opposed to in parallel with the noisy trace.
- Place the external components as close to the device as possible. As shown in [Figure 52](#), keeping RF and RG close to the inverting input minimizes parasitic capacitance.
- Keep the length of input traces as short as possible. Always remember that the input traces are the most sensitive part of the circuit.
- Consider a driven, low-impedance guard ring around the critical traces. A guard ring can significantly reduce leakage currents from nearby traces that are at different potentials.
- Clean the PCB following board assembly for best performance.
- Any precision integrated circuit may experience performance shifts due to moisture ingress into the plastic package. After any aqueous PCB cleaning process, bake the PCB assembly to remove moisture introduced into the device packaging during the cleaning process. A low-temperature, post-cleaning bake at  $85^{\circ}\text{C}$  for 30 minutes is sufficient for most circumstances.

## 10.2 Layout Example



**Figure 51. Schematic Representation**



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**Figure 52. Operational Amplifier Board Layout for Non-inverting Configuration**

## 11 デバイスおよびドキュメントのサポート

### 11.1 デバイス・サポート

#### 11.1.1 開発サポート

##### 11.1.1.1 TINA-TI™(無料のダウンロード・ソフトウェア)

TINA™ は、SPICEエンジンをベースにした単純かつ強力な、使いやすい回路シミュレーション・プログラムです。また、TINA-TIは、TINAソフトウェアの完全な機能を持つ無償バージョンで、パッシブ・モデルとアクティブ・モデルに加えて、マクロ・モデルのライブラリがプリロードされています。TINA-TIには、SPICEの標準的なDC解析、過渡解析、周波数ドメイン解析などの全機能に加え、追加の設計機能が搭載されています。

TINA-TIはAnalog eLab Design Centerから無料でダウンロードでき、ユーザーが結果をさまざまな方法でフォーマットできる、広範な後処理機能を備えています。仮想計測器により、入力波形を選択し、回路ノード、電圧、および波形をプローブして、動的なクイック・スタート・ツールを作成できます。

#### 注

これらのファイルを使用するには、TINA ソフトウェア ( DesignSoft™製) またはTINA-TIソフトウェアがインストールされている必要があります。無料のTINA-TIソフトウェアは、[TINA-TIフォルダ\(http://www.ti.com/tool/tina-ti\)](http://www.ti.com/tool/tina-ti)からダウンロードできます。

##### 11.1.1.2 TI Precision Designs

TI Precision Designsは、<http://www.ti.com/ww/en/analog/precision-designs/>からオンラインで入手できます。TIの高精度アナログ・アプリケーションの専門家により作成されたアナログ・ソリューションで、多くの有用な回路に関して、動作理論、コンポーネント選択、シミュレーション、完全なPCB回路図とレイアウト、部品表、性能測定結果を提供します。

### 11.2 ドキュメントのサポート

#### 11.2.1 関連資料

- 『オペアンプのEMI除去率』
- 『0~1Aの単一電源、ローサイドの電流センシング・ソリューション』
- 『誰でも使えるオペアンプ』

#### 11.3 関連リンク

表 4 に、クイック・アクセス・リンクの一覧を示します。カテゴリには、技術資料、サポートおよびコミュニティ・リソース、ツールとソフトウェア、およびご注文へのクイック・アクセスが含まれます。

表 4. 関連リンク

| 製品      | プロダクト・フォルダ              | ご注文はこちら                 | 技術資料                    | ツールとソフトウェア              | サポートとコミュニティ             |
|---------|-------------------------|-------------------------|-------------------------|-------------------------|-------------------------|
| OPA196  | <a href="#">ここをクリック</a> | <a href="#">ここをクリック</a> | <a href="#">ここをクリック</a> | <a href="#">ここをクリック</a> | <a href="#">ここをクリック</a> |
| OPA2196 | <a href="#">ここをクリック</a> | <a href="#">ここをクリック</a> | <a href="#">ここをクリック</a> | <a href="#">ここをクリック</a> | <a href="#">ここをクリック</a> |
| OPA4196 | <a href="#">ここをクリック</a> | <a href="#">ここをクリック</a> | <a href="#">ここをクリック</a> | <a href="#">ここをクリック</a> | <a href="#">ここをクリック</a> |

#### 11.4 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、ti.comのデバイス製品フォルダを開いてください。右上の隅にある「通知を受け取る」をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

## 11.5 コミュニティ・リソース

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

**TI E2E™ オンライン・コミュニティ** TIのE2E ( *Engineer-to-Engineer* ) コミュニティ。エンジニア間の共同作業を促進するために開設されたものです。e2e.ti.comでは、他のエンジニアに質問し、知識を共有し、アイデアを検討して、問題解決に役立てることができます。

**設計サポート** TIの設計サポート 役に立つE2Eフォーラムや、設計サポート・ツールをすばやく見つけることができます。技術サポート用の連絡先情報も参照できます。

## 11.6 商標

e-trim, E2E are trademarks of Texas Instruments.

TINA-TI is a trademark of Texas Instruments, Inc and DesignSoft, Inc.

Bluetooth is a registered trademark of Bluetooth SIG, Inc.

TINA, DesignSoft are trademarks of DesignSoft, Inc.

## 11.7 静電気放電に関する注意事項



すべての集積回路は、適切なESD保護方法を用いて、取扱いと保存を行うようにして下さい。

静電気放電はわずかな性能の低下から完全なデバイスの故障に至るまで、様々な損傷を与えます。高精度の集積回路は、損傷に対して敏感であり、極めてわずかなパラメータの変化により、デバイスに規定された仕様に適合しなくなる場合があります。

## 11.8 Glossary

[SLYZ022](#) — TI Glossary.

This glossary lists and explains terms, acronyms, and definitions.

## 12 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。この情報は、そのデバイスについて利用可能な最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

## PACKAGING INFORMATION

| Orderable part number        | Status<br>(1) | Material type<br>(2) | Package   Pins   | Package qty   Carrier | RoHS<br>(3) | Lead finish/<br>Ball material<br>(4) | MSL rating/<br>Peak reflow<br>(5) | Op temp (°C) | Part marking<br>(6) |
|------------------------------|---------------|----------------------|------------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|---------------------|
| <a href="#">OPA196ID</a>     | Active        | Production           | SOIC (D)   8     | 75   TUBE             | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | -40 to 125   | OPA196              |
| OPA196ID.B                   | Active        | Production           | SOIC (D)   8     | 75   TUBE             | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | -40 to 125   | OPA196              |
| <a href="#">OPA196IDBVR</a>  | Active        | Production           | SOT-23 (DBV)   5 | 3000   LARGE T&R      | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | -40 to 125   | O196                |
| OPA196IDBVR.B                | Active        | Production           | SOT-23 (DBV)   5 | 3000   LARGE T&R      | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | -40 to 125   | O196                |
| OPA196IDBVRG4                | Active        | Production           | SOT-23 (DBV)   5 | 3000   LARGE T&R      | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | -40 to 125   | O196                |
| OPA196IDBVRG4.B              | Active        | Production           | SOT-23 (DBV)   5 | 3000   LARGE T&R      | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | -40 to 125   | O196                |
| <a href="#">OPA196IDBVT</a>  | Active        | Production           | SOT-23 (DBV)   5 | 250   SMALL T&R       | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | -40 to 125   | O196                |
| OPA196IDBVT.B                | Active        | Production           | SOT-23 (DBV)   5 | 250   SMALL T&R       | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | -40 to 125   | O196                |
| <a href="#">OPA196IDGKR</a>  | Active        | Production           | VSSOP (DGK)   8  | 2500   LARGE T&R      | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | -40 to 125   | O196                |
| OPA196IDGKR.B                | Active        | Production           | VSSOP (DGK)   8  | 2500   LARGE T&R      | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | -40 to 125   | O196                |
| <a href="#">OPA196IDGKT</a>  | Active        | Production           | VSSOP (DGK)   8  | 250   SMALL T&R       | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | -40 to 125   | O196                |
| OPA196IDGKT.B                | Active        | Production           | VSSOP (DGK)   8  | 250   SMALL T&R       | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | -40 to 125   | O196                |
| <a href="#">OPA196IDR</a>    | Active        | Production           | SOIC (D)   8     | 2500   LARGE T&R      | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | -40 to 125   | OPA196              |
| OPA196IDR.B                  | Active        | Production           | SOIC (D)   8     | 2500   LARGE T&R      | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | -40 to 125   | OPA196              |
| OPA196IDRG4                  | Active        | Production           | SOIC (D)   8     | 2500   LARGE T&R      | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | -40 to 125   | OPA196              |
| OPA196IDRG4.B                | Active        | Production           | SOIC (D)   8     | 2500   LARGE T&R      | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | -40 to 125   | OPA196              |
| <a href="#">OPA2196ID</a>    | Active        | Production           | SOIC (D)   8     | 75   TUBE             | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | -40 to 125   | OP2196              |
| OPA2196ID.B                  | Active        | Production           | SOIC (D)   8     | 75   TUBE             | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | -40 to 125   | OP2196              |
| OPA2196IDG4                  | Active        | Production           | SOIC (D)   8     | 75   TUBE             | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | -40 to 125   | OP2196              |
| OPA2196IDG4.B                | Active        | Production           | SOIC (D)   8     | 75   TUBE             | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | -40 to 125   | OP2196              |
| <a href="#">OPA2196IDGKR</a> | Active        | Production           | VSSOP (DGK)   8  | 2500   LARGE T&R      | Yes         | Call TI   Nipdau                     | Level-2-260C-1 YEAR               | -40 to 125   | 2196                |
| OPA2196IDGKR.B               | Active        | Production           | VSSOP (DGK)   8  | 2500   LARGE T&R      | Yes         | Call TI                              | Level-2-260C-1 YEAR               | -40 to 125   | 2196                |
| OPA2196IDGKRG4               | Active        | Production           | VSSOP (DGK)   8  | 2500   LARGE T&R      | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | -40 to 125   | 2196                |
| OPA2196IDGKRG4.B             | Active        | Production           | VSSOP (DGK)   8  | 2500   LARGE T&R      | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | -40 to 125   | 2196                |
| <a href="#">OPA2196IDGKT</a> | Active        | Production           | VSSOP (DGK)   8  | 250   SMALL T&R       | Yes         | Call TI   Nipdau                     | Level-2-260C-1 YEAR               | -40 to 125   | 2196                |
| OPA2196IDGKT.B               | Active        | Production           | VSSOP (DGK)   8  | 250   SMALL T&R       | Yes         | Call TI                              | Level-2-260C-1 YEAR               | -40 to 125   | 2196                |
| <a href="#">OPA2196IDR</a>   | Active        | Production           | SOIC (D)   8     | 2500   LARGE T&R      | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | -40 to 125   | OP2196              |
| OPA2196IDR.B                 | Active        | Production           | SOIC (D)   8     | 2500   LARGE T&R      | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | -40 to 125   | OP2196              |
| <a href="#">OPA4196ID</a>    | Active        | Production           | SOIC (D)   14    | 50   TUBE             | Yes         | NIPDAU                               | Level-3-260C-168 HR               | -40 to 125   | OPA4196             |

| Orderable part number      | Status<br>(1) | Material type<br>(2) | Package   Pins | Package qty   Carrier | RoHS<br>(3) | Lead finish/<br>Ball material<br>(4) | MSL rating/<br>Peak reflow<br>(5) | Op temp (°C) | Part marking<br>(6) |
|----------------------------|---------------|----------------------|----------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|---------------------|
| OPA4196ID.B                | Active        | Production           | SOIC (D)   14  | 50   TUBE             | Yes         | NIPDAU                               | Level-3-260C-168 HR               | -40 to 125   | OPA4196             |
| <a href="#">OPA4196IDR</a> | Active        | Production           | SOIC (D)   14  | 2500   LARGE T&R      | Yes         | NIPDAU                               | Level-3-260C-168 HR               | -40 to 125   | OPA4196             |
| OPA4196IDR.B               | Active        | Production           | SOIC (D)   14  | 2500   LARGE T&R      | Yes         | NIPDAU                               | Level-3-260C-168 HR               | -40 to 125   | OPA4196             |
| OPA4196IDRG4               | Active        | Production           | SOIC (D)   14  | 2500   LARGE T&R      | Yes         | NIPDAU                               | Level-3-260C-168 HR               | -40 to 125   | OPA4196             |
| OPA4196IDRG4.B             | Active        | Production           | SOIC (D)   14  | 2500   LARGE T&R      | Yes         | NIPDAU                               | Level-3-260C-168 HR               | -40 to 125   | OPA4196             |

<sup>(1)</sup> **Status:** For more details on status, see our [product life cycle](#).

<sup>(2)</sup> **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

<sup>(4)</sup> **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

<sup>(6)</sup> **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

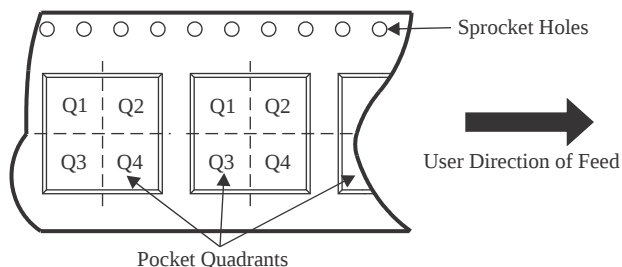
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## TAPE AND REEL INFORMATION



### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



\*All dimensions are nominal

| Device         | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|----------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| OPA196IDBVR    | SOT-23       | DBV             | 5    | 3000 | 180.0              | 8.4                | 3.23    | 3.17    | 1.37    | 4.0     | 8.0    | Q3            |
| OPA196IDBVRG4  | SOT-23       | DBV             | 5    | 3000 | 180.0              | 8.4                | 3.23    | 3.17    | 1.37    | 4.0     | 8.0    | Q3            |
| OPA196IDBVT    | SOT-23       | DBV             | 5    | 250  | 180.0              | 8.4                | 3.23    | 3.17    | 1.37    | 4.0     | 8.0    | Q3            |
| OPA196IDGKR    | VSSOP        | DGK             | 8    | 2500 | 330.0              | 12.4               | 5.3     | 3.4     | 1.4     | 8.0     | 12.0   | Q1            |
| OPA196IDGKT    | VSSOP        | DGK             | 8    | 250  | 177.8              | 12.4               | 5.3     | 3.4     | 1.4     | 8.0     | 12.0   | Q1            |
| OPA196IDR      | SOIC         | D               | 8    | 2500 | 330.0              | 12.4               | 6.4     | 5.2     | 2.1     | 8.0     | 12.0   | Q1            |
| OPA196IDRG4    | SOIC         | D               | 8    | 2500 | 330.0              | 12.4               | 6.4     | 5.2     | 2.1     | 8.0     | 12.0   | Q1            |
| OPA2196IDGKR   | VSSOP        | DGK             | 8    | 2500 | 330.0              | 12.4               | 5.3     | 3.4     | 1.4     | 8.0     | 12.0   | Q1            |
| OPA2196IDGKRG4 | VSSOP        | DGK             | 8    | 2500 | 330.0              | 12.4               | 5.3     | 3.4     | 1.4     | 8.0     | 12.0   | Q1            |
| OPA2196IDGKT   | VSSOP        | DGK             | 8    | 250  | 180.0              | 12.4               | 5.3     | 3.4     | 1.4     | 8.0     | 12.0   | Q1            |
| OPA2196IDR     | SOIC         | D               | 8    | 2500 | 330.0              | 12.4               | 6.4     | 5.2     | 2.1     | 8.0     | 12.0   | Q1            |
| OPA4196IDR     | SOIC         | D               | 14   | 2500 | 330.0              | 16.4               | 6.5     | 9.0     | 2.1     | 8.0     | 16.0   | Q1            |
| OPA4196IDRG4   | SOIC         | D               | 14   | 2500 | 330.0              | 16.4               | 6.5     | 9.0     | 2.1     | 8.0     | 16.0   | Q1            |

## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

| Device         | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|----------------|--------------|-----------------|------|------|-------------|------------|-------------|
| OPA196IDBVR    | SOT-23       | DBV             | 5    | 3000 | 213.0       | 191.0      | 35.0        |
| OPA196IDBVRG4  | SOT-23       | DBV             | 5    | 3000 | 213.0       | 191.0      | 35.0        |
| OPA196IDBVT    | SOT-23       | DBV             | 5    | 250  | 213.0       | 191.0      | 35.0        |
| OPA196IDGKR    | VSSOP        | DGK             | 8    | 2500 | 346.0       | 346.0      | 29.0        |
| OPA196IDGKT    | VSSOP        | DGK             | 8    | 250  | 213.0       | 191.0      | 35.0        |
| OPA196IDR      | SOIC         | D               | 8    | 2500 | 353.0       | 353.0      | 32.0        |
| OPA196IDRG4    | SOIC         | D               | 8    | 2500 | 353.0       | 353.0      | 32.0        |
| OPA2196IDGKR   | VSSOP        | DGK             | 8    | 2500 | 353.0       | 353.0      | 32.0        |
| OPA2196IDGKRG4 | VSSOP        | DGK             | 8    | 2500 | 353.0       | 353.0      | 32.0        |
| OPA2196IDGKT   | VSSOP        | DGK             | 8    | 250  | 213.0       | 191.0      | 35.0        |
| OPA2196IDR     | SOIC         | D               | 8    | 2500 | 353.0       | 353.0      | 32.0        |
| OPA4196IDR     | SOIC         | D               | 14   | 2500 | 353.0       | 353.0      | 32.0        |
| OPA4196IDRG4   | SOIC         | D               | 14   | 2500 | 353.0       | 353.0      | 32.0        |

## TUBE

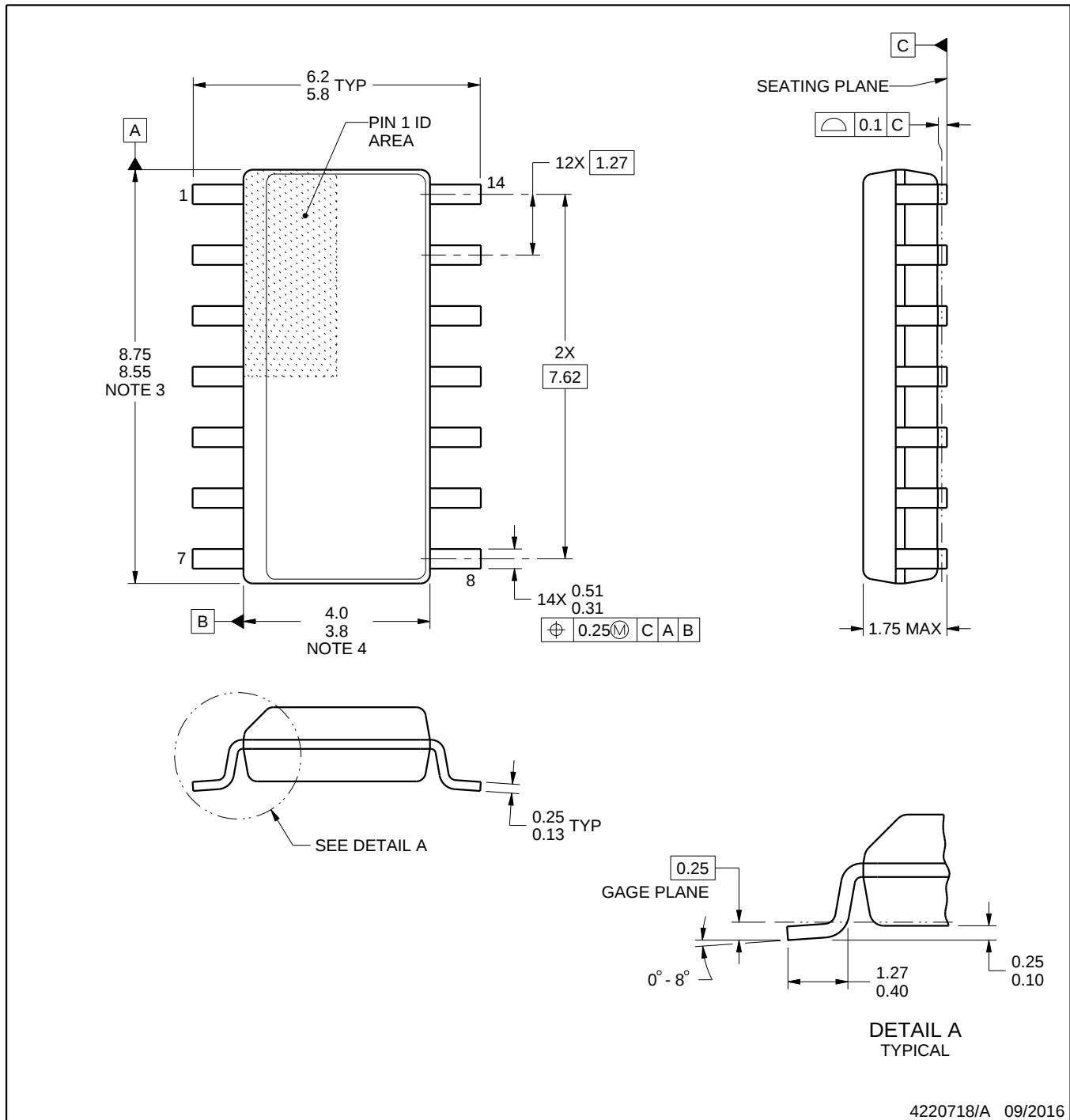


\*All dimensions are nominal

| Device        | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (μm) | B (mm) |
|---------------|--------------|--------------|------|-----|--------|--------|--------|--------|
| OPA196ID      | D            | SOIC         | 8    | 75  | 506.6  | 8      | 3940   | 4.32   |
| OPA196ID.B    | D            | SOIC         | 8    | 75  | 506.6  | 8      | 3940   | 4.32   |
| OPA2196ID     | D            | SOIC         | 8    | 75  | 506.6  | 8      | 3940   | 4.32   |
| OPA2196ID.B   | D            | SOIC         | 8    | 75  | 506.6  | 8      | 3940   | 4.32   |
| OPA2196IDG4   | D            | SOIC         | 8    | 75  | 506.6  | 8      | 3940   | 4.32   |
| OPA2196IDG4.B | D            | SOIC         | 8    | 75  | 506.6  | 8      | 3940   | 4.32   |
| OPA4196ID     | D            | SOIC         | 14   | 50  | 506.6  | 8      | 3940   | 4.32   |
| OPA4196ID.B   | D            | SOIC         | 14   | 50  | 506.6  | 8      | 3940   | 4.32   |

**D0014A****PACKAGE OUTLINE****SOIC - 1.75 mm max height**

SMALL OUTLINE INTEGRATED CIRCUIT



4220718/A 09/2016

**NOTES:**

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.

# EXAMPLE BOARD LAYOUT

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE  
SCALE:8X



SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

## EXAMPLE STENCIL DESIGN

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:8X

4220718/A 09/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.



## PACKAGE OUTLINE

**SOIC - 1.75 mm max height**

SMALL OUTLINE INTEGRATED CIRCUIT



1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.

**D0008A**

**SOIC - 1.75 mm max height**

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:8X



## SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

## EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE  
BASED ON .005 INCH [0.125 MM] THICK STENCIL  
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.



# EXAMPLE BOARD LAYOUT

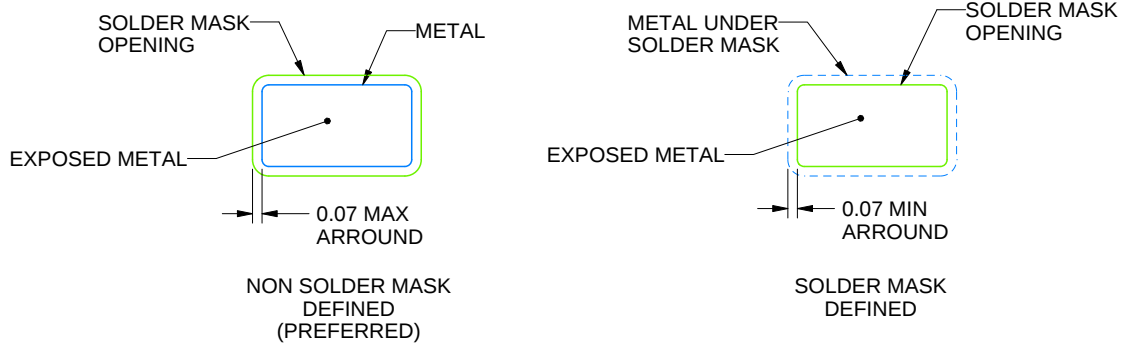
DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:15X



SOLDER MASK DETAILS

4214839/K 08/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

## EXAMPLE STENCIL DESIGN

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR

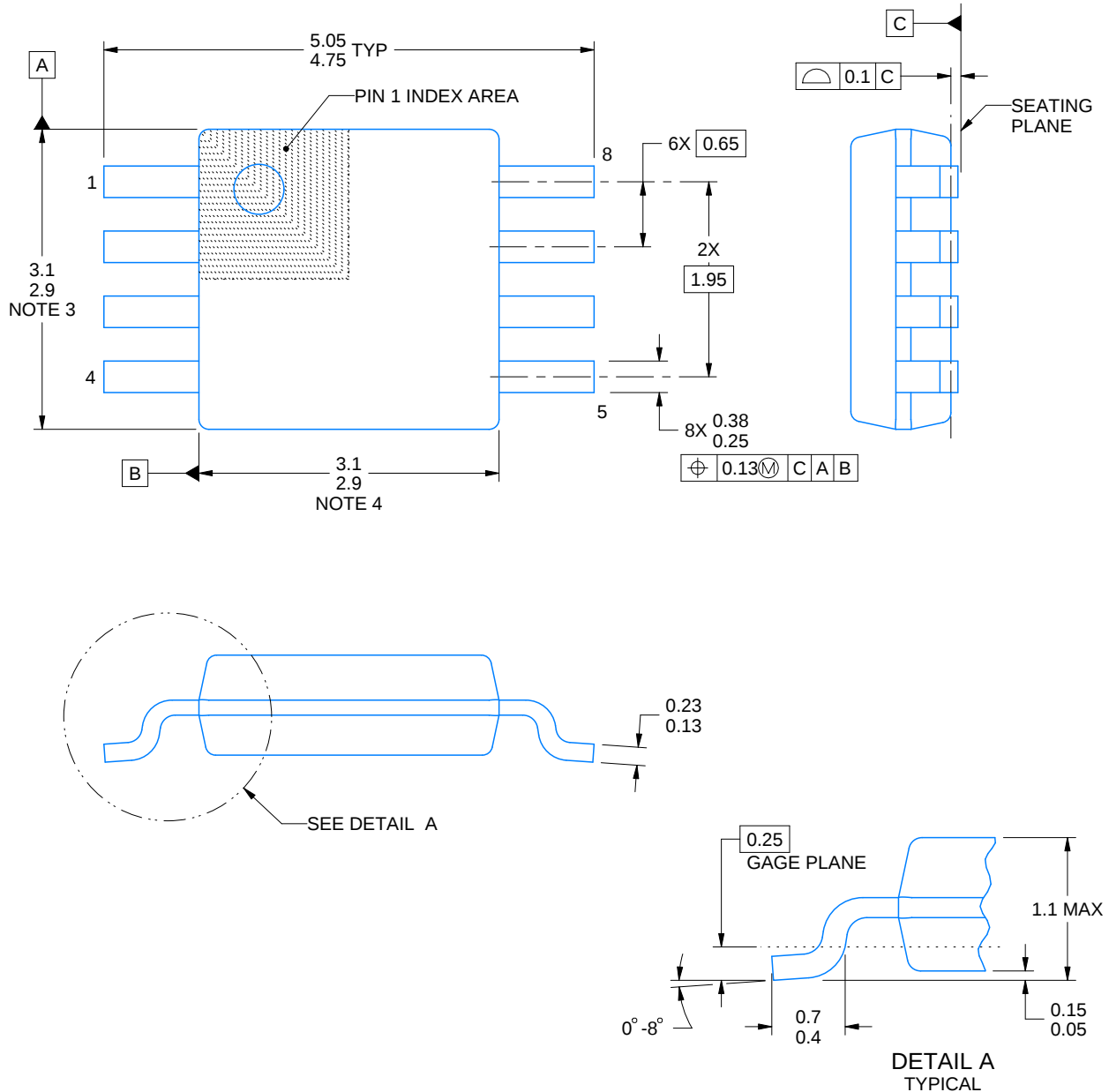
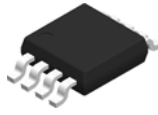


SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:15X

4214839/K 08/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.



4214862/A 04/2023

NOTES:

PowerPAD is a trademark of Texas Instruments.

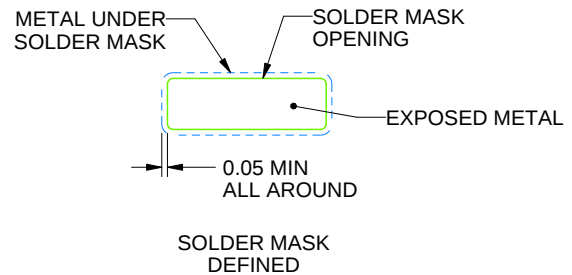
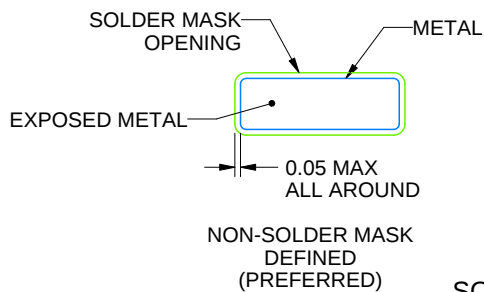
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.

# EXAMPLE BOARD LAYOUT

DGK0008A

™ VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



SOLDER MASK DETAILS

4214862/A 04/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.

## EXAMPLE STENCIL DESIGN

DGK0008A

<sup>TM</sup> VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
SCALE: 15X

4214862/A 04/2023

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

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