TEXAS INSTRUMENTS
OPA210, OPA2210
JAJSG49H – SEPTEMBER 2018 – REVISED AUGUST 2021

OPAx210 2.2nV/√Hz、高精度、低消費電力 36V オペアンプ

1 特長

- 高精度のスーパーベータ入力性能:
  - 低オフセット電圧:5μV (標準値)
  - 非常に低いドリフト:0.1μV/℃ (標準値)
  - 低入力バイアス電流:0.3nA (標準値)
- 超低ノイズ:
  - 0.1Hz～10Hz のノイズ:90μV$_{PP}$
  - 低い電圧ノイズ:1kHz 時に 2.2nV/√Hz
- 高い CMRR:132 dB (最小値)
- ゲイン帯域幅積:18MHz
- スルーレート:6.4 V/μs
- 低い静止電流:2.5mA/ チャネル (最大値)
- 短絡電流:±65mA
- 広い電源電圧範囲:±2.25V～±18V
- 位相反転なし
- レール・ツー・レール出力
- 業界標準パッケージ

2 アプリケーション

- 超音波スキャナ
- マルチパラメータ・メディカル・モニタ
- 商用ネットワークとサーバーの PSU (電源)
- 半導体テスト
- スペクトル・アナライザ
- 実験室およびフィールド計測
- データ・アクイジション (DAQ)
- 業務用マイク / ワイヤレス・システム

3 概要

OPA210 および OPA2210 (OPAx210) は次世代の OPAx209 オペアンプです。OPAx210 高精度オペアンプは、TI の高精度スーパーベータ相補型バイポーラ半導体プロセスで製造され、非常に低いフリッカ・ノイズ、低いオフセット電圧、低いオフセット電圧温度ドリフトを実現しています。

OPAx210 は非常に低い電圧ノイズ密度 (2.2nV/√Hz) を実現し、消費電流はアンプごとにわずか 2.5 mA (最大値) です。また、レール・ツー・レールの出力スイングが可能なため、ダイナミック・レンジを最大限に拡大できます。

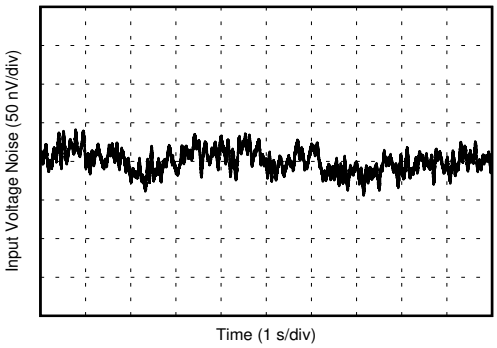
高精度データ収集アプリケーションでは、OPAx210 は 10V の出力スイングでも、16 ビット精度へ高速にセトリングできます。優れた AC 性能と小さなオフセット (全温度範囲で最大 35μV) と小さなドリフト (全温度範囲で最大 0.6μV/℃) を兼ね備える OPAx210 は、高速高精度アプリケーションに非常に適しています。

OPAx210 は ±2.25V～±18V のデュアル電源、または 4.5V～36V のシングル電源という広い電圧範囲と、-40℃～+125℃の温度範囲で動作が規定されています。

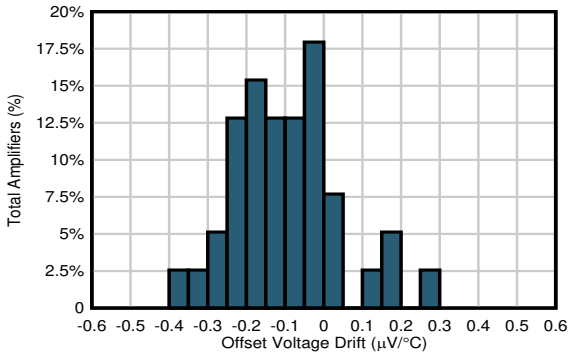
製品情報

部品番号	パッケージ(1)	本体サイズ (公称)
OPA210	SOIC (8)	2.90mm×1.60mm
	SOT-23 (5)	2.90mm × 1.60mm
	VSSOP (8)	3.00mm × 3.00mm
OPA2210	SOIC (8)	4.90mm × 3.91mm
	VSSOP (8)	3.00mm × 3.00mm
	WSON (8)	3.00mm × 3.00mm

(1) 提供されているすべてのパッケージについては、データシートの末尾にあるパッケージ・オプションについての付録を参照してください。



OPAx210 0.1Hz～10Hz のノイズ



OPAx210 オフセット電圧ドリフトの分布

英語版の TI 製品についての情報を翻訳したこの資料は、製品の概要を確認する目的で便宜的に提供しているものです。該当する正式な英語版の最新情報は、www.ti.com で閲覧でき、その内容が常に優先されます。TI では翻訳の正確性および妥当性につきましては一切保証いたしません。実際の設計などの前には、必ず最新版の英語版をご参照くださいますようお願いいたします。

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4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision G (April 2021) to Revision H (August 2021) — **Page**

- OPA210 DBV (SOT-23-5) および DGK (VSSOP-8) パッケージを事前情報 (プレビュー) から量産データ (アクティブ)に変更 ... 1

Changes from Revision F (January 2021) to Revision G (April 2021) — **Page**

- OPA210 D (SOIC-8) パッケージを事前情報 (プレビュー) から量産データ (アクティブ) に変更 ... 1
- OPA210 DBV (SOT-23-5) パッケージを事前情報 (プレビュー) として追加 ... 1

Changes from Revision E (Novembver 2020) to Revision F (January 2021) — **Page**

- OPA210 デバイスの D および DGK パッケージを事前情報 (プレビュー) として追加 ... 1

Changes from Revision D (January 2020) to Revision E (November 2020) — **Page**

- OPA2210 DRG パッケージを事前情報 (プレビュー) から量産データ (アクティブ) に変更 ... 1

Changes from Revision C (September 2019) to Revision D (January 2020) — **Page**

- OPA2210 DRG パッケージを事前情報 (プレビュー) としてデータシートに追加 ... 1

Changes from Revision B (March 2019) to Revision C (September 2019) — **Page**

- 検索を容易にするために super-ß をスーパーベータに変更 ... 1
- SOIC パッケージを追加 ... 1

Changes from Revision A (December 2018) to Revision B (February 2019) — **Page**

- Changed "OPAx145" to "OPA2210" ... 19
- Fixed link to TIDA-01427 ... 22

Changes from Revision * (September 2018) to Revision A (December 2018) — **Page**

- 量産データのデータシートの初版 ... 1

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5 Pin Configuration and Functions

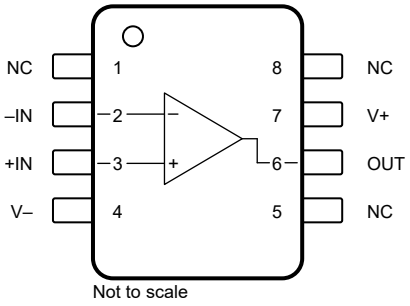


図 5-1. OPA210: D (8-Pin SOIC) and DGK (8-Pin VSSOP) Packages, Top View

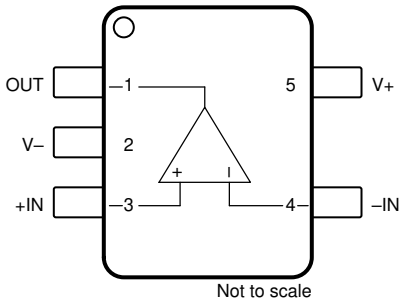


図 5-2. OPA210: DBV (5-Pin SOT-23) Package, Top View

表 5-1. Pin Functions: OPA210

PIN			I/O	DESCRIPTION
NAME	SOIC, VSSOP	SOT-23		
–IN	2	4	I	Inverting input
+IN	3	3	I	Noninverting input
NC	1, 5, 8	—	—	No internal connection
OUT	6	1	O	Output
V–	4	2	—	Negative (lowest) power supply
V+	7	5	—	Positive (highest) power supply

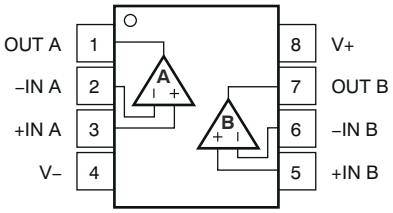


図 5-3. OPA2210: D (SOIC-8), DGK (VSSOP-8), and DRG (WSON-8) Packages, Top View

表 5-2. Pin Functions: OPA2210

PIN		I/O	DESCRIPTION
NAME	NO.		
–IN A	2	I	Inverting input, channel A
+IN A	3	I	Noninverting input, channel A
–IN B	6	I	Inverting input, channel B
+IN B	5	I	Noninverting input, channel B
OUT A	1	O	Output, channel A
OUT B	7	O	Output, channel B
V–	4	—	Negative (lowest) power supply
V+	8	—	Positive (highest) power supply

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
Voltage	Supply voltage, V_S = (V+) – (V–)			40	V
	Signal input pins(2)		(V–) – 0.5	(V+) + 0.5	
	Signal input pins	Differential		1	
Current	Signal input pins(2)		–10	10	mA
	Output short circuit(3)		Continuous		
Temperature	Junction, T_J			150	°C
	Storage temperature, T_{stg}		–65	150	

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the de vice. Theseare stress ratings only, which do not imply functional operation of the device at these or anyother conditions beyond those indicated under *Recommended OperatingConditions*. Exposure to absolute-maximum-rated conditions for extended periods mayaffect device reliability.
(2) For input voltages beyond the power-supply rails, voltage orcurrent must be limited.
(3) Short circuit to ground, one amplifier per package.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±4000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1500	

(1) JEDEC document JEP155 states that 500-V HBM allows safemanufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safemanufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	MAX	UNIT
Specified voltage, V_S	±2.25	±18	V
Specified temperature	–40	125	°C
Operating temperature, T_A	–55	150	°C

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6.4 Thermal Information: OPA210

THERMAL METRIC[1]		OPA210			UNIT
		D (SOIC)	DGK (VSSOP)	DBV (SOT-23)	
		8 PINS	8 PINS	5 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	131.2	171.3	180.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	71.6	64.7	67.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	74.6	92.4	102.1	°C/W
ψ_{JT}	Junction-to-top characterization parameter	22.4	10.4	10.4	°C/W
ψ_{JB}	Junction-to-board characterization parameter	73.8	90.9	100.3	°C/W
$R_{\theta JC(bottom)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	N/A	°C/W

(1) For more information about traditional and new thermalmetrics, see the Semiconductor and ICPackage Thermal Metrics application report.

6.5 Thermal Information: OPA2210

THERMAL METRIC[1]		OPA2210			UNIT
		D (SOIC)	DGK (VSSOP)	DRG (SON)	
		8 PINS	8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	126.1	132.7	52.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	65.7	38.5	51.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	69.5	52.1	24.8	°C/W
ψ_{JT}	Junction-to-top characterization parameter	17.4	2.4	1.1	°C/W
ψ_{JB}	Junction-to-board characterization parameter	68.9	52.8	24.8	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	n/a	9.0	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

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6.6 Electrical Characteristics

at V_S = ±15 V, T_A = 25°C, R_L = 10 kΩ connected to midsupply, and V_{CM} =V_{OUT} = midsupply (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
OFFSET VOLTAGE							
V_{OS}	Input offset voltage	V_S = ±15 V, V_{CM} = 0 V			±5	±35	µV
dV_{OS}/dT	Input offset voltage drift	T_A = –40°C to 125°C			±0.1	±0.5	µV/°C
V_{OS} - matching	Input offset voltage matching				±5	±35	µV
PSRR	vs power supply	V_S = ±2.25 V to ±18 V	T_A = 25°C		0.05	0.5	µV/V
			T_A = –40°C to 125°C			±1	
	Channel separation	DC			±0.1		µV/V
INPUT BIAS OPERATION							
I_B	Input bias current	V_{CM} = 0 V	T_A = 25°C		±0.3	±2	nA
			T_A = –40°C to 85°C			±4	
			T_A = –40°C to 125°C			±7	
I_{OS}	Input offset current	V_{CM} = 0 V	T_A = 25°C		±0.1	±2	nA
			T_A = –40°C to 85°C			±4	
			T_A = –40°C to 125°C			±7	
NOISE							
$e_{n\ p-p}$	Input voltage noise	f = 0.1 Hz to 10 Hz			0.09		μV_{PP}
e_n	Noise density	f = 10 Hz			2.5		nV/√Hz
		f = 100 Hz			2.25		
		f = 1 kHz			2.2		
I_n	Input current noise density	f = 1 kHz			400		fA/√Hz
INPUT VOLTAGE RANGE							
V_{CM}	Common-mode voltage range			(V–) + 1.5		(V+) – 1.5	V
CMRR	Common-mode rejection ratio	(V–) + 1.5 V < V_{CM} < (V+) – 1.5 V		132	140		dB
		(V–) + 1.5 V < V_{CM} < (V+) – 1.5 V, T_A = –40°C to 125°C		120	130		
INPUT IMPEDANCE							
	Differential				400 || 9		kΩ || pF
	Common-mode				10^9 || 0.5		Ω || pF
OPEN-LOOP GAIN							
A_{OL}	Open-loop voltage gain	(V–) + 0.2 V < V_O < (V+) – 0.2 V, R_L = 10 kΩ	T_A = 25°C	126	132		dB
			T_A = –40°C to 125°C	120			
		(V–) + 0.6 V < V_O < (V+) – 0.6 V, R_L = 600 Ω(1)	T_A = 25°C	114	120		
			T_A = –40°C to 85°C	110			
FREQUENCY RESPONSE							
GBW	Gain bandwidth product				18		MHz
SR	Slew rate				6.4		V/µs
	Phase margin (Φm)	R_L = 10 kΩ, C_L = 25 pF			80		degrees
t_S	Settling time	0.1%, G = –1, 10-V step, C_L = 100 pF			2.1		µs
		0.0015% (16-bit), G = –1, 10-V step, C_L = 100 pF			2.6		
	Overload recovery time	G = –10			0.5		µs
	Total harmonic distortion + noise (THD+N)	G = +1, f = 1 kHz, V_O = 20 V_{PP}, 600 Ω			0.000025		%

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6.6 Electrical Characteristics (continued)

at V_S = ±15 V, T_A = 25°C, R_L = 10 kΩ connected to midsupply, and V_{CM} = V_{OUT} = midsupply (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
OUTPUT							
	Voltage output swing	R_L = 10 kΩ, A_{OL} > 130 dB		(V–) + 0.2		(V+) – 0.2	V
		R_L = 600 Ω, A_{OL} > 114 dB		(V–) + 0.6		(V+) – 0.6	
		R_L = 10 kΩ, A_{OL} > 120 dB, T_A = –40°C to 125°C		(V–) + 0.2		(V+) – 0.2	
I_{SC}	Short-circuit current	V_S = ±18 V			±65		mA
C_{LOAD}	Capacitive load drive (stable operation)			See セクション 6.7			
Z_O	Open-loop output impedance			See セクション 6.7			
POWER SUPPLY							
I_Q	Quiescent current (per amplifier)	I_O = 0 A	T_A = 25°C		2.2	2.5	mA
			T_A = –40°C to 125°C			3.25	

(1) Temperature range limited by thermal performance of the package.

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6.7 Typical Characteristics

at T_A = 25°C, V_S = ±15 V, R_L = 10 kΩ connected to midsupply, and V_{CM} = V_{OUT} = midsupply (unless otherwise noted)

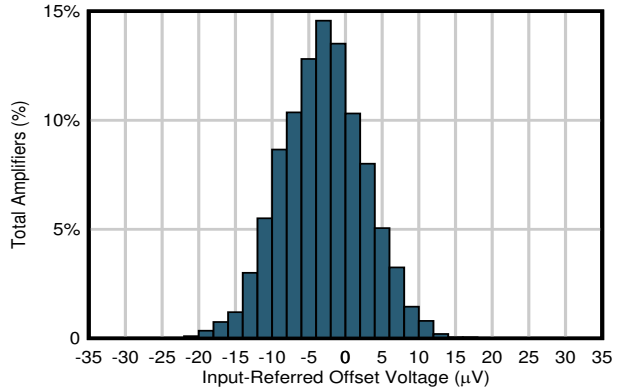


図 6-1. Offset Voltage Production Distribution

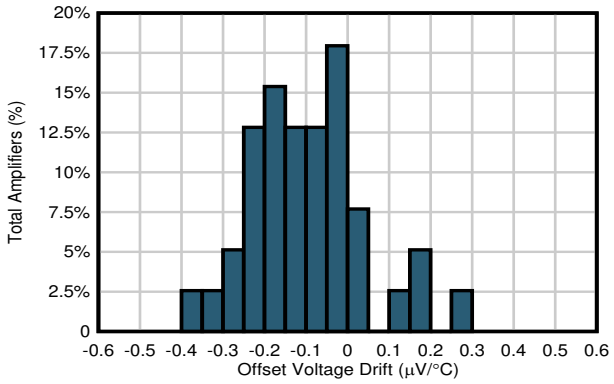


図 6-2. Offset Voltage Drift Distribution

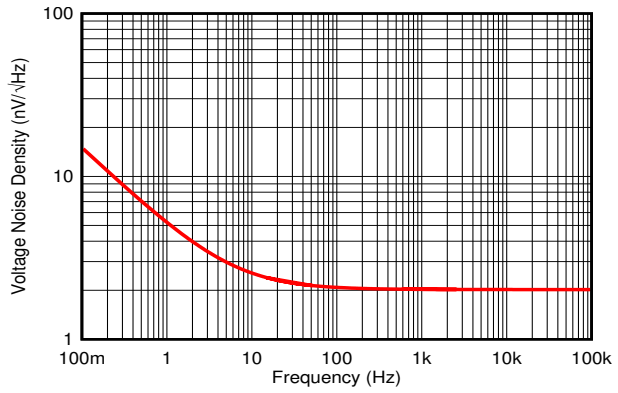


図 6-3. Input Voltage Noise Spectral Density vs Frequency

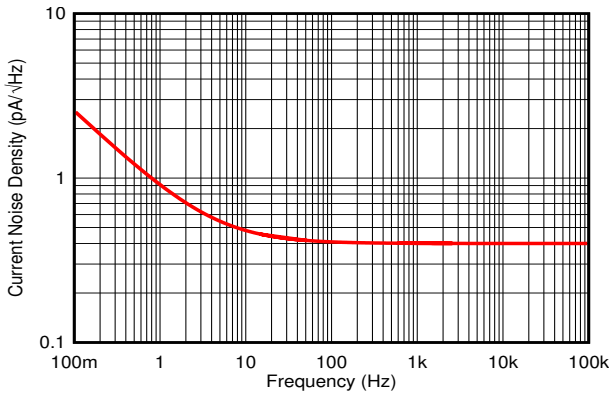


図 6-4. Input Current Noise Spectral Density vs Frequency

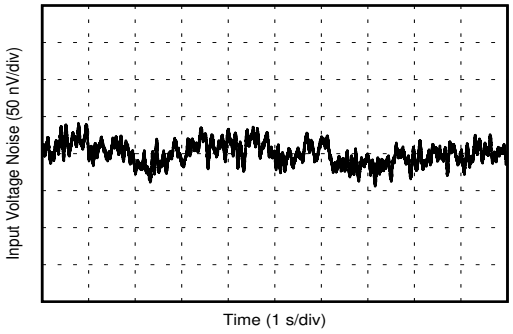
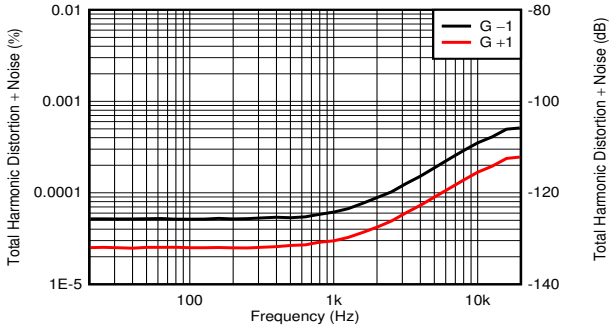


図 6-5. 0.1-Hz to 10-Hz Voltage Noise



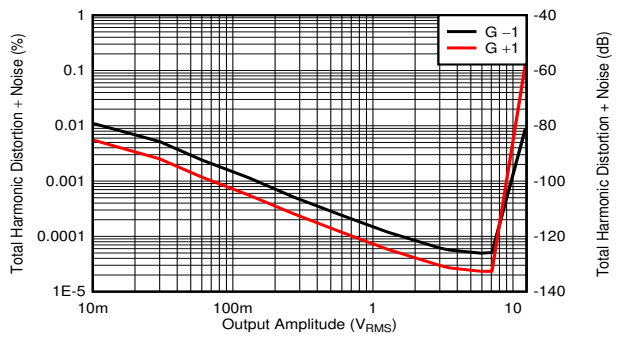
V_{OUT} = 3.5 V_{RMS} R_L = 600 Ω

図 6-6. THD+N Ratio vs Frequency

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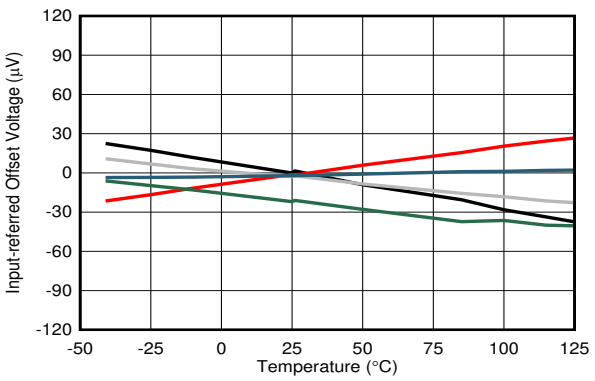
6.7 Typical Characteristics (continued)

at T_A = 25°C, V_S = ±15 V, R_L = 10 kΩ connected to midsupply, and V_{CM} = V_{OUT} = midsupply (unless otherwise noted)



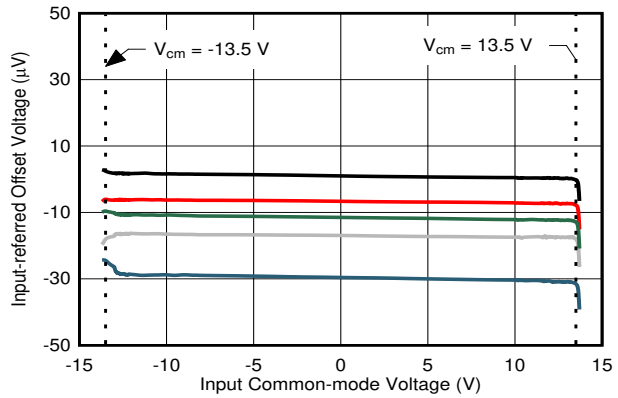
f = 1 kHz R_L = 600 Ω

図 6-7. THD+N vs Output Amplitude



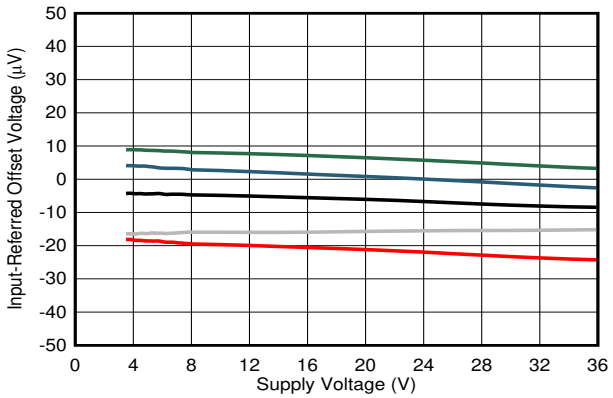
5 typical units

図 6-8. Input Offset Voltage vs Temperature



5 typical units

図 6-9. Offset Voltage vs Common-Mode Voltage



5 typical units

図 6-10. Offset Voltage vs Supply Voltage

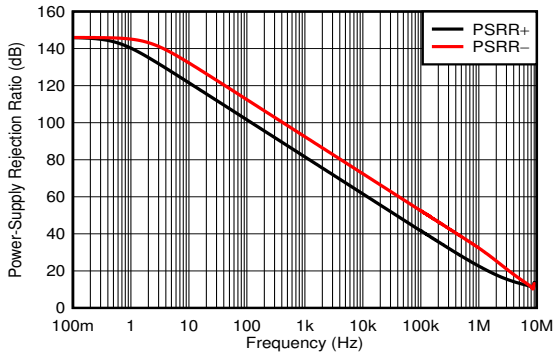


図 6-11. PSSR vs Frequency

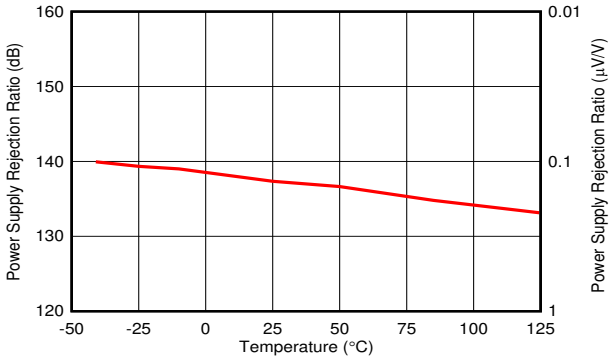


図 6-12. PSRR vs Temperature

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6.7 Typical Characteristics (continued)

at T_A = 25°C, V_S = ±15 V, R_L = 10 kΩ connected to midsupply, and V_{CM} = V_{OUT} = midsupply (unless otherwise noted)

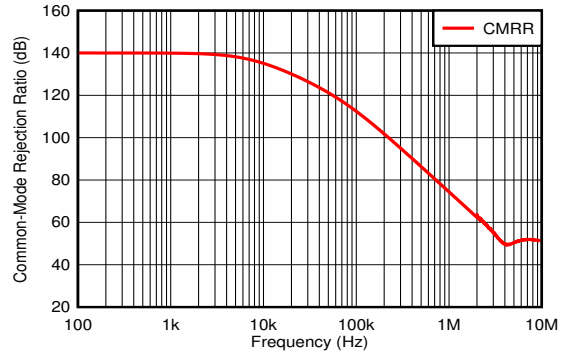


図 6-13. CMRR vs Frequency

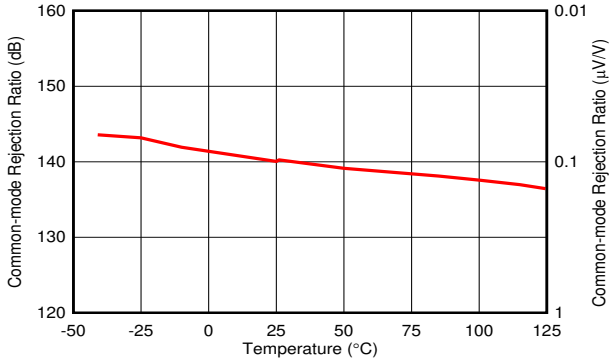


図 6-14. CMRR vs Temperature

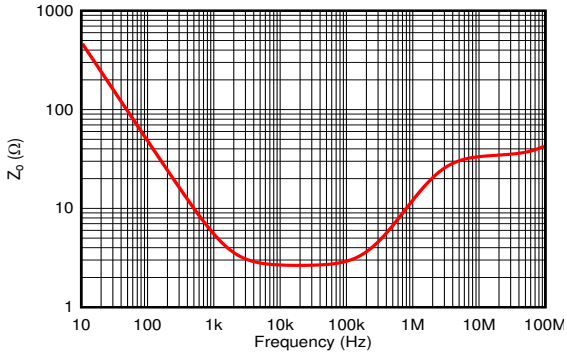


図 6-15. Open-Loop Output Impedance vs Frequency

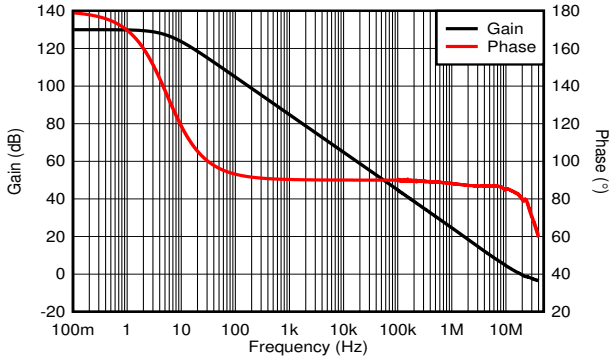


図 6-16. Open-Loop Gain and Phase vs Frequency

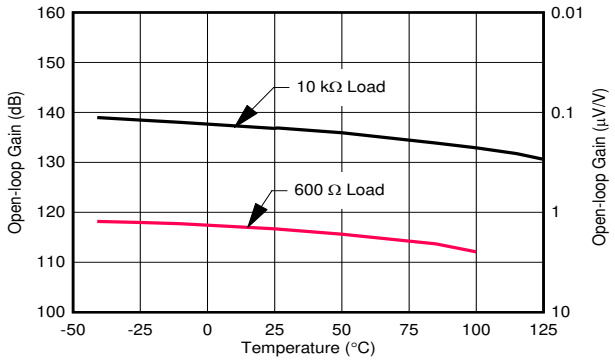


図 6-17. Open-Loop Gain vs Temperature

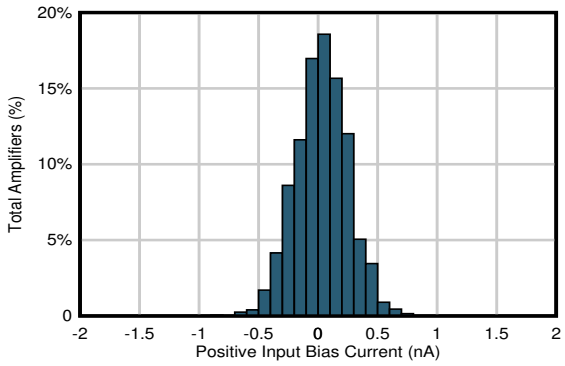


図 6-18. Positive Input Bias Current Production Distribution

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6.7 Typical Characteristics (continued)

at T_A = 25°C, V_S = ±15 V, R_L = 10 kΩ connected to midsupply, and V_{CM} = V_{OUT} = midsupply (unless otherwise noted)

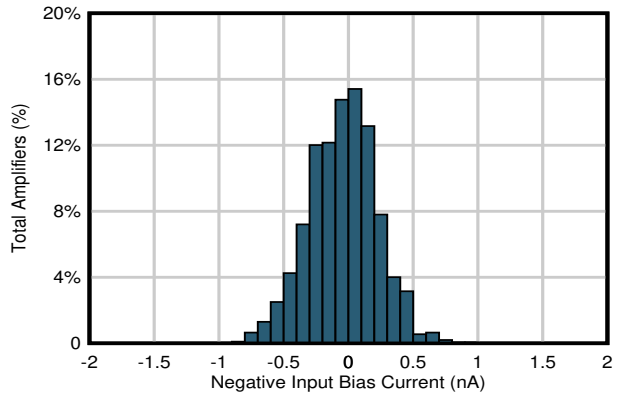


図 6-19. Negative Input Bias Current Production Distribution

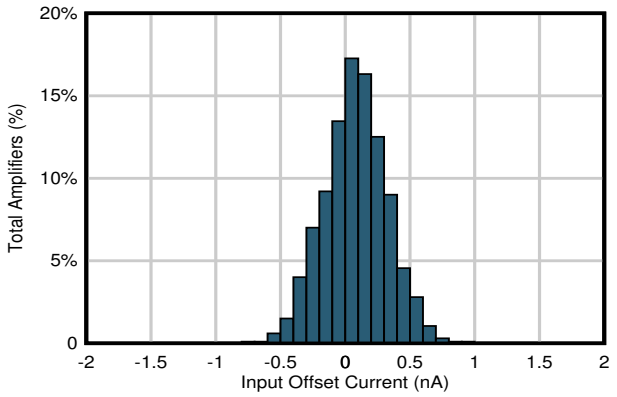


図 6-20. Input Offset Current Production Distribution

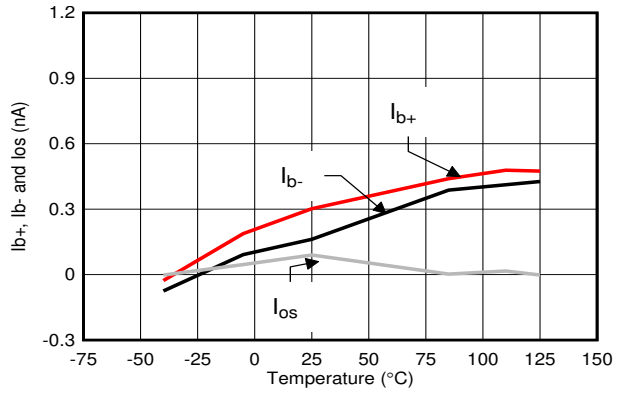


図 6-21. Input Bias and Input Offset Currents vs Temperature

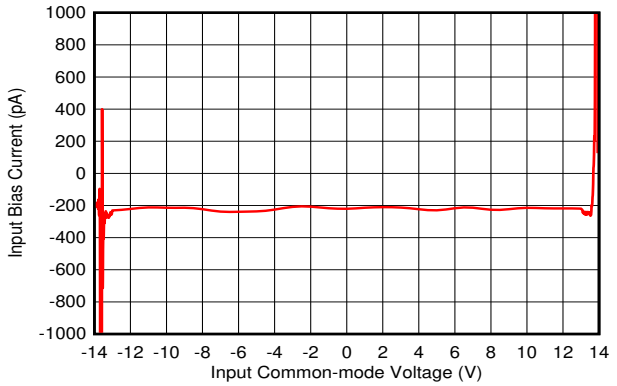


図 6-22. Positive Input Bias Current vs Common-Mode Voltage

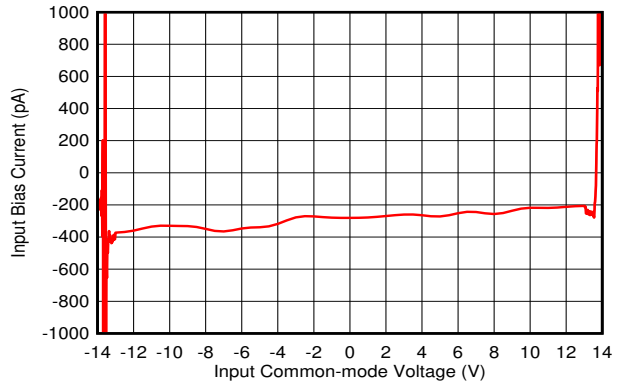


図 6-23. Negative Input Bias Current vs Common-Mode Voltage

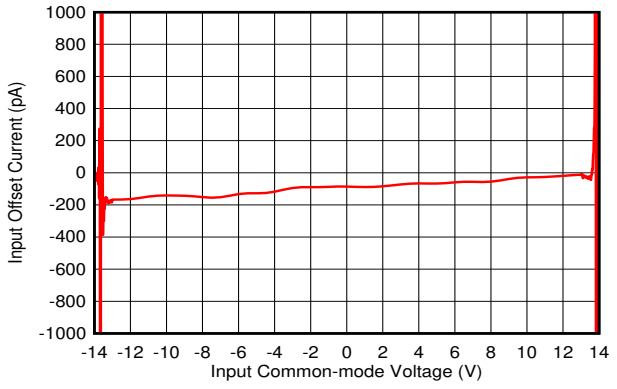


図 6-24. Input Offset Current vs Common-Mode Voltage

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6.7 Typical Characteristics (continued)

at T_A = 25°C, V_S = ±15 V, R_L = 10 kΩ connected to midsupply, and V_{CM} = V_{OUT} = midsupply (unless otherwise noted)

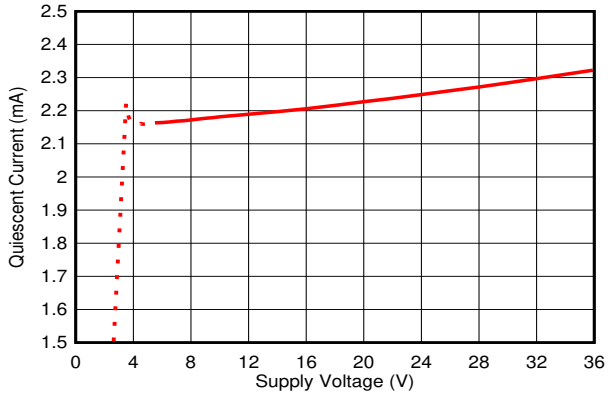


図 6-25. Quiescent Current vs Supply Voltage

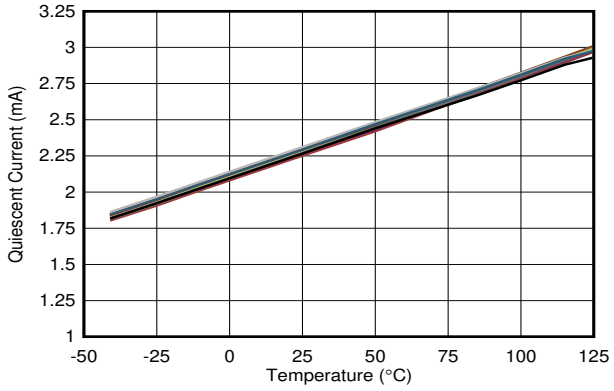
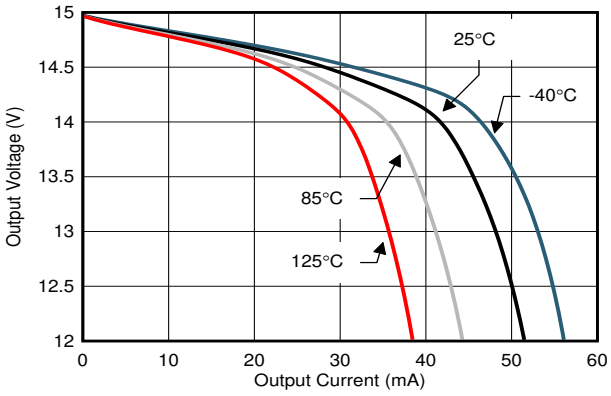
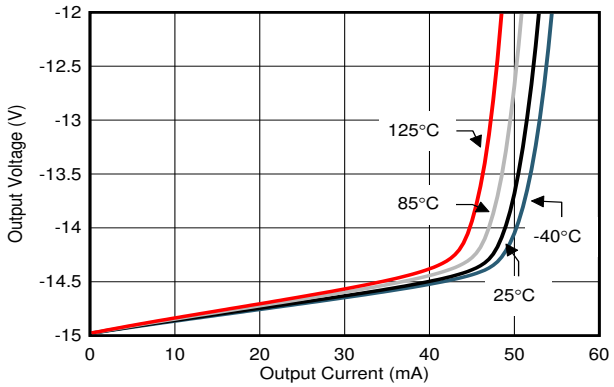


図 6-26. Quiescent Current vs Temperature



A.

図 6-27. Output Voltage vs Output Current (Sourcing)



A.

図 6-28. Output Voltage vs Output Current (Sinking)

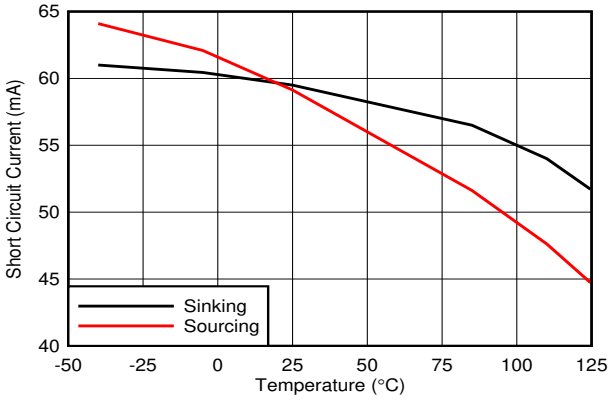


図 6-29. Short-Circuit Current vs Temperature

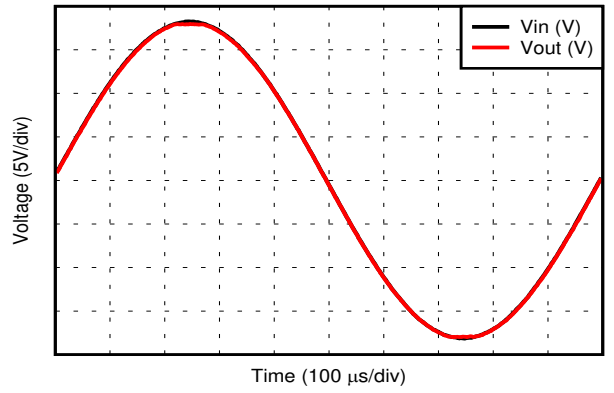
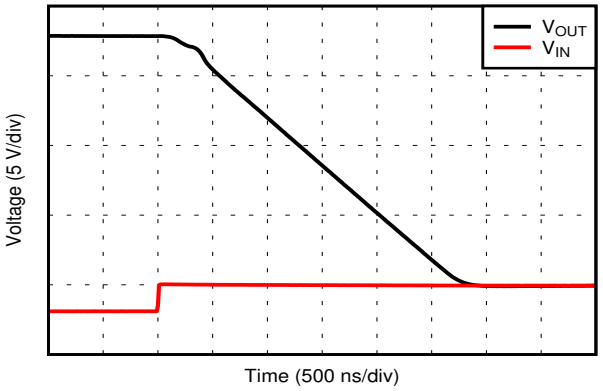


図 6-30. No Phase Reversal

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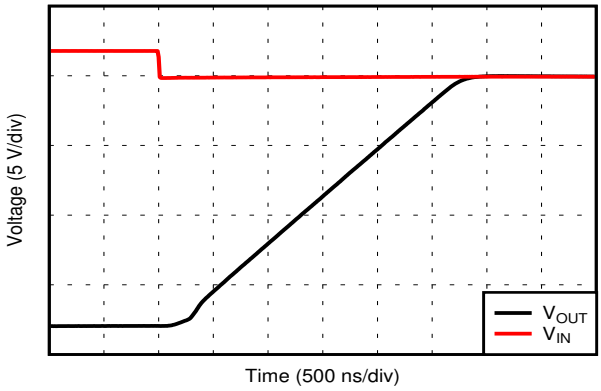
6.7 Typical Characteristics (continued)

at T_A = 25°C, V_S = ±15 V, R_L = 10 kΩ connected to midsupply, and V_{CM} = V_{OUT} = midsupply (unless otherwise noted)



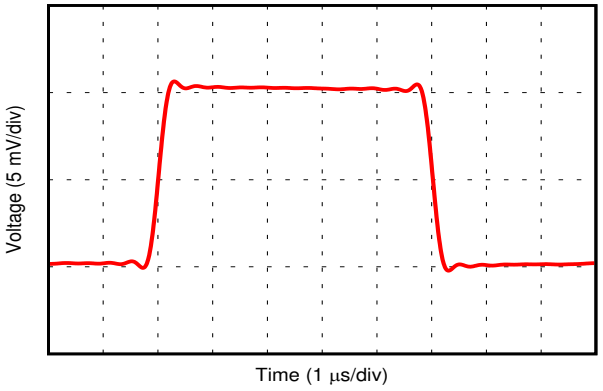
G = –10

図 6-31. Positive Overload Recovery



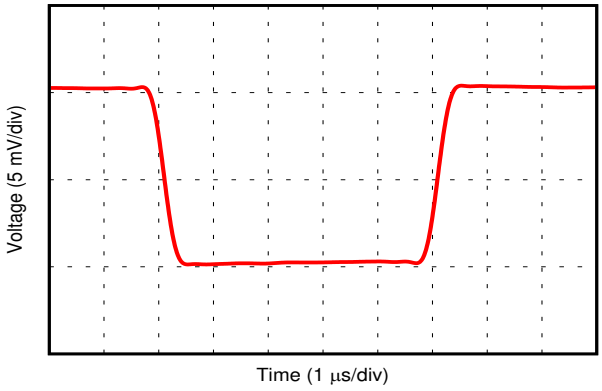
G = –10

図 6-32. Negative Overload Recovery



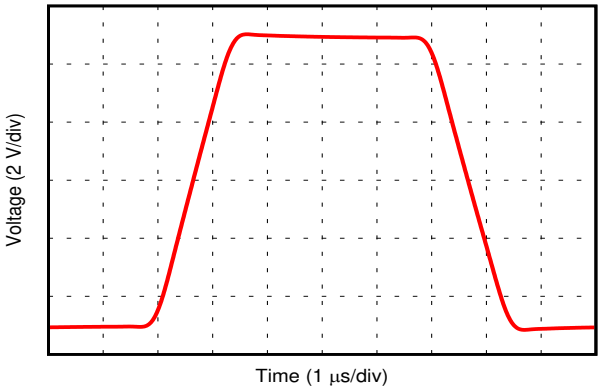
G = +1 10-mV step, C_L = 100 pF, R_L = 600 Ω

図 6-33. Small-Signal Step Response



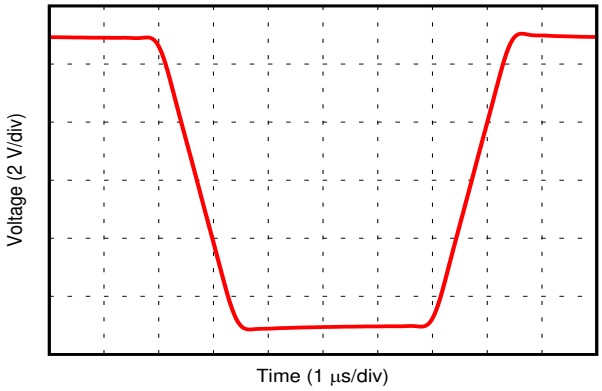
G = –1 10-mV step, C_L = 100 pF, R_L = 600 Ω

図 6-34. Small-Signal Step Response



G = +1 10-V step, C_L = 100 pF, R_L = 600 Ω

図 6-35. Large-Signal Step Response



G = –1 10-V step, C_L = 100 pF, R_L = 600 Ω

図 6-36. Large-Signal Step Response

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6.7 Typical Characteristics (continued)

at T_A = 25°C, V_S = ±15 V, R_L = 10 kΩ connected to midsupply, and V_{CM} = V_{OUT} = midsupply (unless otherwise noted)

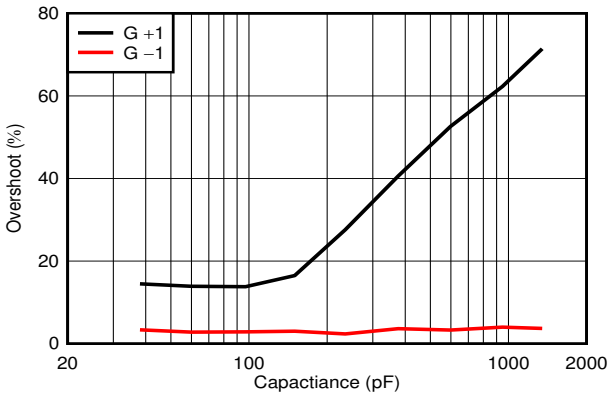
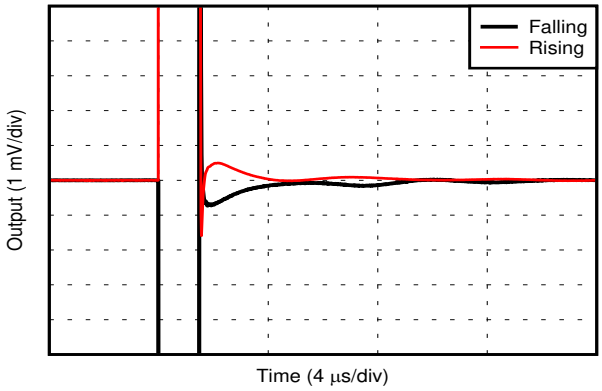
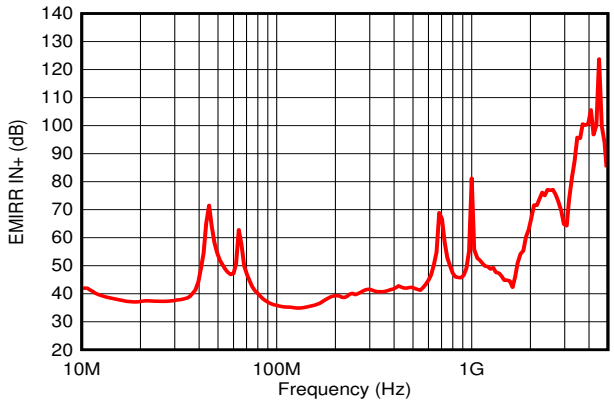


図 6-37. Small-Signal Overshoot vs Capacitive Load



10-V step

図 6-38. Settling Time



P_{RF} = –10 dBm

図 6-39. EMIRR vs Frequency

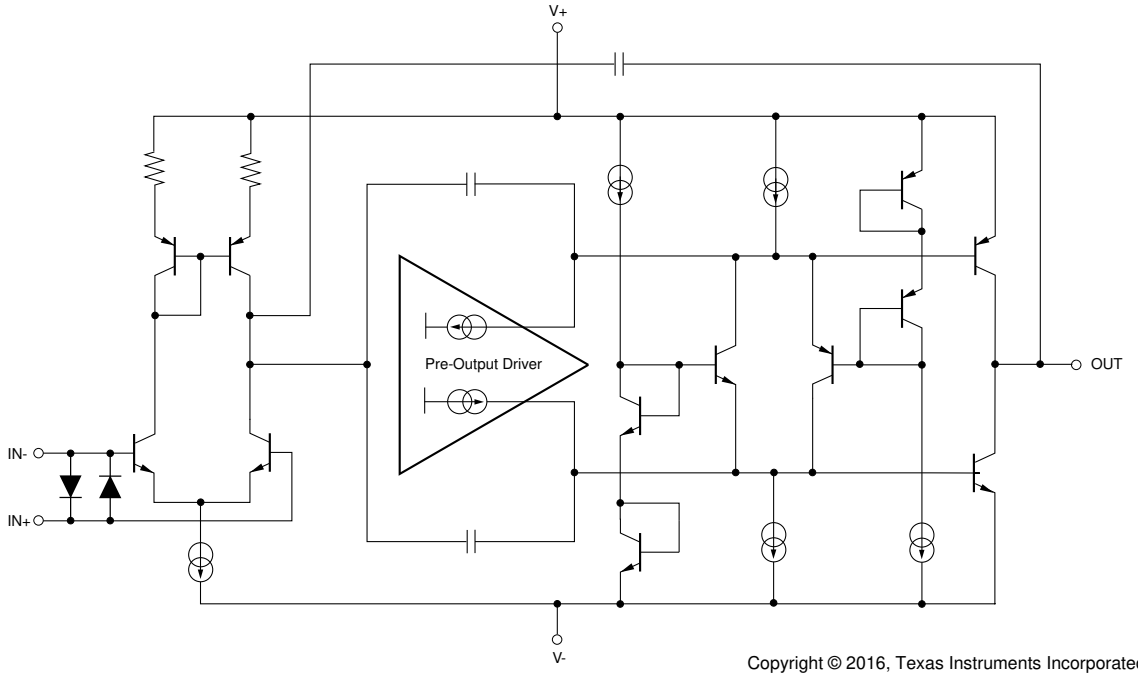
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7 Detailed Description

7.1 Overview

The OPAx210 are the next generation of the OPAx209 operational amplifiers. The OPAx210 offer improved input offset voltage, offset voltage temperature drift, input bias current, and lower 1/f noise corner frequency. In addition, these devices offer excellent overall performance with high CMRR, PSRR, and A_{OL}.The OPAx210 precision operational amplifiers are unity-gain stable, and free from unexpected output and phase reversal. Applications with noisy or high-impedance power supplies require decoupling capacitors placed close to the device pins. In most cases, 0.1-µF capacitors are adequate. セクション 7.2 shows a simplified schematic of the OPAx210. The die uses a SiGe bipolar process and contains 180 transistors.

7.2 Functional Block Diagram



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7.3 Feature Description

7.3.1 Operating Voltage

The OPAx210 op amps can be used with single or dual supplies within an operating range of V_S = 4.5 V (±2.25 V) up to 36 V (±18 V).

CAUTION
Supply voltages greater than 40 V total can permanently damage the device.

In addition, key parameters are specified over the temperature range of T_A = –40°C to +125°C. Parameters that vary significantly with operating voltage or temperature are shown in *セクション 6.7*.

7.3.2 Input Protection

The input pins of the OPAx210 are protected from excessive differential voltage with back-to-back diodes, as shown in 図 7-1. In most circuit applications, the input protection circuitry has no consequence. However, in low-gain or G = 1 circuits, fast-ramping input signals can forward-bias these diodes because the output of the amplifier cannot respond rapidly enough to the input ramp. This effect is illustrated in 図 6-35 and 図 6-36 in *セクション 6.7*. If the input signal is fast enough to create this forward-bias condition, the input signal current must be limited to 10 mA or less. If the input signal current is not inherently limited, an input series resistor can be used to limit the signal input current. This input series resistor degrades the low-noise performance of the OPAx210. See *セクション 7.3.3* for further information on noise performance.

図 7-1 shows an example configuration that implements a current-limiting feedback resistor.

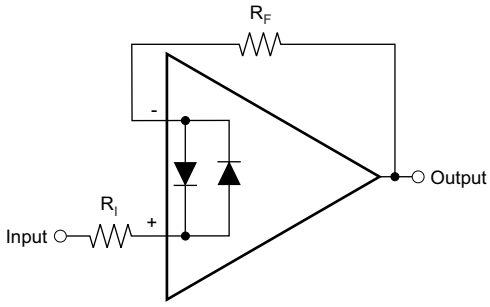


図 7-1. Pulsed Operation

7.3.3 Noise Performance

図 7-2 shows the total circuit noise for varying source impedances with the op amp in a unity-gain configuration (no feedback resistor network, and therefore, no additional noise contributions). Two different op amps are shown with the total circuit noise calculated. The OPAx210 have very low voltage noise, making these devices a great choice for low source impedances (less than 2 kΩ). As a comparable, precision FET-input op amp (very low current noise), the OPA827 has somewhat higher voltage noise, but lower current noise. The device provides excellent noise performance at moderate to high source impedance (10 kΩ and up). For source impedance lower than 300 Ω, the OPA211 may provide lower noise.

The equation in 図 7-2 shows the calculation of the total circuit noise, with these parameters:

- e_n = voltage noise,
- i_n = current noise,
- R_S = source impedance,
- k = Boltzmann's constant = 1.38 × $10^{–23}$ J/K, and
- T = temperature in kelvins

For more details on calculating noise, see *セクション 8.1.1*.

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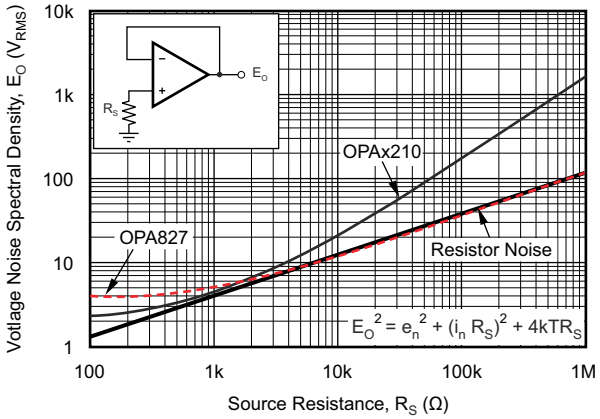


図 7-2. Noise Performance of the OPAx210 and OPA827 in Unity-Gain Buffer Configuration

7.3.4 Phase-Reversal Protection

The OPAx210 have internal phase-reversal protection. Many FET- and bipolar-input op amps exhibit a phase reversal when the input is driven beyond the linear common-mode range. This condition is most often encountered in noninverting circuits when the input is driven beyond the specified common-mode voltage range, causing the output to reverse into the opposite rail. The input circuitry of the OPAx210 prevents phase reversal with excessive common-mode voltage; instead, the output limits into the appropriate rail (see 図 6-30).

7.3.5 Electrical Overstress

Designers often ask questions about the capability of an operational amplifier to withstand electrical overstress. These questions tend to focus on the device inputs, but may involve the supply voltage pins or even the output pin. Each of these different pin functions have electrical stress limits determined by the voltage breakdown characteristics of the particular semiconductor fabrication process and specific circuits connected to the pin. Additionally, internal electrostatic discharge (ESD) protection is built into these circuits to protect them from accidental ESD events both before and during product assembly.

It is helpful to have a good understanding of this basic ESD circuitry and its relevance to an electrical overstress event. See 図 7-3 for an illustration of the ESD circuits contained in the OPAx210 (indicated by the dashed line area). The ESD protection circuitry involves several current-steering diodes connected from the input and output pins and routed back to the internal power-supply lines, where they meet at an absorption device internal to the operational amplifier. This protection circuitry is intended to remain inactive during normal circuit operation.

An ESD event produces a short duration, high-voltage pulse that is transformed into a short duration, high-current pulse as it discharges through a semiconductor device. The ESD protection circuits are designed to provide a current path around the operational amplifier core to prevent it from being damaged. The energy absorbed by the protection circuitry is then dissipated as heat.

When an ESD voltage develops across two or more of the amplifier device pins, current flows through one or more of the steering diodes. Depending on the path that the current takes, the absorption device may activate. The absorption device has a trigger, or threshold voltage, that is greater than the normal operating voltage of the OPAx210 but less than the device breakdown voltage level. After this threshold is exceeded, the absorption device quickly activates and clamps the voltage across the supply rails to a safe level.

When the operational amplifier connects into a circuit such as the one 図 7-3 shows, the ESD protection components are intended to remain inactive and not become involved in the application circuit operation. However, circumstances may arise where an applied voltage exceeds the operating voltage range of a given pin. If this condition occur, there is a risk that some of the internal ESD protection circuits may be biased on, and conduct current. Any such current flow occurs through steering diode paths and rarely involves the absorption device.

図 7-3 depicts a specific example where the input voltage, V_{IN}, exceeds the positive supply voltage, $+V_S$, by 500 mV or more. Much of what happens in the circuit depends on the supply characteristics. If $+V_S$ can sink the

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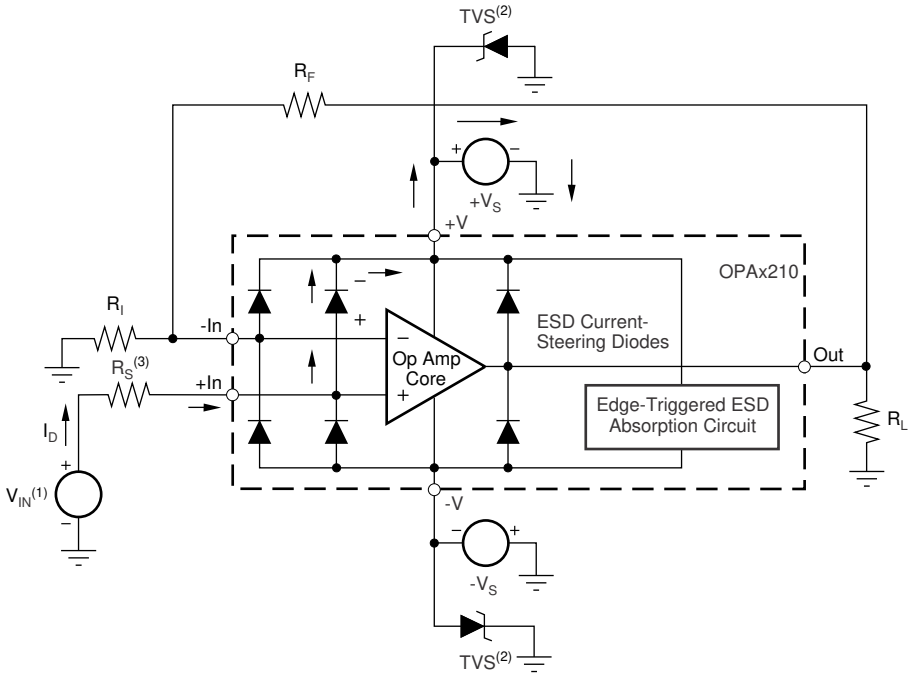
current, one of the upper input steering diodes conducts and directs current to $+V_S$. Excessively high current levels can flow with increasingly higher V_{IN}. As a result, the data sheet specifications recommend that applications limit the input current to 10 mA.

If the supply is not capable of sinking the current, V_{IN} may begin sourcing current to the operational amplifier, and then take over as the source of positive supply voltage. The danger in this case is that the voltage can rise to levels that exceed the operational amplifier absolute maximum ratings.

Another common question involves what happens to the amplifier if an input signal is applied to the input while power supplies $+V_S$, $–V_S$, or both are at 0 V.

Again, the answer depends on the supply characteristic while at 0 V, or at a level less than the input signal amplitude. If the supplies appear as high impedance, then the operational amplifier supply current may be supplied by the input source through the current steering diodes. This state is not a normal bias condition; the amplifier will not operate normally. If the supplies are low impedance, then the current through the steering diodes can become quite high. The current level depends on the ability of the input source to deliver current, and any resistance in the input path.

If there is an uncertainty about the ability of the supply to absorb this current, external transient voltage suppressor (TVS) diodes may be added to the supply pins as shown in 図 7-3. The breakdown voltage must be selected so that the diode does not turn on during normal operation. However, the breakdown voltage must be low enough so that the TVS diode conducts if the supply pin begins to rise to greater than the safe operating supply voltage level.



(1) $V_{IN} = +V_S + 500$ mV.
(2) TVS: $+V_{S(max)} > V_{TVSBR\ (Min)} > +V_S$.
(3) Suggested value approximately 1 kΩ.

図 7-3. Equivalent Internal ESD Circuitry and Relation to a Typical Circuit Application

7.4 Device Functional Modes

The OPAx210 are operational when the power-supply voltage is greater than 4.5 V (±2.25 V). The maximum power-supply voltage for the OPAx210 is 36 V (±18 V).

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8 Application and Implementation

Note

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8.1 Application Information

The OPAx210 are unity-gain stable, precision operational amplifiers with very low noise. Applications with noisy or high-impedance power supplies require decoupling capacitors close to the device pins. In most cases, 0.1-µF capacitors are adequate.

8.1.1 Basic Noise Calculations

Low-noise circuit design requires careful analysis of all noise sources. External noise sources can dominate in many cases; consider the effect of source resistance on overall op amp noise performance. Total noise of the circuit is the root-sum-square combination of all noise components.

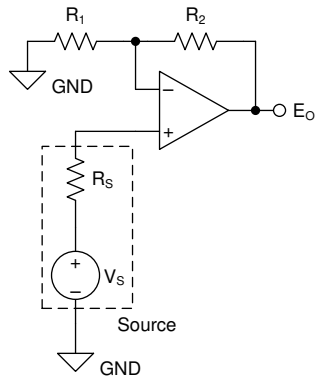
The resistive portion of the source impedance produces thermal noise proportional to the square root of the resistance. This function is plotted in 図 7-2. The source impedance is usually fixed; consequently, select the op amp and the feedback resistors to minimize the respective contributions to the total noise.

図 8-1 illustrates both noninverting **(A)** and inverting **(B)** op amp circuit configurations with gain. In circuit configurations with gain, the feedback network resistors also contribute noise. In general, the current noise of the op amp reacts with the feedback resistors to create additional noise components. However, the extremely low current noise of the OPAx210 means that the device current noise contribution can be neglected.

Generally, the feedback resistor values are chosen to make these noise sources negligible. Low impedance feedback resistors load the output of the amplifier. The equations for total noise are shown for both configurations.

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(A) Noise in Noninverting Gain Configuration



Noise at the output is given as E_O, where

$$(1)\quad E_O = \left(1 + \frac{R_2}{R_1}\right) \cdot \sqrt{(e_S)^2 + (e_N)^2 + \left(e_{R_1 \| R_2}\right)^2 + (i_N \cdot R_S)^2 + \left(i_N \cdot \left[\frac{R_1 \cdot R_2}{R_1 + R_2}\right]\right)^2} \quad [\,V_{RMS}\,]$$

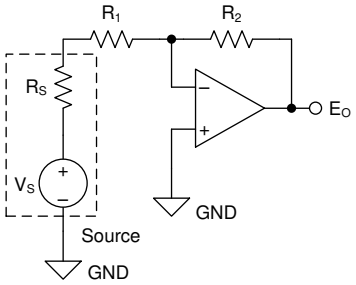
$$(2)\quad e_S = \sqrt{4 \cdot k_B \cdot T(K) \cdot R_S} \quad \left[\frac{V}{\sqrt{Hz}}\right] \quad \text{Thermal noise of } R_S$$

$$(3)\quad e_{R_1 \| R_2} = \sqrt{4 \cdot k_B \cdot T(K) \cdot \left[\frac{R_1 \cdot R_2}{R_1 + R_2}\right]} \quad \left[\frac{V}{\sqrt{Hz}}\right] \quad \text{Thermal noise of } R_1 \text{ || } R_2$$

$$(4)\quad k_B = 1.38065 \cdot 10^{-23} \quad \left[\frac{J}{K}\right] \quad \text{Boltzmann Constant}$$

$$(5)\quad T(K) = 237.15 + T(°C) \quad [\,K\,] \quad \text{Temperature in kelvins}$$

(B) Noise in Inverting Gain Configuration



Noise at the output is given as E_O, where

$$(6)\quad E_O = \left(1 + \frac{R_2}{R_S + R_1}\right) \cdot \sqrt{(e_N)^2 + \left(e_{R_1 + R_S \| R_2}\right)^2 + \left(i_N \cdot \left[\frac{(R_S + R_1) \cdot R_2}{R_S + R_1 + R_2}\right]\right)^2} \quad [\,V_{RMS}\,]$$

$$(7)\quad e_{R_1 + R_S \| R_2} = \sqrt{4 \cdot k_B \cdot T(K) \cdot \left[\frac{(R_S + R_1) \cdot R_2}{R_S + R_1 + R_2}\right]} \quad \left[\frac{V}{\sqrt{Hz}}\right] \quad \text{Thermal noise of } (R_1 + R_S) \text{ || } R_2$$

$$(8)\quad k_B = 1.38065 \cdot 10^{-23} \quad \left[\frac{J}{K}\right] \quad \text{Boltzmann Constant}$$

$$(9)\quad T(K) = 237.15 + T(°C) \quad [\,K\,] \quad \text{Temperature in kelvins}$$

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Where e_N is the voltage noise of the amplifier. For the OPAx210 op amp, e_N = 2.2 nV/√Hz at 1 kHz.
Where i_N is the current noise of the amplifier. For the OPAx210 op amp, i_N = 400 fA/√Hz at 1 kHz.
NOTE: For additional resources on noise calculations visit the *TI Precision Labs Series*.

図 8-1. Noise Calculation in Gain Configurations

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8.2 Typical Application

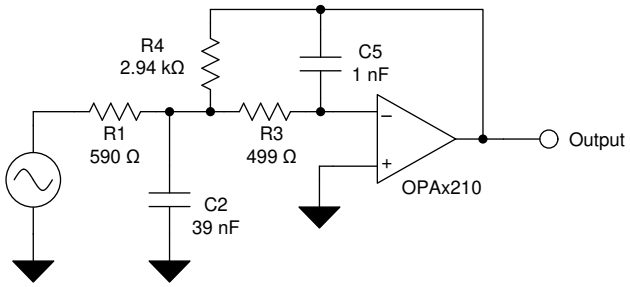


図 8-2. Low-Pass Filter

8.2.1 Design Requirements

Low-pass filters are commonly used in signal processing applications to reduce noise and prevent aliasing. The OPAx210 are designed to construct high-speed, high-precision active filters. 図 8-2 shows a second-order, low-pass filter commonly encountered in signal-processing applications.

Use the following parameters for this design example:

- Gain = 5 V/V (inverting gain)
- Low-pass cutoff frequency = 25 kHz
- Second-order Chebyshev filter response with 3-dB gain peaking in the pass band

8.2.2 Detailed Design Procedure

The infinite-gain, multiple-feedback circuit for a low-pass network function is shown in 図 8-2. Use 式 1 to calculate the voltage transfer function.

$$\frac{\text{Output}}{\text{Input}}(s) = \frac{-1/R_1R_3C_2C_5}{s^2 + (s/C_2)(1/R_1 + 1/R_3 + 1/R_4) + 1/R_3R_4C_2C_5} \quad (1)$$

This circuit produces a signal inversion. For this circuit, the gain at dc and the low-pass cutoff frequency are calculated by 式 2:

$$\text{Gain} = \frac{R_4}{R_1}$$
$$f_c = \frac{1}{2\pi}\sqrt{(1/R_3R_4C_2C_5)} \quad (2)$$

8.2.3 Application Curve

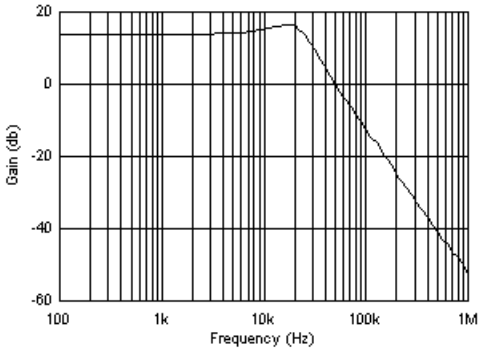


図 8-3. OPAx210 Second-Order, 25-kHz, Chebyshev, Low-Pass Filter

8.3 System Example

8.3.1 Time Gain Control System for Ultrasound Applications

During an ultrasound send-receive cycle, the magnitude of reflected signal depends on the depth of penetration. The ultrasound signal incident on the receiver decreases in amplitude as a function of the time elapsed since transmission. The time gain control (TGC) system helps achieve the best possible signal-to-noise ratio (SNR), even with the decreasing signal amplitude. When the image is displayed, similar materials have similar brightness, regardless of depth. *Linear-in-dB* gain, which means the decibel gain is a linear function of the control voltage (V_{CNTL}), is used to generate this image.

There are multiple approaches for a TGC control circuit that are based on the type of DAC. 図 8-4 shows a high-level block diagram for the topology using a current-output multiplying DAC (MDAC) to generate the drive for V_{CNTL}. The op amp used for current-to-voltage (I-to-V) conversion must have low-voltage noise, as well as low-current noise density. The current density helps reduce the overall noise performance because of the DAC output configuration. The DAC output can go up to ±10 V; therefore, the op amp must have bipolar operation. The OPAx210 is used here because of the low-voltage noise density of 2.2 nV/√Hz, low-current noise density of 500 fA/√Hz, rail-to-rail output, and the ability to accept a wide supply range of ±2.25 V to ±18 V and provide rail-to-rail output. The low offset voltage and offset drift of the OPAx210 facilitate excellent dc accuracy for the circuit.

The OPAx210 is used to filter and buffer the 10-V reference voltage generated by the REF5010. The REF5010 serves as the reference voltage for the DAC8802, which generates a current output on I_{OUT} corresponding to the digital input code. The I_{OUT} pin of the DAC8802 is connected to the virtual ground (negative terminal) of the OPAx210; the feedback resistor (R_{FB} is internal to the DAC8802) is connected to the output of the OPAx210, and results in a current-to-voltage conversion. The output of the OPAx210 has a range of –10 V to 0 V, which is fed to the THS4130 configured as a Sallen-Key filter. Finally, the 10-V range is attenuated down to a 1.5-V range, with a common-mode voltage of 0.75 V using a resistive attenuator. See the *2.3-nV/√Hz, Differential, Time Gain Control DAC Reference Design for Ultrasound* for an in-depth analysis of 図 8-4.

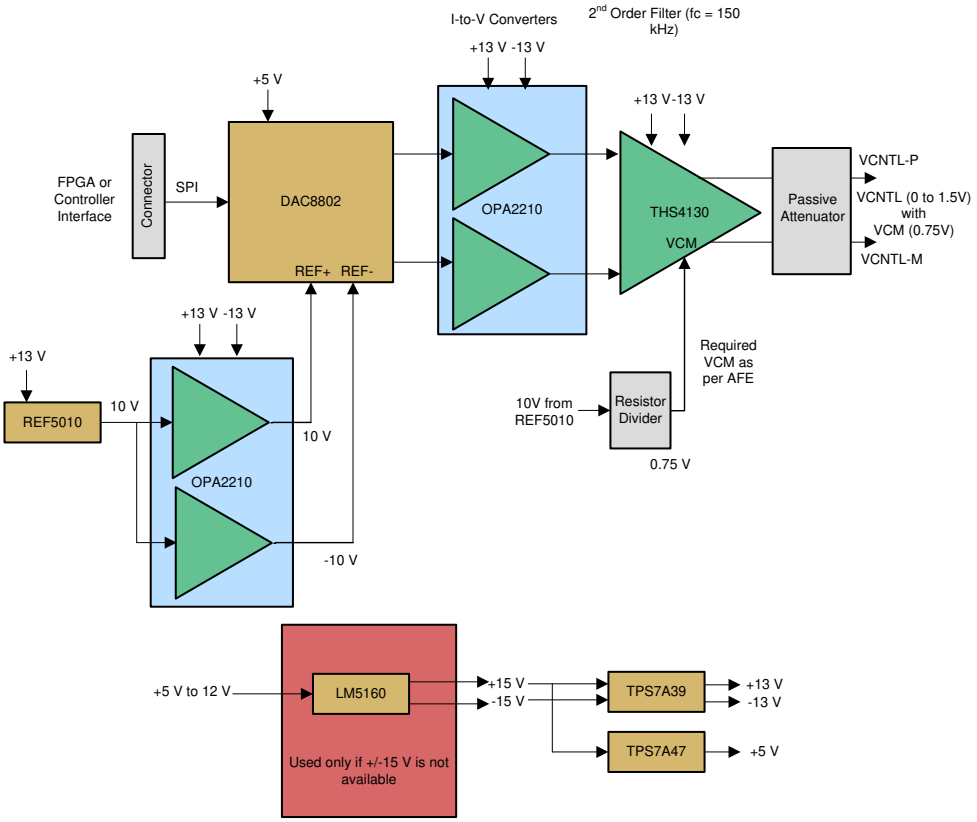


図 8-4. Block Diagram for Time Gain Control System for Ultrasound

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9 Power Supply Recommendations

The OPAx210 are specified for operation from 4.5 V to 36 V (±2.25 V to ±18 V); many specifications apply from –40°C to +125°C. Parameters that can exhibit significant variance with regard to operating voltage or temperature are presented in *セクション 6.7*.

10 Layout

10.1 Layout Guidelines

For best operational performance of the device, use good printed circuit board (PCB) layout practices, including the following guidelines:

- Noise from the amplifier can propagate into other analog circuits through the power pins of the amplifiers. Use bypass capacitors to reduce the coupled noise by providing low-impedance power sources local to the analog circuitry.
- Connect low-ESR, 0.1-µF ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from V+ to ground is applicable for single-supply applications.
- Separate grounding for analog and digital portions of circuitry is one of the simplest and most-effective methods of noise suppression. One or more layers on multilayer PCBs are usually devoted to ground planes. A ground plane helps distribute heat and reduces EMI noise pickup. Make sure to physically separate digital and analog grounds paying attention to the flow of the ground current.
- To reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If these traces cannot be kept separate, crossing the sensitive trace perpendicular is much better than running in parallel with the noisy trace.
- Place the external components as close to the device as possible.
- Keep the length of input traces as short as possible. Always remember that the input traces are the most sensitive part of the circuit.
- Consider a driven, low-impedance guard ring around the critical traces. A guard ring can significantly reduce leakage currents from nearby traces that are at different potentials.
- For best performance, clean the PCB following board assembly.
- Any precision integrated circuit may experience performance shifts due to moisture ingress into the plastic package. Following any aqueous PCB cleaning process, bake the PCB to remove moisture introduced into the device packaging during the cleaning process. A low-temperature, post-cleaning bake at 85°C for 30 minutes is sufficient for most circumstances.

10.2 Layout Example

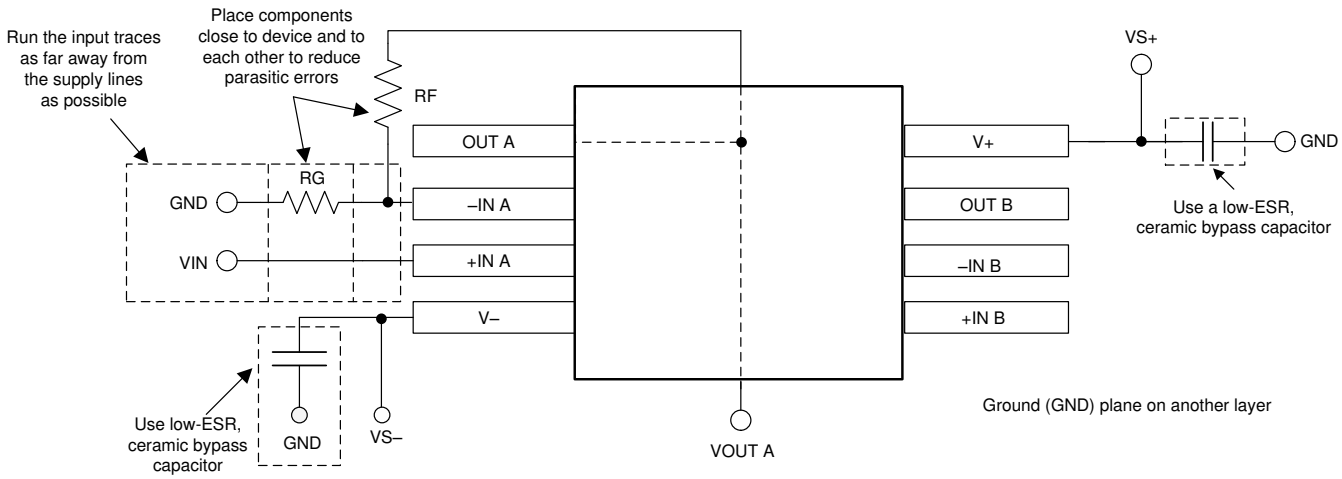


図 10-1. OPA2210 Layout Example

11 Device and Documentation Support

11.1 Device Support

11.1.1 Development Support

11.1.1.1 TINA-TI™ Simulation Software (Free Download)

TINA™ is a simple, powerful, and easy-to-use circuit simulation program based on a SPICE engine. TINA-TI™ simulation software is a free, fully-functional version of the TINA software, preloaded with a library of macro models in addition to a range of both passive and active models. TINA-TI simulation software provides all the conventional dc, transient, and frequency domain analysis of SPICE, as well as additional design capabilities.

Available as a free download from the Analog eLab Design Center, TINA-TI simulation software offers extensive post-processing capability that allows users to format results in a variety of ways. Virtual instruments offer the ability to select input waveforms and probe circuit nodes, voltages, and waveforms, creating a dynamic quick-start tool.

Note

These files require that either the TINA software or TINA-TI software be installed. Download the free TINA-TI software from the TINA-TI software folder.

11.1.1.2 DIP Adapter EVM

The DIP Adapter EVM tool provides an easy, low-cost way to prototype small, surface-mount integrated circuits (ICs). The EVM includes footprint options for the following TI packages:

- D or U (SOIC-8)
- PW (TSSOP-8)
- DGK (VSSOP-8)
- DBV (SOT23-6, SOT23-5 and SOT23-3)
- DCK (SC70-6 and SC70-5)
- DRL (SOT563-6)

The DIP Adapter EVM may also be used with terminal strips or may be wired directly to existing circuits.

11.1.1.3 Universal Operational Amplifier EVM

The Universal Op Amp evalutaion module (EVM) is a series of general-purpose, blank circuit boards that simplify prototyping circuits for a variety of IC package types. The EVM board design allows many different circuits to be constructed easily and quickly. Five models are offered, with each model intended for a specific package type. The PDIP, SOIC, VSSOP, TSSOP, and SOT-23 packages are all supported.

Note

These boards are unpopulated, so users must provide their own ICs. TI recommends requesting several op amp device samples when ordering the Universal Op Amp EVM.

11.1.1.4 TI Precision Designs

TI Precision Designs are analog solutions created by TI's precision analog applications experts. These designs offer the theory of operation, component selection, simulation, complete PCB schematic and layout, bill of materials, and measured performance of many useful circuits.

11.1.1.5 WEBENCH® Filter Designer

The WEBENCH® Filter Designer is a simple, powerful, and easy-to-use active filter design program. The WEBENCH® Filter Designer lets you create optimized filter designs using a selection of TI operational amplifiers and passive components from TI's vendor partners.

Available as a web-based tool from the WEBENCH® Design Center, the WEBENCH® Filter Designer allows you to design, optimize, and simulate complete multistage active filter solutions within minutes.

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11.2 Documentation Support

11.2.1 Related Documentation

The following documents are relevant to using the OPAx210 and recommended for reference. All are available for download at www.ti.com (unless otherwise noted):

- Texas Instruments, *OPA827 Low-Noise, High-Precision, JFET-Input Operational Amplifier* data sheet
- Texas Instruments, *OPA2x11 1.1-nv/√Hz Noise, Low-Power, Precision Operational Amplifier* data sheet
- Texas Instruments, *OPA210, OPA2210, OPA4210 EMI Immunity Performance* technical brief
- Texas Instruments, *OPAx209 2.2-nV/√Hz, Low-Power, 36-V Operational Amplifier* data sheet
- Texas Instruments, *Microcontroller PWM to 12-Bit Analog Out* design guide
- Texas Instruments, *Capacitive Load Drive Solution Using an Isolation Resistor* design guide
- Texas Instruments, *Noise Measurement Post Amp* design guide

11.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.4 サポート・リソース

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11.6 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.7 Glossary

TI Glossary — This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
OPA210IDBVR	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	26T2
OPA210IDBVR.B	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	26T2
OPA210IDBVT	Active	Production	SOT-23 (DBV) | 5	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	26T2
OPA210IDBVT.B	Active	Production	SOT-23 (DBV) | 5	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	26T2
OPA210IDBVTG4	Active	Production	SOT-23 (DBV) | 5	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	26T2
OPA210IDBVTG4.B	Active	Production	SOT-23 (DBV) | 5	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	26T2
OPA210IDGKR	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	2D5J
OPA210IDGKR.B	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	2D5J
OPA210IDGKRG4	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	2D5J
OPA210IDGKRG4.B	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	2D5J
OPA210IDGKT	Active	Production	VSSOP (DGK) | 8	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	2D5J
OPA210IDGKT.B	Active	Production	VSSOP (DGK) | 8	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	2D5J
OPA210IDR	Active	Production	SOIC (D) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA210
OPA210IDR.B	Active	Production	SOIC (D) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA210
OPA210IDT	Active	Production	SOIC (D) | 8	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA210
OPA210IDT.B	Active	Production	SOIC (D) | 8	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA210
OPA2210ID	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OP2210
OPA2210ID.B	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OP2210
OPA2210IDG4	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OP2210
OPA2210IDG4.B	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OP2210
OPA2210IDGKR	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAU | SN | NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	1OHQ
OPA2210IDGKR.B	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	1OHQ
OPA2210IDGKT	Active	Production	VSSOP (DGK) | 8	250 | SMALL T&R	Yes	NIPDAU | SN | NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	1OHQ
OPA2210IDGKT.B	Active	Production	VSSOP (DGK) | 8	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	1OHQ
OPA2210IDR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OP2210
OPA2210IDR.B	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OP2210
OPA2210IDRGR	Active	Production	SON (DRG) | 8	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	O2210
OPA2210IDRGR.B	Active	Production	SON (DRG) | 8	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	O2210

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
OPA2210IDRGT	Active	Production	SON (DRG) | 8	250 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	O2210
OPA2210IDRGT.B	Active	Production	SON (DRG) | 8	250 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	O2210

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

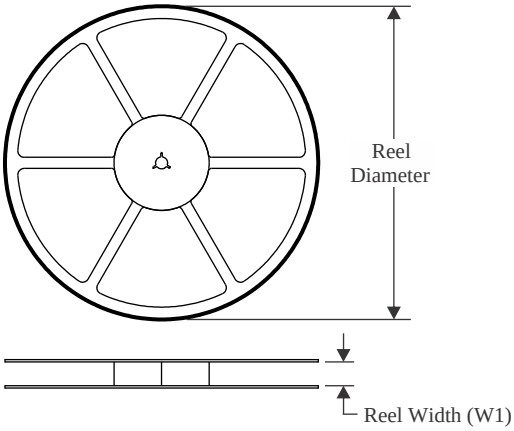
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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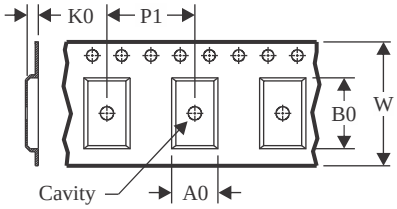
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TAPE AND REEL INFORMATION

REEL DIMENSIONS

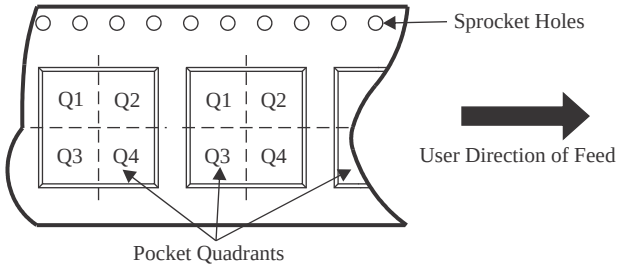


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

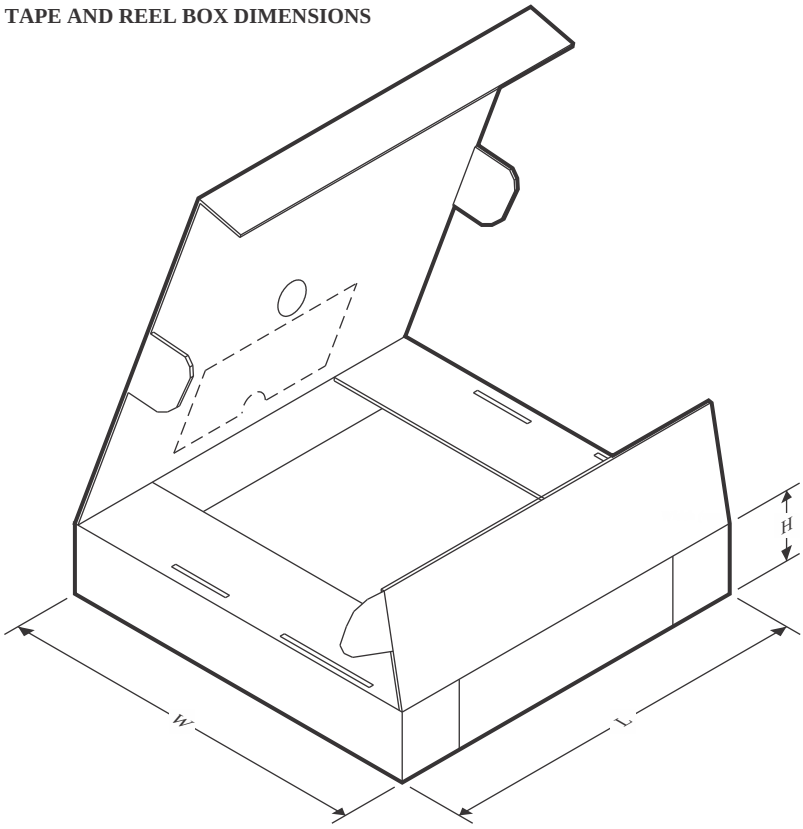
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA210IDBVR	SOT-23	DBV	5	3000	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
OPA210IDBVT	SOT-23	DBV	5	250	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
OPA210IDBVTG4	SOT-23	DBV	5	250	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
OPA210IDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA210IDGKRG4	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA210IDGKT	VSSOP	DGK	8	250	180.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA210IDR	SOIC	D	8	3000	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA2210IDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.25	3.35	1.25	8.0	12.0	Q1
OPA2210IDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA2210IDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA2210IDGKT	VSSOP	DGK	8	250	330.0	12.4	5.25	3.35	1.25	8.0	12.0	Q1
OPA2210IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA2210IDRGR	SON	DRG	8	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
OPA2210IDRGT	SON	DRG	8	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

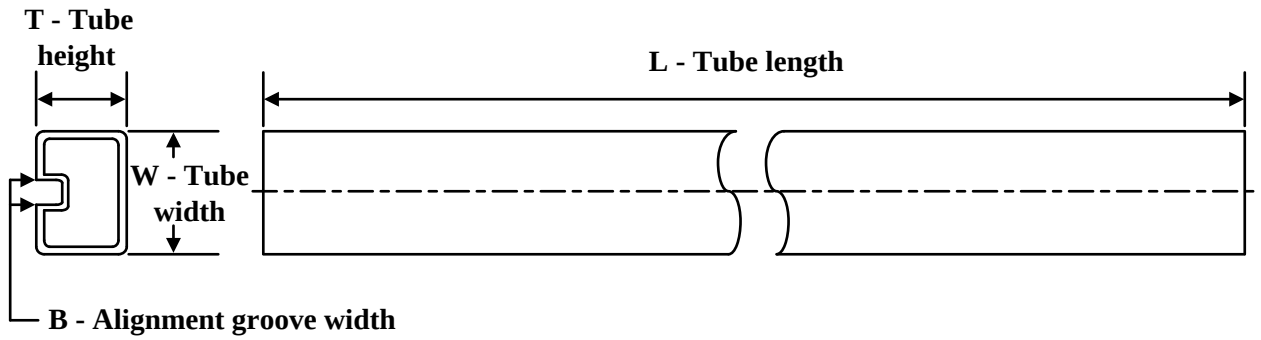
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

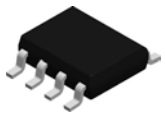
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA210IDBVR	SOT-23	DBV	5	3000	213.0	191.0	35.0
OPA210IDBVT	SOT-23	DBV	5	250	213.0	191.0	35.0
OPA210IDBVTG4	SOT-23	DBV	5	250	213.0	191.0	35.0
OPA210IDGKR	VSSOP	DGK	8	2500	353.0	353.0	32.0
OPA210IDGKRG4	VSSOP	DGK	8	2500	353.0	353.0	32.0
OPA210IDGKT	VSSOP	DGK	8	250	213.0	191.0	35.0
OPA210IDR	SOIC	D	8	3000	353.0	353.0	32.0
OPA2210IDGKR	VSSOP	DGK	8	2500	366.0	364.0	50.0
OPA2210IDGKR	VSSOP	DGK	8	2500	353.0	353.0	32.0
OPA2210IDGKR	VSSOP	DGK	8	2500	366.0	364.0	50.0
OPA2210IDGKT	VSSOP	DGK	8	250	366.0	364.0	50.0
OPA2210IDR	SOIC	D	8	2500	353.0	353.0	32.0
OPA2210IDRGR	SON	DRG	8	3000	360.0	360.0	36.0
OPA2210IDRGT	SON	DRG	8	250	210.0	185.0	35.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
OPA2210ID	D	SOIC	8	75	506.6	8	3940	4.32
OPA2210ID.B	D	SOIC	8	75	506.6	8	3940	4.32
OPA2210IDG4	D	SOIC	8	75	506.6	8	3940	4.32
OPA2210IDG4.B	D	SOIC	8	75	506.6	8	3940	4.32

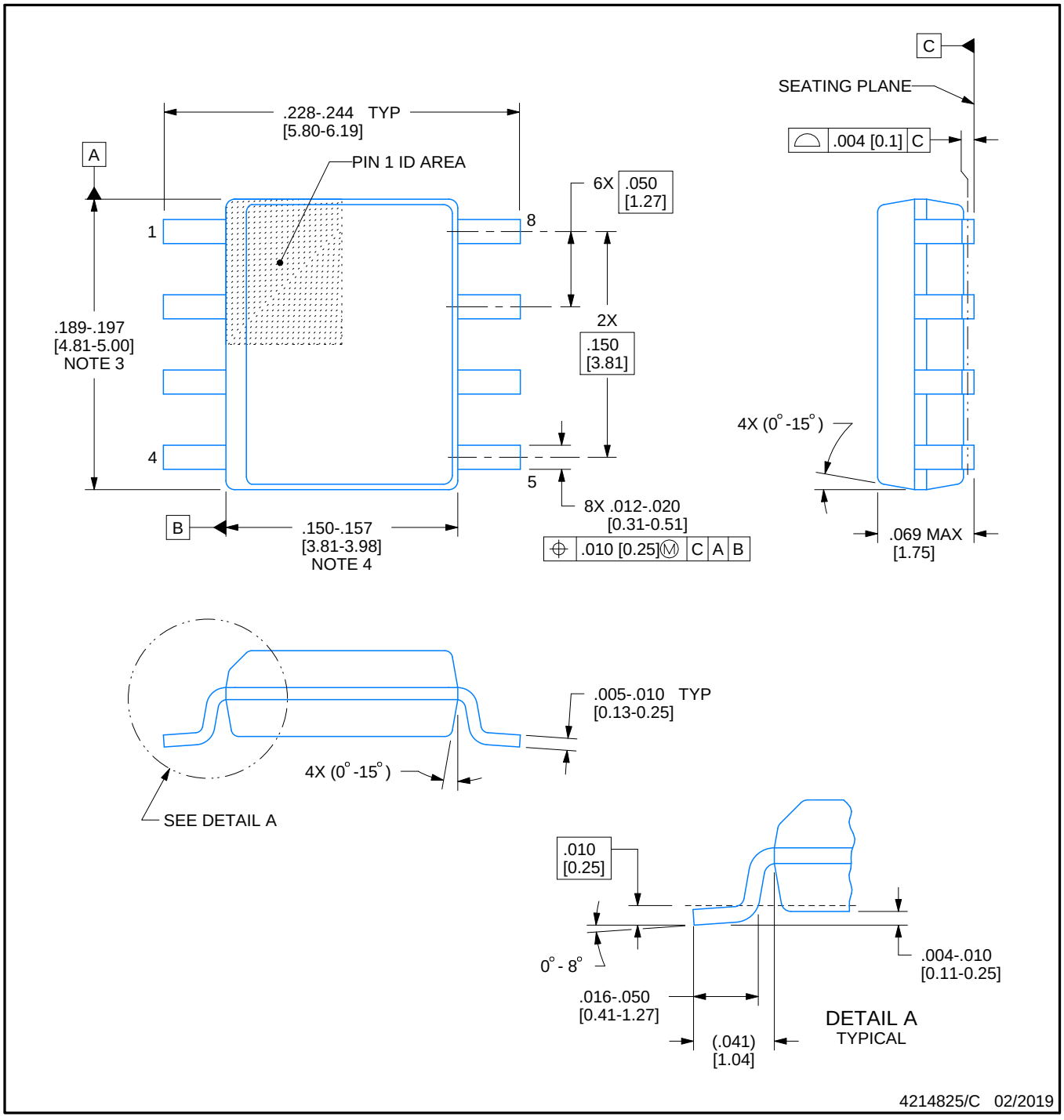


PACKAGE OUTLINE

D0008A

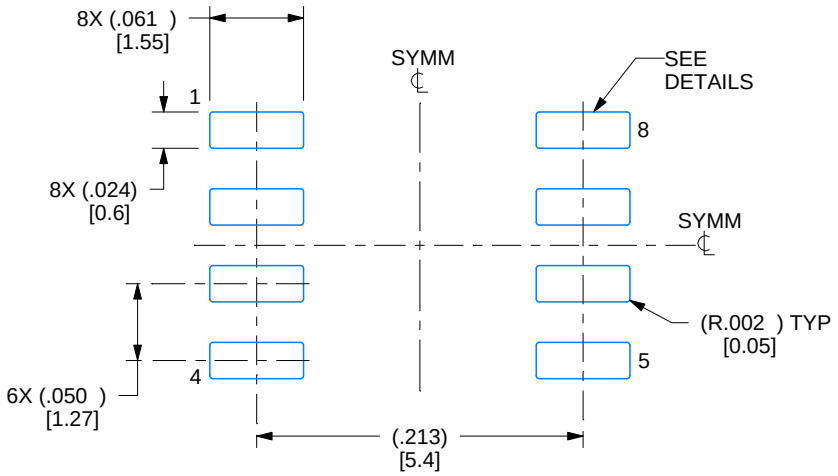
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

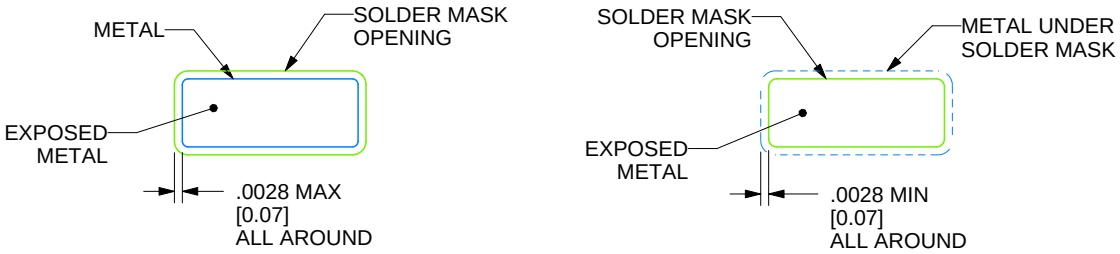


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

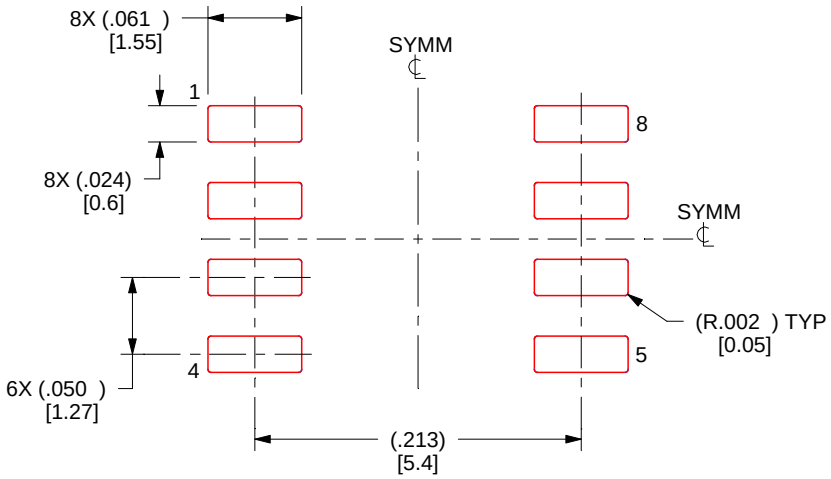
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

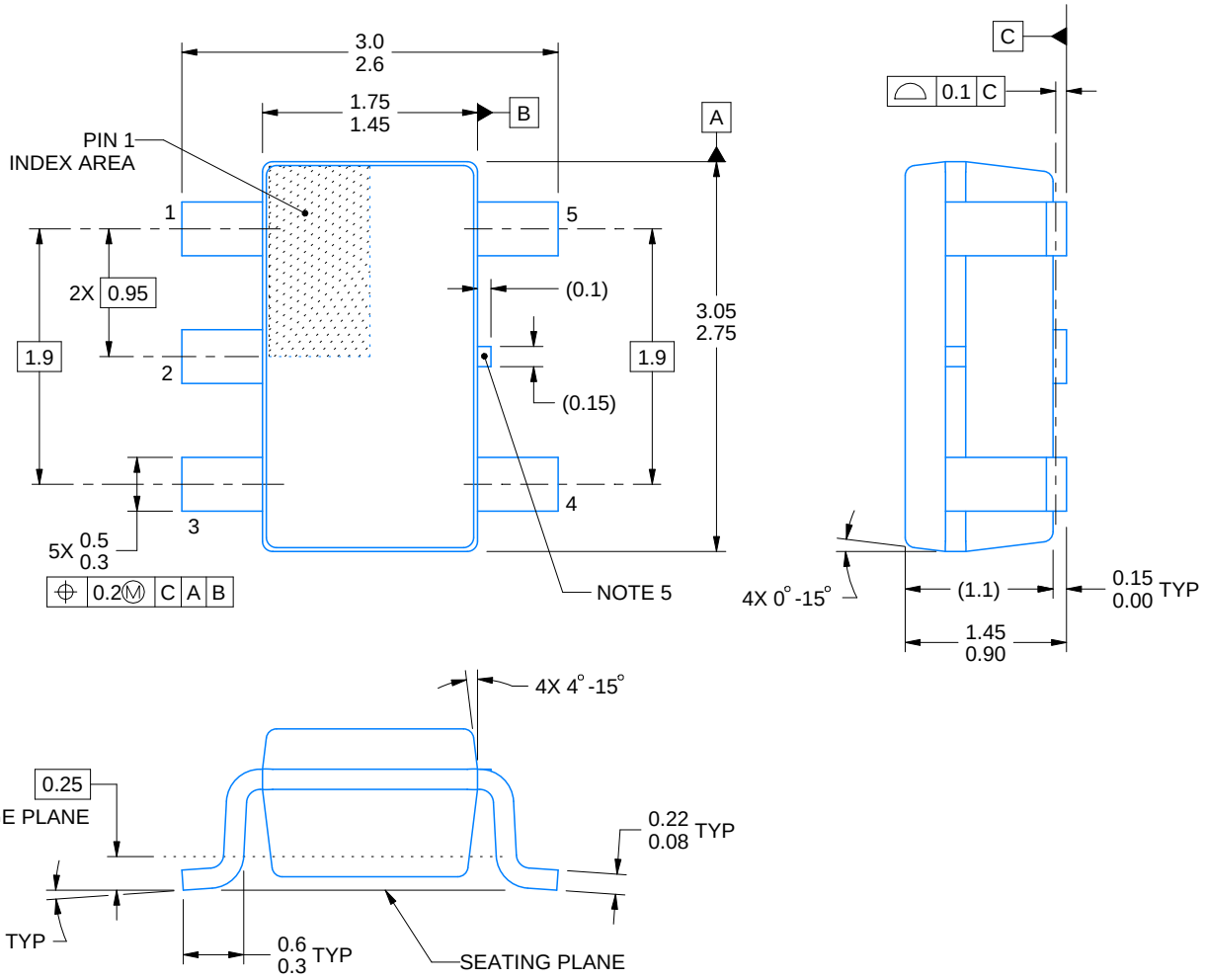
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

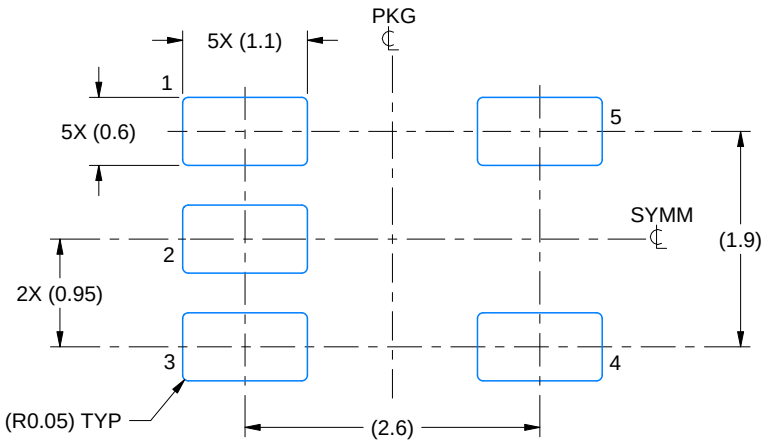
SMALL OUTLINE TRANSISTOR



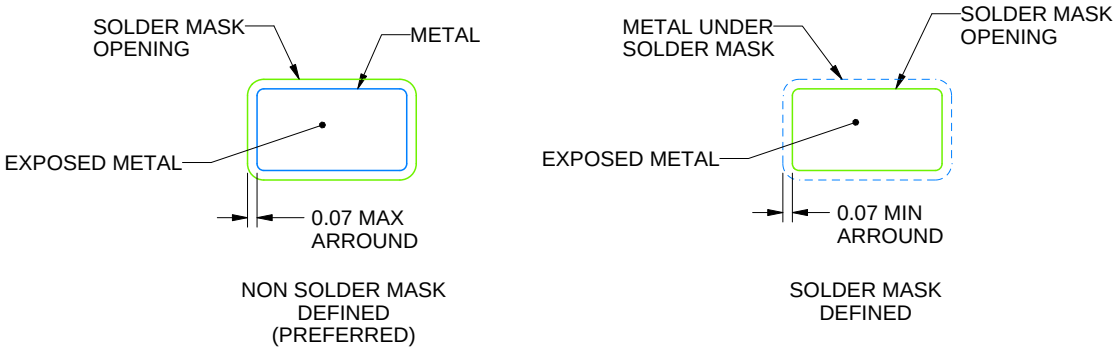
4214839/K 08/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

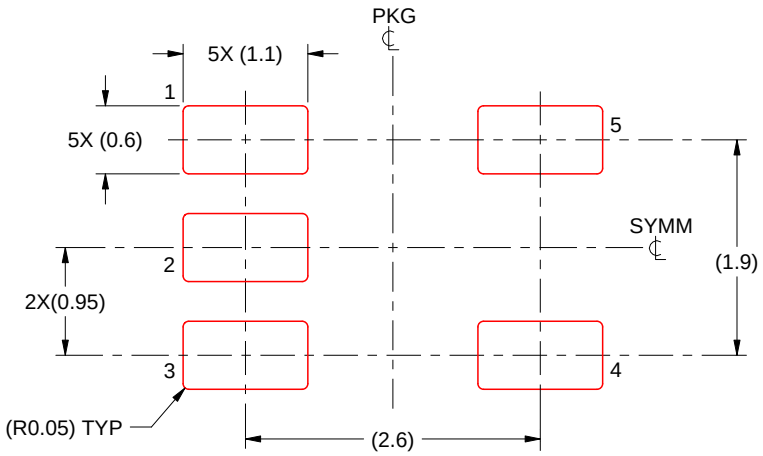


SOLDER MASK DETAILS

4214839/K 08/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/K 08/2024

NOTES: (continued)

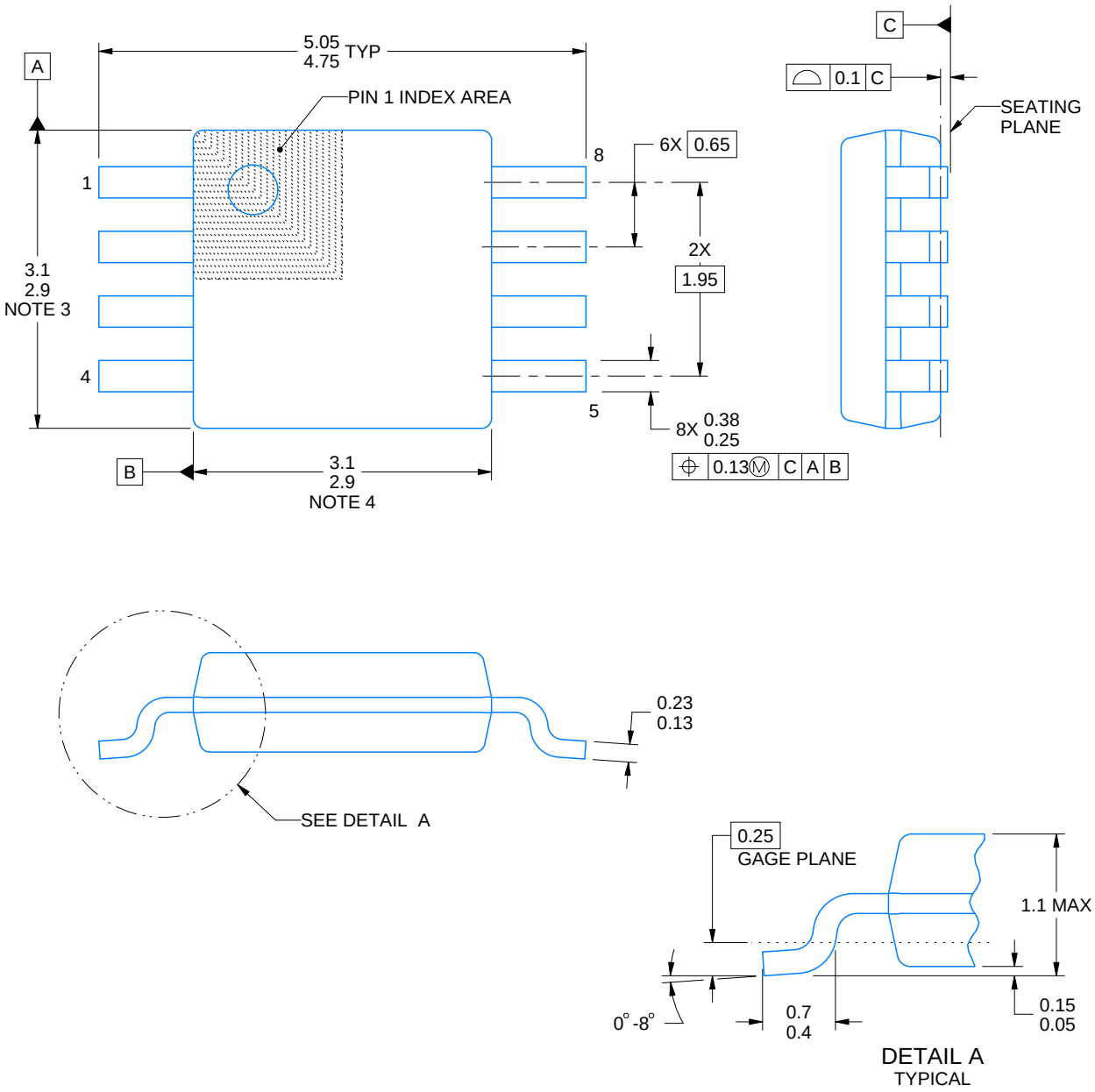
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DGK0008A

VSSOP - 1.1 mm max height

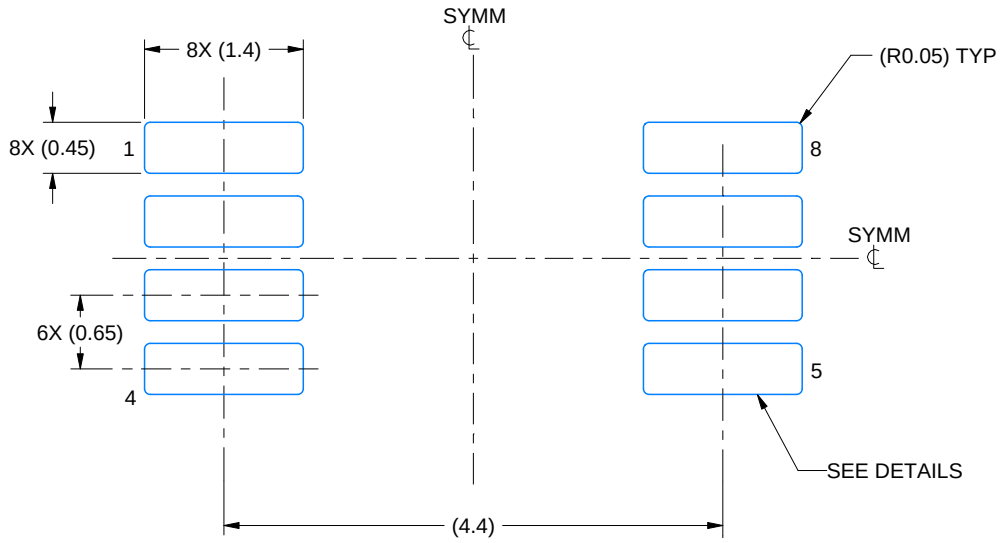
SMALL OUTLINE PACKAGE



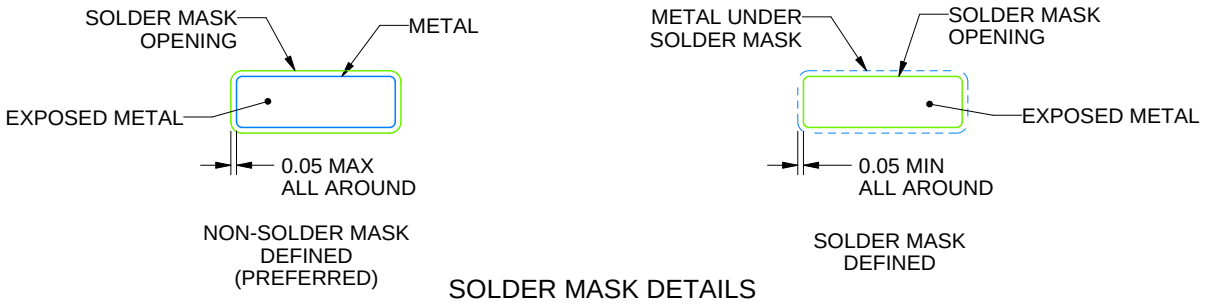
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X

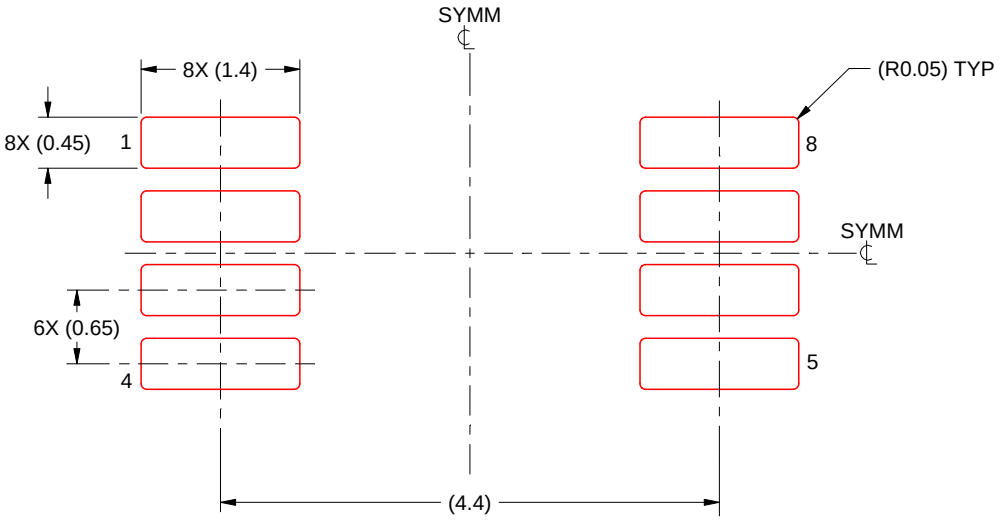


SOLDER MASK DETAILS

4214862/A 04/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
SCALE: 15X

4214862/A 04/2023

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

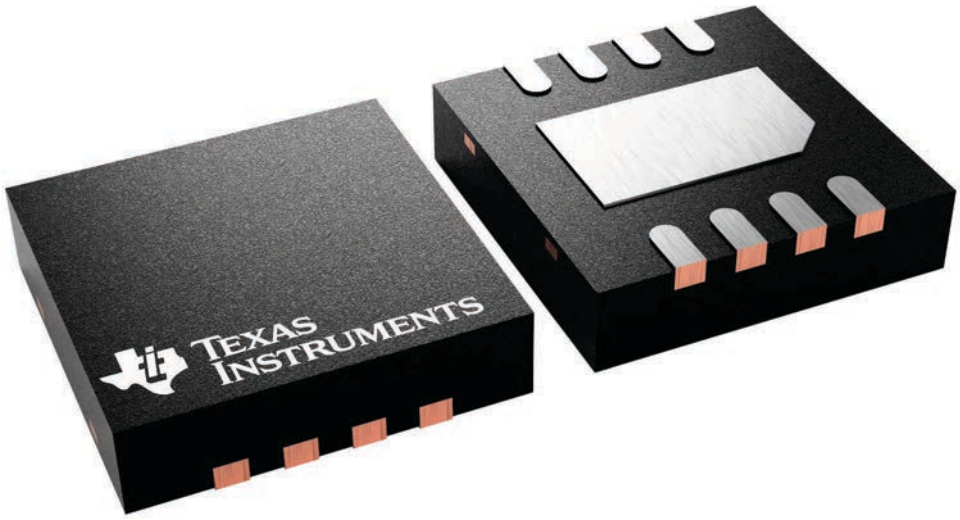
DRG 8

WSON - 0.8 mm max height

3 x 3, 0.5 mm pitch

PLASTIC SMALL OUTLINE - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



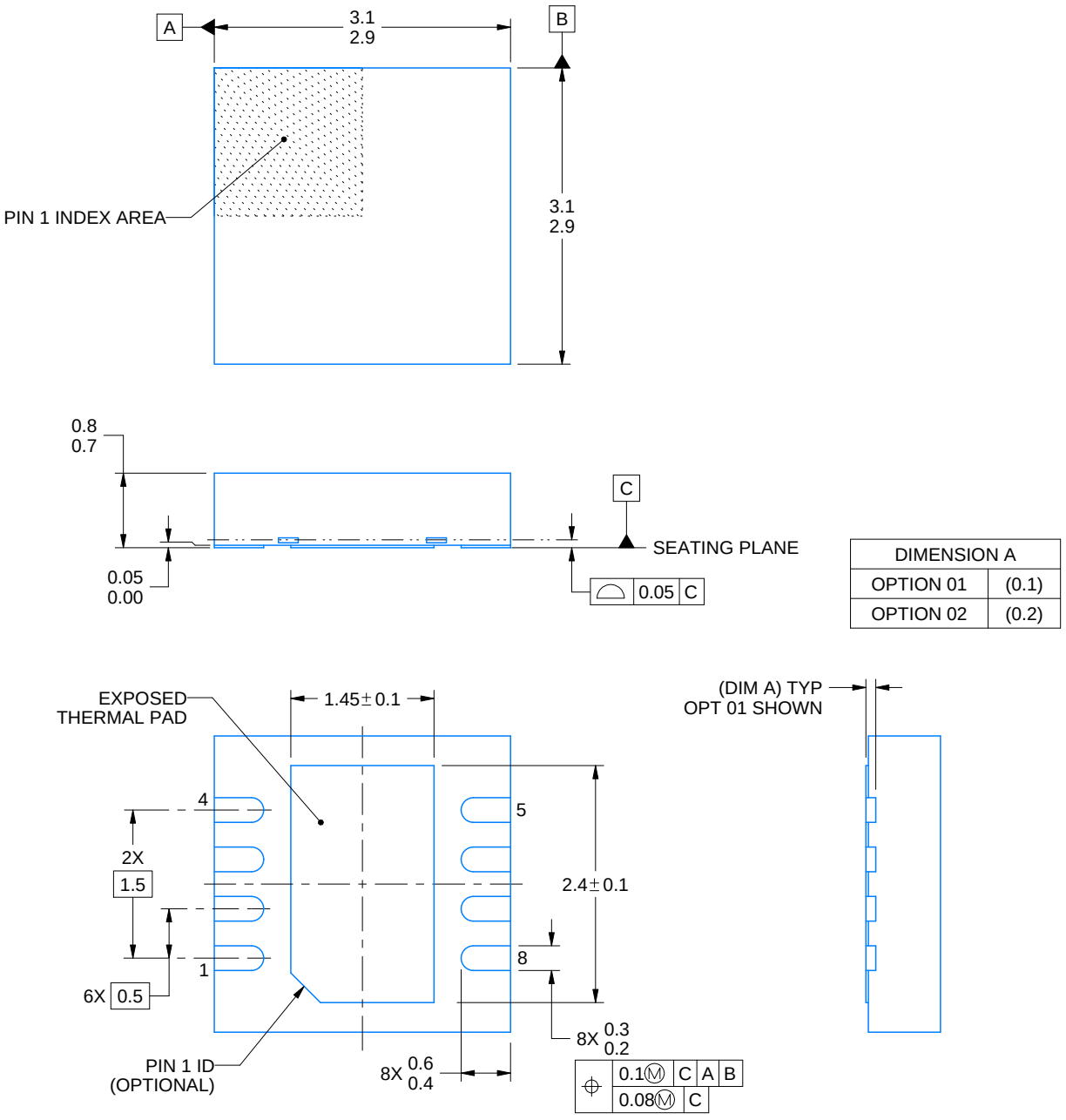
4225794/A

DRG0008B

PACKAGE OUTLINE

WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

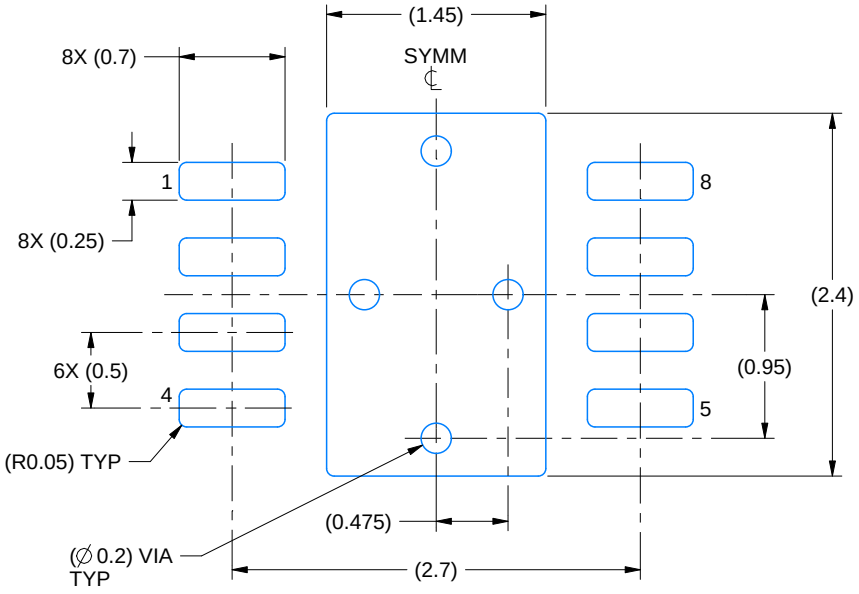


DIMENSION A	
OPTION 01	(0.1)
OPTION 02	(0.2)

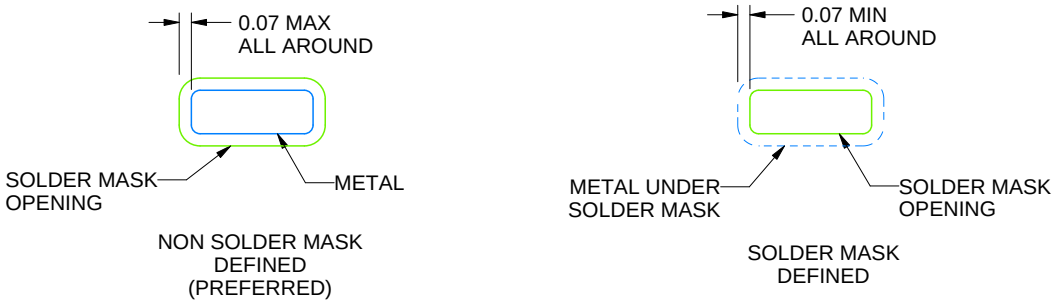
4218886/A 01/2020

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:20X

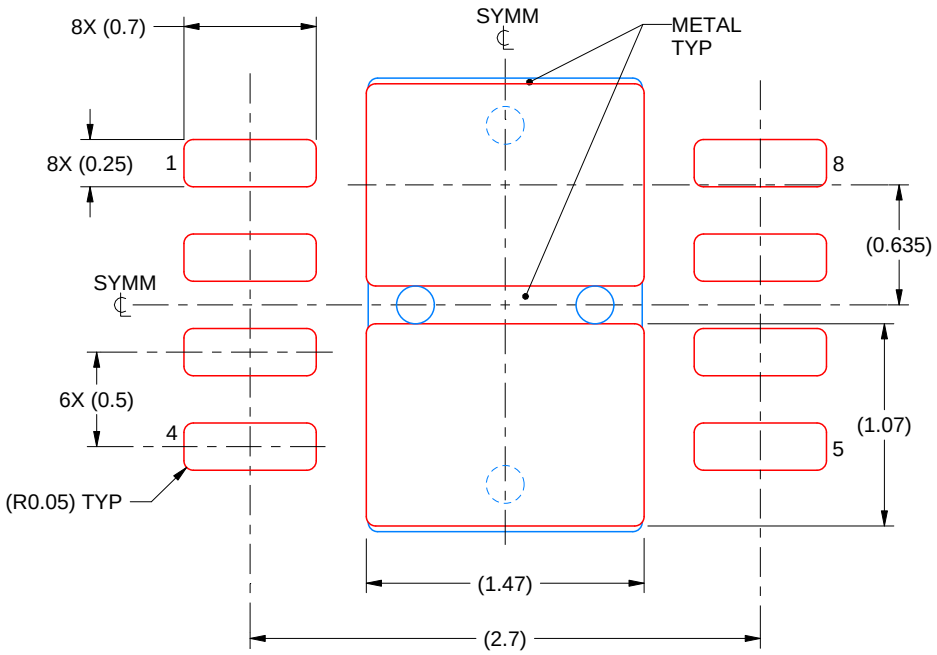


SOLDER MASK DETAILS

4218886/A 01/2020

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
82% PRINTED SOLDER COVERAGE BY AREA
SCALE:25X

4218886/A 01/2020

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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最終更新日：2025 年 10 月