OPA2333P 1.8V、*micro*Power、ゼロドリフト・オペアンプ

1 特長

- 低オフセット電圧：10µV (最大値)
- ゼロ·ドリフト：0.05µV/℃（最大値）
- スタートアップ時間の規定: 500µs (最大値)
- 0.01Hz～10Hzのノイズ：1.1μV_{PP}
- 静止電流：17µA
- 単一電源動作
- 電源電圧：1.8V～5.5V
- レール・ツー・レール入出力
- *micro*Sizeパッケージ: 2mm×2mm WSON

2 アプリケーション

- スマートフォン
- ウェアラブル
- フィットネスおよび保健用製品
- 電子計測器
- 医療用計測機器
- バッテリ駆動計測器
- ハンドヘルド・テスト機器
- サーキット・ブレーカ

3 概要

OPA2333P CMOSオペアンプは、独自の自動較正技法を使用して、非常に低いオフセット電圧(最大値10µV)と、時間経過や温度の変化に対してほぼゼロのドリフト係数を両立しています。この小型、高精度、低静止電流のアンプは、レールを100mV上回る同相範囲を持つ高インピーダンス入力と、レールの50mV以内でスイングするレール・ツー・レール出力を提供します。最低+1.8V (±0.9V)から、最高+5.5V (±2.75V)までの単一またはデュアル電源で使用できます。このデバイスは、低電圧の単一電源動作用に最適化されています。

また、OPA2333Pは最大スタートアップ時間が規定されています。スタートアップ時間の規定により、アンプの電源をオンにした500µs後には高精度のパフォーマンスが保証されるため、動的な電源での動作でも高い信頼性で使用できます。

OPA2333Pは、従来の相補入力段に起因するクロスオーバーがなく、CMRRが優れています。この設計により、アナログ/デジタル·コンバータ(ADC)の微分直線性の低下がなく、優れた性能が得られます。

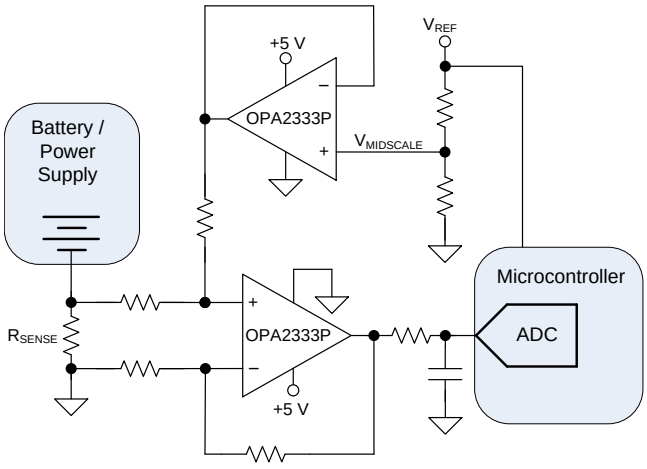
OPA2333Pは、2mm×2mmの8ピンWSONパッケージで供給され、-40℃～125℃で動作が規定されています。

製品情報(1)

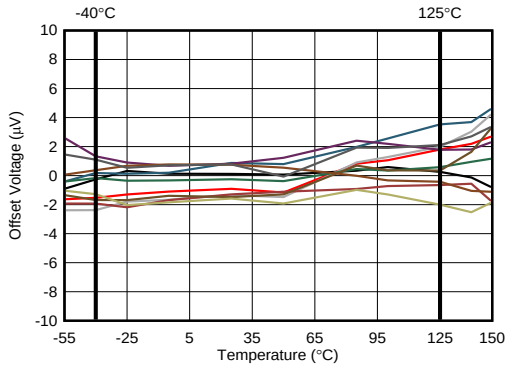
型番	パッケージ	本体サイズ(公称)
OPA2333P	WSON (8)	2.00mm×2.00mm

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。

双方向、ローサイドの電流シャント・アンプ



オフセット電圧と温度との関係



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目次

1 特長 ... 1
2 アプリケーション ... 1
3 概要 ... 1
4 改訂履歴 ... 2
5 **Pin Configuration and Functions** ... 3
6 **Specifications** ... 4
- 6.1 Absolute Maximum Ratings ... 4
- 6.2 ESD Ratings ... 4
- 6.3 Recommended Operating Conditions ... 4
- 6.4 Thermal Information: OPA2333P ... 4
- 6.5 Electrical Characteristics ... 5
- 6.6 Typical Characteristics ... 6

7 **Detailed Description** ... 10
- 7.1 Overview ... 10
- 7.2 Functional Block Diagram ... 10
- 7.3 Feature Description ... 10
- 7.4 Device Functional Modes ... 13

8 **Application and Implementation** ... 14
- 8.1 Application Information ... 14
- 8.2 Typical Application ... 14

9 **Power Supply Recommendations** ... 18
10 **Layout** ... 20
- 10.1 Layout Guidelines ... 20
- 10.2 Layout Example ... 20

11 デバイスおよびドキュメントのサポート ... 21
- 11.1 デバイス・サポート ... 21
- 11.2 ドキュメントのサポート ... 21
- 11.3 ドキュメントの更新通知を受け取る方法 ... 21
- 11.4 コミュニティ・リソース ... 21
- 11.5 商標 ... 21
- 11.6 静電気放電に関する注意事項 ... 21
- 11.7 Glossary ... 21

12 メカニカル、パッケージ、および注文情報 ... 22

4 改訂履歴

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

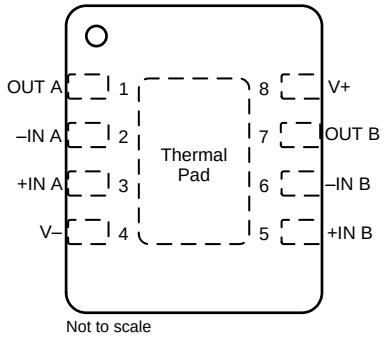
2017年11月発行のものから更新 **Page**

- 表現を変更、タイトルから「CMOS」を 削除 ... 1
- 「*概要*」に新しく段落2を 追加 ... 1
- ページ1の図 変更 ... 1
- Changed "DFN" to "DSG" Package ... 3
- Changed footnote reference for Common-mode and "0.5" V to "0.3" V in footnote 2 ... 4
- Changed "10 mA" to "1 mA" in Abs Max footnotes 2 and 3 ... 4
- Changed "-40" to "-55" in *Abs Max* MIN for T_A ... 4
- Changed "5" to "±5" in PSRR row of *Electrical Characteristics* ... 5
- Deleted "±400" from second row of I_B in *Electrical Characteristics* ... 5
- Changed "100" Hz to "10" Hz in i_N row of *Electrical Characteristics* ... 5
- Deleted second row for AOL in *Electrical Characteristics* ... 5
- Deleted "C_L = 100 pF" from Phase margin and Gain-bandwidth product rows of *Electrical Characteristics* ... 5
- Deleted "RL = 2 kohm" rows ... 5
- Deleted from OUTPUT subsection of *Electrical Characteristics* ... 5
- Deleted "±" from "5" in TYP column of ISC row in *Electrical Characteristics* ... 5
- Changed "Turnon" to "Start-up" in OUTPUT subsection of *Electrical Characteristics* ... 5
- 追加 "Quiescent Current Production Distribution" graph ... 6
- 変更 "DFN" to "WSON"; "SON" to "DFN" in *WSON Package* ... 13
- 削除 "Single-Supply, Very Low Power, ECG Circuit" graphic ... 18
- 削除「*開発サポート*」から「THS4281 超低消費電力、高速、レール・ツー・レール入力および出力の電圧フィードバック型オペアンプ」を ... 21

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5 Pin Configuration and Functions

DSG Package
8-Pin WSON With Exposed Thermal Pad
Top View



Not to scale

Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
+IN A	3	I	Noninverting input, channel A
+IN B	5	I	Noninverting input, channel B
–IN A	2	I	Inverting input, channel A
–IN B	6	I	Inverting input, channel B
OUT A	1	O	Output, channel A
OUT B	7	O	Output, channel B
V+	8	—	Positive (highest) power supply
V–	4	—	Negative (lowest) power supply
Thermal Pad	—	—	Thermal Pad, Connect to V–

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
Supply voltage, V_S = (V+) - (V-)	Single-supply			7	V
	Dual-supply			±3.5	
Signal input pins	Voltage	Common-mode(2)	(V–) – 0.3	(V+) + 0.3	
		Differential(3)		±0.5	
	Current			±10	mA
Output short current(4)			Continuous		
Temperature	Operating, T_A		–55	150	°C
	Junction, T_J			150	
	Storage, T_{stg}		–65	150	

(1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions.* Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Input terminals are diode-clamped to the power-supply rails. Input signals that can swing more than 0.3 V beyond the supply rails must be current-limited to 1 mA or less.
(3) Input terminals are anti-parallel diode-clamped to each other. Input signals that can cause differential voltages of swing more than ±0.5 V must be current-limited to 1 mA or less.
(4) Short-circuit to ground, one amplifier per package.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±4000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_S	Supply voltage, [(V+) – (V–)]	Single supply	1.8		5.5	V
		Dual supply	±0.9		±2.75	
	Specified temperature		–40		125	°C

6.4 Thermal Information: OPA2333P

THERMAL METRIC(1)		OPA2333P DSG (WSON) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	74.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	93.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	41.1	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	4.3	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	41.2	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	15.7	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

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6.5 Electrical Characteristics

At T_A = 25°C, R_L= 10 kΩ connected to V_S / 2, V_{CM} = V_S / 2, and V_{OUT} = V_S / 2 (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
OFFSET VOLTAGE							
V_{OS}	Input offset voltage	V_S = 5 V			±2	±10	µV
dV_{OS}/dT	Input offset voltage drift	V_S = 5 V	T_A = –40°C to +125°C		0.02	±0.05	µV/°C
PSRR	Power-supply rejection ratio	1.8 V ≤ V_S ≤ 5.5 V	T_A = –40°C to +125°C		1	±5	µV/V
	Channel separation, dc				0.1		µV/V
INPUT BIAS CURRENT							
I_B	Input bias current				±70	±200	pA
		T_A = –40°C to +125°C			±150		pA
I_{OS}	Input offset current				±140	±400	pA
NOISE							
E_N	Input voltage noise	f = 0.1 Hz to 10 Hz, peak-to-peak			1.1		μV_{PP}
		f = 0.1 Hz to 10 Hz, RMS			0.2		μV_{RMS}
e_N	Input voltage noise density	f = 10 Hz			55		$nV/\sqrt{Hz}$
		f = 1 kHz			55		$nV/\sqrt{Hz}$
i_N	Input current noise density	f = 10 Hz			100		$fA/\sqrt{Hz}$
INPUT VOLTAGE							
V_{CM}	Common-mode voltage range			(V–) – 0.1		(V+) + 0.1	V
CMRR	Common-mode rejection ratio	(V–) – 0.1 V ≤ V_{CM} ≤ (V+) + 0.1 V, V_S = 5.5 V		106	130		dB
INPUT IMPEDANCE							
Z_{ID}	Differential				10^{13} || 2		Ω || pF
Z_{ICM}	Common-mode				10^{13} || 4		Ω || pF
OPEN-LOOP GAIN							
A_{OL}	Open-loop voltage gain	T_A = –40°C to +125°C	(V–) + 100 mV ≤ V_O ≤ (V+) – 100 mV, R_L = 10 kΩ	106	130		dB
FREQUENCY RESPONSE							
φ_m	Phase margin	V_O = 10 mV_{PP}			65		Degrees
GBW	Gain-bandwidth product	V_O = 10 mV_{PP}			350		kHz
SR	Slew rate	V_O = 4-V step	G = 1		0.16		V/µs
OUTPUT							
	Output voltage swing				30	50	mV
		T_A = –40°C to +125°C				70	mV
I_{SC}	Short-circuit current				±5		mA
C_L	Capactive load drive				See *Typical Characteristics*		
Z_O	Open-loop output impedance	f = 350 kHz, I_O = 0 mA			2		kΩ
	Start-up time	V_S = 5 V			100	500	µs
POWER SUPPLY							
V_S	Specified voltage			1.8		5.5	V
I_Q	Quiescent current (per amplifier)	I_O = 0 A			17	25	µA
			T_A = –40°C to +125°C			28	
TEMPERATURE RANGE							
T_A	Specified range			–40		125	°C
T_A	Operating range			–55		150	°C

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6.6 Typical Characteristics

表 1. List of Typical Characteristics

TITLE	FIGURE
Offset Voltage Production Distribution	図 1
Offset Voltage Drift Production Distribution	図 2
Quiescent Current Production Distribution	図 3
Open-Loop Gain vs Frequency	図 4
Common-Mode Rejection Ratio vs Frequency	図 5
Power-Supply Rejection Ratio vs Frequency	図 6
Output Voltage Swing vs Output Current	図 7
Input Bias Current vs Common-Mode Voltage	図 8
Input Bias Current vs Temperature	図 9
Quiescent Current vs Temperature	図 10
Large-Signal Step Response	図 11
Small-Signal Step Response	図 12
Positive Overvoltage Recovery	図 13
Negative Overvoltage Recovery	図 14
Settling Time vs Closed-Loop Gain	図 15
Small-Signal Overshoot vs Load Capacitance	図 16
0.1-Hz to 10-Hz Noise	図 17
Current and Voltage Noise Spectral Density vs Frequency	図 18

At T_A = 25°C, V_S = 5 V, and C_L = 0 pF, unless otherwise noted.

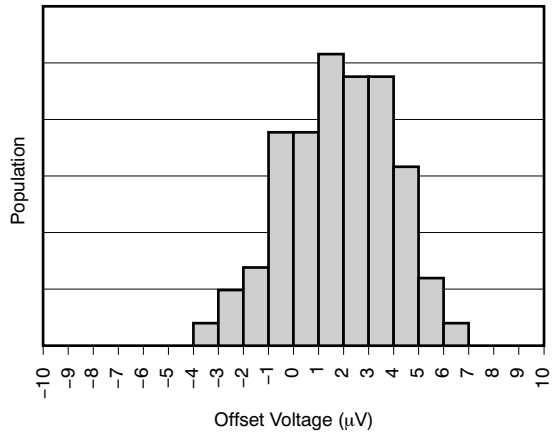


図 1. Offset Voltage Production Distribution

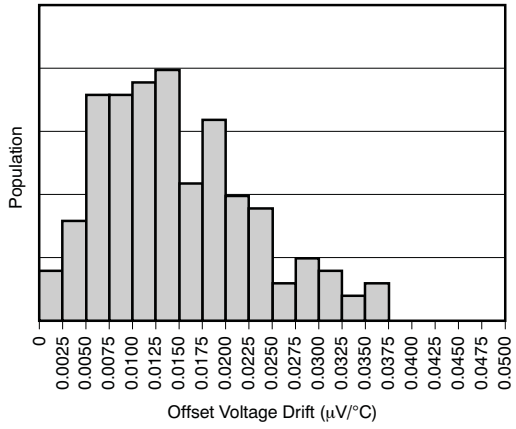


図 2. Offset Voltage Drift Production Distribution

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At T_A = 25°C, V_S = 5 V, and C_L = 0 pF, unless otherwise noted.

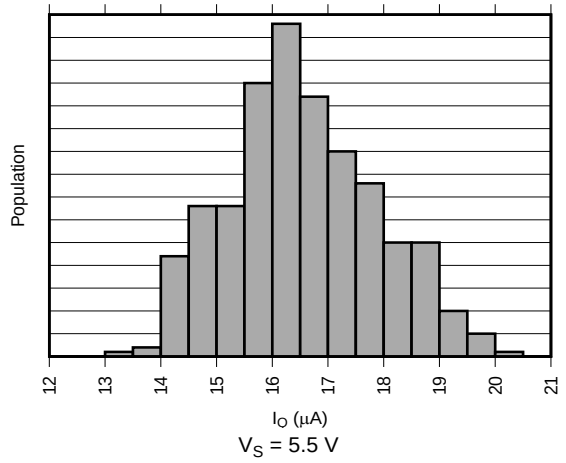


図 3. Quiescent Current Production Distribution

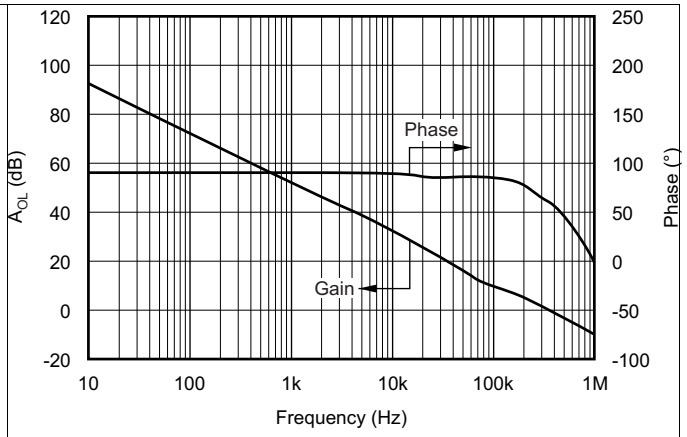


図 4. Open-Loop Gain and Phase vs Frequency

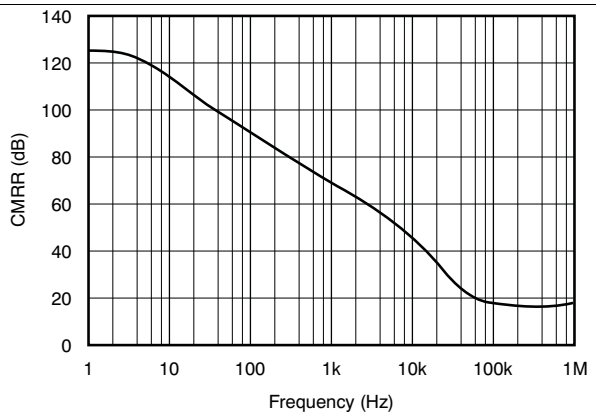


図 5. Common-Mode Rejection Ratio vs Frequency

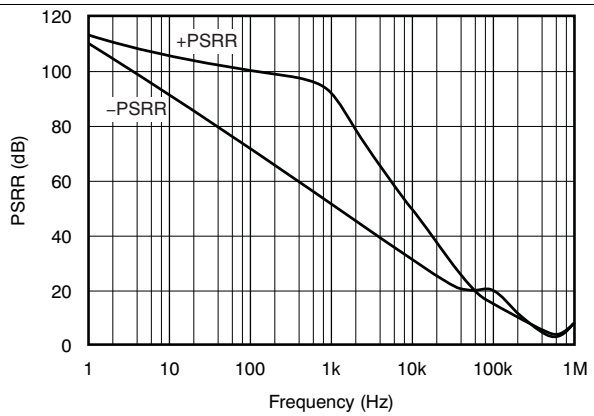


図 6. Power-Supply Rejection Ratio vs Frequency

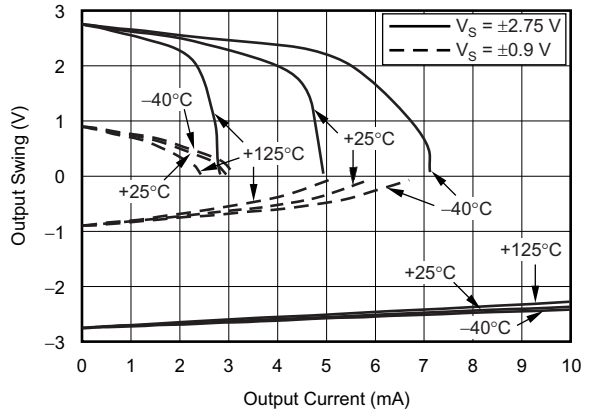


図 7. Output Voltage Swing vs Output Current

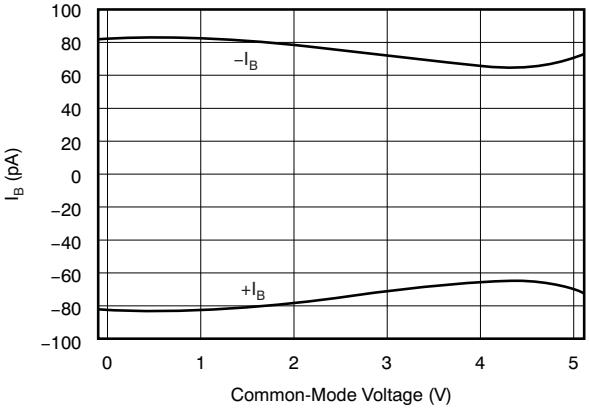


図 8. Input Bias Current vs Common-Mode Voltage

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At T_A = 25°C, V_S = 5 V, and C_L = 0 pF, unless otherwise noted.

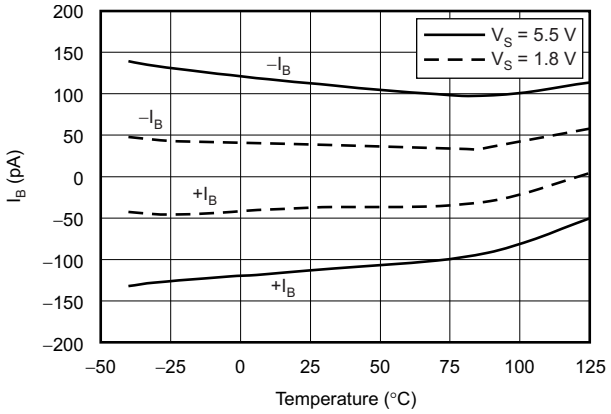


図 9. Input Bias Current vs Temperature

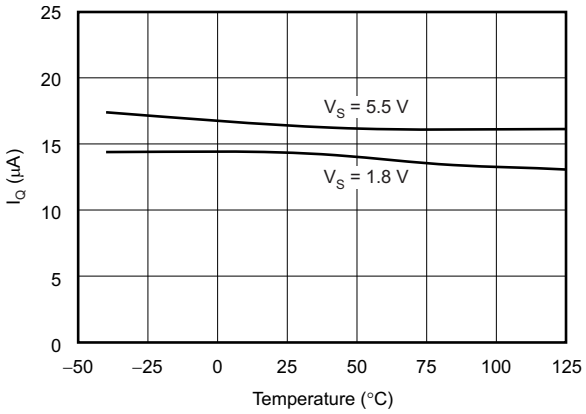


図 10. Quiescent Current vs Temperature

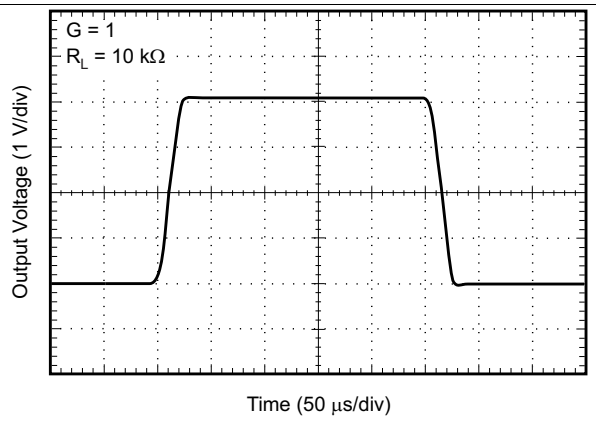


図 11. Large-Signal Step Response

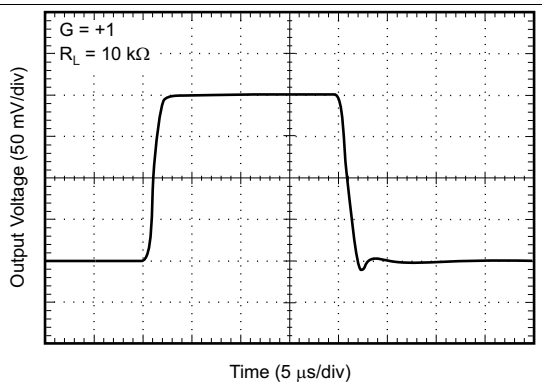


図 12. Small-Signal Step Response

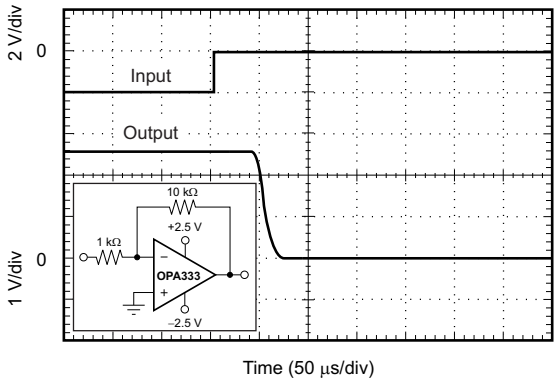


図 13. Positive Overvoltage Recovery

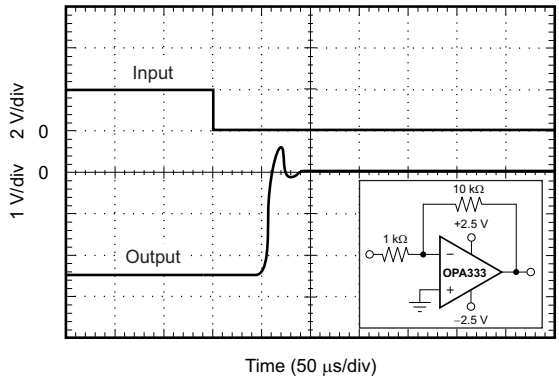


図 14. Negative Overvoltage Recovery

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At T_A = 25°C, V_S = 5 V, and C_L = 0 pF, unless otherwise noted.

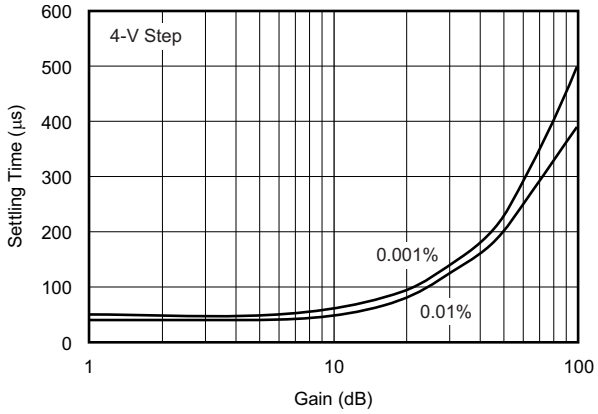


図 15. Settling Time vs Closed-Loop Gain

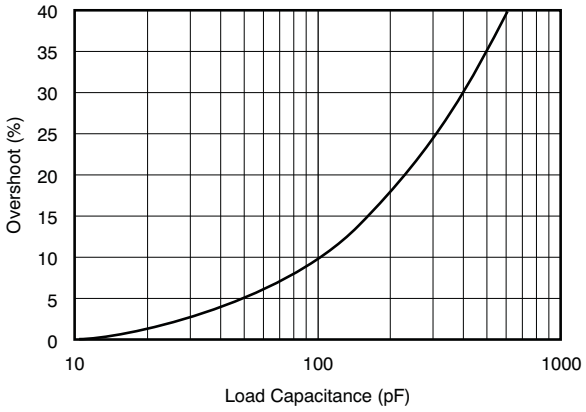


図 16. Small-Signal Overshoot vs Load Capacitance

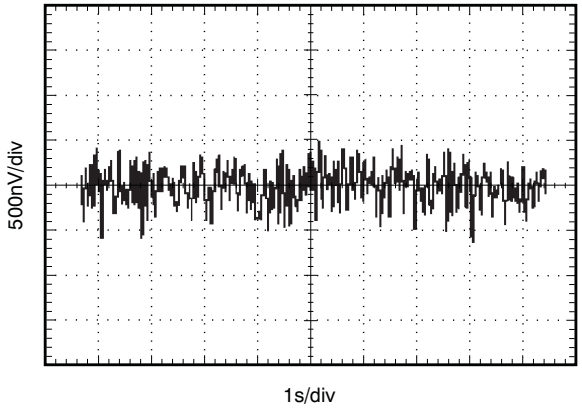


図 17. 0.1-Hz to 10-Hz Noise

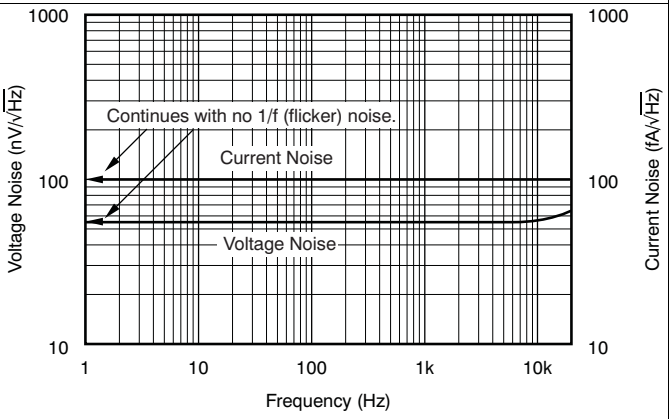


図 18. Current and Voltage Noise Spectral Density vs Frequency

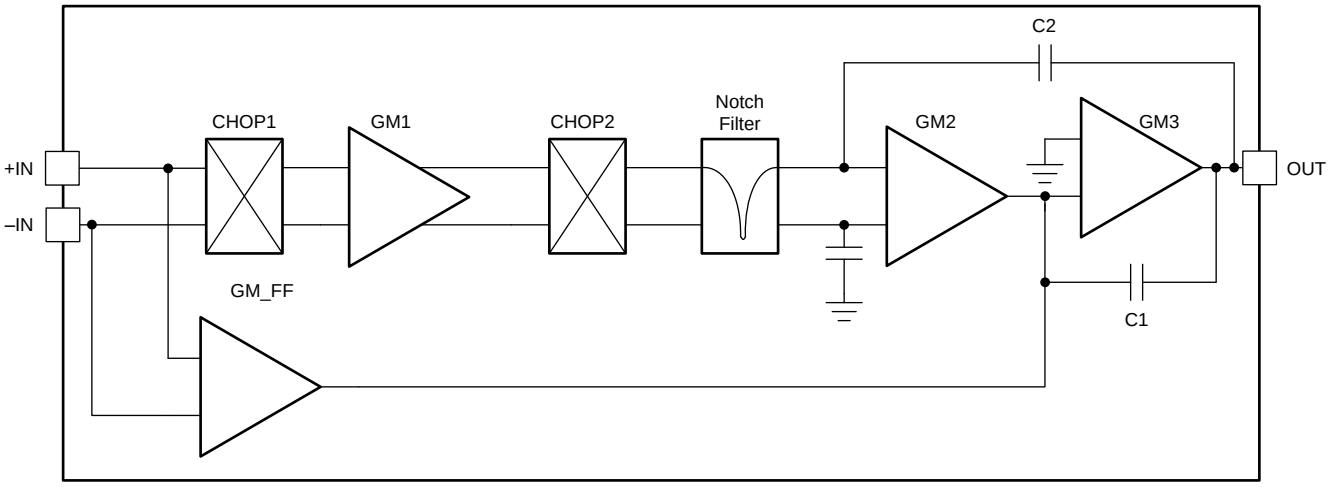
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7 Detailed Description

7.1 Overview

The OPA2333P is a Zero-Drift, low-power, rail-to-rail input and output operational amplifier. The device operates from 1.8 V to 5.5 V, is unity-gain stable, and is suitable for a wide range of general-purpose applications. The Zero-Drift architecture provides ultra-low offset voltage and near-zero offset voltage drift.

7.2 Functional Block Diagram



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7.3 Feature Description

The OPA2333P is unity-gain stable and free from unexpected output phase reversal. This device uses a proprietary auto-calibration technique to provide low offset voltage and very low drift over time and temperature. For lowest offset voltage and precision performance, optimize circuit layout and mechanical conditions. Avoid temperature gradients that create thermoelectric (Seebeck) effects in the thermocouple junctions formed from connecting dissimilar conductors. Cancel these thermally-generated potentials by assuring they are equal on both input terminals. Other layout and design considerations include:

- Use low thermoelectric-coefficient conditions (avoid dissimilar metals).
- Thermally isolate components from power supplies or other heat sources.
- Shield operational amplifier and input circuitry from air currents, such as cooling fans.

Following these guidelines reduces the likelihood of junctions being at different temperatures, which can cause thermoelectric voltages of 0.1 μV/°C or higher, depending on materials used.

7.3.1 Operating Voltage

The OPA2333P operational amplifier operates over a power-supply range of 1.8 V to 5.5 V (±0.9 V to ±2.75 V). Parameters that vary over supply voltage or temperature are shown in the *Typical Characteristics* section.

注意

Supply voltages higher than +7 V (absolute maximum) can permanently damage the device.

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Feature Description (continued)

7.3.2 Input Voltage

The OPA2333P input common-mode voltage range extends 0.1 V beyond the supply rails. The OPA2333P is designed to cover the full range without the troublesome transition region found in some other rail-to-rail amplifiers.

Typically, input bias current is approximately 70 pA; however, input voltages that exceed the power supplies can cause excessive current to flow into or out of the input pins. Momentary voltages greater than the power supply can be tolerated if the input current is limited to 10 mA. This limitation is easily accomplished with an input resistor, as shown in 図 19.

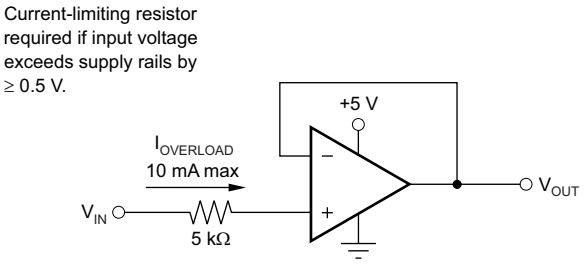


図 19. Input Current Protection

7.3.3 Internal Offset Correction

The OPA2333P operational amplifier uses an auto-calibration technique with a time-continuous 350-kHz operational amplifier in the signal path. This amplifier is zero-corrected every 8 μs using a proprietary technique. Upon power up, the amplifier requires approximately 100 μs to achieve specified V_{OS} accuracy. This design has no aliasing or flicker noise.

7.3.4 Achieving Output Swing to the Op Amp Negative Rail

Some applications require output voltage swings from 0 V to a positive full-scale voltage (such as 2.5 V) with excellent accuracy. With most single-supply operational amplifiers, problems arise when the output signal approaches 0 V, near the lower output swing limit of a single-supply operational amplifier. A good, single-supply operational amplifier may swing close to single-supply ground, but does not reach ground. The output of the OPA2333P can be made to swing to, or slightly below, ground on a single-supply power source. This swing is achieved with the use of the use of another resistor and an additional, more negative power supply than the operational amplifier negative supply. A pulldown resistor can be connected between the output and the additional negative supply to pull the output down below the value that the output would otherwise achieve, as shown in 図 20.

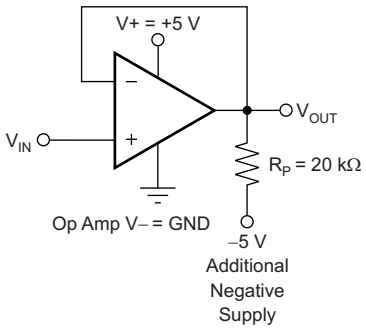


図 20. V_{OUT} Range to Ground

Feature Description (continued)

The OPA2333P has an output stage that allows the output voltage to be pulled to the negative supply rail, or slightly below, using the technique previously described. This technique only works with some types of output stages. The OPA2333P is characterized to perform with this technique; the recommended resistor value is approximately 20 kΩ.

注

This configuration increases the current consumption by several hundreds of microamps.

Accuracy is excellent down to 0 V and as low as –2 mV. Limiting and nonlinearity occur below –2 mV, but excellent accuracy returns after the output is again driven above –2 mV. Lowering the resistance of the pulldown resistor allows the operational amplifier to swing even further below the negative rail. Resistances as low as 10 kΩ can be used to achieve excellent accuracy down to –10 mV.

7.3.5 Specified Start-Up Performance

The OPA2333P has a dedicated start-up circuit that ensures a fast, repeatable startup for all supply conditions. The OPA2333P is specified to have a maximum start-up time that is production-tested as illustrated in the configuration shown in 図 21. Start-up time is defined as the time from when the power supply reaches the minimum specified voltage to the time the output has settled to within 20 mV of the nominal value. See 図 22.

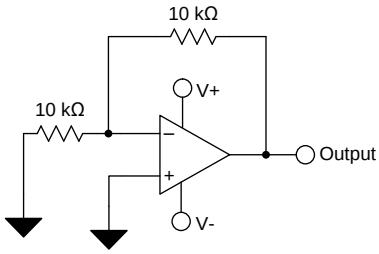


図 21. OPA2333P Equivalent Start-Up Test Configuration

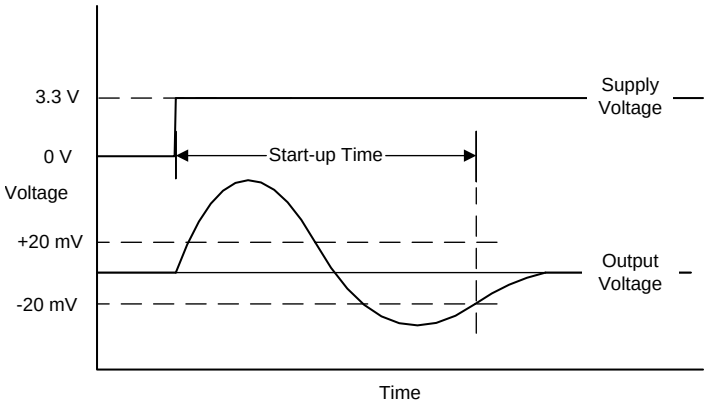


図 22. OPA2333P Start-Up Timing

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Feature Description (continued)

7.3.6 WSON Package

The OPA2333P is offered in an WSON-8 package (also known as *DFN*). The WSON is a QFN package with lead contacts on only two sides of the bottom of the package. This leadless package maximizes board space and enhances thermal and electrical characteristics through an exposed pad.

WSON packages are physically small, have a smaller routing area, improved thermal performance, and improved electrical parasitics. Additionally, the absence of external leads eliminates bent-lead issues.

The WSON package can be easily mounted using standard PCB assembly techniques. See application reports *QFN/SON PCB Attachment* and *Quad Flatpack No-Lead Logic Packages*, both available for download at www.ti.com.

注

The exposed leadframe die pad on the bottom of the package should be connected to V– or left unconnected.

7.4 Device Functional Modes

The OPA2333P device has a single functional mode. The device is powered on as long as the power supply voltage is between 1.8 V (±0.9 V) and 5.5 V (±2.75 V).

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8 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

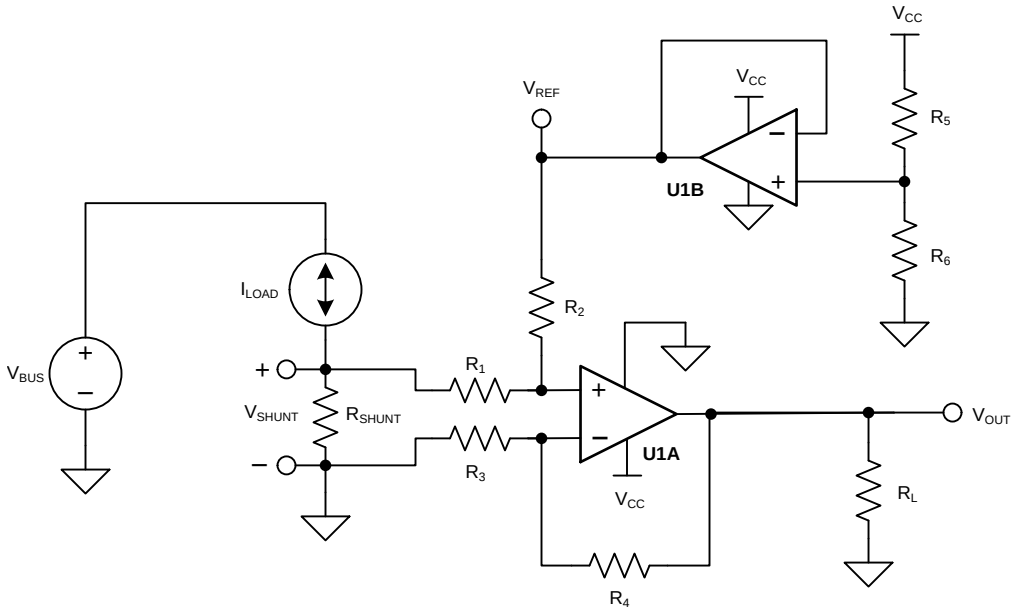
The OPA2333P is a unity-gain stable, precision operational amplifier with very low offset voltage drift; these devices are also free from output phase reversal. Applications with noisy or high-impedance power supplies require decoupling capacitors close to the device power-supply pins. In most cases, 0.1-μF capacitors are adequate.

8.2 Typical Application

8.2.1 Bidirectional Current-Sensing

This single-supply, low-side, bidirectional current-sensing solution detects load currents from –1 A to 1 A. The single-ended output spans from 110 mV to 3.19 V. This design uses the OPA2333P because of its low offset voltage and rail-to-rail input and output. One of the amplifiers is configured as a difference amplifier and the other provides the reference voltage.

図 23 shows the solution.



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図 23. Bidirectional Current-Sensing Schematic

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Typical Application (continued)

8.2.1.1 Design Requirements

This solution has the following requirements:

- Supply voltage: 3.3 V
- Input: –1 A to 1 A
- Output: 1.65 V ±1.54 V (110 mV to 3.19 V)

8.2.1.2 Detailed Design Procedure

The load current, I_{LOAD}, flows through the shunt resistor (R_{SHUNT}) to develop the shunt voltage, V_{SHUNT}. The shunt voltage is then amplified by the difference amplifier, which consists of U1A and R_1 through R_4. The gain of the difference amplifier is set by the ratio of R_4 to R_3. To minimize errors, set $R_2 = R_4$ and $R_1 = R_3$. The reference voltage, V_{REF}, is supplied by buffering a resistor divider using U1B. The transfer function is given by 式 1.

$$V_{OUT} = V_{SHUNT} \times Gain_{Diff_Amp} + V_{REF}$$

where

- $V_{SHUNT} = I_{LOAD} \times R_{SHUNT}$
- $Gain_{Diff_Amp} = \frac{R_4}{R_3}$
- $V_{REF} = V_{CC} \times \left(\frac{R_6}{R_5 + R_6} \right)$

(1)

There are two types of errors in this design: offset and gain. Gain errors are introduced by the tolerance of the shunt resistor and the ratios of R_4 to R_3 and, similarly, R_2 to R_1. Offset errors are introduced by the voltage divider (R_5 and R_6) and how closely the ratio of R_4/R_3 matches R_2/R_1. The latter value impacts the CMRR of the difference amplifier, which ultimately translates to an offset error.

Because this is a low-side measurement, the value of V_{SHUNT} is the ground potential for the system load. Therefore, it is important to place a maximum value on V_{SHUNT}. In this design, the maximum value for V_{SHUNT} is set to 100 mV. 式 2 calculates the maximum value of the shunt resistor given a maximum shunt voltage of 100 mV and maximum load current of 1 A.

$$R_{SHUNT(Max)} = \frac{V_{SHUNT(Max)}}{I_{LOAD(Max)}} = \frac{100\ mV}{1\ A} = 100\ m\Omega \quad (2)$$

The tolerance of R_{SHUNT} is directly proportional to cost. For this design, a shunt resistor with a tolerance of 0.5% was selected. If greater accuracy is required, select a 0.1% resistor or better.

The load current is bidirectional; therefore, the shunt voltage range is –100 mV to 100 mV. This voltage is divided down by R_1 and R_2 before reaching the operational amplifier, U1A. Take care to ensure that the voltage present at the noninverting node of U1A is within the common-mode range of the device. Therefore, it is important to use an operational amplifier, such as the OPA2333P, that has a common-mode range that extends below the negative supply voltage. Finally, to minimize offset error, note that the OPA2333P has a typical offset voltage of ±2 µV (±10 µV maximum).

Given a symmetric load current of –1 A to 1 A, the voltage divider resistors (R_5 and R_6) must be equal. To be consistent with the shunt resistor, a tolerance of 0.5% was selected. To minimize power consumption, 10-kΩ resistors were used.

To set the gain of the difference amplifier, the common-mode range and output swing of the OPA2333P must be considered. 式 3 and 式 4 depict the typical common-mode range and maximum output swing, respectively, of the OPA2333P given a 3.3-V supply.

$$-100\ mV < V_{CM} < 3.4\ V \quad (3)$$

$$100\ mV < V_{OUT} < 3.2\ V \quad (4)$$

The gain of the difference amplifier can now be calculated as shown in 式 5.

$$Gain_{Diff_Amp} = \frac{V_{OUT_Max} - V_{OUT_Min}}{R_{SHUNT} \times (I_{MAX} - I_{MIN})} = \frac{3.2\ V - 100\ mV}{100\ m\Omega \times [1\ A - (-1A)]} = 15.5\ \frac{V}{V} \quad (5)$$

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Typical Application (continued)

The resistor value selected for R_1 and R_3 was 1 kΩ. 15.4 kΩ was selected for R_2 and R_4 because it is the nearest standard value. Therefore, the ideal gain of the difference amplifier is 15.4 V/V.

The gain error of the circuit primarily depends on R_1 through R_4. As a result of this dependence, 0.1% resistors were selected. This configuration reduces the likelihood that the design requires a two-point calibration. A simple one-point calibration, if desired, removes the offset errors introduced by the 0.5% resistors.

8.2.1.3 Application Curve

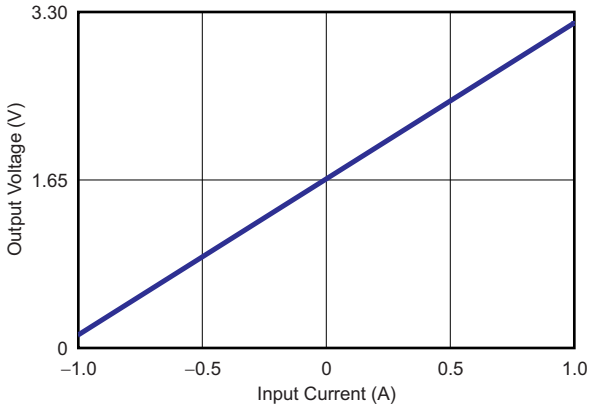


図 24. Bidirectional Current-Sensing Circuit Performance: Output Voltage vs Input Current

8.2.2 High-Side Voltage-to-Current (V-I) Converter

The circuit shown in 図 25 is a high-side voltage-to-current (V-I) converter. It translates to an input voltage of 0 V to 2 V and output current of 0 mA to 100 mA. 図 26 shows the measured transfer function for this circuit. The low offset voltage and offset drift of the OPA2333P facilitate excellent dc accuracy for the circuit.

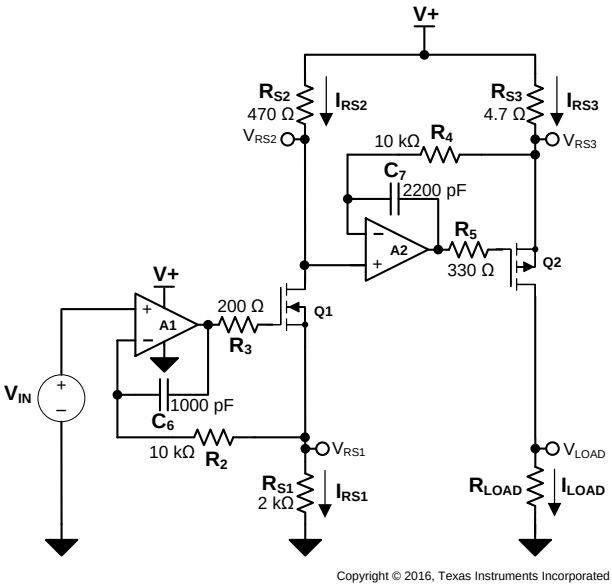


図 25. High-Side Voltage-to-Current (V-I) Converter

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Typical Application (continued)

8.2.2.1 Design Requirements

The design requirements are as follows:

- Supply Voltage: 5 V DC
- Input: 0 V to 2 V DC
- Output: 0 mA to 100 mA DC

8.2.2.2 Detailed Design Procedure

The V-I transfer function of the circuit is based on the relationship between the input voltage, V_{IN}, and the three current sensing resistors, R_{S1}, R_{S2}, and R_{S3}. The relationship between V_{IN} and R_{S1} determines the current that flows through the first stage of the design. The current gain from the first stage to the second stage is based on the relationship between R_{S2} and R_{S3}.

For a successful design, pay close attention to the dc characteristics of the operational amplifier chosen for the application. To meet the performance goals, this application benefits from an operational amplifier with low offset voltage, low temperature drift, and rail-to-rail output. The OPA2333P CMOS operational amplifier is a high-precision, 2-uV offset, 0.02-μV/°C drift amplifier optimized for low-voltage, single-supply operation with an output swing to within 50 mV of the positive rail. The OPA2333P family uses chopping techniques to provide low initial offset voltage and near-zero drift over time and temperature. Low offset voltage and low drift reduce the offset error in the system, making these devices appropriate for precise dc control. The rail-to-rail output stage of the OPA2333P ensures that the output swing of the operational amplifier is able to fully control the gate of the MOSFET devices within the supply rails.

A detailed error analysis, design procedure, and additional measured results are given in TIPD102.

8.2.2.3 Application Curve

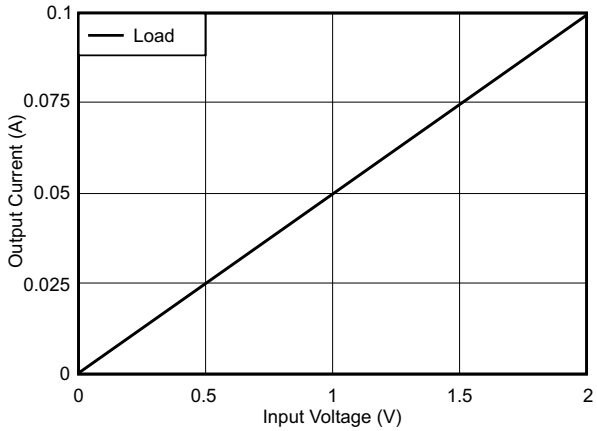


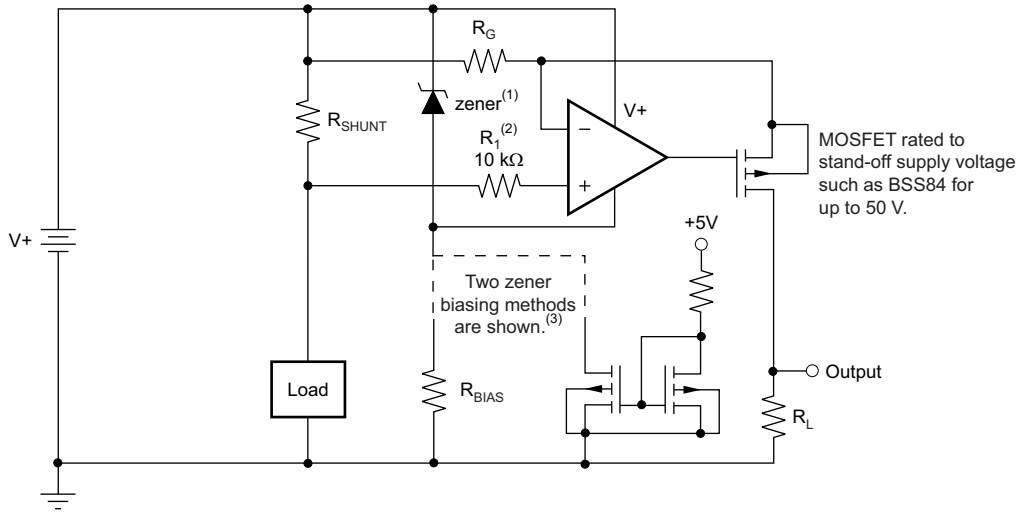
図 26. Measured Transfer Function for High-Side V-I Converter

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Typical Application (continued)

8.2.3 Other Applications

Additional application ideas are shown in 図 27 and 図 28.



(1) Zener rated for op amp supply capability (that is, 5.1 V for OPA2333P).

(2) Current-limiting resistor.

(3) Choose zener biasing resistor or dual N-MOSFETs (FDG6301N, NTJD4001N, or Si1034).

図 27. High-Side Current Monitor

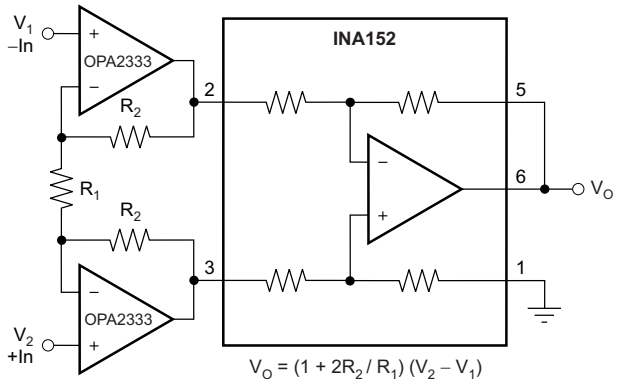


図 28. Precision Instrumentation Amplifier

9 Power Supply Recommendations

The OPA2333P is specified for operation from 1.8 V to 5.5 V (±0.9 V to ±2.75 V); many specifications apply from –40°C to 125°C. The *Typical Characteristics* presents parameters that can exhibit significant variance with regard to operating voltage or temperature.

注意

Supply voltages larger than 7 V can permanently damage the device (see *Absolute Maximum Ratings*).

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TI recommends placing 0.1-μF bypass capacitors close to the power-supply pins to reduce errors coupling in from noisy or high-impedance power supplies. For more detailed information on bypass capacitor placement, refer to the *Layout* section.

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10 Layout

10.1 Layout Guidelines

10.1.1 General Layout Guidelines

Pay attention to good layout practices. Keep traces short and when possible and use a printed-circuit-board (PCB) ground plane with surface-mount components placed as close to the device pins as possible. Place a 0.1-μF capacitor closely across the supply pins. Apply these guidelines throughout the analog circuit to improve performance and provide benefits, such as reducing the electromagnetic interference (EMI) susceptibility.

Operational amplifiers vary in susceptibility to radio frequency interference (RFI). RFI can generally be identified as a variation in offset voltage or DC signal levels with changes in the interfering RF signal. The OPA2333P is specifically designed to minimize susceptibility to RFI and demonstrates remarkably low sensitivity compared to previous generation devices. Strong RF fields may still cause varying offset levels.

10.1.2 WSON (DFN) Layout Guidelines

Solder the exposed leadframe die pad on the WSON package to a thermal pad on the PCB. A mechanical drawing showing an example layout is attached at the end of this data sheet. Refinements to this layout may be necessary based on assembly process requirements. Mechanical drawings located at the end of this data sheet list the physical dimensions for the package and pad. The five holes in the landing pattern are optional, and are intended for use with thermal vias that connect the leadframe die pad to the heatsink area on the PCB.

Soldering the exposed pad significantly improves board-level reliability during temperature cycling, key push, package shear, and similar board-level tests. Even with applications that have low-power dissipation, the exposed pad must be soldered to the PCB to provide structural integrity and long-term reliability.

10.2 Layout Example

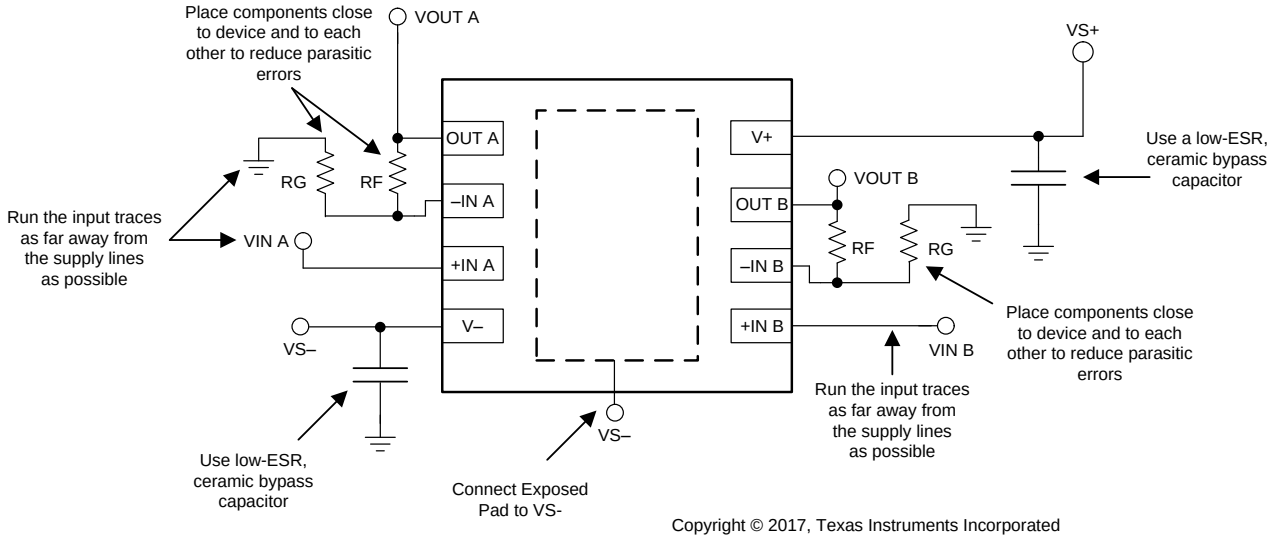


図 29. Layout Example

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11 デバイスおよびドキュメントのサポート

11.1 デバイス・サポート

11.1.1 開発サポート

この製品の開発サポートについては、以下を参照してください。

- *『0V～2V入力、0mA～100mA出力、1%フルスケール誤差のハイサイドV-Iコンバータ』*
- *『0V～5V入力、0μA～5μA出力の低レベルV-Iコンバータのリファレンス・デザイン』*
- *『ADS8881x 18ビット、1MSPS、シリアル・インターフェイス、microPower、小型、精密差動入力、SARアナログ/デジタル・コンバータ』*
- *『最小の歪みとノイズを実現するため最適化された18ビット、1MSPSのデータ収集のリファレンス・デザイン』*
- *『ADS1100 自己較正、16ビットのアナログ/デジタル・コンバータ』*
- *『REF31xx 最大15ppm/℃、100μA、SOT-23シリーズ基準電圧』*
- *『INA326、INA327 高精度、低ドリフト係数、CMOS計装用アンプ』*

11.2 ドキュメントのサポート

11.2.1 関連資料

関連資料については、以下を参照してください。

- *『QFN/SONのPCB実装』*
- *『ゼロドリフト・アンプ: 特長と利点』*

11.3 ドキュメントの更新通知を受け取る方法

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11.4 コミュニティ・リソース

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11.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

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12 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。この情報は、そのデバイスについて利用可能な最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
OPA2333PIDSGR	Active	Production	WSON (DSG) | 8	3000 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	1GFY
OPA2333PIDSGR.B	Active	Production	WSON (DSG) | 8	3000 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	1GFY
OPA2333PIDSGRG4	Active	Production	WSON (DSG) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	1GFY
OPA2333PIDSGRG4.B	Active	Production	WSON (DSG) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	1GFY
OPA2333PIDSGT	Active	Production	WSON (DSG) | 8	250 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	1GFY
OPA2333PIDSGT.B	Active	Production	WSON (DSG) | 8	250 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	1GFY

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

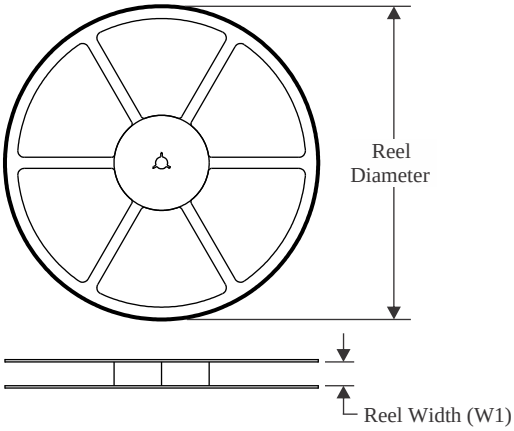
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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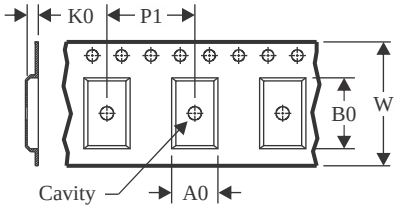
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

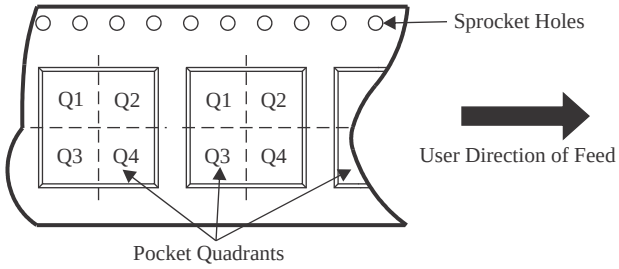


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

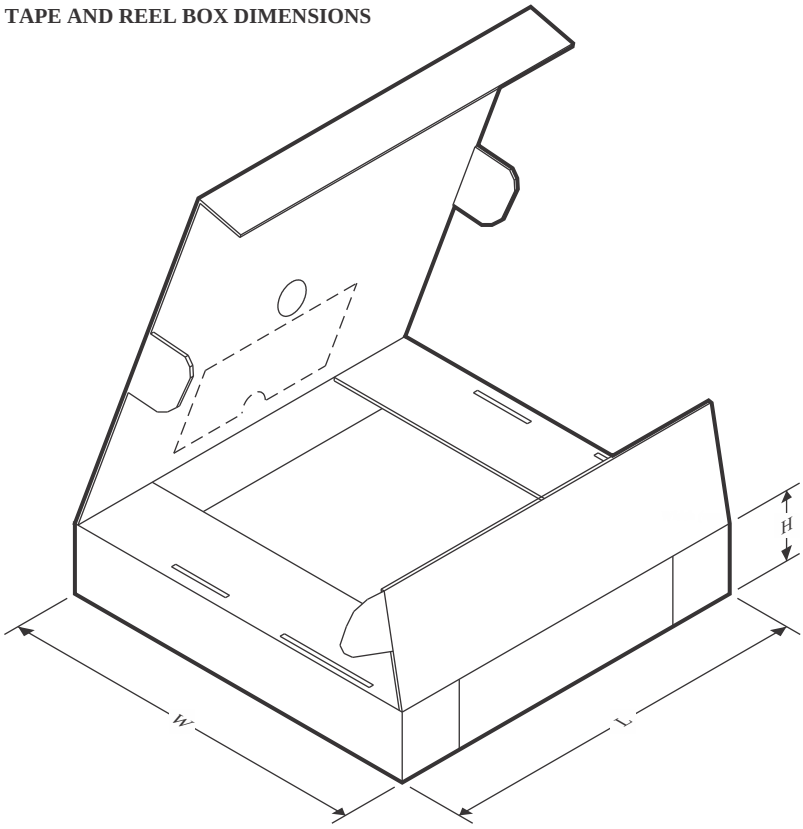
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA2333PIDSGR	WSON	DSG	8	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
OPA2333PIDSGRG4	WSON	DSG	8	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
OPA2333PIDSGT	WSON	DSG	8	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA2333PIDSGR	WSON	DSG	8	3000	210.0	185.0	35.0
OPA2333PIDSGRG4	WSON	DSG	8	3000	210.0	185.0	35.0
OPA2333PIDSGT	WSON	DSG	8	250	210.0	185.0	35.0

GENERIC PACKAGE VIEW

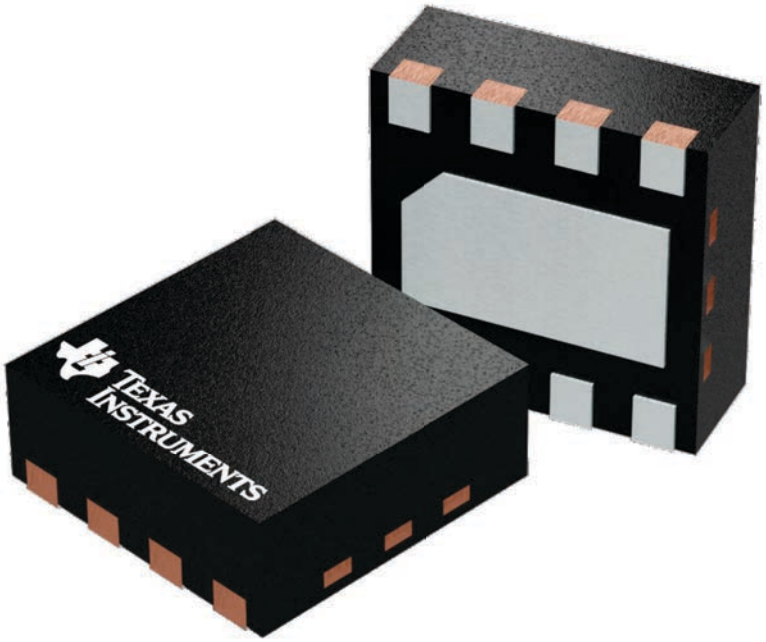
DSG 8

WSON - 0.8 mm max height

2 x 2, 0.5 mm pitch

PLASTIC SMALL OUTLINE - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



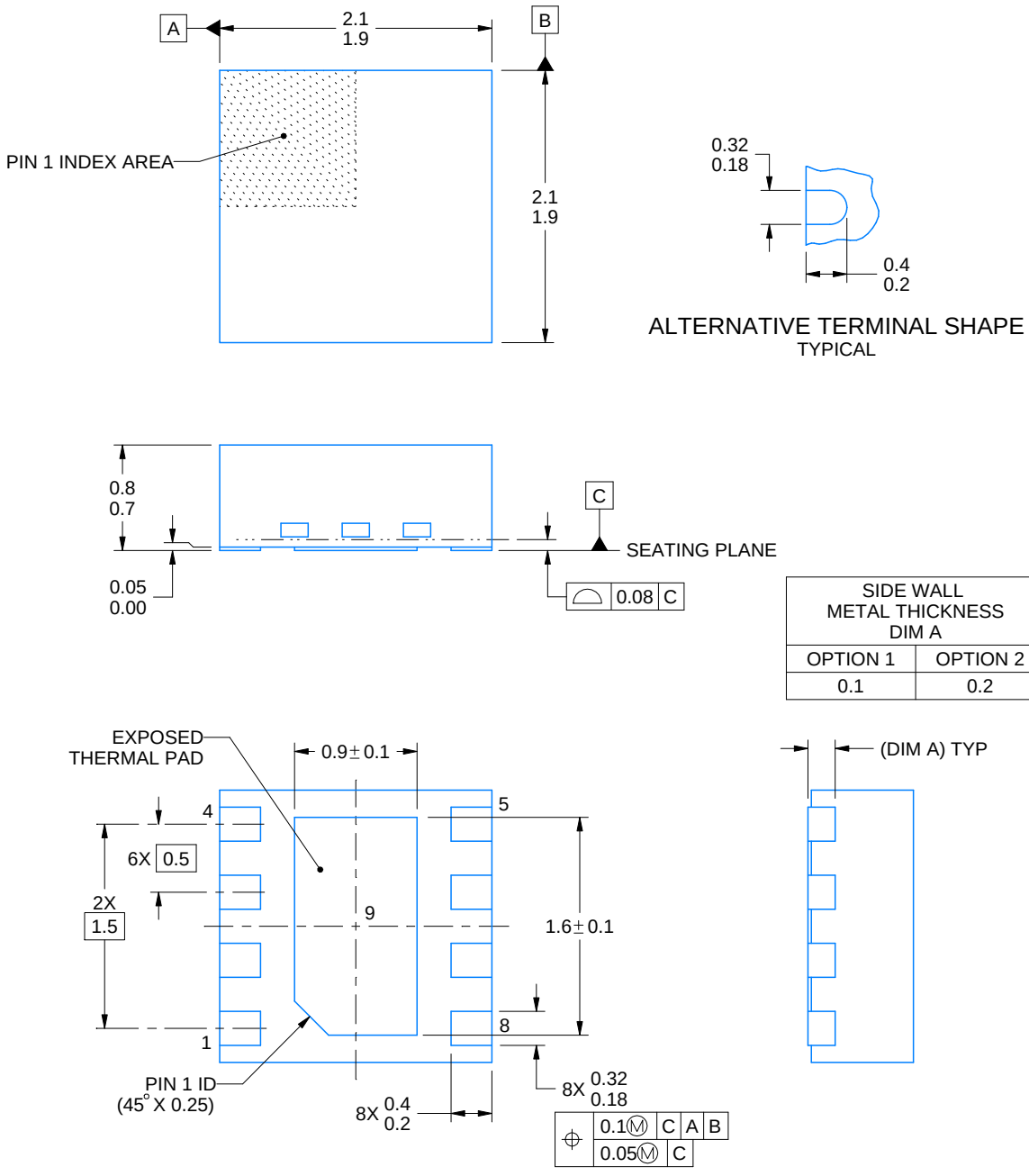
4224783/A

PACKAGE OUTLINE

DSG0008A

WSON - 0.8 mm max height

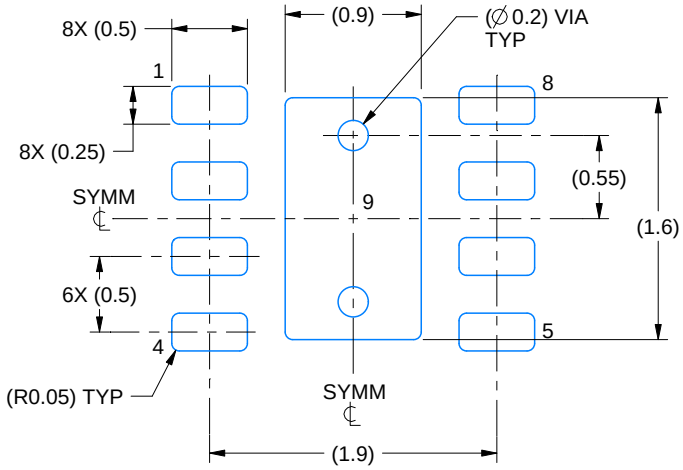
PLASTIC SMALL OUTLINE - NO LEAD



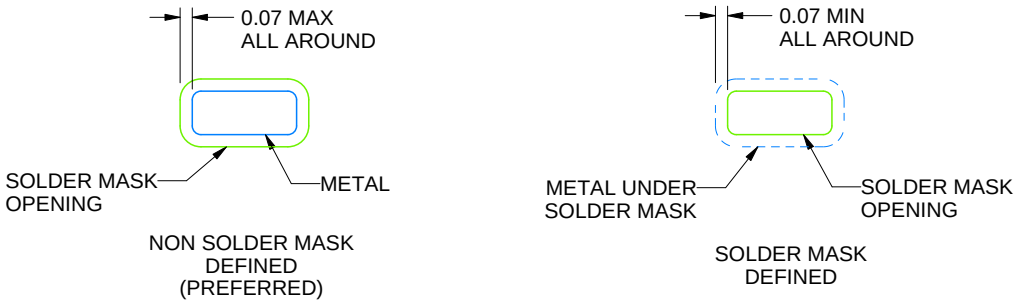
4218900/E 08/2022

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:20X

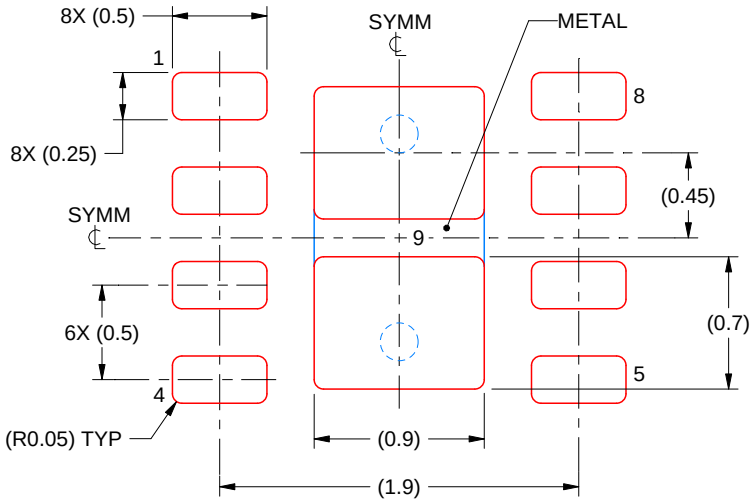


SOLDER MASK DETAILS

4218900/E 08/2022

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 9:
87% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:25X

4218900/E 08/2022

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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