OPA355-Q1 200MHz、シャットダウン機能付きCMOSオペアンプ

1 特長

- **車載アプリケーションに対応**
- **下記内容でAEC-Q100認定済み**
  - デバイス温度グレード 1: 動作時周囲温度 –40℃～+125°C
  - デバイスHBM ESD分類レベル2
  - デバイスCDM ESD分類レベルC4B
- **ユニティ・ゲイン帯域幅**: 450MHz
- **広い帯域幅**: 200MHz GBW
- **高いスルー・レート**: 360V/µs
- **低ノイズ**: 5.8nV/√Hz
- **非常に優れたビデオ性能**
  - 差動ゲイン: 0.02%
  - 差動位相: 0.05° (0.1dB)
  - ゲイン・フラットネス: 75MHz
- **入力範囲にグランドを含む**
- **レール・ツー・レール出力(100mV以内)**
- **低い入力バイアス電流**: 3pA
- **低いシャットダウン時電流**: 3.4µA
- **イネーブル/ディセーブル時間**: 100ns/30ns
- **サーマル・シャットダウン**
- **単一電源動作電圧範囲**: 2.5V～5.5V
- *Micro*SIZEパッケージ

2 アプリケーション

- **車載用**
- **アクティブ・フィルタ**
- **高速積分器**
- A/Dコンバータ(ADC)入力バッファ
- D/Aコンバータ(DAC)出力アンプ

3 概要

OPA355-Q1デバイスは高速の電圧帰還CMOSオペアンプで、広い帯域幅を必要とするアプリケーション用に設計されています。OPA355-Q1デバイスはユニティ・ゲイン安定で、大きな出力電流を駆動できます。さらに、OPA355-Q1デバイスにはデジタル・シャットダウン(イネーブル)機能があります。この機能により、アイドル時の省電力を実現し、出力をハイ・インピーダンス状態にして出力多重化をサポートします。差動ゲインは0.02%、差動位相は0.05°です。静止電流はチャネルごとに8.3mAです。

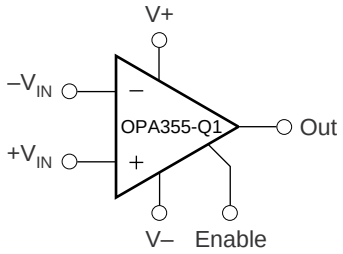
OPA355-Q1デバイスは、最低2.5V (±1.25V)、最高5.5V (±2.75V)のシングル電源またはデュアル電源で動作するよう最適化されています。OPA355-Q1デバイスの同相入力範囲はグランドより100mV下、V+より1.5V上まで伸びています。出力スイングはレールから100mV以内で、広いダイナミック・レンジに対応しています。

OPA355-Q1デバイスは単一のSOT-23-6パッケージで供給され、-40℃～+125℃の拡張温度範囲で動作が規定されています。

製品情報(1)

型番	パッケージ	本体サイズ(公称)
OPA355-Q1	SOT-23 (6)	2.90mm×1.60mm

(1) 提供されているすべてのパッケージについては、データシートの末尾にある注文情報を参照してください。



英語版のTI製品についての情報を翻訳したこの資料は、製品の概要を確認する目的で便宜的に提供しているものです。該当する正式な英語版の最新情報は、www.ti.comで閲覧でき、その内容が常に優先されます。TIでは翻訳の正確性および妥当性につきましては一切保証いたしません。実際の設計などの前には、必ず最新版の英語版をご参照くださいますようお願いいたします。

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4 改訂履歴

Revision B (June 2014) から **Revision C** に変更 **Page**

- Deleted "C55" marking on pinout drawing in *Pin Configuration and Functions* section ... 3
- Added Pin Functions table to *Pin Configuration and Functions* section ... 3
- Deleted storage temperature range from *ESD Ratings* table and moved to *Absolute Maximum Ratings* table ... 4
- Changed title of *Handling Ratings* table to *ESD Ratings* table ... 4
- Added *Recommended Operating Conditions* table ... 4
- 追加 *Functional Block Diagram* ... 12
- 削除 "Independent enable pins are available for each channel, which provide maximum design flexibility" from *Enable Function* section ... 12
- 削除 *Input and ESD Protection* subsection in *Feature Description* section ... 13
- 追加 *Device Functional Modes* section ... 13
- 追加 *Typical Applications* section to *Application and Implementation* section ... 14
- 追加 *Design Requirements* subsection to *Typical Applications* section ... 14
- 追加 *Detailed Design Procedure* subsection to *Typical Application* section ... 14
- 追加 application curves to the *Typical Application* section ... 16
- 追加 *High-Impedance Sensor Interface*, *Driving ADCs*, and *Active Filter* subsections to *Typical Application* section ... 16
- 追加 *Power Supply Recommendations* section ... 19
- 追加 layout example image to *Layout* section ... 19

Revision A (December 2013) から **Revision B** に変更 **Page**

- デバイスのステータスを「*製品プレビュー*」から「*量産データ*」に 変更 ... 1

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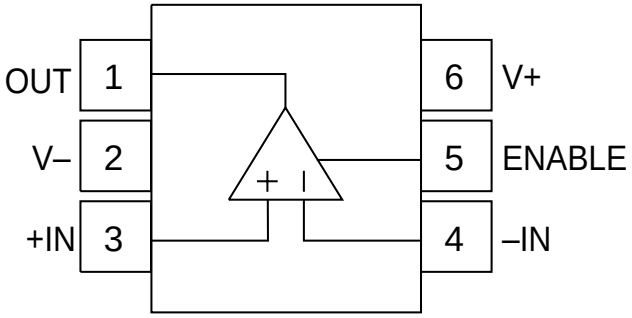
5 Device Comparison Table

5.1 Device Comparison Table

OPA355-Q1 RELATED PRODUCTS	FEATURES
OPA356	200-MHz, Rail-to-Rail Output, CMOS, No Shutdown
OPAx350	38-MHz, Rail-to-Rail Input and Output, CMOS
OPAx631	75-MHz, Rail-to-Rail Output
OPAx634	150-MHz, Rail-to-Rail Output
THS412x	Differential Input and Output, 3.3-V Supply

6 Pin Configuration and Functions

DBV Package
6-Pin SOT-23
Top View



Pin 1 of the SOT-23-6 is determined by orienting the package marking as indicated in the diagram.

Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
ENABLE	5	—	Amplifier power down. Low = disabled, high = normal operation (pin must be driven) .
IN+	3	I	Noninverting input pin
IN–	4	I	Inverting input pin
OUT	1	O	Output pin
V+	6	—	Positive power supply
V–	2	—	Negative power supply

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7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Supply voltage	V+ to V–		7.5	V
Signal input terminals	Voltage	(V–) – 0.5	(V+) + 0.5	V
	Current		10	mA
Output short circuit(2)		Continuous		
Operating temperature		–55	150	°C
Junction temperature			160	°C
Lead temperature (soldering, 10 seconds)			300	°C
Storage temperature range, T_{stg}		–65	150	°C

(1) Stresses above *Absolute Maximum Ratings* may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.
(2) Short-circuit to ground, one amplifier per package.

7.2 ESD Ratings

			MIN	MAX	UNIT
$V_{(ESD)}$ Electrostatic discharge	Human body model (HBM), per AEC Q100-002(1)			2000	V
	Charged device model (CDM), per AEC Q100-011	Corner pins (1, 3, 4, and 6)		750	
		Other pins		500	

(1) AEC Q100-002 indicates HBM stressing is done in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	NOM	MAX	UNIT
V_S Total supply voltage	2.7		5.5	V
T_A Ambient temperature	–40	25	125	°C

7.4 Thermal Information

THERMAL METRIC(1)		OPA355-Q1 DBV (SOT-23) 6 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	187.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	126.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	32.6	°C/W
ψ_{JT}	Junction-to-top characterization parameter	24.1	°C/W
ψ_{JB}	Junction-to-board characterization parameter	32.1	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

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7.5 Electrical Characteristics

V_S = 2.7 V to 5.5 V (single-supply). At T_A = 25°C, R_F = 604 Ω, R_L = 150 Ω, and connected to V_S / 2, (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
OFFSET VOLTAGE							
V_{OS}	Input offset voltage	V_S = 5 V	T_A = 25°C		±2	±9	mV
			T_A = –40°C to +125°C			±15	
DV_{OS}/dT	Input offset voltage vs temperature	T_A = 25°C					µV/°C
		T_A = –40°C to +125°C			±7		
PSRR	Input offset voltage vs power supply	V_S = 2.7 to 5.5 V, V_{CM} = V_S / 2 – 0.15 V	T_A = 25°C		±80	±350	µV/V
			T_A = –40°C to +125°C				
INPUT BIAS CURRENT							
I_B	Input bias current	T_A = 25°C			3	±50	pA
		T_A = –40°C to +125°C				±50	
I_{OS}	Input offset current	T_A = 25°C			±1		pA
		T_A = –40°C to +125°C					
NOISE							
e_n	Input noise voltage density	f = 1 MHz	T_A = 25°C		5.8		$nV/\sqrt{Hz}$
			T_A = –40°C to +125°C				
i_n	Current noise density	f = 1 MHz	T_A = 25°C		50		$fA/\sqrt{Hz}$
			T_A = –40°C to +125°C				
INPUT VOLTAGE RANGE							
V_{CM}	Common-mode voltage range	T_A = 25°C		(V–) – 0.1		(V+) – 1.5	V
		T_A = –40°C to +125°C					
CMRR	Common-mode rejection ratio	V_S = 5.5 V, –0.1 V < V_{CM} < 4 V	T_A = 25°C	66	80		dB
			T_A = –40°C to +125°C	66			
INPUT IMPEDANCE							
	Differential	T_A = 25°C			10^{13} || 1.5		Ω || pF
		T_A = –40°C to +125°C					
	Common-mode	T_A = 25°C			10^{13} || 1.5		Ω || pF
		T_A = –40°C to +125°C					
OPEN-LOOP GAIN							
	Open-loop gain	V_S = 5 V, 0.3 V < V_O < 4.7 V	T_A = 25°C	84	92		dB
			T_A = –40°C to +125°C	80			
FREQUENCY RESPONSE							
f_{-3dB}	Small-signal bandwidth	G = 1, V_O = 100 mVp-p, R_F = 0 Ω, T_A = 25°C			450		MHz
		G = 2, V_O = 100 mVp-p, R_L = 50 Ω, T_A = 25°C			100		MHz
		G = 2, V_O = 100 mVp-p, R_L = 150 Ω, T_A = 25°C			170		MHz
		G = 2, V_O = 100 mVp-p, R_L = 1 kΩ, T_A = 25°C			200		MHz
GBW	Gain-bandwidth product	G = 10, R_L = 1 kΩ, T_A = 25°C			200		MHz
$f_{0.1\ dB}$	Bandwidth for 0.1-db gain flatness	G = 2, V_O = 100 mVp-p, R_F = 560 Ω, T_A = 25°C			75		MHz
SR	Slew rate	V_S = 5 V, G = 2, 4-V output step, T_A = 25°C			300 / –360		V/µs
	Rise and fall time	G = 2, V_O = 200 mVp-p, 10% to 90%, T_A = 25°C			2.4		ns
		G = 2, V_O = 2 Vp-p, 10% to 90%, T_A = 25°C			8		ns
	Settling time	V_S = 5 V, G = 2, 2-V output step, 0.1%, T_A = 25°C			30		ns
		V_S = 5 V, G = 2, 2-V output step, 0.01%, T_A = 25°C			120		ns
	Overload recovery time	V_I × G = V_S, T_A = 25°C			8		ns

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Electrical Characteristics (continued)

V_S = 2.7 V to 5.5 V (single-supply). At T_A = 25°C, R_F = 604 Ω, R_L = 150 Ω, and connected to V_S / 2, (unless otherwise noted)

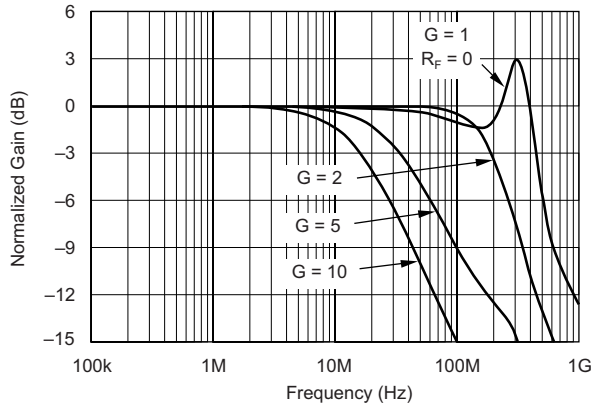
PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
	Harmonic distortion	G = 2, f = 1 MHz, V_O = 2 Vp-p, R_L = 200 Ω T_A = 25°C (second harmonic)			–81		dBc
		G = 2, f = 1 MHz, V_O = 2 Vp-p, R_L = 200 Ω T_A = 25°C (third harmonic)			–93		dBc
	Differential gain error	NTSC, R_L = 150 Ω, T_A = 25°C			0.02%		
	Differential phase error	NTSC, R_L = 150 Ω, T_A = 25°C			0.05		°
OUTPUT							
	Voltage output swing from rail	V_S = 5 V, R_L = 150 Ω, A_{OL} > 84 dB			0.2	0.3	V
		V_S = 5 V, R_L = 1 kΩ			0.1		V
I_O	Output current (continuous) (1)				±60		mA
	Output current (peak) (1)	V_S = 5 V, T_A = 25°C			±100		mA
		V_S = 3 V, T_A = 25°C			±80		
	Closed-loop output impedance	f < 100 kHz			0.02		Ω
POWER SUPPLY							
V_S	Specified voltage range	T_A = 25°C		2.7		5.5	V
	Operating voltage range	T_A = 25°C			2.5 to 5.5		V
I_Q	Quiescent current (per amplifier)	V_S = 5 V, enabled; I_O = 0	T_A = 25°C		8.3	11	mA
			T_A = –40°C to +125°C			14	
SHUTDOWN							
	Logic-LOW threshold (2) (disabled)	T_A = 25°C				0.8	V
	Logic-HIGH threshold (2) (enabled)	T_A = 25°C		2			V
	Enable time	T_A = 25°C			100		ns
	Disable time	T_A = 25°C			30		ns
	Shutdown current (per amplifier)	V_S = 5 V, disabled, T_A = 25°C			3.4		µA
THERMAL SHUTDOWN							
	Junction temperature	Shutdown, T_A = 25°C			160		°C
		Reset from shutdown, T_A = 25°C			140		°C
	Specified range	T_A = 25°C		–40		125	°C
	Operating range	T_A = 25°C		–55		150	°C
	Storage range	T_A = 25°C		–65		150	°C

(1) See the *Output Voltage Swing vs Output Current* (図 21 and 図 23) in the *Typical Characteristics* section.
(2) Logic LOW and HIGH levels are CMOS logic compatible. They are referenced to V–.

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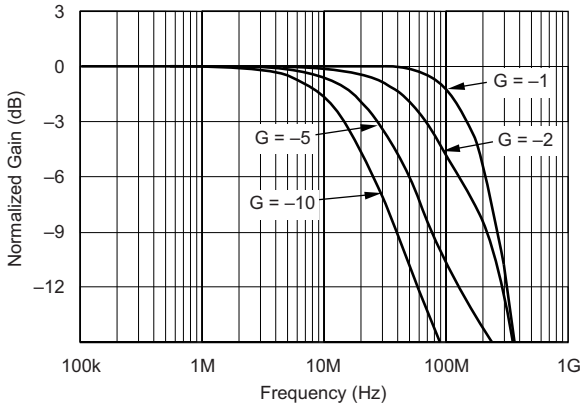
7.6 Typical Characteristics

T_A = 25°C, V_S = 5 V, G = 2, R_F = 604 Ω, and R_L = 150 Ω connected to V_S / 2, (unless otherwise noted)



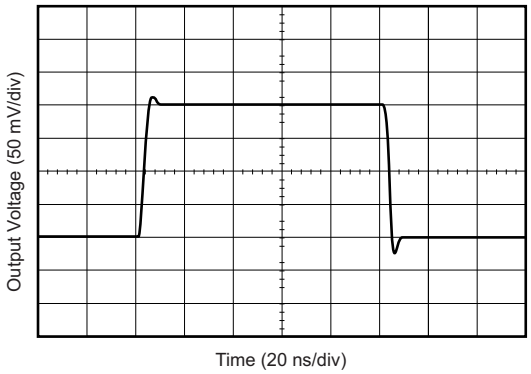
V_O = 0.1 V_{P-P}

図 1. Noninverting Small-Signal Frequency Response



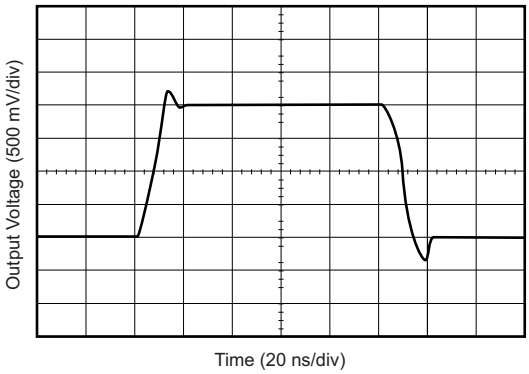
V_O = 0.1 V_{P-P}

図 2. Inverting Small-Signal Frequency Response



G = 2

図 3. Noninverting Small-Signal Step Response



G = 2

図 4. Noninverting Large-Signal Step Response

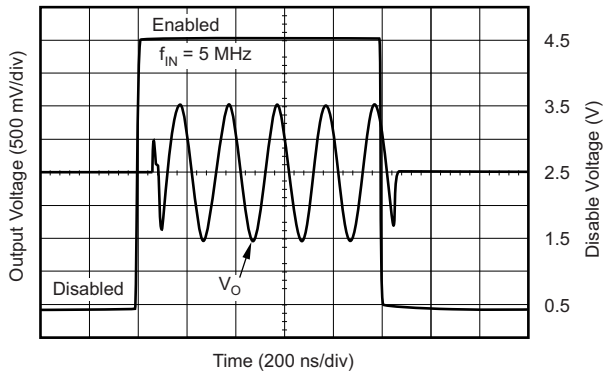
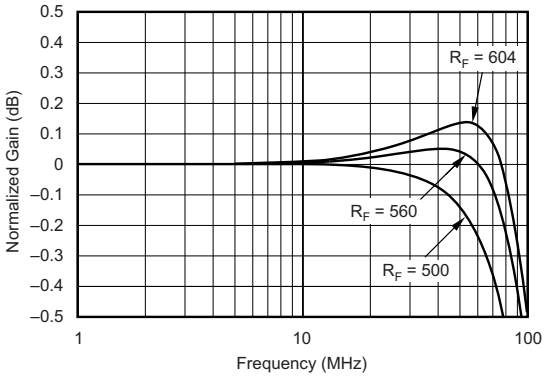


図 5. Large-Signal Disable and Enable Response

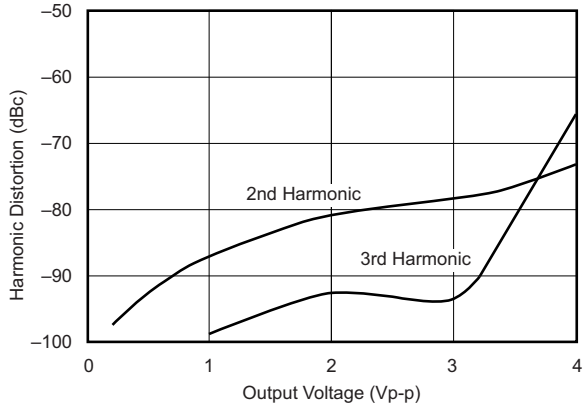


C_L = 0 pF V_O = 0.1 V_{P-P}

図 6. 0.1-dB Gain Flatness for Various R_F Values?

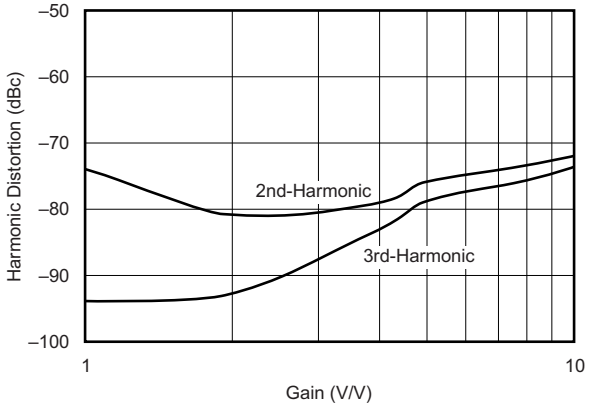
Typical Characteristics (continued)

T_A = 25°C, V_S = 5 V, G = 2, R_F = 604 Ω, and R_L = 150 Ω connected to V_S / 2, (unless otherwise noted)



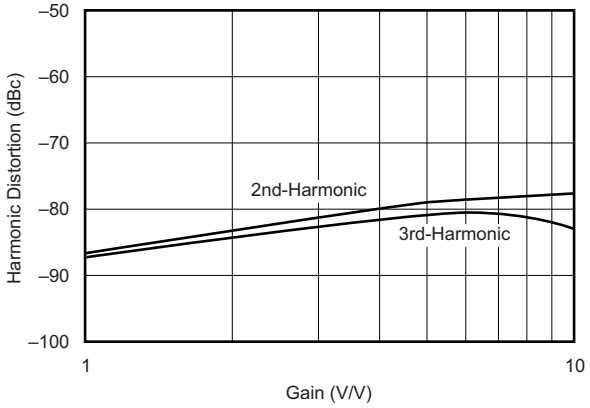
R_L = 200 f = 1 MHz

図 7. Harmonic Distortion vs Output Voltage



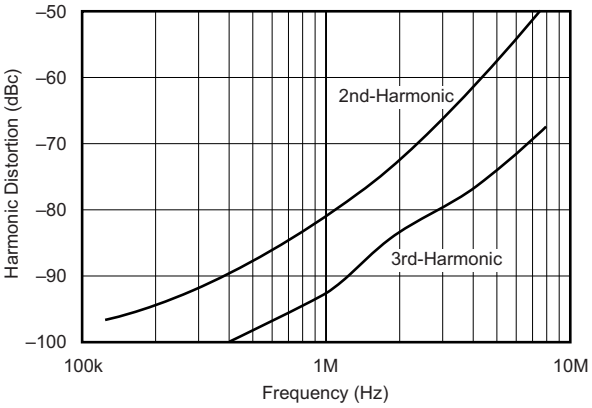
R_L = 200 V_O = 2 V_{P-P} f = 1 MHz

図 8. Harmonic Distortion vs Noninverting Gain



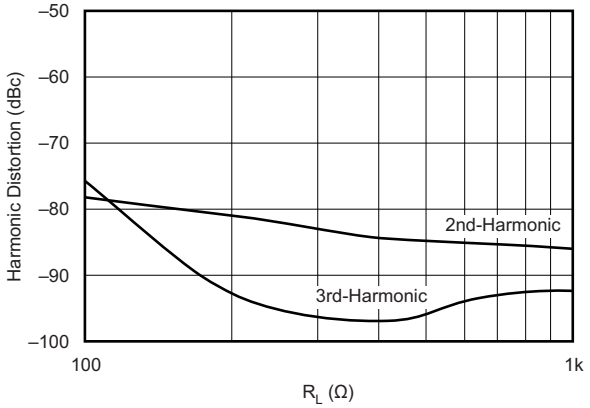
R_L = 200 V_O = 2 V_{P-P} f = 1 MHz

図 9. Harmonic Distortion vs Inverting Gain



R_L = 200 V_O = 2 V_{P-P}

図 10. Harmonic Distortion vs Frequency



f = 1 MHz V_O = 2 V_{P-P}

図 11. Harmonic Distortion vs Load Resistance

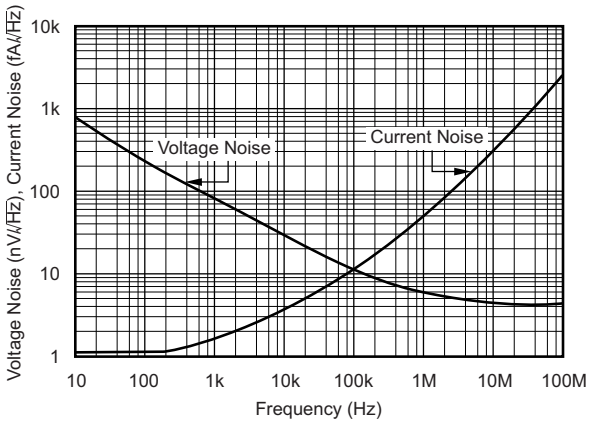
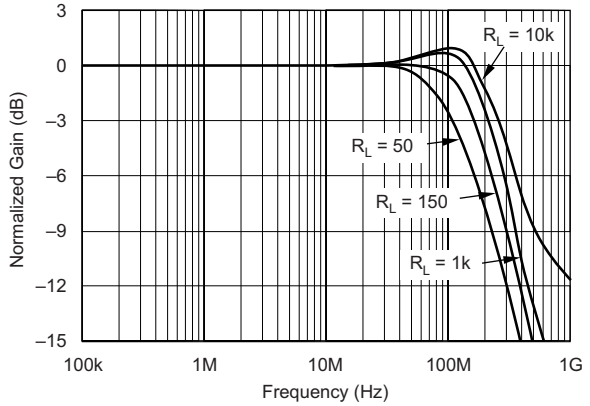


図 12. Input Voltage and Current Noise Spectral Density vs Frequency

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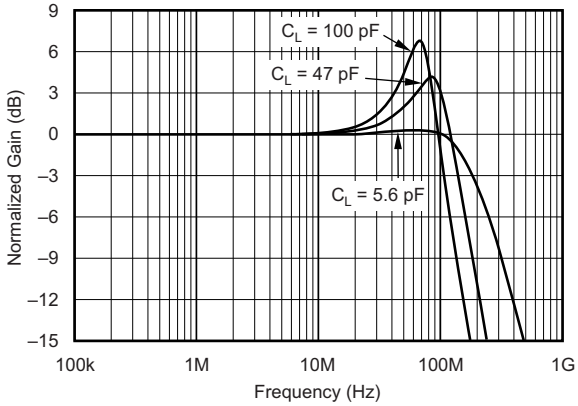
Typical Characteristics (continued)

T_A = 25°C, V_S = 5 V, G = 2, R_F = 604 Ω, and R_L = 150 Ω connected to V_S / 2, (unless otherwise noted)



C_L = 0 pF V_O = 0.1 V_{P-P}

図 13. Frequency Response for Various R_L Values



R_S = 0 V_O = 0.1 V_{P-P}

図 14. Frequency Response for Various C_L Values?

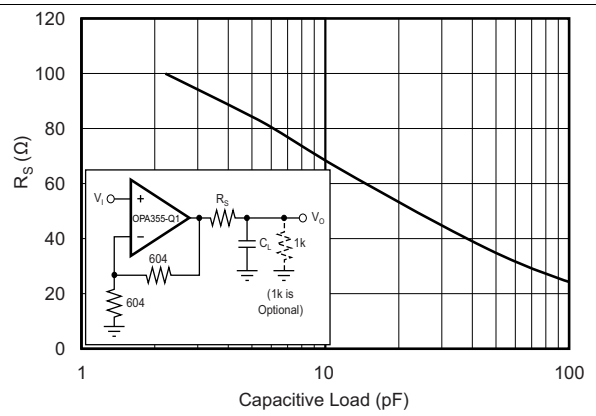


図 15. Recommended R_S Values vs Capacitive Load

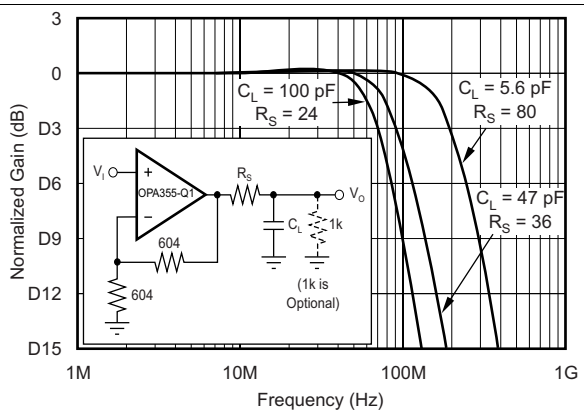


図 16. Frequency Response vs Capacitive Load

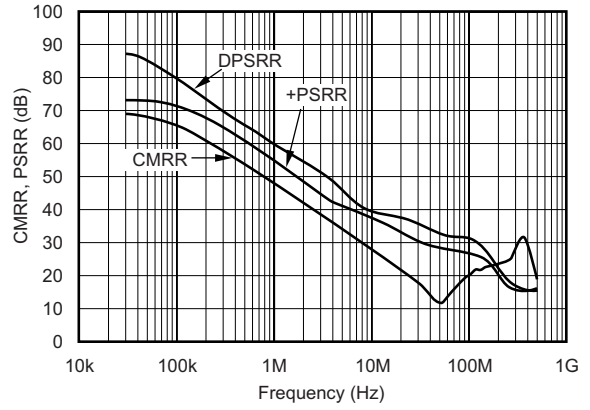


図 17. Common-Mode Rejection Ratio and Power-Supply Rejection Ratio vs Frequency

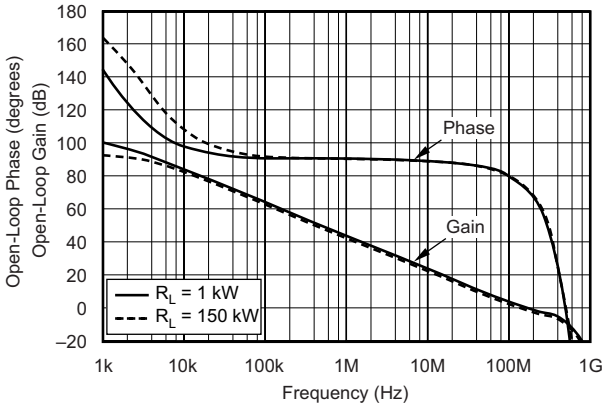


図 18. Open-Loop Gain and Phase

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Typical Characteristics (continued)

T_A = 25°C, V_S = 5 V, G = 2, R_F = 604 Ω, and R_L = 150 Ω connected to V_S / 2, (unless otherwise noted)

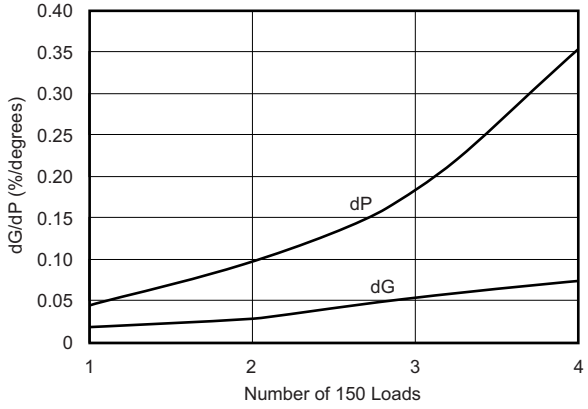


図 19. Composite Video Differential Gain and Phase

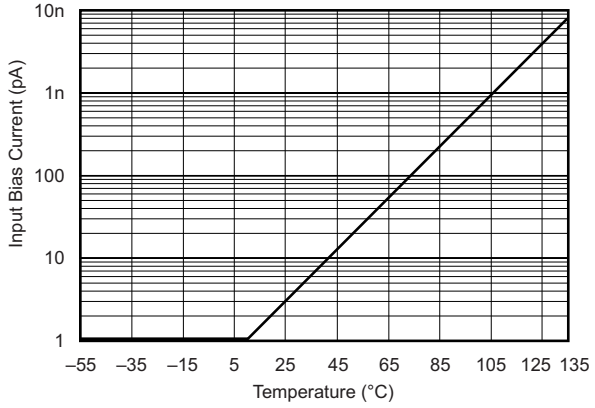
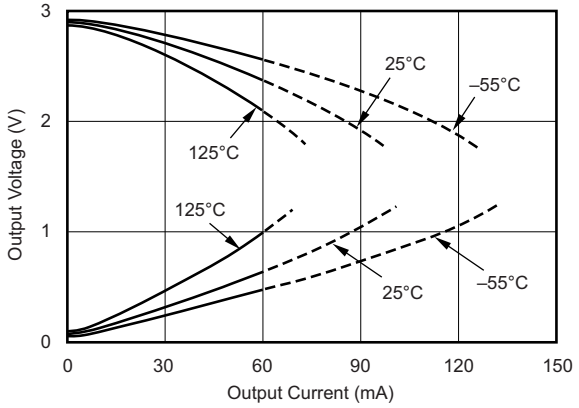


図 20. Input Bias Current vs Temperature



Continuous currents above 60 mA are not recommended

V_S = 3 V

図 21. Output Voltage Swing vs Output Current

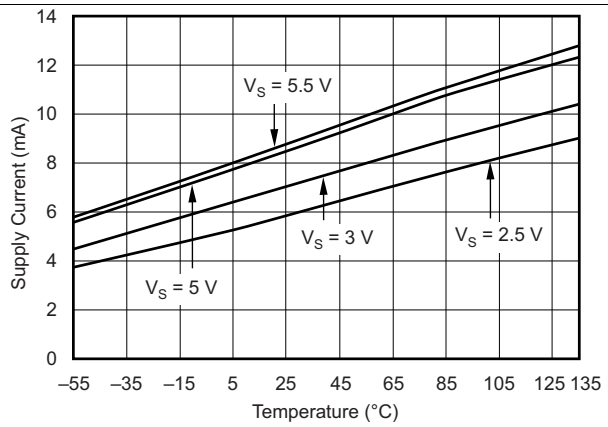
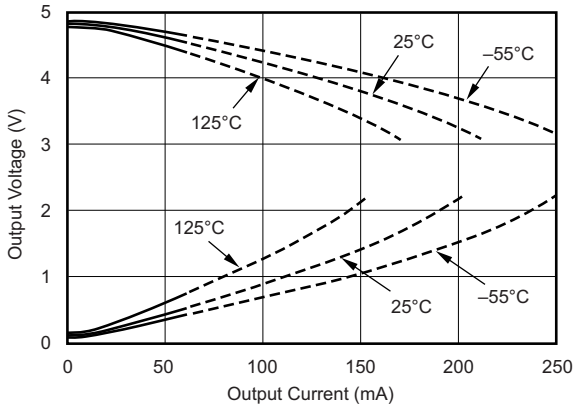


図 22. Supply Current vs Temperature



Continuous currents above 60 mA are not recommended

V_S = 5 V

図 23. Output Voltage Swing vs Output Current

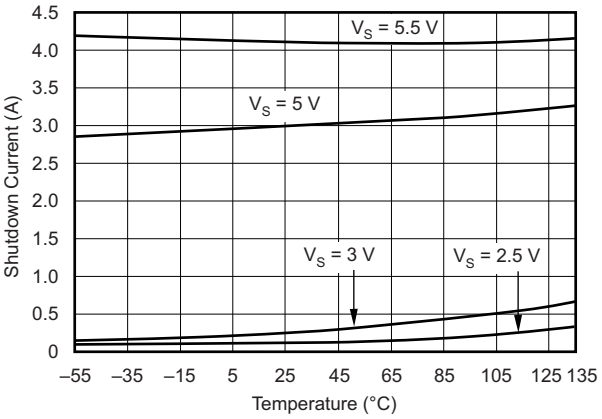


図 24. Shutdown Current vs Temperature

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Typical Characteristics (continued)

T_A = 25°C, V_S = 5 V, G = 2, R_F = 604 Ω, and R_L = 150 Ω connected to V_S / 2, (unless otherwise noted)

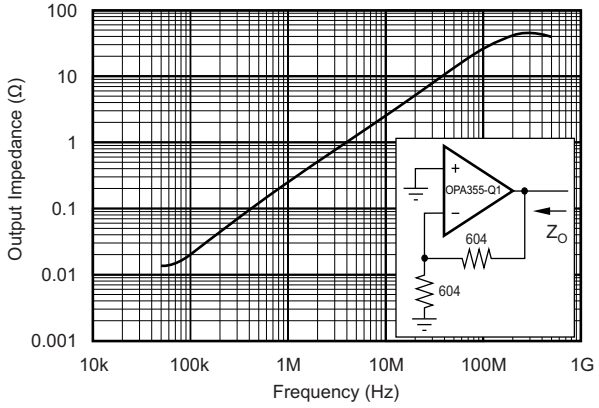
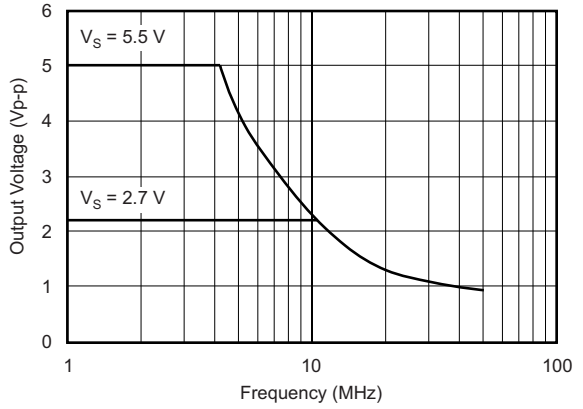
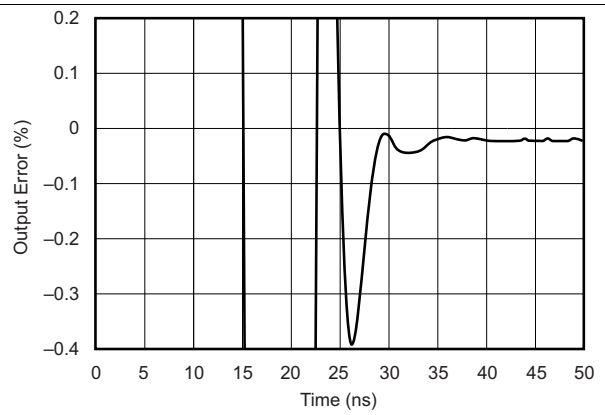


図 25. Closed-Loop Output Impedance vs Frequency



Maximum output voltage without slew-rate induced distortion

図 26. Maximum Output Voltage vs Frequency



V_O = 2 V_{P-P}

図 27. Output Settling Time to 0.1%

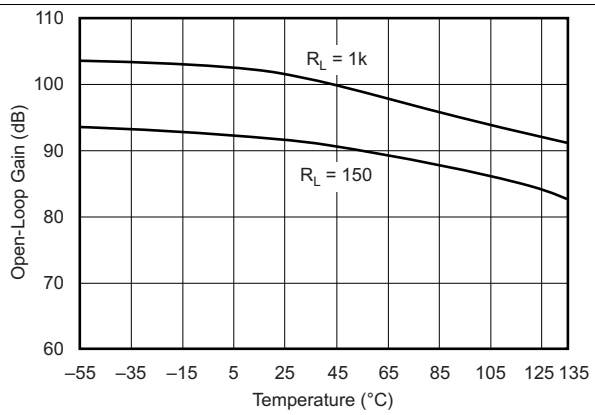


図 28. Open-Loop Gain vs Temperature

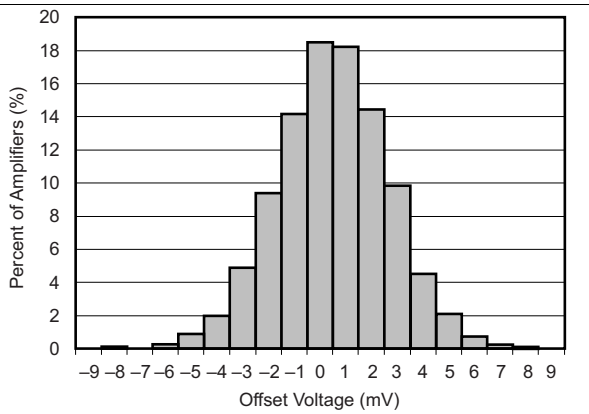


図 29. Offset Voltage Production Distribution

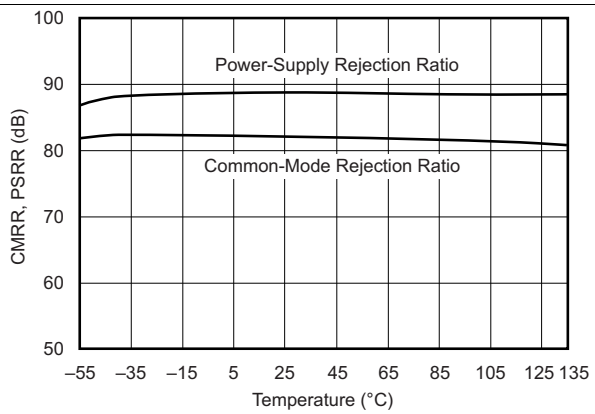


図 30. Common-Mode Rejection Ratio and Power-Supply Rejection Ratio vs Temperature

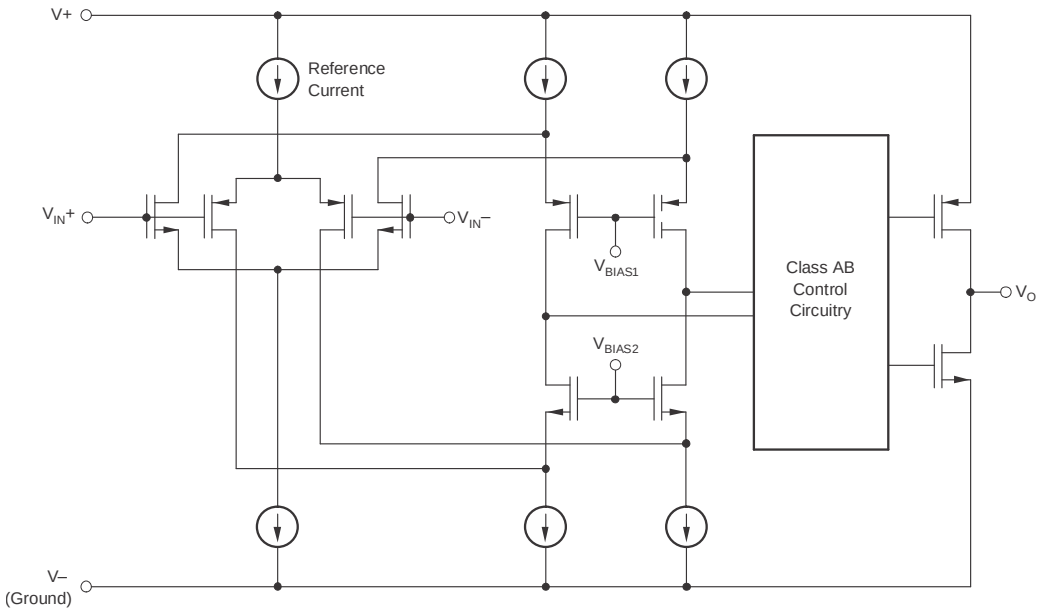
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8 Detailed Description

8.1 Overview

The OPA355-Q1 operational amplifier is a high-speed, 300-V/μs, amplifier, making the device a great option for transimpedance applications. The device is unity-gain stable and can operate on a single-supply voltage (2.7 V to 5.5 V), or a split-supply voltage (±1.35 V to ±2.75 V), making the device highly versatile and simple to use. The OPA355-Q1 amplifier is specified from 2.7 V to 5.5 V and over the automotive temperature range of –40°C to +125°C.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Operating Voltage

The OPA355-Q1 device is specified over a power-supply range of 2.7 V to 5.5 V (±1.35 to ±2.75 V). However, the supply voltage ranges from 2.5 to 5.5 V (±1.25 to ±2.75 V). Supply voltages higher than 7.5 V (absolute maximum) can permanently damage the amplifier.

Parameters that vary significantly over supply voltage or temperature are shown in the Typical Characteristics section of this data sheet.

8.3.2 Enable Function

The OPA355-Q1 device is enabled by applying a TTL high-voltage level to the enable pin. Conversely, a TTL low -voltage level disables the amplifier, which reduces the supply current from 8.3 mA to 3.4 μA per amplifier. This pin voltage is referenced to a single-supply ground. When using a split-supply, such as ±2.5 V, the enable and disable voltage levels are referenced to V–. For portable battery-operated applications, this feature is used to greatly reduce the average current and as a result, extend battery life.

The enable input is modeled as a CMOS input gate with a 100-kΩ pullup resistor to V+. The enable pin assumes a logic high and the amplifier turns on if the enable pin is left open.

The enable time is 100 ns and the disable time is 30 ns, which allows the OPA355-Q1 device to operate as a *gated* amplifier, or to have the output multiplexed onto a common output bus. When disabled, the output assumes a high-impedance state.

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Feature Description (continued)

8.3.3 Output Drive

The output stage supplies a high short-circuit current (typically over 200 mA). Therefore, an on-chip thermal shutdown circuit is provided to protect the OPA355-Q1 device from dangerously-high junction temperatures. At 160°C, the protection circuit shuts down the amplifier. Normal operation resumes when the junction temperature cools to below 140°C.

注

Running a continuous DC current in excess of ±60 mA is not recommended. See the *Output Voltage Swing vs Output Current* graphs (図 21 and 図 22) in the Typical Characteristics section.

8.4 Device Functional Modes

The OPA355-Q1 device is powered on when the supply is connected. The device can operate as a single supply operational amplifier or dual supply amplifier depending on the application. The device can also be used with asymmetrical supplies as long as the differential voltage (V– to V+) is at least 1.8 V and no greater than 5.5 V (example: V– set to –3.5 V and V+ set to 1.5 V).

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9 Application and Implementation

9.1 Application Information

The OPA355-Q1 device is a CMOS, high-speed, voltage-feedback, operational amplifier (op-amp) designed for general-purpose applications.

The amplifier features a 200-MHz gain bandwidth and 300-V/μs slew rate, but the device is unity-gain stable and operates as a 1-V/V voltage follower.

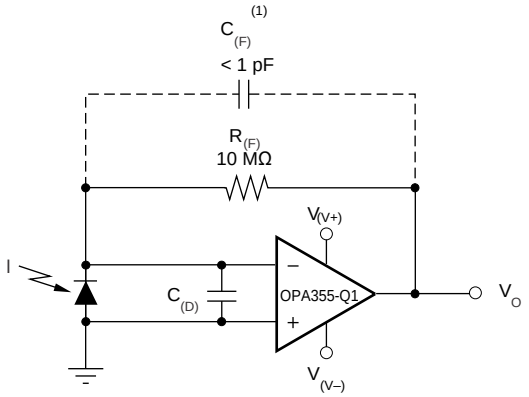
The input common-mode voltage range of the device includes ground, which allows the OPA355-Q1 to be used in virtually any single-supply application up to a supply voltage of 5.5 V.

9.2 Typical Applications

9.2.1 Transimpedance Amplifier

Wide gain bandwidth, low input bias current, low input voltage, and current noise make the OPA355-Q1 device a preferred wideband photodiode transimpedance amplifier. Low-voltage noise is important because photodiode capacitance causes the effective noise gain of the circuit to increase at high frequency.

The key elements to a transimpedance design, as shown in 図 31, are the expected diode capacitance ($C_{(D)}$), which must include the parasitic input common-mode and differential-mode input capacitance (4 pF + 5 pF), the desired transimpedance gain ($R_{(FB)}$), and the gain-bandwidth (GBW) for the OPA355-Q1 device (20 MHz). With these three variables set, the feedback capacitor value ($C_{(FB)}$) is set to control the frequency response. $C_{(FB)}$ includes the stray capacitance of $R_{(FB)}$, which is 0.2 pF for a typical surface-mount resistor.



(1) $C_{(FB)}$ is optional to prevent gain peaking. $C_{(FB)}$ includes the stray capacitance of $R_{(FB)}$.

図 31. Dual-Supply Transimpedance Amplifier

9.2.1.1 Design Requirements

PARAMETER	VALUE
Supply voltage $V_{(V+)}$	2.5 V
Supply voltage $V_{(V–)}$	–2.5 V

9.2.1.2 Detailed Design Procedure

To achieve a maximally-flat, second-order Butterworth frequency response, the feedback pole must be set to:

$$\frac{1}{2 \times \pi \times R_{(FB)} \times C_{(FB)}} = \sqrt{\frac{GBW}{4 \times \pi \times R_{(FB)} \times C_{(D)}}} \quad (1)$$

Use 式 2 to calculate the bandwidth.

$$f_{(-3\ dB)} = \sqrt{\frac{GBW}{2 \times \pi \times R_{(FB)} \times C_{(D)}}} \quad (2)$$

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For other transimpedance bandwidths, consider the high-speed CMOS OPA380 (90-MHz GBW), OPA354 (100-MHz GBW), OPA300 (180-MHz GBW), OPA355 (200-MHz GBW), or OPA656 and OPA657 (400-MHz GBW).

For single-supply applications, the +INx input can be biased with a positive DC voltage to allow the output to reach true zero when the photodiode is not exposed to any light, and respond without the added delay that results from coming out of the negative rail; this configuration is shown in 図 32. This bias voltage appears across the photodiode, providing a reverse bias for faster operation.

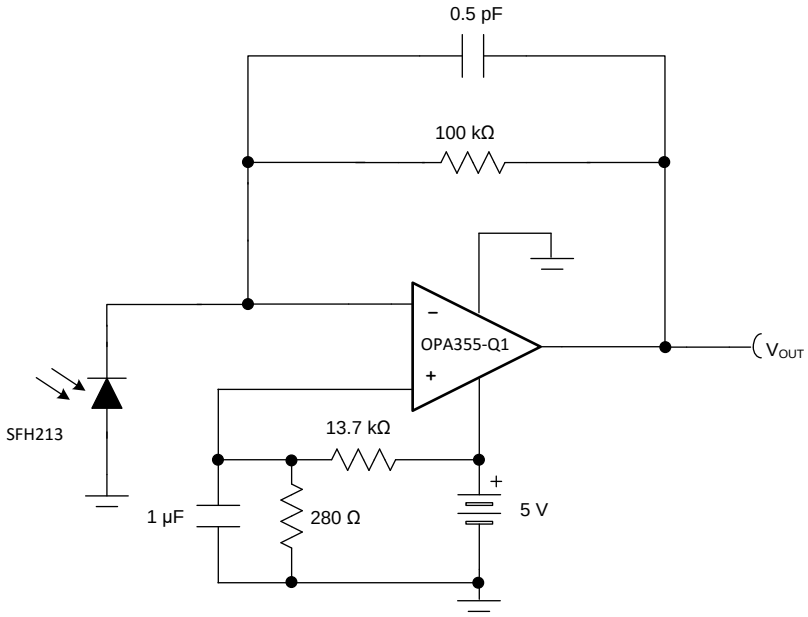


図 32. Single-Supply Transimpedance Amplifier

For additional information, see the *Compensate Transimpedance Amplifiers Intuitively* application bulletin.

9.2.1.2.1 Optimizing The Transimpedance Circuit

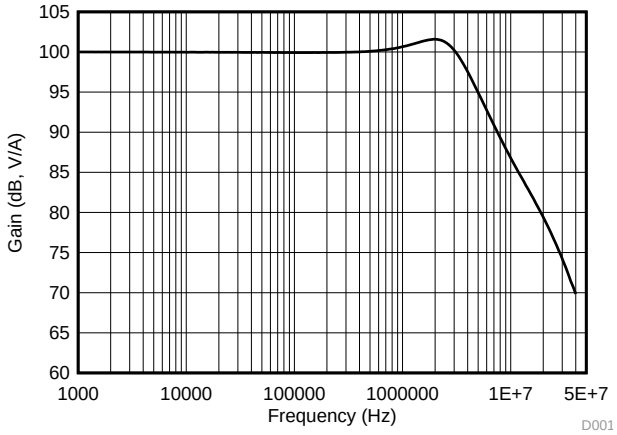
To achieve the best performance, select components according to the following guidelines:

1. For lowest noise, select $R_{(FB)}$ to create the total required gain. Using a lower value for $R_{(FB)}$ and adding gain after the transimpedance amplifier generally produces poorer noise performance. The noise produced by $R_{(FB)}$ increases with the square-root of $R_{(FB)}$, whereas the signal increases linearly. Therefore, signal-to-noise ratio improves when all the required gain is placed in the transimpedance stage.
2. Minimize photodiode capacitance and stray capacitance at the summing junction (inverting input). This capacitance causes the voltage noise of the op amp to amplify (increasing amplification at high frequency). Using a low-noise voltage source to reverse-bias a photodiode can significantly reduce the capacitance. Smaller photodiodes have lower capacitance. Use optics to concentrate light on a small photodiode.
3. Noise increases with increased bandwidth. Limit the circuit bandwidth to only that required. Use a capacitor across the $R_{(FB)}$ to limit bandwidth, even if not required for stability.
4. Circuit board leakage can degrade the performance of an otherwise well-designed amplifier. Clean the circuit board carefully. A circuit board guard trace that encircles the summing junction and is driven at the same voltage can help control leakage.

For additional information, see the *Noise Analysis of FET Transimpedance Amplifiers* and *Noise Analysis for High-Speed Op Amps* application bulletins).

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9.2.1.3 Application Curve



–3 dB bandwidth is 4.56 MHz

図 33. AC Transfer Function

9.2.2 High-Impedance Sensor Interface

Many sensors have high source impedances that may range up to 10 MΩ, or even higher. The output signal of sensors often must be amplified or otherwise conditioned by means of an amplifier. The input bias current of this amplifier can load the sensor output and cause a voltage drop across the source resistance, as shown in 図 34, where ($V_{(+INx)} = V_S – I_{(BIAS)} \times R_{(S)}$). The last term, $I_{(BIAS)} \times R_{(S)}$, shows the voltage drop across $R_{(S)}$. To prevent errors introduced to the system as a result of this voltage, an op amp with very low input bias current must be used with high impedance sensors. This low current keeps the error contribution by $I_{(BIAS)} \times R_{(S)}$ less than the input voltage noise of the amplifier, so that it does not become the dominant noise factor. The OPA355-Q1 op amp features very low input bias current (typically 200 fA), and is therefore a preferred choice for such applications.

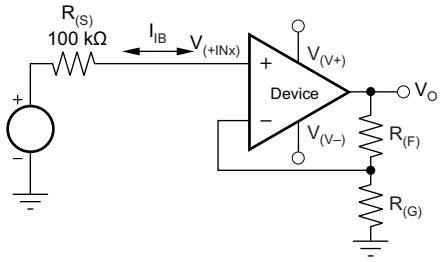


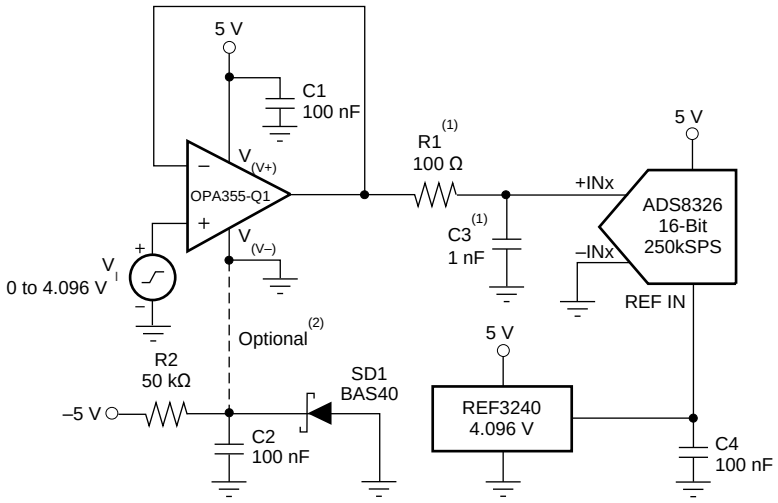
図 34. Noise as a Result of $I_{(BIAS)}$

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9.2.3 Driving ADCs

The OPA355-Q1 op amps are designed for driving sampling analog-to-digital converters (ADCs) with sampling speeds up to 1 MSPS. The zero-crossover distortion input stage topology allows the OPA355-Q1 device to drive ADCs without degradation of differential linearity and THD.

The OPA355-Q1 device can be used to buffer the ADC switched input capacitance and resulting charge injection while providing signal gain. 図 35 shows the OPA355-Q1 device configured to drive the ADS8326.



(1) Suggested value; may require adjustment based on specific application.

(2) Single-supply applications lose a small number of ADC codes near ground as a result of op amp output swing limitation. If a negative power supply is available, this simple circuit creates a –0.3-V supply to allow output swing to true ground potential.

図 35. Driving the ADS8326

9.2.4 Active Filter

The OPA355-Q1 device is designed for active filter applications that require a wide bandwidth, fast slew rate, low-noise, single-supply operational amplifier. 図 36 shows a 500 kHz, second-order, low-pass filter using the multiple-feedback (MFB) topology. The components are selected to provide a maximally-flat Butterworth response. Beyond the cutoff frequency, roll-off is –40 dB/dec. The Butterworth response is preferred for applications requiring predictable gain characteristics, such as the anti-aliasing filter used in front of an ADC.

One point to observe when considering the MFB filter is that the output is inverted, relative to the input. If this inversion is not required, or not desired, a noninverting output can be achieved through one of the following options:

1. Adding an inverting amplifier
2. Adding an additional second-order MFB stage
3. Using a noninverting filter topology, such as the Sallen-Key (see 図 37).

MFB and Sallen-Key, low-pass and high-pass filter synthesis is quickly accomplished using TI's FilterPro™ program. This software is available as a free download at www.ti.com.

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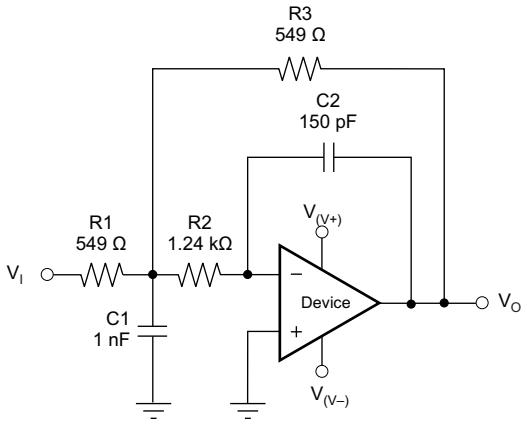


図 36. Second-Order Butterworth 500-kHz Low-Pass Filter

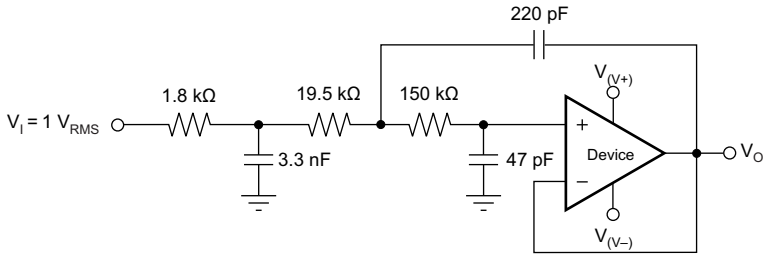


図 37. OPA355-Q1 Configured as a Three-Pole, 20-kHz, Sallen-Key Filter

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10 Power Supply Recommendations

The OPA355-Q1 device is specified for operation from 2.7 to 5.5 V (±1.35 to ±2.75 V); many specifications apply from –40°C to +125°C. Parameters that can exhibit significant variance with regard to operating voltage or temperature are shown in the *Typical Characteristics* section.

Place 0.1-μF bypass capacitors close to the power-supply pins to reduce errors coupling in from noisy or high-impedance power supplies. For more detailed information on bypass capacitor placement, see the *Layout Guidelines* section.

Power dissipation depends on power-supply voltage, signal and load conditions. With DC signals, power dissipation is equal to the product of output current times the voltage across the conducting output transistor, VS – VO. Minimize power dissipation by using the lowest possible power-supply voltage required to ensure the required output voltage swing.

For resistive loads, the maximum power dissipation occurs at a DC output voltage of one-half the power-supply voltage. Dissipation with AC signals is lower. Application bulletin AB-039, *Power Amplifier Stress and Power Handling Limitations* explains how to calculate or measure power dissipation with unusual signals and loads, and is available on www.ti.com.

Any tendency to activate the thermal protection circuit indicates excessive power dissipation or an inadequate heat sink. For reliable operation, limit junction temperature to 150°C maximum. To estimate the margin of safety in a complete design, increase the ambient temperature to trigger the thermal protection at 160°C. The thermal protection must trigger more than 35°C above the maximum expected ambient condition of the application.

11 Layout

11.1 Layout Guidelines

Good high-frequency printed-circuit board (PCB) layout techniques must be used for the OPA355-Q1. Generous use of ground planes, short direct-signal traces, and a preferred bypass capacitor located at the V+ pin ensures clean and stable operation. Large areas of copper help dissipate heat generated within the amplifier in normal operation.

Sockets are not recommended for use with any high-speed amplifier.

A 10-nF ceramic bypass capacitor is the minimum recommended value; adding a 1-μF or larger tantalum capacitor in parallel is beneficial when driving a low-resistance load. Providing adequate bypass capacitance is essential to achieving very low harmonic and intermodulation distortion.

11.2 Layout Example

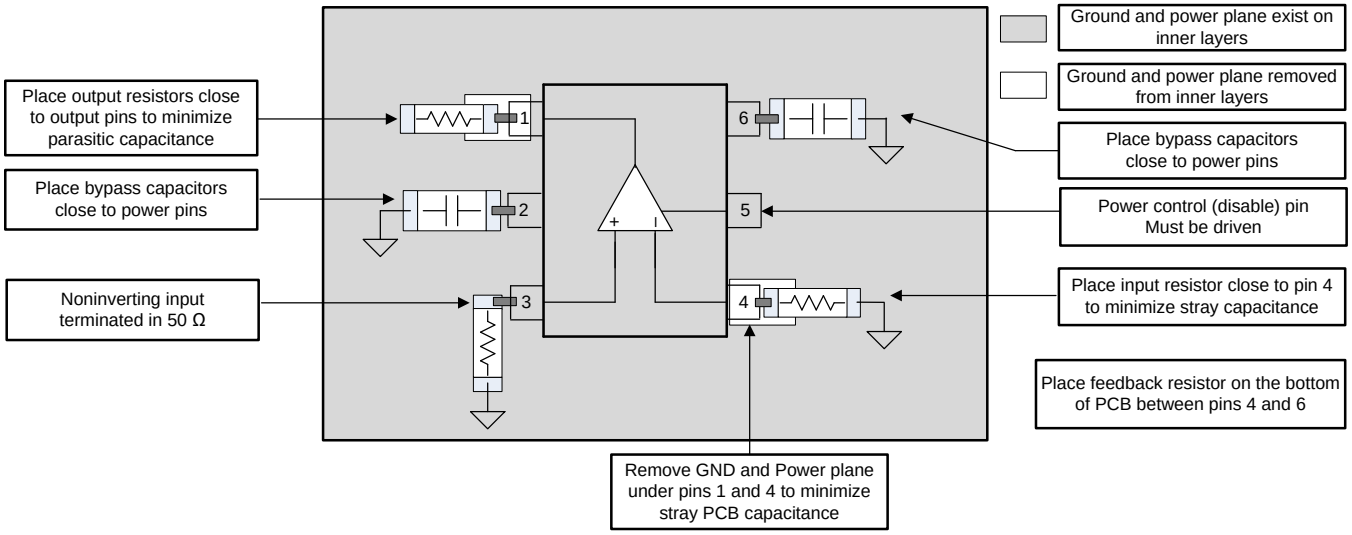


図 38. Layout Example

12 デバイスおよびドキュメントのサポート

12.1 商標

FilterPro is a trademark of Texas Instruments Incorporated.
All other trademarks are the property of their respective owners.

12.2 静電気放電に関する注意事項



これらのデバイスは、限定的なESD（静電破壊）保護機能を内 蔵しています。保存時または取り扱い時は、MOSゲートに対す る静電破壊を防止するために、リード線同士をショートさせて おくか、デバイスを導電フォームに入れる必要があります。

12.3 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。この情報は、そのデバイスについて利用可能な最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
OPA355QDBVRQ1	Active	Production	SOT-23 (DBV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	SLN
OPA355QDBVRQ1.B	Active	Production	SOT-23 (DBV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	SLN

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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OTHER QUALIFIED VERSIONS OF OPA355-Q1 :

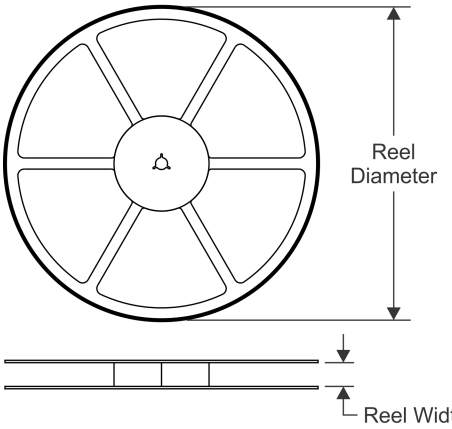
- Catalog : OPA355

NOTE: Qualified Version Definitions:

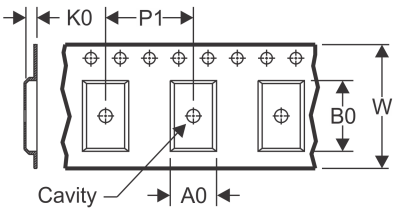
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

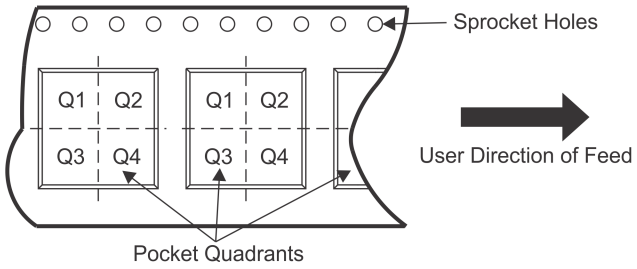


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

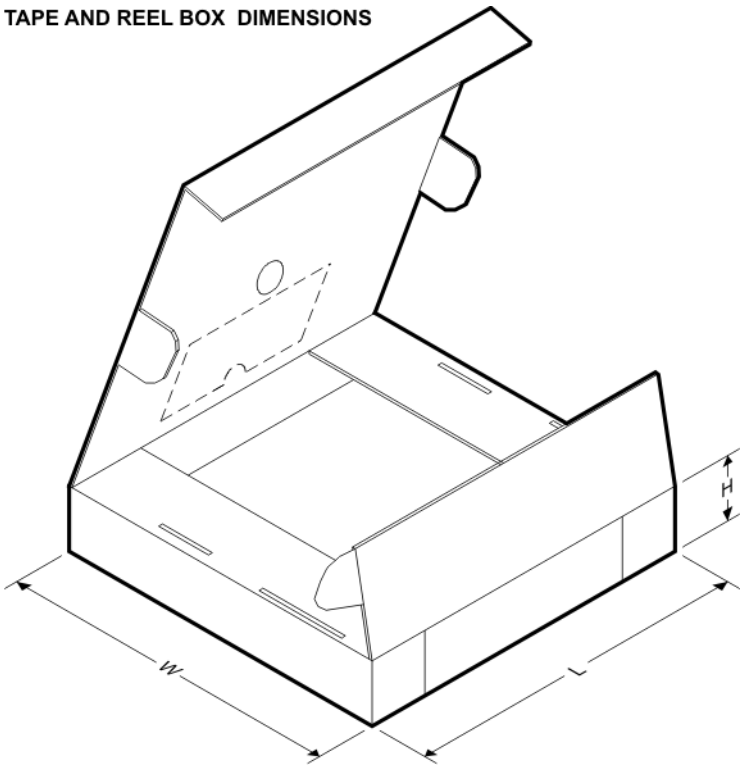
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA355QDBVRQ1	SOT-23	DBV	6	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

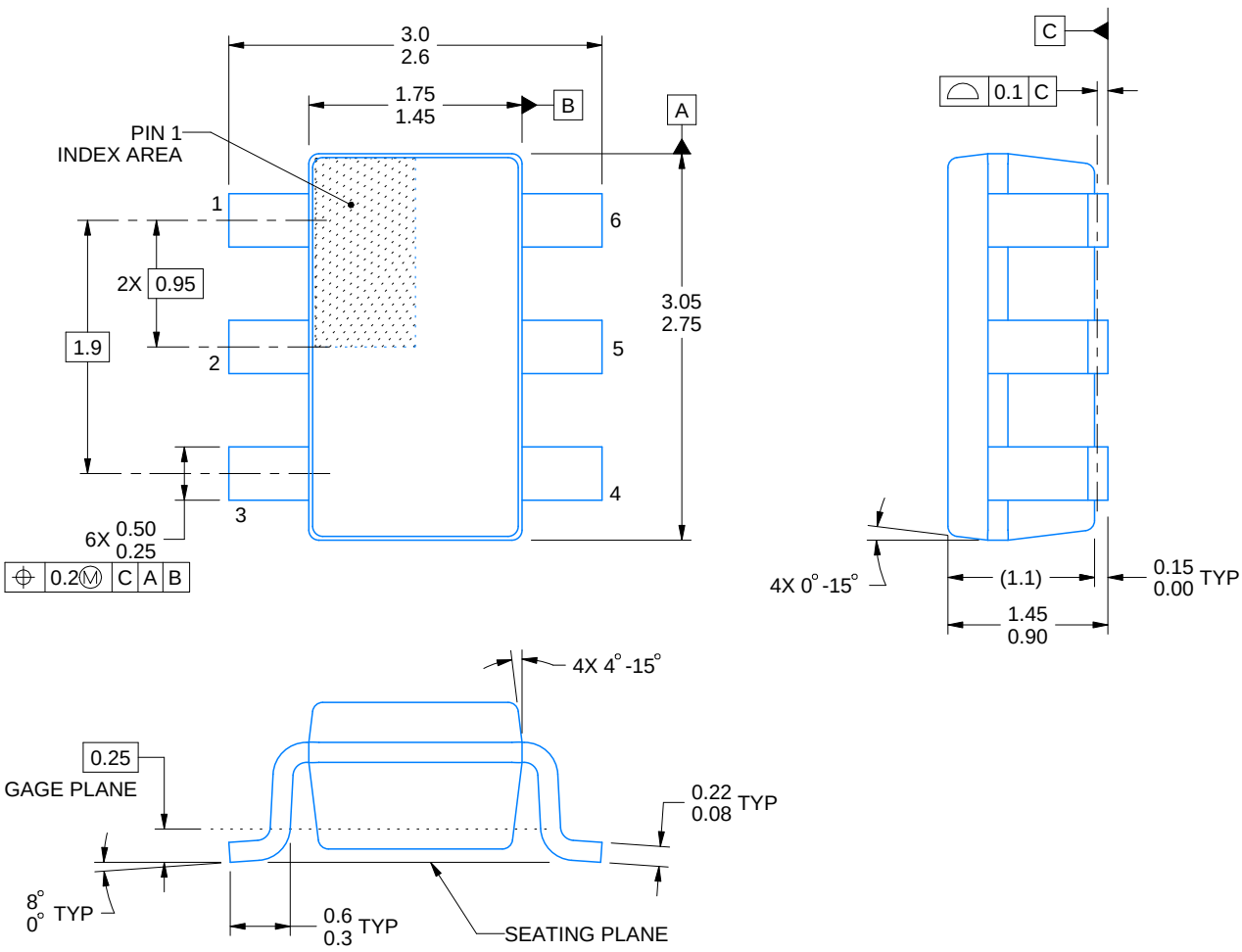
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA355QDBVRQ1	SOT-23	DBV	6	3000	445.0	220.0	345.0

PACKAGE OUTLINE

DBV0006A

SOT-23 - 1.45 mm max height

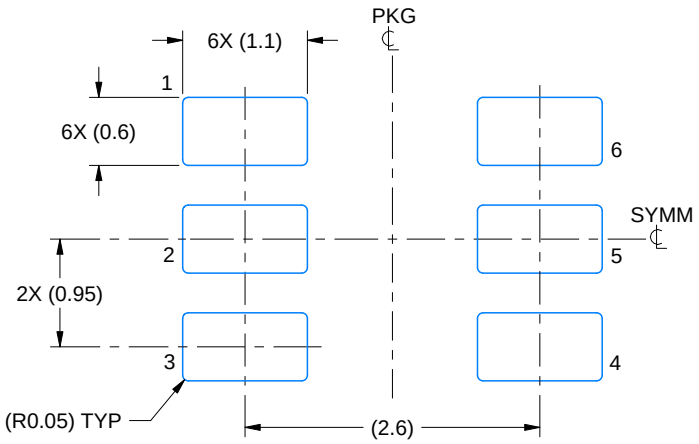
SMALL OUTLINE TRANSISTOR



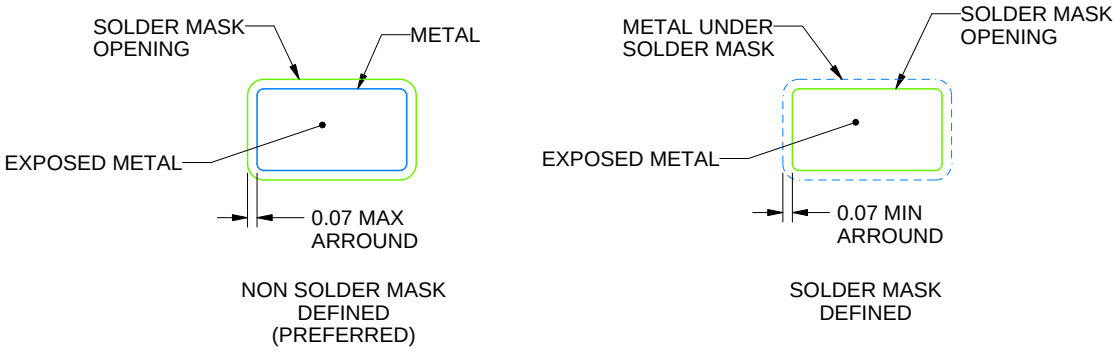
4214840/G 08/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.25 per side.
4. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
5. Refernce JEDEC MO-178.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

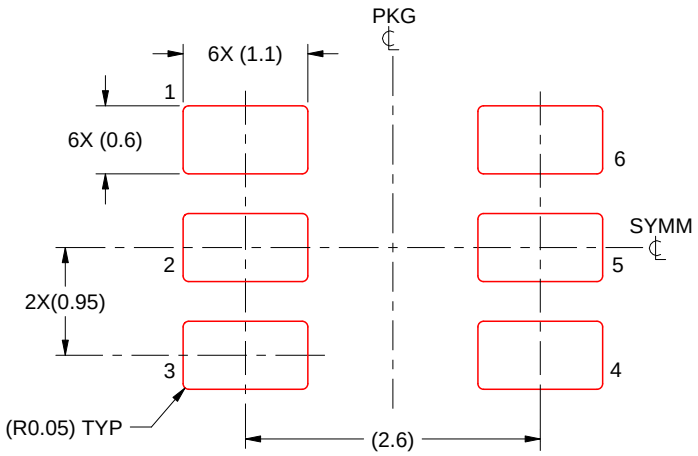


SOLDER MASK DETAILS

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NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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最終更新日：2025 年 10 月